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Regaining a Spatial Dimension: Mechanically Transferrable Two-Dimensional InAs Nanofins Grown by Selective Area Epitaxy

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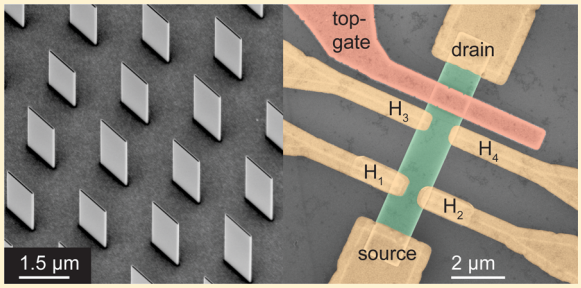
Supporting Information

ABSTRACT: We report a method for growing rectangular InAs nanofins with deterministic length, width, and height by dielectric-templated selective-area epitaxy. These freestanding nanofins can be transferred to lay flat on a separate substrate for device fabrication. A key goal was to regain a spatial dimension for device design compared to nanowires, while retaining the benefits of bottom-up epitaxial growth. The transferred nanofins were made into devices featuring multiple contacts for Hall effect and four-terminal resistance studies, as well as a global back-gate and nanoscale local top-gates for density control. Hall studies give a 3D electron density 2.5−5 × 10^{17} cm^{-3}, corresponding to an approximate surface accumulation layer density 3−6 × 10^{12} cm^{-2} that agrees well with previous studies of InAs nanowires. We obtain Hall mobilities as high as 1200 $cm^2/(V\ s)$, field-effect mobilities as high as 4400 $cm^2/(V\ s)$, and clear quantum interference structure at temperatures as high as 20 K. Our devices show excellent prospects for fabrication into more complicated devices featuring multiple ohmic contacts, local gates, and possibly other functional elements, for example, patterned superconductor contacts, that may make them attractive options for future quantum information applications.



KEYWORDS: *Nanofin, selective area epitaxy, nanowires, Hall effect*

Quantum devices were underpinned for several decades by the interfacial two-dimensional (2D) electron gas found in III−V semiconductor heterostructures.[1] A top-down approach to these systems is costly, with heterostructure complexity limited by interfacial strain issues. Bottom-up approaches have thus generated massive interest with a heavy focus on one-dimensional (1D) nanostructures, that is, nanowires, where small interfaces enable greater heterostructure versatility, including the ability to integrate III−Vs on low-cost Si substrates.[2−4] Researcher ingenuity has meant clever new devices still arise from the nanowire geometry even after two decades. That said, we suspect we are not alone in wishing for extra spatial dimensions to work with. An attractive idea would be to take the hexagonal nanowire cross-section and stretch it to obtain a 2D "nanofin" such that two side-facets have much larger area. These could be transferred to a separate substrate to make devices featuring, for example, multiple contacts and gates by conventional nanofabrication methods. This concept is impossible with vapor−liquid−solid approaches.[5,6] Here we demonstrate it is possible using selective-area epitaxy,[7,8] giving 2D InAs nanofins with precise size control, and opening a path to more interesting nanostructure shapes via appropriate mask design.[9]

Our 2D nanofins offer some interesting potential for nanoelectronics. First, they offer a new route to complex material geometries, for example, the hash-tag structures recently developed toward topological braiding of Majorana zero modes,[10] via established methods such as etching rather than exotic growth strategies. Second, the additional dimension means nanofins are better suited to making quantum devices featuring multiple contacts for Hall and/or four-terminal measurements and multiple gates for separating conduction channels or device regions. Improved contact arrangements

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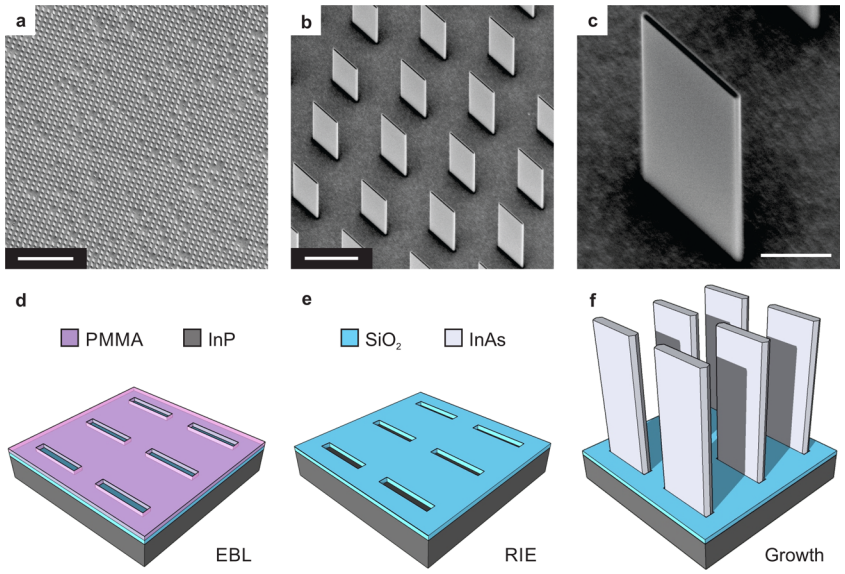

Figure 1. Templated growth of 2D nanofin structures. (a–c) Scanning electron micrographs of 2D nanofins postgrowth and prior to transfer to a device substrate: (a) wide-frame showing a large array of identical rectangular structures, (b) zoom-in of the field in (a) showing finer detail, and (c) zoom-in on a single nanofin to highlight the hexagonal structure featuring two large {110} and four smaller {110} facets on the sides and a {111}B facet at the top. The scale bars for (a–c) represent 20 μm, 1.5 μm, and 500 nm, respectively. All images at 30° tilt from perpendicular to substrate. (d–f) Schematic of key steps in the template fabrication and growth process, which involves starting with a SiO_x-coated InP(111)B substrate (blue on dark gray), spin-coating a PMMA resist (pink), (d) defining the template openings by electron-beam lithography, (e) a CHF_3 reactive ion etch to transfer the pattern to the SiO_x layer followed by resist removal, and finally (f) growth of InAs (light gray) by metal–organic vapor phase epitaxy. More complete details are given in Methods.

facilitate better understanding of materials by enabling us to measure transport mobility versus carrier density rather than resort to single-figure metrics, for example, field-effect mobility, that are used by necessity in nanowires due to contact limitations.[11] Finally, by depositing patterned superconductor films and exploiting electron density accumulation at the facet corners[12,13] at opposite edges of the nanofin, exciting new pathways to Majorana/parafermion zero-mode devices[14,15] for topological quantum computation applications may be possible.[16]

III–V nanowires were originally and are still commonly grown from a nanoparticle catalyst using a vapor–liquid–solid (VLS) approach.[5,6] More recently, self-catalyzed VLS growth has been developed.[17,18] We use an alternative approach called selective-area epitaxy (SAE) that involves using a patterned amorphous dielectric layer to template growth on a crystalline substrate.[7,8] This method, first developed for growing Si-on-Si[19] and quickly extended to GaAs[20] in the 1960s, was only widely used for III–V nanowires after work by Poole et al.[21] and Motohisa et al.[22] in 2003/2004. VLS growth remains popular due to historical momentum and because it provides the only route to stacking-fault-free nanowires.[24] However, the VLS method is limiting in the quest to extend beyond 1D structures. Under appropriate VLS growth conditions "sail-like" two-dimensional (2D) structures will grow as extensions from a 1D nanowire "mast".[25–30] In each case, these structures have significant nonuniformity in shape, dimensions, or orientation across a single growth. They also come with a nanowire "stem" and/or catalyst particle attached; the elimination of either or both would be desirable from a utopian device design perspective.

Selective-area epitaxy offers a more promising path to functional "bottom-up" 2D structures for electronic devices, giving precise and reliable deterministic control over shape, thickness, and crystal structure without the baggage of catalyst particles and nanowire stems. Conesa-Boj et al.[31] obtained V-shaped nanomembranes by molecular beam epitaxy using nanoscale apertures in a SiO_x mask. More recently, trench structures in a SiO_x mask have been used to grow long horizontally oriented InAs,[32–37] GaN,[38] GaAs,[24,37,39] and InSb[43] nanowires, along with more exotic materials.[44] These structures remain on their growth substrate for use as photonic structures,[24,38–42] electronic wires,[33–35,43] or as templates for further growth, for example, InAs nanowires atop GaAs nanomembranes.[45]

Our focus sits in a currently untapped space between the works described above—we seek the large open areas of the 2D sail-like structures from catalyst-driven VLS growth but with the precise shape control and uniformity available from selective-area epitaxy and the ability to transfer the structures to a separate substrate for device fabrication. Here we report the growth and characterization of tall, long, and thin 2D InAs nanofin structures, like those in Figure 1a–c, using dielectric-templated selective-area epitaxy. Our method produces rectangular nanofins with precise control over all three geometric dimensions. These nanofins can be mechanically transferred to a separate substrate for fabrication into devices featuring multiple contacts and electrostatic gate structures. The geometry readily enables characterization via Hall effect and devices with four-terminal contact arrangements for contact-resistance-corrected measurement. Our nanofins give electron transport mobilities up to 1200 $cm^2/(V\ s)$ at typical 3D electron density 2.5–5 × 10^{17} cm^{-3} at temperature T = 300 mK, tunable electron density via electrostatic gating and clear quantum interference structure for T < 20 K. Our work opens a path to a range of more versatile and complex quantum device structures using the bottom-up approach.

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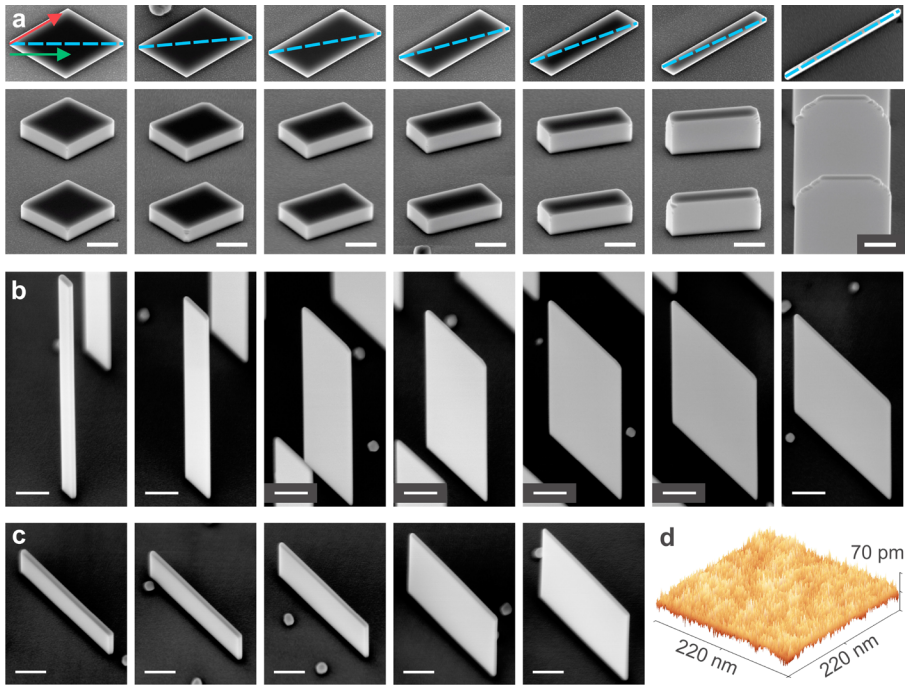

Figure 2. Exerting control over structure via template structure. (a) Overhead (top) and angled (bottom) SEM images of the growth outcome for a sequence of rectangular openings (blue dashed line) at 0°, 5°, 10°, 15°, 20°, 25°, and 30° relative to the ⟨110⟩ substrate direction (green arrow). The ⟨112⟩ direction (red arrow) is shown for reference. (b,c) Angled SEM images of growth outcome for (b) different opening lengths 300 nm (left), 500 nm, 800 nm, 1 μm, 1.3 μm, 1.5 μm, and 1.8 μm (right) and (c) different opening widths 120 (left), 110, 100, 90, and 80 nm (right). All scale bars in (a–c) represent 500 nm. (d) AFM image of a nanofin surface demonstrating the flatness of the large {110} facets. The RMS surface roughness is 80 pm.

Templated Growth of 2D Rectangular InAs Nanofins. Figure 1a–c shows scanning electron micrographs of typical growth results. Figure 1a demonstrates 2D structures can be grown in large arrays with high yield (>80%) and good shape uniformity. Figure 1b,c shows sequential zoom-ins of the nanofins, which have typical length of ∼1 μm, width of ∼80 nm, and height of ∼4 μm (see Supplementary Figure S1a/b). The structure is essentially a nanowire stretched along one symmetry axis, featuring two large {110} face-facets and four smaller {110} edge-facets (see Figure 1c and Figure S1b). The top-facet is {111}B matching the substrate. The structure maintains the shape imposed by the mask during growth for reasons similar to those governing SAE growth of nanowires;[22] the {111}B surface has a high growth rate whereas the {110} surfaces provide poor nucleation suppressing lateral growth.[23] Figure 1d–f highlights key steps in the template fabrication and growth process, which begins with a InP(111)B wafer (dark gray). This substrate was cleaned and 25 nm SiO_x (blue) was deposited by plasma-enhanced chemical vapor deposition. Dielectric-template patterning was performed via a mask transfer process using poly(methyl methacrylate) (PMMA) electron-beam lithography (EBL) resist (pink). The mask pattern was written with a 20 kV electron beam using a Raith-150 EBL system and developed in 1:3 methylisobutylketone/2-propanol to expose the SiO_x surface in regions where growth should occur (Figure 1d). This pattern was then transferred to the SiO_x by CHF_3 reactive-ion etching (RIE) to reveal the InP surface at locations where the SiO_x was exposed. The PMMA was then removed leaving the patterned SiO_x template (Figure 1e). All template holes have their long axis aligned with the InP(111)B substrate ⟨112⟩ direction unless otherwise specified. The final stage was growth of InAs (light gray) by metal–organic vapor phase epitaxy (MOVPE) with nucleation and epitaxial growth occurring at the exposed InP surfaces, giving structures shaped by the SiO_x template (Figure 1f). Further process details are given in Methods.

Figure 2a–c demonstrates three aspects of the template that affect the structures grown. First, the shape is reliant on the rectangular opening's long-axis orientation relative to the underlying InP(111)B substrate's crystallographic axes. The two key surface directions in Figure 2a are ⟨110⟩ (green arrow) and ⟨112⟩ (red arrow). The mask opening orientation is indicated by the blue dashed line in Figure 2a and is rotated in 5° steps from ⟨110⟩ (far left) to ⟨112⟩ (far right). All structures grown have six {110} side-facets and a {111}B top-facet demonstrating a strong preference to {110} facet formation, as found for SAE-grown InAs nanowires.[22,46] For the ⟨110⟩-aligned opening, two of the {110} facets are very small while the remaining four have equal size, giving a rhomboid appearance. As the opening is rotated, two of the four large {110} facets grow while the other two shrink. Once the opening aligns with ⟨112⟩, the structure consists of two large face-facets and four small edge-facets with equal size, giving the 2D nanofins we focus on for the remainder of this work. Figure 2b,c shows the effect of changing opening length l (long axis) and width w (short axis) for ⟨112⟩-aligned openings. The series in Figure 2b clearly demonstrates nanofins are a natural evolution of nanowires, which would be obtained for $l = w$[22,46] into the regime where $l \gg w$. Figure 2c points to our tall freestanding nanofins being an extension of the horizontal SAE-grown nanowires[33,34] taken into the limit of small w and long growth time. The small w involved makes our 2D nanofins challenging to grow; proper nucleation and growth require the opening floor to be very clean and w

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needs to be constant along the opening length, both become tougher prospects as w is reduced. Examples of growth when the mask is not well optimized are shown in Supplementary Figure S2. Even when satisfactory growth occurs, mask opening width variations at the few nanometers level can significantly affect aspect ratio and surface area, dominating over more typical control parameters, for example, temperature and V/III ratio. This occurs because this approach requires mask opening widths (20−30 nm) at the limit of conventional EBL, and the growth physics for free-standing III−V nanofins/membranes is complex and currently only well characterized for GaAs.[23] The observed variability in an array of nominally identical openings is addressed in Supplementary Figure S3.

The nanofin height decreases as the opening's long-axis is rotated away from ⟨112⟩ or l or w is increased, consistent with surface-diffusion controlled growth. Dimensions for the images in Figure 2a−c are given in Supplementary Figure S4. Predicting the final grown height is challenging because one also needs to consider the mask opening spacing and growth conditions, for example, temperature and V/III ratio. The spacing dependence is itself nontrivial compared to, for example, honeycomb arrays of nanowires with hexagonal cross-section, where the spacing is single-valued. Here structural and array symmetries are both broken meaning at least four parameters are required: width, length, and separations in the width and length directions. We can however make some general observations. First, comparable capture area leads to comparable added volume with larger mask opening area giving reduced height under fixed growth conditions and time. The relationship is slightly nonlinear though because of adatom capture onto the growing structure occurring in addition to adatom capture onto the dielectric mask. Second, because these structures are strongly affected by surface diffusion on the mask and in the openings, placing nanofins in close proximity will eventually reduce the axial growth rate due to competition for In adatoms.

Turning to structural aspects, the nanofin oriented along ⟨112⟩ (rightmost in Figure 2a) shows a highly stepped top-facet unlike other nanofins in Figures 1 and 2b,c and was grown at lower temperature and V/III ratio. The stepped top-facet arises from a kinetic limitation to the axial growth rate that depends on both the top surface area and the growth conditions, as evident in Supplementary Figure S5. The likelihood of top-facet stepping increases with {111} top-facet surface area under fixed growth conditions. At fixed top-facet surface area, the incidence of top-facet stepping decreases for conditions favoring enhanced axial growth rate, namely higher temperature and higher V/III ratio. The 2D nanofins show wurtzite-zincblende polytypism, as found for InAs nanowires (for HRTEM data see Supplementary Figure S6).[47] Nonetheless, the large {110} side-facets have high flatness, as shown previously on SAE-grown InAs nanowires by STM.[48] Figure 2d shows an AFM micrograph of the large {110} side-facet, and the RMS surface roughness is ∼80 pm compared to 295 pm for the underlying SiO_2 device substrate surface.

Mechanical Transfer of Nanofins and Device Fabrication. A key motivation was to obtain 2D structures for transfer to a separate substrate for fabrication into devices with multiple gates and contacts. We previously used dry-transfer via a small triangle of lab-wipe for nanowire devices.[49] This works acceptably but is brutal and costly; the large tip rapidly decimates a field like that in Figure 1a, which requires a very long EBL session for writing the growth template. Nanoimprint lithography might help alleviate this cost issue.[50] Wet deposition involving ultrasonication into solvent is also expensive because large arrays are needed to obtain feasible liquid volume with suitable nanofin concentration. Instead we perform deposition using a micromanipulator mounted on a high-resolution optical microscope.[10,26] This enables transfer of single nanofins with a positional accuracy of order 10 μm, high yield (∼80%) and minimal growth field decimation. The ease of detaching a nanofin improves with increased height and/or decreased base length. With care, good technique, and patience, nanofins can mostly be cleaved cleanly at the base, enabling the entire nanofin to be transferred.

Device fabrication thereafter proceeds by conventional methods. The device substrate was a n^+-Si wafer with a 100/10 nm thick SiO_2/HfO_2 insulator and prepatterned Ti/Au interconnect and alignment structures. The n^+-Si substrate was used as a back-gate for all devices. The substrate was cleaned and nanofins were transferred mechanically using a micromanipulator to give a few transferred nanofins per 100 × 100 μm active device field on the substrate. The transferred nanofins adhere strongly by van der Waals forces. We spin-coat PMMA resist prior to defining source and drain leads and Hall probes using EBL. Contacts were passivated with $(NH_4)_2S_x$ solution prior to thermal evaporation of approximately 10/150 nm Ni/Au and lift-off to give the completed device in Figure 3a,b (Device 1). Top-gate structures can be added thereafter. This was achieved with a further two rounds of EBL. First we pattern a gate-insulator, which is approximately 12−20 nm of HfO_2 or Al_2O_3 by atomic-layer deposition (ALD), followed by lift-off. Then we pattern gates, which are approximately

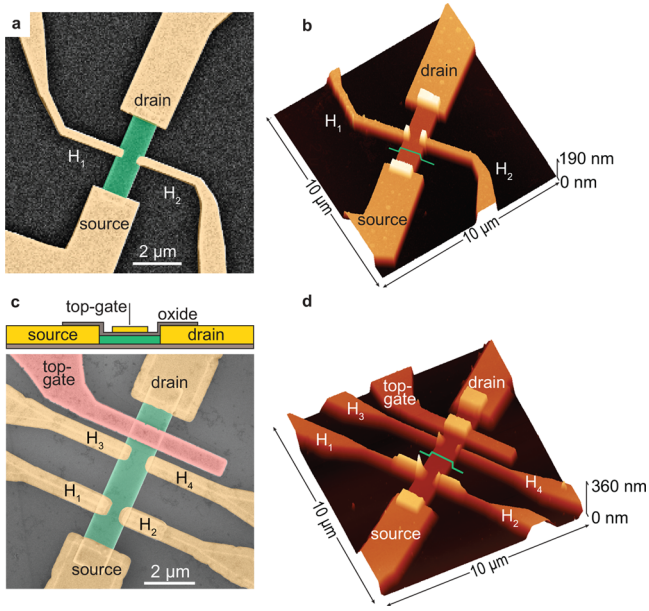

Figure 3. Fabrication of nanofin devices for Hall effect and local gating studies. (a) False-color SEM and (b) AFM image of a device for Hall effect studies (Device 1) featuring a nanofin (green), source, drain, and a pair of Hall contacts H_1 and H_2 (yellow). (c) Schematic and false-color SEM and (d) AFM image of a patterned top-gate device (Device 2) featuring nanofin (green), set of six contacts contacts (yellow), and a HfO_2 insulated top-gate (red). The scale bars in (a,c) represent 2 μm. The green dotted lines in (b,d) indicate the locations of an AFM line-scan revealing nanofin thicknesses of 74 and 85 nm for the two devices, made from separate growths (see Supplementary Figure S7).

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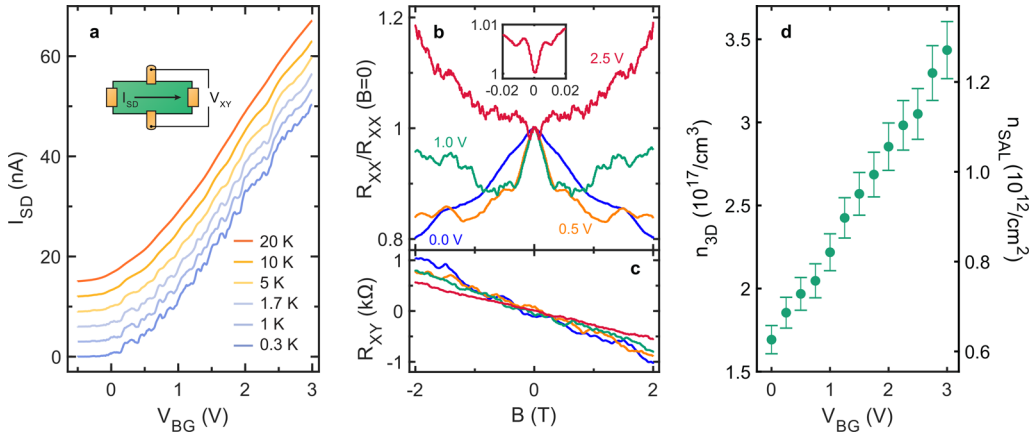

Figure 4. Electrical characterization of nanofin Hall device. (a) Source-drain current I_{SD} versus back-gate voltage V_{BG} as a function of temperature T obtained for the "normal" configuration. The "rotated" configuration data appears in Supplementary Figures S8 and S9 as discussed in the text. Consecutive traces are offset upward by 3 nA as T is increased for clarity (lowest T trace has zero offset). (b) Zero-field-scaled longitudinal resistance R_{XX}/R_{XX} (B = 0) and (c) Hall resistance R_{XY} versus magnetic field B at four different back-gate voltages V_{BG} = 0 V (blue), +0.5 V (orange), +1 V (green), and +2.5 V (red) obtained at T = 300 mK. Inset: Focus on low B for the V_{BG} = +2.5 V data to highlight the R_{XX}/R_{XX} (B = 0) minima at B = 0 (see Supplementary Figure S10 for all traces over this B-range). (d) Measured 3D electron density n_{3D} (left axis) and corresponding approximate surface accumulation layer density n_{SAL} (right axis) versus V_{BG} obtained from Hall effect data. All data were obtained from Device 1 in the normal orientation.

10/135 nm Ti/Au by vacuum thermal evaporation, followed by lift-off. This gives the completed device in Figure 3c,d (Device 2). Full details are in the Methods section with specific values for each device tabulated in Supplementary Table 1.

Electrical Characterization of Hall-Configuration Nanofin Device. We began by studying nanofin structures featuring a pair of Hall contacts and a back-gate (Device 1) as shown in Figure 3a,b. The nanofin forms a channel 1 μm wide and 3.5 μm long with the two Hall probes on opposing sides approximately halfway along the nanofin. Electrical measurements were performed in an Oxford Instruments Heliox VT ^{3}He cryostat with a 2 T superconducting magnet using standard ac lock-in techniques. Before discussing the data, we preemptively highlight some aspects of our conduction channel that are important to understanding these devices. A well-known feature of InAs is the tendency for surface states to pin the surface Fermi energy at the conduction band edge, giving a surface accumulation layer (SAL) with high electron density.[51] Electronic structure calculations for nanowires point to the SALs for the six {110} facets joining to form a hexagonal-cylinder geometry with slightly higher electron density at the corners between adjacent facets.[12,13] However, several experiments indicate conduction is not solely via this SAL with significant transport via the nanowire core,[52−54] where free carrier density is likely only an order of magnitude smaller at most.[12] Thus, a sensible expectation is for an inhomogeneous 3D electron distribution featuring slightly higher density SALs, potentially with poor mobility due to surface proximity, and a lower density core with higher mobility due to screening by the SALs. This explains why, in what follows, we a priori treat our measurements from a 3D perspective.

Figure 4a shows the source-drain current I_{SD} in response to source-drain voltage V_{SD} = 500 μV versus back-gate voltage V_{BG} between T = 280 mK and 20 K. For completeness, we obtained data for both possible Hall configurations. Data for the "normal" orientation is presented in Figure 4. Data for the "rotated" orientation where V_{SD} is applied and I_{SD} passed via H_1 and H_2 is presented in Supplementary Figures S8 and S9 to provide additional insight into the transport. Starting with Figure 4a, negative/positive V_{BG} leads to reduced/increased I_{SD} (depletion/enhancement) consistent with electrons as the majority carrier. The device has relatively low conductivity at V_{BG} = 0 V but this is not unexpected at low temperatures. A positive shift in gate threshold upon cooling and ultimately a positive threshold voltage at low temperature, is commonly seen in past studies of InAs nanowires.[33,55,56] The low temperature data in Figure 4a shows reproducible quantum interference fluctuations that reduce in amplitude with increasing temperature, consistent with observations in both 1D InAs nanowires[57,58] and 2D open quantum dots in GaAs.[59] The fluctuations remain visible up to $T \sim$ 10 K, indicating long electron phase coherence length and are stronger for the rotated orientation due to the reduced contact separation (see Figure S8).

Figure 4b,c shows the zero-field-scaled longitudinal magnetoresistance R_{XX}/R_{XX} (B = 0) where $R_{XX} = V_{SD}/I_{SD}$ and Hall resistance $R_{XY} = V_H/I_{SD}$ versus magnetic field B for four different V_+ values. Corresponding data for the rotated orientation appears in Supplementary Figure S9. The R_{XX}/R_{XX} (B = 0) traces show structure reminiscent of open quantum dots[60] with a central magnetoresistance peak surrounded by symmetric, reproducible quantum interference fluctuations. These fluctuations also appear in the R_{XY} data. The fluctuations are suppressed with increasing T, and to the field range available, show no structures indicative of Shubnikov−de Haas oscillations (Figure 4b) or quantum Hall effect (Figure 4c), as might be expected for a large-area planar 2DEG in InAs (see also Figure S9).[61] This is not surprising given the nanofin dimensions (1 × 3.5 μm) are closer to those of an open quantum dot (~1 × 1 μm)[60] than a conventional AlGaAs/GaAs Hall bar (~0.4 × 1 mm).[62] Shubnikov−de Haas oscillations and quantum Hall plateaus were not observed in separate studies at magnetic fields up to 6 T at T = 4 K either. This may simply be due to insufficient classical and quantum scattering lifetimes in our nanofins.[63] The lack of quantum Hall plateaus might also point to the conduction channel being insufficiently 2D[64] due to conduction via the nanofin core. The peak at B = 0 in Figure

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4b is commonly observed in InAs nanowires and often attributed to weak localization.[65] Our peak is gradually suppressed with more positive V_{BG} with R_{XX} evolving a sharper central minima for V_{BG} > +1.0 V. The sharp central minima obtained for V_{BG} = +2.5 V appears inset to Figure 4b with a more complete series in Supplementary Figure S10. We tentatively attribute this minima to weak antilocalization (WAL).[66] However, the superimposed quantum interference structure makes a definitive attribution of B = 0 maxima/minima to weak localization or antilocalization challenging, as was the case for open quantum dots.[60,67] If we assume the R_{xx} minima are gate-dependent WAL features and fit using the model by Iordanskii et al.,[68] we obtain phase-coherence lengths L_ϕ of 200−600 nm and spin-relaxation lengths L_{SO} as low as 150 nm. These values are comparable to those found for InAs nanowires.[65,69,70] Indicative fits and plots of L_ϕ and L_{SO} versus V_{BG} are presented in Supplementary Figure S10. A detailed study of localization/scattering in our nanofins will be the subject of a separate paper.

A notable aspect of our nanofins is the comparative ease in obtaining Hall measurements. This is difficult for nanowires due to the small contact gaps involved and the overhang generated by the hexagonal geometry.[11,71] Although the measurements are easier, the interpretation needs some care. As mentioned earlier, experiments point to conduction throughout the structure,[52−54] motivating us to start with a 3D treatment. In Figure 4d, we plot the 3D electron density n_{3D} (left axis) versus V_{BG} using the measured nanofin thickness t = 74 nm. Although conduction occurs through the entire structure, there is no avoiding that the electron density is higher closer to the nanofin surface, likely by over an order of magnitude.[12] For our geometry, the Hall voltage is dominated by two of the six side-facets. Thus, we suggest the approximation $n_{SAL} \approx (n_{3D}t)/2$, where n_{SAL} is the surface accumulation layer density. We provide this as the right-hand axis for Figure 4d accordingly. However, some words of caution are warranted. The n_{SAL} estimate automatically implies the top and bottom SALs have equal density, since we cannot measure them independently because they are shorted by the nanofin edge, that is, the four SALs at the four small edge-facets. First, changing V_{BG} will necessarily shift charge between the top and bottom SALs so that $n_{SAL}^{top} = n_{SAL}^{bottom}$ only holds at one V_{BG}. Second, the V_{BG} where $n_{SAL}^{top} = n_{SAL}^{bottom}$ can vary substantially from zero due to surface chemistry affecting surface-state density.[12,72] For Device 1, both surfaces are chemically pristine, contacts aside and ignoring organic residues from lithography. But for our gated devices (Device 2), the addition of a gate-oxide by atomic layer deposition on the top nanofin surface likely means n_{SAL}^{top} differs substantially from n_{SAL}^{bottom} at V_{BG} = 0. Thus, our n_{SAL} is an average of the top and bottom SALs, and at best an order of magnitude estimate. Nonetheless, it is useful for comparison against earlier studies. In Figure 4d, we obtain n_{SAL} values between 0.6×10^{12} and 1.3×10^{12} cm^{-2} for Device 1. This agrees well with the values ranging from 0.45×10^{12} cm^{-2} to 1.3×10^{12} cm^{-2} obtained by Blömers et al.[11] for Hall measurements of InAs nanowires grown by molecular-beam epitaxy. Our values also agree to order of magnitude with capacitance−voltage measurements of InAs nanowire arrays[73] and InAs wafer surfaces.[51] We observe a linear decrease in n_{3D} with increasingly negative V_{BG} due to electron depletion.

Electrical Characterization of Strip-Line-Gated Nanofin Hall-bar Device. Device 2 features six ohmic contacts in a Hall bar arrangement, a global back-gate, and a 650 nm wide HfO_2-insulated top-gate between Hall probes 3 and 4 and the drain contact, as shown in Figure 3c,d. The contact set enables full four-terminal measurement capability for obtaining the longitudinal R_{XX} and Hall R_{XY} resistances independent of contact contributions.[74,75] This is often difficult for nanowires because the contacts cross the entire conduction path causing scattering.[57,76] The strip-line gate is adjacent to the drain to avoid gate metallization from affecting four-terminal transport mobility measurements; if the gate was across the middle, it would be present in the voltage path for R_{XX} but not R_{XY}. We begin in Figure 5a by testing independent action of the top-gate (red) and back-gate (blue). In each case the other gate is grounded. The back-gate achieves full depletion (G_{SD} = 0) at V_{BG} = −4 V whereas the top-gate only achieves partial depletion with $G_{SD} \sim 25$ μS for V_{TG} beyond −3.3 V. Notably, both traces have similar slope despite the back-gate insulator being considerably thicker (100/10 nm SiO_2/HfO_2 for back-gate versus 12 nm HfO_2 for front-gate). If both gates are biased simultaneously (orange trace in Figure 5a), full depletion is achieved at much lower bias, as expected.

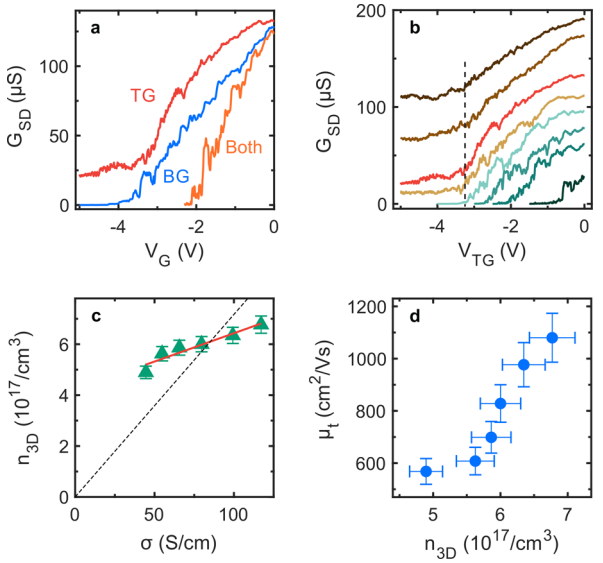

Figure 5. Electrical characterization of dual-gated nanofin device. (a) Source-drain conductance $G_{SD} = I_{SD}/V_{SD}$ versus gate voltage V_G for the back-gate with top-gate grounded (blue), top-gate with back-gate grounded (red), and both gates biased together (orange). (b) G_{SD} versus top-gate voltage V_{TG} at fixed back-gate voltage V_{BG} obtained at V_{BG} = +2 V (brown, top trace), +1, 0 V (red), −0.5, −1, −1.5, −2, and −3 V (green, bottom trace). The dashed line in (b) is a guide to the eye. (c) Three-dimensional electron density n_{3D} obtained at different V_{BG} versus conductivity σ with a linear fit (orange line) and a fit forced through σ = 0, n_{3D} = 0 as per Blömers et al. (black dashed line).[11] (d) Plot of transport mobility μ_t versus n_{3D} calculated on a single-point basis (see text). All data obtained from Device 2 at T = 0.3 K.

We investigate the gating action further in Figure 5b, where we plot G_{SD} versus V_{TG} at various fixed V_{BG}. The data from Figure 5a at V_{BG} = 0 V appears in red. Corresponding data for G_{SD} versus V_{BG} at various fixed V_{TG} is shown in Supplementary Figure S11. The failure of top-gating action always occurs at the same V_{TG} at more positive V_{BG}, as highlighted by the vertical dashed line in Figure 5b. To rule out a gate discontinuity, we put a probe needle at the far end and

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measured a gate strip resistance of <100 ohms. Looking to the left of the dashed line in Figure 5b, the conductance where the top-gate ceases depleting is clearly influenced by the back-gate. This indicates that the part of the conduction channel that cannot be fully depleted by the top-gate clearly can be gated from the opposite side. Interestingly, the top-gate achieves no further depletion out to $V_{TG} < -7$ V at $V_{BG} = -0.7$ V and -0.8 V, but achieves pinch-off at $V_{TG} \sim -4$ V at $V_{BG} = -1.0$ V (see Supplementary Figure S12). This suggests the loss of depletion is strong and onsets sharply. We see similar behavior, that is, failure to achieve pinch-off in a separate device (Device 3, see Figure S15) with 20 nm Al_2O_3 gate insulator, pointing to this being a consistent behavior in nanofin devices. One possible explanation is screening by a high free electron density in the nanofin. To examine this, we modeled our device in COMSOL Multiphysics with results presented in Supplementary Figures S13 and S14. In the model, we can set the free electron density n throughout the nanofin at zero gate bias ($V_{BG} = V_{TG} = 0$). We present data for two densities: $n = 5 \times 10^{16}$ cm^{-3} and 2×10^{17} cm^{-3} corresponding to typical measured n_{3D} for our devices. At $n = 5 \times 10^{16}$ cm^{-3} we see the back-gate head toward pinch-off, whereas the top-gate, which starts with a steeper transconductance dI/dV_g, quickly saturates at finite I_{SD} (see Figure S14a). This behavior exacerbates at $n = 2 \times 10^{17}$ cm^{-3} with both the top- and back-gates saturating at finite I_{SD} (see Figure S14b). We see this behavior in a separate device featuring only a pair of contacts and global top- and back-gates (Device 3). The Device 3 characteristics are shown in Supplementary Figure S15, where we find the top- and back-gate act weakly alone but achieve pinch-off if biased together. Comparison with the COMSOL model points to an additional aspect of Figure 5a to explain the following: Why is the top-gate transconductance so poor and comparable to that of the back-gate despite the thinner high-κ oxide? The most plausible explanation is charge trapping at the upper HfO_2/InAs interface, which is deposited by ALD, whereas the lower HfO_2 interface is by van der Waals force only. The lower interface should have negligible effect on InAs surface chemistry while the upper interface should be radically different due to the chemistry of ALD.[77] The charge trapping effects of gate-oxides on InAs nanowires typically onset at negative gate voltage and become more pronounced with increasingly negative voltage.[78−80] Indeed, in Supplementary Figure S16 we show gate sweeps in both directions for the top-gate and back-gate on Device 2. For the back-gate we see negligible hysteresis over the entire $-4.5 < V_{BG} < 0$ V gate range. However, for the top-gate, we see the onset of hysteresis at $V_{TG} = -2$ V with it becoming very strong for $V_{TG} < -3$ V, close to where top-gate saturation occurs. This suggests charge trapping may also play a role, although our COMSOL modeling suggests we do not require trapping to explain gate saturation, which can be entirely due to screening by free electron density in the nanofin.

Together, the results above suggest the need for careful engineering of screening to implement fully operational local gates on future InAs nanofin devices. One option is to grow thinner nanofins. In our COMSOL model, effective gating can be recovered at reduced nanofin thickness $t = 40$ nm even at the higher free electron density $n = 2 \times 10^{17}$ cm^{-3} (see Figure S14c). Another solution for thicker nanofins would be to use a global back-gate to lower the density independently of other patterned local top- or back-gates.[81,82] Regarding the gate insulator, one possibility is to avoid ALD-deposited oxides and opt for alternative insulators, for example, parylene.[83] We make one final comment regarding the data in Figure 5a,b and Supplementary Figure S11. The two-stage pinch-off[84] that we would expect if conduction was dominated by SALs at the top and bottom facets separated by a nonconducting nanofin core is notably absent in our device. Instead, our roughly linear gate dependencies are more consistent with a picture where conduction is more evenly spread through the nanofin with higher density but lower mobility at the surfaces and lower density with higher mobility in the core.

Four-Terminal Resistivity Capability. We finish by using our four-terminal measurement setup to investigate the mobility for our device. There are two possible mobilities to consider. The first is the transport mobility $\mu_t = \sigma/en_{3D}$, which we can obtain by using Hall measurements to get the electron density and the four-terminal resistance at $B = 0$ combined with the nanofin dimensions to get the conductivity σ. This is the mobility traditionally obtained for 2D systems. The second is the field-effect mobility $\mu_{FE} = \frac{\partial G}{\partial V_{BG}}\frac{L^2}{C}$, where $\frac{\partial G}{\partial V_{BG}}$ is the gate transconductance above threshold, L is the channel/nanofin length, and C is the gate capacitance, which we obtain as $C = \frac{\epsilon_0 LW}{d_{SiO_2}/\kappa_{SiO_2} + d_{HfO_2}/\kappa_{HfO_2}}$ with nanofin width W. This is the mobility more frequently used for InAs nanowires since the transport mobility cannot be readily obtained. Note also that μ_{FE} is a single value obtained in the linear region above threshold voltage whereas μ_t can be obtained over a wide range in gate voltage and therefore electron density.

In Figure 5c, we plot n_{3D} versus σ obtained at several different V_{BG} for Device 2. A linear fit can be used to obtain μ_t, however, in contrast to Blömers et al.,[11] we find that our fit (orange line in Figure 5c) does not pass through $n_{3D} = 0$ at $\sigma = 0$. A forced fit through (0, 0) is obviously poor (black dotted line in Figure 5c). Extrapolating our unforced fit (orange line) implies that $\sigma \to 0$ at finite n_{3D}, an expected outcome of localization due to disorder.[85] Note also that our data is obtained at $T = 0.3$ K. This makes our thermal broadening 1000 times smaller than for Blömers et al.,[11] where all measurements are obtained at 300 K. Our unforced fit to the data in Figure 5c (orange line) gives $\mu_t = 2800$ cm^2/(V s). This compares well to the $\mu_t \sim 3600$ cm^2/(V s) obtained by Blömers et al.[11] for MBE-grown InAs nanowires, which should have fewer impurities than our MOVPE-grown InAs nanofins. Our μ_t obtained this way is likely an overestimate, it may be more correct to assume instead that μ_t varies with n_{3D}. This is not unexpected. Mobility often changes with density, for example, in an InGaAs/InAs/InGaAs heterostructure, the mobility increases with density due to screening of background impurities and native charged point defects.[86] Accordingly, we plot μ_t obtained on a single-point basis using the data in Figure 5c, that is, simply calculate $\mu_t = \sigma/en_{3D}$ for each data point, against n_{3D} in Figure 5d. The μ_t values range from 600−1200 cm^2/(V s), still respectable compared to MBE-grown InAs nanowires.[11] We find that μ_t increases with n_{3D}, which we also attribute to screening. There are likely two contributions here: (a) better screening of background impurities in the core by the highern_{3D}, and (b) enhanced screening of surface scattering by the SALs. A deeper study is a subject for future work, but we encourage theoretical studies of mobility versus density in these more surface-exposed structures to better understand the scattering mechanisms involved. Finally, we compare our transport mobility with field-effect mobility. For Device 2 the

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corresponding μ_{FE} = 4400 cm2/(Vs) is 2−3× higher than μ_t (see Supplementary Figure S17 for underpinning data). If we compare μ_t with μ_{FE} for our other devices, we typically find μ_{FE} ranges from slightly above μ_t to several times μ_t. Our findings are consistent with Blömers et al.,[11] who also found μ_{FE} generally substantially exceeds μ_t due to overestimations implicit in the field-effect mobility technique.

Future Prospects. Our results above demonstrate the ability to transfer nanofins to a substrate with a global back-gate and thereafter add multiple ohmic contacts and/or patterned top-gates. There are several aspects for future work. The first is to improve the performance of patterned top-gates. This may involve reducing the nanofin thickness, engineering the gate-insulator used to reduce trapping, or perhaps replacing it entirely with an insulator that does not change the surface chemistry, for example, parylene.[83] Patterned local back-gates would also be desirable. This could be achieved by positioning the nanofin over prepatterned back-gate structures on the device substrate.[81,82] An interesting direction is to extend beyond normal metals to superconductors toward topological quantum information applications. A current approach involves coupling a superconductor to a semiconductor nanowire with strong spin−orbit coupling, for example, InSb,[87] InAs,[88] or InAsSb.[89] More advanced designs for manipulating parafermion modes involve nanowire networks,[10,34] which might also be implemented by etched or gated 2D nanofin structures with patterned superconductor islands/contacts deposited on them (see, for example, concepts in Alicea and Fendley[15]). The presence of a hard gap in the Al-on-InAs system is demonstrated,[88] as is the ability to achieve a hard-gap without direct epitaxial growth of superconductor-on-semiconductor.[90] However, a more forward-looking option inspired by Krogstrup et al.[91] could involve an MOVPE system load-locked to an MBE system, such that nanofins can be grown, and then transferred to high vacuum[92] without air exposure for epitaxial Al deposition onto the large nanofin facets. An additional nice aspect of the nanofins is the potential for accumulation of high electron density at the two nanofin edges because each edge has three facet corners.[12,13] These might provide natural 1D channels for use in parafermion-based device designs.

In conclusion, we have demonstrated a method for the growth of rectangular InAs nanofins with deterministic length, width, and height by dielectric-templated selective-area epitaxy methods. These freestanding nanofins can be transferred mechanically to lay flat on a separate device substrate for fabrication into device structures. A major benefit is that we regain a spatial dimension to exploit for device design compared to nanowires, while retaining the benefits of the "bottom-up" epitaxial growth approach, for example, tiny interfacial areas to enable high-quality heterostructuring.[3] The transferred nanofins can be prepared into devices featuring multiple contacts for Hall effect and four-terminal resistance studies, as well as a global back-gate and nanoscale local top-gates for density control. Electrical studies of our nanofin transistors point strongly to conduction throughout the nanofin thickness, with two key contributions because the electron density is strongly inhomogeneous. First, there is a high density but low mobility surface accumulation layer that facilitates ohmic contact. Conduction predominantly occurs via the nanofin core, where although the electron density is lower, the mobility should be higher due to screening of surface scattering by the surface accumulation layers. Our Hall studies reveal a 3D electron density 2.5−5 × 10^{17} cm^{-3}, which corresponds to an approximate surface accumulation layer density 3−6 × 10^{12} cm^{-2}, in good agreement with previous studies of InAs nanowires.[11,73] We obtain transport mobilities up to 1200 $cm^2/(V\,s)$ and clear quantum interference structure at temperatures up to 20 K. Our nanofins show excellent prospects for fabrication into more complicated devices featuring multiple ohmic contacts, local gates, and possibly other functional elements, for example, patterned superconductor contacts. This may make them an attractive option for future quantum information applications.

Methods. *SAE Template Fabrication.* Growth was performed on undoped InP(111)B substrates. The template was 25 ± 1 nm of SiO_x deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C in an Oxford Plasmalab 100 system and calibrated using ellipsometry. 70 nm of EBL resist (495k-A2 PMMA) was spin-coated at 3000 rpm for 60 s and baked at 180 °C for 3 min on a hot plate. EBL was performed using a Raith 150 EBL system with 20 kV beam energy and 7.5 μm aperture. Development was performed in 1:3 methylisobutylketone/2-propanol solution for 60 s followed by 2 min oxygen plasma ash (PVA TePla, 300 W, 300 sccm O_2 flow) to remove any resist residue in patterned areas. Pattern transfer from the PMMA into the SiO_x was achieved by CHF_3-based reactive ion etching in an Oxford Plasmalab 80+ system. The PMMA resist was stripped in room temperature acetone, followed by a 20 min oxygen plasma etch (PVA TePla, 300 W, 300 sccm O_2 flow) to ensure all organic residues were completely removed. A 5 s dip in a 1% HF solution was performed immediately prior to growth to ensure the exposed InP surfaces are oxide-free.

SAE InAs Growth. The templated substrates were transferred to an Aixtron 200/4 metal−organic vapor phase epitaxy (MOVPE) immediately after the 1% HF dip noted above. A pregrowth anneal in PH_3/H_2 at 750 °C for 10 min was performed prior to growth. Growth was performed at 550−725 °C at 100 mbar in a 14.5 L/min H_2 carrier gas flow with 35 μmol/min of trimethyl indium (TMIn) for all growth runs and 0.7−6 mmol/min arsine (AsH_3), giving V/III ratio between 110 and 1000. Growth was initiated/terminated by adding/removing the group III precursor to/from the gas flow. Cooling down to 350 °C was done with the adequate hydride/H_2 combination, that is, AsH_3/H_2 for InAs nanostructures, and then to room temperature in N_2.

Characterization. The dimensions, facet determination, and morphology of the nanostructures were obtained using either a FEI Verios 460L or a FEI Helios 600 NanoLab field-emission scanning electron microscope with a through lens detector at accelerating voltage between 2 and 10 kV and beam current between 50 pA and 20 nA. SEM images were recorded at angles of 0° (top-view), 20°, 30° and 45° to normal.

Nanofin Transfer and Device Fabrication. The device substrates are 300 μm 2 in. (100) Si wafers doped *n*-type to 0.001−0.005 Ωcm. On the front-side, we grow 100 nm of thermal SiO_2 and then deposit 10 nm of HfO_2 at 150 °C in a Cambridge Nanotech Savannah 100 Atomic Layer Deposition (ALD) system. The HfO_2 layer is not required but included as an etch-stop layer for cases where an oxide-etch is needed in later processing.[49,82] We protect the front-side with hard-baked photoresist, etch the back-side oxide to completion in buffered HF, then deposit 5 nm of Ti and 100 nm of Au by vacuum thermal evaporation to obtain low-resistance contact to the doped substrate, which we use as a global back-gate. After

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stripping the hard-baked photoresist in hot acetone, we deposited Ti/Au bond-pads, interconnects, and alignment markers by one round of photolithography and one round of EBL. This gave 3.5 × 5.5 mm chips each with 24 adjacent device fields (100 × 100 μm), each with four contacts in the corners. Corner contacts in adjacent fields are common, such that for a device with 4 contacts we need 1 field, 6 contacts needs 2 fields, and so on. Device substrates are cleaved to individual chips and thoroughly cleaned by ultrasonication in acetone and 2-propanol prior to use. Mechanical transfer was performed with a micromanipulator system consisting of a high magnification optical microscope (Leica), precision stage (Zaber) and piezo-controlled robot arm (Eppendorf) driving an ultrasharp needle (American Probe Technologies, 0.1 μm radius), combined with some significant practiced skill and patience. The locations of the transferred nanofins relative to the alignment markers are recorded by dark-field microscopy, and used to design appropriate contact and local-gate structures. The device substrate is spin-coated with 950k-A5 PMMA EBL resist at 5000 rpm for 60 s followed by a bake at 180 °C for 5 min on a hot-plate. EBL was performed using a Raith 150-two EBL system (different from templates) with 20 kV beam energy, 20 μm aperture, and ∼300 μC/cm^2 typical dose. Development was performed in 1:3 methylisobutylketone/2-propanol solution for 60 s for both contacts and local-gates. For the contacts, we perform $(NH_4)_2S_x$ passivation at 40 °C for 2 min immediately prior to vacuum evaporation of approximately 5 nm of Ni and 135 nm of Au and liftoff in acetone. The local-gates require two EBL steps: one for the gate-insulator and one for the gate metal. The gate-insulator is 12 nm of HfO_2 deposited at 100 °C by ALD followed by liftoff. The gate metal is approximately 5 nm of Ti and 135 nm of Au by vacuum evaporation followed by liftoff. The completed devices are electrically tested on a probe station, with those viable for further study packaged in LCC20 packages (Spectrum) and bonded with Al wire.

Electrical Measurements. Electrical measurements were performed with devices mounted on an Oxford Instruments Heliox VL ^{3}He system loaded into a liquid helium dewar (Wessington CH-120). This system has a small 2 T superconducting solenoid integrated into the sample-space vacuum can. Temperatures over the range 280 mK to 30 K are readily achieved with good control. Data was obtained using standard ac lock-in techniques using SR-830 lock-ins for demodulation and *I*-to-*V* conversion. Channel bias and current were both continuously monitored in addition to other potentials, for example, Hall, during measurements.

■ ASSOCIATED CONTENT

Supporting Information

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Additional information including growth characterization, fabrication details, and additional electrical data (PDF)

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Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Ferry, D. K.; Goodnick, S. M.; Bird, J. P. *Transport in Nanostructures*, 2nd ed.; Cambridge University Press: Cambridge, 2009.

(2) Hu, J.; Odom, T. W.; Lieber, C. M. Chemistry and physics in one dimension: Synthesis and properties of nanowires and nanotubes. *Acc. Chem. Res.* **1999**, *32*, 435−445.

(3) Samuelson, L. Self-forming nanoscale devices. *Mater. Today* **2003**, *6* (10), 22−31.

(4) Riel, H.; Wernersson, L.-E.; Hong, M.; del Alamo, J. A. III-V compound semiconductor transistors − from planar to nanowire structures. *MRS Bull.* **2014**, *39*, 668−677.

(5) Wagner, R. S.; Ellis, W. C. Vapor-liquid-solid mechanism of single crystal growth. *Appl. Phys. Lett.* **1964**, *4*, 89−90.

(6) Hiruma, K.; Yazawa, M.; Katsuyama, T.; Ogawa, K.; Haraguchi, K.; Koguchi, M.; Kakibayashi, K. Growth and optical properties of nanometer-scale GaAs and InAs whiskers. *J. Appl. Phys.* **1995**, *77*, 447−462.

(7) Tomioka, K.; Ikejiri, K.; Tanaka, T.; Motohisa, J.; Hara, S.; Hiruma, K.; Fukui, T. Selective-area growth of III-V nanowires and their applications. *J. Mater. Res.* **2011**, *26*, 2127−2141.

(8) Güniat, L.; Caroff, P.; Fontcuberta i Morral, A. Vapor phase growth of semiconductor nanowires: Key developments and open questions, *Chem. Rev.* **2019** DOI: 10.1021/acs.chemrev.8b00649.

(9) Wang, N.; Yuan, X.; Zhang, X.; Gao, Q.; Zhao, B.; Li, L.; Lockery, M.; Tan, H. H.; Jagadish, C.; Caroff, P. Shape engineering of InP nanostructures grown by selective area epitaxy. *ACS Nano* **2019** DOI: 10.1021/acsnano.9b02985.

(10) Gazibegovic, S.; Car, D.; Zhang, H.; Balk, S. C.; Logan, J. A.; de Moor, M. W. A.; Cassidy, M. C.; Schmits, R.; Xi, D.; Wang, G.; Krogstrup, P.; Op het Veld, R. L. M.; Zuo, K.; Vos, Y.; Shen, J.; Bouman, D.; Shojaei, B.; Pennachio, D.; Lee, J. S.; van Veldhoven, P. J.; Koelling, S.; Verheijen, M. A.; Kouwenhoven, L. P.; Palmstrøm, C. J.; Bakkers, E. P. A. M.; et al. Epitaxy of advanced nanowire quantum devices. *Nature* **2017**, *548*, 434−438.

(11) Blömers, Ch.; Grap, T.; Lepsa, M. I.; Moers, J.; Trellenkamp, St.; Grützmacher, D.; Lüth, H.; Schäpers, Th. Hall effect measurements on InAs nanowires. *Appl. Phys. Lett.* **2012**, *101*, 152106.

(12) Heedt, S.; Otto, I.; Sladek, K.; Hardtdegen, H.; Schubert, J.; Demarina, N.; Lüth, H.; Grützmacher, D.; Schäpers, Th. Resolving ambiguities in nanowire field-effect transistor characterization. *Nanoscale* **2015**, *7*, 18188−18197.

(13) Degtyarev, V. E.; Khazanova, S. V.; Demarina, N. V. Features of electron gas in InAs nanowires imposed by interplay between nanowire geometry, doping and surface states. *Sci. Rep.* **2017**, *7*, 3411.

(14) Stanescu, T. D.; Tewari, S. Majorana fermions in semiconductor nanowires: fundamentals, modeling, and experiment. *J. Phys.: Condens. Matter* **2013**, *25*, 233201.

(15) Alicea, J.; Fendley, P. Topological Phases with parafermions: Theory and blueprints. *Annu. Rev. Condens. Matter Phys.* **2016**, *7*, 119−139.

(16) Nayak, C.; Simon, S. H.; Stern, A.; Freedman, M.; Das Sarma, S. Non-Abelian anyons and topological quantum computation. *Rev. Mod. Phys.* **2008**, *80*, 1083−1159.

(17) Mandl, B.; Stangl, J.; Martensson, T.; Mikkelsen, A.; Eriksson, J.; Karlsson, L. S.; Bauer, G.; Samuelson, L.; Seifert, W. Au-free epitaxial growth of InAs nanowires. *Nano Lett.* **2006**, *6*, 1817−1821.
(18) Fontcuberta i Morral, A.; Colombo, C.; Abstreiter, G.; Arbiol, J.; Morante, J. R. Nucleation mechanism of gallium-assisted molecular beam epitaxy growth of gallium arsenide nanowires. *Appl. Phys. Lett.* **2008**, *92*, 063112.
(19) Joyce, B. D.; Baldrey, J. A. Selective epitaxial deposition of silicon. *Nature* **1962**, *195*, 485−486.
(20) Tausch, F. W., Jr.; Lapierre, A. G., III A novel crystal growth phenomenon: Single crystal GaAs overgrowth onto silicon dioxide. *J. Electrochem. Soc.* **1965**, *112*, 706−709.
(21) Poole, P. J.; Lefebvre, J.; Fraser, J. Spatially controlled, nanoparticle-free growth of InP nanowires. *Appl. Phys. Lett.* **2003**, *83*, 2055−2057.
(22) Motohisa, J.; Noborisaka, J.; Takeda, J.; Inari, M.; Fukui, T. Catalyst-free selective-area MOVPE of semiconductor nanowires on (111)B oriented substrates. *J. Cryst. Growth* **2004**, *272*, 180−185.
(23) Albani, M.; Ghisalberti, L.; Bergamaschini, R.; Friedl, M.; Salvalaglio, M.; Voigt, A.; Montalenti, F.; Tütüncüoglu, G.; Fontcuberta i Morral, A.; Miglio, L. Growth kinetics and morphological analysis of homoepitaxial GaAs fins by theory and experiment. *Phys. Rev. Materials* **2018**, *2*, 093404.
(24) Chi, C.-Y.; Chang, C.-C.; Hu, S.; Yeh, T.-W.; Cronin, S. B.; Dapkus, P. D. Twin-free GaAs nanosheets by selective area growth: Implications for defect-free nanostructures. *Nano Lett.* **2013**, *13*, 2506−2515.
(25) Aagesen, M.; Johnson, E.; Sørensen, C. B.; Mariager, S. O.; Feidenhans'l, R.; Spiecker, E.; Nygård, J.; Lindelof, P. E. Molecular beam epitaxy growth of free-standing plane-parallel InAs nanoplates. *Nat. Nanotechnol.* **2007**, *2*, 761.
(26) de la Mata, M.; Leturcq, R.; Plissard, S. R.; Rolland, C.; Magen, C.; Arbiol, J.; Caroff, P. Twin-induced InSb nanosails: A convenient high mobility quantum system. *Nano Lett.* **2016**, *16*, 825−833.
(27) Pan, D.; Fan, D. X.; Kang, N.; Zhi, J. H.; Yu, X. Z.; Xu, H. Q.; Zhao, J. H. Free-standing two-dimensional single-crystalline InSb nanosheets. *Nano Lett.* **2016**, *16*, 834−841.
(28) Kelrich, A.; Sorias, O.; Calahorra, Y.; Kauffmann, Y.; Gladstone, R.; Cohen, S.; Orenstein, M.; Ritter, D. InP nanoflag growth from a nanowire template by *in situ* catalyst manipulation. *Nano Lett.* **2016**, *16*, 2837−2844.
(29) Pan, D.; Wang, J.-Y.; Zhang, W.; Zhu, L.; Su, X.; Fan, F.; Fu, Y.; Huang, S.; Wei, D.; Zhang, L.; Sui, M.; Yartsev, A.; Xu, H. Q.; Zhao, J. Dimension engineering of high-quality InAs nanostructures on a wafer-scale. *Nano Lett.* **2019**, *19*, 1632−1642.
(30) Kang, N.; Fan, D.; Zhi, J.; Pan, D.; Li, S.; Wang, C.; Guo, J.; Zhao, J.; Xu, H. Two-dimensional quantum transport in free-standing InSb nanosheets. *Nano Lett.* **2019**, *19*, 561−569.
(31) Conesa-Boj, S.; Russo-Averchi, E.; Dalmau-Mallorqui, A.; Trevino, J.; Pecora, E. F.; Forestiere, C.; Handin, A.; Ek, M.; Zweifel, L.; Wallenberg, L. R.; Rüffer, D.; Heiss, M.; Troadec, D.; Dal Negro, L.; Caroff, P.; Fontcuberta i Morral, A. Vertical "III-V" V-shaped nanomembranes epitaxially grown on a patterned Si[001] substrate and their enhanced light scattering. *ACS Nano* **2012**, *6*, 10982−10991.
(32) Hsu, C.-W.; Chen, Y.-F.; Su, Y.-K. Dislocation reduction of InAs nanofins prepared on Si substrate using metal-organic vapor-phase epitaxy. *Nanoscale Res. Lett.* **2012**, *7*, 642.
(33) Gooth, J.; Borg, M.; Schmid, H.; Schaller, V.; Wirths, S.; Moselund, K.; Luisier, M.; Karg, S.; Riel, H. Ballistic one-dimensional InAs nanowire cross-junction interconnects. *Nano Lett.* **2017**, *17*, 2596−2602.
(34) Krizek, F.; Sestoft, J. E.; Aseev, P.; Marti-Sanchez, S.; Vaitiekenas, S.; Casparis, L.; Khan, S. A.; Liu, Y.; Stankevič, T.; Whiticar, A. M.; Fursina, A.; Boekhout, F.; Koops, R.; Uccelli, E.; Kouwenhoven, L. P.; Marcus, C. M.; Arbiol, J.; Krogstrup, P. Field effect enhancement in buffered quantum nanowire networks. *Phys. Rev. Mater.* **2018**, *2*, 093401.
(35) Vaitiekėnas, S.; Whiticar, A. M.; Deng, M.-T.; Krizek, F.; Sestoft, J. E.; Palmstrøm, C. J.; Marti-Sanchez, M.; Arbiol, J.; Krogstrup, P.; Casparis, L.; Marcus, C. M. Selective-area-grown semiconductor-superconductor hybrids: A basis for topological networks. *Phys. Rev. Lett.* **2018**, *121*, 147701.
(36) Lee, J. S.; Choi, S.; Pendhakar, M.; Pennachio, D. J.; Markman, B.; Rodwell, M. J. W.; Krogstrup, P.; Palmstrøm, C. J. Selective-area chemical beam epitaxy on in-plane InAs one-dimensional channels grown on InP(001) and InP(111)B surfaces. *arXiv* **2018**, 1808.04563.
(37) Aseev, P.; Fursina, A.; Boekhout, F.; Krizek, F.; Sestoft, J. E.; Borsoi, F.; Heedt, S.; Wang, G.; Binci, L.; Martí-Sánchez, S.; Swoboda, T.; Koops, R.; Uccelli, E.; Arbiol, J.; Krogstrup, P.; Kouwenhoven, L. P.; Caroff, P. Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks. *Nano Lett.* **2019**, *19*, 218−227.
(38) Yeh, T.-W.; Lin, Y.-T.; Ahn, B.; Stewart, L. S.; Dapkus, P. D.; Nutt, S. R. Vertical nonpolar growth templates for light emitting diodes formed with GaN nanosheets. *Appl. Phys. Lett.* **2012**, *100*, 033119.
(39) Tutuncuoglu, G.; de la Mata, M.; Deiana, D.; Potts, H.; Matteini, F.; Arbiol, J.; Fontcuberta i Morral, A. Towards defect-free 1D GaAs/AlGaAs heterostructures based on GaAs nanomembranes. *Nanoscale* **2015**, *7*, 19453−19460.
(40) Yang, Z.; Surrente, A.; Tutuncuoglu, G.; Galkowski, K.; Cazaban-Carrazé, M.; Amaduzze, F.; Leroux, P.; Maude, D. K.; Fontcuberta i Morral, A.; Plochocka, P. Revealing large-scale homogeneity and trace impurity sensitivity of GaAs nanoscale membranes. *Nano Lett.* **2017**, *17*, 2979−2984.
(41) Stutz, E. Z.; Friedl, M.; Burgess, T.; Tan, H. H.; Caroff, P.; Jagadish, C.; Fontcuberta i Morral, A. Nanosails showcasing Zn_3As_2 as an optoelectronic-grade earth abundant semiconductor. *Phys. Status Solidi RRL* **2019**, 1900084.
(42) Güniat, L.; Martí-Sánchez, S.; Garcia, O.; Boscardin, M.; Vindice, D.; Tappy, N.; Friedl, M.; Kim, W.; Zamani, M.; Francaviglia, L.; Balgarkashi, A.; Leran, J.-B.; Arbiol, J.; Fontcuberta i Morral, A. III-V integration on Si(100): Vertical nanospades. *ACS Nano* **2019**, *13*, 5833−5840.
(43) Desplanque, L.; Bucamp, A.; Troadec, D.; Patriarche, G.; Wallart, X. In-plane InSb nanowires grown by selective area molecular beam epitaxy on semi-insulating substrate. *Nanotechnology* **2018**, *29*, 305705.
(44) de la Mata, M.; Zamani, R. R.; Martí-Sánchez, S.; Eickhoff, M.; Xiong, Q.; Fontcuberta i Morral, A.; Caroff, P.; Arbiol, J. The role of polarity in nonplanar semiconductor nanostructures. *Nano Lett.* **2019**, *19*, 3396−3408.
(45) Friedl, M.; Cerveny, K.; Weigele, P.; Tütüncüoglu, G.; Martí-Sánchez, S.; Huang, C.; Patlatiuk, T.; Potts, H.; Sun, Z.; Hill, M. O.; Güniat, L.; Kim, W.; Zamani, M.; Dubrovskii, V. G.; Arbiol, J.; Lauhon, L. J.; Zumbühl, D. M.; Fontcuberta i Morral, A. Template-assisted scalable nanowire networks. *Nano Lett.* **2018**, *18*, 2666−2671.
(46) Mandl, B.; Stangl, J.; Hilner, E.; Zakharov, A. A.; Hillerich, K.; Dey, A. W.; Samuelson, L.; Bauer, G.; Deppert, K.; Mikkelsen, A. Growth mechanism of self-catalyzed group III-V nanowires. *Nano Lett.* **2010**, *10*, 4443−4449.
(47) Caroff, P.; Dick, K. A.; Johansson, J.; Messing, M. E.; Deppert, K.; Samuelson, L. Controlled polytypic and twin-plane superlattices in III−V nanowires. *Nat. Nanotechnol.* **2009**, *4*, 50−55.
(48) Hjort, M.; Knutsson, J. V.; Mandl, B.; Deppert, K.; Lundgren, E.; Timm, R.; Mikkelsen, A. Surface morphology of Au-free grown nanowires after native oxide removal. *Nanoscale* **2015**, *7*, 9998−10004.
(49) Storm, K.; Nylund, G.; Samuelson, L.; Micolich, A. P. Realizing lateral wrap-gated nanowire FETs: Controlling gate length with chemistry rather than lithography. *Nano Lett.* **2012**, *12*, 1−6.
(50) Munshi, A. M.; Dheeraj, D. L.; Fauske, V. T.; Kim, D. C.; Huh, J.; Reinertsen, J. F.; Ahtapodov, L.; Lee, K. D.; Heidari, B.; van Helvoort, A. T. J.; Fimland, B. O.; Weman, H. Position-controlled uniform GaAs nanowires on silicon using nanoimprint lithography. *Nano Lett.* **2014**, *14*, 960−966.

DOI: 10.1021/acs.nanolett.9b01703
Nano Lett. 2019, 19, 4666−4677

(51) Noguchi, M.; Hirakawa, K.; Ikoma, T. Intrinsic electron accumulation layers on reconstructed clean InAs(100) surfaces. *Phys. Rev. Lett.* **1991**, *66*, 2243−2246.
(52) Scheffler, M.; Nadj-Perge, S.; Kouwenhoven, L. P.; Borgström, M. T.; Bakkers, E. P. A. M. Diameter-dependent conductance of InAs nanowires. *J. Appl. Phys.* **2009**, *106*, 124303.
(53) Blömers, Ch.; Lepsa, M. I.; Luysberg, M.; Grützmacher, D.; Lüth, H.; Schäpers, Th. Electronic phase coherence in InAs nanowires. *Nano Lett.* **2011**, *11*, 3550−3556.
(54) Jespersen, T. S.; Hauptmann, J. R.; Sørensen, C. B.; Nygård, J. Probing the spatial electron distribution in InAs nanowires by anisotropic magnetoconductance fluctuations. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2015**, *91*, 041302.
(55) Tian, Y.; Sakr, M. R.; Kinder, J. M.; Liang, D.; MacDonald, M. J.; Qiu, R. L. J.; Gao, H.-J.; Gao, X. P. A. One-dimensional quantum confinement effect modulated thermoelectric properties in InAs nanowires. *Nano Lett.* **2012**, *12*, 6492−6497.
(56) Wu, P. M.; Gooth, J.; Zianni, X.; Svensson, S. F.; Gluschke, J. G.; Dick, K. A.; Thelander, C.; Nielsch, K.; Linke, H. Large thermoelectric power factor enhancement observed in InAs nanowires. *Nano Lett.* **2013**, *13*, 4080−4086.
(57) Thelander, C.; Björk, M. T.; Larsson, M. W.; Hansen, A. E.; Wallenberg, L. R.; Samuelson, L. Electron transport in InAs nanowires and heterostructure nanowire devices. *Solid State Commun.* **2004**, *131*, 573−579.
(58) Liang, D.; Sakr, M. R.; Gao, X. P. A. One-dimensional weak localization of electrons in a single InAs nanowire. *Nano Lett.* **2009**, *9*, 1709−1712.
(59) Bird, J. P.; Akis, R.; Ferry, D. K.; Vasileska, D.; Cooper, J.; Aoyagi, Y.; Sugano, T. Lead-orientation-dependent wave function scarring in open quantum dots. *Phys. Rev. Lett.* **1999**, *82*, 4691−4694.
(60) Bird, J. P.; Akis, R.; Ferry, D. K.; de Moura, A. P. S.; Lai, Y.-C.; Indlekofer, K. M. Interference and interactions in open quantum dots. *Rep. Prog. Phys.* **2003**, *66*, 583−632.
(61) Stephens, A. E.; Miller, R. E.; Sybert, J. R.; Seiler, D. G. Shubnikov-de Haas effect in n-InAs and n-GaSb. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1978**, *18*, 4394−4401.
(62) Störmer, H. L. Nobel lecture: The fractional quantum Hall effect. *Rev. Mod. Phys.* **1999**, *71*, 875−889.
(63) Harrang, J. P.; Higgins, R. J.; Goodall, R. K.; Jay, P. R.; Laviron, M.; Delescluse, P. Quantum and classical mobility determination of the dominant scattering mechanism in the two-dimensional electron gas of an AlGaAs/GaAs heterojunction. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1985**, *32*, 8126−8135.
(64) von Klitzing, K. The quantized Hall effect. *Rev. Mod. Phys.* **1986**, *58*, 519−531.
(65) Hansen, A. E.; Björk, M. T.; Fasth, C.; Thelander, C.; Samuelson, L. Spin relaxation in InAs nanowires studied by tunable weak antilocalization. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2005**, *71*, 205328.
(66) Bergmann, G. Weak localization in thin films: A time-of-flight experiment with conduction electrons. *Phys. Rep.* **1984**, *107*, 1−58.
(67) Akis, R.; Ferry, D. K.; Bird, J. P.; Vasileska, D. Weak localization in ballistic quantum dots. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1999**, *60*, 2680−2690.
(68) Iordanskii, S. V.; Lyanda-Geller, Y. B.; Pikus, G. E. Weak localization in quantum wells with spin-orbit Interaction. *JETP Lett.* **1994**, *60*, 206−211.
(69) Liang, D.; Gao, X. P. A. Strong tuning of Rashba spin-orbit interaction in single InAs nanowires. *Nano Lett.* **2012**, *12*, 3263−3267.
(70) Takase, K.; Ashikawa, Y.; Zhang, G.; Tateno, K.; Sasaki, S. Highly gate-tuneable Rashba spin-orbit interaction in a gate-all-around InAs nanowire metal-oxide-semiconductor field-effect transistor. *Sci. Rep.* **2017**, *7*, 930.
(71) Storm, K.; Halvardsson, F.; Heurlin, M.; Lindgren, D.; Gustafsson, A.; Wu, P. M.; Monemar, B.; Samuelson, L. Spatially resolved Hall effect measurement in a single semiconductor nanowire. *Nat. Nanotechnol.* **2012**, *7*, 718−722.
(72) Babadi, A. E.; Lind, E.; Wernersson, L.-E. Modeling of n-InAs metal oxide semiconductor capacitors with high-κ gate dielectric. *J. Appl. Phys.* **2014**, *116*, 214508.
(73) Astromskas, G.; Storm, K.; Karlström, O.; Caroff, P.; Borgström, M.; Wernersson, L.-E. Doping incorporation in InAs nanowires characterized by capacitance measurements. *J. Appl. Phys.* **2010**, *108*, 054306.
(74) Wenner, F. A method of measuring earth resistivity. *Bur. Stand. (U. S.), Bull.* **1916**, *12*, 469−478.
(75) Valdes, L. B. Resistivity measurements on germanium for transistors. *Proc. IRE* **1954**, *42*, 420−427.
(76) de Picciotto, R.; Störmer, H. L.; Pfeiffer, L. N.; Baldwin, K. W.; West, K. W. Four-terminal resistance of a ballistic quantum wire. *Nature* **2001**, *411*, 51−54.
(77) Wheeler, D.; Wernersson, L.-E.; Fröberg, L.; Thelander, C.; Mikkelsen, A.; Westrate, K.-J.; Sonnet, A.; Vogel, E. M.; Seabaugh, A. Deposition of HfO_2 on InAs by atomic-layer deposition. *Microelec. Eng.* **2009**, *86*, 1561−1563.
(78) Dayeh, S. A.; Soci, C.; Yu, P. K. L.; Yu, E. T.; Wang, D. Influence of surface states on the extraction of transport parameters from InAs nanowire field effect transistors. *Appl. Phys. Lett.* **2007**, *90*, 162112.
(79) Roddaro, S.; Nilsson, K.; Astromskas, G.; Samuelson, L.; Wernersson, L.-E.; Karlström, O.; Wacker, A. InAs nanowire metal-oxide-semiconductor capacitors. *Appl. Phys. Lett.* **2008**, *92*, 253509.
(80) Babadi, A. S.; Lind, E.; Wernersson, L.-E. ZrO_2 and HfO_2 dielectrics on (001) n-InAs with atomic-layer-deposited *in situ* surface treatment. *Appl. Phys. Lett.* **2016**, *108*, 132904.
(81) Fasth, C.; Fuhrer, A.; Björk, M. T.; Samuelson, L. Tunable double quantum dots in InAs nanowires defined by local gate electrodes. *Nano Lett.* **2005**, *5*, 1487−1490.
(82) Gluschke, J. G.; Seidl, J.; Burke, A. M.; Lyttleton, R.; Carrad, D. J.; Ulllah, A. R.; Fahlvik, S.; Lehmann, S.; Linke, H.; Micolich, A. P. Achieving short high-quality gate-all-around structures for horizontal nanowire field-effect transistors. *Nanotechnology* **2019**, *30*, 064001.
(83) Gluschke, J. G.; Seidl, J.; Lyttleton, R. W.; Carrad, D.; Cochrane, J. W.; Lehmann, S.; Samuelson, L.; Micolich, A. P. Using ultrathin parylene films as an organic gate insulator in nanowire field-effect transistors. *Nano Lett.* **2018**, *18*, 4431−4439.
(84) Eisenstein, J. P.; Pfeiffer, L. N.; West, K. W. Independently contacted two-dimensional electron systems in double quantum wells. *Appl. Phys. Lett.* **1990**, *57*, 2324−2326.
(85) Mott, N. F. *Metal-Insulator Transitions*; Taylor and Francis: London, 1974.
(86) Hatke, A. T.; Wang, T.; Thomas, C.; Gardner, G. C.; Manfra, M. J. Mobility in excess of 10^6 cm^2/Vs in InAs quantum wells grown on lattice matched InP substrates. *Appl. Phys. Lett.* **2017**, *111*, 142106.
(87) Mourik, V.; Zuo, K.; Frolov, S. M.; Plissard, S. R.; Bakkers, E. P. A. M.; Kouwenhoven, L. P. Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices. *Science* **2012**, *336*, 1003−1007.
(88) Chang, W.; Albrecht, S. M.; Jespersen, T. S.; Kuemmeth, F.; Krogstrup, P.; Nygård, J.; Marcus, C. M. Hard gap in epitaxial semiconductor−superconductor nanowires. *Nat. Nanotechnol.* **2015**, *10*, 232−236.
(89) Sestoft, J. E.; Kanne, T.; Gejl, A. N.; von Soosten, M.; Yodh, J. S.; Sherman, D.; Tarasinski, B.; Wimmer, M.; Johnson, E.; Deng, M.; Nygård, J.; Jespersen, T. S.; Marcus, C. M.; Krogstrup, P. Engineering hybrid epitaxial InAsSb/Al nanowires for stronger topological protection. *Phys. Rev. Materials* **2018**, *2*, 044202.
(90) Gül, Ö.; Zhang, H.; de Vries, F. K.; van Veen, J.; Zuo, K.; Mourik, V.; Conesa-Boj, S.; Noawk, M. P.; van Woerkom, D. J.; Quintero-Pérez, M.; Cassidy, M. C.; Geresdi, A.; Koelling, S.; Car, D.; Plissard, S. R.; Bakkers, E. P. A. M.; Kouwenhoven, L. P. Hard superconducting gap in InSb nanowires. *Nano Lett.* **2017**, *17*, 2690−2696.
(91) Krogstrup, P.; Ziino, N. L. B.; Chang, W.; Albrecht, S. M.; Madsen, M. H.; Johnson, E.; Nygård, J.; Marcus, C. M.; Jespersen, T.

DOI: 10.1021/acs.nanolett.9b01703
Nano Lett. 2019, 19, 4666−4677

S. Epitaxy of semiconductor−superconductor nanowires. *Nat. Mater.* **2015**, *14*, 400−406.
(92) May, M. M.; Supplie, O.; Höhn, C.; van de Krol, R.; Lewerenz, H.-J.; Hannappel, T. The interface of GaP(100) and H_2O studied by photoemission and reflection anisotropy spectroscopy. *New J. Phys.* **2013**, *15*, 103003.

DOI: 10.1021/acs.nanolett.9b01703
Nano Lett. 2019, 19, 4666−4677