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A 10-b 330nW Third-Order Predictive SAR ADC Dedicated to Neural Recording Brain Implants

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***Abstract*— This paper reports on a predictive analog-to-digital converter (ADC). The proposed ADC employs a linear predictive filter to prepare a prediction for the current sample based on the values of the previous digital codes. This leads to significant reduction in the mean bit cycle of the converter. It is shown in this work that this idea is significantly more effective for the digitization of biological signals (*e.g.*, intra-cortical neural signals). Compared with other similar techniques available in the literature, the proposed predictive ADC is significantly more successful for small signal-to-noise ratios. The proposed algorithm results in 48% and 37% reduction in the converter's mean bit cycle compared with the conventional and LSB-first structures, respectively. Designed and post-layout simulated in a 90-nm standard CMOS technology and operated at 200 kS/s with a supply voltage of 0.4 V, the 10-bit predictive ADC consumes 330 nW. The circuit occupies a core area of 0.025 mm^2, achieves an ENOB of 9.42 bits, a figure-of-merit of 2.4 fJ/conv.-step, and an SFDR of 65.8 dB. The DNL and INL of the circuit are within 0.45 LSB and 0.56 LSB, respectively.**

Keywords*— *SAR ADC, neural-specific ADC, predictive ADC, linear predictive filter

I. Introduction

Analog-to-digital converters (ADCs) are key building blocks in almost any electronic system that interacts with the analog peripheral world. In advanced biomedical applications, implantable and wearable devices employ ADCs with medium resolution, rather low conversion speed, and low power consumption. The successive approximation register ADC (SAR-ADC) is a common choice for such devices due to its low power consumption and digital-like structure [1]. One approach in the design of low-power SAR-ADCs is the reduction of power consumption through lowering the DAC switching energy [1]-[2].

As a different approach to the design of low-power SAR-ADCs, there are a family of techniques that aim at lowering the switching activity of the ADC. From among the effective techniques proposed for this purpose, one can name the LSB-first (LSBF) ADC [3], in which the conversion process starts from the least significant bits (LSBs) rather than the most-significant bits (MSBs). It is shown that in this method, the conversion cycle can be shortened for slow and smooth input signal variations. A major application for LSBF ADCs is in biomedical devices because of the sparse and rather low-frequency variation of bio-signals around a base line (*e.g.*, for electrocardiograms as studied in [3]). However, if the input signal is contaminated by noise or fast artifacts, power efficiency of the LSBF algorithm degrades drastically. The idea of a dynamic tracking SAR ADC is proposed in [4] and [5]. In this method, a dynamic tracking window is used to predict the range of the input sample. This method helps reduce switching activities of the ADC especially when the signal does not exhibit instantaneous large variations.

Another idea in lowering the switching activity of SAR ADCs was the introduction of a *bypass window* around a predefined signal baseline [6]. If the input signal sample lies within this window, it skips the conversion steps associated with some of the most-significant bits (MSBs). This saves a considerable amount of power if the signal is confined within the bypass window most of the time. The incremental converting SAR (ICSAR) presented in [7] is in essence a bypass window SAR ADC that digitizes the difference between every two consecutive input samples. The fact that the sample difference has a narrower range than that of the original samples makes the ICSAR idea more power efficient than the basic bypass window SAR ADC.

In this paper, a predictive SAR ADC is proposed, which exhibits high power efficiency when the input signal has a low signal-to-noise ratio (SNR) or a wide range of amplitude variation. An example of such an input signal scenario is the neural signals intra-cortically recorded by brain-implantable microsystems [8]. In the proposed architecture, a high-order prediction filter calculates a sufficiently accurate prediction for the present analog sample based on the previous digital output. This prediction helps the proposed ADC save significant power through lowering the average bit cycle.

II. Proposed Idea

The idea presented in this paper is to embed a digital predictor into a SAR ADC. This predictor monitors the previous digital codes at the output of the ADC, and obtains an initial guess for the digital code associated with the next analog sample being converted into digital. The initial guess is then converted into analog using the same DAC block that is used in the SAR ADC. The difference between the analog sample and the analog equivalent of the initial guess is subsequently the signal that is converted to digital in the proposed predictive ADC. Conversion of the deviation from the initial guess (rather than the analog sample itself) helps reduce the operations required for analog-to-digital conversion, hence considerable saving in the consumed power is achieved. After the digitization of the aforementioned difference, the resulting digital code is added to the initial guess, and the digital output corresponding to the analog sample is provided at the output. A simple block diagram of the proposed idea is shown in Fig. 1. The prediction is calculated using a *linear prediction filter* (*LPrF*) in the digital domain according to the previous samples prepared at the output of the ADC. Converting this prediction to analog, the difference is obtained in the analog domain.

A linear prediction filter is a type of *finite impulse response* (*FIR*) filter that predicts the next sample of a signal s a linear combination of previous samples. Function of an *m*-th order LPrF can be described as:

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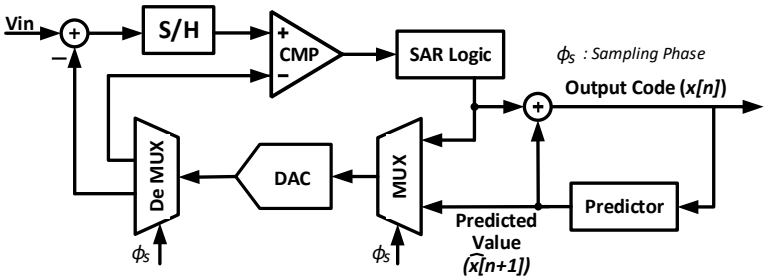


Fig. 1. Simplified block representation of the proposed predictive ADC

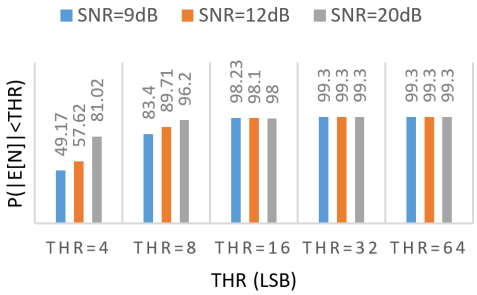


Fig. 2. Effect of the threshold value (max. permissible prediction error, ref. eq. (2)) on prediction error probability for different SNR scenarios

$$\hat{x}[n] = \sum_{i=1}^{m} a_i x[n-i] \quad n \geq m \tag{1}$$

in which a_i is the i-th filter coefficient, $x[n-i]$ the previous observed sample, and $\hat{x}[n]$ is the predicted value of $x[n]$. Proper filter coefficients, a_i, can be found using the autocorrelation method of all-pole modeling [9].

Associated with the value predicted for the next sample, given by (1), there is a prediction error, $e[n]$, that needs to be smaller than a certain maximum value, *THR*, in order to have an accurate enough prediction. Suppose that the prediction is performed for a duration of N signal samples, and that for K samples (out of the total N samples), the prediction error is lower than *THR*. As a measure for the accuracy of prediction, *probability of sufficiently-accurate prediction* is given as:

$$P(|e[n]| < THR) = \frac{K}{N} \tag{2}$$

The idea of using a prediction of the sample under conversion in the analog-to-digital conversion process leads to significant power saving. This is achieved through considerable reduction in the number of bit cycles required to convert an input analog sample to the corresponding digital code at the output. As will be discussed later, this power saving is much more significant than the additional power that needs to be spent on prediction. It should be added that the extent of the achieved power saving depends on the filter design (*i.e.*, its order and the choice of coefficients), the ADC sampling frequency, and the input signal.

III. Predictive Filtering of Neural Signals

The key idea proposed in this work relies on the fact that action potentials in a neural signal are of a continuous and rather smooth amplitude variation regime. This makes it possible for a proper prediction filter to provide a reasonable estimation of the sample under study based on the values of the previous samples. On the other hand, amplitude variations of the background noise in a neural signal (in the absence of action potentials) occur within a rather small range. Therefore, even though background noise variation does not follow a specific predictable regime, estimation of the next sample of the background noise would most likely lie within the prediction range of the filter.

A. Design of a neural-specific LPrF

To design an LPrF specifically for neural signals, one needs to specify the proper order and coefficients for the filter. The higher the filter order is, the smaller the maximum prediction error ($|e[n]|$) and consequently the higher the probability of achieving a small-enough prediction error (*i.e.*, $P(|e[n]|<THR)$) will be. In other words, from the perspective of the achieved prediction performance, designing the filter with a higher order result in a more accurate prediction. However, this benefit comes at the cost of a higher physical implementation. According to our studies, going beyond 3rd-order results in additional increase in circuit complexity, while it barely adds to the accuracy of the prediction. Therefore, the LPrF used in this work was chosen to be of 3rd-order with predicted signal formulated as:

$$\hat{x}[n] = a_1 x[n-1] - a_2 x[n-2] + a_3 x[n-3] \tag{3.a}$$

in which the vector $\boldsymbol{a} = [a_1 \; a_2 \; a_3]$ contains the filter coefficients. For a given filter order and at a certain sampling frequency, coefficients of the filter need to be determined for the specific type of signal being processed. To come up with proper values for the coefficients of an LPrF specifically designed for neural signals, and also for the evaluation of the performance of the predictive ADC proposed in this work, a library of intra-cortical neural signals reported by Quiroga, *et al*, in [10] was used.

Designed for a 1-minute neural signal with *signal-to-noise ratio* (*SNR*) of a low as ~10dB containing 3 different action potential wave shapes (spike classes), filter coefficients are calculated as:

$$\mathbf{a} = [2.4325 \quad -2.1636 \quad 0.7307] \tag{3.b}$$

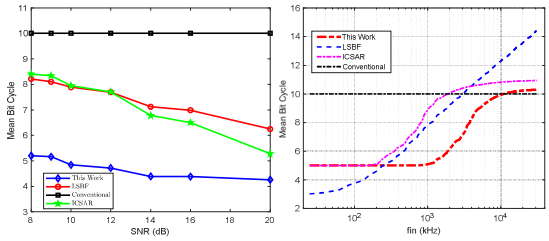
It should be added that for spike classes #1, #2, and #3, the number of spikes present in the signal were 1208, 1137, and 1189, respectively. In order to implement the filter using a power- and area-efficient standard digital circuit, the coefficients are replaced with such approximate values that can be expressed using *canonic signed digit* (*CSD*) representation [11]:

$$a_1 \cong 2^1+2^{-1}=2.5,\; a_2 \cong -(2^1+2^{-2}) = -2.25,\; a_3 \cong 2^{-1}+2^{-2}=0.75 \tag{3.c}$$

With this set of coefficients, the filter can be implemented merely using combinational shifters and binary adders. As a result of using approximate coefficients, prediction of the filter is degraded by less than 1% (worst case).

B. The Choice of the Threshold Value

Choosing a proper threshold value (THR) is of critical importance in the efficacy of the proposed idea in terms of bit cycle saving and consequently energy saving of the predictive SAR ADC presented in this work. With a rather large threshold value, a small bit cycle saving is achieved for the majority of samples with a rather high probability of sufficiently-accurate prediction $P(|e[n]| < THR)$. Lowering the threshold level results in achieving a larger extent of bit cycle saving with a lower probability of prediction error, albeit for a limited number of samples. In other words, there is a tradeoff



(a) (b)

Fig. 3. Comparison of the mean bit cycle of the proposed ADC with that of conventional SAR ADC, LSB-first ADC, and ICSAR ADC (a) Mean bit cycle as a function of the input signal frequency in the case of sinusoidal inputs (b) Mean bit cycle as a function of the input SNR for neural input signals (acquired from [10])

between the saving achieved in conversion bit cycles (and consequently the consumed power) and the prediction accuracy. Decision on the proper choice for the threshold level depends on the attributes of the input signal (*e.g.*, speed and pattern of amplitude variations of the signal in the time domain) and the frequency at which the signal is sampled.

For the LPrF designed in (3.c), probability of sufficiently-accurate prediction $P(|e[n]| < THR)$ is plotted in Fig. 2 as a function of the prediction error threshold, THR, for three different SNR values: 9, 12, and 20dB. It should be noted that digitization resolution or least significant bit (LSB). According to this plot, threshold values greater than 8 LSBs cause negligible improvement in the probability of sufficiently-accurate prediction. The threshold value is therefore chosen to be THR=8 LSB.

C. Performance for Action Potentials

According to the conceptual explanation provided above, because of the continuous and rather smooth regime of amplitude variations for action potentials, it is expected that the prediction mechanism helps save some of the conversion steps in the A/D conversion process. The extent of this saving, however, depends on the success of the LPrF in its prediction. To obtain a sense of the significance of the prediction success, Table II presents the probability of sufficiently-accurate predictions for the three different spike wave shapes. It should be added that the results presented in Table I are achieved for an SNR range of as wide as 8-26 dB for an SNR range of as wide as 8-26 dB. The neural spikes were acquired from the intra-cortical dataset recorded from the neocortex and basal ganglia (available online at [8]). The results achieved indicate that regardless of the specific wave shapes of the spikes, the general pattern of amplitude variations leads to almost the same probability of sufficiently-accurate prediction. According to Table I, the probability itself is meaningfully high (ranging from 0.64 to 0.8), and for a given SNR scenario, the maximum deviation from one class to another is as low as 0.07. It should be noted that the results reported in Table II are achieved for a total of 1000+ noisy spikes per class.

D. Performance for Background Noise

Occurrence of action potentials in a typical intra-cortical neural signal is a sparse phenomenon, meaning that for the majority of time, the ADC converts the analog background noise to digital. Therefore, performance of the proposed predictive ADC (*e.g.*, power consumption, average bit cycle saving, and total prediction performance) is predominantly determined by the background noise. Performance of the LPrF in the case of a background noise input is also presented in Table I. Noting that the threshold level in this case is the same

TABLE I: PROBABILITY OF PREDICTION ERROR FOR NEURAL SIGNALS WITH DIFFERENT SPIKE WAVE SHAPES AND WITH THE PRESENCE OF BACKGROUND NOISE AS A FUNCTION OF SNR

SNR (dB)	$P(\lvert e[n]\rvert < THR)$				
	Spikes			Bckgnd Noise	**Overall (Spikes + BckgndNoise)**
	Class1	Class2	Class3		
26	0.8	0.74	0.8	0.99	**0.97**
20	0.79	0.73	0.78	0.99	**0.97**
16	0.77	0.71	0.75	0.98	**0.96**
14	0.77	0.72	0.79	0.98	**0.96**
12	0.73	0.68	0.74	0.95	**0.92**
10	0.72	0.67	0.73	0.93	**0.91**
9	0.68	0.64	0.7	0.89	**0.84**
8	0.68	0.64	0.7	0.88	**0.84**

as that for spike studies (*i.e., THR*=8), subrange prediction of the noise samples is significantly more successful than that of spike samples. Probability of sufficiently-accurate prediction for the background noise ranges from 0.88 in the worst-case noise level scenario to as high as 0.99.

E. Overall Performance

To realistically measure the performance of the proposed ADC, a complete intra-cortical neural signal (containing action potentials and background noise) is used as the input. In this signal, action potentials are of the three different wave shapes. Fig. 3 presents the average number of the bit cycles required for the completion of a conversion cycle for a 10-bit predictive SAR ADC equipped with a 3rd-order LPrF in the case of a sine wave (Fig. 3.a with a sampling rate of 200 kS/s) and a neural signal (Fig. 3.b with a sampling rate of 24 kS/s). To highlight the significance of the superiority of the proposed converter over other major ADC techniques, Fig. 3 presents the mean bit cycles for a conventional SAR ADC, an LSB-first ADC (LSBF) [3], and an incremental converting SAR ADC (ICSAR) [7], all of the same resolution and operating at the same sampling rate. According to Fig. 3.a (for sine waves), the mean bit cycle of the proposed ADC (as well as that of the ICSAR technique) is equal to 5 for extremely low frequencies. While the mean bit cycle of the LSBF and ICSAR techniques rises at rather low frequencies (~300 Hz), that of the proposed technique remains low, and is in fact the smallest from this point forward. It is true that the mean bit cycle of LSBF is the smallest at extremely low frequencies, but it goes up to 22 as the frequency increases. As presented in Fig. 3.b, for neural signals, the prediction mechanism in the proposed ADC reduces the average number of bit cycles by 48%-57% compared with the conventional SAR scheme when the SNR varies from 8-20 dB. This is a significant achievement noticing the fact that the number of bit cycles directly contributes to the power consumption of the ADC. One of the advantages of the proposed predictive ADC is the fact that unlike LSBF and ICSAR architectures, performance of the converter (average number of bit cycles and consequently power consumption) remains almost constant as the SNR decreases.

IV. THE PROPOSED PREDICTIVE ADC

Fig. 4 shows a simplified circuit diagram of the proposed predictive ICSAR ADC. The key difference between the ADC proposed in this work and the basic ICSAR ADC architecture introduced in [7] is the fact that the initial guess in this work is produced using an LPrF (rather than based on the previous sample). Predicted amplitude of the next sample (a digital codeword) is made ready as soon as the conversion

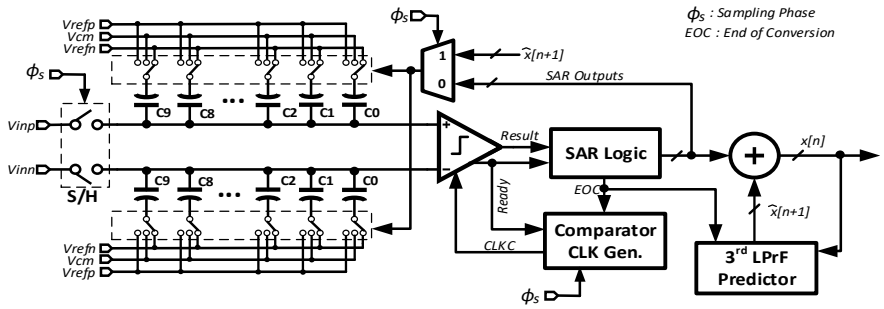


Fig. 4. Simplified circuit diagram of the proposed predictive ADC

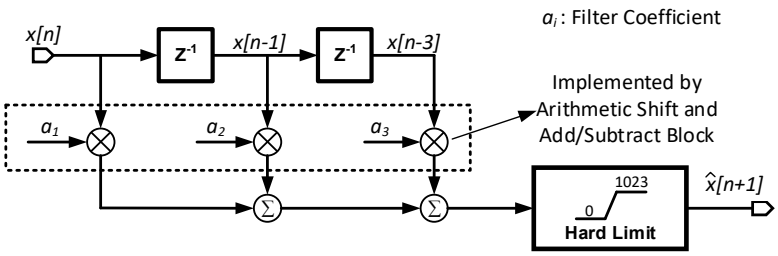


Fig. 5. Digital implementation of the 3rd-order LPrF used in this work

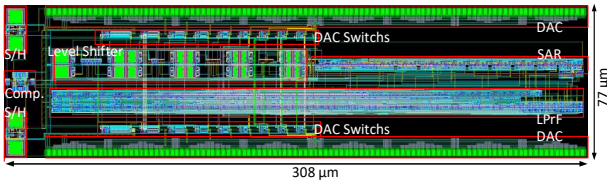


Fig. 6. Physical layout of the proposed ADC

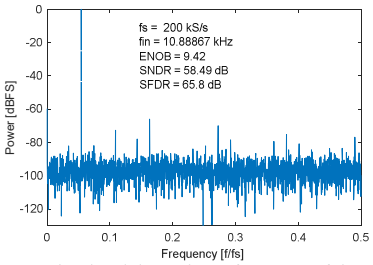


Fig. 7. Simulated dynamic performance of the proposed ADC (4096 points)

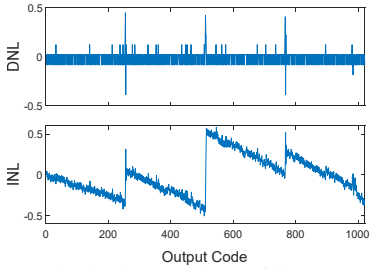


Fig. 8. Simulated DNL and INL of the proposed ADC

TABLE II: COMPARATIVE SPECIFICATION SUMMARY

	[3]	[7]	[12]	[13]	[14]	This Work*
Tech. (nm)	180	180	180	180	90	**90**
Supply (V)	0.6	0.6	0.75	0.65	0.3	**0.4**
No. of Bit	10	10	11	10	10	**10**
f_s/f_{in} (kHz)	450/0~225	200/10	10/0.5	320/8	3000/-	**200/10**
ENOB (Bit)	9.82	9.3	9.76	9.61	9.08	**9.42**
SNDR (dB)	60.3	57.86	60.5	59.60	56.4	**58.49**
SFDR (dB)	83.5	72.27	72	73.87	74	**65.8**
DNL (LSB)	0.08	+0.29/ -0.26	+0.6/ -0.37	0.30	+0.83/ -0.54	**+0.45/ -0.38**
INL (LSB)	0.2	+0.39/ -0.80	+0.94/ -0.89	0.43	+0.84/- 0.89	**+0.56/ -0.50**
Power (µW)	3.7u~13u	2	0.25	1.6	6.6	**0.33**
Area (mm^2)	0.12	0.154	0.126	0.056	0.08	**0.034**
FoM (fJ/c.-s.)	9.1~35	15.51	28.8	6.38	4.065	**2.408**

*Based on post-layout simulation

of the current sample is completed. According to the basics of ICSARs [7], during the sampling phase, the difference between the predicted value and the current analog sample is provided to the CDAC, compared with an 8-LSB bypass window (*i.e.*, THR), and subsequently converted to digital. For immunity against common mode noise and to suppress the even harmonics, we use a fully differential architecture.

To be used in a 10-b ICSAR ADC, a 9-b CDAC is designed in this work with top plate sampling. To minimize the power dissipation associated with DAC switching and also taking into consideration the capacitor mismatch and kT/C noise, the unit capacitance is chosen about 2 fF. The DAC unit capacitor is implemented with the Metal-Oxide-Metal (MOM) structure using metal layers 3-7.

A two-stage dynamic comparator adopted from [12] is used in this work in order to achieve sufficiently-low kickback noise and low power consumption. According to Monte Carlo simulations, offset (1 sigma) of the comparator used in this work is about 3.1 mV.

As the sample & hold circuit, the double bootstrap scheme introduced in [2] is adopted for its linearity at low supply voltages.

For next-sample prediction, a 3rd-order LPrF is designed based on the block representation shown in Fig. 5. The LPrF is implemented using transmission gates (TGs) and clocked-CMOS digital circuits, and also TG-based D-type flip-flops for storage elements. To realize the filter function, coefficients are implemented by using the *canonic signed digit* representation [11], realized using combinational arithmetic shifters and adders/subtractors.

V. RESULTS

The proposed predictive SAR ADC was designed in a 90-nm standard CMOS process. The layout of the proposed ADC presented in Fig. 6, which measures 308 µm x 77 µm. For a 10-kHz sine wave input and a sampling rate of 200 kS/s, the 4096-point FFT of the post-layout simulated ADC output is shown in Fig. 7. The signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 58.49 dB and 65.8 dB respectively. For the proposed predictive SAR ADC, the effective number of bits (ENOB) is 9.42 bits, and the DNL and INL of are given in Fig. 8, according to which the max/min DNL and INL are +0.45/-0.38 LSB and +0.56/-0.50 LSB, respectively. The total power dissipation of the proposed ADC is 330 nW (V_{dd}= 0.4V), and the figure of merit (energy per conversion step) is 2.91 fJ/conv.-step. Performance summary for the proposed ADC along with those for some of the recent relevant works are presented in Table II.

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