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Ishihara, R.

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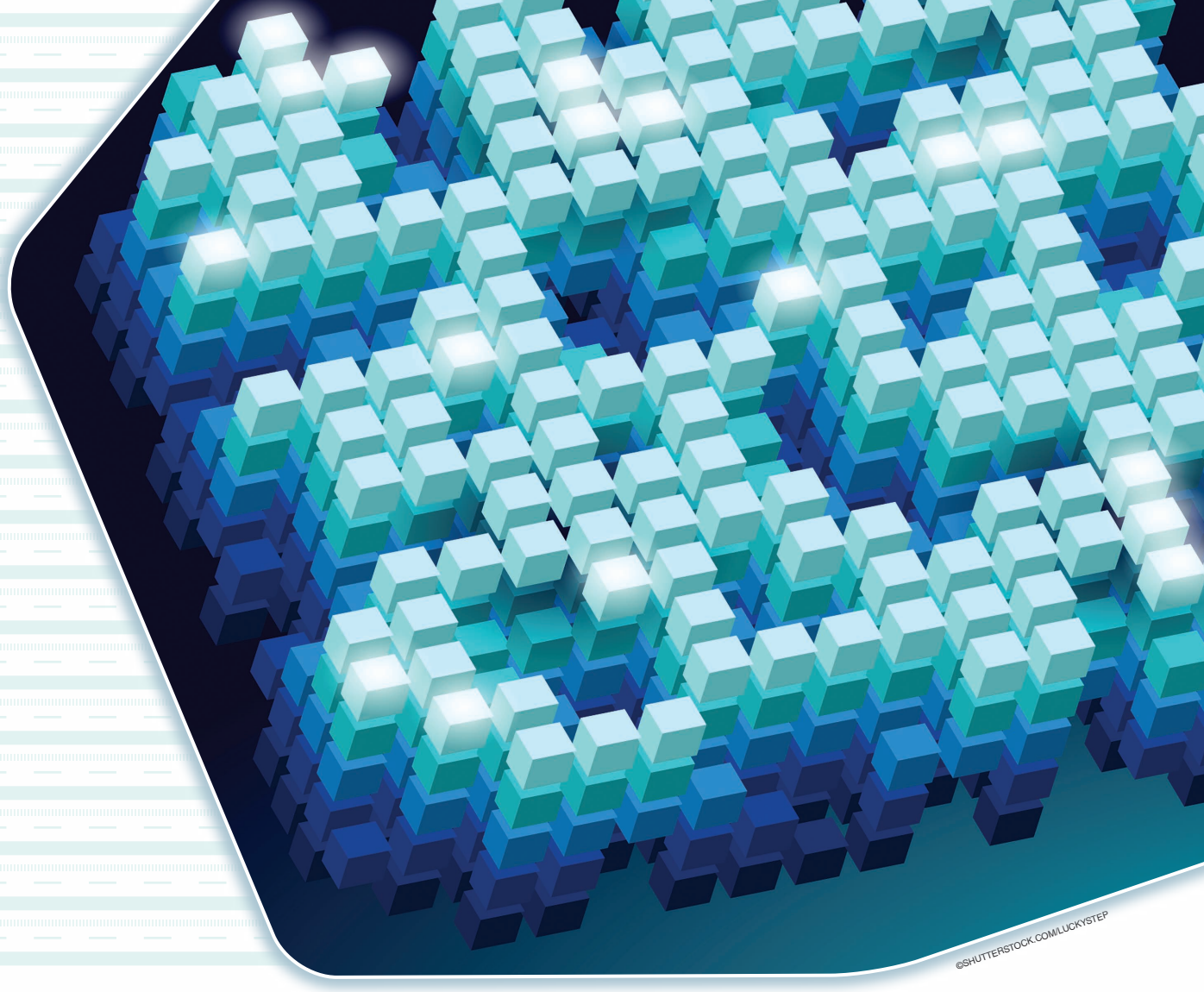

Integration Technology Challenges in Quantum Computers

The Size, Noise and Wires Matter

By Ryoichi Ishihara

Quantum computers are expected to unlock information processing capabilities and speed up simulation times to rates that cannot be achieved by classical computers [1]. But the technology is still in its nascent stages compared to the aspirations of achieving large-scale fault-tolerant computing.

Today's noisy intermediate-scale quantum algorithms [2] can solve a few specific problems in chemistry, material science, and machine learning faster than their classical counterparts. However, the noise and overhead of current systems affect their general applicability.

Quantum hardware development is limited by the qubit count (presently ~100) [3], [4], error rates, and coherence times. Integration remains a major challenge to demonstrating systems at scale. Multiple approaches for qubit platforms include superconducting qubits [5], semiconductor spins [6], trapped ions [7], neutral atoms [8], photonics [9], and

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color centers in diamond [10], [11]. Each has its tradeoffs in terms of scalability, error rates, connectivity, and operation temperature, as discussed below.

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MUCH RESEARCH AND DEVELOPMENT ARE REQUIRED, AND IT IS DIFFICULT TO PREDICT AT THIS STAGE HOW THE FIELD WILL EVOLVE.

Qubit Size

Over the last two decades, tremendous progress in superconducting qubits has resulted in their becoming mainstream. Superconducting qubits [5] can provide fast and high-fidelity control and readout with great tunability. More recently, superconducting qubits have been fabricated via industrial processes on 300-mm wafers [5]. However, the size of the qubit is on the order of millimeters, dictated by the size of microwave resonators and capacitors, and the large size could be a showstopper for a large-scale superconducting quantum computing chip. For example, 1 million qubits would require a surface area of 1 m^2, which would not fit in a dilution fridge. Therefore, other qubit platforms that require less area have emerged as serious contenders. These include, and may not be limited to, spin qubits in semiconductors [6] and diamond [10], [11].

Crosstalk

Will we solve the problem of scalability if we employ a smaller-sized qubit, like Moore's law scaling of semiconductor devices and circuits? The answer is no, as we have a specific challenge in a quantum computing chip. Because a qubit consists of a few small particles, it is naturally prone to noise, such as charge or magnetic field. When tiny qubits are densely packed in a small space, the noise from neighboring qubits acts as the noise source, and this reduces the fidelity or increases the error rate. On the other hand, having a larger distance between qubits is less attractive for reasons stated above. Therefore, it is preferable to have high scalability and small crosstalk between qubits. The ultimate approach could be a modular quantum computing architecture [12], [13], [14], [15], as shown in Figure 1, which is devised with long-range quantum links connecting many modules having only a few qubits. The advantage of a modular quantum computing architecture is that the number of qubits can be increased by repeating the module without deteriorating the fidelity because the noise can be kept to a minimum.

Connectivity

Another issue is the connectivity between qubits/modules. In modern classical high-performance computing, performance relies very much on parallelization by interconnects among MPUs. In quantum computers, connectivity is even more critical and beneficial because it determines how qubits can interact with one another to deliver entanglement and superposition capability. This interaction is necessary for performing quantum operations and executing quantum algorithms. The logical states of N qubits can increase exponentially by $2N$. One can reduce the qubit resource for fault-tolerant quantum computers with high connectivity. While the mainstream superconducting qubit system is limited by nearest-neighbor entanglement [3], [4], optically active spin systems, such as ion traps [7], neutral atoms [8], and color centers in diamond [10], [11], are capable of beyond-nearest-neighbor and even all-to-all entanglement [16]. Optical quantum links enabling long-range entanglement [17] can be used for interconnecting modules on chip. Here, on-chip photonics ICs [18] will become a key enabling technology. Furthermore, quantum computing chiplets could be integrated on an electro-optical interposer, analogous to 3D heterogeneous packaging in electronic semiconductors.

Wiring/Thermal

The last, but not the least, among the challenges is the wiring, which is related to the need for a cryogenic temperature for most qubits. To control and read the state of a qubit, electrical wires need to be connected from electronics at room temperature (RT) to nearby qubits at close to 0 K inside a cryostat. Many types of qubits operate in a microwave frequency range to control the state and

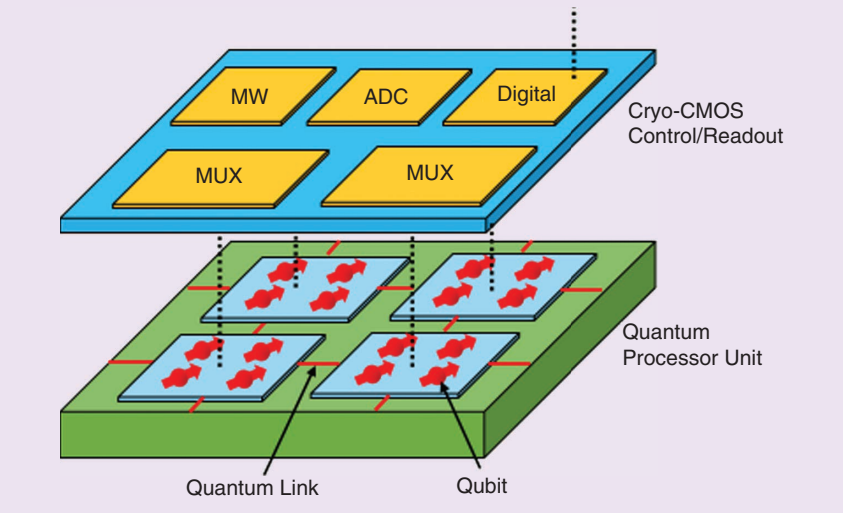

FIGURE 1. A modular quantum computing chip with spins, with 3D integrated control/readout circuits. The quantum processor unit consists of modules of arrays of qubits (red arrows and circles) that are connected by quantum links. The qubits are controlled by the chip bonded above, which generates microwave (MW) signals. The analog signals of the qubits are read and converted to digital signals via an ADC. The incoming serial digital signals are demultiplexed to parallel signals by a MUX and fed into the qubits and/or the MW generator. Those control and readout circuits can be made with a CMOS chip operating at cryogenic temperature (cryo-CMOS).

need thick and bulky superconducting RF coaxial cables. Already, the current quantum computing chip with superconducting qubits employs a fan-out and vertical connection with TSVs [19] from the back side instead of the traditional wire bonds. However, the pins for coaxial cable are even larger than the superconducting qubits, which prohibits high-density wiring for a large-scale quantum computer. Another problem is the heat dissipation from RT to qubits through many cables, as the cooling power of the dilution fridge is limited. A possible solution could be to include CMOS control electronics near qubits operating at cryogenic temperature (cryo-CMOS) [13], [14], [20], [21] or control electronics made by superconductors [22], which can demultiplex the signals and, hence, reduce the number of wires significantly. Integration of a microwave generator and DAC [23] will be even more beneficial. Here, ultralow-power operation is the key challenge. If the classical chip is flip-chipped on the qubit plane via superconducting microbumps [14], [19], [24], it will be even more scalable. Another solution is to scale the operation temperature. Many superconducting and semiconductor qubits require an operation temperature of ~100 mK. Other qubits, such as color centers in diamond, trapped ions, and photonic qubits, operate at higher temperatures, and this will alleviate the cooling power limitation and, hence, the issue of the integration of qubit and cryo-CMOS chips.

In summary, the four integration technology challenges of a large-scale quantum computing chip must be addressed simultaneously; however, there is no one-size-fits-all solution. This is why much research and development are required, and it is difficult to predict at this stage how the field will evolve. However, one thing is evident: electron device technologies play a key role in resolving these issues. To make R&D activities more effective, we need a community. The IEEE Electron Devices Society has formed the Quantum Technology Technical Committee, and we will keep supporting industry and academia toward a quantum-enabled future.

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Biographie

Ryoichi Ishihara (r.ishihara@tudelft.nl) is with the Faculty of Electrical Engineering, Mathematics, and Computer Science, QuTech, Delft University of Technology, 2628 CD Delft, The Netherlands.

References

[1] Y. Alexeev et al., "Quantum computer systems for scientific discovery," *PRX Quantum*, vol. 2, no. 1, 2021, Art. no. 017001, doi: 10.1103/PRXQuantum.2.017001.

[2] J. Preskill, "Quantum computing in the NISQ* era and beyond," *Quantum*, vol. 2, p. 79, Jan. 2018, doi: 10.22331/q-2018-08-06-79.

[3] M. AbuGhanem, "IBM quantum computers: Evolution, performance, and future directions," *J. Supercomput.*, vol. 81, Apr. 2025, Art. no. 687.

[4] Google Quantum AI, "Suppressing quantum errors by scaling a surface code logical qubit," *Nature*, vol. 614, no. 7949, pp. 676–681, 2023.

[5] J. Van Damme et al., "Advanced CMOS manufacturing of superconducting qubits on 300 mm wafers," *Nature*, vol. 634, no. 8032, pp. 74–79, 2024, doi: 10.1038/s41586-024-07941-9.

[6] S. G. J. Philips et al., "Universal control of a six-qubit quantum processor in silicon," *Nature*, vol. 609, no. 7929, pp. 919–924, 2022, doi: 10.1038/s41586-022-05117-x.

[7] D. L. Moehring et al., "Entanglement of single-atom quantum bits at a distance," *Nature*, vol. 449, no. 7158, pp. 68–71, 2007, doi: 10.1038/nature06118.

[8] S. Ritter et al., "An elementary quantum network of single atoms in optical cavities," *Nature*, vol. 484, no. 7393, pp. 195–200, 2012, doi: 10.1038/nature11023.

[9] S. Slussarenko and G. J. Pryde, "Photonic quantum information processing: A concise review," *Appl. Phys. Rev.*, vol. 6, no. 4, 2019, Art. no. 041303.

[10] F. Jelezko and J. Wrachtrup, "Single defect centres in diamond: A review," *Phys. Status Solidi A*, vol. 203, no. 13, pp. 3207–3225, 2006, doi: 10.1002/pssa.200671403.

[11] E. Rugar et al., "A quantum photonic interface for tin-vacancy centers in diamond," *Phys. Rev. X*, vol. 11, Jul. 2021, Art. no. 031021.

[12] N. H. Nickerson, J. F. Fitzsimons, and S. C. Benjamin, "Freely scalable quantum technologies using cells of 5-to-50 qubits with very lossy and noisy photonic links," *Phys. Rev. X*, vol. 4, no. 4, 2014, Art. no. 041041, doi: 10.1103/PhysRevX.4.041041.

[13] L. M. K. Vandersypen et al., "Interfacing spin qubits in quantum dots and donors—Hot, dense, and coherent," *npj Quantum Inf.*, vol. 3, no. 1, 2017, Art. no. 34, doi: 10.1038/s41534-017-0038-y.

[14] R. Ishihara et al., "3D integration technology for quantum computer based on diamond spin qubits," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp. 14.5.1–14.5.4, doi: 10.1109/IEDM19574.2021.9720552.

[15] A. Gold et al., "Entanglement across separate silicon dies in a modular superconducting qubit device," *npj Quantum Inf.*, vol. 7, no. 1, 2021, Art. no. 142, doi: 10.1038/s41534-021-00484-1.

[16] M. H. Abodeih et al., "Fault-tolerant operation of a logical qubit in a diamond quantum processor," *Nature*, vol. 606, pp. 884–889, May 2022.

[17] B. Hensen et al., "Loophole-free Bell inequality violation using electron spins separated by 1.3 kilometres," *Nature*, vol. 526, no. 7575, pp. 682–686, 2015, doi: 10.1038/nature15759.

[18] H. Atabaki et al., "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," *Nature*, vol. 556, no. 7701, pp. 349–354, 2018, doi: 10.1038/s41586-018-0028-z.

[19] D. Rosenberg et al., "3D integrated superconducting qubits," *npj Quantum Inf.*, vol. 3, no. 1, 2017, Art. no. 42, doi: 10.1038/s41534-017-0044-0.

[20] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018, doi: 10.1109/JSSC.2017.2737549.

[21] R. Acharya et al., "Multiplexed superconducting qubit control at millikelvin temperatures with a low-power cryo-CMOS multiplexer," *Nature Electron.*, vol. 6, no. 11, pp. 900–909, 2023, doi: 10.1038/s41928-023-01033-8.

[22] M. G. Castellano et al., "Rapid single-flux quantum control of the energy potential in a double SQUID qubit circuit," *Supercond. Sci. Technol.*, vol. 20, no. 6, p. 500, 2007, doi: 10.1088/0953-2048/20/6/003.

[23] L. Enthoven, M. Babaie, and F. Sebastiano, "Optimizing the electrical interface for large-scale color-center quantum processors," *IEEE Trans. Quantum Eng.*, vol. 5, no. 1, pp. 1–17, 2024, doi: 10.1109/TQE.2024.3416836.

[24] S. Kosen et al., "Building blocks of a flip-chip integrated superconducting quantum processor," *Quantum Sci. Technol.*, vol. 7, no. 3, 2022, Art. no. 035018, doi: 10.1088/2058-9565/ac734b.

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