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Wireless Power and Bidirectional Data Transfer for Modern Closed-Loop Neural Implants

Ouyang, Y.

DOI
10.4233/uuid:a4ef8275-1737-42b5-90e6-6457b074c4b6

Publication date
2025

Document Version
Final published version

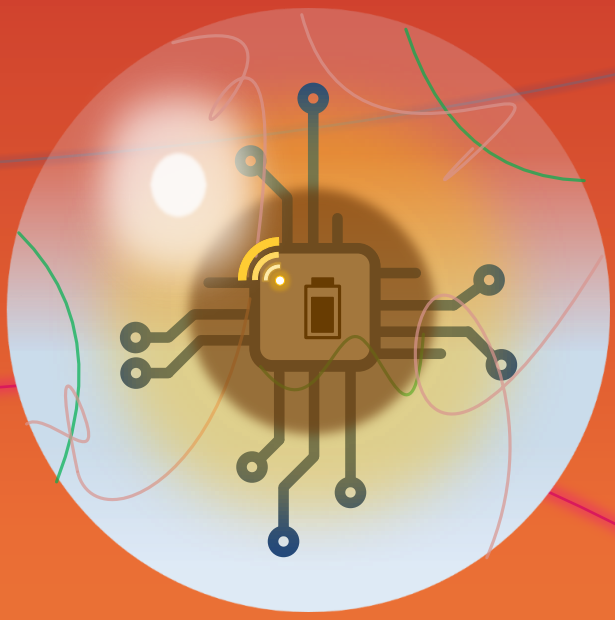
Citation (APA)
Ouyang, Y. (2025). *Wireless Power and Bidirectional Data Transfer for Modern Closed-Loop Neural Implants*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:a4ef8275-1737-42b5-90e6-6457b074c4b6

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Wireless Power and Bidirectional Data Transfer

for Modern Closed-Loop Neural Implants

Yihan Ouyang

Wireless Power and Bidirectional Data Transfer for Modern Closed-Loop Neural Implants

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus, Prof. dr.ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
Thursday 22 January 2026 at 10:00 o'clock

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Keywords: Inductive Powering, Wireless Data Communication, Dual Output Rectifier, Wireless Power Transfer, Neural Implants

Printed by: Johannes Gutenberg

Cover by: Yihan Ouyang

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978-94-6518-201-8
An electronic copy of this dissertation is available at
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Chapter 1

Introduction

1.1 Motivation

Implantable biomedical electronic systems are becoming increasingly prevalent in modern healthcare, offering personalized therapies for previously untreatable diseases. Over the past few decades, significant progress has been made in the development of implantable devices such as cochlear implants [1–3], retinal prostheses [4–8], and brain-machine interfaces [9–13]. Recent advancements in microelectronics [8, 14–18] and microfabrication [19–23] have enabled increasingly miniaturized and high-precision implantable systems. Further advancing these devices creates stringent demands on power delivery and data communication, necessitating efficient energy management and high-bandwidth wireless telemetry. Wireless Power Transfer (WPT) is essential in such implant systems, eliminating the constraints and potential risks associated with cable tangling and tethering [24–26]. Simultaneously, reliable wireless bi-directional data transmission is crucial for real-time operation and closed-loop control. These challenges drive ongoing research efforts to improve the efficiency and robustness of wireless power and communication links for biomedical implants, including the design of implantable wireless chips.

Wireless Power Transfer for Neural Interfaces

While significant progress has been made in wireless power transfer (WPT) for implantable neural interfaces (NIs), critical challenges remain. One challenge is delivering sufficient power to implants operating in lossy tissue environments, typically on the order of tens of milliwatts [27–29]. The demand for increased functionality and complexity in NIs, such as high-density neural recording and multi-channel neural stimulation, necessitates even greater power delivery. However, simply increasing transmitter power can lead to issues like reduced battery life, excessive heat dissipation, and increased size and weight of the external power source. Therefore, maximizing end-to-end power efficiency, from the transmitter to the implanted load, is crucial. This requires optimizing the efficiency of the transmitter, the wireless link, and the power management unit (PMU) within the receiver chip.

Robustness is another major challenge in WPT for implantable NIs. Movement within the human body and changing load conditions can

significantly impact system performance and pose potential risks to patients. Body movement can cause misalignment of the wireless link, degrading power transfer efficiency. Load variations can lead to instability and fluctuations in the power supply, potentially disrupting the implant's functionality. Addressing these challenges requires careful co-design of the wireless link and the PMU to ensure stable and regulated power delivery under various operating conditions.

Wireless Data Telemetry for Neural Interfaces

Beyond wireless power transfer, bi-directional data communication is a crucial aspect of modern implantable NIs [30], enabling precise, dynamic interaction between the implant and external controllers for optimal therapeutic outcomes. Recent research in implantable NIs [24–26] highlights several key requirements for future bidirectional communication in NIs: high channel counts necessitate high-bandwidth links and advanced modulation/demodulation techniques to support high data rates; stringent power constraints demand highly efficient transmitter and receiver designs; minimal reliance on off-chip components is crucial for a compact, implantable form factor; and seamless bidirectional data exchange with minimal latency is necessary for closed-loop neural modulation.

Modern closed-loop neuromodulation systems can intelligently deliver stimulation patterns. They can generate responsive neurostimulation when specific physiological conditions are met; they can also generate adaptive neurostimulation by dynamically optimizing stimulation parameters to modulate the effect on each channel [31, 32]. These functionalities rely on the recording and analysis of both spontaneous and stimulus-evoked neural activity, making both downlink (external-to-implant) and uplink (implant-to-external) communication equally critical. However, many existing systems prioritize open-loop stimulation, neglecting real-time uplink communication necessary for closed-loop operation [6, 33, 34]. Consequently, these systems often implement only unidirectional telemetry or support limited uplink data rates, which are insufficient for the high data exchange demands of future NIs. To support over 1000 to 10,000 neural recording channels with 10-bit resolution at a sampling rate of 20,000 samples per second, the uplink data rate should reach approximately 200 Mbps [35] to 2 Gbps [32](calculated as $\textit{data rate} = \textit{channel count} \times \textit{bit depth} \times \textit{sampling rate}$).. Achieving such high data rates with low power consumption in a compact implant necessitates careful co-design of the transmitter circuits and the wireless link. Therefore, improving existing telemetry architectures and developing efficient, fully integrated solutions remain key research challenges for future neural implant systems.

1.2 Background

1.2.1 Wireless Powering and Data Communication Methods

Wireless powering and data communication can be implemented using several methods, including near-field inductive coupling, mid/far-field RF/electromagnetic coupling, near-field capacitive coupling, ultrasonic transmission, and optical communication, each with distinct advantages and limitations (Fig 1.1). These methods are typically evaluated based on link efficiency, data rate, spatial constraints, and penetration depth. Link efficiency is crucial, as implanted devices often depend on external power sources and are subject to strict transmission and safety regulations. The data rate is another key factor and depends heavily on the target application. For example, some medical implants, like pacemakers, function effectively with low data rates of around 25 kbps [36], while more complex neural implants for brain activity monitoring may require data rates up to 500 Mbps [27]. Implant size also imposes constraints, requiring a balance between communication performance and device miniaturization. Finally, the penetration depth of these different communication methods varies. Each method is briefly described below, and their characteristics are summarized in Table 1.1. A comprehensive comparison of various wireless power and data transfer technologies is presented in Fig 1.2, based on literature published over the past decade.

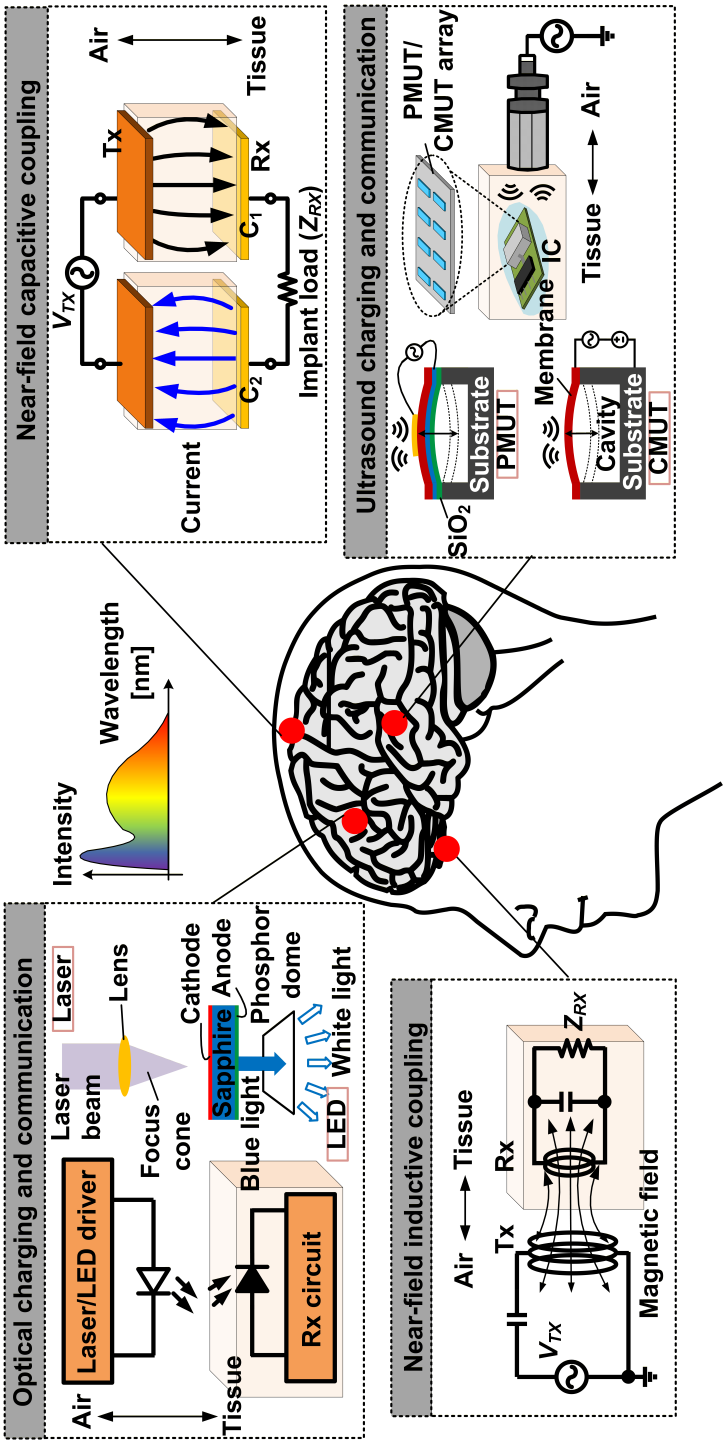


Figure 1.1: Conceptual diagrams illustrating the operating principles of four selected wireless technologies. The nominal implant depth for each topology is indicated by red dots in the figure.

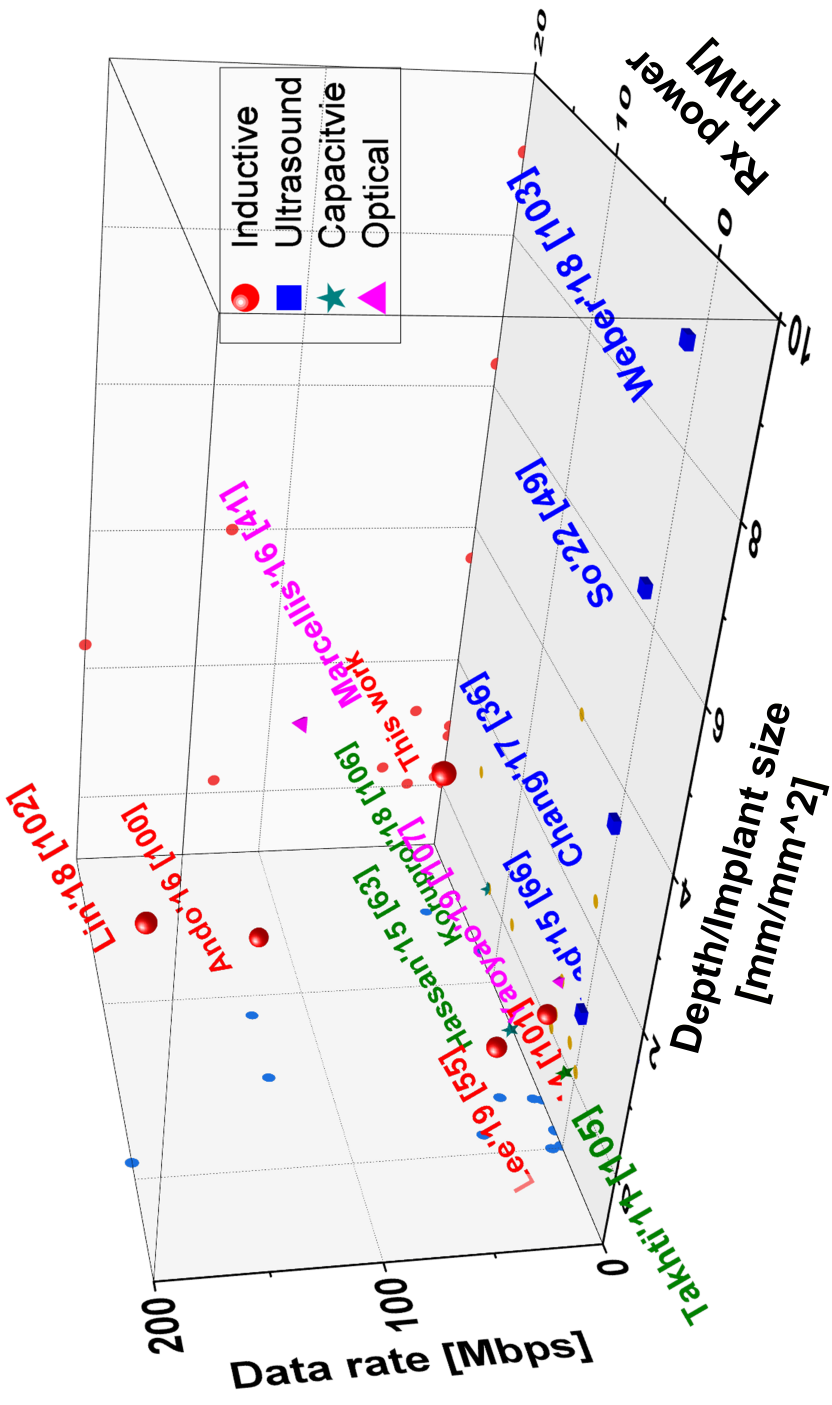


Figure 1.2: Survey of application ranges for various wireless technologies and the potential operational region of this research.

Optical Coupling Optical transmission uses light emission as a means of wireless power and data transfer. On the Tx side, a laser diode or light-emitting diode (LED) converts electrical energy into an optical beam, which can be either focused or diffused (Fig 1.1, top-left). The beam then propagates through air and biological tissue. On the Rx side, a light-sensitive transistor or photovoltaic diode [37] captures the incident light and converts it back into electrical energy, achieving both power delivery and data recovery (also known as optical wireless communication [38]). A typical capacity for optical powering is on the order of 1 mW/cm^2 [39, 40]. The maximum achievable data rate is theoretically constrained by the carrier frequency, which can exceed several terahertz. However, practical implementations are limited by parasitic reflections and light diffusion, resulting in demonstrated data rates of approximately 100 Mbps [40–42]. In addition to its high data rate capability, this technique offers strong immunity to electromagnetic (EM) interference, making it a promising solution for high-speed communication in implantable applications.

Despite its advantages, the primary limitation of optical transmission lies in the misalignment between the transmitting and receiving ends caused by body movement. Misalignment can occur as either a lateral shift or an angular shift, each significantly affecting power delivery. Studies have shown that lateral misalignment can reduce the received power density by approximately 89%, while angular misalignment results in an average reduction of 7%, both of which severely degrade the signal quality of the optical link [43]. In addition to misalignment, optical links suffer from high signal attenuation due to tissue-related phenomena such as absorption, scattering, and reflection, thereby restricting their feasibility for deeply implanted neural interfaces. These limitations impose several requirements, including a direct line-of-sight transmission path and the placement of the optical receiver near the skin surface with optimized wavelength selection. For instance, near-infrared LEDs operating at 810 nm have been reported to achieve a penetration depth of 40 mm through biological tissue [43]. However, such constraints pose significant challenges for biomedical applications requiring deep implantation.

Near-field Inductive Coupling Near-field inductive coupling (NIC) is the most widely used technique in commercial implantable NIs for wireless power transfer and bidirectional data communication, due to its reliability and easy integration. The operational region of an electromagnetic link depends on the intended separation distance (d) of the link. It can be categorized into three main domains: near-field inductive coupling, mid-field coupling, and far-field EM radiation. The following equations define these regions:

$$d_{NF} = \frac{\lambda}{2\pi}, d_{FF} = \frac{2D^2}{\lambda} \tag{1.1}$$

where d_{NF} denotes the near-field boundary, d_{FF} represents the far-field boundary, D is the largest side dimension of the Tx coil and λ is the correspondent wavelength at the operation frequency.

The mid-field region is defined as $d_{NF} < d < d_{FF}$, whereas the far-field region corresponds to $d > d_{FF}$. Since most implantable NIs applications require a link separation distance of a few centimeters, near-field inductive coupling ($d < d_{NF}$) is widely employed, with operation frequencies ranging from a few kilohertz (kHz) to several gigahertz (GHz). This method establishes an inductive coupling between the Tx and Rx coils (Fig 1.1, bot-left), enabling efficient energy and data transfer via a magnetic field. The time-varying magnetic field induces an electromotive force at the Rx coil, which can be harvested for power and data delivery. Assuming a circular type coil link with a separation distance of d is used for power delivery. On the Tx side, the magnetic flux density B_d at a distance d from the center of the Tx coil can be expressed as Eq. (1.2) using Biot-Savart Law [44, 45]:

$$B_d = \frac{\mu_0}{2} \frac{R_1^2 N_1 I_1}{(d^2 + R_1^2)^{3/2}} \tag{1.2}$$

where μ_0 is the permeability of free space, R_1 is the Tx coil diameter, N_1 is the number of turns, and I_1 is the circular loop current.

On the Rx side, the induced voltage and received power can be estimated as Eq. (1.3) using Faraday's law of induction [45, 46]:

$$V_{\text{coil,RX}} = N_2 \frac{d\Phi}{dt} = A_2 \times N_2 \frac{dB_d}{dt}, P_{\text{coil,RX}} \approx \frac{\pi^2 N_2 B_d R_2^3}{4\mu} \times \frac{dB_d}{dt} \tag{1.3}$$

where A_2 is the effective area of the Rx coil, N_2 is the number of turns, R_2 is the Rx coil diameter, and μ denotes the permeability of Rx coil. This equation highlights that the effective power is significantly influenced by the effective coil area perpendicular to the magnetic field, the Rx coil size, and the magnet field strength at the implant position.

Under the loosely coupled conditions typically encountered in these multi-tissue layer environments, where coupling coefficients generally range from 0.05 to 0.24 [47, 48, 50, 71], resonance tuning is commonly used to enhance power transfer efficiency (PTE). Depending on the load requirements, either a series [51–53] or parallel [54–57] resonance topology can be employed. Series resonance tuning provides a high current and low voltage to low-impedance loads (typically less than 200Ω), whereas parallel resonance tuning delivers a high voltage and low current to high-impedance loads (typically 200Ω to 5kΩ). Given that NIs typically operate in the milliwatt power range and rectifier circuits exhibit better efficiency at high voltage levels, parallel resonance tuning has become the preferred choice in such designs [58]. The resulting LC resonator amplifies the Rx voltage by a quality factor (Q), which

typically ranges from 10 to 100 [50]. While higher Q factors at sub-GHz frequencies improve PTE, tissue absorption increases exponentially with frequency, limiting the WPT frequency to below a few tens of MHz [60, 61, 71]. This frequency constraint also limits the achievable data rate. However, high data rates can be achieved by using a separate data antenna in addition to the power coil. For example, the work in [27] demonstrates a dual-band system operating at 13.56 MHz for power transfer and achieving a 500 Mbps uplink data rate, although this requires separate links for power and data transmission.

Near-field Capacitive Coupling Near-field capacitive coupling (NCC) enables WPT via electric field coupling between two sets of electrodes. As illustrated in Fig. 1.1 top right, this approach employs one pair of electrodes for the forward current path and another for the return path, forming a complete current loop without requiring a direct conductive medium between the transmitting and receiving electrodes.

NCC offers a cost-effective WPT solution with notable advantages in terms of fabrication flexibility and seamless integration with ultra miniaturized integrated circuits. One key benefit of this approach is its negligible eddy current loss, distinguishing it from inductive power transfer systems, where EM losses become a major concern at high operating frequencies. Additionally, NCC exhibits superior resilience to angular misalignment and positional variations compared to acoustic-based energy transfer methods (e.g., ultrasonic powering). These characteristics make it particularly well-suited for applications involving flexible and conformal electronics.

NCC can also achieve high data rate communication. Unlike inductive coupling, which exhibits a low-pass nature, the capacitive link relies on an electric field as the data carrier between the Tx and Rx electrodes. This allows the upper bound of the data bandwidth to reach the carrier signal frequency. A high data rate of 200 Mb/s has been reported using NCC [62–65].

Despite its advantages, NCC is inherently constrained by its strong dependence on operating frequency and capacitance. The output voltage signal V_{Rx} at the implant load Z_{Rx} is given by Eq. (1.4):

$$V_{Rx} = V_{Tx} \frac{Z_{Rx}}{Z_{Rx} + \frac{1}{j\omega}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} \tag{1.4}$$

where V_{Tx} is the voltage amplitude of the AC source at the Tx side, ω is the angular frequency, and C_1 and C_2 denote the electrode capacitance. As this equation indicates, achieving a substantial output voltage at the implant side requires both high operating frequencies and large capacitance values. However, increasing capacitance necessitates larger electrode areas and reduced mutual distances, which impose practical constraints on device miniaturization and implantation feasibility.

Furthermore, the capacitive reactance between the Tx and Rx plates introduces substantial impedance that varies significantly with frequency. While higher frequencies enhance power transfer efficiency, they also increase dielectric losses and limit the penetration depth of the electric field, ultimately reducing the effective transmission range. This trade-off imposes a fundamental limitation on the power delivery capability of NCC, making it less suitable for most neural implant applications, which typically require milliwatt-level power transfer (0.1∼35.2 mW in [27–29, 66]) over Tx-Rx separation distances exceeding 10 mm.

Ultrasonic Coupling Ultrasound (US) wireless power and data transmission uses acoustic waves to propagate through biological tissue, offering an alternative to inductive coupling. As illustrated in Fig. 1.1 bot right, in an ultrasonic implant system, the Tx unit generates mechanical surface vibrations, producing acoustic pressure waves typically between 140 kHz and 10 MHz [58, 67–70]. These waves propagate through tissue and are captured by an acoustic energy harvester, which is implanted within the body and ideally positioned within the primary radiation lobe of the Tx source. The energy harvester, which can be based on piezoelectric micromachined ultrasonic transducer (PMUT) [36, 71–74] or capacitive micromachined ultrasonic transducer (CMUT) [75–77] technology, converts the incident acoustic energy into electrical power, enabling efficient, contactless energy delivery to deeply embedded biomedical implants.

A key distinction between ultrasonic and inductive coupling lies in their propagation mechanisms: while inductive coupling can operate even in a vacuum, ultrasonic power transfer necessitates a physical medium for wave propagation. Nevertheless, ultrasound-based techniques exhibit lower attenuation in biological tissues (with values ranging from 0.0022 dB/cm/MHz to 1.0 dB/cm/MHz for fluids and organs [78–80]) compared to inductive transmission, which suffers from significant absorption and attenuation. For instance, [81] demonstrated an ultrasonic energy transfer link capable of delivering 35 mW of power at an implant depth of up to 85 mm, operating at a frequency of 720 kHz. Similarly, [82] developed a 5 MHz PMUT array for 3D intracardiac ultrasound imaging, achieving a penetration depth of 8–10 cm. To ensure patient safety, the U.S. Food and Drug Administration (FDA) specifies a maximum permissible intensity of 7.2 mW/mm^2 for diagnostic ultrasound applications [83], which is nearly two orders of magnitude higher than the limit for conventional inductive coupling (0.1 mW/mm^2) [84].

While ultrasonic power transfer offers advantages for powering deep implants, it suffers from significant power losses at the air-tissue interface due to the large acoustic impedance mismatch. The attenuation of ultrasound in air is an order of magnitude higher than that in soft tissue, with values of 7.50 dB/cm/MHz for air compared to 0.75 dB/cm/MHz for soft tissue [78]. Additionally, the limited bandwidth of

ultrasonic transducers at a given carrier frequency constrains achievable data rates. These challenges require careful design of modulation schemes and transducer architectures to optimize energy efficiency and improve the viability of ultrasonic telemetry for implantable NIs.

1.3 Objectives

Previous research on NIs has highlighted the growing demand for wirelessly powered smart implants. Two fundamental aspects must be considered in the design of these devices to ensure seamless interaction with external systems. First, NIs should incorporate all essential functional blocks, including power management and data telemetry modules, to facilitate efficient power reception and data telemetry. Power efficiency in the implant is essential to minimize tissue heating and damage. Second, these devices must be miniaturized to meet their intended clinical applications, ideally occupying only a few mm^3. Achieving such a compact form factor is crucial not only for minimizing surgical invasiveness but also for enhancing long-term biocompatibility and patient safety.

This research focuses on inductive wireless power and data transmission due to its established efficacy and practicality. Compared to alternative methods like capacitive or ultrasonic coupling, inductive coupling offers superior end-to-end efficiency for our target application of a retinal implant, with reduced integration complexity and operation within safe frequency ranges. Furthermore, its ability to simultaneously deliver wireless power and support high-data-rate bidirectional communication makes it well-suited for next-generation neural interface systems.

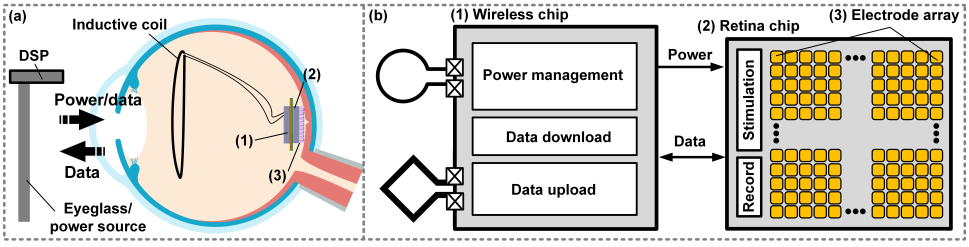


Figure 1.3: A conceptual representation of an artificial retina implant system. The implant system comprises (1) A wireless chip with off-chip coils for wireless power and data transfer, (2) A retina chip powered by the wireless chip, and (3) A microelectrode array (MEA) interfacing with retinal ganglion cells. The entire system is positioned on the retina layer at the back of the eye.

This research aims to address three critical aspects of implantable NIs:

Table 1.1: Summary of the major advantages and disadvantages of some popular WPT and Data Communication Approaches

Types	Working principles	Advantages	Disadvantages
Near field inductive link	Based on magnetically coupled circuits where energy is transferred between a primary (Tx) coil and a secondary (Rx) coil through strong magnetic field coupling; Typically operates at frequencies in the kHz to MHz range.	High power transfer efficiency at close range, typically millimeters to a few centimeters. The efficiency can be further improved by resonant tuning.	Efficiency is strongly influenced by the coil geometry and relative alignment. The link's bandwidth and data rate are limited by the carrier frequency due to its low-pass nature [64]).
Far field RF link	Typically operates at higher frequencies (MHz to GHz), leveraging strongly resonant electromagnetic coupling rather than pure inductive coupling.	Data communication can be achieved over long distances with high data rates, offering less stringent alignment requirements compared to near-field inductive coupling.	Lower efficiency than near-field inductive power transfer. Can cause higher energy absorption in biological tissues due to the high operation frequency.
Capacitive link	Uses two aligned parallel plates placed on the inner/external side of skin. The inner tissue acts as lossy dielectric.	High data bandwidth communication due to the capacitive link's high-pass nature. High level immunity to Electromagnetic Interference (EMI) due to its confined field lines within plates [65].	The seperation depth is typically less than 1 cm, and the capacitor plate size is at least 10 times of the desired distance due to the fundamental nature of capacitive coupling [40].
Ultrasound link	Transmits acoustic waves through biological tissues, which are converted to electrical energy by either piezoelectric or capacitive micromachined ultrasound transducers (MUTs) inside the body.	Ultrasound link exhibits low loss propagation and high power safety limit in the tissue environment due to the lower attenuation of acoustic waves in biological tissues [83, 85].	Energy loss due to acoustic mismatch between air-tissue and tissue-bone interfaces. Transducer integration complexity. The achievable data rate is generally low (around several Mb/s) [72]. High reflection rate on the air-tissue interface [71].
Optical link	Uses laser or LED-based light transmission to deliver power to a photovoltaic receiver.	High level immunity to EMI inteference and high achievable data rate due to its THz operation frequency (infrared to visible light range).	Significant reduction in received energy due to misalignment of the Tx-Rx pair caused by body movement.

(1) the co-optimization of the power and data antenna structure alongside the implantable chip to maximize power transfer efficiency while minimizing the overall device footprint, (2) the development of a compact and reliable bi-directional data communication system to facilitate future closed-loop neuromodulation devices, and (3) the design of a PMU for wireless power transfer that minimizes power conversion losses and provides dedicated stable voltage outputs for neural stimulation and recording.

This research is embedded within the development of an artificial retina implant (Fig 1.3). This application exemplifies the technological and engineering challenges associated with miniaturized closed-loop neurostimulation devices. An implanted device records and stimulates neurons in the retina through a microelectrode array to provide artificial vision in patients that suffer from retina degeneration [32]. The implanted device nominally consumes 5 mW of power and requires 200 kb/s downlink and 20 Mb/s uplink bidirectional data transfer. This thesis explores the feasibility of both wireless power transfer and data communication methods, considering factors such as power efficiency, tissue safety, and implantation procedures. The analysis identifies the most suitable approach for stable, reliable energy delivery while minimizing device size. It also examines the trade-offs between power transmission performance and biocompatibility, critical factors in designing next-generation, miniaturized implants.

1.3.1 Research questions

The key research questions in this thesis revolve around the development of a highly efficient and miniaturized wireless power transfer and data communication system for an artificial retina. The primary focus is to overcome existing limitations in power efficiency, robust communication, form factor, and integration constraints while ensuring compatibility with clinical requirements. To achieve this, the following research questions are formulated:

1. **For the wireless link design:** What is the optimal link structure and topology for the wireless power and data telemetry link? What are the optimal parameters for coil number, number of external devices, coil diameter, separation distance, materials, frequency, and other relevant factors? How should the power RX coil be interconnected with the chip? What are the associated power losses, and how can they be minimized? Should the resonance frequency be tunable?

2. **For the data telemetry:** How should the communication topology be selected based on the system clock and input voltage requirements? How can these topologies be designed for compatibility with the implanted chip (a highly asymmetrical system with greater constraints inside the chip and more flexibility outside)? How can external components be minimized or eliminated?

3. For the PMU design: How can the power efficiency of the PMU IC be maximized, given the chosen coil link design? How should voltage regulation be implemented (e.g., LDO, DC-DC) considering load variations? How can multiple outputs with different loading conditions be generated from a single AC input? How can external components (resonant capacitors, filtering capacitors, etc.) be minimized while maintaining competitive performance?

1.3.2 Research approach

This research proposes a comprehensive investigation into the design and implementation of power-efficient wireless implantable NIs, encompassing three key approaches:

1) Wireless Link Design: This research will establish a general guiding principle for the design of resonant inductive wireless power transfer links for biomedical implants. Both power and data telemetry links will be modeled and optimized using finite element analysis to achieve optimal performance at the chosen operating frequency. Link performance, including the impact of angular misalignment, separation distance, and tissue absorption, will be evaluated through simulations and experimental validation in a laboratory setting.

2) Data Telemetry Design: A comprehensive survey of data telemetry techniques for similar implantable applications will be conducted. The optimal topology meeting the required data rate within the available frequency band will be selected, considering power and area budgets for both downlink and uplink data communication. The robustness of the data communication link will be assessed under varying carrier signal amplitude and operating frequency. A chip prototype will be fabricated and measured to validate the data telemetry circuits.

3) Power Management Unit Design: Simplified behavioral models will be developed to compare the performance of different PMU topologies. Simulation results will be validated against analytical calculations for key performance metrics, including voltage ripple, maximum achievable receiver voltage and current, and loop stability. The PMU will be designed to provide dual output voltages while maintaining high efficiency, with loading conditions that match those of modern closed-loop neuromodulation devices. A chip prototype will be fabricated and measured to validate the PMU.

1.4 Thesis goal and organization

This research aims to develop a highly efficient and fully integrated wireless implant system for a future artificial retina. It addresses the limitations of existing solutions in power management, wireless data communication, and integration with the coil link in closed-loop neuromodulation devices. To achieve this, the research introduces several innovations at

both the system and circuit levels to enhance the overall power efficiency of the wireless chip under inductive power transmission.

The thesis is organized into five chapters:

Chapter 2 describes the design and optimization of a high-efficiency inductive link operating under weak coupling conditions and an ultra-wideband (UWB) data uplink. A quality-factor-based optimization procedure is presented to reduce simulation complexity during finite element modeling for the power inductive link. Both power coil and data antenna link designs are experimentally validated.

Chapter 3 introduces a wireless implant system featuring bi-directional data communication, employing a dual-loop, any-load-stable regulator for power management and a fully digital envelope detector for downlink data.

Chapter 4 presents a 40.68 MHz fully integrated dual-output PMU for wireless neural implants, addressing the challenge of providing a low-voltage, high-power supply alongside a high-voltage, low-power supply. This chapter also introduces a novel resonance breakup switch for improved efficiency and independent startup in dual-mode rectifiers.

Chapter 5 concludes the dissertation, summarizing the main contributions and discussing potential future research directions.

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Chapter 2

Coil Link Design For Wireless Power Transfer And Data Communication

2.1 Introduction

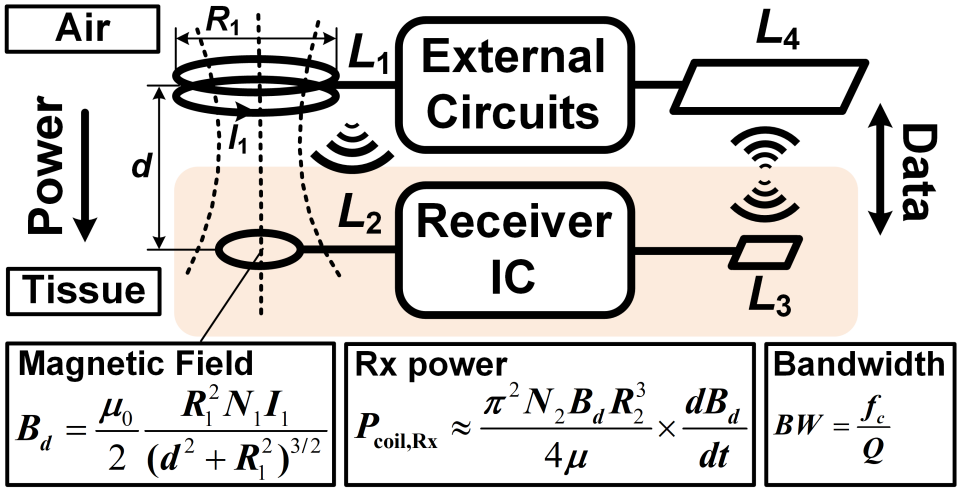


Figure 2.1: The general system architecture of a wireless power and data transfer system, where power is delivered through a power coil pair ($L_1 - L_2$), while downlink and uplink data are transmitted via a data antenna pair ($L_3 - L_4$).

Fig. 2.1 shows a typical wireless power and data transfer system structure with bi-directional data communication capability for an implant system [1–3]. Implantable devices must be small, lightweight, and long-lasting due to strict surgical and usage requirements. However, as smaller coils inherently have a weaker magnetic field and, therefore, a lower coupling coefficient between the Tx and Rx coils, miniaturization makes it challenging to maintain adequate power efficiency, especially when relying on inductive wireless power and data transfer. This means

less power is transferred for the same input power, directly impacting power transfer efficiency and signal-to-noise ratio in the data path. Furthermore, the power transfer efficiency is strongly dependent on the alignment and distance between the coils, posing a challenge for transcutaneous power delivery. This chapter describes the design approach used for both the power and data links in the artificial retina implant.

A key design parameter for maximizing the RF inductive link efficiency is the operating frequency. The equations presented in Fig. 2.1 (as well as Eq. (1.2) and Eq. (1.3) in Chapter 1) indicate that a higher operating frequency enhances the magnetic flux density, thereby increasing the received power. However, in practice, the operating frequency is not arbitrarily high and is often chosen within the industrial-scientific-medical (ISM) band. There are two main reasons for this selection. First, many off-the-shelf commercial components are designed to operate within this band, facilitating device compatibility and easing component selection. Second, higher frequencies lead to increased power absorption by biological tissues, which not only affects power transfer efficiency but also raises concerns regarding safety limits and regulatory compliance. Particularly, for the power coil link, higher frequencies introduce increased switching losses and pose challenges for the subsequent power conversion stage. Therefore, an optimal frequency of operation exists that maximizes the WPT efficiency through biological media by balancing these effects [4]. The frequency range of 1–30 MHz is generally considered optimal for effectively powering medical implants without heating surrounding tissues [5, 6], though other frequency bands have also been explored to meet specific design requirements, such as 2 MHz [7], 50 MHz [8]. Lower frequency bands such as the 6.78 MHz [9,10], and the 13.56 MHz [11–13] band have been widely used in prior work due to their lower attenuation in tissue and relatively easier circuit implementation. However, the low operation frequency results in lower received power and larger resonant component sizes. In contrast, higher operating frequencies within the ISM band, such as 433.92 MHz or 915 MHz, degrade the power conversion efficiency (PCE) during the AC to DC rectification stage due to higher switching losses, which are proportional to the operation frequency. While recent research has explored the feasibility of wireless power transfer at 40.68 MHz for implantable systems [14, 15], these investigations have primarily focused on the design of power conversion circuits rather than the design and optimization of the inductive link itself. A comprehensive study of a complete wireless power transfer link operating at 40.68 MHz, including the implant power conversion chip, is currently lacking. This chapter investigates this and demonstrates a design that achieves a favorable balance between power transfer efficiency and power conversion losses in the load circuitry.

Using 40.68 MHz instead of 6.78 MHz or 13.56 MHz for the inductive power link also offers the potential for higher data rates when incorpo-

rating a data downlink on the same carrier frequency. This can be beneficial to reduce the number of separate wireless links needed in the implantable system and reduce the overall footprint [16–18]. This concept is briefly introduced in this chapter and further elaborated in Chapter 3.

Another key aspect that affects the link efficiency is the geometry of the Tx and Rx coils. While the characterization and design of efficient inductive power transfer links have been extensively studied [19, 20], optimization of implant coil geometry for neural prostheses, considering all factors affecting link efficiency, remains relatively unexplored. Previous works [21, 22] have addressed Tx and Rx coil design and optimization in the low MHz range, these studies often assume air as the coupling medium, neglecting the impact of tissue, particularly at higher frequencies like 40.68 MHz. While some research [23–25] has incorporated tissue losses into coil link models, building upon the methodology in [21], limitations remain. Specifically, [21] treats the operating frequency as a discrete parameter, potentially deviating from its optimal value for a given geometry. Furthermore, optimizing multiple coil parameters simultaneously (e.g., frequency, radius, number of turns, trace spacing, and coil width), as opposed to the two-variable sweep (coil width and fill factor) employed in [21], increases the complexity of the optimization problem and can lead to excessive simulation time due to slow convergence of electromagnetic (EM) simulators. Therefore, a guided EM-based iterative optimization process is necessary to mitigate this complexity. This chapter demonstrates that careful design of coil geometry and appropriate frequency selection enables the achievement of wireless power transfer (WPT) efficiencies exceeding those reported by previous studies employing comparable coil dimensions but operating at lower frequencies. The experimentally validated results from a fabricated coil link prototype are also presented.

Finally, establishing a high-speed wireless data link (>10 Mbps) from an implantable device to the external world presents significant challenges. While inductive coupling is efficient for power transfer, it is typically limited in supporting such high data rates using conventional approaches, and the limitations come from the quality factor and the relatively low carrier frequency, as defined in the Eq.(2.1):

$$BW = \frac{f_C}{Q} \tag{2.1}$$

where BW is the bandwidth of data communication, f_C is the carrier frequency, and Q is the quality factor of the primary (Tx) coil. A higher quality factor improves the power transfer efficiency of the wireless link but significantly restricts the achievable data rate [26]. As an example, backscattering communication [18] is commonly employed in uplink data transmission due to its low energy requirements and minimal hardware complexity. However, since the conventional backscattering

technique transmits data through the same high-quality-factor power link and it relies on the power carrier frequency tone, this introduces a substantial blocker for the uplink signal and restricts the achievable data rate. Alternatively, ultra-wideband (UWB) communication uses very short pulses that are spread across a broad frequency spectrum, typically spanning several gigahertz, thereby enabling high data rates. The use of short pulses necessitates high center frequencies, which in turn facilitates the design of smaller antennas, making UWB communication particularly suitable for miniaturized implantable systems [27]. Furthermore, the pulse-based approach [28] (more details in Section 3.3.1) in UWB communication reduces the power consumption in the implanted transmitter, achieving low-power operation. This chapter introduces the design of a small antenna for UWB data uplink communication. The antenna is designed to maximize the achievable data rate within the severe size constraints of the retinal implant. The experimentally validated results from a fabricated prototype are also presented.

The organization of this chapter is as follows: Section II introduces the fundamental theory for power transfer efficiency. Section III and Section IV describe the design and optimization procedure of the power coil link and the uplink data telemetry link, respectively. Section V presents the measurement results of the fabricated coil link and a benchmark comparison with the state-of-the-art. Finally, conclusions are drawn in Section VI.

2.2 Background on Power Transfer Efficiency

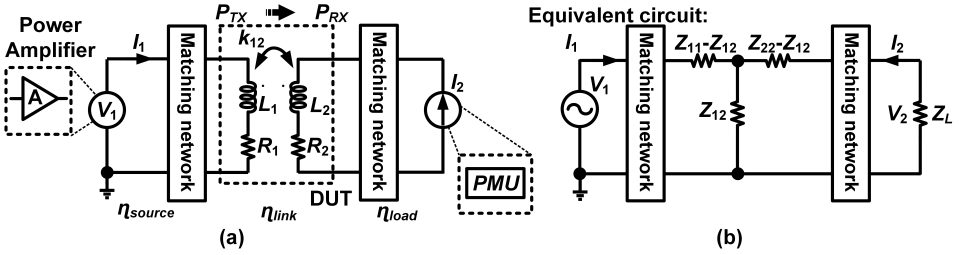


Figure 2.2: (a) Typical structure of a 2-coil wireless link for implant systems, and (b) The equivalent lump circuit model for impedance analysis.

This section derives the maximum achievable efficiency of a typical 2-coil wireless link for implant systems, as shown in Fig. 2.2(a). The circuit model consists of a power source (V_1, typically implemented by a power amplifier), matching networks on both the Tx and Rx sides, the inductive link under investigation, and an output load (I_2, typically implemented

by a power management unit). The end-to-end power transfer efficiency is defined in the Eq.(3.9):

$$\eta_{link} = \frac{P_2}{P_1} \tag{2.2}$$

where P_2 is the power delivered to the load (I_2) and P_1 is the power provided by the source (V_1). The end-to-end power efficiency consists of three parts, the source-to-link efficiency η_{source}, the link efficiency η_{link}, and the link-to-load efficiency η_{load}, as defined by Eq.(2.3)

$$\eta_{tot} = \eta_{source} \times \eta_{link} \times \eta_{load} \tag{2.3}$$

The source efficiency is usually determined by the efficiency of the power amplifier used in the transmitter, including its matching network. The link efficiency is determined by the ratio of the Rx coil output power divided by the Tx coil input power (P_{TX} and P_{RX} in Fig. 2.2). The load efficiency represents the power transfer efficiency of the matching network at the Rx side. η_{source} and η_{load} can be improved by proper design of the impedance matching network and can be close to 100% when the matching network only consists of capacitors [4], whereas η_{link} can be optimized through several approaches, including the optimization of Tx/Rx coil geometry, medium modification (affecting its conductivity and permittivity) [29], and implementing additional intermediate EM-field-guided resonator stages [29]. The end-to-end efficiency can be quantitatively evaluated using impedance parameters derived from the equivalent lump circuit model shown in Fig. 2.2(b):

$$\begin{aligned} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} &= \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \\ &= \begin{bmatrix} R_{11} + iX_{11} & R_{12} + iX_{12} \\ R_{21} + iX_{21} & R_{22} + iX_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \end{aligned} \tag{2.4}$$

where $V_{1,2}$ and $I_{1,2}$ represent the voltage and current ports at the Tx and Rx sides, R and X represent the real and imaginary parts of the equivalent impedance. It has been shown that the maximum achievable power transfer efficiency through the link depends only on the two-port parameters when neglecting the matching network [4]. The general form for the link efficiency is given by

$$\begin{aligned} \eta_{\text{link}} &= \frac{k_{12}^2 Q_1 Q_2^*}{1 + k_{12}^2 Q_1 Q_2^*} \times \frac{R_2^*}{Z_L + R_2^*}, \\ \text{where} \quad R_2^* &= \frac{R_2}{Q_2^2 + 1}, \quad Q_2^* = \frac{Z_L}{Z_L + R_2^*} \times Q_2 \end{aligned} \tag{2.5}$$

where k_{12} is the coupling coefficient, $Q_{1,2}$ is the quality factor of the coil, R_2 is the series resistance of L_2, and Z_L is the loading impedance. If the

optimal load Z_L is used (either by using matching networks or by using multiple coil designs [30, 31]), the maximum link efficiency expression can be simplified to

$$\eta_{\max} = \frac{\xi}{\left(1+\sqrt{1+\xi}\right)^2}, \quad \text{where} \quad \xi = \frac{X_{12}^2 + R_{12}^2}{R_{11}R_{22} - R_{12}^2}$$

The following section details the design and optimization procedure used to determine the WPT coil geometry, subject to a defined set of constraints, to maximize Eq.(2.3).

2.3 Power Coil Link Design for WPT and Data Download

The goal is to design a Tx-Rx coil link and optimize it to maximize its PTE while satisfying the design constraints of a future epiretinal implant. To mimic the human eye environment, two spiral coils with a nominal 14 mm separation distance (consisting of 5 mm in air and 9 mm in tissue) are modeled and simulated in the high-frequency structural simulator (HFSS) from ANSYS (Canonsburg, PA) - see Fig 2.3(a). The electromagnetic model includes a power coil link with a Tx power source and an Rx power receiver. The power Rx coil is placed behind the lens, working as the power receiver to supply the implanted chip that is fixed to the retina clip at the back of the eye. Two interconnection wires (8 mm 29 American Wire Gauge (AWG) copper wire and 2 mm 25 μm gold bonding wire) tether the power Rx coil to the chip implant. The coil pattern of the power link is shown in Fig. 2.3 (b). The tissue environment is modeled along with the coil link. The EM properties of different parts of the human eye needed for the model are frequency dependent (see Fig. 2.4 for the retina layer). The values at 40.68 MHz are used in the model and summarized in Table 2.1. More details and information about the EM properties of the eye can be found in [32].

2.3.1 Power coil design and optimization procedure

Design constraints: The geometry of a spiral coil is defined by five key parameters, with design constraints imposed either by manufacturing limitations or implant size requirements: (i) the inner radius $r_{1,2}$ (or equivalently, the outer diameter $d_{1,2}$, where d_2 must be < 16 mm), (ii) the trace width $w_{1,2}$ (> 0.15 mm), (iii) the trace spacing $s_{1,2}$ (> 0.15 mm), (iv) the number of turns $n_{1,2}$, and (v) the trace thickness $t_{1,2}$ (fixed at 35 μm), as illustrated in Fig. 2.3(b). For simplicity, the design algorithm assumes that the Rx is perfectly aligned at the center of the Tx coil, as shown in Fig. 2.3(a). Fig 2.5 illustrates the design procedure for the inductive powering coil link and the optimization steps undertaken to maximize power transfer efficiency (PTE). This process begins with the application

of design constraints derived from either manufacturing limitations or the surgical requirements of the target retinal prosthesis application.

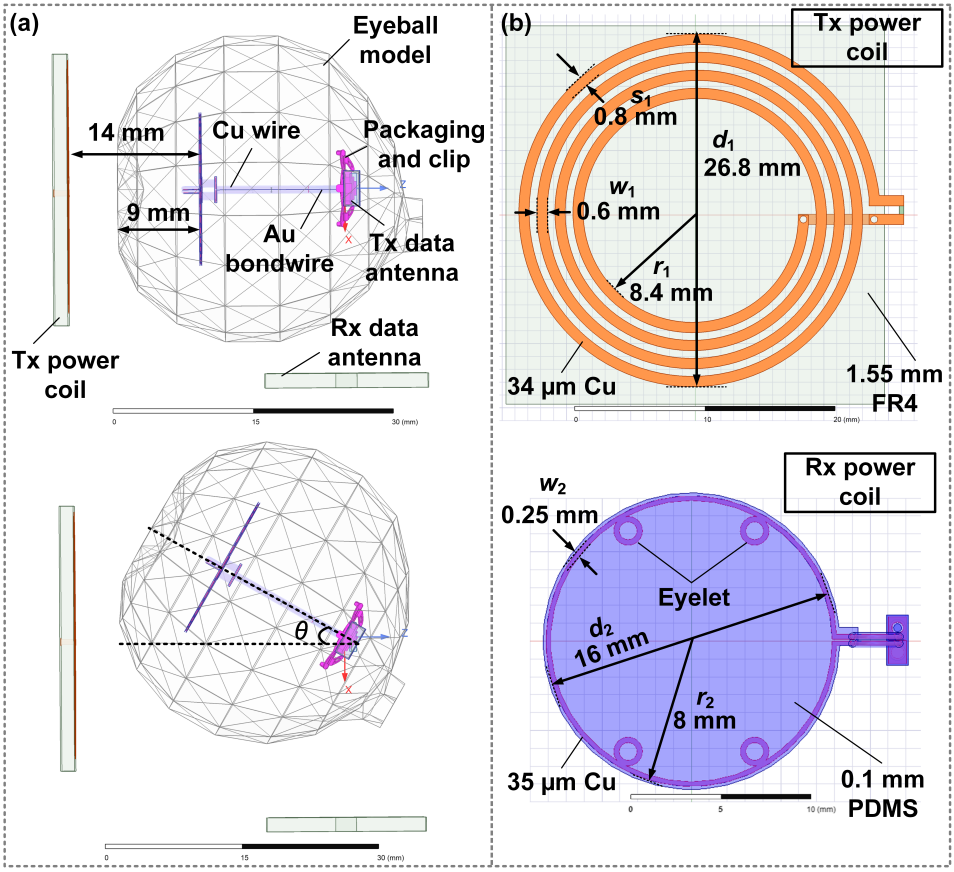


Figure 2.3: (a) HFSS simulation model of the inductive wireless powering system in a human eye model (w/o and w/ rotation), and (b) Top view of the Tx and Rx power coils.

The primary constraints on the coil design arise from the Rx coil (L_2), which, in this application, is implanted within the eye. L_2 can be implemented as either a separate coil [1, 25, 33] or integrated on-chip [4, 27, 34]. While on-chip coils offer a significantly reduced volumetric form factor (by more than two orders of magnitude), their overall power transfer efficiency (PTE) is limited to unacceptably low levels (below 0.1% as reported in [34]) due to factors such as weak coupling, increased parasitic components, and substrate losses [4, 35, 36]. This restricts their applicability to very short-range (several mm) communication or ultra-low power (several μW) devices. Conversely, a separate coil provides

Table 2.1: Dielectric Properties of Human Eye Tissue media at 40.68 MHz

Item	Mass density [kg/m^3]	Relative permittivity [(F · m^{-}1)/(F · m^{-}1)]	Conductivity [S/m]
Vitreous humor	1170	69.202	1.5026
Lens	1100	69.868	0.57168
Retina	1050	87.337	0.86187
Cornea	1076	104.86	0.96684

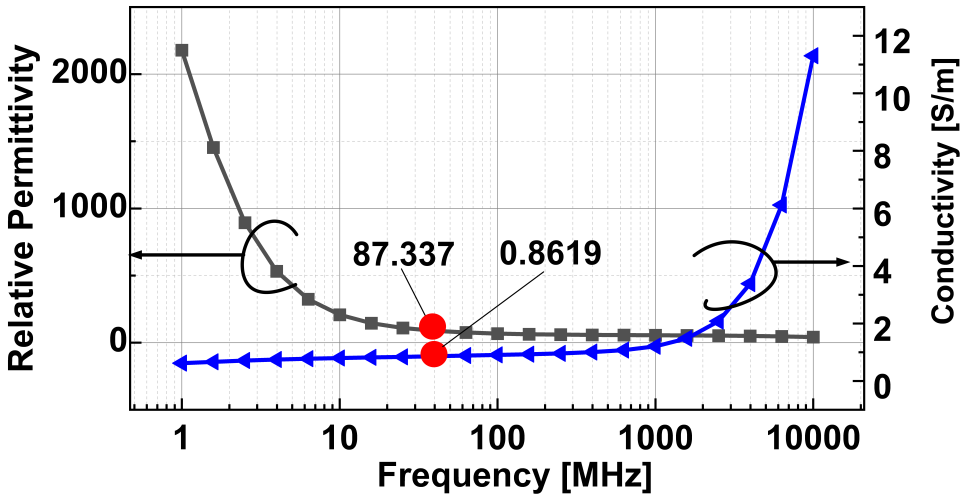


Figure 2.4: The frequency-dependent dielectric properties of the retina layer. At 40.68 MHz, the relative permittivity and the conductivity are 87.337 and 0.8619 S/m, respectively

greater flexibility in placement and offers a higher Q-factor, significantly impacting the overall PTE. Therefore, a separate coil design is adopted here. Given that L_2 is positioned behind the lens, its outer radius r_2 and number of turns n_2 are constrained by the surgical incision size (approximately 5 mm). The final version of the implant will use Nitinol coils to make it possible to be folded when inserted through the eye slit during surgery, which constrains the coil thickness to 35 μm. Considering material properties and surgical constraints, the outer diameter r_2 of the Rx coil is limited to 8 mm, and the number of turns n_2 is restricted to 1. For simplicity, the initial proof-of-concept presented in this chapter uses a standard FR4 PCB for both Tx and Rx coils. Although wire-wound coils are an alternative, PCB-based coils are preferred due to their ease of

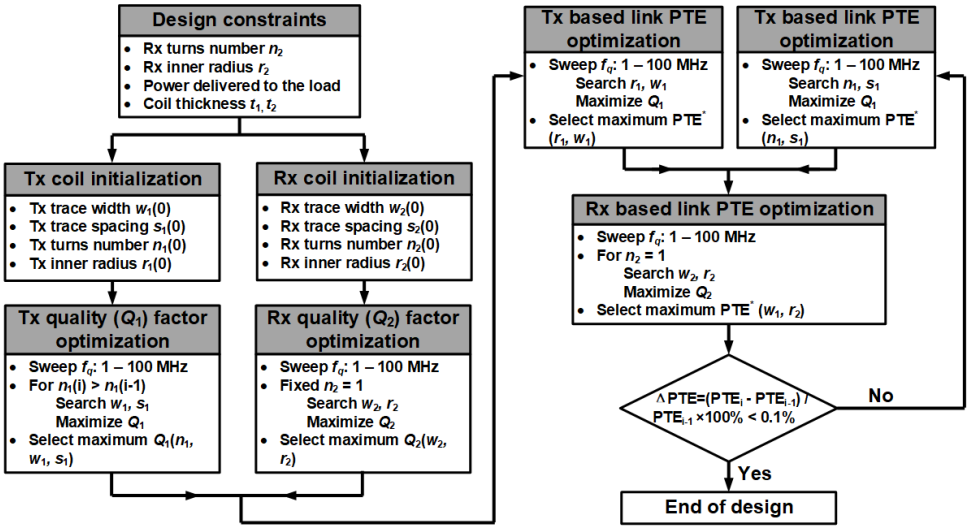


Figure 2.5: The flow chart of the design and optimization procedure for the proposed inductive powering link.

modeling, and improved integration with the test chip [4]. Beyond physical constraints, the power delivered to the load is determined by the application requirement (approximately 5 mW in this case). Assuming a 1V DC output voltage, a 200 Ω resistor is used as the nominal load.

The design constraints for the transmitting (Tx) coil (L_1) are less stringent than those for the Rx coil due to its placement on eyeglasses, allowing for greater design flexibility. L_1 and L_2 are designed to be positioned coaxially and coplanar, separated by an air-tissue interface.

Initialization: The Tx-Rx coil dimensions are initialized based on the design constraints mentioned above. While the inner radius of the Tx coil L_1 is a design parameter influenced by the Rx coil L_2 dimensions, the width $w_{1,2}$, trace spacing $s_{1,2}$, and number of turns $n_{1,2}$ of both coils are subject to optimization. Initially, both inner radii are set to 8 mm (the maximum allowed size for the Rx coil) to maximize the magnetic field strength. The initial trace width and spacing are set to the minimum values allowed by the fabrication process. Similarly, the initial number of turns for both coils is set to one. Optimal operating frequency selection is coupled with coil size optimization, as it depends on coil dimensions, substrate properties, and the electromagnetic characteristics of the biological medium. Critically, in such near-field communication systems, the optimal frequency is strongly dependent on the Rx coil size, decreasing as the Rx coil size increases. For mm-sized Rx coil pairs, the optimal frequency typically lies within the several hundreds of MHz range [37]. High operating frequencies, such as 144 MHz [38,39], 400 MHz [40], and

434 MHz [41,42], have been explored for powering implantable systems. However, these frequencies are primarily optimized for on-chip coil integration, where the coil size is limited to approximately 3 mm. As a result, the achievable link power transfer efficiency (PTE) is typically below 5%. Additionally, the increased power conversion losses associated with high-frequency operation further degrade the overall end-to-end efficiency. For instance, [42] presents a three-coil link design comprising a 13.56 MHz intermediate PCB resonator (with 23% efficiency), a 434 MHz on-chip resonator (with 0.14% link efficiency), and a power converter (with 41% efficiency), resulting in an overall efficiency of only 0.013%. In contrast, for cm-sized Rx coil pairs, the optimal frequency typically falls within the several tens of MHz range, such as 6.78 MHz [43], 13.56 MHz [44], and 40.68 MHz [45]. Given that the proposed system employs an external cm-sized Rx coil to enhance PTE and received power, the optimal frequency in this application is expected to be within this range. This work targets 40.68 MHz, one of the highest available ISM band frequencies within the typically utilized 50 MHz range. As illustrated in Fig. 2.6, utilizing a higher operating frequency than conventional bands (6.78 MHz and 13.56 MHz) improves system PTE. The PTE initially increases with frequency due to increases in the coupling coefficient k_{12} and the Figure-of-Merit (FoM) $k_{12}Q_1Q_{2L}$, and then decreases gradually as the FoM eventually declines.

Coarse optimization for coil geometry: The optimization process begins by independently determining optimal coil dimensions for the Tx and Rx coils to maximize their respective quality factors across the 1-100 MHz frequency range. This decoupled approach significantly reduces computational complexity and HFSS convergence time by decreasing the dimensionality of the search space. In each optimization step, the number of turns is held constant while the width $w_{1,2}$ and trace spacing $s_{1,2}$ are varied. Convergence time is dependent on the preset accuracy and step sizes. A multi-dimensional gradient descent algorithm yields a coarse estimate of coil parameters, identifying optimal turn number, trace width, and trace spacing, but without considering the coil radius. Separating the quality factor optimization for the Tx and Rx coils, rather than directly optimizing link PTE, offers the advantage of rapidly providing coil dimensions suitable for the selected operating frequency, which can then be further refined using the subsequent steps of this algorithm.

Fine optimization for coil geometry: Building upon the coarse parameter estimations from the previous step, the Tx-Rx link PTE optimization refines these values. This optimization considers the two-port efficiency and incorporates the coil radius ($r_{1,2}$) as optimization variables, in addition to $w_{1,2}$, $s_{1,2}$, and $n_{1,2}$. To manage the increased dimensionality of the search space and reduce computational complexity, these four variables are divided into two groups, each optimized independently, as illustrated in Fig. 2.7. The parameter set yielding the highest PTE within

each optimization procedure is selected, subject to size and manufacturing constraints. This iterative optimization process continues until the achievable PTE converges with a variation of less than 0.1%. The final result yields the optimal coil geometry parameters that maximize PTE at the target operating frequency.

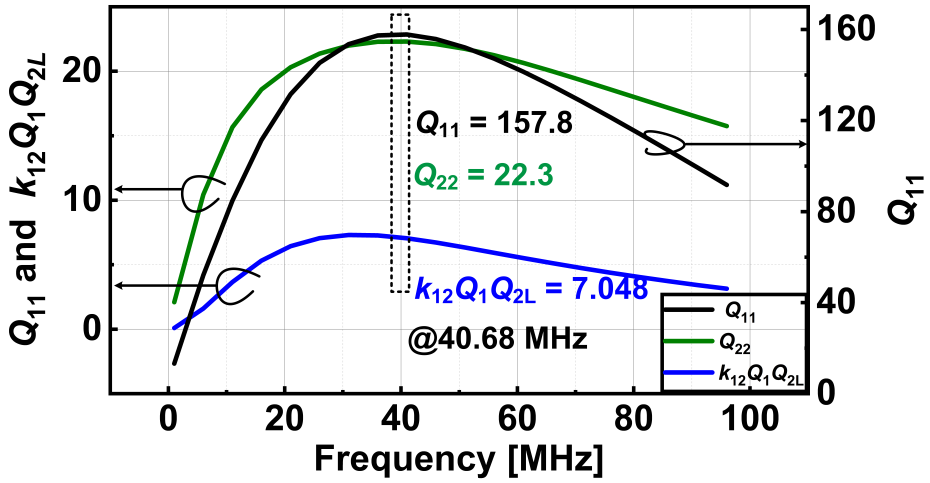


Figure 2.6: The frequency sweep result of Q_{11}, Q_{22}, and $FoM = k_{12}Q_1Q_{2L}$. Both of Q_{11} and Q_{22} reach their peak values at the optimal frequency of 40.68 MHz for a rough estimation of optimal sizes, to reduce the computation complexity.

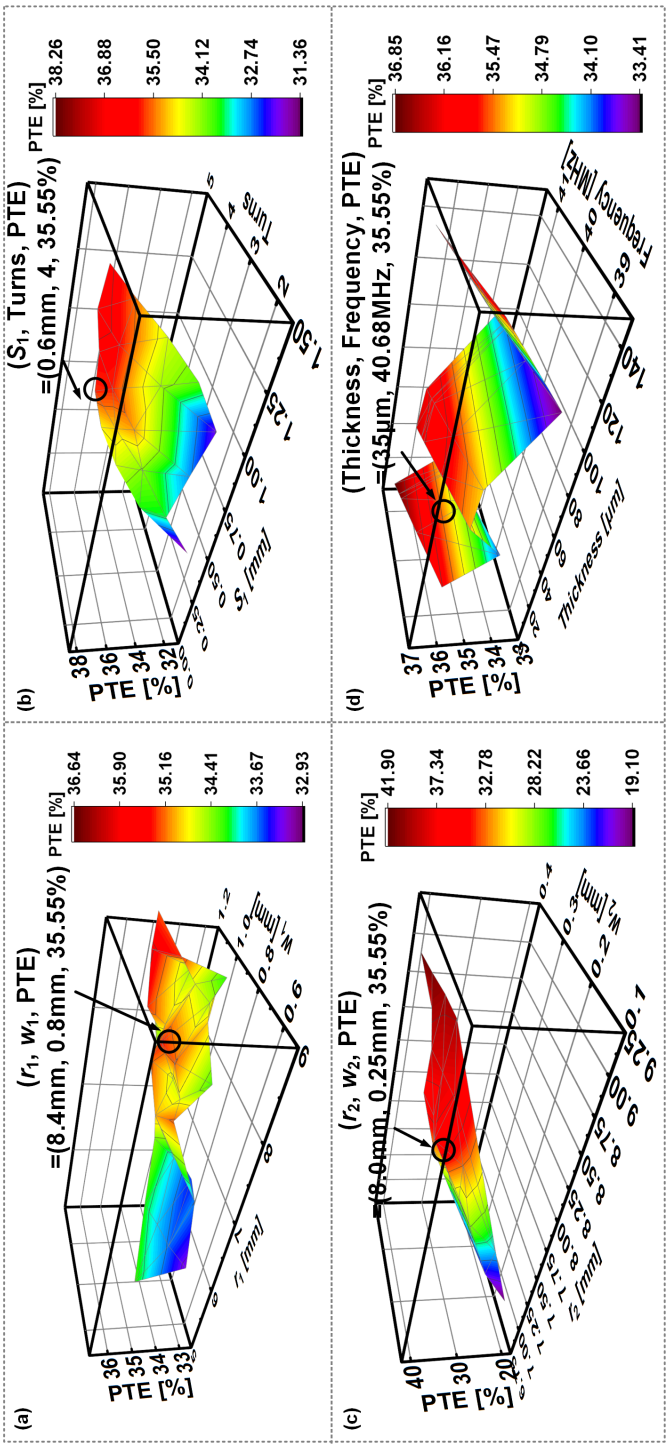


Figure 2.7: The 2-dimension sweep procedure of coil geometry optimization. (a) Simulated PTE versus r_1 and w_1, and the selected point is $r_1 = 8.4$ mm, $w_1 = 0.8$ mm, (b) Simulated PTE versus s_1 and n_1, and the selected point is $s_1 = 0.6$ mm, $n_1 = 4$, (c) Simulated PTE versus r_2 and w_2, and the selected point is $r_2 = 8.0$ mm, $w_2 = 0.25$ mm, and (d) Simulated PTE versus thickness and frequency, and the selected point is thickness = 0.35μm, frequency = 40.68 MHz.

2.3.2 Effect of coils relative position and interconnection wires

Coil separation and misalignment: The coil separation distance, *d*, comprises a 5 mm air gap between the transmitting (Tx) coil (mounted on eyeglasses) and the cornea, and a 9 mm distance through tissue between the cornea and the receiving (Rx) coil. In practice, this separation may vary slightly, impacting link PTE, as demonstrated by the simulation results in Fig. 2.8(a). PTE increases as the separation distance decreases toward 9 mm. At 14 mm separation distance and 0° misalignment, the PTE and coupling coefficient, k_{12}, are 35.55% and 0.0572, respectively. Considering the practical eye rotation range (0° to 15°, indicated by the orange region in Fig. 2.8(b)), these values decrease to 34.53% and 0.0482, respectively. With a 30° rotation, the PTE and k_{12} can further decrease to 24.23% and 0.026, respectively. However, sufficient power delivery remains achievable without exceeding the Specific Absorption Rate (SAR) limit of 1.6 W/kg.

Interconnection wires: The resistance of the two 8 mm copper interconnect cables, connecting the Rx coil to the implant PCB pads, impacts the Rx coil's resistance and, consequently, the link PTE (Fig. 2.8(c)). Selecting the cable diameter requires balancing a trade-off between flexibility and the PTE. Copper wire with a diameter of 254-321 μm (30-28 AWG) offers a suitable compromise, providing sufficient flexibility (better than 24 AWG used in [46]) to minimize pressure on the retina during implantation while maintaining an adequate PTE by reducing interconnection resistance. Additionally, the limited quality factor of the 25μm gold bonding wires, connecting the implant PCB pads to the chip, at the operating frequency also restricts the achievable PTE. Fig. 2.8(d) illustrates the PTE as a function of the bonding wire diameter. Increasing the number of parallel bonding wires can equivalently increase the quality factor of bonding wires, thereby improving the achievable PTE.

2.3.3 Data downlink on power carrier

Downlink data functionality is an essential requirement in neural implant systems. The implementation of the data link depends on several factors, including the link configuration, the required data rate and bandwidth, and the data modulation scheme.

Link configuration: The data downlink can be achieved using either a dedicated inductive link or a shared inductive link. Dedicated inductive links are commonly employed in high-bandwidth and high-data-rate communication systems, typically achieving data rates in the range of several tens of Mbps or higher. For instance, [47] demonstrates a 100 Mbps data transmission using a 2.4 GHz carrier frequency with Ultra-Wide Bandwidth (UWB) communication. However, the drawback of a separate antenna design makes it less appealing. Alternatively, neural implant devices often utilize a shared inductive link for both wireless power and data transfer. This approach benefits from the higher quality factor of

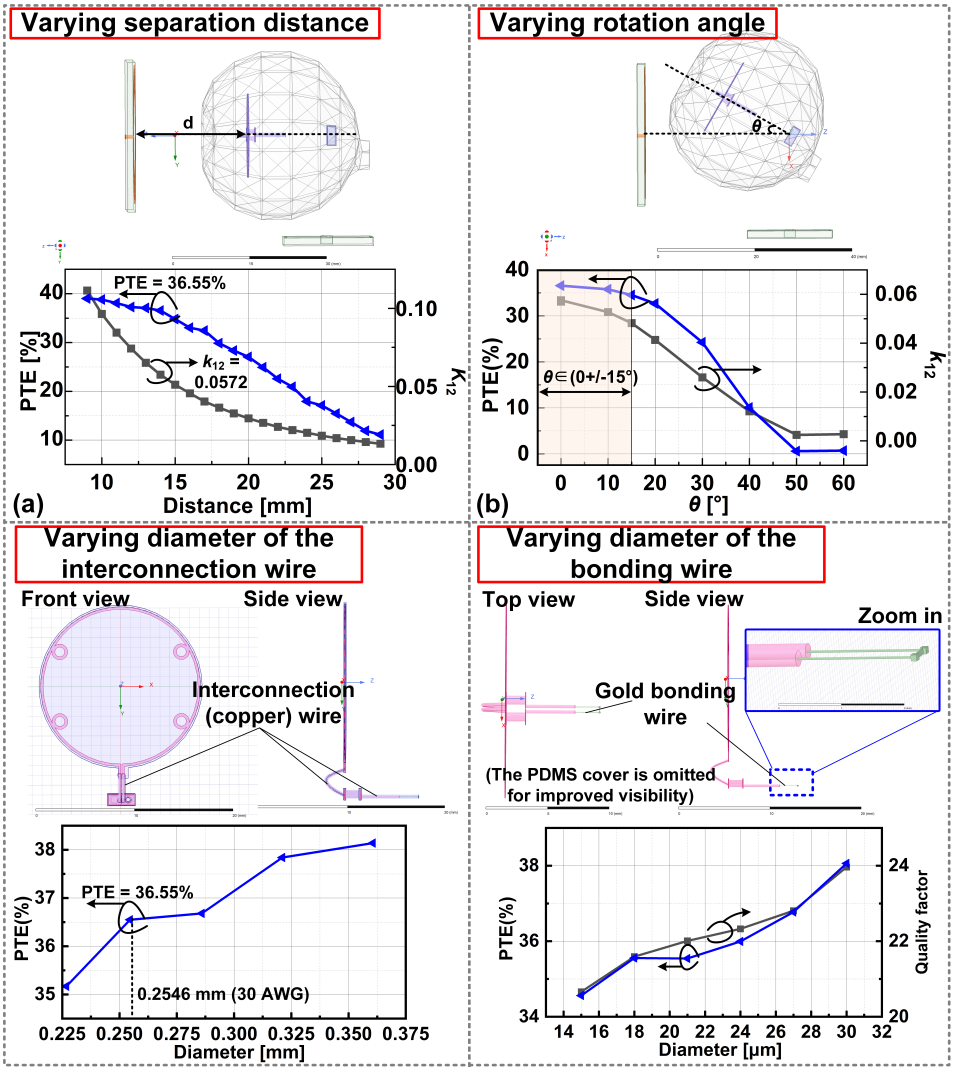


Figure 2.8: (a) The PTE and k_{12} versus coil separation distance (9 mm in tissue and 1-21 mm in air), (b) The PTE and k_{12} versus eye rotation angle, (c) The PTE versus the diameter of interconnection copper wires, and (d) The quality factor of different size Au bonding wires at 40.68 MHz frequency and the relevant PTE simulation results.

the power link but typically supports a lower data rate compared to dedicated link topologies.

Data rate and link bandwidth: The target retinal prosthesis implant sys-

tem requires a data command stream (including a 3-bit preamble and a 23-bit data packet) to configure the states of the wireless chip and retina chip. The total frequency of each configuration operation is approximately 8 kHz. Considering that 26 bits of data need to be sent, the resulting data rate per command bit is around 200 kbps. For successful data modulation, the data rate (f_{data}) must be significantly lower than the carrier signal rate (f_c) and meet the bandwidth requirements. The bandwidth at the receiver side is determined by the quality factors (Q_{Rx}) of the power coils and can be expressed as:

$$\text{Bandwidth} = \frac{f_c}{Q_{\text{Rx}}} \tag{2.6}$$

With $Q_{\text{Rx}} = 22.3$ (as derived in the previous section and illustrated in Fig. 2.6), the resulting bandwidth is 1.82 MHz. This bandwidth is sufficient to accommodate the required data rate of 200 kbps.

Modulation scheme: Common modulation methods include Amplitude Shift Keying (ASK), Phase Shift Keying (PSK), and Frequency Shift Keying (FSK), along with their respective variants. Among these, ASK modulation is particularly well-suited for this design due to several advantages: (i) it features the simplest modulation and demodulation circuitry by encoding and decoding information through amplitude variations of the carrier signal; (ii) it preserves the embedded clock frequency and phase, which is critical for system clock recovery; and (iii) It exhibits lower average power consumption compared to FSK and PSK for transmitting low-bandwidth data, owing to the direct modulation of the carrier's amplitude. However, conventional ASK modulation schemes have challenges in achieving reliable synchronization between the clock and the data. To address the clock/data synchronization problem, one solution is to employ a locally generated precise system clock within the Rx implant chip, but this approach necessitates power-intensive Phase-Locked Loop (PLL) circuits and area-consuming oscillator designs. An alternative is to use Manchester-encoded data with ASK modulation [11, 16], which improves synchronization but significantly reduces power transfer efficiency due to the long duration time of flipping data. To achieve a balance between power efficiency and communication robustness, this design adopts Amplitude Shift Keying with Pulse Position Modulation (ASK-PPM) [48] (more details regarding the considerations for topology selection are illustrated in Fig. 3.6 in Chapter 3.2.2). While ASK-PPM reduces the data rate margin compared to conventional ASK—due to the involvement of four pulses per bit transmission—the resulting pulse rate of approximately 800 kbps remains well within the available 2.08 MHz bandwidth.

Importantly, the integration of the data link does not interfere with the coil design, as the coils are primarily optimized for PTE rather than data communication. Therefore, the simplicity and efficiency of the power coil link are preserved.

Further details regarding the implementation of the data downlink scheme, including the more comprehensive survey on modulation schemes, and demodulation techniques, are discussed in depth in Chapter 3.

2.4 Data Antenna Link Design for Data Upload

Similar to the power coil link design process, which focuses on maximizing the PTE at the 40.68 MHz operating frequency, the design of the data uplink antenna aims to optimize S_{21} at the target operating frequency. As discussed in Chapter 2.1, UWB is particularly attractive for short-range, high-speed communication in compact implantable systems. The Federal Communications Commission (FCC) defines the UWB frequency range as 3.1 GHz to 10.6 GHz in the United States (which is used for discussion in this work), whereas in Europe, the allocated frequency range is divided into two bands: 3.4 GHz to 4.8 GHz and 6 GHz to 8.5 GHz [49]. This work targets a center carrier frequency of 4 GHz while strictly adhering to the design constraints imposed by the epiretinal implant system. This frequency selection can ensure minimal interference between commercial wireless bands (5 GHz) and this implantable device. Notably, the specifications in this implant are more stringent for the wireless power delivery than for the wireless data link. Hence, the data antennas are designed to minimize the overall footprint while achieving sufficient performance.

To accurately model the human eye environment, two square loop antennas [50] are designed and simulated in HFSS (see Fig 2.9(a), considering a nominal separation distance (around 5 mm in air and 19 mm in tissue). The square loop shaped antenna is selected to better position it around the wire bonded chip, and the chip PCB can be affixed to the retinal clip at the back of the eye. While the data Tx antenna is placed internally in the implant, the data Rx antenna is externally placed on the leg of the spectacles, as illustrated in Fig. 2.20, forming an orthogonal loop configuration to avoid the null radiation field formed by the Tx antenna.

2.4.1 Data antenna link design and optimization

The geometry of a square loop antenna is characterized by two key parameters: (i) the outer side dimension $d_{3,4}$, and (ii) the trace width $w_{3,4}$ (Fig. 2.9 (b)). For analytical simplicity, the design algorithm assumes that the Tx and Rx antennas are positioned in an orthogonal configuration, with their normal directions perpendicular to each other. Additionally, their center points are aligned along the normal axis of the Rx antenna, as depicted in Fig. 2.9 (a).

To illustrate the design methodology of the data antenna link, Fig 2.10 presents the overall design flow. To simplify the dimension sweep process, the feeding lines in both antennas are omitted during the simula-

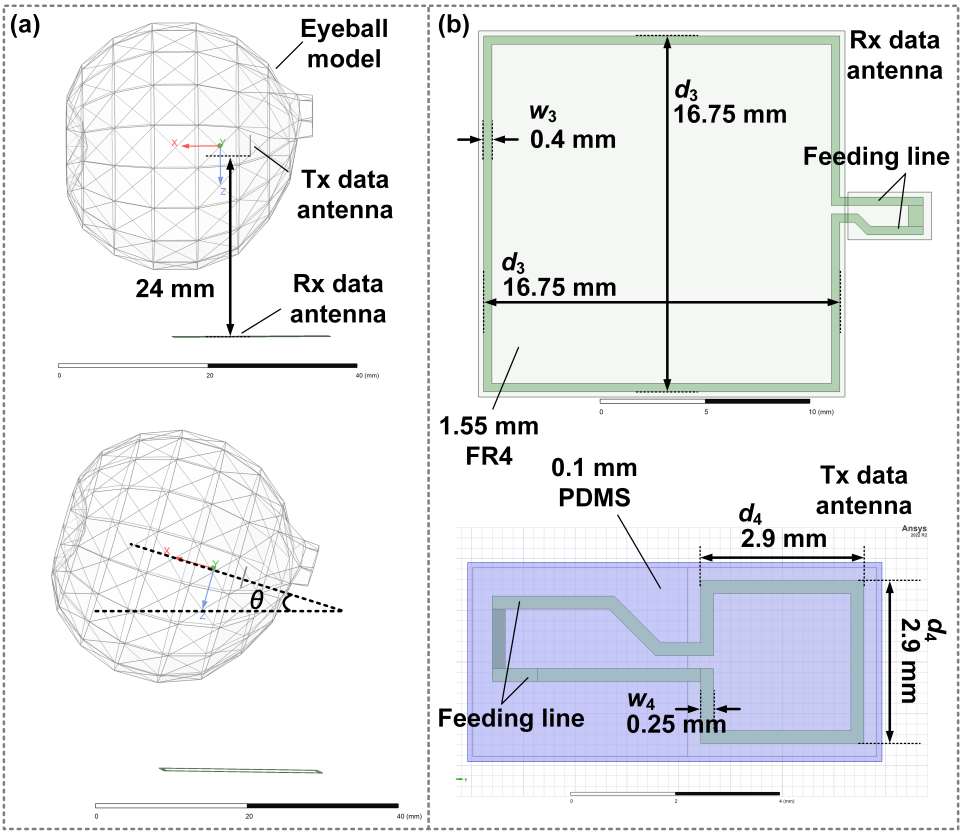


Figure 2.9: (a) HFSS simulation model of the uplink antenna pair in a human eye environment (w/o and w/ rotation), and (b) Top view of the Rx and Tx data antennas.

tions.

Design constraints: There are three design constraints: (i) the Tx data antenna side length d_3 should be less than 3.5 mm to conform to the implant form factor, (ii) the transmitted power of the Tx antenna is limited to be less than -10 dBm, which corresponds to the maximum output power of the Tx driver, and (iii) the antenna thickness is limited to 35 μm (Cu trace).

Initialization: As an initial trial, the geometry of the data Rx antenna is set to be the same as the data Tx antenna. The side length $d_{3,4}$ is swept from the maximum allowable form factor, while the trace width $w_{3,4}$ is initially set to the minimum value specified by the manufacturer.

Optimization: The optimization process involves several iterations to maximize S_{21} at the target 4GHz operation frequency while ensuring

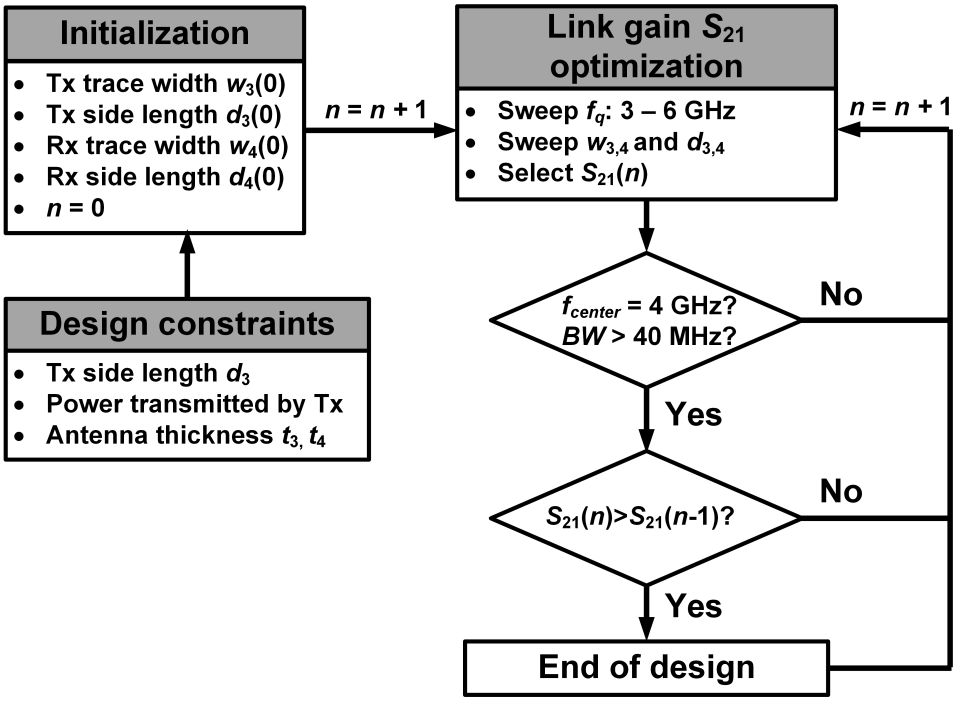


Figure 2.10: The flow chart of the design and optimization procedure for the proposed antenna link for data communication.

sufficient bandwidth to meet the 20 Mbps data rate requirement (Section 3.2). Compared to the power coil design procedure (Section 2.3.1) which involves eight unknown parameters, the data antenna link design requires solving only four variables. As a result, the computational complexity is significantly reduced, allowing for a faster convergence to the optimal solution, as shown in Fig 2.11.

The optimized geometry, represented by Point A, is selected as a potential design choice. However, the antenna dimensions should be adjusted to accommodate the feeding lines for experimental testing. The finalized dimensions for Rx and Tx antennas are shown in Fig. 2.9 (b) top and bottom, respectively.

The sweep result indicates that the link gain S_{21} is mainly constrained by the small Tx antenna aperture, as represented by points A and B. In contrast, the center carrier frequency is mainly determined by the large Rx antenna, as represented by points B and C. These observations can be attributed to the resonant characteristics of the antenna:

$$\lambda = \frac{c}{f_{center}\sqrt{\varepsilon_r}} \tag{2.7}$$

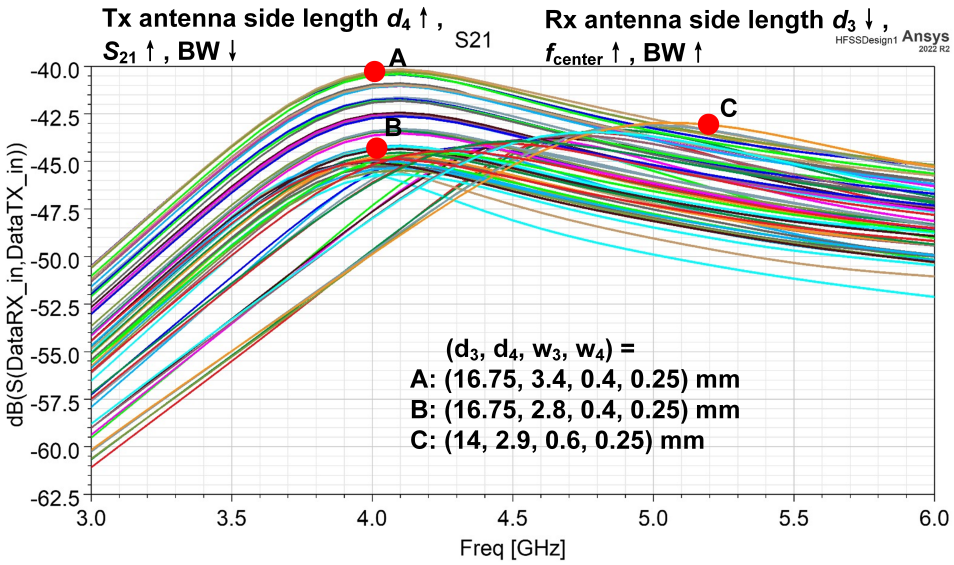


Figure 2.11: The 4-dimension loop antenna geometry sweep result (w/o feeding lines, w/o matching network) with 50 Ω test port impedance. The plot presents the simulated S_{21} as a function of frequency, along with the variations in dimensions $d_{3,4}$ and $w_{3,4}$.

where c is the speed of light in vacuum, f_{center} is the intended operation frequency (4 GHz), ε_r is the relative permittivity in the retina tissue (ε_r = 50.475 at 4 GHz [32]), and λ is the carrier wavelength. For the Tx antenna, the effective circumference is approximately 17.4 mm (as shown in Fig. 2.9(b)), which falls between 10.5 mm (the equivalent wavelength in tissue at 4 GHz) and 18.75 mm (the equivalent quarter-wavelength in air at 4 GHz). The cross-medium transition between air and retina tissue limits its ability to radiate power effectively. For the Rx antenna, the effective circumference is approximately 75 mm, which is sufficiently long to resonate with the carrier wavelength at the intended center carrier frequency.

The bandwidth is determined both by the center carrier frequency and the quality factor, and can be approximated by:

$$BW = \frac{f_{center}}{Q} \tag{2.8}$$

where Q is the quality factor of the loop antenna which is inversely proportional to the circumference of the antenna (as shown by points B and C).

2.4.2 Total gain distribution of the data Tx antenna

Fig. 2.12 presents the total gain distribution of the data transmission antenna. The color gradient represents simulated gain values, ranging from −15.46 dB to −11.23 dB, providing a visual representation of the spatial gain variation. The symmetric, double-lobed radiation pattern confirms its suitability for directional transmission. Peak gain occurs along the main lobe, aligned with the intended propagation direction.

The spatial gain distribution is analyzed over an 80 mm span, encompassing the antenna's designed operational range (the nominal separation of the data Tx-Rx link is 24 mm). The average gain across this region is approximately -13.2 dB, with the highest gain concentration at the center of the main lobes, validating the antenna's efficacy for short-range communication.

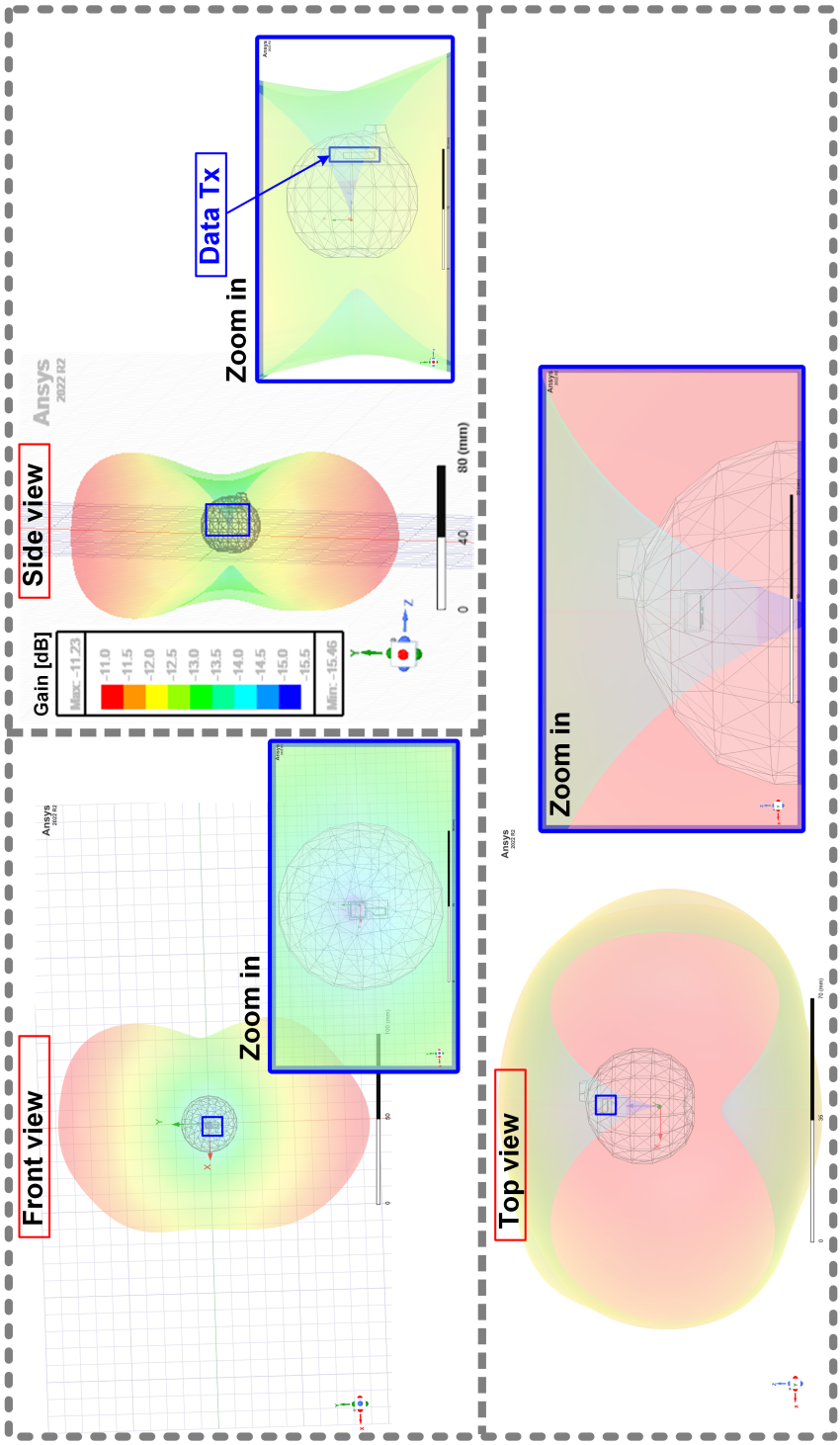


Figure 2.12: The total gain distribution of the data Tx antenna.

2.4.3 Link gain versus antenna relative position

Fig. 2.13 illustrates the simulated S_{21} (link gain) as a function of frequency, accounting for the relative positional changes of the antenna link. Fig. 2.13(a) depicts the simulation model, where the relative positioning of the antennas is affected by the eye rotation angle (θ) and the separation distance (d). This setup effectively replicates the dynamic ocular environment.

Fig. 2.13 (b) presents the simulated S_{21} as a function of operating frequency under varying eye rotation angles ($\theta = 0°, \pm 15°$) and separation distances ($d = 24$ mm, 34 mm). When the eye remains stationary ($\theta = 0°$), the link gain achieves its maximum value of 39.54 dB at 4.0 GHz, with a 3 dB bandwidth spanning 3.5–4.6 GHz; when the eye rotates by ±15°, the link gain degrades negligibly by less than 0.5 dB, attributed to the omnidirectional electromagnetic radiation characteristics of the square-loop Tx antenna. In contrast, variations in the separation distance have a more significant impact on S_{21}, with the link gain degrading by more than 3 dB as the separation distance increases from 24 mm to 34 mm.

Fig. 2.13 (b) also evaluates the achieved link gain to ensure that the received signal at the Rx can be successfully detected by the Low Noise Amplifier (LNA) stage. The -3 dB link gain is around -43 dB. Assuming a Tx antenna input power level P_{Tx} = -10 dBm (200 mV_{pp}), the corresponding output power at the Rx antenna is -53 dB, which should remain above the Rx input sensitivity of the LNA. In this design, a commercial off-the-shelf component (COT) LNA (ADL5611, Analog Devices, Inc) is used, with an input sensitivity of -87.9 dB as specified in the RF signal chain calculator (ADIsimRF, Analog Devices, Inc). Consequently, the resulting link margin of 24.9 dB is sufficient to account for potential additional losses in practical scenarios, such as cable losses, impedance mismatches, eye rotation (Fig. 2.13 (c)), and variations in link separation distance (Fig. 2.13 (d)).

2.4.4 Link gain characterization with impedance matching

Fig. 2.14 presents the simulated scattering parameters and the frequency response of the data antenna link after proper matching.

The Smith Chart (Fig. 2.14(a)) demonstrates moderately good impedance matching at both the Tx and Rx ports to the 50 Ω characteristic impedance, with only minor reactive components that could introduce phase distortions. The proximity of the impedance points to the chart's center also indicates acceptable return loss, promoting efficient signal transmission.

The frequency response (Figure 2.14(b)) characterizes the system's link gain, which is crucial for evaluating data link bandwidth and performance at high frequencies. Simulation results show a peak link gain of -24.53 dB at the 4 GHz operating frequency. The -3 dB bandwidth is approximately 160 MHz, extending from 3.92 GHz to 4.08 GHz. This

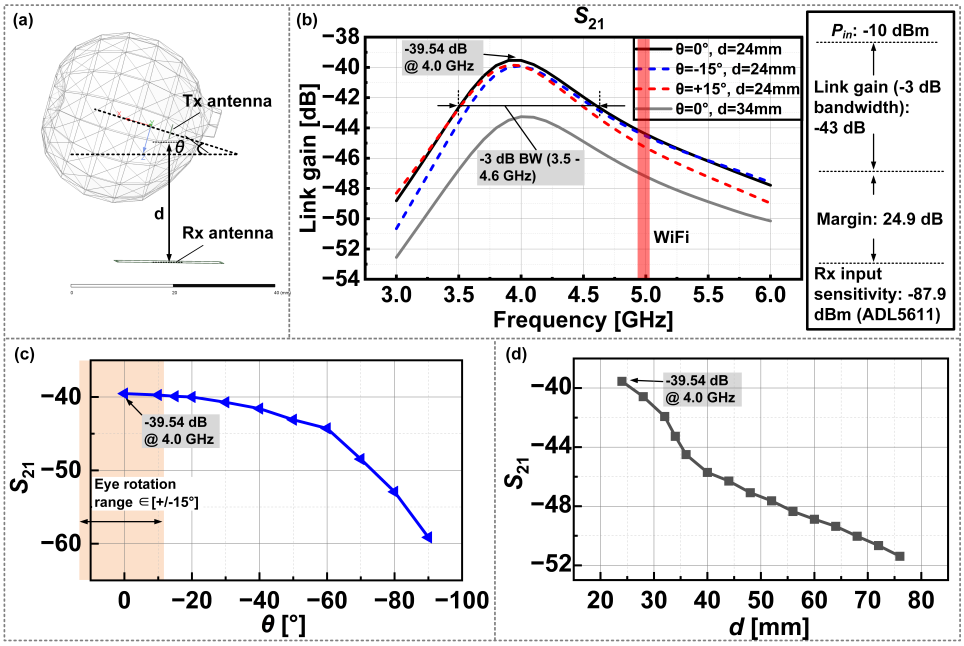


Figure 2.13: (a) The simulation model illustrating the position of the data antenna link embedded within the human eyeball, with the relative position influenced by the eye rotation angle (θ), and the separation distance (d), (b) The simulated S_{21} as a function of operating frequency for varying eye rotation angles and separation distances, (c) The simulated S_{21} at 4 GHz as a function of the eye rotation angle (θ), and (d) The simulated S_{21} at 4 GHz as a function of the link separation distance (d).

bandwidth is suitable for applications requiring moderate data rates and low latency, such as short-range wireless communication or industrial IoT systems. Additionally, the gain curve indicates minimal interference from adjacent frequency bands, such as the WiFi band above 5 GHz.

2.5 EM safety considerations

Transferring power through magnetic fields inherently suffers from substantial signal attenuation in human tissues. Therefore, to ensure patient safety, they must adhere to strict power emission guidelines. Regulatory standards strictly limit human exposure to radio frequency (RF) energy to ensure safety. The FCC has established a maximum averaged Specific Absorption Rate (SAR) of 1.6 W/Kg for human head tissue, measured

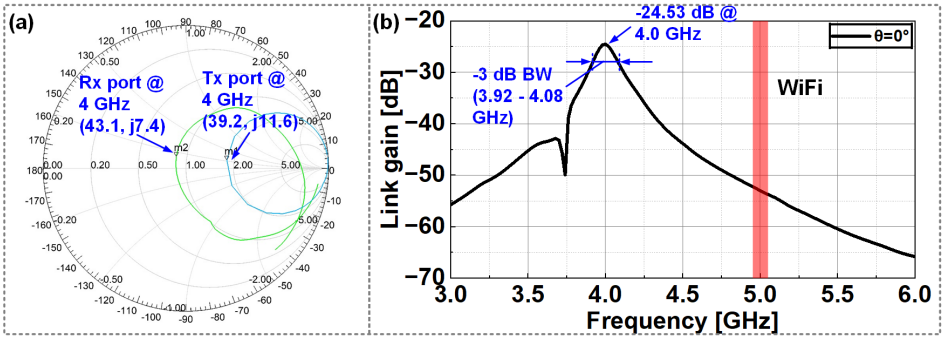


Figure 2.14: Characterization of the data transmission link at 4 GHz (a) Smith chart of S_{11} (Tx) and S_{22} (Rx) with port impedance matched to around 50 Ω, and (b) Link Gain (S_{21}) plot

over a 6-minute duration for a 1-gram tissue sample [51]. The SAR can be mathematically expressed as:

$$SAR = \frac{\sigma |E_{rms}|^2}{\rho} \tag{2.9}$$

where E_{rms} represents the root-mean-square value of the electric field, while σ and ρ denote the electrical conductivity and density of the tissue, respectively. Using Maxwell's equations, the relationship between the electric field E and the magnetic field B can be derived as:

$$\nabla \times E = -\frac{\partial B}{\partial t} \propto \omega_p I_1 \tag{2.10}$$

where ω_p signifies the operating frequency, and I_1 is the current flowing through the system. Based on simulation studies of RF exposure, SAR is often assumed to be proportional to $(\omega_p I_1)^2$. We can conclude that the electric field strength is directly influenced by both the current and operating frequency.

Fig. 2.15(a-b) shows the simulated average SAR distribution within the eyeball model for the entire system, with and without a PDMS isolation layer covering the Rx power coil. The transmitted power levels from the power Tx coil and the data Tx antenna are 17.2 dBm (52.5 mW) (discussed in Section 4.4.3) and -10 dBm (0.1 mW) (discussed in Section 2.6.3), respectively. With the PDMS coating, the peak average SAR across the eyeball is 0.0039 W/kg, located near the retina surface, and the radiated energy is distributed around the Rx coil. Without the coating, the energy concentrates near the coil extension terminals, and the peak average SAR increases to 0.0074 W/kg. The peak SAR with the

PDMS coating remains below the FDA regulation until the total transmitted power from the Tx coil reaches 43.5 dBm (22.4 W), demonstrating a substantial margin under nominal operating conditions (Fig. 2.15(c)). This indicates that electromagnetic losses within the highly lossy tissue medium during nominal operation will not cause a significant temperature increase.

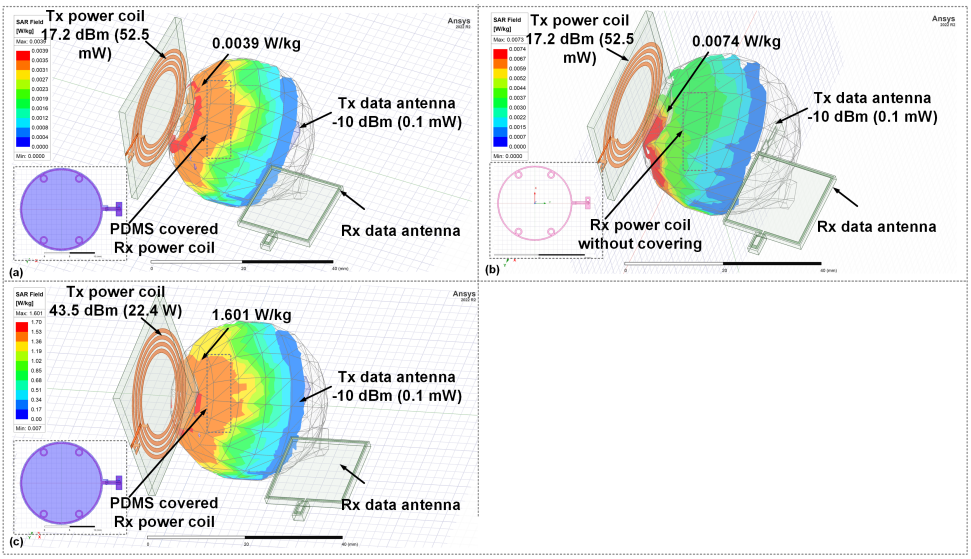


Figure 2.15: The simulated SAR across the eyeball model when (a) the Rx power coil is covered with PDMS layer and the Tx power coil is transmitting 17.2 dBm power, (b) The Rx power coil is not covered with PDMS layer and the Tx power coil is transmitting 17.2 dBm power, (c) The Rx power coil is covered with PDMS layer and the Tx power coil is transmitting 43.5 dBm power to reach the EM safety limitation.

2.6 Prototype Design and Experimental Results

2.6.1 Class-E power amplifier efficiency measurement

Fig. 2.16 (a) depicts the circuit diagram of the class-E power amplifier, which is connected to the transmitter power coil at its output. The selected N-channel MOSFET switch (CSD17484F4) offers several advantages, including low ON-resistance (approximately 180 mΩ), fast switching speed (3 ns turn-on delay and 1 ns rise time), low output capacitance (44 pF), and high voltage tolerance (up to 30 V). The gate bias voltage of

this switch is set to 1 V, which is close to the MOSFET's threshold voltage (0.85 V), to enhance operational efficiency.

A notch filter is employed to suppress the base-band signal's second and third harmonic tones at the output. Both the input and output are impedance-matched to 50 Ω to minimize power reflection. The simulated 1-dB compression point occurs at P_{in} = 4 dBm, as Fig. 2.16 (b) shows. The measured output power when P_{in} = 0 dBm is shown in Fig. 2.16 (c). The S_{21} gain is 20.062 dB which is close to the simulation result.

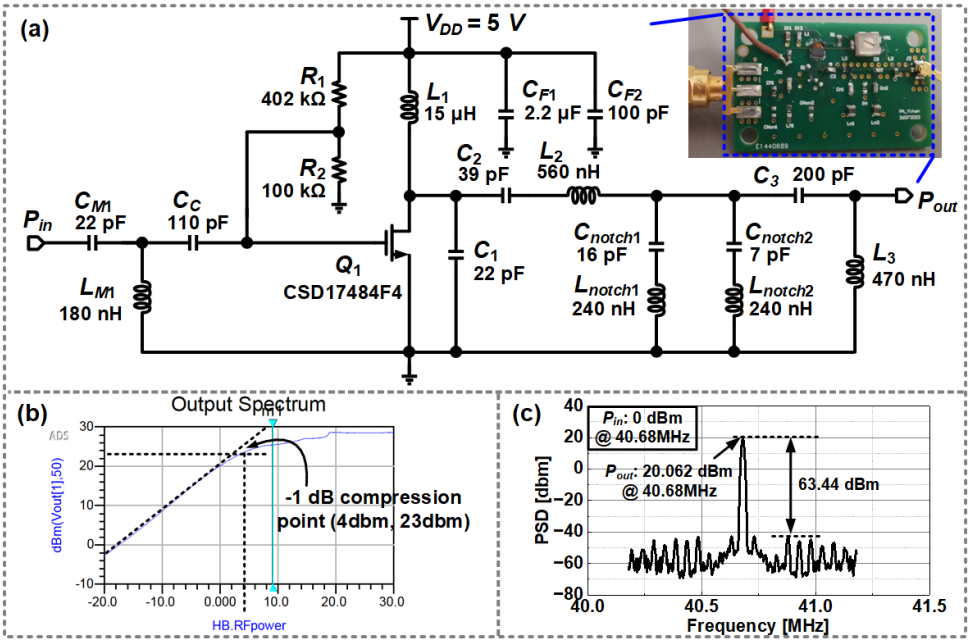


Figure 2.16: (a) The circuit diagram of the class-E power amplifier, (b) The simulated 1-dB compression point, and (c) The measured output power of the class-E power amplifier.

2.6.2 Power coil link measurement

Fig. 2.17(a) shows the experimental setup used to measure coil link parameters with a network analyzer (Keysight P9374A-20GHz). A bare coil measurement (without the resonance capacitor) is performed to characterize the inductor parameters. This is accomplished by converting the measured S-parameters of the inductive link into Z-parameters [52], as illustrated by the equivalent circuit in Fig. 2.17(a). Consequently, the inductance, qualify factor, and coupling coefficient of the link can be derived as follows:

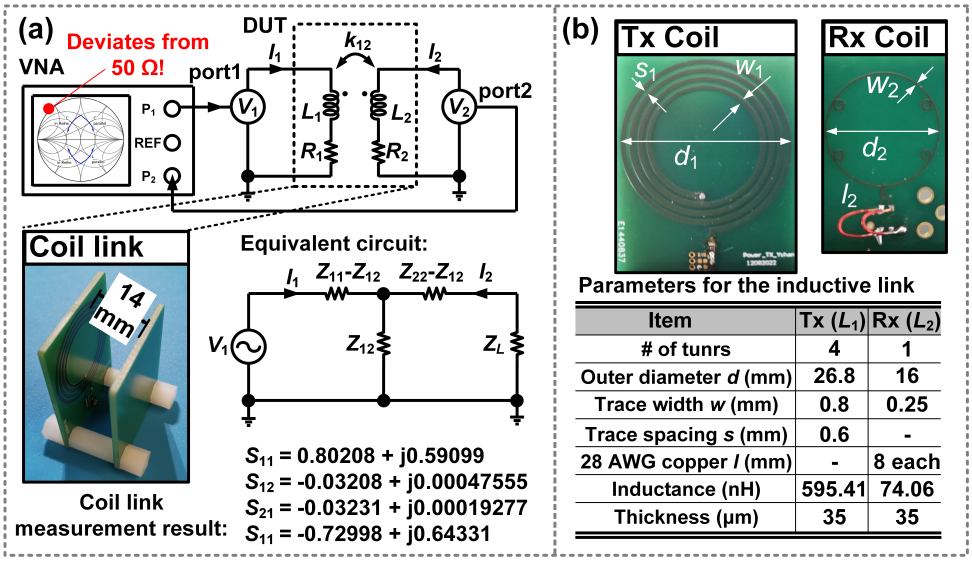
$$L_1 = \frac{\mathrm{Im}(Z_{11})}{2\pi f_q}, \quad L_2 = \frac{\mathrm{Im}(Z_{22})}{2\pi f_q} \tag{2.11}$$

$$Q_1 = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})}, \quad Q_2 = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})}, \quad k_{12} = \sqrt{\frac{\mathrm{Im}(Z_{12}) \cdot \mathrm{Im}(Z_{21})}{\mathrm{Im}(Z_{11}) \cdot \mathrm{Im}(Z_{22})}} \tag{2.12}$$

The inductive coil link (Fig. 2.17(b)), was fabricated on printed circuit boards (FR4). Physical dimensions were chosen based on the HFSS modeling result, as detailed in the table in Fig. 2.17(b). The link is separated by a 14 mm gap in air, center-aligned, and secured using plastic standoffs. The Tx coil has an outer diameter of 26.8 mm with four turns, while the Rx coil has an outer diameter of 16 mm with a single turn, constrained by the surgical incision size. Both coils are connected to SMA connectors for accurate measurement with the calibrated Vector Network Analyzer (VNA). Based on the measured S-parameters and Equations (2.11) and (2.12), key coil characteristics are summarized and compared with simulation results in Table 2.2. The measured inductance is higher than the simulated value for the same geometry due to the longer feed lines between the coil and SMA connectors. These feed lines are intended for the matching network; however, 0 Ω jumper resistors were used for this coil measurement. This discrepancy can also be attributed to the deviation of the impedance of the device under test (DUT) link from the calibrated 50 Ω reference impedance at ports P_1 and P_2. Since the measurement is performed on an inductive impedance, the extracted Z-parameters, converted from the measured S-parameters, for the Tx coil (P_1 port) and the Rx coil (P_2 port) are $Z_{11} = 0.81464 + j152.18801$ and $Z_{22} = 0.76441 + j18.92933$, respectively. Both impedance values exhibit significant deviations from 50 Ω, which can possibly account for the observed variations in the measured inductance and quality factor from the simulated result.

To maximize link PTE, the inductive link should operate in resonance. Fig. 3.26(a) shows the measurement setup to characterize the complete coil link network with impedance matching. A matching network is essential to minimize reflection loss at the transmitter. A simple LC matching network is employed to transform the equivalent inductive link load (R_L) to 50Ω, as shown in the Smith chart in Fig. 3.26(b). Since R_L is smaller than the source impedance, a high-Q inductor is connected in series with the L_1C_1 tank to increase its impedance. This low-loss matching condition is readily achievable due to the commercial availability of high-Q inductors. The S-parameter measurement results in Fig. 3.26(c) demonstrate minimal reflection loss at the transmitter (4.11% reflected energy). Resonance at 40.68 MHz for both Tx and Rx coils is confirmed by the two minima in the S_{11} and S_{22} plots.

Wireless power transfer measurements were performed in both air and tissue mediums to validate link PTE (Fig 2.19(a)). The experimental setup is similar to that in Fig. 3.26(a), with a trimming resistor replacing the loading port and a fixed 13 dBm (20 mW) power source (Agilent N5183B MXG) at the source port. Output power was determined by measuring



Item	Tx (L_1)	Rx (L_2)
# of tunrs	4	1
Outer diameter d (mm)	26.8	16
Trace width w (mm)	0.8	0.25
Trace spacing s (mm)	0.6	-
28 AWG copper l (mm)	-	8 each
Inductance (nH)	595.41	74.06
Thickness (μm)	35	35

Figure 2.17: (a) Inductive link measurement setup, in which Tx and Rx coils were connected to a pair of SMA connectors, and held by 14 mm plastic standoffs in the air medium to measure S-parameters using a network analyzer, and (b) The physical dimensions of the Tx and the Rx coil. The Rx coil consists of a PCB coil and two 28 AWG interconnection wires.

Table 2.2: Comparison between the simulated and the measured results of the coil link

Item		Simulation	Measurement
Tx(L_1)	Inductance (nH)	559	595.41
	Quality factor	133.34	186.82
Rx(L_2)	Inductance (nH)	53	74.06
	Quality factor	19.2	24.76
Separation distance (mm)		14 in air	
Coupling coefficient k_{12}		0.048	0.0523

the voltage amplitude across the load resistor. For tissue simulation, the Rx coil was encased in a 9 mm thick layer of meat, and the Tx coil was positioned 5 mm away. In addition to the PTE calculation based on transient simulation results, the S_{21}-based simulation setup is constructed as shown in Fig. 2.19(b). The S_{21} parameter is utilized to calculate PTE following the approach in [53]:

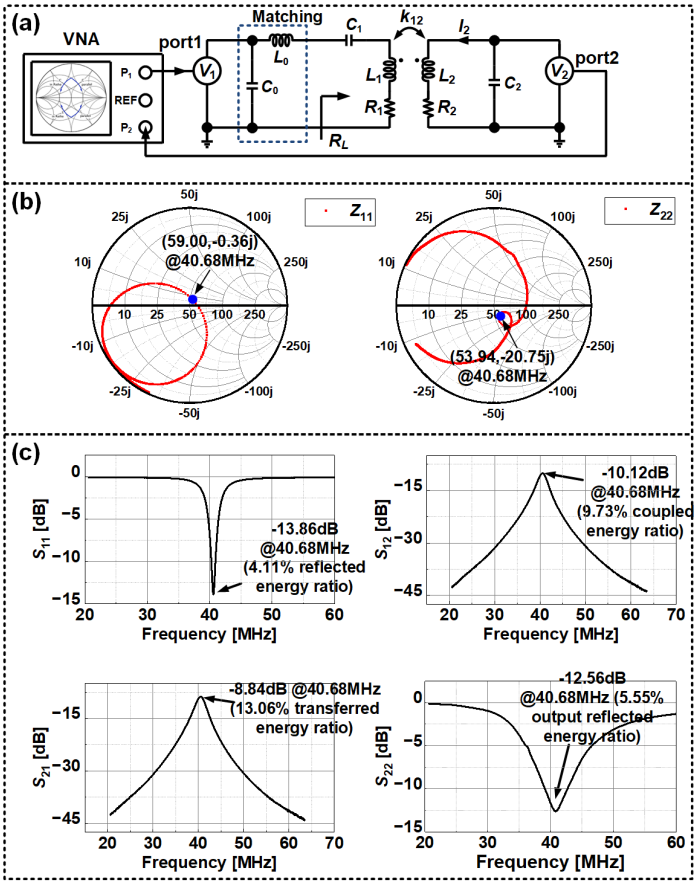


Figure 2.18: (a) Characterization of the inductive link in resonance mode; (b) The Smith chart of two-port measurement results after proper matching; and (c) The S-parameter measurement result shows minimum reflection loss (S_{11}, S_{22}) and high forward gain (S_{21}). S_{21} is identical to S_{12}in the reciprocal network.

$$PTE = 100\% \times |S_{21}|^2 \times \frac{R_L}{50} \tag{2.13}$$

Eq(2.13) is only valid when measuring S_{21} using the load configuration shown in Fig.2.19(b). This calculation method is particularly useful when the operating frequency exceeds the oscilloscope bandwidth, where transient measurements become imprecise. However, in simulation, this equation only considers the frequency response, neglecting harmonic distortion and assuming an ideal 50 Ω source impedance. Consequently,

the simulated PTE based on S_{21} deviates slightly from the transient simulation.

The simulated and measured results are shown in Figure 2.19(c). The transient simulation based result (the blue curve) agrees more closely with measurements, whereas the S_{21} based simulation result exhibits a greater discrepancy (the red curve). The measured link PTE in air (14 mm air gap, the grey line with solid square markers) peaks at 29.28% with a 175 Ω load. This decreases slightly to 28.42% when the air-tissue medium is introduced (black line with open square markers), indicating that tissue absorption does not significantly degrade link efficiency. The measured power delivered to the load (PDL) in the air (black line with star markers) follows a similar trend to the PTE, ranging from 5 mW to 6 mW for loads between 100 Ω and 350 Ω. Fig. 2.19(d) shows the PTE as a function of interconnect wire diameter. These wires connect the single-turn Rx coil (located at the eye's lens) to the chip (placed at the epiretinal layer). The overall quality factor of the Rx coil is proportional to the interconnect wire thickness. Balancing comfort and efficiency, 28 AWG copper wire was selected, resulting in better PTE compared to 29 AWG and 30 AWG wires.

Fig. 2.19(e) illustrates the PTE's dependence on operating frequency. The LC resonator and matching network are designed for 40.68 MHz. A small frequency shift (approximately 0.5 MHz) can degrade efficiency by around 3%. Therefore, the operating frequency should remain stable at 40.68 MHz.

2.6.3 Data uplink measurement

Fig. 2.20 shows the measurement setup for the data telemetry uplink. The antennas were fabricated on FR4 PCB. The Tx antenna aperture (2.9 mm × 2.9 mm) is constrained by the implanted chip form factor and bonding pattern. The Rx antenna is not implanted and has a relatively larger aperture (16.75 mm × 16.75 mm), with less stringent size constraints. The Rx and Tx antennas are separated by a 24 mm air gap, and positioned perpendicularly. The Rx antenna is mounted on a holder 21 mm from the eyeglass lens center, while the Tx antenna is placed on the eyeglass temple. Both antennas are connected to small UMCC connectors (50 Ω impedance) to minimize parasitic effects and electromagnetic interference. Space is provided between the antenna traces and UMCC connectors for matching networks.

Two key link characteristics were verified: the output power at the operating frequency and the forward gain S_{21}. The output power was measured using a spectrum analyzer (Keysight E4446A-44GHz), and forward gain was measured using a network analyzer (Keysight P9374A-20GHz). The measurement results are shown in Fig. 2.21 and Fig. 2.22, respectively.

For the output power measurement, a -10 dBm (0.1 mW) signal was

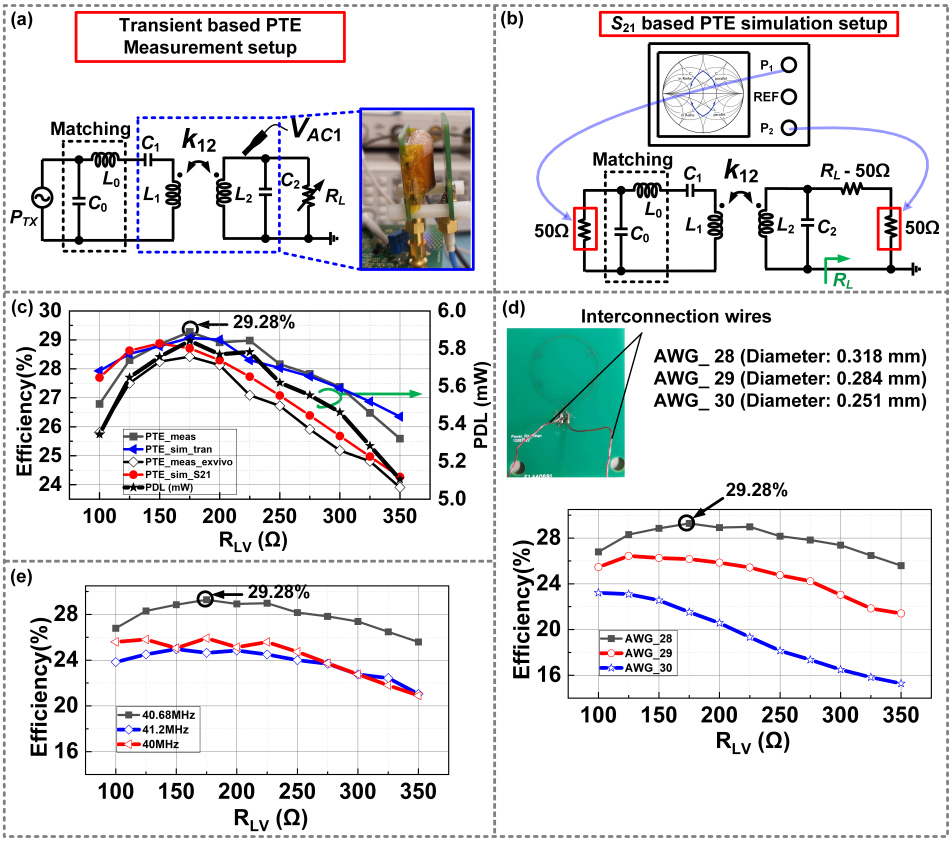


Figure 2.19: Inductive link simulation/measurement setup and the PTE curves. (a) The transient based PTE measurement setup. The Rx coil was wrapped with a 9 mm thick layer of pork to mimic the lossy tissue environment. The Tx coil was spaced from the tissue by 5 mm, (b) The S_{21} based PTE simulation setup using VNA, (c) The simulated and measured PTE and PDL curves versus different loads, (d) The measured PTE as a function of R_{LV} with varying diameters of interconnection wires, and (e) The measured PTE as a function of R_{LV} with varying operating frequency.

input to the Tx antenna using the VNA. The frequency response at the Rx antenna was recorded by the spectrum analyzer. The output signal has a peak amplitude of -38.89 dBm (129.1 μW) at 4 GHz and a noise floor of -74.60 dBm (determined by the average noise level, the resolution bandwidth of the spectrum analyzer, and the noise introduced by the VNA input port), resulting in a link gain of -28.89 dBm (Fig. 2.21). No

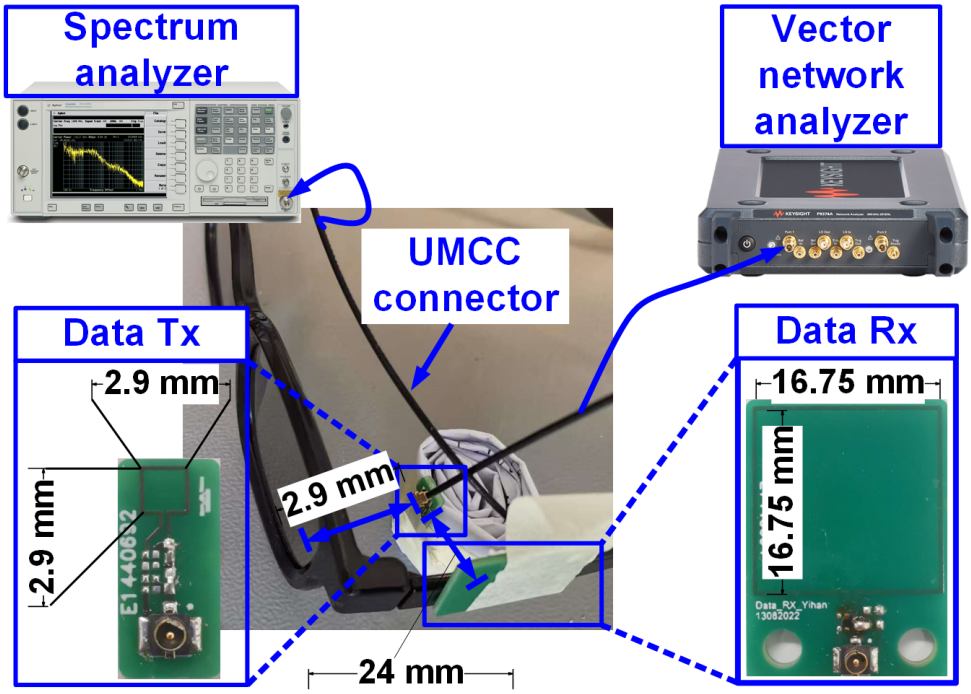


Figure 2.20: Data uplink measurement setup, in which Tx and Rx antennas were placed near an eyeglass. Both the Tx and Rx antenna were connected to a pair of UMCC connectors, and separated by a 24 mm air medium to measure S-parameters and signal powers by using a network analyzer, and a spectrum analyzer, respectively.

significant frequency interference is observed in the selected frequency range (3.95 GHz to 4.05 GHz).

To measure forward gain, both Tx Rx antennas were connected to the VNA ports. The measured S_{21} gain (black curve in Fig. 2.22) peaks at -25.07 dB at 4.08 GHz, with a -3 dB bandwidth from 3.56 GHz to 4.27 GHz, providing a sufficient attenuation for the WiFi band at 5 GHz. Alternatively, forward gain was measured using the spectrum analyzer, similar to the previous output power measurement, but with a frequency sweep (blue curve in Fig. 2.22). Similar to the VNA measurement result, a peak gain of -28.89 dB at 4.00 GHz was observed, with a -3 dB bandwidth from 3.65 GHz to 4.35 GHz. The approximately 3 dB discrepancy between the two curves is primarily attributed to cable and connector losses, as the VNA was calibrated to the UMCC connector ends, while the spectrum analyzer measurement included these losses, reducing its

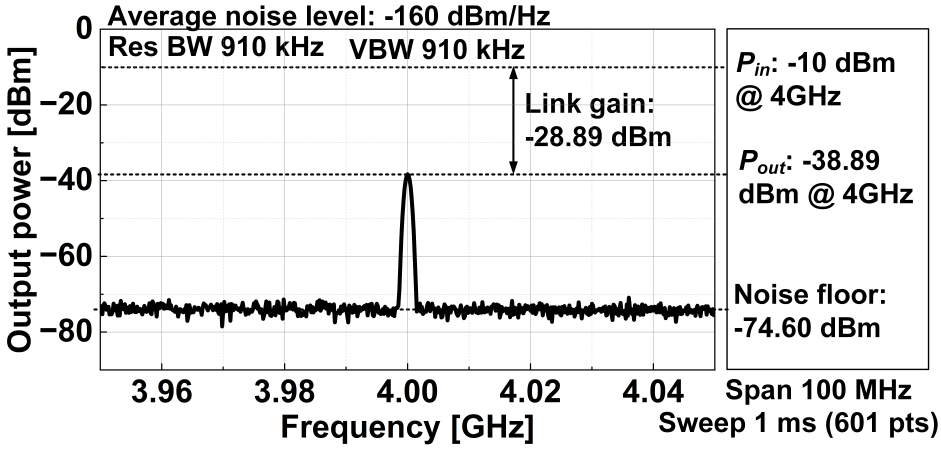


Figure 2.21: The measured power of the receiver signal at the Rx antenna. With -10 dBm of input power level, the output power level is -38.89 dBm, resulting in -28.89 dBm link gain.

accuracy compared to the VNA measurement.

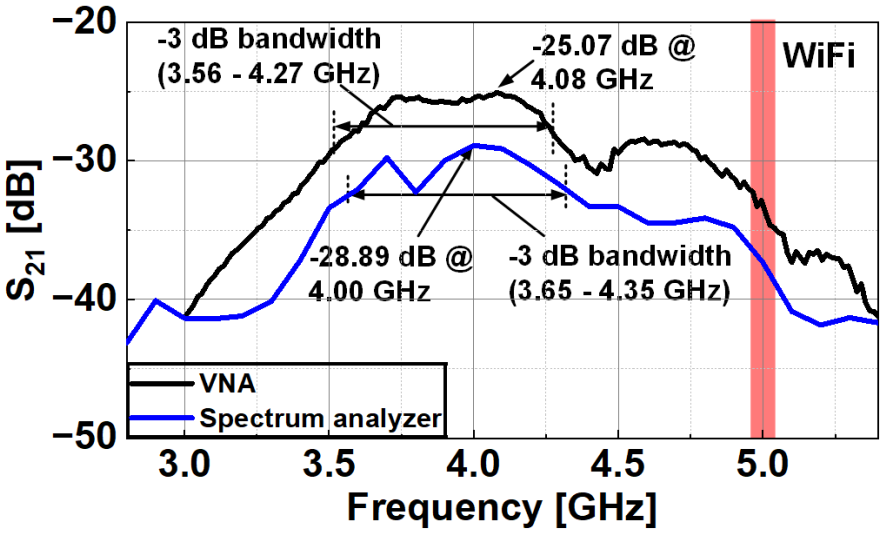


Figure 2.22: The measured link gain of the upload data antenna pair using VNA and spectrum analyzer, respectively. The measured S_{21} gain is maximal (-28.89 dB) at 4 GHz with 0.7 GHz bandwidth, providing sufficient attenuation for the 5 GHz WiFi frequency band.

Fig 2.23 presents the circuit implementation and measurement result of the uplink data telemetry block. This prototype uses commercial off-the-shelf (COTs) components and the custom-designed antenna link. A -10 dBm (200 mVpp) IR-UWB signal is input to the antenna link (-28.89 dB link gain) and amplified by a custom-designed two-stage gain block (Fig. 2.23(a)). The gain block consists of two low-noise amplifiers (LNAs) (ADL5611, Analog Devices, Inc), providing a theoretical total power gain of 40.21 dB from 500 MHz to 6 GHz. Each AC-coupled gain stage is inductively coupled to a 5V/200 mA power supply. Figure 2.23(b) compares simulated (ADIsimRF, Analog Devices, Inc.) and measured results. The simulated power gain is 40.21 dB, while the measured gain is slightly lower at 37.77 dB, resulting in a difference in output power level (1.32 dB simulated vs. -1.12 dBm measured). This discrepancy is attributed to cable losses and matching imperfections.

The measurement setup is shown in Fig. 2.23(c). The input power is provided by the VNA, and the output power is measured by the spectrum analyzer. The operation frequency is 4 GHz, which is the IR-UWB data telemetry carrier frequency, with a 1 GHz span. Results are shown in Fig. 2.23(d). The overall gain at 4 GHz is 12.54 dB. With a -10 dBm input, the gain block output reaches -1.12 dBm, well above the Rx noise floor of -49.62 dBm, ensuring successful data recovery.

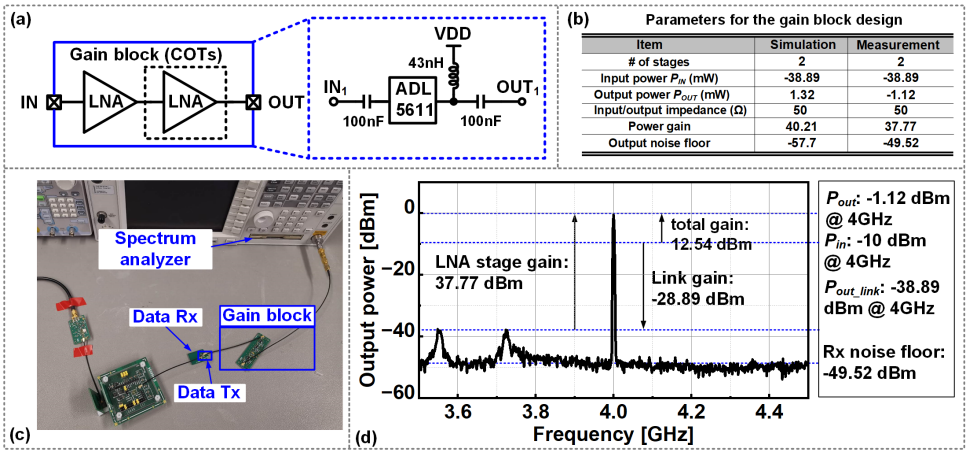


Figure 2.23: The complete uplink data telemetry circuit. (a) 2-stage gain block using commercial off-the-shelf components, (b) Parameters for the gain block design, (c) Implemented hybrid antenna link and gain block prototype, and (d) Measured output power at 4 GHz.

Table 2.3: Benchmarking wireless power transmission and data antenna telemetry on small implants

Item	**TBCAS'16** [47]	**TBCAS'17** [2]	**CICC'19** [18]	**JSSC'20** [27]	**JSSC'21** [54]	**RFIC'22** [55]	**This work**
Power link							
Link type	Inductive (3 power coils+duplex data transceiver)	Inductive (2 power coils+2 data antennas)	Inductive (3 power/data coils)	Inductive (2 power/data coils)	Inductive (2 power/data coils)	ME[1] (3 power coils+ME film)	Inductive (2 power coils+2 data antennas)
Tx diameter (mm)	42 (driver coil) and 20 (repeater coil)	N/A	N/A	N/A	40	4 × 2 (transducer)	26.8
Rx diameter (mm)	10	13.5	0.5 × 0.5 (on-chip square loop antenna)	0.116 (on-chip square loop antenna)	10	0.8 mm^3 ME film	16
Distance	36 mm tissue	N/A	8 mm liquid brain phantom	1 mm air	23 mm Retina implant	20 mm implant	14 mm air
PTE (%)	41.6	N/A	1.4125	1.2×10^{-3}	25	0.2	Max 29.28
PDL (mW)	10.4	18	0.017	0.01	N/A	35.2	Max 10
Frequency	13.56 MHz	2 MHz	30 MHz	5.8 GHz	13.56 MHz	0.34 MHz	40.68 MHz
Data antenna link							
Link type	Inductive	Inductive	Inductive	Inductive	Inductive	Inductive	Inductive
Tx aperture (mm × mm)	10 × 10 (loop antenna)	13.5 diameter (circular antenna)	backscattering	backscattering	backscattering	0.25	2.9 × 2.9
Rx aperture (mm × mm)	N/A	N/A	N/A	2 × 2	N/A	N/A	16.75 × 16.75
Distance	36 mm tissue	N/A	N/A	1 mm air	23 mm Retina implant	Max 60 mm air	24 mm air
Link gain (dB)	N/A	N/A	N/A	-39.2 (simulation)	N/A	N/A	-28.89
Data rate/Bandwidth (Mbps/MHz)	100/N/A	0.5/N/A	10/N/A	0.0042/~350	N/A	0.04/N/A	20/710
Frequency	2.4 GHz	20 MHz	900 MHz	5.8 GHz	13.56 MHz	31 MHz	4 GHz

[1] Magnetoelectric

2.6.4 Benchmark comparison with state-of-the-art wireless implant designs

Table 2.3 summarizes the performance of the proposed inductive link and compares it to other compact wireless designs. Most listed works utilize inductive links for wireless power transfer due to their sufficiently high PTE for discrete coil implantation [47,54], or their compatibility with on-chip integration [18, 27]. While on-chip inductors offer superior integration compared to conventional two- or three-coil approaches, their small aperture limits PTE and power delivery to the load (PDL). The magnetoelectric transducer used in [55] achieves higher PTE than typical inductive approaches, but it requires a complicated film structure at the Rx side of the chip and is limited to lower operating frequencies (100 kHz - 1 MHz) [56]. Instead of three-coil structures or magnetoelectric transducers, this work maximizes the Rx coil quality factor by increasing the operating frequency to 40.68 MHz. With optimized link parameters, this approach achieves a maximum of 29.28% PTE and 10 mW PDL using a simple two-coil inductive link.

For the data link, this work, similar to [2,47,55], separates the uplink antennas (20 Mbps at 4 GHz) from the power/downlink coils (200 kbps at 40.68 MHz) to prevent interference during data telemetry. This separation enables more efficient bidirectional communication. Backscattering, used in [18, 27, 54], eliminates the need for an active uplink transmitter and separate antenna. However, this approach results in lower data rates; for example, [27] reports only a 4.2 kbps uplink rate. With a 24 mm air gap, this work achieves a -28.89 dB link gain at 4 GHz.

2.7 Conclusion

This chapter formulates a general design flow and parameter optimization process for resonant inductive wireless power and data transfer links in biomedical implants, using retinal prostheses as a case study. Finite element models for both power and data telemetry links were developed to validate the proposed concept. Beyond characterizing the link performance concerning angular misalignment and separation distance, the impact of tissue absorption on the electromagnetic field was also evaluated.

Prototype links for the power and the uplink data telemetry were fabricated on PCBs and experimentally validated. VNA characterization confirmed that the power coil link achieves inductance and quality factor values consistent with simulation results. A maximum power transfer efficiency of 29.28% was observed at a 175 Ω load, with only a 0.86% efficiency reduction when the link was separated by the tissue-air medium, ensuring sufficient power for wireless operation. The uplink data antenna link achieved a gain of -28.89 dB at 4 GHz with a 0.7 GHz (-3 dB) bandwidth. A two-stage LNA gain block was used to amplify the weak IR-UWB

signal at the Rx antenna, ensuring successful uplink data recovery.

The experimental results presented in this chapter validate the prototype's ability to perform both wireless powering and data telemetry for implantable applications. The following chapters will focus on integrating the Rx chip with the link design presented here.

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Chapter 3

A 40.68-MHz Wireless Implant System With Bi-directional Data Communication

3.1 Introduction

As mentioned in Chapter 1, the growing demands of modern intelligent neural modulation systems have driven the development of closed-loop control systems, which can generate specific stimulation patterns based on recorded neural activities. Given the strict power and area constraints in implanted devices, a part of the processing and control is often offloaded to an external device. As a result, such systems should be capable of communicating with an external device. Additionally, to support battery-free operation, these systems must be capable of receiving power wirelessly, which introduces several design challenges. There is a trade-off between implant size, power budget, bi-directional communication capabilities, and achievable data rates. Several prior works have explored these trade-offs for different implantable systems. For example, the work in [1, 2] presented a downlink data telemetry for a retinal prosthesis, but no uplink was considered. To gain deeper insights into neural activities and to enable more intelligent control, an uplink function is crucial in such systems. The uplink packet can encode digitized data along with a clock signal (e.g., using Manchester encoding) to ensure synchronization for reliable clock/data recovery. Bi-directional data communication is reported in [3, 4] using an inductive wireless link that also delivers power. However, these systems require an external crystal oscillator to provide an accurate reference clock, decreasing system integration. The work in [5, 6] replaces the external frequency reference with a clock recovered from the power carrier signal to reduce the number of external components. However, to satisfy the high data rate (9 Mbps) uplink communication, these designs use power-hungry (108 μW at 434 MHz) phase-locked loops (PLLs) to generate high-frequency carrier signals. Furthermore, the system requires four antennas in the Rx, limiting integration. Some other works have been presented in [7–10] that achieve successful downlink/uplink communication. Unfortunately, none of them meet our design objectives, which aim to achieve closed-loop power level

control and energy-efficient data telemetry within a compact chip while minimizing the use of external components.

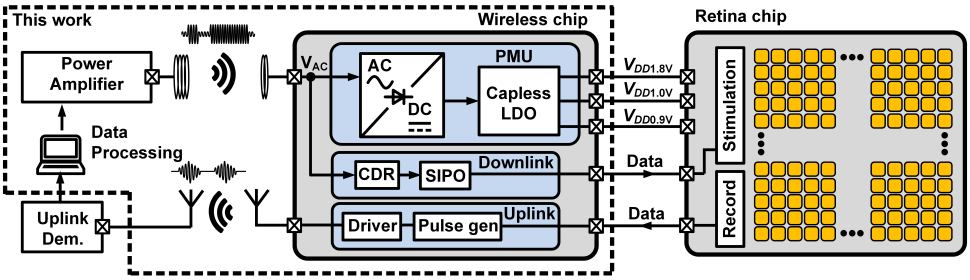


Figure 3.1: System diagram of the proposed wireless implant system featuring bi-directional communication.

In this chapter, we introduce a comprehensive power management and data communication system that minimizes chip area, reduces reliance on off-chip components, and has fully independent supply generation, bi-directional wireless communication capability, and high reliability for implantable devices. The compact Rx chip design (Fig. 3.1) can efficiently perform voltage regulation (realized by the power management unit (PMU)) and clock/data recovery (CDR, realized by the downlink unit) from a 40.68 MHz inductive downlink, and data transmission on a 4 GHz ultra-wideband uplink (realized by the uplink unit). These functions are realized based on the power and data link designs in Chapter 2.

In the proposed system, power is received at the implanted chip by a power Rx coil link working at a resonant frequency of 40.68 MHz. The received AC voltage in the coil is converted into a DC voltage supply by a full-wave rectifier and regulated by a capacitor-less low drop-out regulator (LDO). The same coil carries the 200 kbps downlink data using Amplitude Shift Keying combined with Pulse Position Modulation (ASK-PPM). The source power level and command bits can be regulated and managed by a Class-E power amplifier and a data processing platform, respectively. The uplink data telemetry is performed by an Impulse Radio Ultra-Wideband (IR-UWB) pulse generator and a data Tx coil working at a carrier frequency of 4 GHz. The pulse generator converts the input data into short-duration pulses modulated at UWB frequencies. These pulses are then transmitted through a custom-designed off-chip PCB antenna and received by the external system.

At the circuit level, this work introduces innovations in a dual-loop, any-load-stable regulator in the power management unit, a sampling-based envelope detector in the downlink data unit, and a dual-edge-sensitive IR-UWB transmitter in the uplink unit:

1. For the power management unit, this design employs a full-bridge rectifier and dual-loop, any-load-stable regulator structures to de-

liver three different output voltages (0.9V/1.0V/1.8V), supporting the analog front-end, digital back-end, and high-voltage stimulation circuits. By introducing a source degeneration bypass capacitor in the class-AB gain stage of the regulator loop, the loop bandwidth is effectively enhanced, resulting in improved load transient performance without increasing power consumption. The modular design of this dual-loop rectifier structure ensures scalability while maintaining stability under any load conditions.

2. For the downlink data telemetry, a sampling-based envelope detector circuit is presented, eliminating the need for the area-consuming filtering capacitor typically used in conventional envelope-detector-based demodulator structures. This approach can also support a lower modulation index in ASK-based communication while maintaining a reliable envelope extraction, resulting in a lower voltage ripple in the rectified DC output.

3. For uplink data telemetry, the conventional IR-UWB transmitter structure is enhanced by reducing the digital logic delay, enabling a higher carrier frequency. Additionally, the data rate for uplink telemetry is increased by introducing a new dual-edge-sensitive pulse generator structure.

The organization of this chapter is as follows: Section 3.2 discusses the design considerations behind the proposed power management and bi-directional data communication system. Section 3.3 details the circuit implementations of each unit. Section 3.4 presents the measurement results of the fabricated chip. Section 3.5 introduces a new sampling-based envelope detector and its simulated performance. Finally, Section 3.6 provides a comparison with state-of-the-art designs and concludes the chapter.

3.2 Design considerations

Table 3.1: Specifications for the wireless system design

Item	Values
Downlink carrier frequency	40.68 MHz
Data rate (downlink)	~200 kbps (~8 kHz × 3 bits preamble + 23 bits commands) nominal ±50%
Uplink carrier frequency	4 GHz ±10%
Data rate (uplink)	~20 Mbps (~1024 ch × 20 kHz × 10 bit / ~10x compression) ±50%
SAR constraint	< 1.6 W/kg
Supply voltages	0.9/1.0/1.8V
Power delivered to the load	~10 mW ±50%
Power coil separation distance	5 mm (air) + 9mm (tissue)
Data antenna separation distance	> 24 mm
Form factor of the PCB with implantable chip	< 3.5 mm sidelength
Chip size	1 mm^2 ± 50%

The communication topology must be carefully chosen to ensure high data rate communication and power efficiency while maintaining a compact and implantable form factor. Fig. 3.2 summarizes prior work on data telemetry in implantable devices over the past decade, highlighting advancements and trade-offs in different approaches.

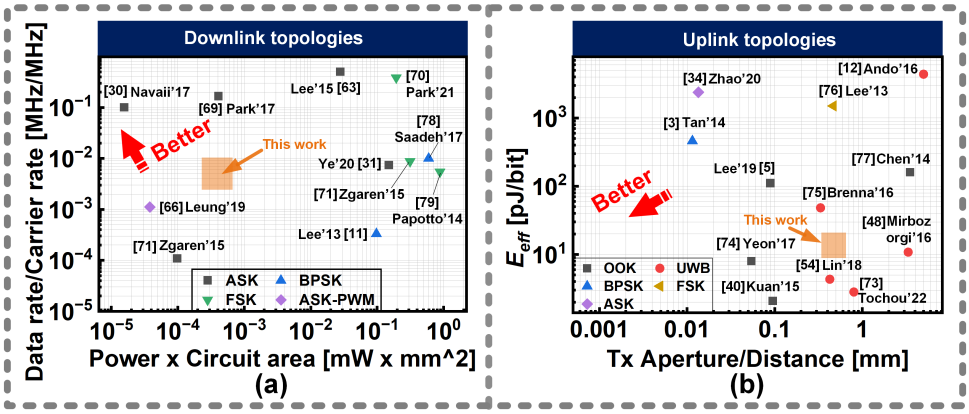


Figure 3.2: Survey on data telemetry for implant applications: (a) downlink techniques, and (b) uplink techniques.

For the downlink, power and area can be compared against bandwidth performance using the figure of merit (FoM) defined in [11]:

$$\text{FoM} = \frac{\text{Data rate}}{\text{Power} \times \text{Circuit area}} \tag{3.1}$$

where power refers to the power consumption, and circuit area denotes the layout area, both associated with the downlink circuit block. However, this expression does not account for the carrier frequency that determines the data rate. This work defines a new FoM that includes the carrier frequency as well:

$$\text{FoM} = \frac{\text{Data rate}}{\text{Carrier frequency} \times \text{Power} \times \text{Circuit area}} \tag{3.2}$$

This work targets a 200 kbps data rate with a 40.68 MHz carrier frequency while consuming minimal power (only several tens of μW) and area. Under these constraints, the possible downlink techniques can be selected from ASK modulation, Frequency Shift Keying (FSK) modulation, and Phase Shift Keying (PSK) modulation. ASK is more suitable in this design due to its simpler circuitry and lower power consumption in the receiver compared to other modulation strategies.

For the uplink, the relationship between the transmitter (Tx) antenna aperture, link distance, data rate, and power consumed by the Tx driver

circuit can be evaluated. Possible topologies are on-off keying (OOK), ASK, ultra-wide bandwidth (UWB), binary phase shift keying (BPSK), and FSK. By considering the target system specifications, including the constrained implant device form factor (<3.5 mm sidelength), the communication distance constraint imposed by the air and tissue separation (>24 mm), the power consumption budget for the uplink transmitter (<1 mW), and its required data rate (~20 Mbps), either UWB or OOK are suitable candidates for the uplink scheme. UWB is adopted here since it offers several advantages over other approaches: a wide bandwidth communication capability with a high data rate and efficiency (typically over 100 Mbps while consuming less than 20 pJ/bit), minimal interference with other frequency bands due to its low output power level (below –41.3 dBm/MHz [12]), and operation at GHz-range frequencies, which enables the use of compact implantable antennas with apertures below 1/4 wavelength.

The following sections explain the operating principle for the PMU, the downlink, and the uplink.

3.2.1 Power management unit

The power management unit (PMU) converts the AC voltage harvested by the Rx coil into multiple stable DC outputs, providing supply voltages and bias currents for the remaining circuitry and the retinal chip load, as shown in Fig. 3.1. Key performance metrics considered for this chip design in the power conversion circuits include Power Conversion Efficiency (PCE) for the rectifier, load regulation performance, and Power Supply Rejection (PSR) for the regulator. Notably, there is often confusion about the definitions of PSR [13,14] and the well-known Power Supply Rejection Ratio (PSRR) due to the lack of standardization between these terms, and sometimes they are used interchangeably [15]. Generally, PSR is mostly used to characterize LDOs and bandgap references, while PSRR is primarily used for operational amplifiers (OPAMPs). The respective definitions are presented in Eq(3.3) and Eq(3.4):

$$\mathrm{PSR} = 20\log\left(\frac{\Delta V_{\mathrm{out}}}{\Delta V_{\mathrm{in}}}\right) \tag{3.3}$$

$$\mathrm{PSRR} = 20\log\left(\frac{\Delta V_{\mathrm{in}}}{\Delta V_{\mathrm{out}}}\right) \tag{3.4}$$

where V_{in} is the power supply ripple, while V_{out} is the resulting output voltage variation.

A full-bridge passive rectifier utilizing Schottky diodes (Fig. 3.3 (a)) is adopted in this design for its simplicity and reliability in handling input voltages. Although the PCE of the Schottky rectifier (~68%) is generally lower compared to the differential V_{th} cancellation rectifier (~67.5% at 953 MHz [16], Fig. 3.3 (b)) and the active rectifier (~80.2% at 13.56 MHz

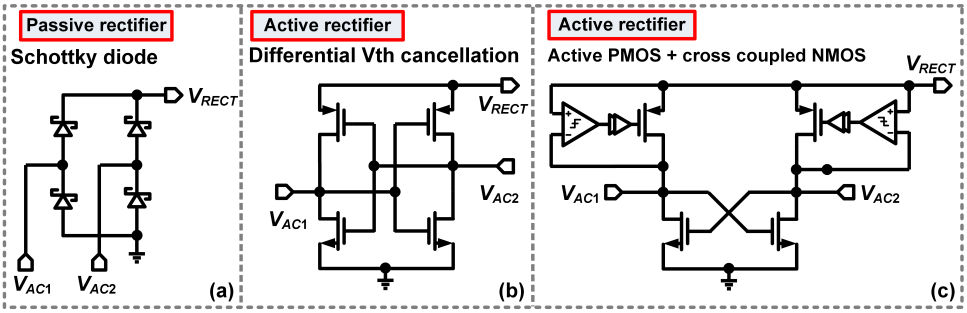


Figure 3.3: Low-voltage-drop rectifier topologies: (a) Passive rectifier using Schottky diodes, (b) Active rectifier using differential threshold voltage cancellation [16], and (c) Active rectifier using offset-compensated comparators [17].

[17], Fig. 3.3 (c)) at the target frequency of 40.68 MHz, its robustness makes it a suitable choice for this work. More advanced rectifier designs will be discussed in detail in Chapter 4.

The rectifier stage in the PMU typically generates an output voltage with a noticeable ripple (~25 mV with 200Ω/2nF loading capacitor at 40.68 MHz - mathematical derivation presented in Chapter 4) that is also susceptible to input and output load variations. To address these challenges, a low-dropout regulator (LDO) is often succeeding the rectifier to provide ripple reduction and voltage regulation. The classic regulator structure includes a pass transistor driven by an error amplifier and a feedback path Fig. 3.4(a). Traditionally, large output capacitors (~μF) are employed to set the dominant pole at the output node of the regulator and stabilize the loop, as demonstrated in [18, 19]. This approach inherently results in excellent load transient performance and PSR at the cost of integration. However, in practical miniaturized implants, the output capacitance must be reduced to a few nF due to the limited volume budget, compromising the regulator's output voltage performance.

Over the past decades, capacitor-less LDO designs have been proposed, see Fig. 3.4(b)-(c) [13, 14, 20–22]. Fig. 3.4(b) splits the poles by using Miller compensation. The dominant pole (p_0) is contributed by the capacitor at the error amplifier output and C_{gd} at the gate of the pass transistor. Fig. 3.4(c) splits the poles by inserting an intermediate buffer stage between the error amplifier and the pass transistor. Both Miller compensation-based and buffer-based techniques eliminate the bulky off-chip output capacitor and shift the dominant pole to the internal node of LDOs. While these approaches address area constraints, they reduce both the DC gain and the effective bandwidth to maintain stability, leading to degraded undershoot and overshoot performance in the regulator output.

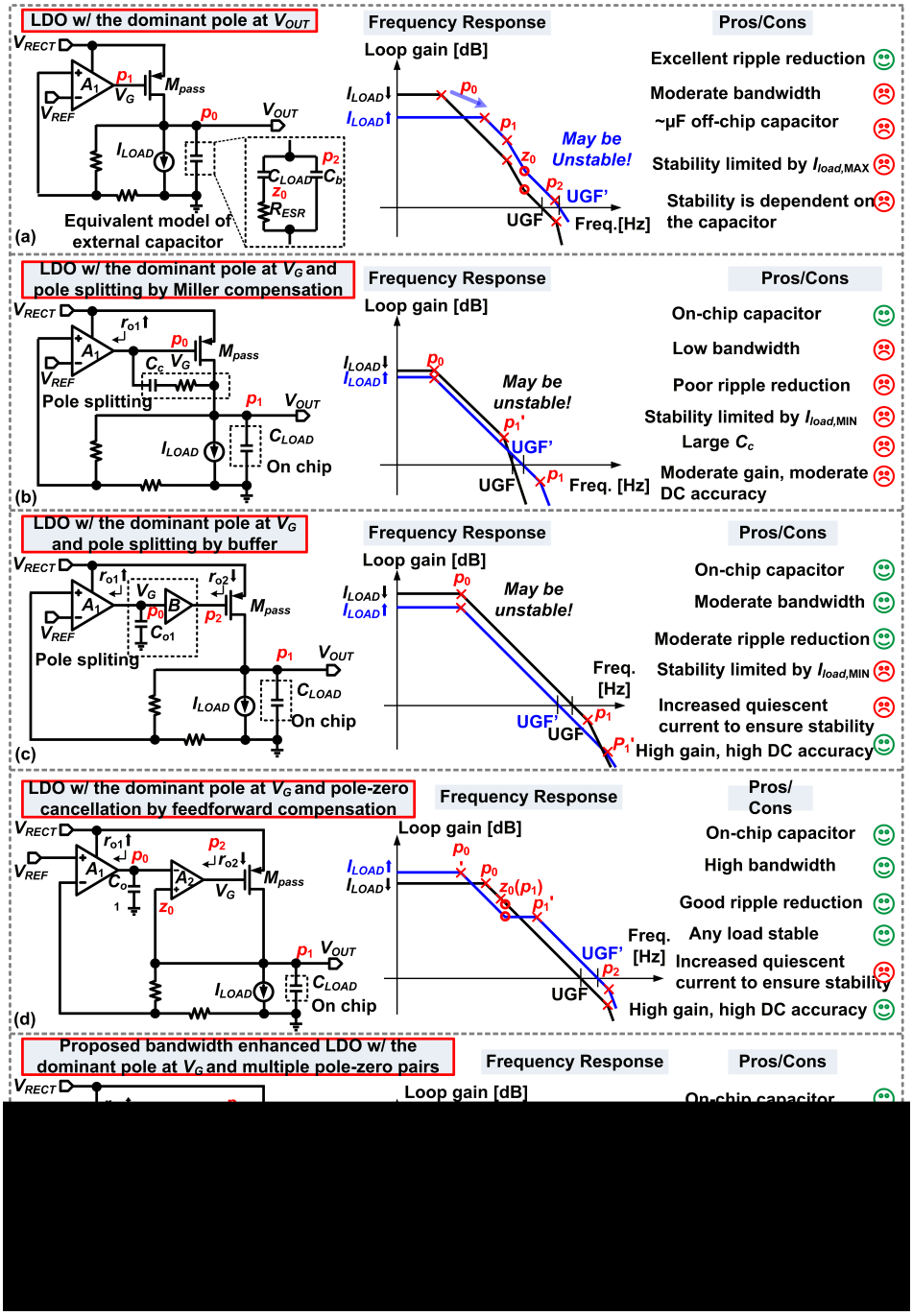


Figure 3.4: Low-dropout regulator topologies: (a) Conventional LDO with an external capacitor [18], (b) Conventional pole-splitting LDO with miller compensation [22], (c) Conventional pole-splitting LDO with an intermediate buffer stage [21], (d) Bandwidth-enhanced LDO with a pole-zero pair cancellation realized by the feedforward path [14], and (e) Proposed bandwidth-enhanced LDO.

To overcome these limitations, specific design strategies have been developed. Most of these works have applied the feed-forward pole-zero cancellation concept [26] in the buffer stage design, as Fig. 3.4(d) shows. The simplest buffer structure is illustrated in Fig. 3.5(a), consisting of a common-gate stage, commonly referred to as a flipped voltage follower [23, 24]. In this configuration, M_1 and M_{pass} establish a fast feedback loop in addition to the slower loop formed by the error amplifier. Specifically, M_1 detects variations in the output voltage and provides a feedback signal to the gate of M_{pass}. To further enhance the loop gain, an additional buffer stage [13, 25] can be introduced, as shown in Fig. 3.5(b). The concept of feed-forward pole-zero cancellation is also adopted in other published works. For instance, the work in [20] presents an instantaneous load regulation LDO structure that incorporates a high-bandwidth intermediate buffer stage. This design enhances the loop bandwidth while introducing an additional zero to compensate for the non-dominant pole (p_1) at the regulator's output. Though this approach successfully addresses the limitations in Fig. 3.4(b) and (c), the loop bandwidth is still limited by the non-dominant pole (p_2) at the gate of the pass transistor, requiring a significant amount of quiescent current consumed by the buffer stage. As reported in the work [14], around 276 μA quiescent current is required to push the non-dominant pole at the buffer output into the high-frequency range for stability. Alternatively, [13] proposes a tri-loop LDO structure, achieving overshoot and undershoot of 82 mV and 43 mV, respectively, within a 200 ps edge time. Nevertheless, the trade-off between error amplifier gain and loop stability in this design results in a slow settling time of 200 ns and a PSR of only -21 dB at low frequencies, making it more suitable for wideband communication applications rather than Industrial, Scientific, and Medical (ISM) band applications. In this work, a dual-loop fast-transient capacitor-less LDO structure Fig. 3.4(e) is employed to meet integration requirements. The proposed design offers the advantage of minimizing overshoot and undershoot during load transitions while maintaining good PSR performance within the operational bandwidth (less than -50 dB with frequency ranging from 0 to 1 kHz for the 1.8V regulator at 4 mA heavy load). This is achieved through the combination of a fast-transient FVF buffer loop and a slow, high-gain error amplifier loop. An innovative FVF buffer stage with improved bandwidth performance is proposed in this design. This approach introduces an additional zero to effectively cancel the non-dominant pole (p_2) at high frequencies, thereby improving overall frequency response (more details in Section 3.3.1)).

3.2.2 Downlink data communication unit

As discussed at the beginning of Section 3.2, ASK modulation is adopted in this work due to its low power consumption and simplified circuit implementation. However, conventional ASK modulation (Fig. 3.6(a))

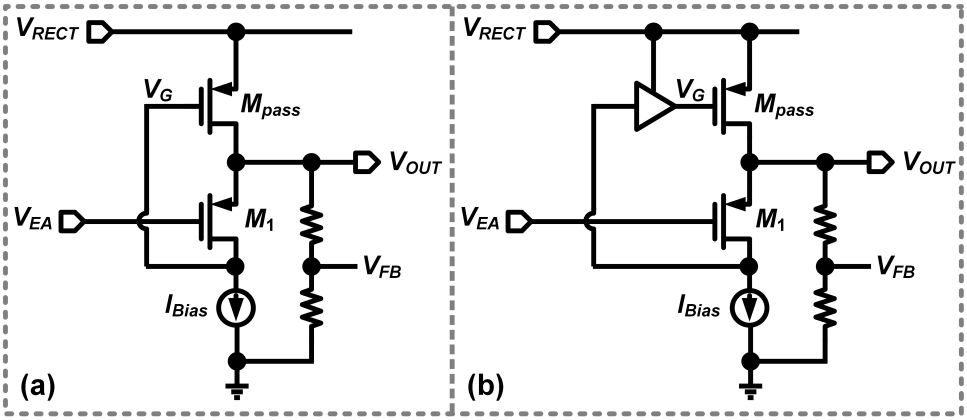


Figure 3.5: Buffer structures used in pole-spiting LDO designs: (a) Flipped voltage follower (FVF) [23, 24], and (b) Improved FVF with inserted buffer [13, 25].

suffers from severe clock and data synchronization issues, significantly limiting the achievable data rate, which has been reported to be only 60 kbps in [27].

To address this synchronization challenge, clock and data information can be both modulated onto the power carrier signal using Manchester encoding [28, 29] (Fig. 3.6(b)) or ASK with Pulse Width Modulation (ASK-PWM) [1]. These approaches require a transition detector or a Delay-Locked Loop (DLL) for clock recovery. However, the former is highly sensitive to clock jitter, which can lead to data sampling errors due to incorrect clock edge alignment, while the latter requires excessive area and power consumption. More critically, ASK with Manchester encoding and ASK-PWM significantly reduce the received power level due to the long duration time of low amplitude carrier signal corresponding to a '0' in Fig. 3.6(b).

Unlike Manchester encoding and ASK-PWM, which encode data by modulating amplitude over varying durations, ASK with Pulse Position Modulation (ASK-PPM) utilizes short-duration pulses at distinct time positions, as illustrated in Fig. 3.6(c). Each data bit is encoded using three pulses, where the duty cycle of the first detected pulse determines whether a '1' or '0' is transmitted. For example, a '1' can be represented by time intervals between pulses occupying 70% and 30% of a data bit duration time, while a '0' can be represented by time intervals between pulses occupying 30% and 70% of a data bit duration time. In addition to encoding data, the clock signal is inherently embedded in the pulse sequence and can be extracted using a simple toggle register, as described in the sawtooth PWM detector in Section 3.3.2. Since ASK-PPM employs minimal amplitude variations within the power carrier due to the short pulses, it

effectively reduces power loss across the inductive power transfer link, enhancing overall system efficiency. The behavior model simulation result illustrates that the ASK-PPM modulation scheme improves the wireless power transfer efficiency by 87.7% when the modulation index is 0.5, compared to ASK modulation(and Manchester encoded ASK modulation), see Fig. 3.7. The modulation index (MI) [30, 31] is defined as follows:

$$\mathrm{MI} = \frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}} \tag{3.5}$$

where $V_{\max}$ and $V_{\min}$ represent the maximum and minimum voltage amplitudes of the AC signal, respectively.

Notably, the terms modulation index and modulation depth (MD) [9, 32] are often used interchangeably. However, modulation depth is more commonly expressed as a percentage, as given by:

$$\mathrm{MD} = \frac{V_m}{V_c} \times 100\% \tag{3.6}$$

where V_m denotes the amplitude of the modulated signal, and V_c represents the amplitude of the carrier signal.

The modulation index is equivalent to the modulation depth. To maintain consistency and avoid confusion, this work uses the modulation index rather than the modulation depth for analysis.

With its unique advantages in power efficiency and communication robustness, ASK-PPM modulation is selected for the downlink due to its simplicity, reduced bit error rate (BER), and inherent self-synchronization capabilities. The downlink unit consists of an ASK signal demodulator, a clock/data recovery circuit, and a Serial-In-Parallel-Out (SIPO) circuit with identity (ID) detection functionality. The data downlink communication unit recovers data and clock information by detecting amplitude changes in the received AC signal. Fig. 3.8 illustrates the configuration of the data bits used in this design. Depending on whether the preamble bits of the data packet match their predefined values, either this chip or another recording/stimulation chip can be activated. In this design, the preamble bits for this chip are configured as preamble [2:0] = [1, 0, 1], while for the recording/stimulation chip, the preamble bits are defined as preamble [2:0] = [1, 1, 0]**.**

The operating principle of the downlink unit is as follows: 1. During the data exchange phase, if the bit stream contains the preamble bits [1, 0, 1], which match the ID of the wireless chip (Rx chip), the wireless chip is enabled while the retina chip remains disabled. Once 23 data bits are loaded into its shift register array, the wireless chip activates a data write signal. The power consumption of the download unit, including the ASK demodulator and the clock/data recovery (CDR), is 28.88 μW. At a data rate of 200 kbps, the download unit achieves 144.4 pJ/bit when

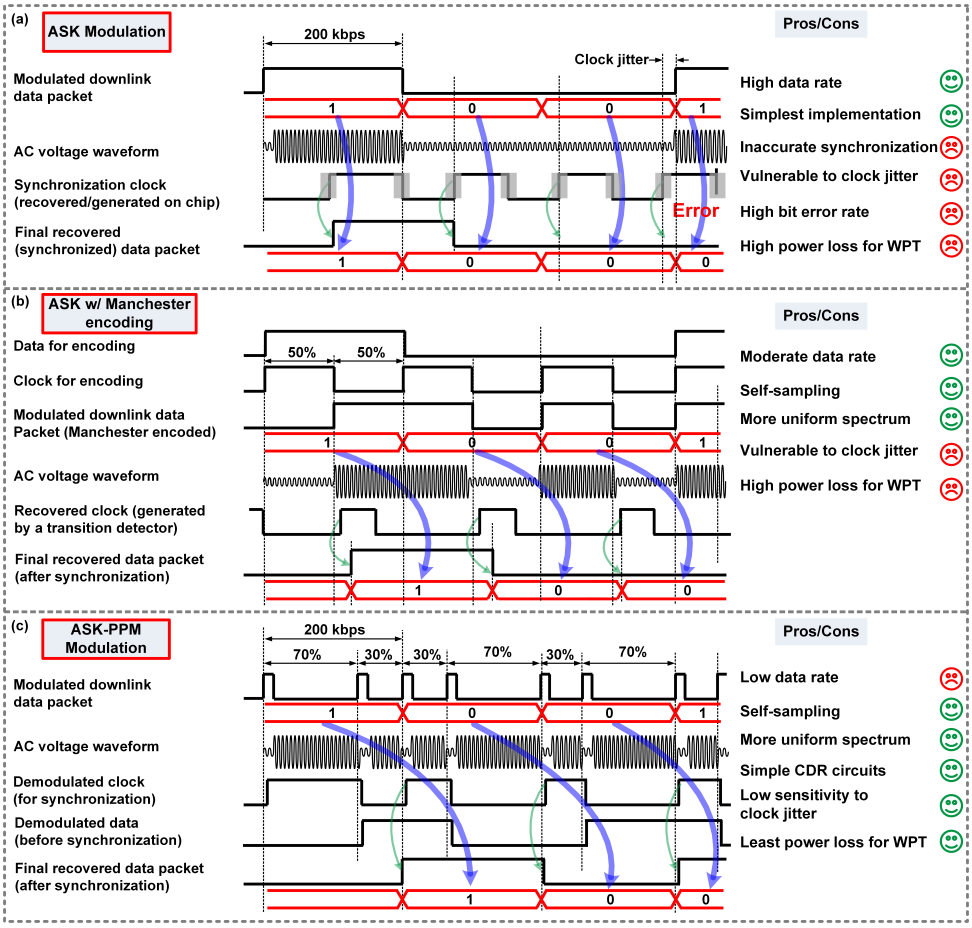


Figure 3.6: ASK modulation topologies for data recovery: (a) Standard ASK modulation with the synchronization clock recovered from carrier signal [27] or generated on-chip, (b) Standard ASK modulation with Manchester encoding, and (c) ASK modulation with PPM [33] to achieve self-sampling and low power link loss.

demodulating data. 2. During the idle phase, the download circuit block consumes negligible current as no state transitions occur in the digital circuits. 3. During the subsequent data exchange phase, if the bit stream contains the preamble bits [1, 1, 0], which match the ID of the retina chip, the retina chip is enabled while the wireless chip remains disabled. Conversely, if the bit stream contains the preamble sequence [1, 0, 1], matching the ID of the wireless chip, the wireless chip is enabled while the retina chip remains disabled. Therefore, the register data in both the

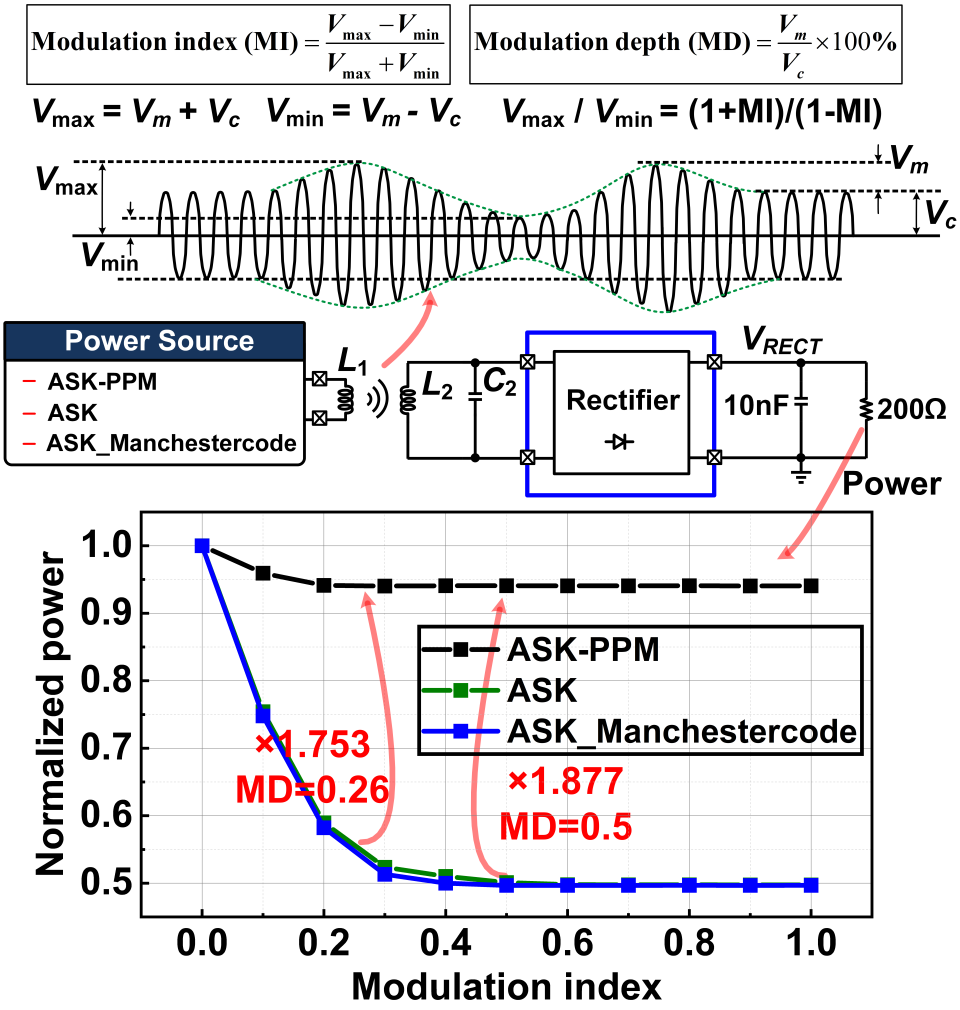


Figure 3.7: The normalized power level comparison between different ASK topologies. The x-axis is the modulation index. The ASK-PPM modulation scheme shows the least power loss due to its inherent minimal variation time on the power carrier signal.

wireless and retina chips can be reconfigured accordingly.

The ASK demodulator is a key component that defines the overall performance of the downlink receiver, converting the analog signal shape into digital pulses for subsequent processing. Conventional envelope detectors, commonly used in ASK downlink applications, are based on the RC current sink and comparator/Schmitt trigger structures (Fig. 3.9(a)) [1, 34, 35]. The Low-Pass Filter (LPF) at the rectifier output can filter out

the high-frequency power carrier signal for a smooth comparison, while the current sink provides a current-sinking path for the LPF capacitor. When the DC level of the input signal is in the high state (representing data bit of '1'), the low pass capacitor is charged through the diode, presenting a high voltage; when the DC level of the input signal is in the low state (representing data bit of '0'), the low pass capacitor discharges through the current sink, presenting a low voltage. Therefore, the following hysteresis comparator stage can detect the high and low voltage transitions. A trade-off exists when deciding the value of the low-pass capacitor and the discharging current. The former affects the ripple on the filtered signal, while the latter determines the amplitude variation when the data bit transits. More detailed analyses are provided in Section 3.5. There are two main issues related to this type of ASK demodulator design: (i) the area footprint and (ii) the power consumption.

(i) The circuit area of the conventional ASK demodulator is usually dominated by the LPF capacitor. Typically, a large LPF capacitor (e.g., 10 pF for carrier frequencies of 1-10 MHz and data rates of 25-250 kbps, as reported in [1]) is used in this type of ASK demodulator to achieve proper signal shaping. However, the large capacitor hinders on-chip integration. In addition, this topology exhibits high sensitivity to the absolute capacitance value, particularly when handling high data rate signals. Any variation in capacitance due to process variation can significantly distort the demodulated envelope shape, potentially leading to data recovery failures (more details in Section 3.3.2).

(ii) The power consumption of a conventional ASK demodulator is determined by the discharge current and the power dissipation of the comparator (or Schmitt trigger in some applications [36]), both of which continuously draw current from the voltage supply. The discharge current is proportional to the amplitude of the envelope signal, whereas the comparator/Schmitt trigger significantly increases the power budget for detecting modulation signals with a low modulation index.

In recent years, high-detection range ASK demodulators [11,30,37,38], illustrated in Fig. 3.9(b), have been proposed to reduce power consumption and improve integration. In these structures, the filtering capacitor

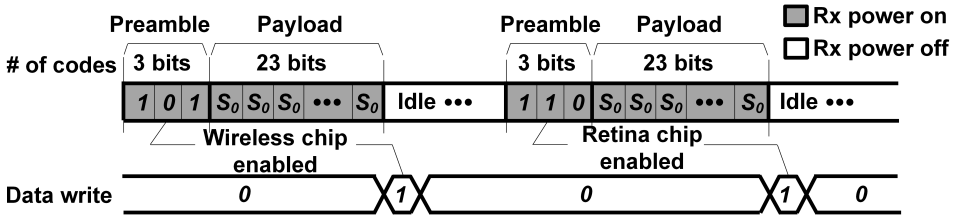


Figure 3.8: The configuration for the downlink data packet.

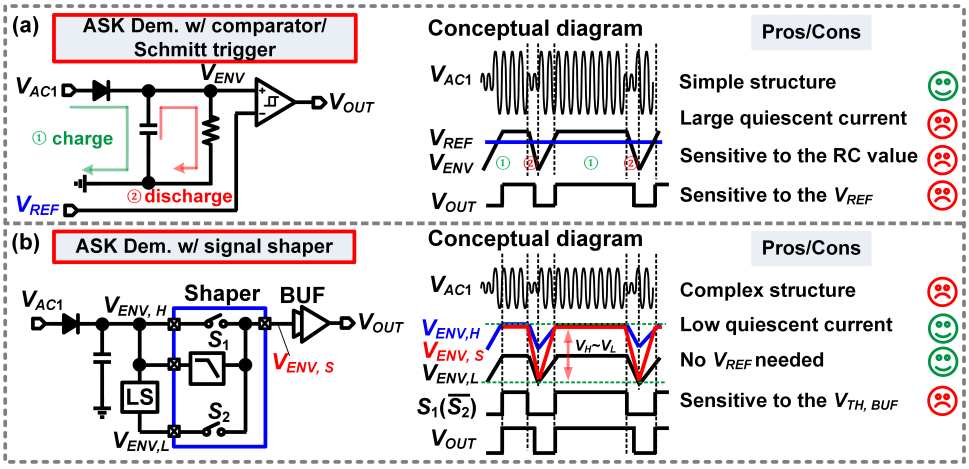


Figure 3.9: Downlink data communication topologies of (a) conventional ASK demodulator based on capacitor filtering and comparator/Schmitt trigger [1], and (b) improved comparator-less ASK demodulator designs based on signal shaping [37].

is typically implemented by a MOS capacitor for area reduction and process compatibility. Instead of a conventional comparator, these designs employ a shaper and a buffer stage to achieve low static current consumption. The shaper enhances the amplitude difference of the original envelope signal, which is subsequently processed by the buffer stage to generate a rail-to-rail output. For example, in Fig. 3.9(b), the switching operation of $S_{1,2}$ expands the amplitude variation range of $V_{ENV,H}$ to $V_{ENV,S}$, thereby improving signal distinction. While these designs eliminate the need for a comparator/Schmitt trigger, they rely heavily on stable transistor threshold voltages, making them highly sensitive to process, voltage, and temperature (PVT) variations.

Additionally, most of these designs use passive diodes for half-wave rectification. However, the significant forward voltage drop (~0.7 V for standard diodes and ~0.45 V for Schottky diodes) poses a challenge in advanced CMOS technologies with reduced supply voltages (e.g., 1.1 V for the 40 nm CMOS process). In this case, more than half of the signal amplitude is wasted across the diode during rectification, leaving insufficient amplitude for shaping and comparison. This also limits the maximum achievable data rate due to inadequate charging of the damping AC signal through the diode.

For the sake of simplicity and safety, this work uses a conventional capacitor-based envelope detector as Fig. 3.9(a). The detailed circuit implementation is introduced in Section 3.3.2. Section 3.5 discusses the limitations of such a structure and introduces an innovative sampling-

based envelope detector with its simulated performance.

3.2.3 Uplink data communication unit

Impulse Radio Ultra-Wideband (IR-UWB) technology has been employed as the modulation technique in the uplink data communication unit due to its potential for low-power and high-data-rate communication in implantable systems [39, 40, 47–49]. UWB pulse generation can generally be categorized into three primary methods: (i) oscillator-based [39–43] (Fig. 3.10 (a)), , (ii) filter based [44–46] (Fig. 3.10 (b)), and (iii) edge-combine based [47–49] (Fig. 3.10 (c) and (d)).

A ring oscillator is commonly employed as the local oscillator (LO) for pulse generation (Fig. 3.10(a)). However, it inherently suffers from frequency instability, necessitating frequency calibration through either a Frequency-Locked Loop (FLL) [39] or foreground calibration [42]. While LC oscillators offer a more stable alternative, they come with trade-offs, including larger silicon area requirements and increased power consumption [43, 50]. Beyond frequency inaccuracy, another critical drawback of LO-based pulse generators is their slow startup time, particularly in high-Q resonator systems characterized by low power consumption and low phase noise. This issue poses challenges for implementation in power-efficient duty-cycled systems [51]. Additionally, the output of an LO-based pulse generator requires proper filtering and shaping to comply with emission mask regulations. However, designing a highly adjustable on-chip signal shaper remains a significant challenge in these architectures [41–43]. Furthermore, the output power of the antenna driver is inherently reduced due to these design constraints.

The filter-based method (Fig. 3.10(b)) [44–46] can also be employed to generate *n*-th-order Gaussian-like UWB pulses. This approach uses the impulse or step response of a filter, potentially in conjunction with the antenna. The circuit implementation consists of an impulse generator followed by a bandpass filter. However, to achieve a higher-order Gaussian-like waveform, the bandpass filter network, which comprises passive inductors and capacitors, can become significantly bulky and is typically implemented off-chip. Another drawback of the filter-based method is its constant power consumption due to the biasing circuit [44] and the filter stages [45, 46], which degrades overall energy efficiency.

The delay-chain-based filtered combined edges method (Fig. 3.10(c)) is an attractive solution due to its low power consumption, as each monocycle pulse (the square waves before combining in Fig. 3.10 (c) and (d)) can be independently generated based on the bandwidth requirement [52, 53]. Additionally, it demonstrates superior pulse-shaping capability, making it well-suited for stricter emission mask compliance [51]. Another key advantage is its near-zero startup time, making it highly suitable for duty-cycle-controlled applications aimed at energy efficiency. However, achieving Federal Communications Commission (FCC)-compliant

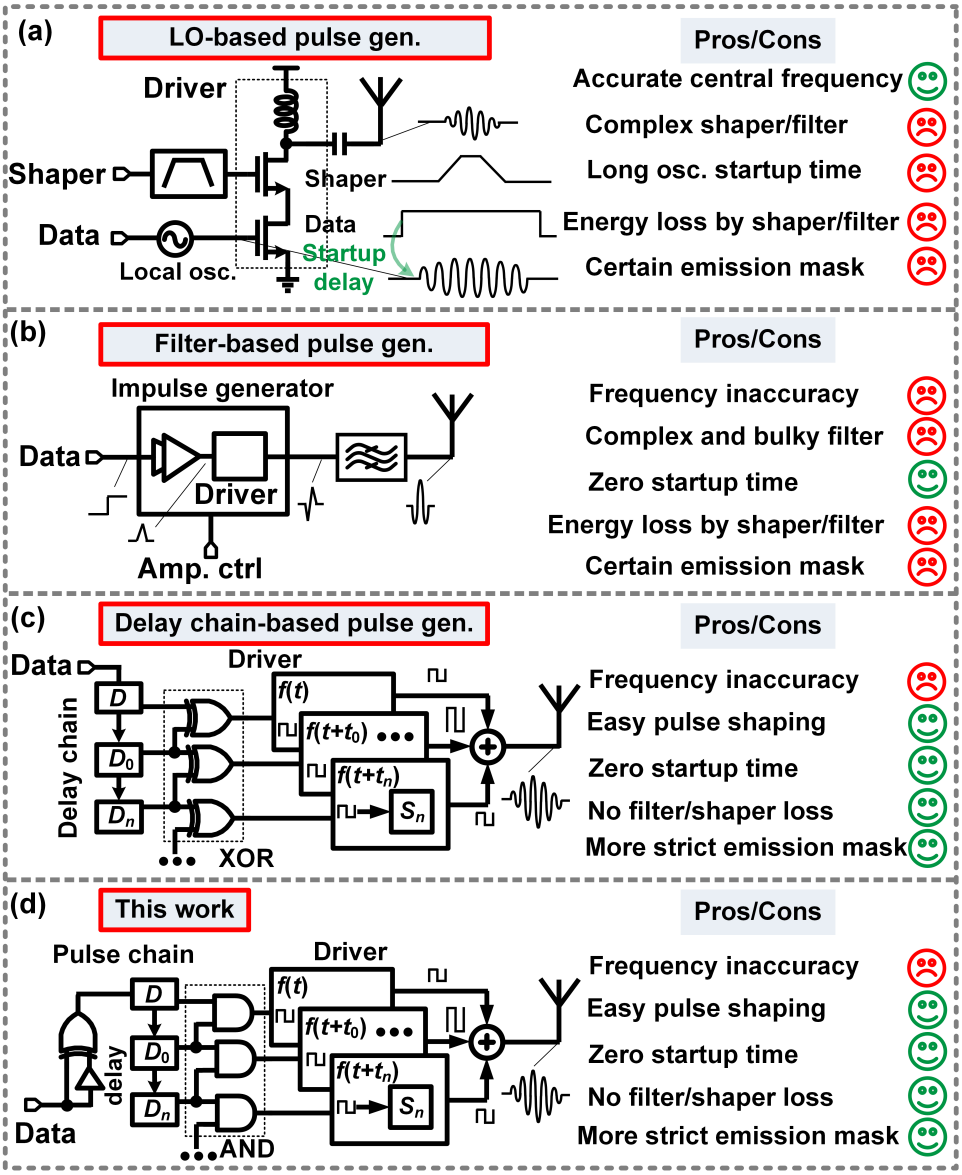


Figure 3.10: Uplink data communication topologies of (a) Local-oscillator based pulse generator [39–43], (b) Filter based pulse generator [44–46], (c) Delay-chain based pulse generator [47–49], and (d) Proposed frequency-improved delay-chain based pulse generator.

pulses requires either a resource-intensive filter implementation [47] or complex calibration procedures [54].

A programmable IR-UWB pulse generator using the combined edge method was proposed in [49], offering a low-power, filter-free solution. However, this implementation converts only the rising edge of the input pulse. To enable dual-edge pulse conversion, an XOR logic gate can be used to replace the original AND gate logic from [49, 53]. While this approach allows dual-edge transmission, it introduces a delay equal to approximately twice the rising/falling delay (80 ps each in a 180 nm BCD process) of the AND gate, significantly reducing the achievable maximum center carrier frequency. Moreover, at higher center frequencies, the falling-edge pulse may overlap with the rising-edge pulse under worst-case scenarios [53], further constraining the maximum achievable frequency.

To overcome the limitation on the maximum achievable center carrier frequency imposed by the XOR logic in [53], this design moves the XOR logic to the input stage, as illustrated in Fig. 3.10(d). The XOR logic works as a dual-edge pulse generator for the Manchester code input data. The dual-edge pulses are subsequently converted into short-duration pulse sequences using AND logic. Consequently, the carrier frequency is no longer constrained by the long propagation delay of the XOR logic (further details are provided in Section 3.3.3). In this approach, both the amplitude and frequency of each monocycle (the square waves before combining) are adjustable. This flexibility ensures that the power spectral density (PSD) conforms to the FCC emission mask requirements. Furthermore, this method eliminates the need for complex calibration procedures or area-intensive filter designs, making it a more efficient and practical solution.

3.3 Hardware Implementation

Fig. 3.11 illustrates the proposed power/data management ASIC architecture. The system receives a 40.68 MHz power carrier signal via an inductive wireless link and performs AC-DC conversion using a passive rectifier. The rectified voltage (2 V) is filtered and stored in an off-chip 10 nF decoupling capacitor. The capacitor-less regulators further regulate the rectified voltage to improve power supply rejection (PSR) and load regulation. These regulators provide voltage supplies of 1.8 V, 1.0 V, and 0.9 V for I/O pads, digital circuits, and analog circuits, respectively. To achieve the lowest supply voltage of 0.9 V, the bandgap reference (BGR) output voltage is set to 0.6 V. The power-on-reset (POR) circuit generates an enable signal with a startup delay (20.69 ms measured at a 60 ms supply voltage rising edge) and hysteresis (0.15 V based on simulation) to ensure stable digital circuit operation. For data communication, the ASK-PPM modulated downlink data, transmitted at a 200 kbps data rate,

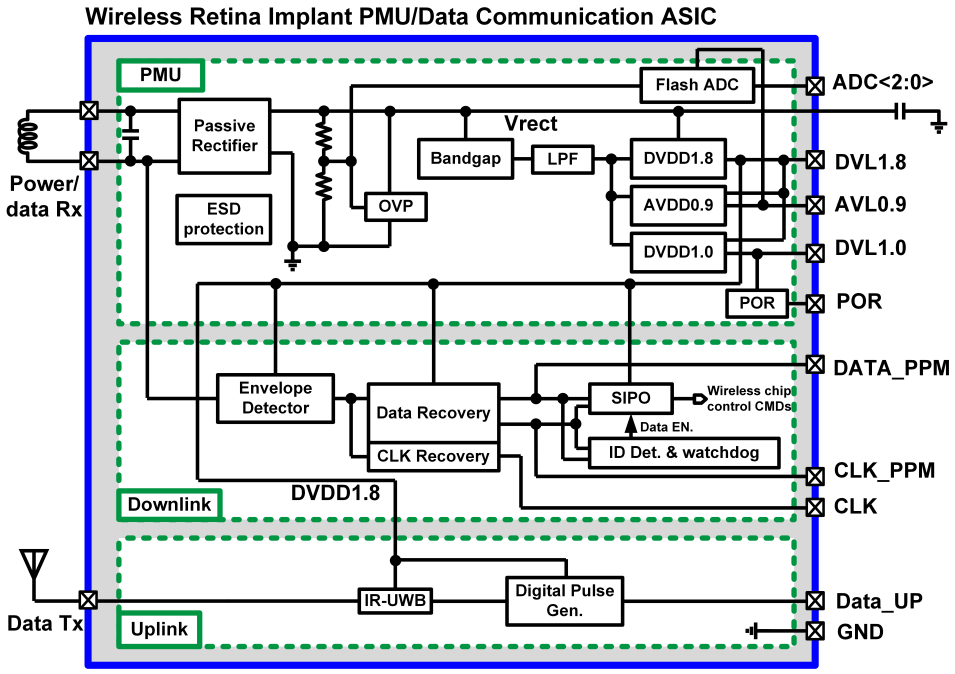


Figure 3.11: The overall structure of the proposed design.

is recovered using an envelope detector followed by data/clock recovery circuits. The recovered command data is stored in a 26-bit shift register and parsed to the desired memory (wireless chip or retina chip) based on the 3-bit preamble. The uplink unit receives Manchester-encoded data from the retina chip at a data rate of 20 Mbps. The data is converted into IR-UWB short pulses with a 4 GHz center carrier frequency to drive the PCB-mounted antenna. This architecture supports Manchester-encoded data processing and achieves simultaneous wireless powering, downlink, and uplink functionality with a minimized number of off-chip components (a power coil, an uplink antenna, and a decoupling capacitor). The power link's 240 pF resonance metal-insulator-metal capacitor (MIM capacitor) is integrated on-chip.

The power/data management ASIC is organized into three primary blocks described in the following sections: the power management unit, the downlink data unit, and the uplink data unit.

3.3.1 Power Management Unit

Sub-1V bandgap voltage reference: The PMU employs a sub-1V bandgap voltage reference [55] (Fig. 3.12(a)) to generate supply-independent bias currents and reference voltage (0.6 V). This is achieved through a

high-gain error amplifier (64.5 dB at low frequency) and a cascode PMOS bias structure. The bipolar-based bandgap voltage reference was chosen over transistor-based bias current generators [56, 57] due to its superior robustness to process and supply voltage variations. Additionally, it supports self-startup without requiring manual intervention. The output reference voltage can be adjusted using a 2-bit trimming code, ranging from 0.52 V to 0.64 V, with a nominal voltage of 0.6 V. *Supply voltage*

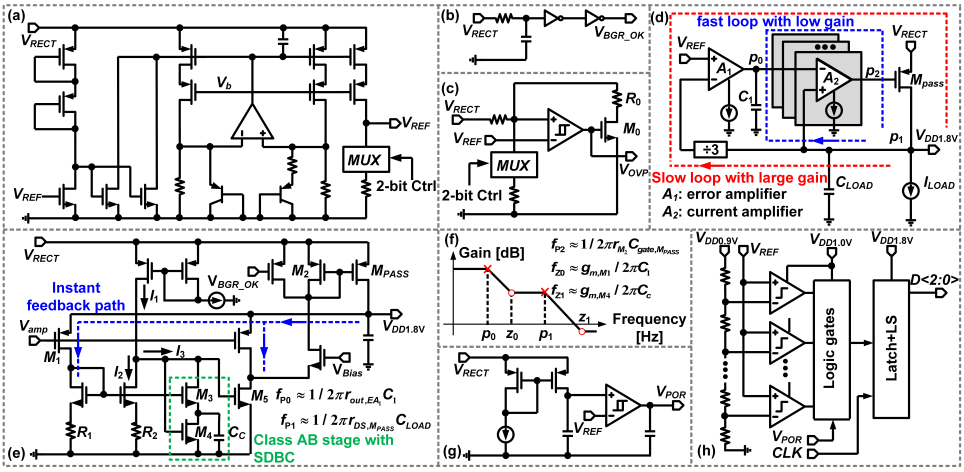


Figure 3.12: The circuit implementation of (a) bandgap voltage reference [55], (b) supply voltage level detector circuit for the startup, (c) over-voltage protection circuit, (d) dual loop fast settling LDO structure [58], (e) proposed class AB stage with SDBC structure for the fast-loop FVF buffer, (f) power-on-reset (POR) circuit for digital logic, and (g) 3-bit flash ADC structure for monitoring the Rx voltage.

ready signal generator: A simple supply voltage level detector circuit, shown in Fig. 3.12(b), is used to indicate whether voltage regulation should be performed or not. The circuit consists of a delay stage and an inverter buffer stage. This design prevents oscillation issues at the regulator output during the rising phase of the rectified voltage V_{RECT}.

Over-voltage protection: To address potential variations in the received power level, an over-voltage protection (OVP) circuit (Fig. 3.12(c)) is incorporated into the Rx chip to clamp the voltage level within a safe operating range. This design employs a 500Ω current sink resistor (R_0 in Fig. 3.12(c)) to dissipate excess power received by the Rx coil. The maximum voltage of V_{RECT} is constrained to less than 4.8 V, slightly below the standard operating voltage (5V for thick-oxide devices) in this process, through careful design of the comparator's hysteresis window. The OVP block can handle up to 186.68 mW of Tx power and 40.58 mW

of Rx power, which corresponds to 3.34 times the nominal power level. This ensures that V_{RECT} does not exceed the breakdown voltage due to power fluctuations. However, such extreme conditions may lead to tissue heating issues. To ensure reliable and safe wireless power transfer, a power-level monitoring ADC (Fig. 3.12(c)) is implemented. A current sink resistor is utilized instead of a resonant frequency tuning capacitor [17], as capacitors across the coil are more challenging to drive with switches when full bridge rectification is used, as is the case here.

Dual-loop any-load stable LDO with source degeneration bypass capacitor: This design uses a capacitor-less LDO architecture to meet the requirements of fully integrated on-chip design. While some LDO designs employ Miller compensation to establish a dominant pole at the internal node of the LDO, this approach inherently has stability issues under light load conditions. To address this, the non-dominant pole at the LDO output must be shifted further away from the unity gain frequency. However, this adjustment typically comes at the cost of increased quiescent current (e.g., a minimum of 3 mA in [25]) or a larger Miller compensation capacitor (e.g., over 300 pF in [59]), making them unsuitable for compact wireless power systems. This work adopts a dual-loop, any-load-stable LDO structure as introduced in [58]. The topology features a high-gain, low-bandwidth error amplifier and a low-gain, high-bandwidth FVF buffer stage, achieving both high DC accuracy and fast transient voltage regulation, as illustrated in Fig. 3.12(d). Multiple FVF buffer cells, each capable of driving 1 mA, are controlled by the common error amplifier and combined at the gate of the pass transistor. The primary advantage of implementing the second (buffer) stage using parallel-connected cells is that the design can be easily scaled according to the maximum load requirement. For instance, the two regulators—one driving the loading circuits and the other driving the I/O pad—experience different loading currents. Furthermore, stability is maintained regardless of the number of parallel-connected cells, as the non-dominant pole at the buffer's output node (P_2 at the pass transistor gate) remains unchanged. The dominant pole (P_0) is established by the high-gain amplifier with a compact 3-pF capacitor at its output for compensation. The first non-dominant pole (P_1) is positioned at the LDO output. A left-plane zero is introduced between these two poles, created by the FVF buffer 's instantaneous feedback (or active feedforward) path between $V_{DD1.8V}$ and V_{amp} (Fig. 3.12(e)). The zero frequency is determined by the transconductance (g_m) and gate capacitance (C_{gate}) of the PMOS input transistor (M_1) in the FVF buffer . The second non-dominant pole (P_2) can be tuned to a higher frequency by adjusting the size of the diode-connected transistor (M_2). This approach ensures loop stability, as demonstrated in Fig. 3.13. The worst-case stability scenario occurs under light load conditions, achieving a phase margin of 60 degrees which can be further improved by allocating more quiescent current to M_2.

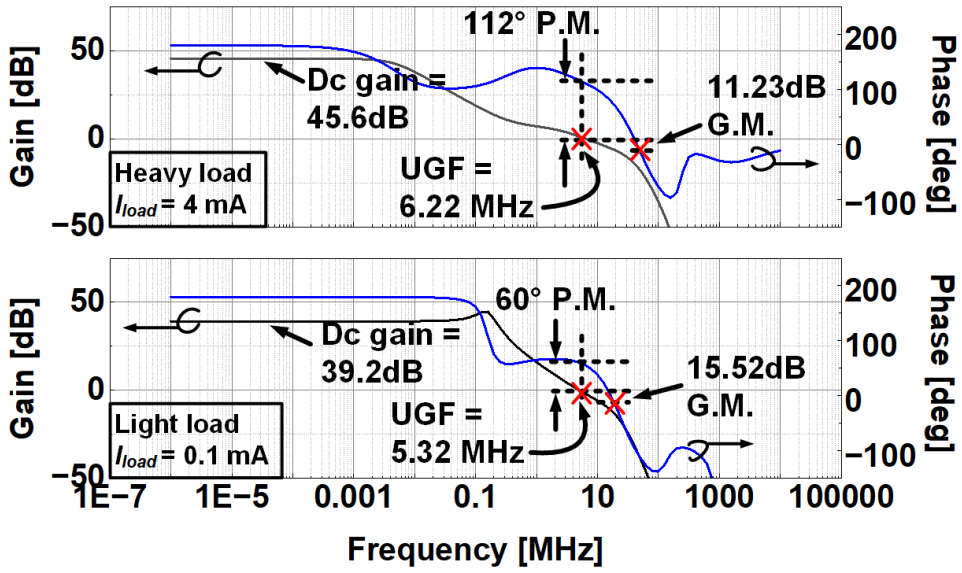


Figure 3.13: The loop gain simulation result of the LDO.

The Class AB stage depicted in Fig. 3.12(e) functions as a gain attenuation block, designed to reduce the gain of the multi-stage amplifier. It comprises a diode-connected combination of transistor M_3/M_4. This Class AB amplifier has lower gain under small input conditions (stable state) and higher gain during significant input variations (transition stage) [58]. Consequently, it mitigates instability issues while enabling rapid compensation for output voltage variations during load transitions, achieving a recovery time of less than 200 ns in this design. In the stable state, the source degeneration transistor M_4 operates in the saturation region with a drain-source voltage of approximately 300 mV, comparable to the voltage drops across R_1 and R_2. The current I_1 splits into I_2 and I_3, attenuating the gain of the M_3 stage. During a load current step-up event, the output voltage ($V_{DD1.8V}$) drops, and this change is immediately propagated through the instantaneous feedback path established by M_1. This feedback causes the gate potential of M_3 to drop, decreasing the drain voltage of M_4. As a result, most of the I_1 current flows directly into M_3, increasing its gain due to reduced resistive loading at its source. This amplified gain drives a rapid voltage drop at the gate of M_3, turning M_5 on and pulling down the gate of the pass transistor. Subsequently, $V_{DD1.8V}$ recovers to its stable state.

The drawback of the class AB stage in this design is that it deteriorates the bandwidth in the heavy load condition. To further enhance the transient performance of this structure, a source degeneration bypass

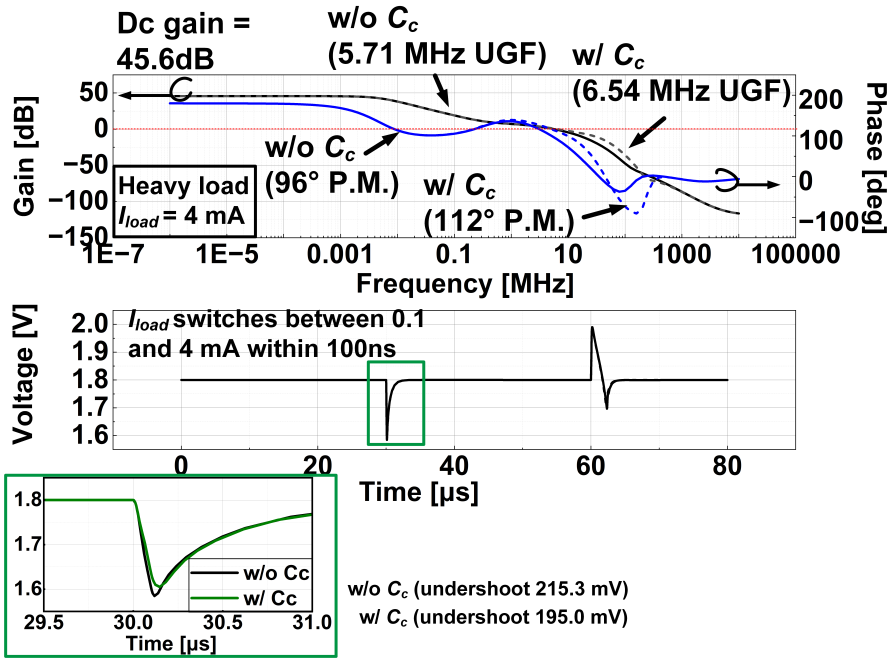


Figure 3.14: The loop gain and the load transient result with and without the coupling capacitor C_c.

capacitor (SDBC) is introduced to strengthen the gain link between M_1 and M_5 during load transitions while maintaining DC gain accuracy. A bypass capacitor (172 fF) is placed near the drain of M_4. In the frequency domain, the SDBC acts as a low-impedance path that bypasses M_4, while in the transient domain, and it serves as a charge storage element to stabilize the drain voltage of M_4, allowing M_5 to turn on more rapidly. Simulation results shown in Fig. 3.14 compare the loop gain and load transient responses with and without the SDBC. Under heavy load conditions (I_{LOAD}= 4 mA), the unity gain frequency improves from 5.7 MHz to 6.54 MHz, reducing the undershoot to 20.3 mV when the load current steps from 0.1 mA to 4 mA. Achieving the same undershoot reduction without the SDBC would require either an additional 720 pF decoupling capacitor or a 14.3% increase in quiescent current - from 81.89 μA to 93.61 μA under light load and from 151.2 μA to 158.8 μA under heavy load.

Power-on reset: The power-on reset (POR) (Fig. 3.12(f)) circuit provides an enable signal with a startup delay (150 μs delay at 40 μs rising edge of $V_{DD1.8V}$) and a hysteresis (0.15 V) for a stable operation of the digital circuits.

3-bit flash ADC: A 3-bit flash analog-to-digital converter (ADC) (Fig.

3.12(g)) continuously monitors the voltage level of V_{RECT}. The monitoring range is designed from 1.6 V to 3 V, with a nominal voltage of 2.3 V and a resolution of 175 mV per digital code. The simulated dynamic performance of this 3-bit flash ADC is illustrated in Fig. 3.15 (a), demonstrating an effective number of bits (ENOB) of 3, verified through a 4096-point simulation using a sinusoidal input (F_{in}= 19.942 MHz). Therefore, it can monitor the voltage variation of V_{RECT} at a maximum rate of 20 MHz, which corresponds to the uplink data rate. Notably, during the uplink phase, V_{RECT} exhibits the highest variation due to high current demand (around 2 mA). The simulated static performance, as illustrated in Fig. 3.15 (b), demonstrates that the linear conversion range of the input signal is from 1.74 V—below which the decoded outputs are [0 0 0]—to 2.62 V, beyond which the decoding result saturates at [1 1 1]. This range can effectively cover the possible variations of V_{RECT} in WPT.

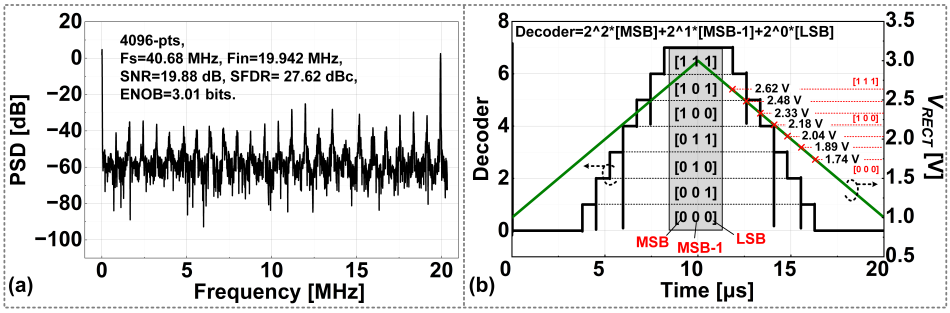


Figure 3.15: (a) The dynamic performance of the 3-bit flash ADC and (b) the static performance. The decoding result shows no missing code when applying a ramp diagonal input signal ranging from 1 V to 3 V.

3.3.2 ASK-PPM for downlink data modulation

Envelope extraction and clock recovery: The downlink unit in Fig. **??**(a) extracts both clock and envelope information from the power carrier signal. Clock recovery is performed using a simple latch that compares the two voltage signals across the Rx coil. The recovered 40.68 MHz clock signal, with a 50% duty cycle, is supplied to the ADC circuit and the retina chip, providing timing for the dynamic comparator and digital logic. This eliminates the need for an external crystal oscillator or an internal frequency reference circuit. Envelope extraction is achieved using a conventional capacitor-based envelope detector circuit. The AC signal, which consists of a high-frequency carrier and baseband data, undergoes envelope detection through a half-wave rectifier followed by a low-pass filter, allowing AM demodulation. The rectified voltage, V_{ENV}, is subsequently shaped by a current sink and a low-pass filter. The current sink

determines the fall slope of V_{ENV}, while the low-pass filter determines the rise slope of V_{ENV}. The envelope signal and a reference voltage from the bandgap circuit are fed into a hysteresis comparator with a 45 mV hysteresis window. Amplitude transitions at the input nodes produce a binary output from the comparator, which is sent to the PPM data recovery circuit (Fig. **??** (b)) for further processing.

The PPM data recovery process begins by converting the binary pulse signal V_{ENV} into a sawtooth waveform. The pulse duration determines the sawtooth signal's peak amplitude and is compared against a reference voltage (0.9 V). A hysteresis comparator then converts pulses of varying durations into digital signals. Synchronized with the extracted clock signal CLK_PPM (V_{ENV} frequency divided by 2), the data signal DATA_PPM is finally recovered. A conceptual waveform illustrating this downlink data recovery process is shown in Fig. **??** (d).

At the end of the downlink phase, preamble detection is performed. If the received preamble codes match the predefined sequence ([1, 0, 1] in this design), the enable signal 'DATA_EN' is activated to latch the received data bits. These bits are used to reconfigure the wireless chip. After every successful downlink communication between the wireless chip and the external device, the data temporarily stored in the shift register arrays must be reset to ensure a correct ID detection before the next event. This is done by generating a reset signal 'DATA_CLR' (Fig. **??** (c)) following 'DATA_EN'. The reset signal is triggered under one of the following cases: (i). the power-on reset is enabled (enabled when $'POR' = 0$, all register bits are reset to 0), (ii). a specific timing interval after 'DATA_EN' happens, and (iii). the watchdog circuit output is triggered. The watchdog circuit enhances the reliability of the downlink process by addressing potential reset signal 'DATA_CLR' failures to prevent erroneous ID detection.

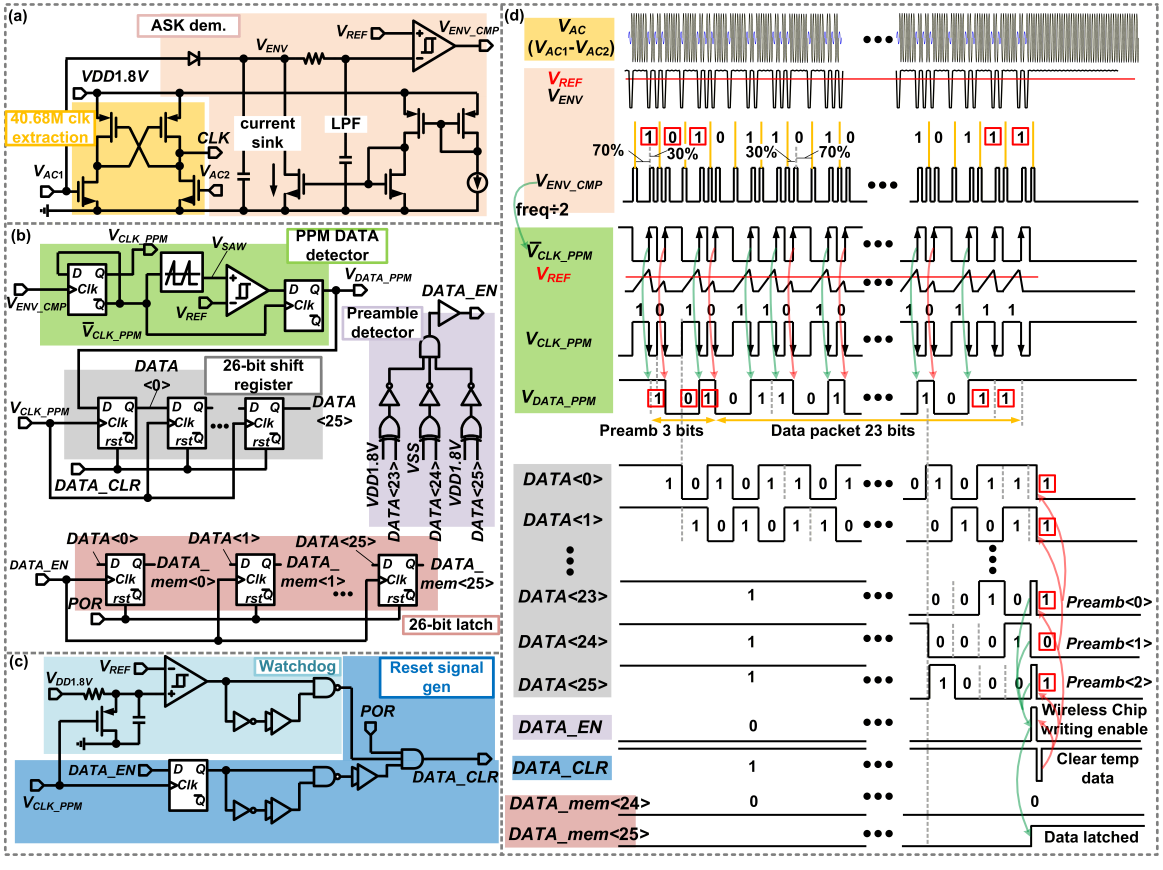


Figure 3.16: The circuit implementation of (a) ASK demodulator for downlink data telemetry, (b) Data recovery circuit and 3-codeword preamble detector, (c) register clear signal generation circuit, and (d) Conceptual waveforms of downlink data communication.

3.3.3 Impulse-radio ultra-wide-bandwidth for uplink data modulation

Ultra-short pulses are used in IR-UWB transmitters to achieve low-power communication. Compared to its LO-based counterpart, the delay-chain-based pulse generator [52] offers near-zero static power consumption and ultra-fast startup time, making it highly efficient for energy-constrained applications. This architecture is based on edge-combined delay signals, as illustrated in Fig. 3.17(a). Upon detecting an incoming data edge, an ultra-short pulse (D_0) is generated in the first phase (ϕ_1). This initial pulse propagates through a delay chain with a fixed delay equal to the period of D_0, sequentially producing additional delayed pulses (D_1 in phase ϕ_2 and D_2 in phase ϕ_3). These pulses are then combined in the time domain at a designated node, typically the output node of the power amplifier or driver. To meet the wideband spectrum requirements, a band-pass filter implemented using two LC resonators is placed after the driver output. This filter shapes the final output voltage at node D for transmission. The band-pass filter must be designed with an appropriate loaded quality factor Q to balance the trade-offs among frequency roll-off, emission power loss, and pulse ringing effects. The conceptual frequency response of the band-pass filter network is illustrated in Fig. 3.17(a), exhibiting a peak response at the desired resonant frequency f_0, followed by a roll-off with a slope of −20 dB/dec beyond the passband. The corresponding timing diagram is depicted in Fig. 3.17(b). Notably, the duration of each pulse, along with the total pulse sequence duration, determines the frequency and bandwidth of the UWB RF carrier signal (D), respectively. The amplitude of each pulse determines the emission power of the carrier signal.

The circuit implementation of the above concept can be found in [49] (Fig. 3.18(a)). In the original design presented in [49], only the rising edge of the incoming signal at the input is detected and converted into a short-duration pulse by the first cell (single pulse cell 0 in Fig. 3.18 (a)). A chain of cascaded pulse cells then generates a combined pulse sequence, as shown in Fig. 3.10(c) and Fig. 3.17(b). The structure presented in [49] has the main drawback of only focusing on rising edge detection and pulse conversion. While this approach works for basic input signals, it becomes insufficient for Manchester-type encoded data, where both the rising and falling edges carry critical information that must be converted into pulses. An example of an error bit appearing in the data decoding process due to the single-edge detection is illustrated in Fig. 3.18 (b). Assuming a missing rising edge detection appears in the third data bit (marked as the grey curve), the data decoder in the Rx side translates this data bit as ’0’ instead of ’1’ by mistake. However, if the falling edge can also be converted into a pulse, such a problem can be avoided.

To address this limitation, this design enhances the original structure

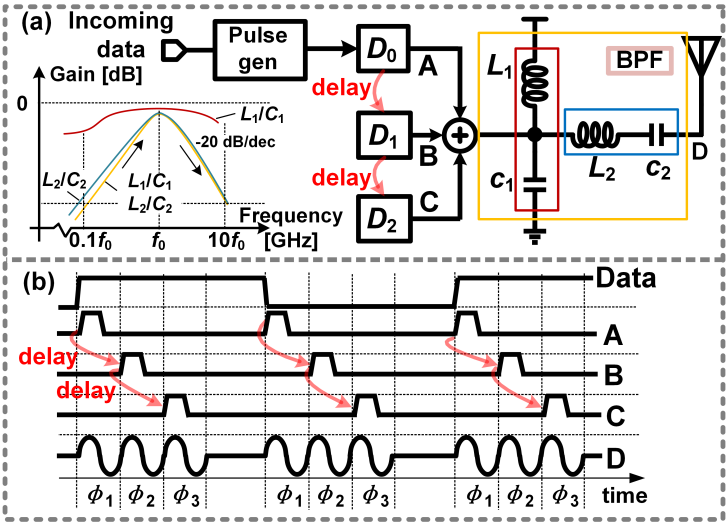


Figure 3.17: (a) The edge combining concept, (b) The signal shape in each node.

by incorporating dual-edge detection, allowing both the rising and falling edges of the input data to be effectively converted into pulses. This improvement ensures compatibility with Manchester encoding.

Unlike conventional designs that employ XOR gates with long propagation delays in the output stage [53], the proposed architecture increases the achievable center carrier frequency by shifting the XOR logic to the input stage, forming a dual-edge pulse generator. Simultaneously, the XOR-based output logic in conventional single-pulse cells is replaced with an AND gate implementation. Since the XOR logic is positioned in the first stage, its output is further processed into ultra-short pulses by subsequent delay chains. As a result, the long propagation delay of the XOR logic does not impact the final output pulses.

The dual-edge pulse generator and single-pulse cell serve as the fundamental building blocks of this approach, facilitating improved frequency performance while maintaining design simplicity. The dual-edge pulse generator (Fig. 3.19 (a), marked in the blue square) employs XOR logic to produce short-duration pulses (0.6 ns) by comparing a signal with its delayed version. This block receives Manchester-encoded data as input and converts both the rising and falling edges of the data into output pulses. In the single pulse cell (Fig. 3.19 (b), an AND gate logic is employed to transform the incoming pulses (from the dual-edge generator) into delayed signals. Each signal features programmable amplitude, controlled by a 3-bit amplitude tuning command, and programmable delay, controlled by a 3-bit delay tuning command. To minimize power con-

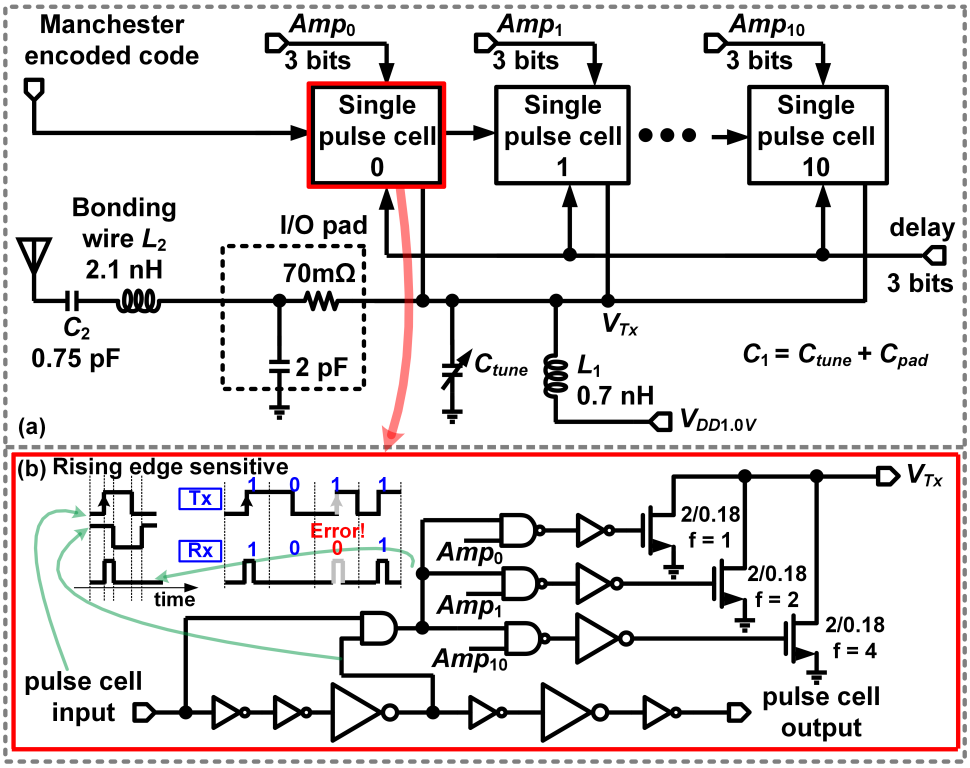


Figure 3.18: (a) The circuit implementation of the edge-combine-based UWB IR transmitter with a rising-edge pulse generator, (b) the circuit implementation of the single pulse cell with rising-edge sensitivity.

sumption, the amplitudes of these cells are distributed according to a Gaussian profile, while the delay of each cell is fixed at 0.25 ns, corresponding to 4 GHz in the frequency domain. The chip integrates 10 pulse cells, generating a signal bandwidth of 0.8 GHz. This bandwidth, defined as the spacing between the two -10 dB sidelobes, is designed to ensure compliance with the FCC spectral mask (3.1 GHz to 10.6 GHz in the US, 3.4 GHz to 4.8 GHz and 6 GHz to 8.5 GHz in Europe) while avoiding interference with the 5 GHz communication band. After the pulse conversion is completed, all transistors remain in an off state, thereby eliminating static power consumption until the next transmission. The outputs of the delay cells converge at the node V_{TX}, which is connected to a band-pass filter composed of two resonators: the parallel-connected L_1C_1 (consisting of C_{tune} and C_{pad}) and the series-connected L_2C_2, as shown in Fig. 3.20(b). Here L_1 is a 0.7 nH on-chip spiral inductor (Fig. 3.20 (a)), while L_2 is a 2.1 nH bond wire inductor. The practical im-

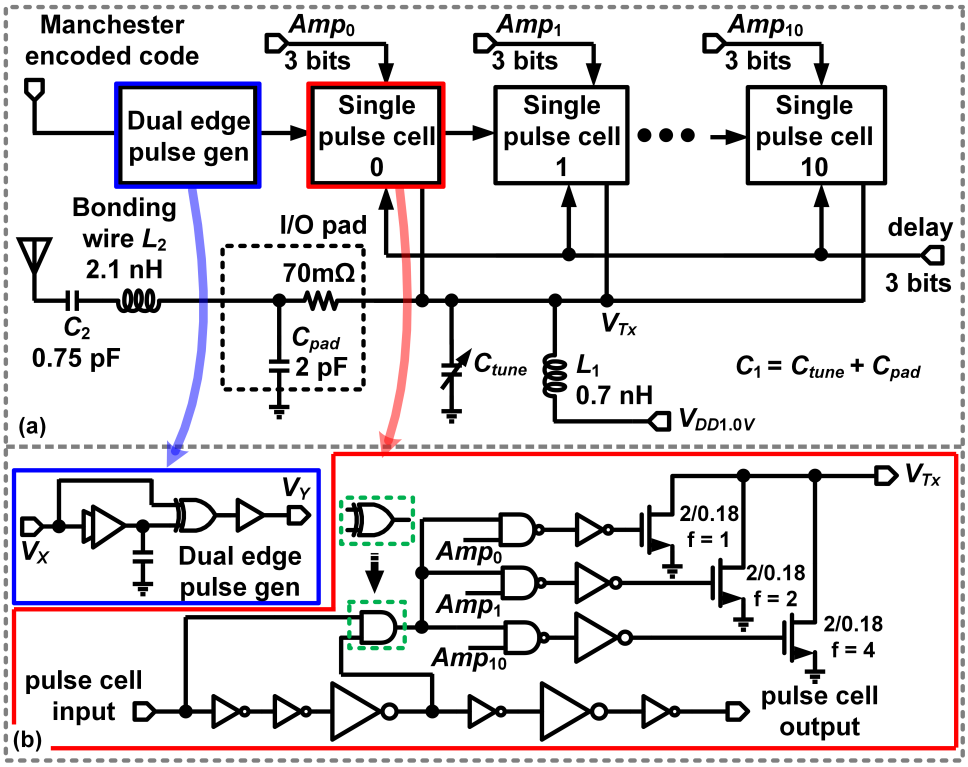


Figure 3.19: (a) The circuit implementation of the edge-combine-based UWB IR transmitter with a dual-edge pulse generator, (b) the circuit implementation of the dual-edge pulse generator and the single pulse cell.

plementation of the bandpass filter is illustrated in Fig. 3.20 (c). The bonding wire connecting the chip's I/O pad to the PCB pad behaves as an inductor, which can effectively save the limited on-chip area. Similar approaches are employed in UWB transmitter designs that necessitate an output bandpass filter to suppress low-frequency pulse components while enhancing resonance at the desired frequency [49, 54, 60]. This design incorporates a tunable on-chip capacitor C_{tune} to enable flexible capacitance adjustment for bandpass frequency tuning. The capacitor consists of two components: a fixed 1.1 pF MIM capacitor and a 5-bit MIM capacitor bank. The capacitor bank features a most-significant-bit (MSB) unit with a capacitance of 1.1 pF and a least-significant-bit (LSB) unit with a capacitance of 68.8 fF. The simulated frequency response of the bandpass filter demonstrates a flat attenuation over a wide frequency band, achieving a -3 dB bandwidth of 6.26 GHz with a center frequency of 4.0 GHz.

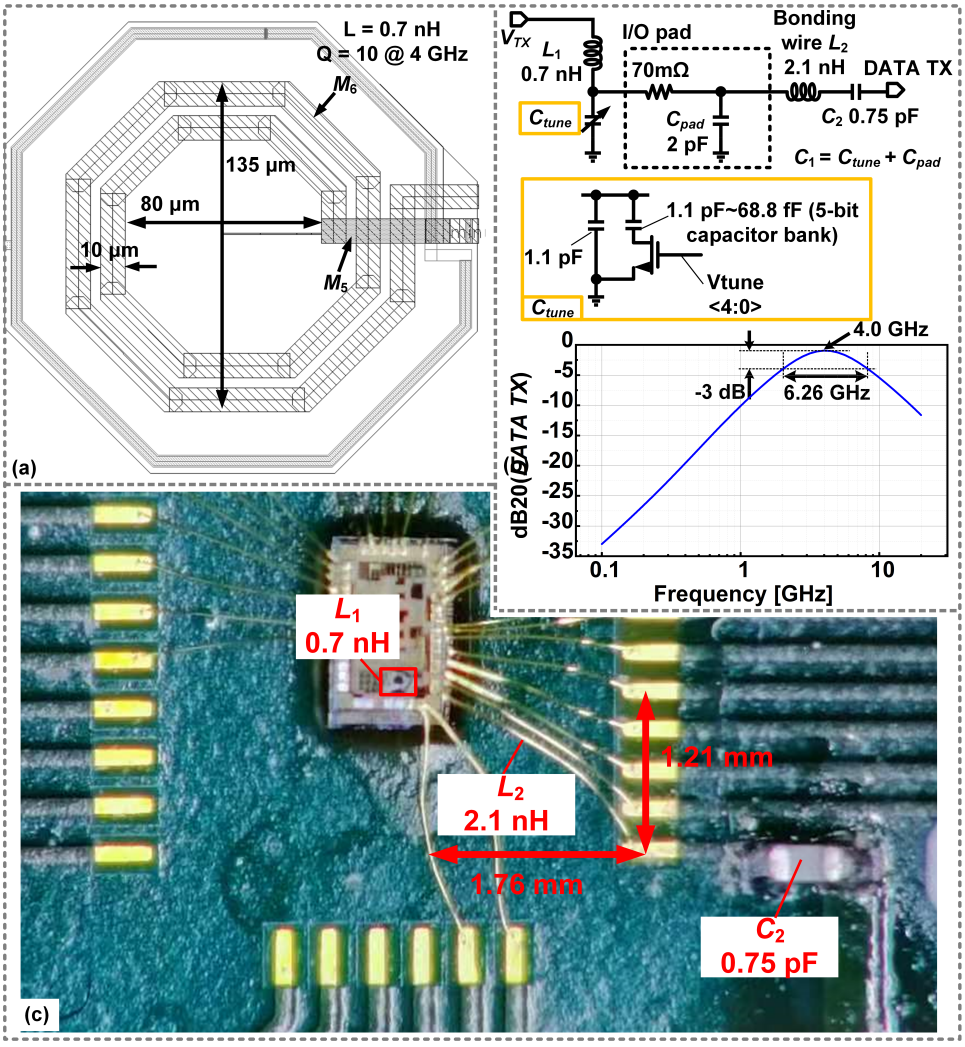


Figure 3.20: (a) The on-chip spiral inductor layout, (b) The simulated frequency response of the LC bandpass resonators, and (c) Photograph of the chip assembly showing the implementation of the bandpass filter at the transmitter output.

The following section describes the uplink data generation procedure and presents the simulation results of the corresponding transient waveforms. The uplink data is transmitted from the retina chip and subsequently converted into impulse radio waveforms by the transmitter driver. The uplink data packet consists of preamble bits for chip identification, recorded neural signals, and ADC codes used for closed-loop

power regulation. Since the data is initially in an n-bit parallel format, it must be serialized for wireless telemetry. Fig. 3.21(a) shows the top-level

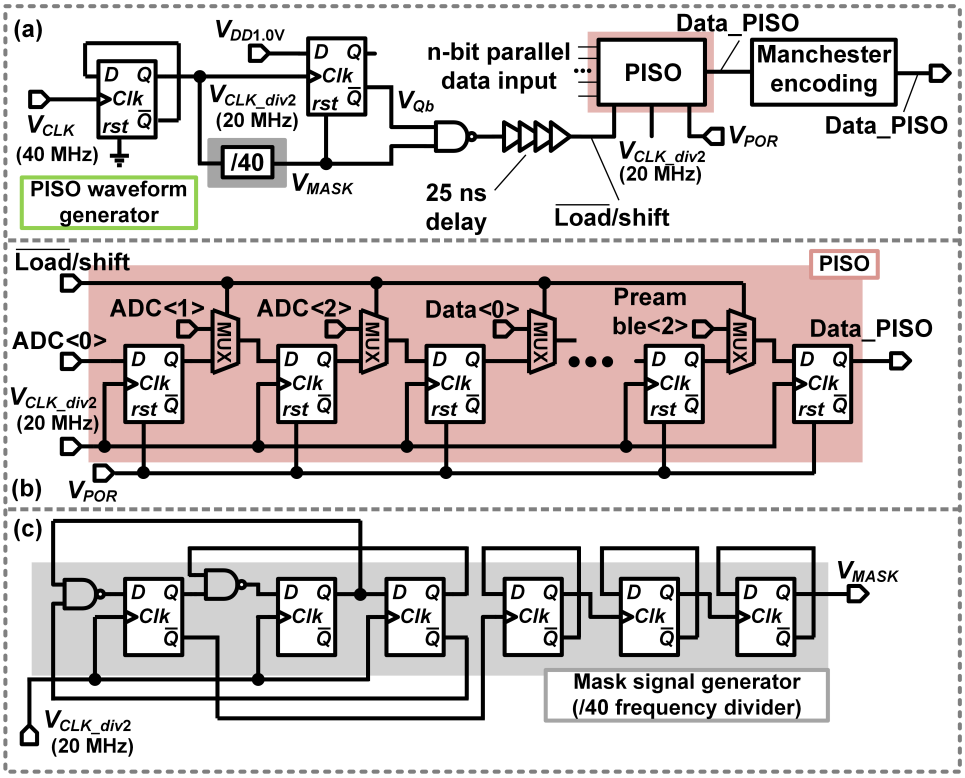


Figure 3.21: The circuit implementations of (a) the PISO waveform generator, (b) the PISO register array, and (c) the mask signal generator.

circuit implementation of a parallel-in-serial-out (PISO) waveform generator designed on the retina chip. The main block is a synchronous PISO register array, illustrated in Fig. 3.21(b), which is driven by a 20 MHz clock (V_{CLK_div2}) and a selection signal ($\overline{\text{load}}$/shift). When the selection signal is low, the n-bit parallel input data is loaded into the register array. Once the signal transitions from low to high, the array operates as a shift register, sequentially outputting each bit at the rising edge of V_{CLK_div2}.

The low phase of the selection signal spans one V_{CLK_div2} period (approximately 49.2 ns), with its rising edge positioned at the center of this interval to ensure sufficient setup and hold times. The high phase of the selection signal must be long enough to accommodate the intended number of bits. In the presented example, a high state duration of 489 ns ensures reliable telemetry of 10-bit data. As a result, the selection signal

operates at a lower frequency and a significantly smaller duty cycle than V_{CLK_div2}.

This timing control is achieved using a mask signal generator, as shown in Fig. 3.21(c). The generator, implemented with a NAND gate and a delay cell as seen in Fig. 3.21(a), produces a mask signal (V_{MASK}) through a divide-by-40 frequency divider composed of divide-by-5 and divide-by-8 submodules. When V_{MASK} is low, it forces the $\overline{Q}$ output of the D-flip-flop to '1' by asserting the reset pin. When V_{MASK} goes high, $\overline{Q}$ transitions from '1' to '0' after a one-clock-cycle delay (49.2 ns). A delay cell introducing approximately 25 ns of delay is inserted after the NAND gate to align the rising edge of V_{CLK_div2} near the midpoint of the $\overline{\text{load}}$/shift signal at its low state.

Fig. 3.22 presents the simulated waveforms of the PISO signal generator, validating its timing behavior and demonstrating its functionality in serializing parallel data for uplink telemetry.

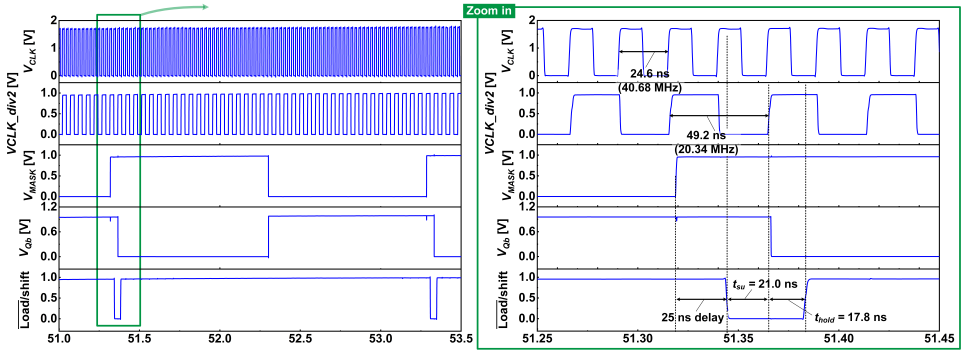


Figure 3.22: Simulated waveform of the PISO signal generator, with a zoomed-in view showing the duration of $\overline{\text{load}}$/shift and its timing relationship with V_{CLK_div2}.

Fig. 3.23 presents the simulated waveforms of the PISO output signal (DATA_UP) from the retina chip and the IR-UWB transmitter output (DATA_TX) from the wireless chip. To illustrate the functionality of the proposed design, the DATA_UP signal in this example consists of a 3-bit preamble for synchronization, a 4-bit data packet representing neural recording data, and a 3-bit ADC code for power regulation. Two time instances, around 57.5 μs and 59.5 μs, are selected to demonstrate how the ADC output codes vary with changes in the rectified voltage amplitude (V_{RECT}). The corresponding zoomed-in views are shown in the right panel of the figure, confirming that the digital codes are successfully converted into Gaussian-shaped pulses in Manchester-encoding form, enabling effective wireless telemetry via the IR-UWB transmitter.

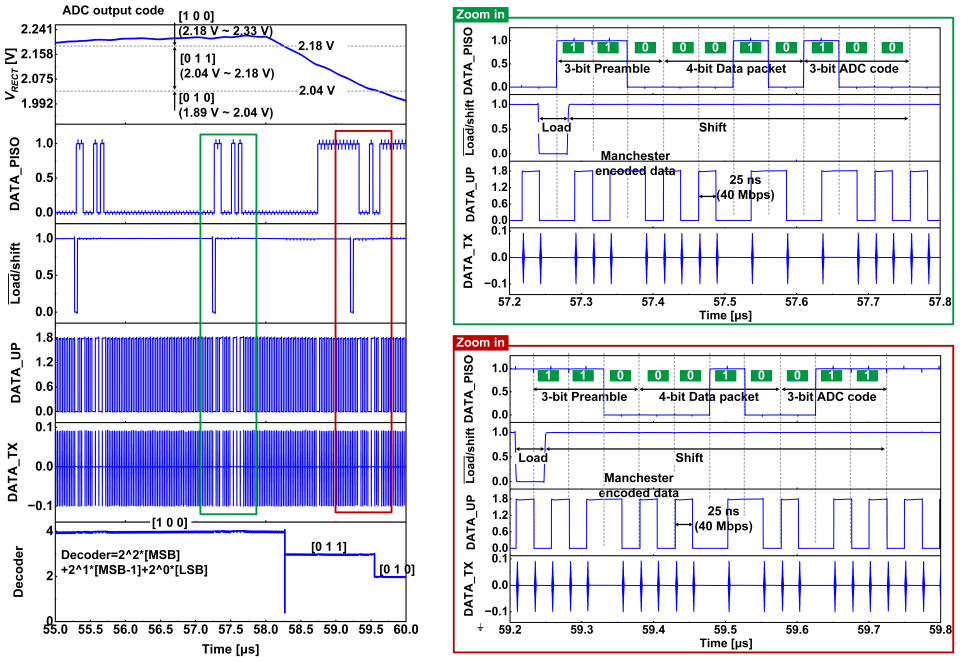


Figure 3.23: Simulated waveform of the IR-UWB transmitter output, demonstrating the closed-loop power regulation capability of the proposed design.

3.4 Experimental Results

The proposed wirelessly powering and communication system was fabricated using standard 180-nm BCD technology and wirebonded to an FR4 PCB to minimize parasitic effects. The chip micrograph (Fig 4.12) reveals that the design occupies a core area (active circuit area, excluding test I/O pads) of 0.55 mm^2, and a total area of 1.15 mm^2.

Measurements were conducted using a 200 MHz arbitrary waveform generator (Rigol DG4202), a 350 MHz digital oscilloscope (*DSOX3032A*), and a 44 GHz power spectrum analyzer (*Keysight E4446A*). However, due to the unavailability of a high-precision calibration kit for the Vector Network Analyzer (VNA) during the measurement process, the power coil link could not be accurately characterized. Consequently, wireless power transfer and data communication could not be performed through the wireless link. Instead, the following measurement results were obtained by directly connecting the function generator output to the AC input pads to validate the functionality of the prototype chip. For the same reason, the performance of the passive rectifier, implemented using Schottky diodes, was not measured under these conditions and is

therefore not presented in this section. However, a detailed investigation of an advanced active rectifier design, along with its measurement results for an identical wireless power transfer link, is provided in Chapter 4.

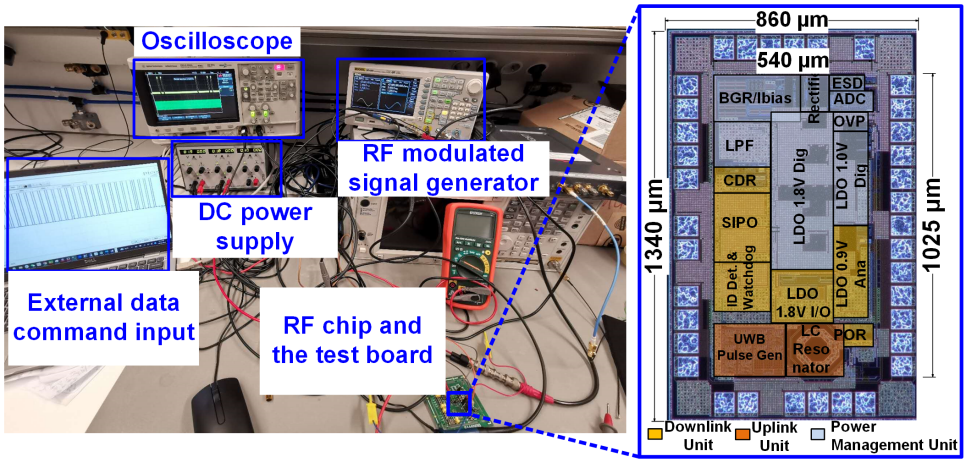


Figure 3.24: The measurement setup and the die photograph of the BCD 180-nm PMU chip.

3.4.1 Power-on reset and regulator startup measurement

The startup waveforms of the power-on-reset signal and the regulated voltage supplies (0.9 V, 1.0 V, and 1.8 V) were measured under a 2 V voltage applied to the output of the rectifier, V_{rect}. As shown in Fig. 3.25 (top), the power-on reset delay is measured to be 20.69 ms, corresponding to a 60 ms rising edge of V_{rect}. The power-on reset stabilizes at 1.8 V, which is the output voltage of the 1.8 V regulator.

Fig. 3.25 (bottom) presents the startup waveforms of the regulators at different output voltage levels. After an approximately 11.31 ms delay, primarily determined by the *RC* time constant of the low-pass filter at the bandgap voltage reference output, the 0.9 V and 1.0 V regulator output voltages rise and eventually settle at their predefined levels. Meanwhile, the 1.8 V regulator output tracks the rising edge of V_{rect} before stabilizing. These measurement results confirm both the accuracy of the DC voltage levels and the stability of the regulator design during the startup process.

3.4.2 Voltage Regulator Measurement

This section reports the LDO load regulation performance and power-supply rejection ratio performance.

Fig. 3.26(a) illustrates the setup used to measure the load regulation

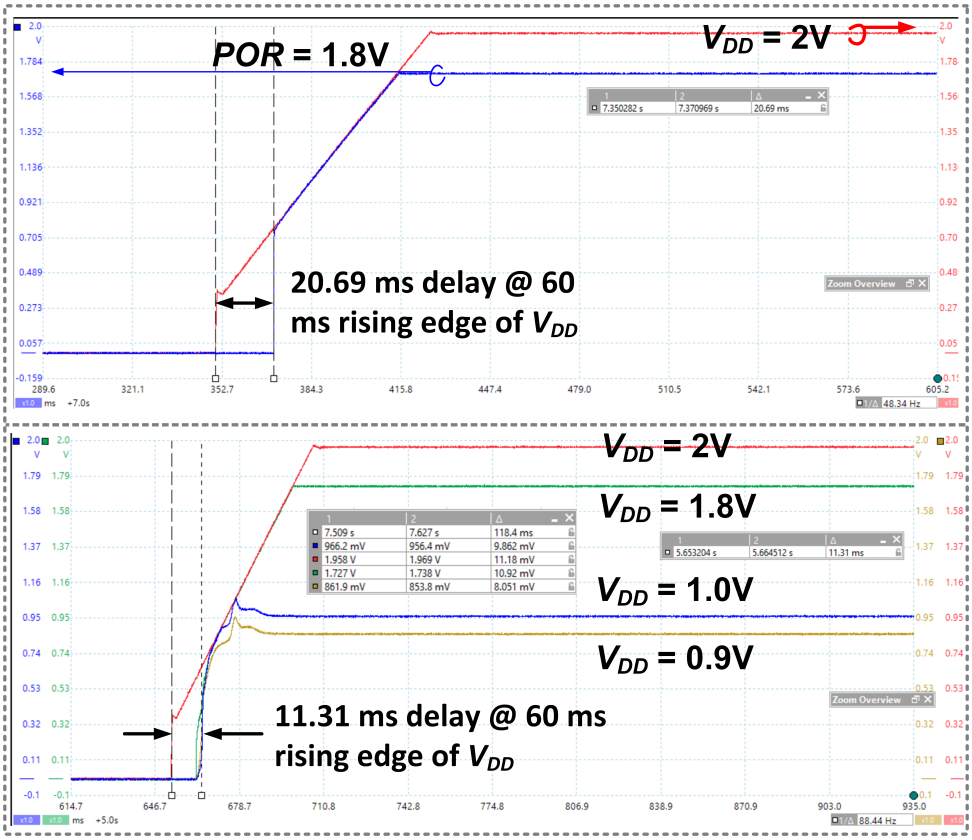


Figure 3.25: Measured start-up procedure of the power-on-reset signal and the 0.9/1.0/1.8V regulator outputs.

performance of the 1.8 V main regulator, with the corresponding waveforms shown in Fig. 3.26(b). The power supply node is connected to a source meter (Keithley 6430), while the output node is loaded with a 360Ω resistive load, corresponding to a 5 mA current loading. A high-speed, off-the-shelf NMOS transistor switch is used to connect the resistor to the ground, with its gate driven by a square wave generated by a function generator. The rise and fall times of the switching signal are set to 15 ns. The measured load transient response (depicted by the green waveform) demonstrates an overshoot of +96 mV and an undershoot of -120 mV, which closely align with the post-layout simulation results of +99 mV and -95 mV, respectively. The discrepancy can be attributed to fabrication-induced variations in the fast loop FVF buffer's bandwidth within the regulator circuit. After reaching the peak overshoot or undershoot, the output voltage gradually stabilizes at 1.8 V, with the settling time determined by the slow loop bandwidth.

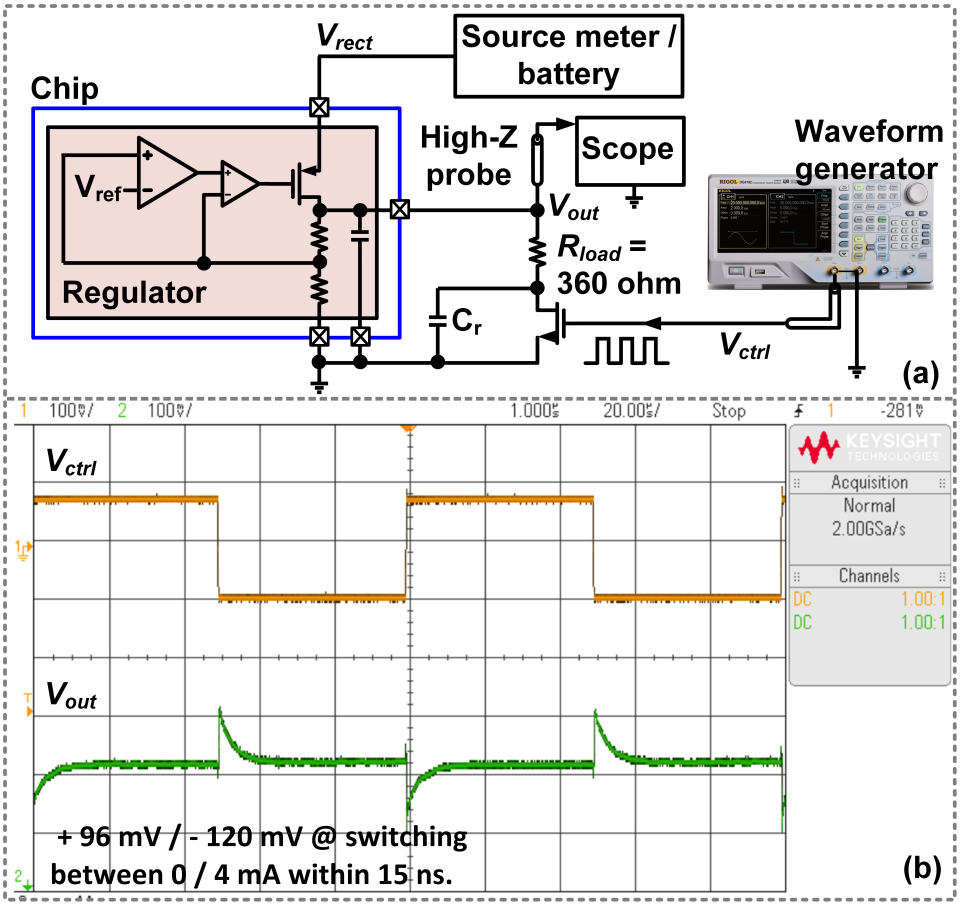


Figure 3.26: (a) The voltage regulation measurement setup, and (b) the measured load transient performance of the 1.8V regulator.

The dual-loop structure employed in the regulator design ensures robust load regulation performance during transitions between light and heavy loads. The design exhibits no stability issues, highlighting its reliability under varying load conditions.

Fig. 3.27(a) illustrates the measurement setup used to evaluate the PSR performance of the proposed low-dropout regulator (LDO). The low-frequency ripple is suppressed by the high-gain operational amplifier in the slow feedback loop, while the high-frequency ripple is attenuated by the output capacitor.

To assess the ripple reduction performance, the regulator's power supply consists of a combined AC and DC voltage source. The AC component, with a small amplitude, is generated by a function generator, while

the DC voltage bias is provided by a source meter. The input and output voltage ripples are measured using an oscilloscope (or a spectrum analyzer). To analyze the PSR in the interested frequency, the acquired waveforms are converted to the frequency domain using fast Fourier transform (FFT), and the PSR is computed based on the difference between the spectral components of the input and output signals.

Fig. 3.27(b) and Fig. 3.27(c) depict the measured PSR performance (blue curves) of the 1.8 V and 0.9 V regulators, respectively. For the 1.8 V regulator, the measured PSR at 40.68 MHz under heavy load conditions is -12.35 dB, compared to the post-layout simulation result of -7.8 dB. Similarly, for the 0.9 V regulator, the measured PSR at 40.68 MHz under heavy load conditions is -9.7 dB, while the simulated value of -20.16 dB. The discrepancy observed between the measured and simulated results is likely attributable to process variations that affect the amplifier's gain, as well as inaccuracies introduced by the measurement setup.

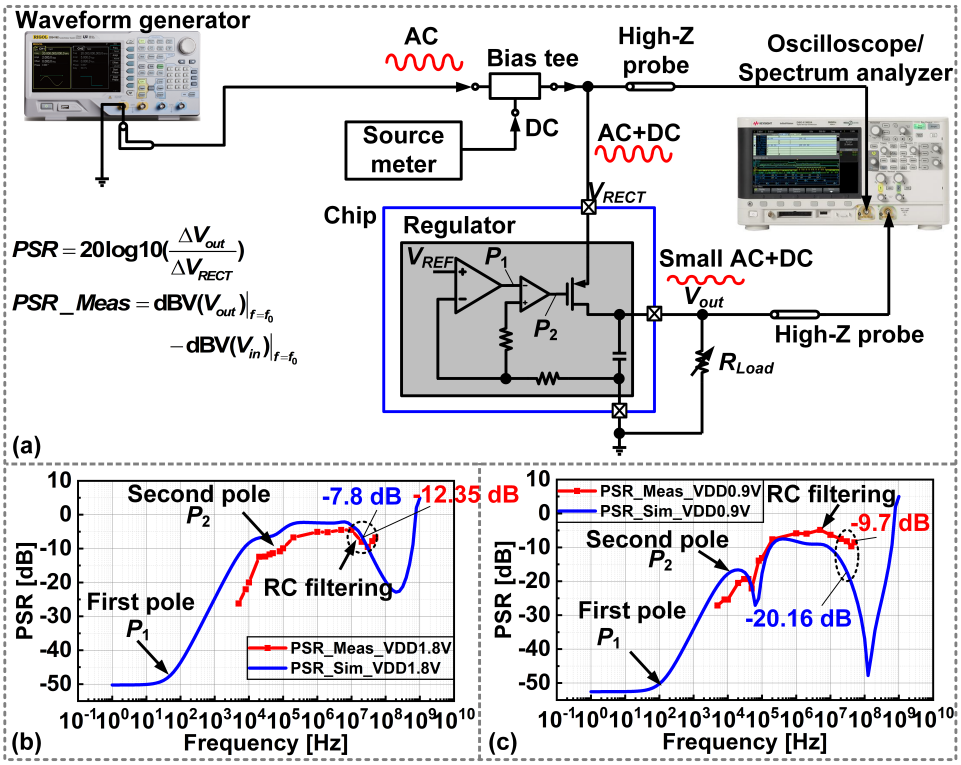


Figure 3.27: (a) Measurement setup of the LDO PSR, (b) Simulated (post-layout) and measured PSR of the 1.8V regulator, and (c) Simulated (post-layout) and measured PSR of the 0.9V regulator.

3.4.3 Downlink communication measurement

This section reports measurement results of successful data and clock recovery from the downlink communication.

Fig. 3.28 and Fig. 3.29 present the measured V_{DATA_PPM} (top panel) to validate the downlink data decoding process under different modulation indices (0.68 and 0.26, respectively). The bottom panel illustrates the AC input voltage, V_{AC}, which comprises a 40.68 MHz power carrier signal combined with a 200 kbps modulated data signal. In this measurement, the V_{AC} is directly driven by the function generator instead of a coil, as explained in Section 3.4. The transmitted data sequence includes a preamble of three bits followed by 23 bits of data content. The PPM data pattern is generated on a laptop and transmitted via a USB interface to a function generator. In both modulation index cases (0.68 and

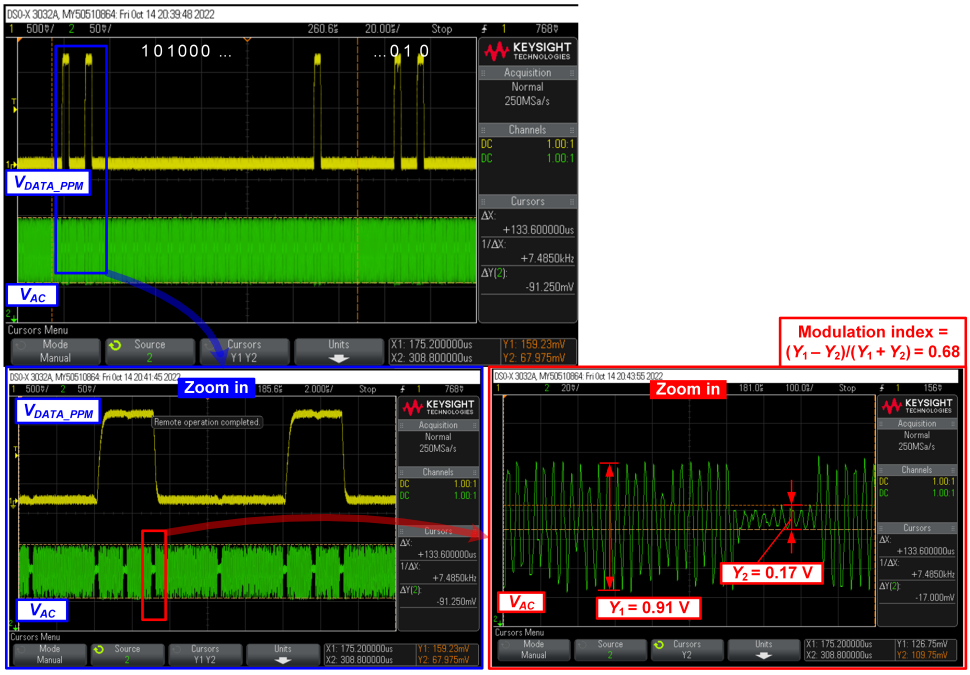


Figure 3.28: Measured downlink data recovery waveform with a 0.68 modulation index.

0.26), the predefined data packet, [1 0 1 0 0 ... 0 1 0], is successfully recovered from the modulated AC signal, validating the proposed ASK-PPM scheme (Fig. **??**) for downlink data communication. However, measurement results indicate that a modulation index of 0.26 represents the lower bound for reliable data recovery. Below this threshold, successful decoding is not achieved, deviating from simulation expectations (further discussed in Section 3.5). A potential reason for this discrepancy is that

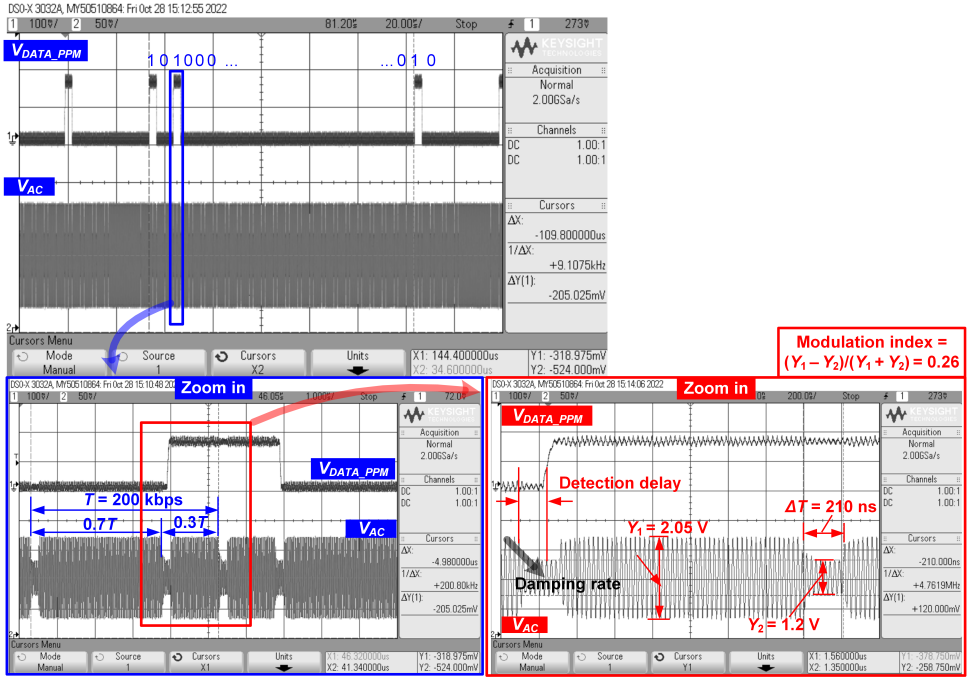


Figure 3.29: Measured downlink data recovery waveform with a 0.26 modulation index.

the damping rate of V_{AC} in practical measurements exhibits a flatter response compared to simulations, leading to a slower envelope extraction by the ASK-PPM demodulator. This results in a detection delay of approximately 160 ns, as observed in Fig. 3.29. Given that the pulse duration in its lower voltage state is limited to $\Delta T = 210$ ns, lower modulation index cases may suffer from insufficient response time. Nevertheless, the ASK-PPM scheme achieves a substantial improvement in power efficiency compared to conventional ASK-based schemes, even at a high modulation index, demonstrating approximately a 75.3% efficiency gain when the modulation index is 0.26 (Fig. 3.7).

In addition to data download, clock recovery from the power carrier signal is verified. Fig. 3.30 illustrates the measured V_{CLK} waveform (the green curve) to validate the clock recovery function. The V_{AC} voltage, shown in the top panel, is identical to that in Fig. 3.29 corresponding to a modulation index of 0.26. Due to the limited driving capability of the 1.8 V I/O pads, a 3.3 V digital buffer (74AUP1G126GW) is connected after the V_{CLK} pad and is tested using a passive probe. The measurement result shows that the recovered clock signal has a 50% duty cycle, which can be used by other digital logic. The simulated shmoo plot for clock

recovery, shown in Fig. 3.30 (bottom-right), confirms that the selected modulation index of 0.26 falls within the simulated acceptable range for clock recovery.

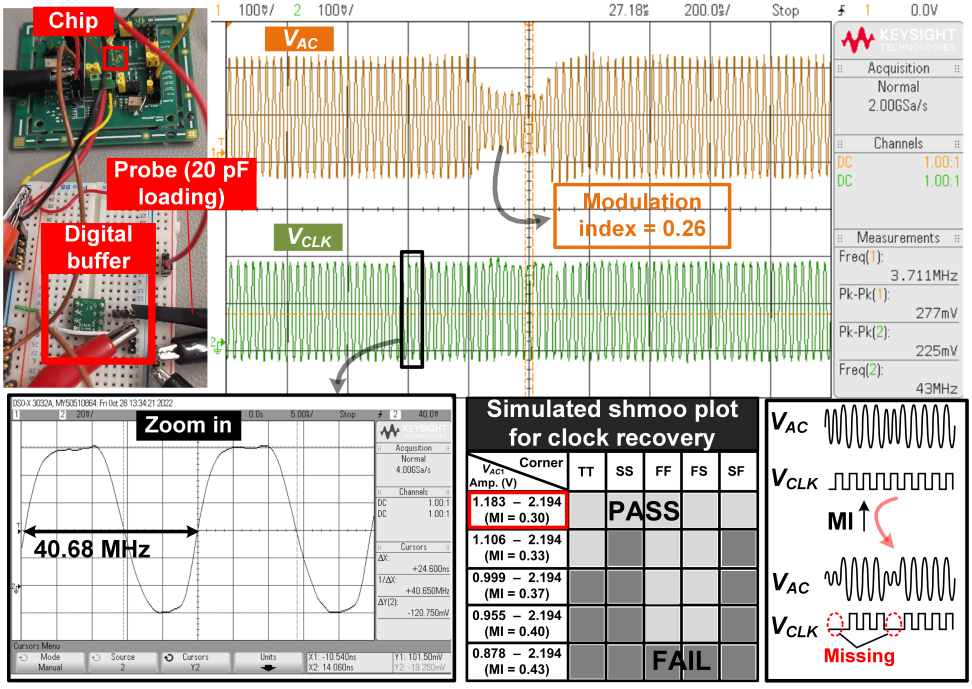


Figure 3.30: Measured clock recovery waveform with a modulation index of 0.26, aligning with the simulated modulation index range for clock recovery.

3.4.4 Uplink communication measurement

Fig. 3.31(a) presents the measured frequency-domain representation of the IR-UWB pulse. The measurement results demonstrate a wide frequency tuning range from 2.16 GHz to 4.56 GHz, including 4.05 GHz, thereby verifying the concept of high-frequency carrier generation through short propagation delay pulse sequences. However, the measured emission power is significantly lower than the simulated results (-45/-49.8 dBm/MHz at 3/4 GHz in simulation, compared to -64.45/-70.85 dBm/MHz in measurement). This discrepancy is because of the parasitic components in the I/O pad, which were not properly modeled during the design phase. As depicted in the top-left inset of Fig. 3.31(a), the parasitic capacitance to ground introduces an unintended leakage path, altering the resonance condition of L_2 and C_2. To mitigate this issue, Focused Ion Beam (FIB) modification was applied to adjust the internal metal interconnections, as

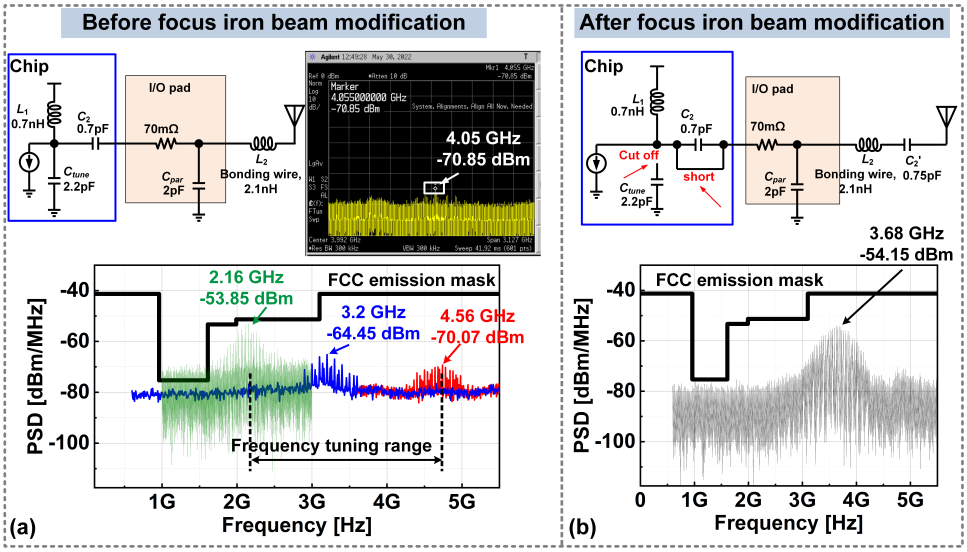


Figure 3.31: Measured power spectral density of the uplink transmitter output in the UWB band: (a) before FIB modification and (b) after FIB modification. The measurement results validate the proposed design's wide center carrier frequency tuning range, spanning from 2.16 GHz (the green curve) to 4.56 GHz (the red curve). After mitigating the emission power leakage caused by parasitic components in the I/O pad, the peak emission power is improved by approximately 10 dBm/MHz.

shown in Fig. 3.31(b). Specifically, the internal capacitor connections of C_{tune} and C_2 were modified by disconnecting and shorting them, respectively. Consequently, C_{par} and C_2' serve as the new resonant capacitors for L_1 and L_2. Post-modification measurements indicate an improvement of approximately 10 dBm/MHz in transmitter output power. With a repeated 20 Mbps data sequence (Manchester-encoded), the transmitter achieves a center frequency of 3.68 GHz and a signal power level of -54.15 dBm/MHz. However, as the frequency increases beyond 4 GHz, the signal power degrades due to the shift in the resonance state of the output band-pass filter, formed by L_1C_{par} and L_2C_2'. The measured power spectrum confirms compliance with the FCC emission mask for both indoor and outdoor applications, demonstrating over 20 dB of sidelobe suppression without requiring any off-chip filters or external frequency generators.

The power spectral density (PSD) -10 dB bandwidth is approximately 800 MHz, defined by the edge-combined pulse sequence (10 pulses,

each with a 0.25 ns pulse duration). This wide bandwidth ensures compliance with the FCC mask and strong immunity to interference from other frequency bands, including 2.4 GHz (Wi-Fi), 3 GHz, and 5 GHz.

The power consumption of the transmitter was analyzed at a fixed 20 Mbps uplink data rate, as shown in Fig. 3.32. The transmitted pulse energy is 16.37 pJ/bit, which is calculated based on the average power measurement results.

3.4.5 Power breakdown

The wireless chip provides voltage supplies for the loading retina chip. The latter has three main working phases: the neural recording phase, the stimulation phase, and the standby phase. Since the neural recording phase consumes most of the power (Section 1.1), special attention is given to the neural recording phase measurement, where the measurement setup is shown as Fig. 3.32 (a). A source meter with a 2-V DC supply is fed to the rectifier stage output to measure the power change when enabling or disabling each circuit block. Therefore, the power consumption of each circuit block with its supply voltage rails can be approximately calculated, as shown in Fig. 3.32 (b) and (c), where simulated and measurement results are provided. The comparison indicates a good consistency of total power consumption between these two results. In measurement, most of the power consumption after the rectifier stage comes from the main regulator output $V_{DD1.8V}$, occupying 44.3% (2.7379 mW) of the overall power consumption (6.053 mW). This is the power dissipation on the power switch of the $V_{DD1.8V}$ regulator. The remaining part of the power consumption is distributed relatively equally between (i) the power consumed by the IR-UWB Tx driver (0.6548 mW), (ii) the 860 Ω resistive load at the $V_{DD0.9V}$ output (0.9292 mW), (iii) the 1000 Ω resistive load at $V_{DD0.9V}$ output (0.8671 mW), and (iv) the I/O pads power consumption (0.9932 mW) with their dedicated $V_{DD1.8V}$ voltage supply regulator. The IR-UWB transmitter consumes less power than the simulated result (0.726 mW), resulting in a lower center carrier frequency and a lower signal amplitude. The measured PSD of the transmitter pulse is -54.15 dBm/MHz in the center frequency (Fig. 3.31), while the simulated result is -45.46 dBm/MHz. Regarding the remaining part of the power consumption, the I/O pads' power consumption can be removed from the calculation since only a few I/O pads remain functional in a practical implant chip. The overall system efficiency is 47.23% (I/O pads power consumption is excluded) and is limited by the efficiency drop in the 1.8 V to 0.9 V regulation. Chapter 4 addresses this main limitation and designs a new PMU to achieve high power conversion efficiency in applications where dual outputs are required and most of the power is consumed by the low-voltage output.

Table 3.2: Comparison to state-of-the-art wireless power transferring with bi-directional data communication system designs

Item	JSSC'15 [7]	TBCAS'16 [8]	TBCAS'17 [4]	CICC'19 [9]	JSSC'21 [61]	RFIC'22 [10]	This work
Process	65-nm	180-nm	180-nm HV	65-nm	180-nm	180-nm	180-nm BCD
Test condition	30 mm meat	36 mm tissue	Spinal cord implant in a rat	8 mm liquid brain phantom	Retina implant	60 mm implant	14 mm air
Power carrier frequency (MHz)	1	13.56	2	30	13.56	0.34	40.68
Link type	Ultrasonic + inductive	Inductive	Inductive	Inductive	Inductive	Magnetoelectric	Inductive
No. of link pairs		2	2[1]	2	1	2	2
Downlink topology	ASK	OOK	DPSK	ASK-PWM	Pulsed ASK	Pulse duration encoding[2]	ASK-PPM
Downlink data rate	10 kbps @ 1 MHz carrier	100 Mbps @ 2.4 GHz carrier	2 Mbps @ 20 MHz carrier	1000 kbps @ 900 MHz carrier	100 kbps @ 13.56 MHz carrier	62.3 kbps @ 0.34 MHz carrier	200 kbps @ 40.68 MHz carrier
Uplink topology	IR-UWB (LC osc + PA)	IR-UWB (edge combining)	LSK	LSK	LSK	LSK	IR-UWB (edge combining)
Uplink data rate	N/A	100 Mbps @ (3.1-7) GHz carrier	2 Mbps	10 Mbps @ 900 MHz carrier	N/A	40 kbps @ 31 MHz carrier	20 Mbps @ 3.8 GHz carrier
Uplink energy dissipation (pJ/bit)	9+18	10.8	N/A	N/A	N/A	N/A	16.37
Output voltage	1.0V	1.2/1.8V	$\pm$ 1.8V, $\pm$ 12V	1.5	$\pm$ 3V	2.8	0.9/1.0/1.8V
Reference clock generation	Ring osc	N/A	Ring osc/external	Oscillator	Clock recovery	Clock recovery + ring osc	Clock recovery
Auxillary circuits	OVP+POR	N/A	POR	N/A	POR	N/A	OVP+POR
Global regulation	No	No	No	No	Yes	Yes	Yes
Die area (mm^2)	31.2	0.8	25.08	0.25	5	0.99	1.15

[1] Including a power link and a duplex data link [2] Similar to ASK-PWM, but this scheme encodes multiple bits into a single pulse to compensate for the transducer's low switching speed

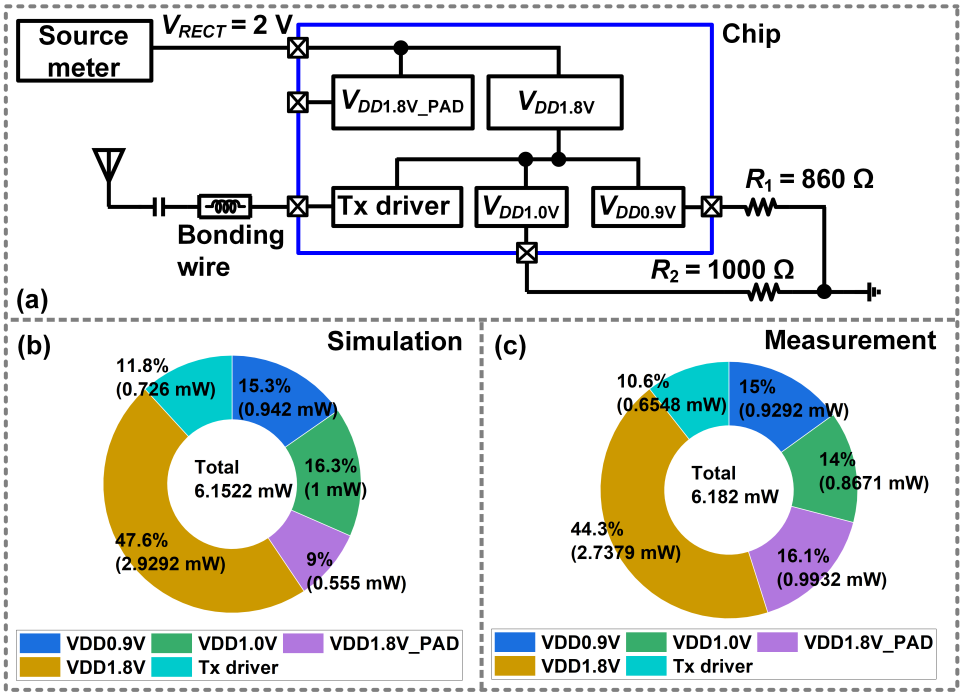


Figure 3.32: (a) The test setup for evaluating the power distribution of the chip. $V_{DD0.9V}$ and $V_{DD1.0V}$ are connected to an 860 Ω and a 1000 Ω resistive load, respectively, to simulate the loading condition of the retina chip operating in the neural recording phase, (b) and (c) The simulated and measured power breakdown of the chip.

3.4.6 Comparison with state-of-the-art

Table 4.2 summarizes the performance of the proposed data communication system, comparing it with state-of-the-art designs that employ both downlink and uplink functionality. Most of these designs use separate links for downlink and uplink to avoid message collisions [7–10]. The design in [61] uses only one single coil link for power/clock recovery and duplex data telemetry, but the data rate of the uplink communication is not reported.

ASK modulation and its variants are widely adopted in [7–10,61]. Specifically, [9] uses the ASK-PWM modulation scheme to achieve inherent synchronization of data and clock, eliminating the need for an accurate clock reference. However, the power carrier signal with ASK-PWM modulation exhibits a higher ripple swing [62] on the recovered voltage, due to the longer duration of the lower-level signal compared to the ASK-PPM modulation scheme used in this work.

This design employs IR-UWB with edge combining to achieve energy-efficient, high-data-rate uplink communication. The energy consumed per bit (16.37 pJ/bit) is lower than that of [62], which uses a conventional local oscillator and power amplifier structure. Additionally, the achievable uplink data rate (20 Mbps) is higher than that of other designs that use LSK for back-telemetry communication.

This design supports analog, digital, and high-voltage stimulation circuits with three different regulated voltages. The reference clock is directly extracted from the power carrier signal, as in [10, 61], thereby circumventing the problem of noisy clock signals generated by on-chip oscillators, as seen in [4]. This design also achieves both local voltage regulation (over-voltage protection and regulator circuits) and global voltage regulation (voltage monitoring ADC), enabling intelligent power level control, a feature not implemented in other works.

3.5 Sampling-based envelope detector

An envelope extractor is a critical circuit block for successful data recovery. Conventional RC-based averaging circuits are very sensitive to the RC time constant of the rectifier output, V_{ENV} (see Fig. 3.33 (a)). The limited sensitivity of the detector circuit may result in failed data recovery if the RC time constant is not properly optimized. If the RC time constant is too long (Fig. 3.33 (b) top), the capacitor discharges too slowly to track rapid changes in the modulating signal, leading to insufficient envelope change for comparison. Conversely, if the RC time constant is too short (Fig. 3.33 (b) bottom), the capacitor discharges too quickly, and the carrier ripple significantly impacts the comparison accuracy. An optimal RC time constant can balance these effects, ensuring accurate envelope extraction. The optimal value of RC time constant can be derived as Eq. (3.7) (the derivation can be found in Appendix):

$$\frac{1}{2\pi f_C} \ll RC \ll \frac{1}{2\pi f_M}\frac{\sqrt{1-\mu^2}}{\mu} \tag{3.7}$$

where f_c is the power carrier frequency (40.68 MHz), f_M is the data rate for downlink modulation (200 kbps), and μ is the modulation index. Assuming $\mu = 0.5$, an intermediate value of RC (10 times away from the upper/lower boundary), and fixing the capacitor to be 1 pF, the allowable variation range of the resistor for current sinking is only 49 kΩ with a nominal resistance of 88 kΩ. Considering the PVT variation, this small range of resistance choice marginally meets the ASK demodulation requirement. Additionally, the constant current leakage path continuously consumes power from the Rx coil input, making the conventional RC-based averaging circuit both less robust and energy inefficient. While some alternative designs circumvent these issues by using capacitor-less approaches, they come with specific limitations. These

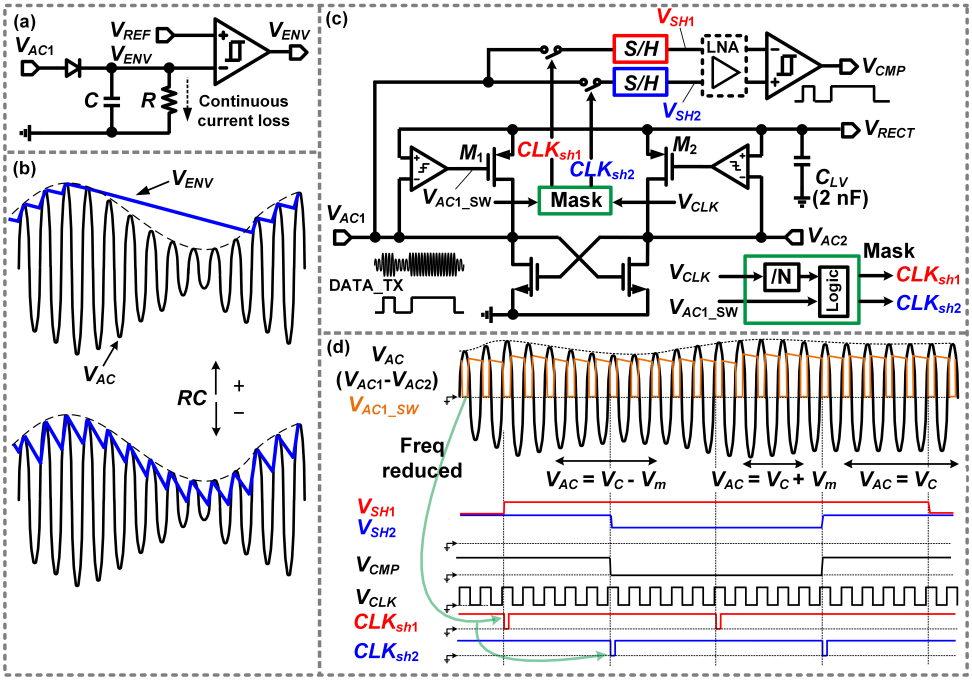


Figure 3.33: (a) The circuit implementation of conventional ASK demodulators, (b) Conceptual waveform of demodulated envelope signal in conventional structures, (c) The circuit implementation of proposed sampling-based ASK demodulator suitable for the low voltage applications, and (d) Conceptual waveform of the demodulated envelope signal in the proposed structure.

include dependency on threshold-sensitive detectors (e.g., Schmitt triggers or buffers) [30,36,37], reliance on area-consuming high-speed comparators [63], or the use of complex high-gain stages [31], which have been briefly explained in Fig. 3.9 in Section 3.2.

To address the limitations in conventional ASK demodulator structure, and to meet the significant challenges (low modulation index, short pulse duration time) in the adopted ASK-PPM modulation scheme, a simple ASK demodulation scheme (Fig. 3.33 (c)) targeting low-voltage applications (i.e., $V_{DD} = 1\ V$) is proposed (though not implemented in the chip presented in this chapter). The proposed structure is fully compatible with the full-bridge active rectifier circuit that will be introduced in Chapter 4. The active rectifier employs actively controlled MOSFET switches to replace conventional half-wave rectification diodes, thereby reducing the forward voltage drop associated with passive diodes. The switch control

signal, V_{AC1_SW}, of the power transistor M_1 is generated by a common-gate comparator [17]. V_{AC1_SW}, along with a 40.68 MHz clock recovered by a latch comparator from the carrier signal, is sent to a mask circuit to generate two sampling signals, $CLK_{SH1,2}$, each with a short duration. These sampling signals control the turn-on/off states of the sampling and hold switches to track the envelope variations of the V_{AC1} signal. A low-noise amplifier stage may be required to ensure an adequate signal-to-noise ratio (SNR) for the subsequent comparison stage.

Since V_{AC1_SW} exhibits a falling edge near the peak amplitude of the V_{AC1} signal in each comparison cycle at a frequency of 40.68 MHz, it can be utilized to generate sampling and hold signals for tracking the envelope of V_{AC1}. To capture distinct envelope variations between the highest and lowest levels, the sampling frequency must be reduced. This can be achieved by using a masking circuit consisting of a '/N' frequency divider and digital logic, similar to the implementation shown in Fig. 4.10 (c) in Chapter 4. The frequency division ratio must be carefully determined to accommodate the short pulses (pulse duration $\Delta T_{pulse} = 210$ ns, which is significantly narrower than conventional ASK modulation schemes) used in ASK-PPM data communication. The pulse duration of the masking circuit can be set to half of ΔT_{pulse}, allowing the generation of two pulses ($CLK_{SH1,2}$) with a time interval of approximately 105 ns, which serve as sample-and-hold (S/H) signals. The sampled voltages of V_{AC1} at different times ($CLK_{SH1,2}$) are then sent to a hysteresis comparator to assess their voltage difference. If the voltage difference between the high sample (V_{AC1} sampled at CLK_{SH1}) and the low sample (V_{AC1} sampled at CLK_{SH2}) due to ASK modulation is sufficiently large, the comparator output undergoes a voltage transition.

As V_{AC1} recovers to its high state after ΔT_{pulse}, the comparator subsequently compares the newly sampled low voltage (V_{AC1} at CLK_{SH1}) and high voltage (V_{AC1} at CLK_{SH2}), triggering another voltage transition. Consequently, the detected PPM signals at the comparator output—caused by the amplitude variations of V_{AC1}—are sent to digital logic for further processing. The conceptual waveform is illustrated in Fig. 3.33(d), while the simulation waveform (TT corner) is depicted in Fig. 3.34.

The proposed structure offers several advantages: (i) The design avoids the use of passive components typically used in RC-based ASK modulators. (ii) Due to the sampling process and hysteresis-based comparison, the SNR is improved. Therefore, the ASK demodulator can still successfully recover data even under low modulation index conditions. (iii) Zero static current is realized, enhancing overall power efficiency. Although the main power consumption in this circuit is attributed to the hysteresis comparator, it remains as low as 20 μW at a modulation index of 0.015 in the TT corner.

Fig. 3.35 illustrates the achievable modulation index under various process and voltage (PV) corners. Notably, a low modulation index of 0.016

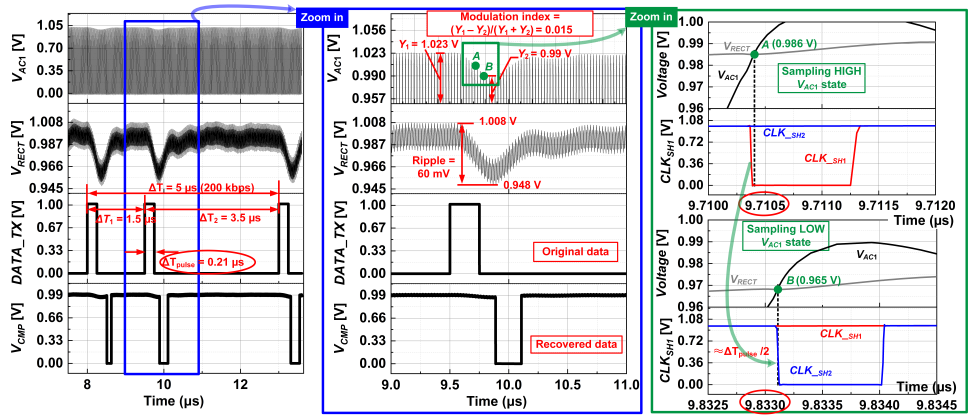


Figure 3.34: Transient simulation waveforms of the proposed sampling-based method.

in the TT corner demonstrates the efficacy of the proposed method.

Proposed

V_{AC1} Amp. (V) \ Corner	TT	SS	FF	FS	SF
0.97 – 1.011 (MI = 0.021)		PASS			
0.975 – 1.011 (MI = 0.018)					
0.981 – 1.011 (MI = 0.015)			FAIL		
0.986 – 1.011 (MI = 0.012)					

Figure 3.35: Shmoo plot for various modulation index checks under different corners using the proposed sampling-based method.

3.6 Conclusion

This work focuses on the development of an implantable chip that is clinically viable, fully wireless, and capable of bi-directional communication with external devices. A proof-of-concept chip for the wireless power and data system has been fabricated using a CMOS BCD 0.18-µm process. The full-custom chip occupies an area of 1.15-mm^2. Compared to other state-of-the-art designs, this work features a high-speed data uplink with a capability of 20 Mbps for closed-loop data communication. For power transfer, a high-frequency carrier signal at 40.68 MHz in the ISM

band is chosen to minimize the area consumed by passive components. Additionally, this work employs a 200 kbps ASK-PPM downlink modulation scheme, which provides a self-synchronized clock and data stream, addressing the synchronization issues inherent in conventional methods. Furthermore, several overshoot/undershoot reduction techniques are proposed to improve the load transient response of the capacitor-less voltage regulator. Experimental results validate that the prototype chip design can successfully generate different voltage outputs and perform bi-directional data communication.

Appendix

For the derivation of Eq. (3.7), we assume that V_{AC} is a single-tone amplitude modulated (AM) signal expressed as Eq. (3.8):

$$V_{AC}(t) = A[1 + \mu cos(\omega_m t)]cos(\omega_c t) \tag{3.8}$$

where A represents the amplitude, μ is the modulation index. ω_m and ω_c are the angular frequency of the modulating and carrier signals, respectively.

The interval between two successive carrier peaks is given by Eq. (3.9):

$$\frac{1}{f_c} = \frac{2\pi}{\omega_c}, \quad \text{and} \quad RC \gg \frac{1}{\omega_c} \tag{3.9}$$

This implies that the time constant RC is significantly larger than the interval between two successive carrier peaks. As a result, the envelope voltage $V_{ENV}(t)$ can be approximated (by means of a first-order Taylor approximation) as Eq. (3.10):

$$V_{ENV}(t) \approx E_0(1 - \frac{t}{RC}) \tag{3.10}$$

where $E_0 = A[(1 + \mu cos(\omega_m t_0)]$ is the capacitor voltage at time t_0 following each charging cycle. To ensure that V_{ENV} closely tracks the AM envelope of $V_{AC}(t)$, it is required that for any t_0:

$$E_0\left(1 - \frac{1}{RCf_c}\right) \leq A\left\{1 + \mu\cos\left[\omega_m\left(t_0 + \frac{1}{f_c}\right)\right]\right\}. \tag{3.11}$$

Assuming $\omega_m \ll \omega_c$, the right-side equation can be expanded as follows (with 'A' omitted):

$$\begin{aligned} 1 + \mu\cos\left[\omega_m\left(t_0 + \frac{1}{f_c}\right)\right] &= 1 + \mu\cos\left(\omega_m t_0 + \frac{\omega_m}{f_c}\right) \\ &\approx 1 + \mu\cos(\omega_m t_0) - \mu\sin(\omega_m t_0)\sin\frac{(\omega_m t_0)}{f_c} \end{aligned} \tag{3.12}$$

Substituting Eq. (3.12) into Eq. (3.11) results in:

$$[1+\mu\cos(\omega_m t_0)]\left(1-\frac{1}{RCf_c}\right)\geq\mu\omega_m t_0\frac{\sin(\omega_m t_0)}{f_c} \tag{3.13}$$

From Eq. (3.13), the following inequality can be derived :

$$\mu\left[\omega_m\sin(\omega_m t_0)-\frac{1}{RC}\cos(\omega_m t_0)\right]\leq\frac{1}{RC} \tag{3.14}$$

Using the trigonometric combination formula, Eq. (3.14) can be rewritten as:

$$\mu\sqrt{\omega_m^2+\left(\frac{1}{RC}\right)^2}\sin(\omega_m t_0+\tan^{-1}\frac{1}{\omega_m RC})\leq\frac{1}{RC}. \tag{3.15}$$

Since this inequality must hold for all t_0, we obtain the following conditions:

$$\mu\sqrt{\omega_m^2+(\frac{1}{RC})^2}\leq\frac{1}{RC} \tag{3.16}$$

$$RC\leq\frac{1}{\omega_m}\frac{\sqrt{1-\mu^2}}{\mu} \tag{3.17}$$

This establishes the necessary condition for μ to ensure that $V_{ENV}(t)$ follows the envelope of the AM signal $V_{AC}(t)$.

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Chapter 4

A 40.68-MHz Fully-Integrated Voltage/Current-Mode Dual-Output PMU for Wireless Neural Implants[1]

4.1 Introduction

In the previous Chapter 3, a highly integrated data communication system was proposed to address the increasing demand for efficient data exchange in modern neural implant systems. A critical component in such systems is the power management unit, which is responsible for delivering the necessary power to the load circuit by wirelessly receiving power. Enhancing the power transfer efficiency in a compact implant system is a key specification. However, the data communication chip design discussed in Chapter 3 faces a significant limitation in terms of power conversion efficiency. This limitation primarily arises from the use of conventional passive rectifier and regulator circuits, which impose substantial losses during the power conversion process. This chapter aims to explore advanced power management circuit design techniques to overcome the bottlenecks associated with conventional methods.

Modern neuromodulation implants record neural signals for decoding brain activities and stimulate neurons for targeted and personalized treatments in a closed-loop fashion [1–7] - see Fig. 4.1. Three key blocks - recording, stimulation, and data telemetry/processing - are typically needed in such systems, each with

[1]This chapter is based on the journal paper: Yi-han Ou-yang, Ronald Wijermars, Pyungwoo Yeon, Tianqi Lu, Amin Arbabian, Wouter A. Serdijn, Sijun Du, Dante G. Muratore, "A 40.68-MHz Fully-Integrated Voltage/Current-Mode Dual-Output PMU for Wireless Neural Implants," in *IEEE Transactions on Biomedical Circuits and Systems (Early Access)*

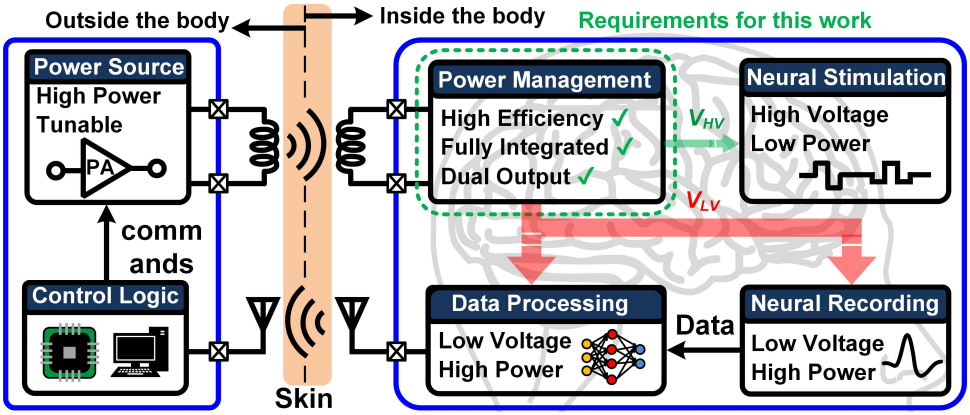


Figure 4.1: The general structure of a wireless closed-loop neuromodulation implant.

different voltage/power requirements. As a result, such applications often require a power management unit (PMU) that can provide various output voltages—including a high-voltage supply (V_{HV}) and a low-voltage supply (V_{LV})—from a single AC input while maintaining high power efficiency. V_{HV} drives the stimulation circuit to allow sufficient voltage headroom, while V_{LV} powers the recording, processing, and control circuits. In conventional neural implant systems, V_{HV} experiences the highest load as stimulation is delivered continuously in an open-loop fashion [5, 8–11]. Recent advances in on-chip neural signal processing, driven by the need to overcome data transmission bottlenecks, have enabled real-time closed-loop neural stimulation, drastically reducing the charge delivered to the tissue [12–16]. Furthermore, advances in electrode design, stimulation parameters optimization, and implantation techniques [17–19] reduced the required stimulation intensity to elicit a neural response. These improvements lead to a reduced load on V_{HV}, with power levels reported in the microwatt range in [20, 21]. Instead, the need for continuous multi-channel recording and on-chip signal processing to monitor brain activity results in a larger load on V_{LV} [20, 22–25]. This marks a new trend in neuromodulation implants, where the PMU is required to provide both a high-power supply (V_{LV}) and a low-power supply (V_{HV}). Furthermore, because V_{LV} is used in precision circuits such as analog front ends, it has stricter voltage ripple requirements than V_{HV}. Finally, since stimulation is not performed continuously, V_{HV} does not need to be constantly regulated. Future wireless power transfer (WPT) systems for closed-loop neuromodulation should con-

sider these requirements to exploit power and area efficiency.

Modern PMU structures have gradually evolved from cascaded power conversion stages [26–32] and multi-tapped rectifiers [11, 33] to more compact and advanced topologies. In recent years, several dual-output voltage-mode (VM) rectifiers based on a single resonant *LC* tank have been proposed, operating in either half-wave or full-wave rectification modes [22, 34–42] (Fig. 4.2(a)). Dual-output regulation is achieved through time-interleaved switching of multiple power transistors connected to different loads. However, since the charging current for each output is identical, these structures are only efficient when the load currents at both outputs are comparable and when V_{HV} draws the majority of power. In emerging neuromodulation implants, where V_{LV} dominates overall power consumption, significant regulation losses appear at V_{HV}. For example, the tested power conversion efficiency (PCE) in [35] reduces by 8% when V_{LV} dominates the power consumption and further decreases by 19% due to voltage regulation. In addition, the output voltage ratio of the VM rectifier is strongly dependent on the corresponding loads [35] and the switch controller accuracy [36, 42]. Particularly, [22] achieves an output voltage ratio of seven by employing series and parallel resonant configurations for each output; however, its efficiency is relatively lower compared to other works due to strict load requirements and passive rectification.

Current-mode rectifiers (CM) [23, 44–47], or resonant current-mode rectifiers (RCM) [43, 48–52], are boost converter structures that can generate high voltage level outputs from an AC input signal resonating at a low amplitude, based on the principles of charge accumulation and charge transfer. These structures typically achieve a voltage gain exceeding two ($V_{HV}/|V_{AC1}| > 2$), as shown in Fig. 4.2(b), offering a promising solution to the efficiency bottlenecks of dual-output VM designs. However, dual-output generation using a CM charging scheme inherently introduces significant voltage ripple on both outputs, as it requires multiple resonant cycles before each subsequent charge transfer can commence. To address this issue, bulky off-chip filtering capacitors are required [23, 43–52], which restricts implant miniaturization. Furthermore, the breakup switch SW_1, which plays an essential role in the *LC* tank loop, degrades the power transfer efficiency (PTE) of the link and complicates the startup procedure, as the switch control requires V_{LV} or V_{HV} before it becomes available. As a result, all prior works implementing CM operation achieve only half-wave rectification and suffer from power switch stress due to the negative swing of V_{AC}. This issue can be addressed by using thick-oxide devices, albeit at the cost of reduced PCE. In particular, [52]

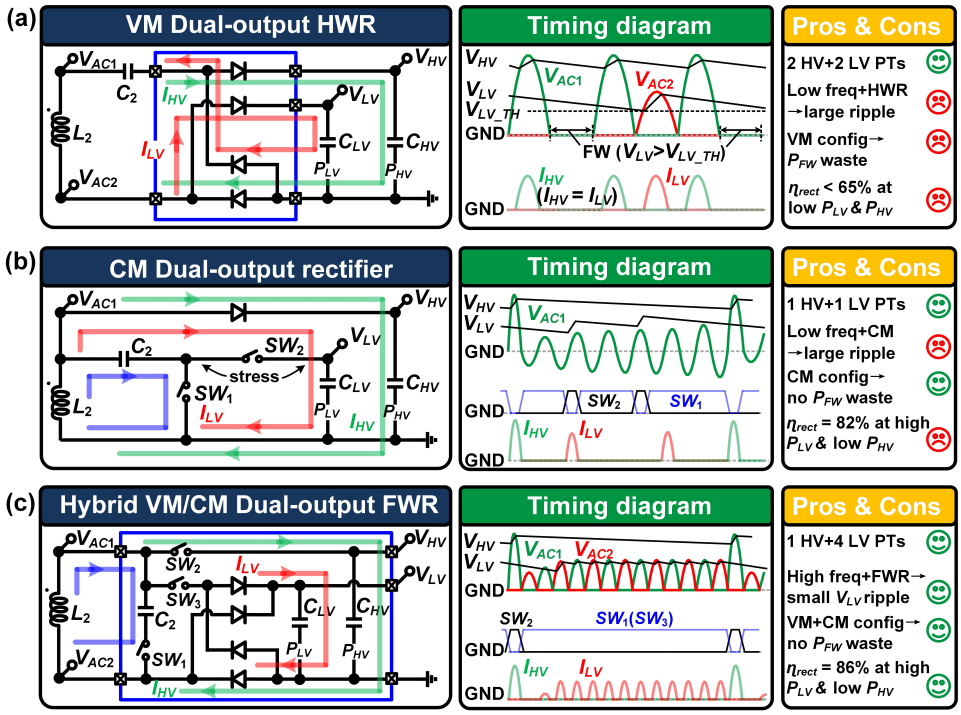


Figure 4.2: Existing and proposed PMU topologies for dual-output applications with highlighted current flow paths: (a) Dual-output Half-Wave Rectifier (HWR) with VM charging [35], (b) Dual-output rectifier with CM charging [43], and (c) Proposed Full-Wave Rectifier (FWR) with dual VM/CM charging.

introduced a voltage doubler structure capable of full-wave rectification with zero negative swing, similar to its VM counterpart structure [40, 41]; however, it requires two identical off-chip capacitors (2 µF each), and fixes the output voltage ratio at two, restricting its applications.

To address the aforementioned new challenges in WPT for neuromodulation implants, this paper introduces a fully on-chip, single-input dual-output (SIDO) PMU with dual-mode powering (Fig. 4.2(c)). By incorporating two distinct operation modes, the proposed SIDO PMU can provide two supplies without compromising efficiency or voltage ripple: a low-level, low-ripple voltage (V_{LV}) with high output power, and a high-level high-ripple voltage (V_{HV}) with low output power. Unlike prior monolithic-mode designs, this work eliminates bulky passive components, achieving high power and area efficiency, low output ripple, and fully inde-

pendent startup. To the best of the author's knowledge, this is the first work that fully exploits the advantages of a dual-mode charging strategy to realize all these features within a miniaturized implant system. As an intended application, a next-generation retinal prosthesis [53] has been investigated, as it demands two distinct voltage levels with load-driving capabilities ranging from the microwatt to milliwatt scale. The organization of this paper is as follows: Section 4.2 discusses the operation principle of the dual-mode PMU. Section 4.3 describes the detailed circuit implementation of the main components. Section 4.4 presents the measurement results of the fabricated chip and a comparison with the state-of-the-art. Finally, conclusions are drawn in Section 4.5.

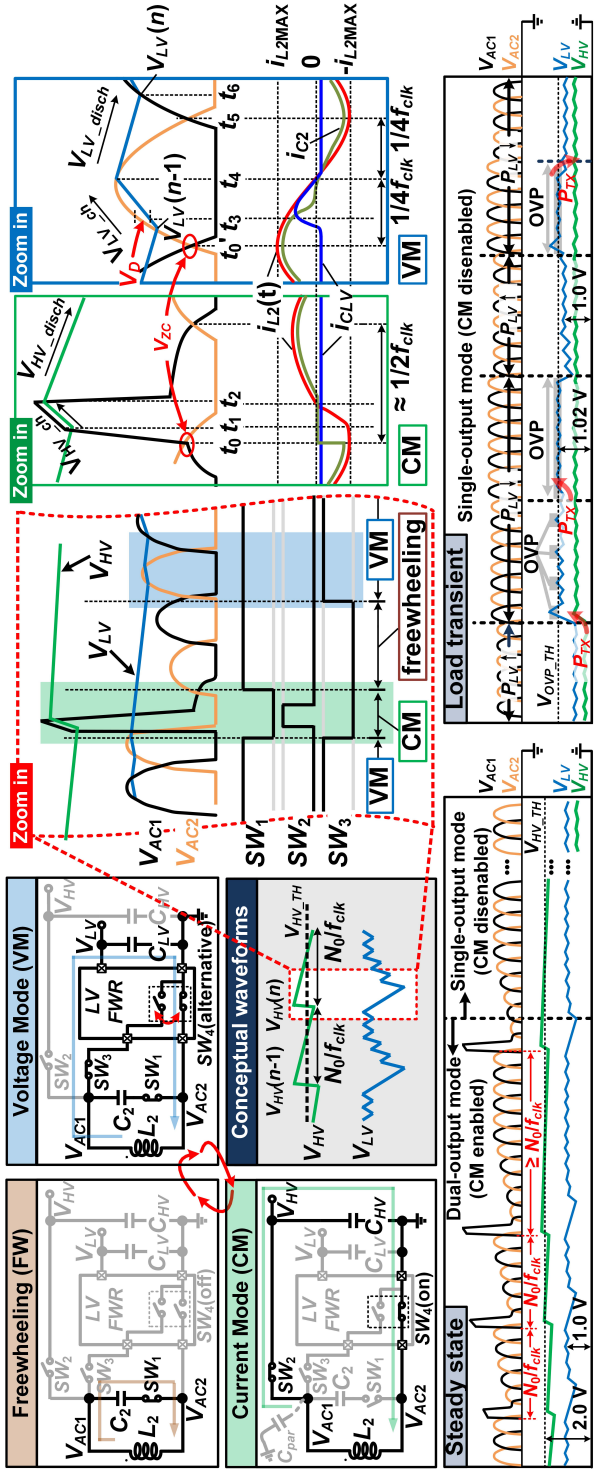


Figure 4.3: Mode configurations and their conceptual transient waveforms.

4.2 Operating Principle

The wireless link operates at 40.68 MHz to reduce the size of the on-chip resonance and filter capacitors, and to increase the Q-factor of the coils for better PTE. The receiver resonates at a low AC voltage ($V_{AC} \simeq V_{LV}$) to maximize power delivery in VM for V_{LV}; while the CM rectifier can boost the AC voltage to generate V_{HV} when needed. Both VM and CM phases are realized using active switch control for higher PCE.

The proposed dual-mode PMU for dual-output WPT systems operates in three phases controlled by a mode-switching algorithm: the freewheeling phase, the VM charging phase, and the CM charging phase. The circuit configuration and their conceptual waveforms are shown on the left and right sides of Fig. 4.3, respectively. The following sections explain the operation of each phase and the mode-switching algorithm.

4.2.1 Freewheeling phase

The freewheeling (FW) phase builds up the resonance in the parallel-connected LC tank and accumulates energy within the loop (Fig. 4.3, the mode labeled 'FW'). During this phase, the switch SW_1 is closed while switches SW_2, SW_3 and SW_4 are open. Energy starts to accumulate within the LC resonator and V_{AC} gradually increases. The FW phase is activated at startup and after the CM charging phase to ensure that VM charging is performed only when $V_{AC} > V_{LV}$. This condition may not always be satisfied without the FW phase, as an offset is introduced to V_{LV} for delay compensation. Consequently, the FW phase avoids the potential reverse charging issue. Moreover, the FW phase incurs no power penalty, since the energy accumulated during this phase is fully transferred to the load in the subsequent VM phase.

4.2.2 Current mode charging phase

In the CM phase, the energy stored in the LC resonator is delivered to the V_{HV} load (Fig. 4.3, the mode labeled 'CM'). SW_1 disconnects C_2 and L_2 to break the resonance; meanwhile, SW_3 is open to disconnect the VM rectifier, and SW_2 is closed to allow the L_2 current to flow into the V_{HV} load and output capacitor C_{HV}. SW_4 remains closed, connecting V_{AC2} to the ground and providing the current return path (the green line). When the resonance breakup switch opens, the V_{AC1} node is boosted to a high voltage to charge V_{HV}. Although CM charging mitigates the need for a large AC voltage amplitude, it has a lower PCE than VM charging [44, 45].

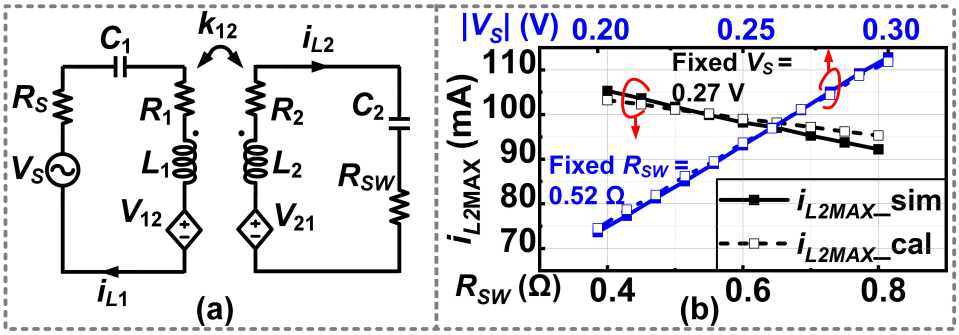


Figure 4.4: (a) The equivalent model of a series-parallel Tx-Rx inductive link, (b) Comparison between the simulated and calculated result of i_{L2MAX} vs. R_{SW} and $|V_S|$.

The activation timing of the CM phase should be carefully chosen to maximize energy transfer to the V_{HV} load, thus a sufficiently high V_{HV} can be achieved. Consider an inductive coil link as in Fig. 4.4(a), where V_S is a voltage source that can be modeled as $|V_S|\cos(wt)$ at the Tx side, V_{12} and V_{21} are the induced voltage at the transmitter (Tx) and the receiver (Rx) sides, respectively, ω is the angular frequency, k_{12} is the coupling coefficient between L_1 and L_2, and M_{12} is the mutual inductance, given by $M_{12} = k_{12}\sqrt{L_1 L_2}$. R_{SW} represents the breakup switch resistance, while R_1 and R_2 are the equivalent series resistances of L_1 and L_2, respectively. The energy $E(t)$ stored in the L_2C_2 tank can be derived as:

$$E(t) = \frac{1}{2}L_2 I_{L2}^2(t) + \frac{1}{2}C_2 V_{C2}^2(t) \tag{4.1}$$

where I_{L2} is the current flowing through L_2 and V_{C2} is the voltage across C_2. According to Eq. (4.1), the maximum current I_{L2} in the receiver coil can be found when $V_{C2} = V_{AC2} - V_{AC1}$ is zero. Breaking the resonance loop at this point yields the maximum ΔV_{HV}.

It is important to quantify the voltage change ΔV_{HV} in each CM charging step. According to Kirchhoff's Voltage Law:

$$V_{21}(t) = L_2\frac{di_{L2(t)}}{dt} + \frac{1}{C_2}\int_0^t i_{L2}(t)dt + (R_2 + R_{SW})i_{L2}(t) \tag{4.2}$$

where $V_{21}(t)$ can be expressed as $|V_{21}|\sin(wt)$. In steady state,

V_{21} in the receiver side can be derived as [49]:

$$|V_{21}| = \left| \frac{j\omega V_S M_{12}}{R_1 + \frac{\omega^2 M_{12}^2}{R_2 + R_{SW}}} \right| = \frac{\omega |V_S| M_{12}}{R_1 + \frac{\omega^2 M_{12}^2}{R_2 + R_{SW}}} \tag{4.3}$$

Given the initial conditions $i_{L2}(0) = 0$ and $\frac{di_{L2}(t)}{dt}\Big|_{t=0} = 0$ at startup, the solution of Eq. (4.2) leads to the complete form of $i_{L2}(t)$ and its maximum value $i_{L2\text{MAX}}$ in steady state, as shown in Eq. (4.4) and Eq. (4.5), respectively:

$$i_{L2}(t) = \frac{|V_{21}|}{R_2 + R_{\text{SW}}} \sin(\omega t) - e^{-\alpha t} \frac{\omega |V_{21}|}{\omega_d (R_2 + R_{SW})} \sin(\omega_d t) \tag{4.4}$$

$$i_{L2\text{MAX}} = \frac{|V_{21}|}{R_2 + R_{\text{SW}}} = \frac{\omega |V_s| M_{12}}{R_1 (R_2 + R_{\text{SW}}) + \omega^2 M_{12}^2} \tag{4.5}$$

where $\alpha = \frac{R_2 + R_{\text{SW}}}{2L_2}$ represents the neper frequency and $\omega_d = 1/\sqrt{L_2 C_{\text{par}}}$ is the undamped natural angular frequency. Fig. 4.4(b) compares the simulated and calculated results of $i_{L2\text{MAX}}$, demonstrating a close agreement between them. Increasing the transmitter side voltage or reducing the breakup switch resistance can lead to a higher $i_{L2\text{MAX}}$.

The derived expressions for $i_{L2}(t)$ and $i_{L2\text{MAX}}$ can be further used to estimate the achievable V_{HV} after n cycles of CM operation. In the Appendix, we present the analytical derivation of the charging and discharging voltages, $V_{HV,\text{ch}}(n)$ and $V_{HV,\text{disch}}(n)$, respectively, as functions of $i_{L2}(t)$, R_{HV}, and C_{HV}. Based on these expressions, the cumulative result of $V_{HV}(n)$ can be calculated accordingly:

$$V_{HV}(n) = \sum_{i=0}^{n} \left(V_{HV_ch}(i) - V_{HV_disch}(i) \right) \tag{4.6}$$

4.2.3 Voltage mode charging phase

The VM phase starts once the resonating AC voltage amplitude reaches the desired voltage level of V_{LV}. Fig. 4.3 (the mode labeled 'VM') illustrates the simplified configuration for VM operation with full-wave rectification. Only the positive V_{AC1} cycle is shown for simplicity. During this phase, the switch SW_1 is closed to enable energy accumulation in the LC resonator (similar to the FW phase). The switch SW_2 is open to disable the CM rectifier. The switch SW_3 closes to conduct current into the FWR. SW_4 represents the cross-coupled NMOS transistor within the FWR that grounds V_{AC2} and provides the current return path (the blue line).

The VM charging phase performs high-efficiency charging from the LC resonator to the V_{LV} load and output capacitor C_{LV}. It performs full-wave voltage rectification to reduce the output ripple approximately by half compared to conventional half-wave rectification used in dual output rectifiers [43, 44].

Similar to Eq. (4.6), the achievable V_{LV} after n switching cycles in the VM can be recursively calculated based on the voltage expressions derived in the Appendix:

$$V_{LV}(n) = \sum_{i=0}^{n} \left(V_{LV_ch}(i) - V_{LV_disch}(i) \right) \tag{4.7}$$

Eq. (4.6) and Eq. (4.7) can be used to determine the optimal time interval for the transition between the VM and CM phases, as further discussed in the following section.

The regulation mechanism for V_{LV} is depicted in Fig. 4.3 (labeled 'load transient'). Unlike V_{HV}, which employs a self-adaptive charging scheme, V_{LV} is regulated by an over-voltage protection (OVP) circuit with a trigger voltage near 1.0 V. Under light load, excess power is dissipated by the OVP, while under heavy load, the DC voltage level is maintained, ensuring robust operation across dynamic load conditions.

4.2.4 Mode-switching algorithm

Fig. 4.5 illustrates the mode-switching algorithm implemented by the control logic on chip. The algorithm starts from the FW mode to build up the AC signal swing and store energy within the LC resonator. Once the amplitude of the AC signal reaches the target level of V_{LV}, the system transitions to VM. To enable dual-output rectification, the transition from VM to CM is required. Three conditions must be satisfied for the system to switch from VM to CM: (i) the CM control flag CM_EN is active. If CM_EN=0, the system works as a single output rectifier to generate only V_{LV}, (ii) V_{HV} is below the regulation threshold V_{HV_TH}, and (iii) there have been sufficient cycles (N_0) since the last CM charging operation, ensuring adequate time for the AC signal swing to rebuild and preventing consecutive CM charging operations that could disrupt V_{LV} regulation.

If all three conditions are satisfied, the system performs CM charging for one cycle before switching to FW mode to build up the resonance again. Notably, an optimal N_0 exists that is constrained by both a lower and an upper limit.

The lower limit for N_0 is decided by the acceptable PCE degradation in VM for the high-load output V_{LV} - see Fig. 4.6(a). If N_0 is too

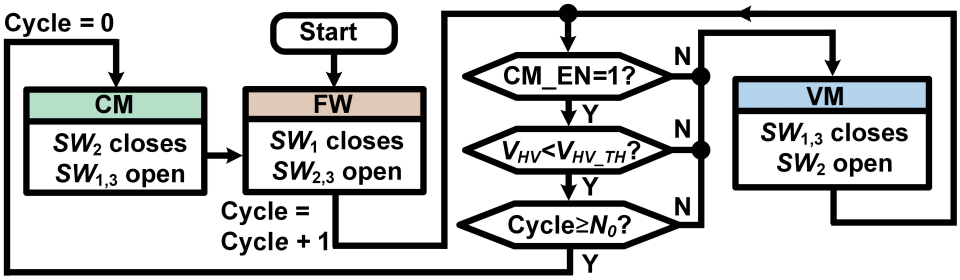


Figure 4.5: The flowchart of the mode-switching algorithm.

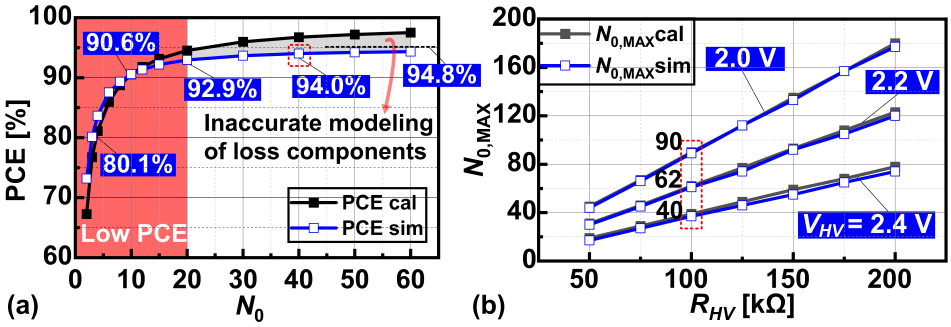


Figure 4.6: The comparison between the calculation and behavioral simulation results of (a) PCE versus N_0, and (b) $N_{0,\mathrm{MAX}}$ versus R_{HV} with achievable V_{HV} from 2.0 V to 2.4 V.

small, then the system does not spend sufficient time in VM charging the high output load V_{LV}. To evaluate the power degradation of the proposed dual-mode charging scheme under different N_0, the corresponding PCE is formulated in Eq. (4.8):

$$\mathrm{PCE} = \frac{P_{LV}}{P_{LV} + P_{Loss,total}} \tag{4.8}$$

$$P_{LV} = \left[\frac{1}{n+1}\sum_{m=0}^{n=\infty}\left(V_{LV}(0) + \sum_{i=1}^{m}\Delta V_{LV}(i)\right)\right]^2 / R_{LV} \tag{4.9}$$

where P_{LV} is the output power, $\Delta V_{LV}(i)$ is the voltage accumulation on V_{LV} at step i based on Eq. (4.7), and $P_{Loss,total}$ is the power loss as derived in [54]. Notably, ensuring $N_0 > 20$ limits the PCE degradation to less than 2.0%.

The upper limit for N_0 is decided by the desired output voltage V_{HV} for a given load R_{HV}. When N_0 is too large, the CM charg-

ing (V_{HV_ch}) may not fully compensate for the discharging in between CM cycles (V_{HV_disch}). For a given output level and load, there exists a maximum $N_{0,max}$ that can sustain proper CM operation - see Fig. 4.6(b)). For our target specifications ($V_{HV} = 2$ V and $R_{HV} = 100$ kΩ), the calculated theoretical $N_{0,\mathrm{MAX}} = 90$. However, considering the potential losses due to imperfect switching timing and power leakage, selecting $N_0 = 40$ provides a sufficient margin.

Considering both lower and upper limits, this work uses $N_0 = 40$. Notably, this number significantly exceeds those previously reported in CM-based schemes [43, 50], mainly because the majority of power is delivered to the V_{LV} output in the high-efficiency VM charging phase. The conceptual waveform showing the mode switching and V_{HV} regulation is depicted in Fig. 4.3 (labeled 'steady state'). The CM rectification starts at the zero-crossing point. A high voltage is induced on V_{AC1}, and current flows into the V_{HV} load capacitor C_{HV}. During the CM rectification and the subsequent FW mode, V_{LV} is not being charged, which leads to a larger ripple and reduced power efficiency in VM. However, the system operates in the high-efficiency VM to drive the heavy load on V_{LV} most of the time. Hence, the overall efficiency in VM is not affected significantly. For example, with V_{HV} connected to a 225kΩ load, the end-to-end efficiency in VM charging only drops by 2.38% in this work (detailed in Section 4.4).

4.3 Hardware Implementation

Fig. 4.7 illustrates the proposed VM/CM PMU system architecture that regulates a 40.68 MHz inductive wireless link to generate dual outputs. The chip simultaneously achieves rectification, regulation, bias generation, and overvoltage protection using only the Rx coil as an external component. The 240 pF resonance capacitor C_2 (consisting of 80 pF C_{2a}, 80 pF C_{2b}, and 80 pF parasitic capacitance seen from node connections), the 250 pF filtering capacitor C_{HV} and the 2 nF V_{LV} filtering capacitor C_{LV} are integrated on-chip. C_{LV} and C_{HV} use a stacked structure with a metal-on-metal (MOM) capacitor on top of a thick-oxide low-leakage varactor (2.5 V voltage rating) to achieve high capacitance density and low power leakage, while C_2 uses a MOM capacitor to ensure minimal variation and low resistance. The PMU comprises three main blocks: the VM rectifier, the resonance breakup switch, and the CM rectifier with the control logic.

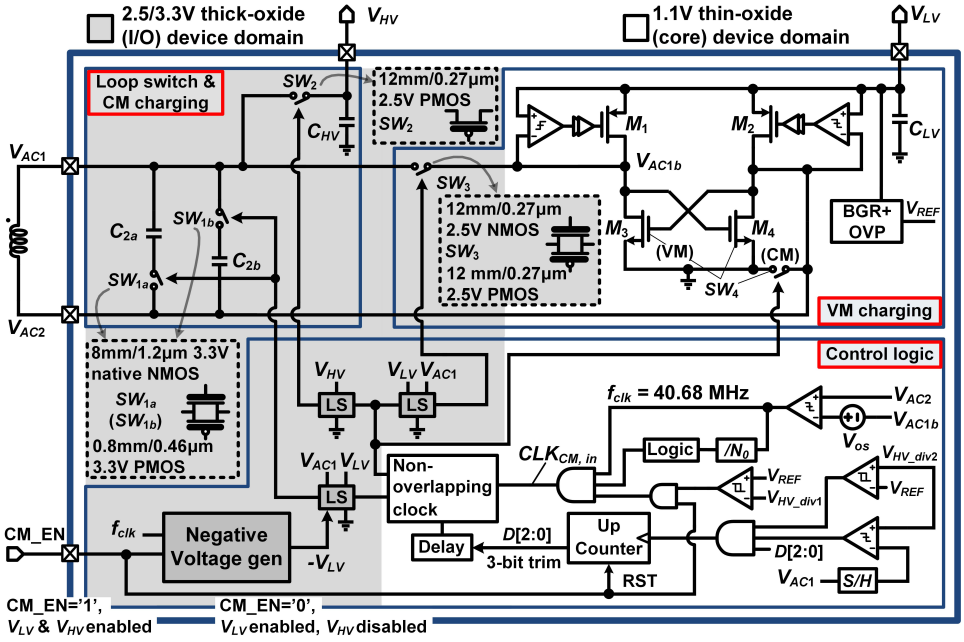


Figure 4.7: The overall structure of the proposed design.

4.3.1 VM rectifier

The VM rectifier uses active PMOS diodes ($M_{1,2}$) with a cross-coupled NMOS pair structure ($M_{3,4}$). The active diodes are controlled by a common-gate comparator and a gate driver, both optimally sized to minimize switching losses. The rectifier uses thin-oxide devices to minimize power losses.

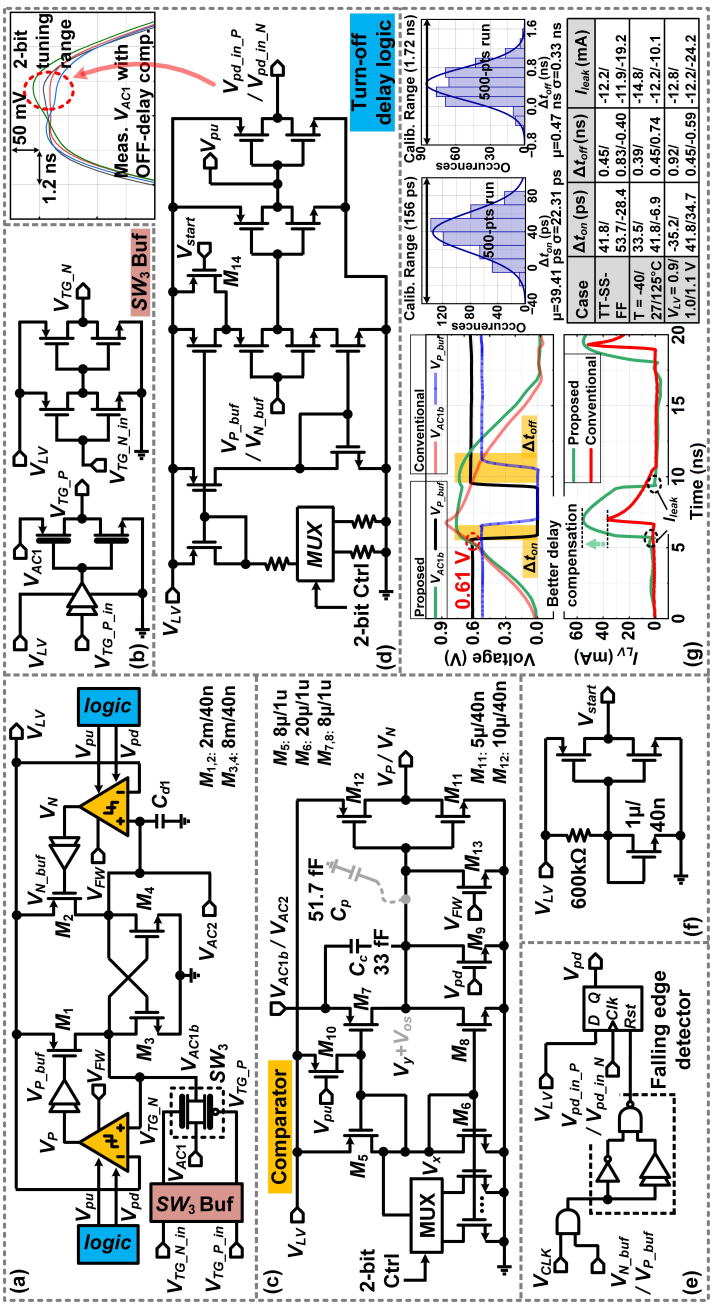


Figure 4.8: The circuit implementation of (a) active voltage rectifier, (b) driving circuits for the high-voltage protection switch, (c) common gate comparator, (d) pulse duration time control circuit, (e) digital logic to prevent multiple-pulsing, (f) startup auxiliary circuit, and (g) the simulated waveform of the turn-on delay compensation using the conventional mismatch-based scheme (M_6 size = 100/1 µm for a fair comparison) and proposed coupling capacitor-based scheme. The robustness of the proposed scheme is verified through a 500-point Monte Carlo simulation and PVT analysis.

High-Voltage Protection Switch: SW_3 (Fig. 4.8(a)) protects the rectifier core devices during CM by turning off before V_{AC1} exceeds 1.25 V (40-nm CMOS limit), and remains ON during VM. To fully turn off SW_3 during CM, the switch buffer (Fig. 4.8(b)) supplies V_{AC1} and ground to the PMOS and NMOS gates, respectively. Conversely, to turn on SW_3 during the VM phase, the switch buffer supplies ground and V_{LV} voltage rails to the transmission gate. V_{HV} is not used as the supply since CM operation is not always enabled. SW_3 is upsized to reduce conduction loss during VM charging (PCE decreases by 1.2% when assuming 0.5Ω resistance), at the cost of notable parasitic capacitance at V_{AC1b}. As a result, the delayed switching of pull-down transistor M_4, increases switching loss due to the negative swing at V_{AC2}. To mitigate this, a dummy capacitor, $C_{d1} = 24$ pF is placed at V_{AC2}. This solution effectively compensates for asymmetrical loading of V_{AC1b} and V_{AC2}, offering area advantages over a dummy switch and has a negligible impact on matching. Simulation results show a 2.27% improvement in rectifier PCE at the R_{LV} load of 200 Ω, without degrading link PTE.

Common Gate Comparator: The common-gate (CG) comparator used in this work (Fig. 4.8(c)) can accommodate a high input common-mode voltage and has a low static power consumption [55]. It operates in the VM comparison when the FW control signal (V_{FW}) is not enabled. To compensate for the turn-on delay, this design uses comparator offset compensation [54, 56]. The offset is introduced through a programmable mismatch in the current mirror M_6 and M_8 to accommodate process variations, and functions well in the steady state when $V_{LV} > V_{th,M5} + V_{th,M6}$ (strong inversion). However, the generated offset is dependent on the working region and varies with V_{LV} during startup, reducing the effective power transferred to the load. Apart from the late turn-on problem, this technique also has a reverse current problem during startup [54, 57]. Although the fixed delay problem can be solved using a voltage-controlled delay cell with a feedback loop design, it cannot properly compensate the turn-on delay during startup [57], which increases startup power and may risk device breakdown [39]. To prevent the AC voltage from exceeding safety limits during startup, an auxiliary coupling voltage V_{os} at V_y is introduced by a coupling capacitor C_c. The capacitive divider between C_c (33 fF) and the total parasitic capacitance C_p (51.7 fF) at the node V_y sets the value of V_{os} as a function of V_{AC}. It can operate at V_{LV} as low as 0.61 V. Consequently, the proposed design accelerates startup by reducing reverse current at low V_{LV} (Fig. 4.8(g)). In this work, the C_c-induced coupling voltage compensates for 0.2 ns delay (typical value), while the input pair pro-

grammable offset (2 bits) compensates for up to 0.25 ns (typical value). Monte Carlo and corner simulations show robustness of this method across PVT variations (Fig. 4.8(g)).

The comparator's turn-off delay leads to reverse current loss. This design uses a current-starved delay cell (Fig. 4.8(d)) to create a delayed signal (V_{pd}) of the turn-on signal (V_{P_buf}) to switch off the power transistor ($M_{1,2}$) in the rectifier at the right time. V_{pd} pulls V_y in the comparator to ground through M_9, while V_{pu} pulls V_x to V_{LV} through M_{10}, causing the comparator to generate a high signal and switch off $M_{1,2}$. The delay time can be manually controlled by a 2-bit resistor array that adjusts the bias current of the delay cell, as verified by the measurement V_{AC1} waveform (shown above Fig. 4.8(d)). To prevent the multiple pulsing issue [58] which increases switching losses, this design uses digital logic as shown in Fig. 4.8(e) to latch the V_{pd} signal until the next comparison cycle starts. To prevent excessive power demand during startup, an auxiliary circuit (Fig. 4.8(f) [59]) is designed to shorten the startup delay by providing additional current to the delay cell through M_{14} (Fig. 4.8(d)). When V_{LV} reaches its stable state, V_{start} transitions from low to high, disabling the current path.

4.3.2 Resonance breakup switch

The resonance breakup switch (SW_1) is an essential part of this design that affects both the CM and VM operation. When SW_1 is OFF during CM operation, it should completely block the conduction path within the LC tank to maximize ΔV_{HV}. When SW_1 is ON during VM operation, it should have a small equivalent resistance to reduce the losses in the link. For example, assuming an on-resistance of 0.5 Ω, SW_1 degrades the PTE by 2.2%.

A transmission-gate structure is used to allow full-wave rectification in VM. A thick-oxide native (normally-on) NMOS device enables self-startup when V_{LV} has not yet reached its stable value. A negative supply voltage $-V_{LV}$ (Section 4.3.4) is used to turn the native NMOS switch OFF during CM. The thick-oxide PMOS switch is driven between ground (ON in VM) and V_{AC1} (OFF in CM), similarly to the one in SW_3.

Fig. 4.9(a) shows the circuit implementation of the resonance breakup switch (SW_1) during VM in conventional structures with an FWR. This structure suffers from a significant increase in ON resistance during the Φ_2 phase, when $V_{AC2} > V_{AC1}$. In the Φ_1 phase, where $V_{AC2} = 0$, R_{eq} is only 0.52 Ω due to a fixed V_{GS} applied to the NMOS switch. However, when $V_{AC2} > 0$, R_{eq} increases due to the reduced gate drive voltage, especially during $V_{AC2} < V_{th,P}$. As a result, rather than charging the intended resonant capacitor C_2

through the high-impedance path, the inductor current is diverted to an unintended low impedance path formed by the parasitic capacitance and the rectifier power transistor (M_3 in Fig. 4.8(a)), which increases switching losses and degrades PCE.

To reduce R_{eq} to an acceptable value based on simulation results, it would require a PMOS switch ∼20 times larger. Instead, this work addresses this problem by splitting the switch-capacitor pair into two anti-parallel structures - Fig. 4.9(b). When V_{AC2} increases, the equivalent resistance ($R_{eq,a}$) of SW_{1a} increases as before, while $R_{eq,b}$ of SW_{1b} remains small. Hence, in this phase, the majority of the current flows through SW_{1b}. Vice versa, when V_{AC1} increases, current flows through SW_{1a}. This way, the overall ON resistance is low over the full cycle, leading to lower power losses in the breakup switch. In addition, the negative voltage swing in V_{AC1} is eliminated, which mitigates the switching losses in the NMOS power transistor pair and further improves the rectifier PCE by 5.7% under the nominal load condition of 200 Ω. The proposed topology avoids the need for complex bias schemes or excessive use of transistors and capacitors [52].

4.3.3 CM rectifier

The CM rectifier in Fig. 4.10(a) uses an active diode (SW_2) with a dynamic body bias to prevent leakage current to the substrate [60]. The active structure minimizes the voltage drop across the diode to maximize efficiency, as shown in Fig. 4.10(b). During CM, the resonance-breakup switches SW_{1a}/SW_{1b} and the protection switch SW_3 are open. The pull-down switch SW_4 connects V_{AC2} to ground to provide current return path. A negative voltage $-V_{LV}$ is applied to the native NMOS transistors in SW_{1a}/SW_{1b}. V_{AC1} directly drives the PMOS transistors in SW_{1a}/SW_{1b} and SW_3, while the NMOS transistor in SW_3 can be grounded.

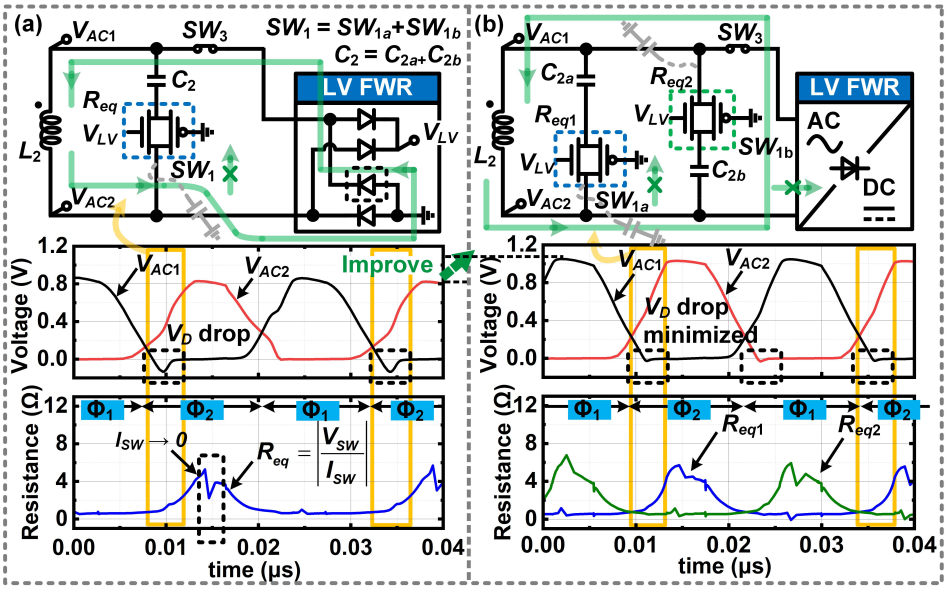


Figure 4.9: The VM configuration of the resonance breakup switch and its equivalent resistance in (a) the conventional half-wave and (b) proposed full-wave scheme. The size of SW_1 in (a) is double that of SW_{1a}/SW_{1b} for a fair comparison.

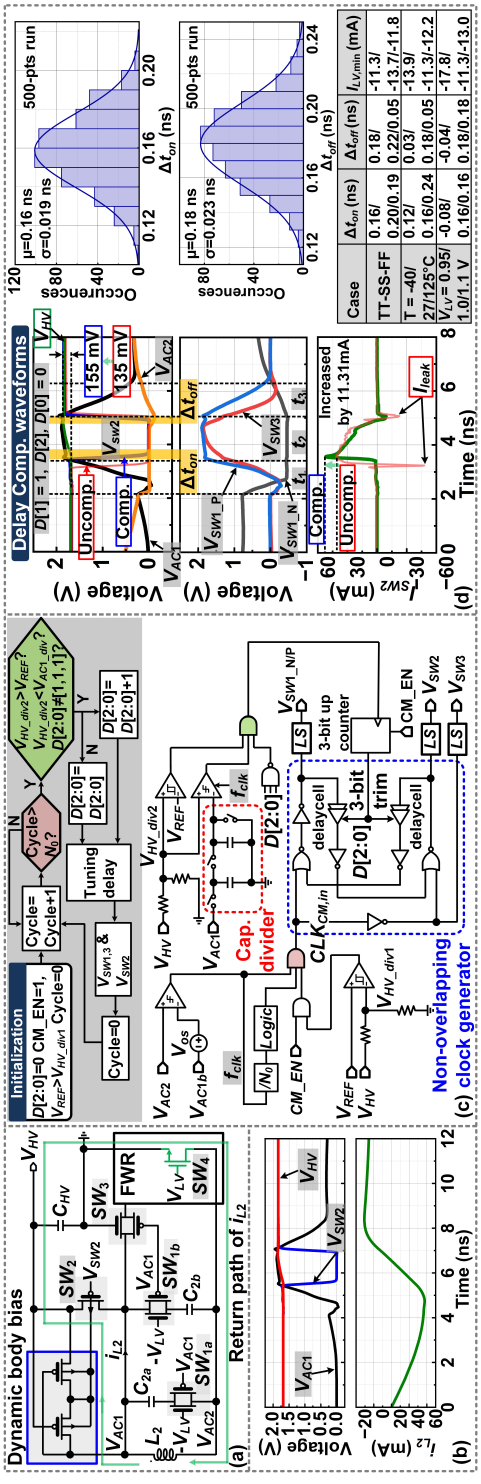


Figure 4.10: (a) The circuit implementation of the CM charging rectifier, (b) Simulated charging waveforms, (c) The operation flowchart and the circuit implementation of the non-overlapping clock generator, and (d) Simulated CM charging waveform with uncompensated/compensated non-overlapping clock signals. The robustness of the proposed scheme is verified through a 500-point Monte Carlo simulation and PVT analysis.

As mentioned above, this work focuses on applications where most of the power is required for V_{LV}, while V_{HV} has a light load. Hence, the resonance breakup switches SW_{1a}/SW_{1b} and the protection switch SW_3 are optimized to reduce conduction losses during VM. The drawback is that they contribute a large parasitic capacitance to the V_{AC1} node. If passive charging with a diode voltage drop ($\sim$ 0.7 V) is adopted [43, 45, 46, 50, 61], most of the current in the inductor is used to charge the parasitic capacitance at node V_{AC1}, and V_{HV} cannot be properly regulated to the expected high voltage. This can be a significant bottleneck, especially in low-power, high-frequency applications, because both the available power and the charging time are insufficient for conducting the CM charging. To overcome this passive mode charging limitation, this work proposes an active charging structure to reduce the voltage drop between V_{AC1} and V_{HV}.

The following requirements have to be satisfied: (i) SW_3 needs to open before the CM phase starts to protect the core devices in the VM rectifier, (ii) SW_1 needs to open when $V_{AC1} = V_{AC2}$ to maximize the current coming from the inductor, and (iii) SW_2 needs to close when $V_{AC1} \geq V_{HV}$ to start charging the output capacitor C_{HV}. Similarly to the VM rectifier, the early switch-ON or the late switch-OFF of SW_2 when $V_{AC1} < V_{HV}$ can introduce a reverse current from V_{HV} to V_{AC1}. Also, the late switch-ON or the early switch-OFF of SW_2 when $V_{AC1} > V_{HV}$ (SW_1 in OFF state) can generate large spikes on V_{AC1} [36] and cause stress problems since there is no low-impedance path for the inductor current.

To address these issues, the CM control logic uses a non-overlapping clock with adaptive delay. The operation principle is illustrated in the flowchart in Fig. 4.10(c). Initially, a comparator recovers the system clock in phase with the zero crossing point (ZCP). This clock is sent to the digital control unit along with the CM_EN signal and the output of the N_0 counter (Section 4.2.4) to generate the enable signal for the CM charging periodically ($CLK_{CM,in}$). The comparator is offset compensated to minimize its delay and maximize the inductor current when the LC tank is opened (details in Section 4.3.4).

First, $CLK_{CM,in}$ derives the overlapping clock signal to open the protection switch SW_3 before SW_1 opens. SW_2 is closed only when SW_1 (and SW_3) are open. The required non-overlapping time demands dynamic adjustment, as it increases proportionally with V_{HV}. This is realized using a programmable delay line controlled by a 3-bit counter. At every CM charging cycle, V_{AC1} is sampled when SW_2 closes and compared with V_{HV}. If $V_{AC1} < V_{HV}$, the non-overlapping time is increased by incrementing the counter output

bits. If $V_{AC1} > V_{HV}$, the counter is not updated. Fig. 4.10(d) shows the delay compensation for the control signal of SW_2. When V_{SW2} turns on before $V_{AC1} > V_{HV}$, the counter continues to increase until the cross-point reaches its optimal timing. Monte Carlo and corner simulations confirm that the proposed CM delay compensation scheme can effectively suppress reverse current under PVT variations (Fig. 4.10(d)).

4.3.4 Auxiliary circuits

Bandgap reference and overvoltage protection

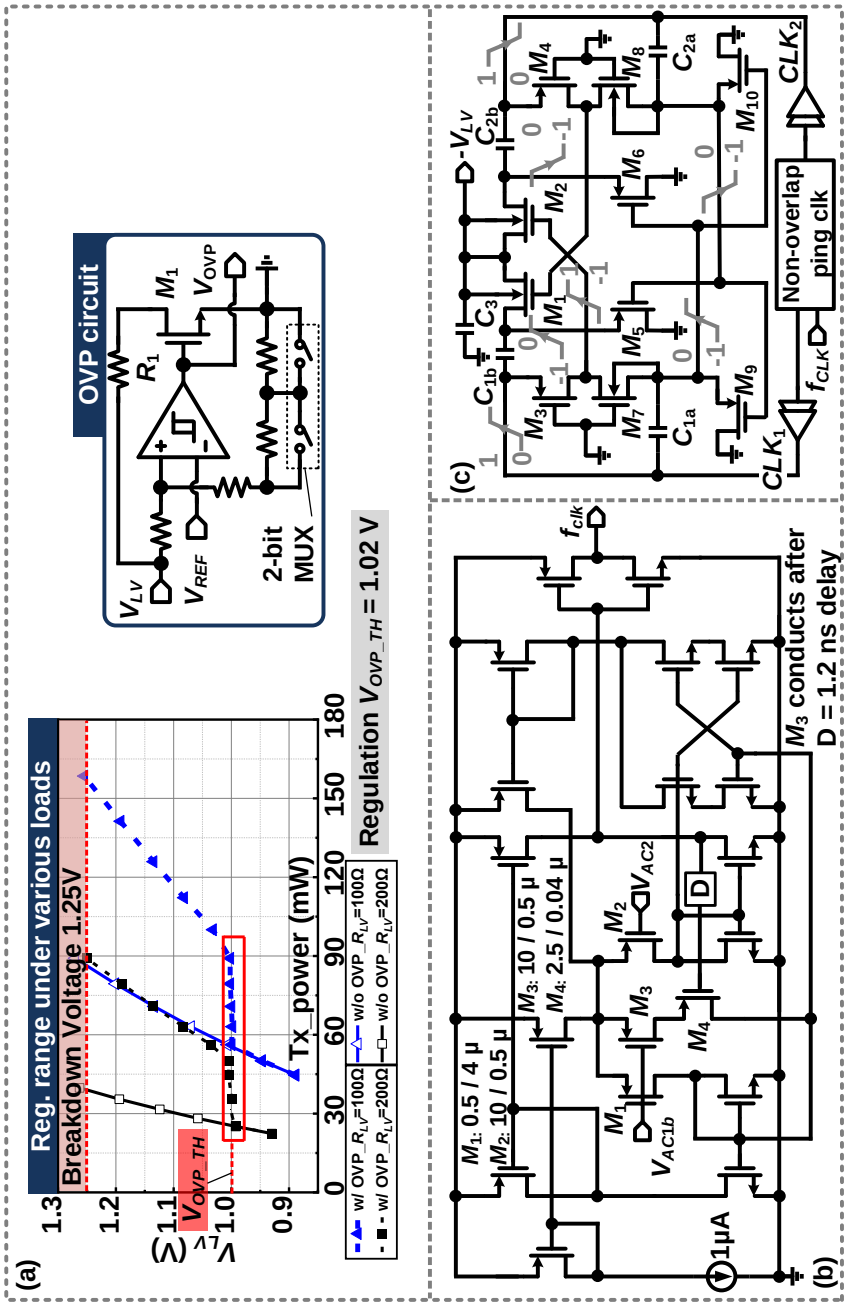


Figure 4.11: (a) The circuit implementation of the OVP and the simulated V_{LV} w/ and w/o OVP versus different Tx powers, (b) Comparator with a mismatched input pair, and (c) Negative voltage generator.

A low-voltage bandgap reference circuit [62] generates the 0.55V reference voltage (V_{REF}) for the control logic and the OVP circuit (Fig. 4.11(a)). The OVP circuit ensures that V_{LV} remains within the safe operating range and also enables voltage regulation. When V_{LV} exceeds the 1.02V threshold voltage (decided by V_{REF}, the resistive divider, and the hysteresis window), the output of the hysteresis comparator V_{OVP} goes high. As a result, the NMOS transistor (M_1) conducts and discharges V_{LV} through a 100Ω resistor (R_1) connected to the ground. This local voltage regulation can regulate V_{LV} across a wide range of Tx power (31.6 mW to 63.1 mW when $R_{LV} = 200\ \Omega$, and 50.1 mW to 112.2 mW when $R_{LV} = 100\ \Omega$). By implementing a global power control scheme through backward data telemetry [63, 64], the V_{OVP} can also be used to regulate the Tx power (P_{TX}) level. In this configuration, the OVP circuit can protect V_{LV} against high Tx power up to approximately 158.5 mW.

Clock recovery and zero-crossing detection

The 40.68 MHz system clock is recovered from the AC signals using a comparator. However, the conventional latch-based comparator [65] suffers from a significant comparison delay, leading to losses during CM charging as explained in Section 4.2.2. This work uses a delay-compensated comparator (Fig. 4.11(b)) [66] to achieve clock recovery and zero-crossing detection. The unbalanced sizing in the PMOS input pair ($M_{1,2}$) introduces an offset voltage V_{os} ($V_{AC1b} + V_{os} = V_{AC2}$) of approximately 250 mV to account for the delay between the cross point of the AC signals and the rising edge of the comparator output (f_{clk}), resulting in a 25% increase in inductor current during the CM operation. Additionally, the M_3 transistor, sized identically to M_2, is placed alongside M_1 to generate the falling edge of f_{clk}, thereby maintaining the duty cycle of the 40.68 MHz clock close to 50%.

Negative voltage generator

A negative supply ($-V_{LV}$) is required to strongly turn OFF the native NMOS transistor used in resonance breakup switches SW_{1a}/SW_{1b} during CM operation. This supply is provided by the negative voltage generator illustrated in Fig. 4.11(c), which consists of two charge pumps (formed by M_3~M_{10} and C_{1a}~C_{2b}) working in time-interleaved mode and two output switches (M_1 and M_2). The charge pumps are controlled by the non-overlapping 40.68 MHz clock outputs CLK_1 and CLK_2, to continuously charge the output capacitor C_3 through the output switches. The nominal output voltage when CM is activated is -0.5 V.

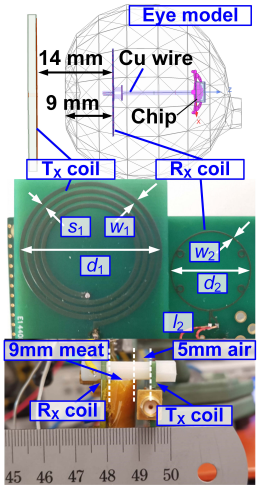
4.4 Experimental Results

The proposed dual-output PMU was implemented using standard 40-nm CMOS technology. The chip micrograph (Fig. 4.12) shows that the design occupies a core area (active circuit area, w/o test I/O pads) of 1.18 mm^2, and a total area of 2.28 mm^2. A replica rectifier circuit (not included in the core area) without the on-chip resonance capacitor is also integrated to measure the rectifier input power for PCE.

The measurements of the PMU chip use a custom-designed coil link, following the design methodology introduced in [67]. The Tx/Rx coils are separated by 14 mm, a typical separation distance for retinal prostheses applications. The coil dimensions are optimized to meet the strict surgical constraints, and its parameters have been characterized using a vector network analyzer (Keysight P9374A) - details in Table 4.1. The Tx *LC* resonator is matched to the 50Ω impedance of an RF power source (Agilent N5183B MXG), and the Tx power is adjusted to regulate V_{LV} = 1 V according to the load R_{LV}.

Table 4.1: Parameters used for the WPT system measurement

Item	Tx(L_1)	Rx(L_2)
Outer diameter d [mm]	26.8	16
# of turns	4	1
Trace width w [mm]	0.8	0.25
Trace spacing s [mm]	0.6	-
28-AWG Cu wire l_2	-	8 mm
Inductance [nH]	595.41	74.06
Quality factor	186.82	24.76
Frequency [MHz]	40.68	
Cu trace thickness	35 µm	
Substrate thickness	1.57 mm Fr4	
Distance [mm]	14 (air+tissue)	
Coupling factor k_{12}	0.0523	



4.4.1 Cold startup measurement

Fig. 4.13 presents the measured cold start-up waveforms of the Rx chip under a 250Ω load at V_{LV} with a transmitter power of 13.6 dBm (22.91 mW). The rectifier initially operates in a passive-mode configuration, formed by the transistors $M_1(M_2)$, with uncertain gate voltage, and the body diode of $M_4(M_3)$. As V_{LV} increases,

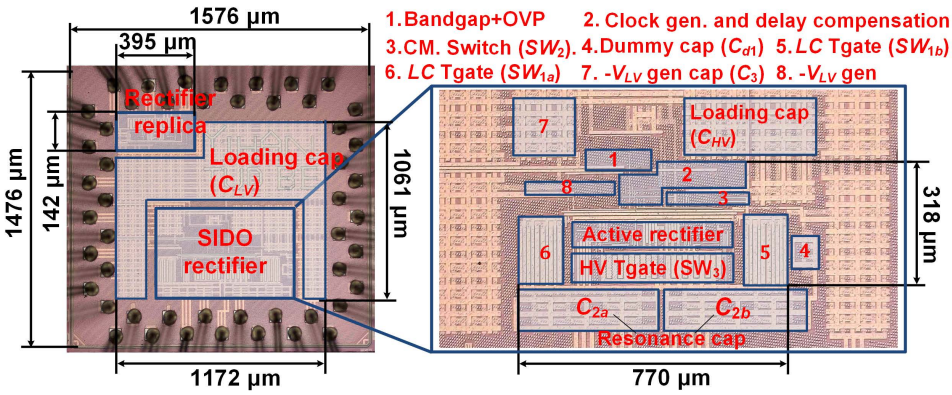


Figure 4.12: Die photograph of the 40-nm CMOS PMU chip.

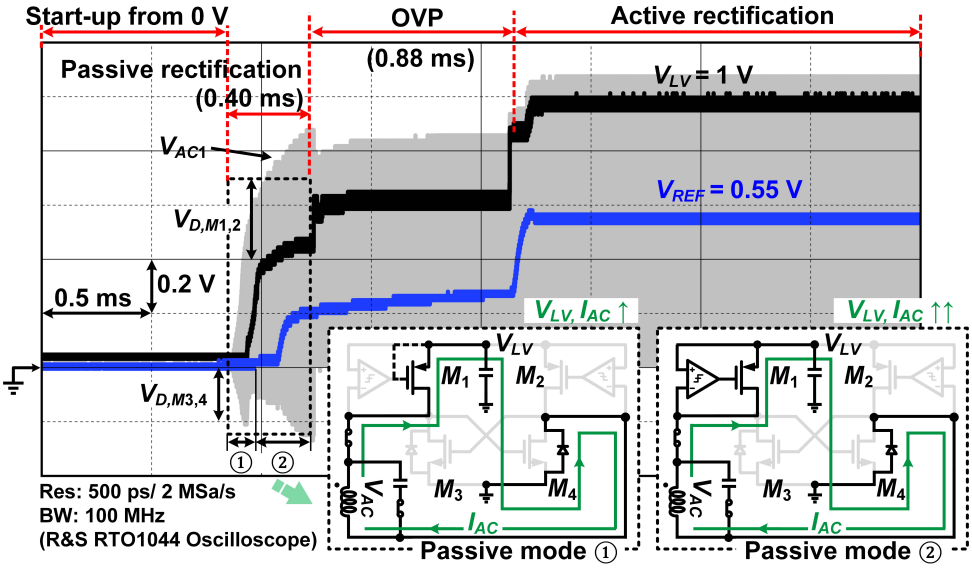


Figure 4.13: Measured cold start-up procedure at R_{LV} = 250 Ω and P_{TX} = 22.91 mW. The passive mode configuration at one of the conduction phases is shown in the lower right corner.

the uncompensated comparator begins to generate digital control signals to drive $M_1(M_2)$. After approximately 0.4ms of passive rectification, V_{LV} reaches 0.6 V, activating the OVP while V_{REF} gradually increases. The OVP phase lasts for 0.88 ms until V_{REF} exceeds 0.3 V, and the chip starts operating normally to regulate V_{LV}.

4.4.2 Voltage-mode (single) output measurement

Fig. 4.14(a) shows the setup for measuring the voltage conversion ratio (VCR) in the VM rectifier and presents the AC-in and DC-out waveforms during VM operation. The phase differences between different channels on the oscilloscope have been calibrated to ensure accuracy. With a 250Ω load at V_{LV}, the measured mean value of V_{LV} is 0.99 V, with a ripple of 31.67 mVpp. The peak-to-peak amplitude of V_{AC} is 2.11 V, yielding a VCR of 93.84%.

Since this design incorporates an on-chip resonant capacitor (C_2), a replica circuit without the integrated resonant capacitor is used to measure the rectifier PCE, avoiding the need for complicated current measurements in the *LC* tank. Fig. 4.14(b) illustrates this setup, based on [36, 58]. A 10Ω current-sensing resistor captures the input current, which is then multiplied by V_{AC} to calculate the average input power across several cycles. Meanwhile, the average output power at V_{LV} is measured using an isolated voltage meter. For a 250 Ω load, the measured input power is 4.02 mW with $V_{LV} = 0.91$ V, resulting in a PCE of 82.5%.

Fig. 4.14(c) provides a summary of the simulated and measured VCR and PCE across all loads, ranging from 100 Ω to 350 Ω. The measured VCR peaks at 94.23% at R_{LV} = 350 Ω, while the PCE reaches 85.87% at $R_{LV} = 150$ Ω.

4.4.3 Dual-mode (dual) outputs measurement

Fig. 4.15 shows the measured transient waveforms to validate the dual VM/CM operation. The test conditions are set to R_{HV} = 400 kΩ and $R_{LV} = 150$ Ω, with a transmitter power of 17.2 dBm. The negative voltage generator operates as intended, producing -0.5 V to disconnect the *LC* resonator and enable the CM operation every 0.98 µs (N_0 = 40). As a result, V_{AC1} rises above V_{HV} (2.0 V), leading to an undershoot in V_{LV} of 113.83 mV due to the lack of charging in the CM and FW phases. Thanks to the FWR structure, the undershoot only lasts for one cycle. This is acceptable since V_{LV} has more relaxed requirements during HV stimulation.

Fig. 4.16(a) shows the measured charging procedure of V_{HV} alongside the delay compensation logic outputs, validating the CM charging concept. The test conditions are set at R_{HV} = 1 MΩ and R_{LV} = 200 Ω, with a transmitter power of 15.7 dBm. During V_{HV} charging, the voltage rises from 1.078 V to 2.029 V within 7 µs. The delay compensation logic $D[1:0]$ ($D[2]$ not shown) automatically changes as V_{HV} increases according to the functionality described in Section 4.3.3. The maximum achievable V_{HV} depends on the transmitter power (Fig. 4.16(b)) and the load current I_{HV}.

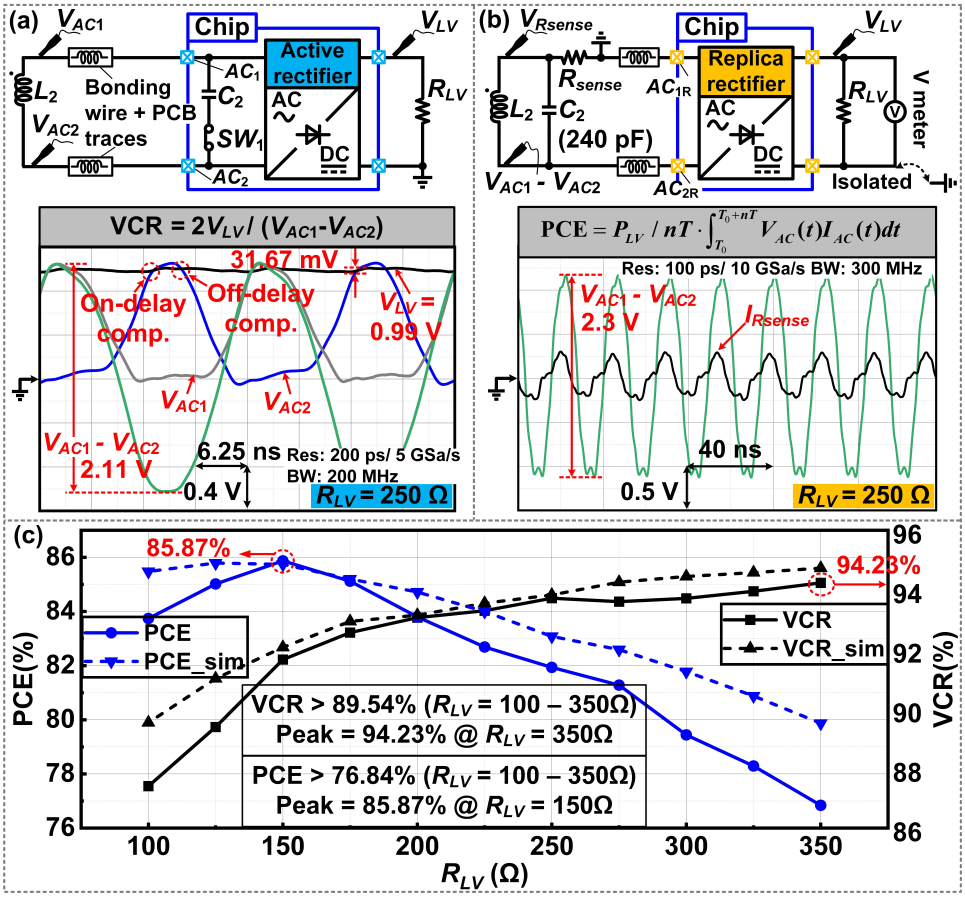


Figure 4.14: (a) VCR measurement diagram with measured waveforms of V_{LV}, V_{AC1}, and V_{AC2} for VCR calculation at R_{LV} = 250 Ω, (b) PCE measurement diagram with measured waveforms of V_{AC2} - V_{AC1} and V_{Rsense} for PCE calculation at R_{LV} = 250 Ω, (c) Measured PCE and VCR versus R_{LV}.

When I_{HV} increases to 4.88 μA, V_{HV} can be regulated to 1.95 V. Fig. 4.16(c) illustrates the correlation between V_{HV} and the maximum current load, as a function of the transmitter power. High output current can be achieved by increasing P_{TX}.

4.4.4 Load transient measurement

Fig. 4.17(a) and (b) present the load transient responses of V_{LV} and V_{HV}, respectively. As the Tx power increases from 12.2 dBm to 16.0 dBm, V_{LV} is regulated around 1.0 V under both light and

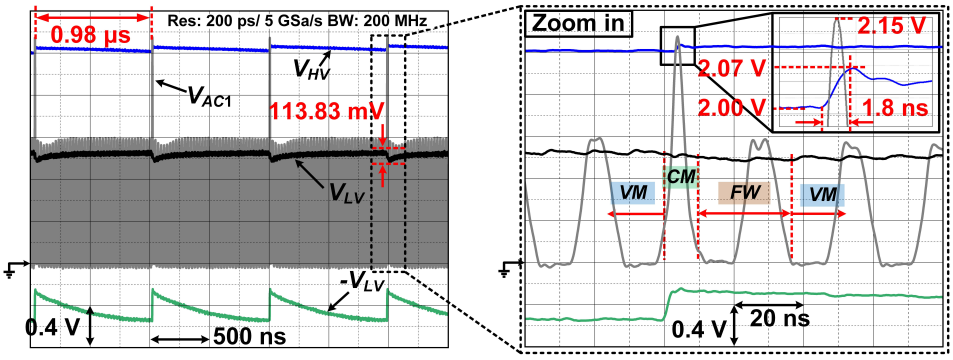


Figure 4.15: Measured dual VM/CM operation waveforms under the conditions of R_{HV} = 400 kΩ and R_{LV} = 150 Ω.

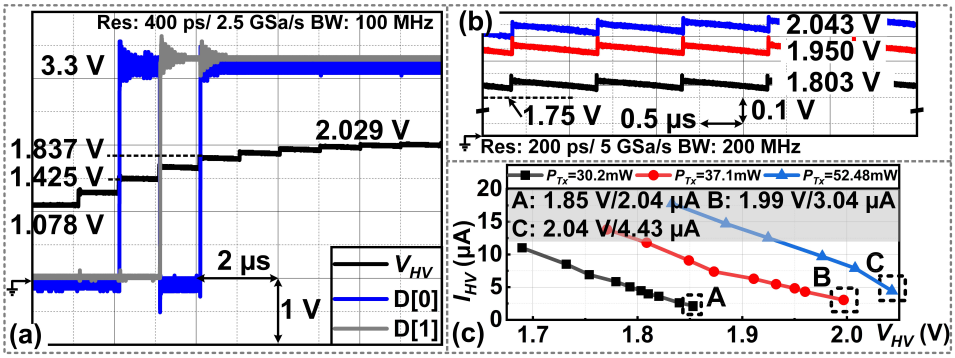


Figure 4.16: (a) Measured V_{HV} charging and delay compensation logic (3.3V I/O) waveforms with R_{HV} = 1 MΩ, (b) Measured steady state V_{HV} with R_{HV} = 400 kΩ under different P_{TX}, (c) Measured maximum I_{HV} and V_{HV} under different P_{TX}.

heavy load conditions, exhibiting a 105 mV undershoot and a 97.4 mV overshoot at 20 ns rise/fall load step. The V_{HV} regulation is achieved through a self-adaptive scheme that adjusts to varying load conditions. Under the light load condition, the slower discharge rate requires less frequent recharging, validating the proposed mode-switching concept.

4.4.5 System-level efficiency measurement

Fig. 4.18(d) presents the system-level efficiency results, covering both PTE and end-to-end (E2E) efficiency using the Tx/Rx coils in Table 4.1. The PTE is measured using an external reso-

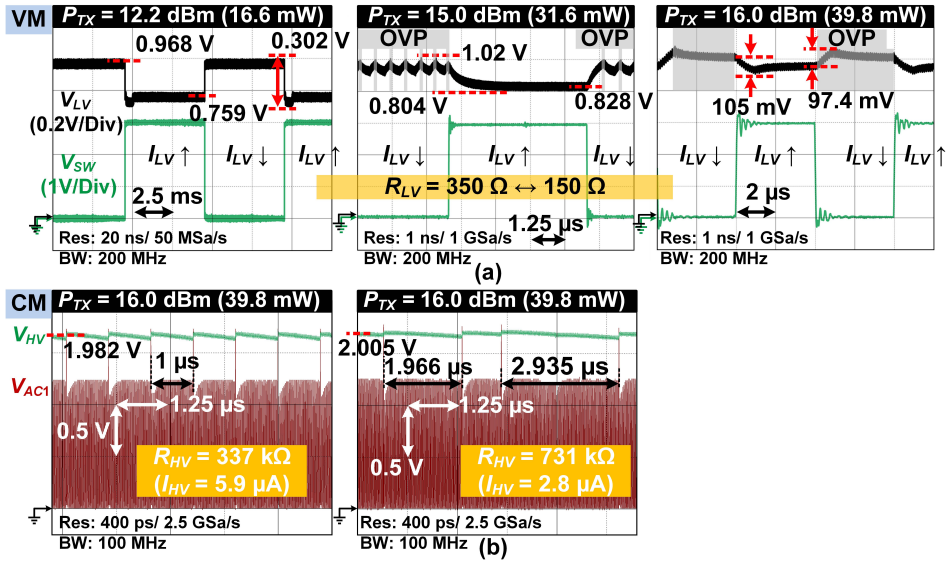


Figure 4.17: Measured load transient response waveform of (a) V_{LV} with R_{LV} switching between 150 Ω ~ 350 Ω and (b) V_{HV} with R_{HV} switching between 338 kΩ and 731 kΩ.

nant capacitor C_2 terminated with a resistive load R_{LV} without the chip (Fig. 4.18(a)). The measured PTE matches the simulated PTE closely, achieving 28.98% at 225Ω load. The E2E efficiency is measured using the PMU chip with the integrated resonant capacitor and a resistive load for each output, R_{LV} and R_{HV} (Fig. 4.18(b)). The peak E2E efficiency for VM and dual VM/CM are 17.32% and 14.94%, respectively, when R_{LV} = 225 Ω. Notably, the E2E efficiency decreases at most by 2.7% across all loads when regulating also V_{HV}. The E2E efficiency was measured using a 9-mm pork sample with a 5-mm air gap between the Tx/Rx coils to simulate biomedical implant conditions (see Table 4.1, bottom-right). The *ex vivo* experiment results show negligible efficiency degradation, with E2E efficiency decreasing by less than 0.48% across all loads.

The difference between the PTE and E2E efficiencies is due to three main reasons: (i) The rectifier PCE accounts for 3.66% losses, (ii) The breakup switch in the *LC* resonator accounts for 2.83% losses, (iii) The impedance of the bonding wires (gold, 1.5 mm long, 25 µm diameter, two parallel-connected wires per AC input) and PCB traces between the Rx coil and the on-chip resonance capacitor account for 5.17% losses. This is due to the quality factor drops of the receiver from 28.1 to 21.8 (simulated result, see Fig. 4.18(c)).

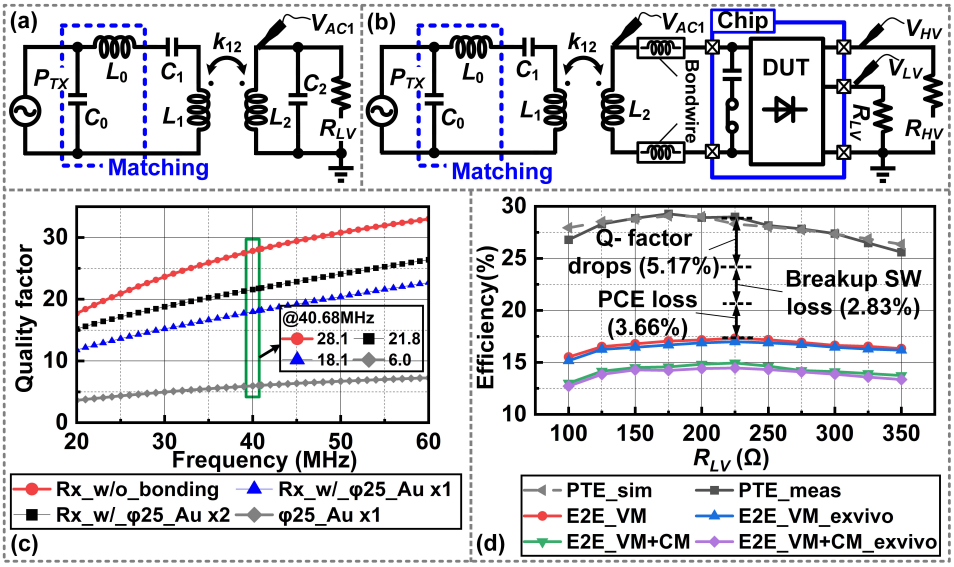


Figure 4.18: (a) PTE measurement setup, (b) E2E efficiency measurement setup, (c) Simulated Q-factors of the receiver coil w/ and w/o the bonding wires connections, and (d) Measured system-level PTE/E2E vs. R_{LV} with R_{HV} fixed at 400 kΩ.

This issue can be mitigated using parallel bonding wires to lower their equivalent resistance and adjust the PCB/coil designs.

4.4.6 Power breakdown

Fig. 4.19 shows the simulated power breakdown of the proposed Rx chip design operated in the VM and dual VM/CM under the load condition of R_{LV} = 250 Ω. The dual VM/CM operation achieves an output efficiency of 68.1% on V_{LV}, which is slightly less (4.19%) than that of the VM operation. The lower power efficiency is mainly due to the extra power consumption for the level shifters and the negative voltage generation block in Fig. 4.7(b), in addition to the cycles used for the CM and FW phases, during which V_{LV} is not charged.

4.4.7 Comparison with state-of-the-art

The performance of the proposed PMU is summarized and compared with the state-of-the-art in Table 4.2. Most designs using voltage-mode charging [34–37] assume that V_{HV} has the largest load, thus V_{AC}>V_{HV} most of the time. While other works adopt current-mode charging to mitigate the need for large V_{AC}, their

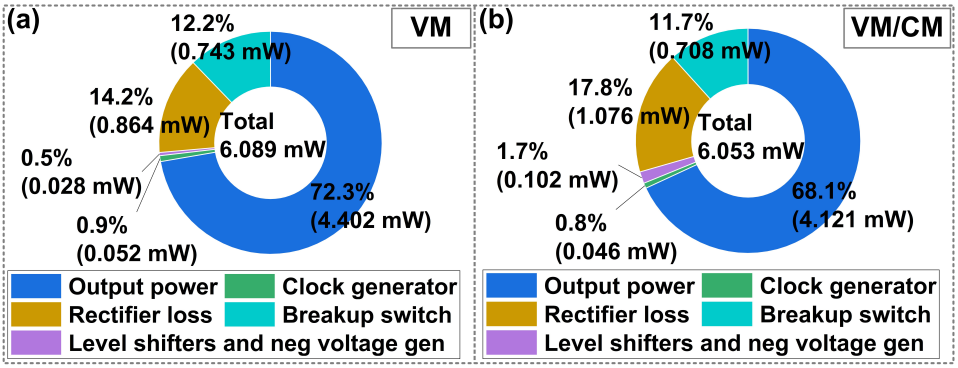


Figure 4.19: Simulated power breakdown of the chip working at R_{LV} = 250 Ω in (a) VM operation, (b) VM/CM operation.

performance in terms of voltage ripple and voltage rating (by using thick-oxide devices) remains constrained by using HWM charging [11, 23, 48]. Additionally, the large off-chip output capacitors (several µF) hinder system integration for implantable devices.

In contrast, the proposed SIDO PMU is the only design that prioritizes delivering the main portion of power to V_{LV} while achieving high power efficiency. This represents a significant advantage over previous VM rectifier designs that prioritize identical currents to charge both outputs. With all resonant and output capacitors integrated on-chip, the proposed design occupies only 1.18 mm^2 of active chip area. The measured voltage ripple on V_{LV} remains competitive with other designs that rely on off-chip capacitors (100 ∼ 500× higher than the on-chip capacitor used in this work), thanks to the FWR structure and high resonance frequency.

4.5 Conclusion

This paper presents a fully integrated SIDO PMU for wirelessly powering modern closed-loop neuromodulation implants. The proposed SIDO PMU is configurable to operate in either single-output (V_{LV}) or dual-output mode (V_{LV} and V_{HV}). In the dual-output configuration, it uses a combined voltage/current-mode strategy to simultaneously generate V_{LV} for high-power loads and V_{HV} for low-power loads. The chip operates at 40.68 MHz and requires only an external Rx coil while achieving a peak E2E efficiency of 14.94% when enabling the dual VM/CM charging. The wireless power link can provide a maximum output power of 10 mW on V_{LV} and drive µA load levels on V_{HV}. These advantages make this work attrac-

Table 4.2: Comparison to state-of-the-art dual-output rectifier designs

Item	TBioCAS'19 [23]	TBioCAS'20 [34]	JSSC'21 [35]	JSSC'22 [11]	TCAS-I'23 [48]	JSSC'24 [36]	JSSC'24 [37]	This work
Process	350-nm	180-nm	180-nm	180-nm HV BCD	180-nm	65-nm	65-nm	40-nm
Frequency (MHz)	1	1-10	6.78	40.68	6.78	40.68	13.56	**40.68**
Structure	CM	Full-wave VM	HWM[2]	HWM + CM	CM	Full-wave VM + HWM	Full-wave VM	**Full-wave VM + CM**
Cold-startup	No	No	Yes	Yes	Yes	Yes	Yes	**Yes**
Output voltage	2.6 V & 3.9 V	1.5 - 3 V & 1.5 - 3 V	1.8 V & 3.3 V	10 V & 4.7 V & 2 V	1.8 V & 3 V	1.1 V& 2.2 V	1.2 V & 2.5 V	1.0 V & 2.0 V
Power P_{OUT} (mW)	4.7 (mainly P_{LV})	≤65 (mainly P_{HV})	≤1020 (mainly P_{HV})	186 (mainly P_{HV})	≤ 7 (mainly P_{HV})	≤60.5 (mainly P_{HV})	≤ 20 (mainly P_{HV})	**≤ 10 (mainly P_{LV})**
PCE@P_{HV} (mW) & P_{LV} (mW)	75.3%@N/A & 4.7	90.75%@62.5 & 1 83%@6.25 & 1.0	91.9%@660 & 360 65%@66 & 36	81%@186 & N/A & N/A	85.1%@1 & 1	90.1%@55 & 1.1 76%@5.5 & 5.5	88%@8 & 8	**85.87%@0.011 & 6.7**
Active area (mm^2)	1.35	< 6	< 0.601	< 4.6	2.7	< 0.74	0.145[4]	**1.18 & 0.24**[5]
Tx/Rx diameter ratio	70 mm / 22 mm	N/A (cap. coupling)	N/A	33 mm / 24 mm	41 mm / 23 mm	16.5 mm / 4 mm	35 mm / 30 mm	26.8 mm / 16 mm
Coil distance (mm)	N/A	N/A	15	12	10	2	6-15	14
Link efficiency	N/A	N/A	N/A	86.6%	N/A	N/A	N/A	25.59% - 29.28%
End-to-end efficiency	N/A	N/A	N/A	69.66%	31.3% @ P_{OUT} = 2 mW	N/A	32.4-62.7%	VM: 17.32%, VM + CM: 14.94%
Output voltage ripple	N/A	< 6 mV_{pp}	42 - 60 mV_{pp}	N/A	CM: 180 mV_{pp}	90 mV_{pp}	N/A	**VM: 31.67 mV_{pp}, VM + CM: 113.83 mV_{pp}**
No. of off-chip capacitors[1]	4 (0.1 µF / 4.7 µF / 4.7 µF / 100 µF)	2 (0.47 µF / 1 µF)	3 (1.1 nF[3] / 4.7 µF / 4.7 µF)	4 (N/A)	3 (N/A)	3 (194 pF[3] / 220 nF / 470 nF)	3 (238 pF[3] / 1 µF / 1 µF)	**0**

[1] Including the resonant capacitor [2] Half-wave mode [3] Calculated from the resonant frequency [4] Including the on-chip decoupling capacitor [5] w/ & w/o on-chip capacitors

tive for applications requiring distinct power levels and precision on different outputs.

Appendix

In this section, we derive Eq. (4.6) and Eq. (4.7) for the optimal resonant cycle analysis using rectifier waveforms in Fig. 4.3.

CM operation

The CM operation begins at $t = t_0$. i_{L2} first charge the parasitic capacitor C_{par} until V_{AC1} exceeds V_{HV} ($t = t_1$). Neglecting the inductor resistance R_2, and assuming the initial condition of $i_{L2}(t_0) = i_{L2\text{MAX}}$ and $\frac{di_{L2}(t)}{dt}\big|_{t=t_0} = 0$, the nodal equation can be derived as:

$$L_2 \frac{di_{L2}(t)}{dt} + \frac{1}{C_{\text{par}}} \int_{t_0=0}^{t_1} i_{L2}(t)dt = 0 \tag{4.10}$$

At t_1, C_{par} is charged to $V_{AC1} = V_{HV}(n)$, where n is the current CM charging cycle. Across two consecutive charging cycles (from t_2 to the next t_1, approximated as $\Delta T \approx \frac{N_0}{f_{clk}}$, V_{HV} decreases by Eq. (4.11), due to the absence of charging:

$$V_{HV_disch}(n) = V_{HV}(n-1)(1 - e^{-\Delta T/\tau}) \tag{4.11}$$

where $\tau = R_{HV}C_{HV}$ is the time constant formed by the load and filtering capacitor at V_{HV}, f_{clk} is the resonant frequency, and N_0 is the number of AC periods in between CM charging cycles. Hence, V_{HV} at step n can be derived as (neglecting the zero crossing voltage, V_{ZC}, for simplicity):

$$V_{HV}(n) = V_{HV}(n-1)e^{-\Delta T/\tau} = \frac{1}{C_{\text{par}}} \int_{t_0=0}^{t_1} i_{L2}(t)dt \tag{4.12}$$

By solving Eq. (4.10) and Eq. (4.12), the solution for t_1 and the corresponding current $i_{L2}(t_1)$ can be obtained:

$$t_1 = \frac{1}{\omega_d} \arcsin\left[\frac{\omega_d C_{\text{par}} V_{HV}(n-1)e^{-\Delta T/\tau}}{i_{L2,\max}}\right] \tag{4.13}$$

$$i_{L2}(t_1) = i_{L2,\max} \cos(\omega_d t_1) \tag{4.14}$$

During the CM charging transfer phase (t_2), $i_{L2}(t)$ decreases approximately linearly with a slope of $i'_{L2}(t_1)$ due to the short charging time ($t_2 < 2$ ns). Hence, $i_{L2}(t_2)$ can be derived as:

$$i_{L2}(t_2) = i_{L2}(t_1) + i'_{L2}(t_1) \cdot (t_2 - t_1) \tag{4.15}$$

Finally, the voltage increase per charging cycle can be analytically approximated using Eq. (4.16):

$$V_{HV_ch}(n) = \frac{\int_{t_1}^{t_2} i_{L2}(t)dt}{C_{HV}} \simeq \frac{i_{L2}(t_1) + i_{L2}(t_2)}{2} \cdot \frac{t_2 - t_1}{C_{HV}} \tag{4.16}$$

$V_{HV}(n)$ can be derived recursively based on Eq. (4.11) and (4.16).

VM operation

The VM operation begins at $t = t_0'$. $i_{L2}(t)$ first charge the resonant capacitor C_2, and the parasitic capacitance C_{par}, until V_{AC2} exceeds V_{LV} plus the rectifier power switch drop V_D at $t = t_3$:

$$\frac{1}{C_2}\int_{t_0'=0}^{t_3} i_{L2}(t)\frac{C_2}{C_2 + C_{\text{par}}}dt + V_{ZC} = V_{LV}(n-1) + V_D \tag{4.17}$$

By solving Eq. (4.17), the expression for t_3 is derived as follow:

$$t_3 = \frac{1}{\omega}\arcsin\left\{\frac{\omega(C_2 + C_{\text{par}})[V_{LV}(n-1) + V_D - V_{ZC}]}{i_{L2,\max}}\right\} \tag{4.18}$$

Similar to Eq. (4.11) and Eq. (4.16), the precise charging and discharging voltages of V_{LV} in each half-period cycle can be calculated as follows:

$$V_{LV_ch}(n) = \frac{1}{C_{LV}}\int_{t_3}^{t_4} i_{L2}(t)dt \tag{4.19}$$

$$V_{LV_disch}(n) = [V_{LV}(n-1) + V_{LV_ch}(n)](1 - e^{-\Delta T'/\tau'}) \tag{4.20}$$

where $t_4 = 1/4f_{clk}$, $\tau' = R_{LV}C_{LV}$ is the time constant formed by the load and filtering capacitor at V_{LV}, $\Delta T' = t_6 - t_4 \simeq t_3 + 1/4f_{clk}$. $V_{LV}(n)$ can be derived recursively based on Eq. (4.19) and Eq. (4.20).

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Chapter 5

Conclusion and Outlook

This dissertation presents the circuit- and system-level designs of highly integrated wireless power and data telemetry systems for an artificial retina prosthesis using inductive links. The proposed solutions address several critical challenges in future implant system designs. This chapter summarizes the research by discussing the common limitations of existing approaches, highlighting the key contributions of this work, and outlining directions for future research. Section 5.1 introduces the motivation behind this study and explains how the selected topology is best suited for the intended application. Section 5.2 presents the key findings obtained throughout the research. Section 5.3 explores the emerging research trends and potential improvements for future developments.

5.1 Motivation and main contributions

The motivation and main contributions of this thesis are discussed in this section, in order to address the following research questions:

1. For the wireless link design: What is the optimal link structure and topology for the wireless power and data telemetry link?[Q1.1] What are the optimal parameters for coil number, number of external devices, coil diameter, separation distance, materials, frequency, and other relevant factors?[Q1.2] How should the power RX coil be interconnected with the chip?[Q1.3] What are the associated power losses, and how can they be minimized?[Q1.4] Should the resonance frequency be tunable?[Q1.5]

2. For the data telemetry: How should the communication topology be selected based on the system clock and input voltage requirements?[Q2.1] How can these topologies be designed for compatibility with the implanted chip (a highly asymmetrical system with greater constraints inside the chip and more flexibility outside)?[Q2.2] How can external components be minimized or eliminated?[Q2.3]

3. For the PMU design: How can the power efficiency of the PMU IC be maximized, given the chosen coil link design?Q3.1 How should voltage regulation be implemented (e.g., LDO, DC-DC) considering load variations?Q3.2 How can multiple outputs with different loading conditions be generated from a single AC input?Q3.3 How can external components (resonant capacitors, filtering capacitors, etc.) be minimized while maintaining competitive performance?Q3.4

Modeling of Inductive Wireless Power and Data Telemetry Links Compatible with a Biological Environment. (Chapter 2)

Designing and optimizing an inductive link for high power and data efficiency in a biological environment presents significant challenges. Existing inductive power and communication systems mostly rely on either commercial off-the-shelf (COTS) components [1] or handmade wire-wound coils, such as Litz wire-based designs [2, 3], typically consisting of single or multiple turns with insulated layers. While commercial coil products simplify the design process, they often fail to meet specific application requirements, such as power range and miniaturization constraints. In contrast, wire-wound coils provide greater flexibility in tuning and placement while also exhibiting reduced skin effect losses. However, they offer limited geometric optimization without sophisticated post-processing machinery. Moreover, conventional analytical methods for coil geometry calculation often lead to reduced accuracy. Variations in modeling parameters, such as frequency-dependent lumped component values, introduce inconsistencies between simulation results and fabricated prototypes, necessitating additional calibration steps [4, 5]. These challenges make wire-wound coils less suitable for applications that demand minimal calibration efforts. In recent years, printed circuit board (PCB) coil designs have gained popularity in implantable systems [6–8] due to their cost-effective fabrication process and strong correlation between modeled and actual parameters. Additionally, PCB coils offer greater flexibility in shape and geometric optimization, making them well-suited for concept verification. Despite the widespread use of PCB coils in implantable systems, limited research has focused on optimizing coil geometries to maximize link efficiency within a biological environment. Further exploration in this area is essential to enhance the performance and reliability of wireless power and data telemetry systems for biomedical implants.

To address the aforementioned challenges, a general design principle for inductive wireless power and data transmission using PCB coils has been developed, with a retinal prosthesis as a case study.

Due to the complexity introduced by the frequency-dependent lossy tissue model and the parasitic component network, conventional analytical methods conducted in an air medium are no longer sufficient [9, 10]. Consequently, finite element method (FEM) tools are utilized to achieve high-accuracy simulations and to extract scattering parameters for link characterization. The proposed methodology employs a parameter sweep method to determine the optimal dimensions of planar spiral PCB coils, maximizing efficiency while satisfying dimensional constraints. Though FEM simulations ensure consistency between theoretical models and experimental measurements, they suffer from slow convergence, particularly when multiple parameters require optimization. To solve this problem, this work introduces a guided iterative search process for inductive link optimization, effectively reducing computational complexity and design time. Compared to conventional design and optimization procedures [9,11], the proposed approach significantly alleviates the design effort. The optimization process is divided into two stages: coarse optimization and fine optimization. The coarse optimization stage focuses on improving the quality factor and provides an initial estimation of the parameter range corresponding to the selected operating frequency. The fine optimization stage further refines link efficiency based on the preliminary results, ultimately determining the final geometries. By independently optimizing the quality factors of the transmitter and receiver coils instead of directly optimizing link efficiency through exhaustive parameter sweeps, the iterative FEM simulation process achieves faster convergence while maintaining computational accuracy[Q1.2]. This methodology provides a systematic and efficient approach for inductive link optimization.

The optimization process for the power and data links is determined after selecting a suitable topology and operating frequency. Amplitude shift keying with pulse position modulation (ASK-PPM) is particularly suitable for wireless power transfer in this application. This modulation scheme offers several advantages: (i) a simple demodulation circuitry with low energy consumption, (ii) straightforward clock and data recovery without frequency or phase shifts, and (iii) infrequent pulses that ensure a sufficient received power level. For the data link topology, 4 GHz ultra-wideband (UWB) communication is preferred, as it aligns well with the form factor of the target implant design while providing sufficient link gain with minimal energy consumption in the transmitter driver circuit[Q1.1]. Since the power coil link geometries are primarily optimized for high power transfer efficiency at the selected 40.68 MHz carrier frequency and the frequency-invariant ASK-PPM modulation scheme is chosen for robust data communication, the resonance frequency

must remain stable within this design. This ensures reliable system performance and addresses the research question concerning resonance frequency tuning[Q1.5].

This work demonstrates that by implementing the proposed optimization procedure and selecting an appropriate operating frequency, the achieved inductive link efficiencies can surpass those reported in previous studies employing comparable coil dimensions but operating at lower frequencies. A power coil link operating at 40.68 MHz and a data antenna link operating at 4 GHz were fabricated to validate the proposed concept. For the power link, a maximum power transfer efficiency of 29.28% was observed at a 175 Ω load, with only a 0.86% efficiency reduction when the link was separated by the tissue-air medium, ensuring sufficient power for wireless operation. Notably, the Rx coil consists of two components: a planar spiral coil and two interconnection wires. The interconnection wire allows the spiral coil to be positioned closer to the Tx power coil, thereby achieving higher efficiency. Furthermore, the Rx received power is transferred through the wire. The interconnection wire is composed of an 8 mm 29 AWG copper wire and a 2 mm 25 μm gold bonding wire, which connects the Rx circular coil to the chip and offers the flexibility of frequency tuning to match the on-chip resonance capacitor. The power loss caused by the interconnection wire is modeled and can be minimized by adding more parallel wires, addressing the interconnection problem[Q1.3] and loss minimization[Q1.4]. For the data link, a gain of -28.89 dB at 4 GHz with a 0.7 GHz -3 dB bandwidth was achieved. The experimental results presented in this chapter validate the prototype's ability to perform both wireless powering and data telemetry for implantable applications.

Provide a Systematic Solution for Power Management and Bi-directional Data Communication (Chapter 3)

Analyzing neural networks benefits from measuring activity from more neurons, which calls for building large-scale neural recording with high channel counts [12–14]. This imposes a challenge on the miniaturization of the chip dimension to the millimeter scale. Modern intelligent neural modulation also requires the implant systems to be designed in a closed-loop control form, which means that specific stimulation codes/control demands can be generated based on the recorded activities. As a result, bi-directional data communication should be implemented in such systems. As a fully blind test has to be performed on the implant chip without any cable connection to an external supply, the chip should be capable of receiving power through a wireless power link with a dedicated power management system. These functionalities intro-

duce trade-offs between implant size, power budget, and available design choices. Though several prior state-of-the-art systems [15–18] with wireless power and data transfer capabilities have been explored before, few of them can achieve high-efficiency fully wireless powering, low energy cost high data rate communication, and the minimal usage (ideally zero) of external components. To address these system-level design challenges[Q2.3], specific considerations have been made regarding the topology for power and data transfer.

The power management unit implements a full-bridge rectifier stage composed of Schottky diodes to perform AC-DC conversion. Zener diodes are applied on the AC input pads to prevent electrostatic discharge (ESD) breakdown. Capacitorless regulator circuits with different driving purposes are designed for high-voltage (1.8/1.8 V) and low-voltage (0.9/1.0 V) outputs, respectively. The capacitorless regulator employs a bandwidth-enhanced dual-loop structure, with the dominant pole at the error amplifier output and the non-dominant pole canceled by the active feedforward buffer stage. By implementing the concept of scaling block design based on the loading current requirement, any-load stable loop compensation can be achieved. With an on-chip reference voltage (0.6 V) generated by a sub-1V bandgap circuit, the measured 1.8 V capacitorless low-dropout (LDO) output achieves less than 11 mV ripple and +96/-120 mV overshoot/undershoot when the loading current switches between 0/4 mA within 15 ns, without stability issues or slow recovery time. In addition to self-reference generation and voltage regulation, over-voltage protection and voltage monitoring are implemented on-chip using a short-to-ground resistor and a 3-bit flash ADC, respectively, ensuring safe operation in the implant.

The data downlink unit extracts the ASK-PPM data from the power carrier signal through the power coil link. The ASK-PPM modulation scheme is selected for its reduced power loss compared to other conventional amplitude-varying modulation schemes and its self-synchronization characteristics. ASK-PPM also enables simple clock recovery using a latch comparator, eliminating the need for any on-chip precise clock reference, which typically suffers from power, area, and process-voltage-temperature (PVT) sensitivity issues[Q2.1]. The downlink data demodulator consists of an envelope detector, a PPM clock/data decoder, and a series-in-parallel-out (SIPO) circuit. Measurement results validate that both 200 kbps data recovery and 40.68 MHz clock extraction can be performed on the encoded AC input signal. The lowest achievable modulation index is 0.42, resulting in approximately 60% efficiency gain compared to conventional ASK-based schemes, leading to a significant

reduction in the on-chip filtering capacitor value, and addressing the research question of communication topology selection based on the system clock[Q2.1].

The data uplink unit operates in the ultra-wideband (UWB) frequency range, primarily to reduce the antenna size and match the overall implant size constraint (≤ 3.5 mm). Various antenna sizes within the strict 3.5 mm aperture limit have been investigated, and the resulting sweep results reveal that the frequency range between 3.5 GHz and 4.6 GHz is favorable for the small loop antenna with a 2.9 mm aperture, achieving a 39.54 dB link gain at the center carrier frequency of 4.0 GHz[Q2.2]. To meet the bandwidth and center frequency specifications of the data link, this work implements an impulse radio UWB (IR-UWB) generator, which provides a high data rate while consuming low power and area. The proposed programmable IR-UWB pulse generator is based on the edge-combining concept. By combining time-shifted short pulse sequences with tunable amplitude and frequency, this technique avoids the need for an oscillator, mixer, and filter. To enhance robustness during uplink data recovery, the design transmits both the rising and falling edges of the Manchester code. However, this approach requires an XOR logic gate before the driver circuit, which introduces long propagation delays and degrades the achievable carrier frequency. Since a high-parasitic process is used in this design (TSMC 180-nm BCD, ×1.708 parasitic than TSMC 180-nm GP and ×3.193 than TSMC 40-nm) achieving a high carrier frequency is challenging. To address this issue, a dual-edge pulse conversion stage is introduced before the transmitter driver to reduce the long propagation delay caused by the XOR logic. This design allows the detection of both the rising and falling edges without compromising the frequency of each time-shifted pulse. Measurement results demonstrate that the frequency tuning range is from 2.16 GHz to 4.56 GHz, covering the target 4.0 GHz center carrier frequency band. The power spectrum density of the measured Gaussian-distributed pulse sequence at the IR-UWB transmitter output shows a peak tone of -54.15 dBm at 3.68 GHz, complying with the FCC emission mask.

Finally, this work presents a sampling-based envelope detector circuit that eliminates the need for the area-consuming filtering capacitor and static current consumption typically needed in conventional average-detector-based demodulator structures. This approach can achieve a lower modulation index and is fully compatible with the ASK-PPM data demodulation scheme. A lower voltage ripple in the rectified DC output can also be expected.

Propose an Innovative Dual-Mode Dual-Output Full-Bridge Rectifier Structure with Zero Off-Chip Capacitor (Chapter 4)

Modern closed-loop neural implants require a low-voltage, high-power supply for always-on neural state monitoring and a high-voltage, low-power supply for personalized event-driven stimulation. To provide different supply rails, conventional wireless power receivers typically involve several cascaded power conversion stages consisting of a rectifier and a regulator or DC-DC power converter. However, the two-stage cascaded structure introduces efficiency penalties and increases circuit volume, resulting in a reported overall power conversion efficiency of only 75% [19]. Alternatively, single-stage rectifiers capable of generating two regulated output voltages with distinct voltage levels have been widely studied in recent years. Most of these topologies are based on several active rectifiers working in voltage mode and connected in parallel. Since no cascade stage loss occurs during power conversion, state-of-the-art single-stage rectifiers can achieve power conversion efficiencies exceeding 88% [6–8]. However, voltage mode rectifiers exhibit reduced efficiency when the output power is dominated by the low-voltage output. Due to the sinusoidal nature of the inductor current, the charging current flowing to each output is identical. If the high-voltage output is not charged frequently, approximately 27% efficiency degradation is observed [6]. Alternatively, current-mode charging circuits function as voltage boosters, which can increase the AC input voltage to the high-voltage output when required. If the power consumption on the high-voltage output is significantly lower than that of the low-voltage output, current mode charging can complement voltage mode charging. Therefore, a new approach is proposed to generate regulated dual-output voltages while satisfying the power level requirements of modern closed-loop neural implants.

This work presents a fully integrated dual-output power management unit with dual voltage/current mode operation for a 40.68 MHz inductive wireless power link. The chip primarily operates in voltage mode, utilizing an active full-wave rectifier (FWR) to regulate a low-voltage output with high power efficiency and minimal output ripple. It transitions to current mode rectification only when a high-voltage output is required. This dual-mode operation enables the receiver antenna to resonate at an AC input amplitude close to the low output voltage (with high output power) to maximize end-to-end efficiency in voltage mode while still supporting high output voltage generation (with low output power) in current mode[Q3.1]. The relatively high resonance frequency of 40.68

MHz reduces the required resonant and filtering capacitance, allowing both to be integrated on-chip[Q3.4]; the only external component is the receiver coil. A novel resonance breakup switch control scheme ensures a seamless cold start-up of the chip without any external supply voltage. The chip was fabricated using 40 nm CMOS technology with an active area of 1.18 mm^2 and was tested in a wireless power link. Measurement results demonstrate that the chip can simultaneously regulate two outputs, $V_{LV} = 1$ V and $V_{HV} = 2$ V[Q3.3], with a maximum output power of 10 mW and 32.6 μW for V_{LV} and V_{HV}, respectively. Under optimal output power conditions ($P_{LV} \approx 4.4 \sim 6.7$ mW), the system achieves a peak power conversion efficiency (PCE) of 85.87% and a peak end-to-end (E2E) efficiency of 17.32% when only V_{LV} is regulated. The E2E efficiency decreases to 14.94% when both outputs are regulated.

5.2 Main findings

1. The 4 GHz data antenna link has lower sensitivity to angle misalignment caused by eye rotation compared to the power coil link operating at 40.68 MHz. This is because its subwavelength dimension enables a large angle misalignment range, thereby reducing the effect of implant rotations on the achievable link gain (Chapter 2).
2. The ASK-PPM modulation scheme achieves significantly higher power efficiency in the receiver circuit than conventional ASK-based methods. Higher power efficiency can be attained by optimizing the modulation index of the AC signal while maintaining accurate data extraction (Chapter 3).
3. Parasitic capacitance is a primary bottleneck limiting the speed and performance of analog circuits, affecting the loop bandwidth of the dual-loop regulator, the resonant frequency of the IR-UWB pulse generator, and the achievable high-level output voltage of the dual-output rectifier. The regulator exhibits a high-frequency pole at the power transistor gate, the pulse generator experiences noticeable propagation delays in logic gates, and the rectifier, operating in both voltage and current modes, suffers power losses due to parasitic capacitance. Consequently, these parasitic effects must be carefully evaluated. Mitigating these issues requires efficient power allocation in the design phase (Chapter 3 and Chapter 4).
4. The presented novel resonance breakup switch reduces resistive losses within the resonator loop during a full-wave rectification period. This enables high efficiency in full-wave voltage mode rectification when the breakup switch is closed and facil-

itates high voltage output in current mode when the breakup switch is open (Chapter 4).

5.3 Future research direction

1. **ASK-demodulator for low voltage system applications:** Conventional ASK demodulators typically consist of cascaded stages, including a passive rectifier followed by an envelope detector. However, the passive rectifier introduces a diode voltage drop (∼0.7 V) on the AC input signal. For low-voltage system applications with a supply voltage of approximately 1 V, such a voltage drop can impact sensitivity during envelope extraction when the modulation index is high or affect the common-mode DC voltage level for the subsequent comparator stage. Given the increasing adoption of active rectifiers in low-voltage applications, it is beneficial to achieve envelope extraction by utilizing the comparison result from the active rectifier. This concept is illustrated in Fig. 5.1(a) [15], where the internal node voltage of the comparator, V_X, is reused to control the conduction state of SW_1. When the voltage amplitudes of V_{AC1} and V_{AC2} fall below the sum of the threshold voltages of M_1 and M_2, SW_1 switches off, allowing the bias current (I_1) to charge the capacitor (C_1). The accumulated voltage on C_1 then passes through a level shifter to trigger a transition in the data signal. However, this simple structure has notable constraints: it is highly sensitive to PVT variations, requires a significantly long duration for the AC signal to remain in its 'low' state, and demands a high modulation index, which degrades the received power level. An innovative structure capable of achieving a modulation index as low as 0.1% is presented in [20]. This design employs low-noise amplification stages to facilitate a low modulation index. The 13.56 MHz modulation signal is AC-coupled to the wireless data transfer (WDT) receiver. A shifter limiter amplifies the small difference between the carrier and data with different conversion gains, enabling the amplified voltage difference to be further processed by subsequent stages, including a rectifier, a variable gain amplifier, and a low-pass filter, for data recovery. The primary limitation of this design is that the shifter limiter has restricted bandwidth, preventing it from achieving high data-rate communication. The maximum reported data rate for this structure is 150 kb/s, which is insufficient to support ASK-PPM modulation with a short pulse duration of 210 ns (equivalent to approximately 5 Mb/s). Additionally, the reported rectifier efficiency in ASK downlink mode is limited

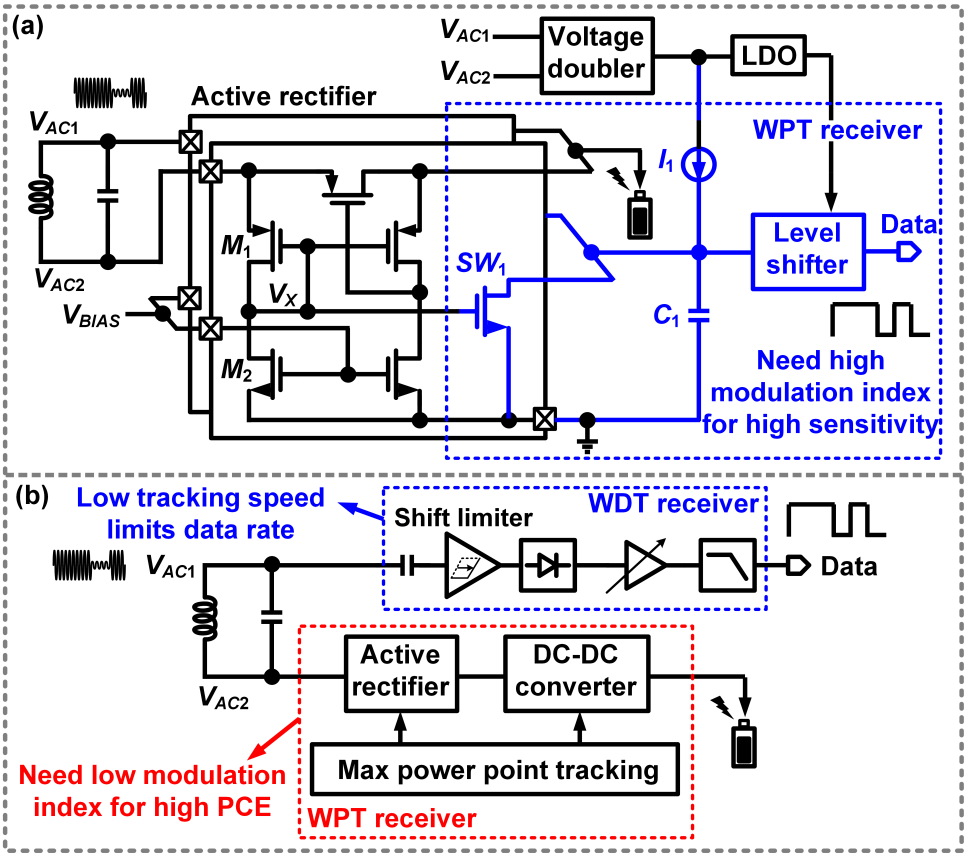


Figure 5.1: Novel ASK data recovery circuit design topologies of (a) Envelope extraction by reusing the comparator output signals in the active rectifier circuit [15], and (b) Shift-limiter based envelope extraction by amplifying the carrier and data signal with different conversion gains [20].

to 75.4%. This efficiency can be further improved by adopting the more power-efficient ASK-PPM modulation scheme. However, specific trade-offs between signal sensitivity, bandwidth requirements, and overall power efficiency must be carefully considered.

2. **Other dual-output regulating rectifier structures:** The regulating rectifier continues to attract significant research interest due to its unique ability to achieve rectification and regulation simultaneously within a single stage. This feature makes it highly suitable for integration into modern implantable systems as a high-efficiency power solution. Typi-

cally, voltage regulation in regulating rectifiers is achieved by controlling the switch-on time of power switch signals, with the control metric based on an analog feedback loop [21–23]. In contrast, this work employs a different approach to voltage regulation using an over-voltage protection (OVP) circuit, as discussed in Chapter 4, due to the use of low-voltage-rated devices in the core rectifier[Q3.2]. All the aforementioned methods suffer from energy loss during the regulation period, where residual power is dissipated as heat on resistive components, as illustrated in Fig. 5.2(a) [8]. In [8], the dual-output voltage generation is achieved through pulse frequency modulation (PFM) controlled power switches $M_1 \sim M_3$. During the first half-cycle ($V_{AC2} > V_{AC1}$), the low-voltage output V_{LV} is charged by V_{AC2}, whereas in the second half-cycle ($V_{AC1} > V_{AC2}$), the high-voltage output V_{HV} is charged by V_{AC1}. A significant portion of power is lost during the regulation phase, particularly when regulating V_{LV}, as the low-voltage output consumes less power in the intended application. This issue has been ad-

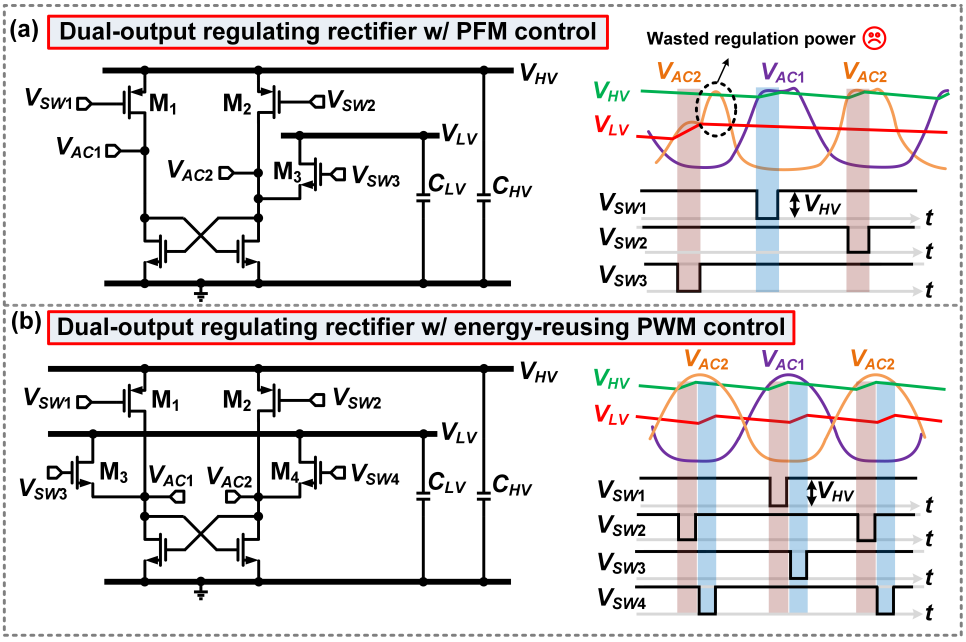


Figure 5.2: Novel dual-output regulating rectifier circuit design topologies, which have the power switch control signals generated by (a) Pulse frequency modulation (PFM) [8], and (b) Pulse modulation modulation (PWM) with regulation power reusing [24].

dressed in [24] using an energy-recycling PWM control structure, as shown in Fig. 5.2(b). Instead of using PFM control, which charges each regulated output infrequently, this structure employs PWM control to charge each regulated output in every half-cycle. As a result, the residual power from regulation is fully reused to charge V_{LV}, achieving a peak power conversion efficiency (PCE) of 92.74% under optimal load conditions (4.5 V V_{HV} with a 200 Ω load and 2.5 V V_{LV} with a 1000 Ω load). However, the main limitation of this design is that the PCE is primarily optimized for V_{HV}, which has higher power consumption than V_{LV}. If the power consumption of the load on V_{HV} is significantly lower than that of V_{LV}, the overall PCE would be much lower. Additionally, the operating frequency in this work is only 6.78 MHz, which permits longer switch-on times but results in higher output ripple and makes it more challenging to reduce the number of passive components. Nevertheless, the concept of residual power reuse is promising and can be further extended to generate additional independent power supplies, such as an analog/digital low-voltage supply for neural recording circuits and an analog high-voltage supply for neural stimulation or light-emitting diode (LED) drivers in optogenetic systems.

3. **In Vivo Validation:** Though new techniques for wireless power transfer [25–29] and data communication [27,30] in implantable system applications have been proposed, these designs have only been verified in ex vivo or in vitro conditions. Few designs have undergone successful verification through a fully blind test [15,17,31]. Fully blind test verification provides more conclusive results compared to other verification methods, as the integrated circuit (IC) and its external components must be completely encapsulated without any access to wires or printed circuit boards (PCBs). This approach best demonstrates the system's functionality and reliability in a tissue environment and holds significant scientific value in validating the real-world applicability of implantable electronic systems.

5.4 Conclusions

This thesis has presented a comprehensive investigation into the design and implementation of a highly efficient and fully integrated wireless implant system for a future artificial retina system. The proposed designs have addressed the limitations of existing solutions in power management, wireless data communication, and integration with the coil link in closed-loop neuromodulation devices. The innovations introduced in this work pave the way for

the development of next-generation IMDs, enabling more effective and reliable powering and communicating for specific application needs.

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Summary

This dissertation presents the development of a highly integrated and energy-efficient electronic system for modern closed-loop neural implants, addressing critical challenges in power management, communication, and integration inherent in such applications.

Chapter 1: Introduction

Chapter 1 establishes the critical need for robust wireless power transfer (WPT) and high-bandwidth bidirectional data telemetry in next-generation closed-loop neural implants. Recognizing the increasing functionality of these systems, which demand greater power delivery and high data rates, the dissertation selected near-field inductive coupling as the most suitable wireless link technology for the target retinal implant due to its established efficacy, superior end-to-end efficiency, reduced integration complexity, and operation within safe frequency ranges. The foundational work sets out three primary objectives: (1) co-optimizing the wireless link to maximize efficiency and minimize footprint, (2) developing a compact and reliable bi-directional data communication system, and (3) designing a high-efficiency Power Management Unit (PMU) capable of providing multiple stable voltage rails for neural stimulation and recording.

Chapter 2: Coil Link Design For Wireless Power Transfer And Data Communication

Chapter 2 presents a systematic, guided, and iterative optimization methodology based on the finite element method to maximize link efficiency within the constraints of practical operating conditions. The design addresses the crucial concern of potential efficiency degradation and tissue damage caused by locating the target inductive links within an air-tissue environment. This optimization involves detailed analysis based on the operation frequency, the physical dimensions of the links, and the power budgets. The process resulted in a two-coil power link that achieved its maximum Power Transfer Efficiency (PTE) at a given load, with sufficient margins against tissue heating to avoid violating safety regulations. Furthermore, the chapter details the dual-band strategy by employing ASK-PPM (amplitude shift keying with pulse position modulation) on the central power carrier frequency

(40.68 MHz) for the downlink data communication due to its self-synchronization feature and efficiency. Separately, it establishes a high-speed, low-power impulse radio ultra-wideband (IR-UWB) link at a Giga band center frequency (4 GHz) for the necessary high-data-rate uplink communication. This separate antenna design achieved a link gain (−28.89 dB) that is sufficient to cover the loss through the media with minimal misalignment effect under the laboratory test conditions.

Chapter 3: A 40.68-MHz Wireless Implant System With Bi-directional Data Communication

Chapter 3 validates the chip-level integration of the power management and telemetry blocks in a 1.15 mm^2 total area, minimizing the use of external components. The PMU utilized a full-bridge passive rectifier and introduced an innovative dual-loop, capacitor-less LDO regulator structure with a source degeneration bypass capacitor in the flipped voltage follower buffer stage. This enhanced the loop bandwidth, enabling fast-transient regulation while minimizing area. Besides the voltage regulation, this design successfully performs clock extraction and data recovery for the downlink data communication, therefore validating the concept of self-synchronization and flexibility of modulation index using the proposed ASK-PPM communication in the selected implant application. Moreover, an improved edge-combining IR-UWB transmitter architecture featuring a dual-edge pulse generator was proposed for the uplink, which overcomes the long propagation delay bottleneck. It achieves a measured energy efficiency of 16.37 pJ/bit at the selected center carrier frequency(3.68 GHz) when performing the uplink data communication with 20 Mbps. The choice of this high-frequency band ensures that the uplink data transmission has minimal interference with the 40.68 MHz power and downlink carrier frequency.

Chapter 4: A 40.68-MHz Fully-Integrated Voltage/Current-Mode Dual-Output PMU for Wireless Neural Implants

Chapter 4 addresses the new challenge in modern closed-loop neuromodulation integrated chip designs where the low-voltage supply (V_{LV}) becomes the dominant supply voltage for high-power recording and processing circuits. To tackle this, an innovative power management system (PMU) with dual Voltage-Mode (VM)/Current-Mode (CM) operation and full-wave rectification (FWR) was proposed. This design achieves both significant area reduction (by integrating all resonant and filtering capacitors on-chip) and competitive efficiency, thus overcoming the major

limitation of conventional dual-output PMU designs. The system prioritizes the VM operation with an active FWR to efficiently regulate V_{LV} to 1 V, achieving a peak power conversion efficiency (PCE) of 85.87%. It transitions to the CM only to boost voltage for the high-voltage V_{HV} to 2 V output, minimizing energy penalties on the V_{LV} rail. To address the voltage drop problem on the resonance tank of the proposed FWR structure, a novel anti-parallel capacitor pair was proposed, eliminating negative voltage swing issue in conventional CM structures and improving VM PCE by 5.7%. This architecture achieved a peak end-to-end efficiency of 17.32% for the VM and 14.94% for the dual VM/CM operation under the ex-vivo test conditions..

Chapter 5: Conclusion and Outlook

Chapter 5 summarizes the key contributions, highlighting that the work successfully demonstrated a systematic, high-efficiency, and highly integrated wireless solution for the VLV-heavy, dual-output, and high-data-rate requirements of future artificial retina systems. Key achievements include the optimized multi-band wireless link, the energy-efficient bidirectional telemetry, and the dual VM/CM PMU architecture. The research confirmed that parasitic capacitance is the primary performance bottleneck in high-speed and high-frequency analog IC design. The chapter concludes by outlining compelling future research, such as developing sampling-based ASK demodulators for ultra-low-voltage operation and conducting in-vivo validation to confirm real-world clinical viability.

Samenvatting

Dit proefschrift presenteert de ontwikkeling van een sterk geïntegreerd en energie-efficiënt elektronisch systeem voor moderne gesloten-lus neurale implantaten, waarbij kritieke uitdagingen op het gebied van stroombeheer, communicatie en integratie, die inherent zijn aan dergelijke toepassingen, worden aangepakt.

Hoofdstuk 1: Introductie

Hoofdstuk 1 stelt de cruciale behoefte vast aan robuuste draadloze energieoverdracht (WPT) en bidirectionele datatelemetrie met hoge bandbreedte in de volgende generatie gesloten-lus neurale implantaten. Erkenning gevend aan de toenemende functionaliteit van deze systemen, die een grotere energielevering en hoge datasnelheden vereisen, selecteerde het proefschrift nabijveld inductieve koppeling als de meest geschikte draadloze verbindingstechnologie voor het beoogde retinale implantaat. Dit is te danken aan de bewezen effectiviteit, superieure end-to-end efficiëntie, verminderde integratiecomplexiteit en werking binnen veilige frequentiebereiken. Het fundamentele werk stelt drie primaire doelstellingen vast: (1) het mede-optimaliseren van de draadloze verbinding om de efficiëntie te maximaliseren en de voetafdruk te minimaliseren, (2) het ontwikkelen van een compact en betrouwbaar bidirectioneel datacommunicatiesysteem, en (3) het ontwerpen van een zeer efficiënte Power Management Unit (PMU) die in staat is om meerdere stabiele spanningsrails te leveren voor neurale stimulatie en registratie.

Hoofdstuk 2: Ontwerp van de Spoelverbinding voor Draadloze Energieoverdracht en Datacommunicatie

Hoofdstuk 2 presenteert een systematische, geleide en iteratieve optimalisatiemethodologie, gebaseerd op de eindige-elementenmethode (FEM), om de verbindingsefficiëntie te maximaliseren binnen de beperkingen van praktische operationele omstandigheden. Het ontwerp richt zich op de cruciale zorg over potentiële efficiëntiedegradatie en weefselschade veroorzaakt door de beoogde inductieve verbindingen in een lucht-weefselomgeving. Deze optimalisatie omvat een gedetailleerde analyse op basis van de werkfrequentie, de fysieke afmetingen van de verbindingen, en de vermogensbudgetten. Het proces resulteerde in een tweespoels-stroomverbinding die zijn maximale

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Power Transfer Efficiency (PTE) bereikte bij een gegeven belasting, met voldoende marges tegen weefselverwarming om de veiligheidsvoorschriften niet te schenden. Verder beschrijft het hoofdstuk de dubbele-bandstrategie door ASK-PPM (Amplitude Shift Keying met Pulse Position Modulation) toe te passen op de centrale draaggolffrequentie van de stroomvoorziening (40.68 MHz) voor de downlink datacommunicatie vanwege de zelfsynchronisatiefunctie en efficiëntie. Afzonderlijk wordt een snelle, energiezuinige Impulse Radio Ultra-Wideband (IR-UWB) verbinding op een Gigaband-middenfrequentie (4 GHz) tot stand gebracht voor de noodzakelijke hoge datasnelheid uplink communicatie. Dit afzonderlijke antenneontwerp behaalde een verbindingsversterking (−28.89 dB) die voldoende is om het verlies door het medium op te vangen met minimale effecten van uitlijnfouten onder laboratoriumtestomstandigheden.

Hoofdstuk 3: Een 40.68-MHz Draadloos Implantaatsysteem Met Bidirectionele Datacommunicatie

Hoofdstuk 3 valideert de chip-niveau integratie van de stroombeheer- en telemetrieblokken in een totale oppervlakte van 1.15 mm^2, waarbij het gebruik van externe componenten wordt geminimaliseerd. De PMU maakt gebruik van een passieve volbrugsgelijkrichter en introduceert een innovatieve dual-loop, condensatorloze LDO-regulatorstructuur met een source degeneration bypass-condensator in de flipped voltage follower bufferfase. Dit verbeterde de lusbandbreedte, waardoor snelle transiënte regulatie mogelijk werd, terwijl het oppervlak minimaal bleef. Naast de spanningsregeling voert dit ontwerp met succes klokextractie en dataherstel uit voor de downlink datacommunicatie, waarmee het concept van zelfsynchronisatie en flexibiliteit van de modulatie-index wordt gevalideerd met behulp van de voorgestelde ASK-PPM-communicatie in de geselecteerde implantaattoepassing. Bovendien werd een verbeterde edge-combining IR-UWB-zenderarchitectuur met een dual-edge pulsgenerator voorgesteld voor de uplink, die de lange voortplantingsvertragingsoverlast overwint. Het behaalt een gemeten energie-efficiëntie van 16.37 pJ/bit bij de geselecteerde middenfrequentie (3.68 GHz) bij het uitvoeren van de uplink datacommunicatie met 20 Mbps. De keuze voor deze hoogfrequente band zorgt ervoor dat de uplink datatransmissie minimale interferentie heeft met de 40.68 MHz stroom- en downlink draaggolffrequentie.

Hoofdstuk 4: Een 40.68-MHz Volledig Geïntegreerde Voltage-/Stroommodus Dual-Output PMU voor Draadloze Neurale Implantaten

Hoofdstuk 4 behandelt de nieuwe uitdaging in moderne gesloten-lus neurale geïntegreerde chipontwerpen, waarbij de laagspanningsvoeding (V_{LV}) de dominante voedingsspanning wordt voor registratie- en verwerkingscircuits met een hoog vermogen. Om dit aan te pakken, werd een innovatief Power Management System (PMU) met dubbele Voltage-Mode (VM)/Current-Mode (CM) werking en Full-Wave Rectification (FWR) voorgesteld. Dit ontwerp bereikt zowel een aanzienlijke oppervlaktevermindering (door alle resonante en filtercondensatoren op de chip te integreren) als een concurrerende efficiëntie, waarmee de belangrijkste beperking van conventionele dual-output PMU-ontwerpen wordt overwonnen. Het systeem geeft prioriteit aan de VM-werking met een actieve FWR om V_{LV} efficiënt te reguleren tot 1 V, met een piek Power Conversion Efficiency (PCE) van 85.87%. Het schakelt alleen over naar de CM om de spanning te verhogen voor de hoogspanningsuitgang V_{HV} tot 2 V, waardoor energieverliezen op de V_{LV}-rail worden geminimaliseerd. Om het spanningsvalprobleem op de resonantietank van de voorgestelde FWR-structuur aan te pakken, werd een nieuw anti-parallel condensatorpaar voorgesteld, dat het probleem van de negatieve spanningszwaai in conventionele CM-structuren elimineert en de VM PCE met 5.7% verbetert. Deze architectuur behaalde een piek end-to-end efficiëntie van 17.32% voor de VM en 14.94% voor de duale VM/CM-werking onder ex-vivo testomstandigheden.

Hoofdstuk 5: Conclusie en Vooruitzichten

Hoofdstuk 5 vat de belangrijkste bijdragen samen en benadrukt dat het werk met succes een systematische, zeer efficiënte en sterk geïntegreerde draadloze oplossing heeft gedemonstreerd voor de VLV-zware, dual-output en hoge datasnelheidvereisten van toekomstige kunstmatige retinasystemen. De belangrijkste prestaties zijn onder meer de geoptimaliseerde multi-band draadloze verbinding, de energie-efficiënte bidirectionele telemetrie en de duale VM/CM PMU-architectuur. Het onderzoek bevestigde dat parasitaire capaciteit het primaire prestatieknelpunt is in snelle en hoogfrequente analoge IC-ontwerpen. Het hoofdstuk sluit af met een schets van veelbelovend toekomstig onderzoek, zoals het ontwikkelen van sampling-gebaseerde ASK-demodulatoren voor ultralage spanning en het uitvoeren van in-vivo validatie om de klinische haalbaarheid in de praktijk te bevestigen.

Acknowledgments

As the coldest season in the Netherlands draws near, and the wind whispers outside my window, I sit at my warm and familiar desk to write this final chapter of acknowledgment—the closing page of my dissertation. The completion of this PhD journey, a period marked by profound learning, growth, and perseverance, would not have been possible without the steadfast support and guidance of many individuals. I extend my deepest gratitude to all who have contributed to this work and who have walked alongside me throughout this long and meaningful journey.

First and foremost, I would like to express my deepest gratitude to my supervisory team—my promoter, Prof. Wouter Serdijn, and my daily supervisor, Dr. Dante Muratore. Without their dedicated mentorship and support, this work would never have been able to reach the depth of research. I sincerely thank both of them for the many forms of support I have received: insightful advice on research directions, guidance throughout my studies, numerous rounds of constructive feedback on my scientific writing, warm encouragement during moments of rejection, heartfelt congratulations upon successes, and so much more. Wouter is a true mentor whom I deeply admire and respect. He is not only visionary in leading state-of-the-art research, but also committed to build a supportive environment within our team. Dante has supervised me extensively throughout the artificial retina project. His constant stream of ideas, meticulous attention to detail, and thorough reviews have been invaluable.

Second, I would like to express my sincere gratitude to all the members of my doctoral committee—Prof. Frans Widdershoven, Prof. Edoardo Bonizzoni, Prof. Kea-Tiong (Samuel) Tang, Dr. Sijun Du, and Prof. Paddy French—for kindly accepting to serve on my thesis defense committee and for providing valuable comments that helped further refine this dissertation. I am truly grateful to have my work reviewed by all of you, distinguished experts from diverse fields.

During this wonderful journey, I have had the opportunity to work with some of the most experienced and knowledgeable researchers in the world. I would like to thank Dante once again for including me in the meetings of the Stanford Artificial Retina Project, and all the team members. Special thanks go to Dr. Pyungwoo Yeon, who provided me with the prototype designs, which ulti-

mately led to Chapters 2 and 3. He also contributed to the writing of Chapter 4. I sincerely appreciate his contributions and wish him all the best in his career.

Next, I feel deeply grateful to all my colleagues and friends at TU Delft. I would like to thank our supervisory team—Leon, Tiago, Vasiliki, Achilleas, Bert, Yao-Hong—and our support staff: Kellen, Esther, Minke, Marion, Rosario, Chris, Brian, Tarique, Zu-Yao, Ron, Lukas, Antoon, Atef, Juan, and Marco. I am also thankful to our post-docs and alumni: Christos, Xiaohua, Yuyang, Amin, Hassan, Gandhika, Peng, Suman, Alireza, and Murat. My gratitude further extends to our PhD candidates and alumni: Bakr, Kimia, Arash, Masoumeh, Maria, Chenyan, Samuel, Diogo, Rui, Konstantina, Beatriz, Liwen, Rabia, Johan, Raphael, Mustafeez, Tao, Ignasi, Stefania, Andrada, Hoda, Nandor, Douwe, Tianqi, Wenyu, Yunzhe, Xiao, Mohammad, Amir, Floris, Imad, as well as Nasim, Ronaldo, Samprajani, Shaogang, Francesc, Xinling, and Zhong. Many of my MSc students friends and alumni, and my dear officemates('academic support')—Niloufar, Eshani, and Limitha, have also been an important part of this journey. I would like to especially thank Ronald and Marvin for allowing me to co-supervise them during their Master programmes. To my friends who enriched my campus life—Yingwen, Pu-chen, Chunyu, and Yukun—and to my former roommates, Congbiao, Jingxuan, Shubo, and Wenyi, I offer my heartfelt thanks. And to many others not mentioned here.

I would also like to express my gratitude to my former colleagues at Montage Technology—Yanhong, Qiuyan, Wenjuan, Peng, Jian, Juan, Yaomin, and Pengzhan—and to my friends at NTHU: Yu-Po, Chien-Hua, and Yan-Peng. All of them generously offered helpful suggestions during my research, and I truly appreciate their support.

Finally, I owe my deepest gratitude to my family and my girlfriend. To my parents, thank you for your unwavering love, support, and encouragement, which have always been the foundation of my life. To my partner, Jiaojiao, thank you for standing by my side through every step of this journey. I hope that together we can overcome many challenges and celebrate many joys in the years ahead.

I am profoundly grateful to have received so much kindness, patience, and professional guidance. This dissertation is dedicated to all of you.

December 2025

Delft, The Netherlands

Curriculum Vitæ



Yihan Ouyang was born in China in 1992. He received the M.Sc. degree in Electrical Engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2018. He then joined Montage Technology Co., Ltd., where he worked as an analog IC designer for DDR5 memory buffers.

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He is the recipient of Best Master's Thesis Award in Application Field in 8th IEEE Tainan Section, the 2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) Best Paper award. He served as a reviewer for IEEE International Symposium on Circuits and Systems (ISCAS), IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), and IEEE Transactions on Circuits and Systems Part II: Express Briefs (TCAS-II).

List of Publications

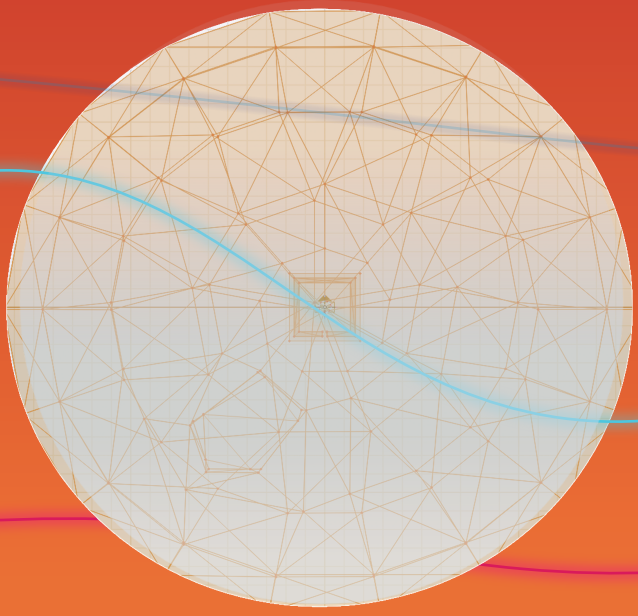
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1. R. Wijermars, **Y.-H. Ou-Yang**, S. Du, and D. G. Muratore. “A 40.68-MHz, 200-ns-Settling Active Rectifier for mm-Sized Implants”. In: *IEEE Solid-State Circuits Letters* Volume:8 (2025), pp. 305–308. doi: 10.1109/LSSC.2025.3611484
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