Amplifier design for a piezoelectric transducer

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TU Delft

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by

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Abstract

This thesis is part of a larger graduation project aimed at achieving precise control over the displacement of an ultrasonic transducer in order to obtain a flat displacement response in the frequency domain. This thesis specifically presents a detailed report on selecting and driving a piezoelectric transducer around its resonance frequency

By means of laser interferometry, the position of the surface of the transducer is measured. Based on design requirements, an ultrasonic transducer and an amplifier design are chosen. Using structured electronics design, design considerations such as voltage & current drive capability, noise analysis and the dynamic behaviour are investigated. Frequency compensation is implemented to enhance the stability of the designed system. To conclude, the dynamic behaviour of the design shows instabilities. Applying frequency compensation does not change the behavior of the system. The design is therefore not suitable to be implemented in a real life application and another design should be created. Also a custom made amplifier can be built for this type of application.

Preface

This report is part of our Bachelors graduation project for the studies Electrical Engineering at the faculty of EEMCS at Delft University of Technology.

We would like to express our gratitude to our supervisor Dr.ir. Arjan van Genderen, and our subgroup supervisor Anton Montagne for their guidance and assistance over the course of this bachelors graduation project. Additionally, we would like to express our thanks to Michiel Pertijs for assisting us during this project. Furthermore, we would like to express our gratitude to Warner Venstra for granting us the opportunity to work with your company Quantified Air.

Nathan van Klaveren & Marick Vermeulen
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1

Introduction

Piezoelectric transducers nowadays are widely used in many different fields, such as medical imaging, acoustic engineering and sensor technology. In certain specific research areas, these vibrating objects have to be measured very precisely. There are many different methods to measure the displacement of these transducers very accurately, one of them is laser interferometry.

Figure 1.1: Ultrasonic transducer

The purpose of this project is to control the position of an ultrasonic transducer around its resonance region. Using a laser interferometer the position of this transducer is measured. The end goal is to have designed and created a prototype for a system that can control the position for ultrasonic transducers. In this report, the design and creation of an amplifier is outlined for driving a piezoelectric transducer.

1.1. State-of-the-art analysis

Piezoelectric devices are used in a wide variety of fields, such as medical imaging, acoustic engineering and sensor technology [1] [2]. Transducers consist of different materials [3] with many different displacement properties [1], such as a high precision positioning and a fast frequency response. The piezoelectric effect is the driving factor for all these applications [4]. Applying an electric field to the transducer causes a displacement on the surface of the transducer. The transducer behaves as an actuator. On the other hand, transducers can also act as a sensor.
When driving a piezoelectric transducer, common and usually undesired effects of piezoelectric transducers are their hysteresis and creep effects. When a voltage is applied to these devices the position of the transducer is not proportional to the voltage. The transfer of the transducer shows hysteresis, which is a non-linear effect[5]. Solutions to mitigate this are considered. for instance, one would be able to model it, as done in [6]. However, transducers driven with charge show far fewer hysteresis effects and would be easier to implement. Charge-driven piezoelectric actuators have shown far fewer hysteresis effects than voltage-driven transducers [7][8][9]. Models for a piezoelectric actuator have

been investigated, such as the Butterworth Van Dijke (BVD) model, the modified Van Dijke model, and the easy model [10] [11] [12]. Important to note is that the easy model and the Van Dijke model are interchangeably used and when implemented correctly, they should obtain the same response.[13].

There are two main types of feedback amplfiers; current feedback (CFA) and voltage feedback amplifiers (VFA)[14][15] [16]. The amplifiers have different typologies, and some of their properties are useful for our application. VFA's are the most common type of amplifier, and their inverting input is sensitive to voltage. When negative feedback is applied to a voltage amplifier, it tries to drive the error voltage to zero. A VFA typically has a high input impedance, while a CFA has a low input impedance. A CFA tries to drive the error current to zero. So for a CFA, the inverting input is sensitive to current. It usually has two voltage buffers and a transimpedance stage. Because of the structure of a CFA, the bandwidth and slew rate are usually orders of magnitude higher than voltage feedback amplifiers. CFA's usually have a higher input current and voltage bias than VFA's.

1.2. Report structure

Firstly, this report will give an overview of the project and its associated Programme of Requirements (PoR) for the complete system in chapter 2. In chapter 3 the programme of requirements for the ultrasonic transducer is elaborated on and a model of the transducer is created. To drive this transducer well, the amplifier design should have a clear idea of the load it is driving. When also considering the input of the amplifier, one can determine the design considerations for this amplifier. In chapter 4 the requirements for the amplifier are mentioned, as well as the design considerations. One design is chosen and simulated. From the simulated results conclusions and recommendations are given in chapter 5.

2

Programme of Requirements

The purpose of this project is to control an ultrasonic transducer around its resonance frequency, ultimately creating a flat frequency response. The goal is to have designed a prototype for a system that can improve a flat frequency response for ultrasonic transducers. The displacement of the ultrasonic transducer should therefore be independent to frequency within a certain frequency band.

2.1. Requirements of the complete design

This section covers the requirements of the complete design. They are subdivided into functional and performance requirements. Functional requirements being requirements of what the system must do, and performance requirements being attributes that the system must have; they indicate at what quality level the functional requirements must be fulfilled.

2.1.1. Functional requirements

- The system must detect the vibrating motion from the transducer using a high accuracy measurement device.
- The system must control the transducer's displacement.
- The system must be able to determine a minimum of 4 frequencies and based on a controlling system change the behavior of the transducer.
- The time before the complete system is operational must be 120 seconds.

2.1.2. Performance requirements

- The operating center frequency of the signals is on the resonance point of the transducer, in the MHz range.
- The sound power output must be $1W$.
- The bandwidth of the flat band must be $50kHz$.
- The steady state ripple of the frequency band must be less than $0.5dB$.
- The system has to implement a parameter, that will be a baseline for controlling the response of the transducer.
- The bandwidth disturbance rejection must be $10kHz$. This is how fast the system can respond to a parameter change, for example, temperature.
- The design should be realized using commercially available circuitry and equipment.
- The complexity needed to operate the system is minimized.

Another requirement is that the costs of the prototype have to be less than 1500 euros.

In order to measure the position of the transducer, some high accuracy measurement technique is required. For this optical interferometry is used, as it meets the requirements in terms of resolution and bandwidth. The displacement of the surface of the transducer is measured by the laser interferometer,

which has high precision displacement and can measure the position up to high frequencies in the MHz range. An FPGA is used to process the interferometry data. This provides us with the position of the ultrasonic transducer. The laser interferometer needs a control unit to control its laser wavelength.

This project also requires a learning model to control the position response of the ultrasonic transducer. For this multiple techniques can be used, such as a P(ID) controller, or a machine learning model. In this project, a type of model adaptive feedforward control is used. This means that the signals that are sent into the system are compared with the signals that come out of the system. A feed-forward controller is then used to correct our linear model of the system. This model should also be able to take external variables into account, such as temperature. Adding these parameters to the model makes controlling the displacement of the ultrasonic transducer more accurate when non-linear effects affect the behavior of the system.

2.2. Subdivision of tasks

With the general approach on how this problem is tackled, 3 main tasks need to be done for this project to succeed. These tasks ultimately define the different subgroups.

- One group has to design an amplifier to drive the ultrasonic transducer. This group takes care of driving the transducer. Its tasks are to choose an appropriate transducer and to design an amplifier.
- One group has to process the data using an FPGA. Its tasks are to choose a laser interferometer, an ADC, a DAC, and an FPGA and to do the data processing such that the laser interferometer will give the displacement of the transducer.
- One group has to apply a self-learning model to control the ultrasonic transducer. This is implemented with a feed-forward model. Another task is to control the wavelength of the laser light coming from the interferometer.

This report focuses on the choice of the ultrasonic transducer and the design of the amplifier. The next chapters are covering the considerations concerning these subsystems for the project.

3

Piezoelectric transducer

A piezoelectric transducer is a device capable of converting electrical energy to mechanical energy and vice versa using the piezoelectric effect [2]. It is a passive reciprocal transducer, acting both as an actuator and sensor. In this project, the goal is to measure the displacement of the piezo caused by an electrical impulse using laser interferometry. Next, the displacement of this transducer is controlled. The piezoelectric transducer will act as an actuator, i.e. a speaker. A piezoelectric device is usually made out of polymer or ceramic materials, which have different properties, eg. the piezoelectric coefficient, the Q factor, and efficiency. In this project, one has to note that the piezoelectric transducer is the output of the amplifier. Therefore the designer of the amplifier needs to know how the output behaves to accurately create an amplifier for a certain transducer.

In this chapter, the requirements for the transducer and the choice for a certain transducer are outlined, based on the PoR in chapter 2, design choices from other subsystems, and other considerations. Lastly, two measurement techniques are considered for generating an electrical impedance model for this specific transducer that is created based on the Butterworth Van Dijke (BvD) model. The characteristic is modeled and compared to the actual response. This model will then be used to design the amplifier.

3.1. Considerations and limitations for ultrasonic transducer system

Laser interferometer

Because the vibrations of the transducer are measured using light using a laser interferometer, the vibrating material cannot be encapsulated in a structure where the light cannot reach it. This eliminates some of the possible transducer types.

Noise considerations

Since the displacement of the piezo is measured, one would want to see the amount of noise contribution from the amplifier and the input source to the displacement of the piezo. With a model that describes both the mechanical and the electrical properties of the transducer, one would be able to say what this contribution is, by transferring the noise from the input source and the amplifier(s) and transferring them to a noise displacement. A model like the one used in [17] would give a good representation for both the electrical domain and the mechanical domain. Figure 3.1 shows an electro-mechanical model for a piezo.

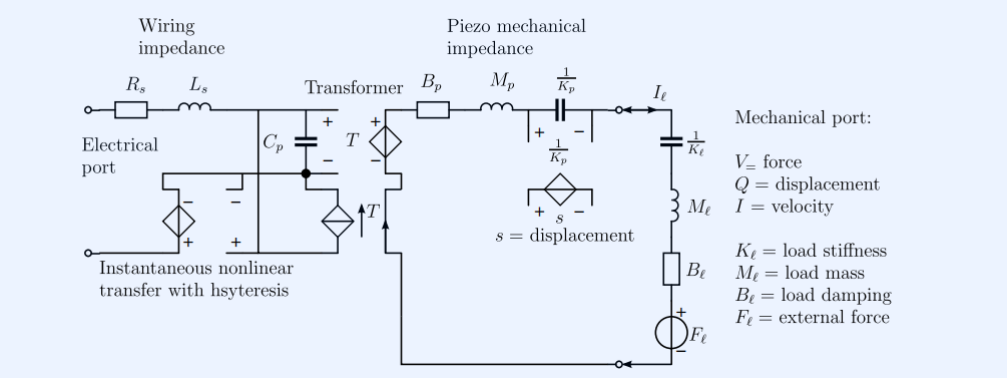


Figure 3.1: Electro mechanical model of a piezo. This model takes into account the electrical components (R_s, L_s, C_p), and the mechanical components (K_l, M_l, B_l, F_l) together with the transmission coefficient from the electrical to the mechanical domain.

However, as seen in figure 3.1, one would have to know the transmission coefficient T in $[N/Q]$, the piezo mass M_l, the load damping B_l and the load stiffness K_l. One other thing to consider is that the effective area of the piezo that is vibrating could be different from the physical area; one could say that a circular piezo may vibrate less at the outer parts, where it is attached to the non-vibrating rest of the material. The transducer that was chosen does not provide us with the specifications to be able to precisely say how much noise is realistically transferred from the electrical domain to the mechanical domain. Unfortunately, there is no precise specification of these coefficients to be able to accurately give a noise quantity. So the relation between the electrical and mechanical domains is not completely known. The relation between Newtons and Coulombs will not be considered. However, in as can be seen in section 3.3, the relation between displacement and voltage (m/V) will be used to estimate the noise performance.

Sound power considerations

One would like to get an estimate of the displacement needed by the piezo based on the sound power required. The acoustic sound power is given by the following equation:

$$P = AI \tag{3.1}$$

where A is the area of the surface of the transducer, and I is the sound intensity. The sound intensity is given by the following equation:

$$I = \frac{\Delta p^2}{2\rho v} \tag{3.2}$$

where Δp is the change in pressure variation, ρ is the density of the material the wave is traveling through, and v is the speed of the observed sound. With measurements on a specific transducer, it is probably possible to measure the pressure variation, but usually, these parameters are not provided when selecting a transducer. A pressure wave is proportional to a displacement wave in terms of frequency. The change in pressure variation is directly proportional to the displacement of the transducer, with an efficiency factor.

So one thing to consider is the coupling between the vibrating material and the air that is displaced when working with acoustic energy transfer. This coupling with air is relatively poor compared to for example water. This coupling factor should be measured for a transducer to ensure that it meets the requirements. As we will see, the Q factor is very large, which means that there is little damping; all the energy stays in the equivalent mass-spring system of the transducer and is not transferred in the air. Also, cavitation should be considered. Cavitation in liquids is the generation of microbubbles when the transducer is generating a pressure gradient. This phenomenon can also occur in the air. With a very high-pressure gradient, one side of the transducer can become locally vacuum. The material would not be able to displace further beyond the point where one side of the vibrating material the gradient becomes (partially) vacuum. This is a strong nonlinear effect and can affect the sound pressure as well. These unknown factors make it too complicated to give an estimation of the displacement needed for this required amount of sound power because the effects of the coupling and the cravitation are unknown. Since there is not an accurate enough conversion from the required sound power to a specific

displacement of the transducer without doing measurements, we consider a paper that estimates the power output from electrical impedance measurements and use their results as a baseline for this use case. In this paper[18], a transducer is used which also has its resonance peak in the MHz range. The measurements from this paper show the measured acoustic power of 2 transducer types on their resonance peaks. The values vary between $10 - 20[mW]$ of sound power for a peak excitation of $1V$. The transducers in this paper show a similar efficiency as the ones that are selected. The paper also shows that there is a linearity between the acoustic pressure and the driving voltage of these transducers.
As will be seen, commercially available amplifiers can deliver up to $20V$ peak excitation. The power relates to the voltage squared, so with the measurements in the paper, this would give an acoustic sound power of $4W$. Even though the transducers in the paper may be different from the one that we select, with this comparison we can compare that the sound power level can be achieved with commercially available circuitry.
As will be seen in section 3.3 the Q factor is 86, which means that the coupling with the air is poor.

Considerations for driving the transducer

Ultrasonic transducers are usually driven between a few volts to thousands of Volts [19] and typical commercially available circuitry can only deliver up to $20V$. The transducer should still be able to deliver enough displacement. Therefore, a transducer with a high Q factor is favored over a transducer with a low Q factor. This means that on its resonance point, the transducer resonates with higher amplitudes[20]. Because the choice for small bandwidth is chosen, one can choose a piezoelectric transducer with a higher Q factor. the Q factor is described by:

$$Q = \frac{f_r}{\Delta f} \tag{3.3}$$

where f_r is the resonance frequency and Δf is the resonance width or the full width at half maximum. For a bandwidth of $50kHz$ and a resonance frequency of $1.6MHz$, one needs a Q factor of 32. Any transducer with a higher Q factor will have a shorter bandwidth than required. There is a trade-off between the bandwidth and the displacement of the piezoelectric transducer. As mentioned before, the displacement is difficult to estimate, if there is certain conversion factors not available. Therefore, the bandwidth requirement should be favored over the displacement requirement. So the Q factor should not exceed 32.

Noise considerations

The laser interferometer has a detection noise level of $1pm/\sqrt{Hz}$. When considering the whole spectrum up to $1.625MHz$, the position noise becomes $1.27[nm]$. However, the spectrum is filtered apart from the frequency range of interest. The frequency band ranges from $1.575MHz$ to $1.625MHz$. When operating over the desired frequency band this gives a noise level of $0.22[nm]$ displacement on the output. For a first estimation of the estimation model from the other subgroup, the dynamic range is set at $20dB$. Also averaging the signal will improve the SNR of the signal if needed. This gives a displacement requirement of $2.2[nm]$. The ultrasonic transducer's displacement needs to vibrate above this threshold.

3.2. Requirements for the ultrasonic transducer

The specifications for the transducer are listed here, based on the requirements of the complete design in chapter 2. This gives us the following requirements:

- The ultrasonic transducer has to have a resonance peak between 1.575 and $1.625MHz$.
- The transducer should have a minimum displacement of $2.2nm$.
- The transducer must have a Q factor of 32.

3.3. Choice for the transducer

Considering the specifications for the piezoelectric transducer in section 3.2, the M165D25 ultrasonic transducer[21] is selected based on the programme of requirements for the transducer:

- It has its resonance frequency at $1.6MHz$.
- The surface of the transducer can be exposed to the laser from the interferometer.

Considering that this is the only transducer with a resonating peak at $1.6MHz$, the Q factor requirement is not met. Its mechanical Q factor is $1000 \pm 20\%$ from the datasheet [3]. However, from [1] the electrical Q factor can be determined by

$$Q = \frac{L_s \omega_s}{R} = 86 \tag{3.4}$$

Even though the bandwidth requirement is not met, the displacement has a higher chance of meeting its requirement, since the higher Q factor allows the transducer to oscillate a lot more, but over a smaller bandwidth. In a different medium other than air, for example, water, the coupling between the transducer and the medium is better. This means that the medium will lower the Q factor, because the medium damps the mass-spring system. As this project is performed in air, the coupling between the surface of the transducer and the air is assumed to be very poor.
From the datasheet of this transducer, one can see the static piezoelectric coefficient of $220pm/V$. With the minimum requirement of the displacement of $2.2nm$, the voltage that should be over the piezo has to be $V_{min} = 10V$. Note that this is a static conversion factor and does not represent the actual behavior of the transducer when oscillating on resonance. Since this is the only specification provided, this is what is used as a reference.

3.4. Butterworth Van Dijke model

To design the amplifier, a model of the transducer is needed. Figure 3.2 shows the electrical equivalent Butterworth van Dijke (BvD) model for a piezoelectric transducer. This model is a basic model for these types of transducers [11] [12]. R_s represents the mechanical losses or the damping, C_s the stiffness, and L_s the mass. One can also consider the coupling of the material with the air, but since the Q factor is so large, and there is no damping, the coupling with the air is very little; almost all the energy stays in the transducer and is not transferred in the air.

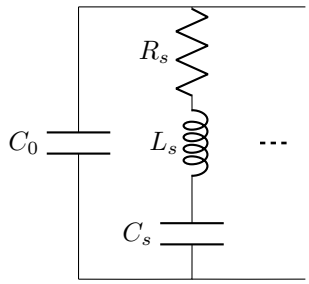


Figure 3.2: Butterworth Van Dijke model for piezoelectric transducer. A capacitor in parallel with a RLC series connection; C_0 is the equivalent capacitance, C_s and L_s model the resonating parts of the piezo, and R_s is taking into account the losses. More RLC parallel connections can be made to account for more resonance peaks

The impedance of C_0 is:

$$Z_{C_0} = \frac{1}{sC_0} \tag{3.5}$$

where $s = j\omega$ and the impedance of the RLC circuit is:

$$Z_{RLC} = \frac{1}{sC_s} + sL_s + R_s \tag{3.6}$$

Since we have an unknown amount of RLC parallel elements, using the equation for a parallel connection, we get:

$$Z_{RLC,eq} = \frac{1}{\sum_{i=1}^{\infty} \frac{1}{Z_{RLC}i}} \tag{3.7}$$

Combining equations 3.5 and 3.7 the total equivalent impedance becomes:

$$Z_{eq} = \frac{Z_{C_0} Z_{RLC,eq}}{Z_{C_0} + Z_{RLC,eq}} = \frac{\frac{1}{sC_0 \sum_{i=1}^{\infty} \frac{1}{Z_{RLC^i}}}}{\frac{1}{sC_0} + \frac{1}{\sum_{i=1}^{\infty} \frac{1}{Z_{RLC^i}}}} \tag{3.8}$$

3.4.1. Deriving the BvD parameters

As seen in section 3.5.1, RLC components will only change the impedance in a certain region. Assuming that the resonance peaks are spaced far enough and that they do not influence each other on their region of operation, one can for each RLC element deduce their parameters to fit the measurement data later. The value for C_0 is usually given for piezoelectric transducers, but they are given. From the measurement, one can later fit the correct value of C_0 to the model. Using equation 3.7 and only accounting for Z_{C_0} and one RLc circuit in parallel, we obtain the following:

$$Z_{eq} = \frac{\frac{1}{sC_0}\dot{(}R_s + sL_s + \frac{1}{sC_s})}{\frac{1}{sC_0} + R_s + sL_s + \frac{1}{sC_s}} \tag{3.9}$$

Since there is one inductor and two capacitors, there are two resonance frequencies [10], a series resonance frequency ω_s and a parallel resonance frequency ω_p:

$$\omega_s = \frac{1}{\sqrt{L_s C_s}} \tag{3.10}$$

$$\omega_p = \frac{1}{\sqrt{L_s \frac{C_s C_0}{C_s + C_0}}} \tag{3.11}$$

At the resonance peak, i.e. at $\omega = \omega_s$, there is C_0 in parallel with R_s. The series resonance Z_s is obtained as:

$$Z_s = \frac{1}{\frac{1}{R_s} + sC_s} \tag{3.12}$$

From this R_s is derived as $R_s = \Re(Z_s)$.
For determining the values of L_s and C_s, rewriting the equations 3.10 and 3.11 gives the following:

$$C_s = C_0(\frac{\omega_p^2}{\omega_s^2} - 1) \tag{3.13}$$

and

$$L_s = \frac{1}{\omega_s^2 C_s} \tag{3.14}$$

This same reasoning can be used for more RLC parallel-connected circuits. One has to change the series resonance and the parallel resonance peaks to obtain the corresponding parameter values.

3.5. Impedance measurement of piezoelectric transducer

There are multiple ways to obtain parameters for the BvD model of the transducer. One method is to use an impedance analyzer. The other method is to do a reflection measurement using a network analyzer.
With a reflection measurement, one would use a network analyzer and perform a frequency sweep on the Device Under Test (DUT) over a frequency range of interest. Then, using a reflection bridge, one would compare the incoming signal with the reflected signal, as you are usually unable to measure the transmitted signal directly. Figure 3.3 shows the reflection measurement of this piezo. From the reflected signal you can determine the frequencies where the resonance and antiresonance of the piezo are located. At series resonance, all the power is transmitted, so the figure shows a dip in the reflection measurement. With parallel resonance, there is no a clear point. At parallel resonance, most of the power is reflected. Based on these resonance frequencies, an estimation could be made about the parameters. This however is not a direct measurement to one-on-one compare the impedance with, but from the data it produces, it is possible to estimate the component values for the BvD model. The impedance analyzer is directly comparable to the BvD model and is therefore used to obtain the parameters. It is a more reliable method.

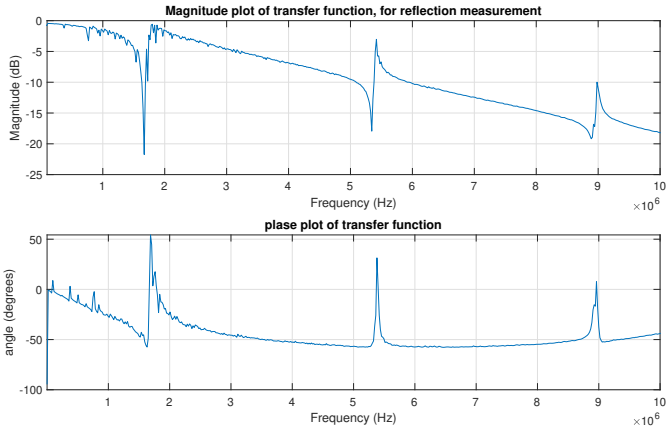


Figure 3.3: Reflection measurement of the piezoelectric transducer. The plots show the magnitude and phase response of the piezoelectric transducer. The magnitude plot shows the reflected magnitude compared to the full power that is injected into the system.

3.5.1. Impedance analyser measurement

The impedance measurement is performed using the Keysight e4990a impedance analyser [22]. The instrument follows an open circuit and a short circuit calibration test to account for, respectively the parasitic capacitances and inductances. Figure 3.4 shows the impedance measurement.

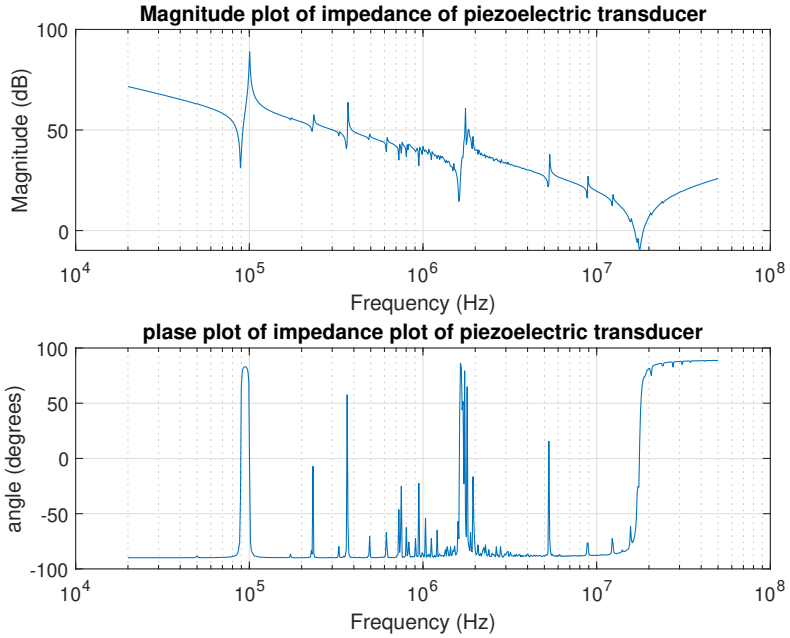


Figure 3.4: Impedance of piezoelectric transducer

From figure 3.4 a few things can be determined.

- There are 4 main resonance peaks, located at $88.91kHz$, $361.7kHz$, $1.608MHz$, and $5.247MHz$. The resonance peaks are the peaks where the phase angle of the frequency characteristic changes from negative to positive.
- At $17.7MHz$ there is an inductive behavior becoming more dominant. This is due to the wires that run towards and from the piezo. When performing this measurement, the wires were twisted to create the least amount of coupling and thereby shifting the point where the inductive behavior dominates to higher frequencies. With a better coupling, i.e. you create a circle/loop such that the

inductance becomes higher, the inductive behavior dominates the spectrum at a lower frequency. This behavior will not be modeled, because the wires are cut off in the final implementation, thus eliminating this behavior.

- In between the second and third resonance peak, so between $445kHz$ and $1.4MHz$ we can see some imperfections from the performance of the piezo, which will not be taken into account.

Since we consider 4 resonance peaks, we will extend the BvD model to have 4 RLC components as well. Figure 3.5 shows the equivalent circuit for the BvD model.

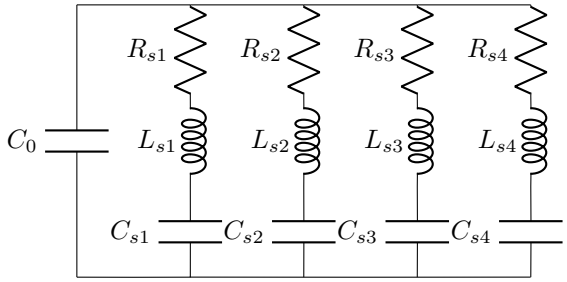


Figure 3.5: BVD model with 4 resonant parallel circuit elements

Table 3.1 shows the parameters deduced from the circuit analysis done in 3.4.1 for each of the parameters.

Table 3.1: Table presenting the component values for the BvD model

Circuit element	Value capacitor (nF)	Value inductor (μH)	Value resistor (R)
C_0	1.35	-	-
RLC_1 at $88.91kHz$	0.37154	8600	17.20
RLC_2 at $361.7kHz$	0.061011	3200	59.83
RLC_3 at $1.608MHz$	0.2611	37.51	4.37
RLC_4 at $5.247MHz$	0.06101	15.08	11.1211

Figure 3.6 shows the impedance and the model.

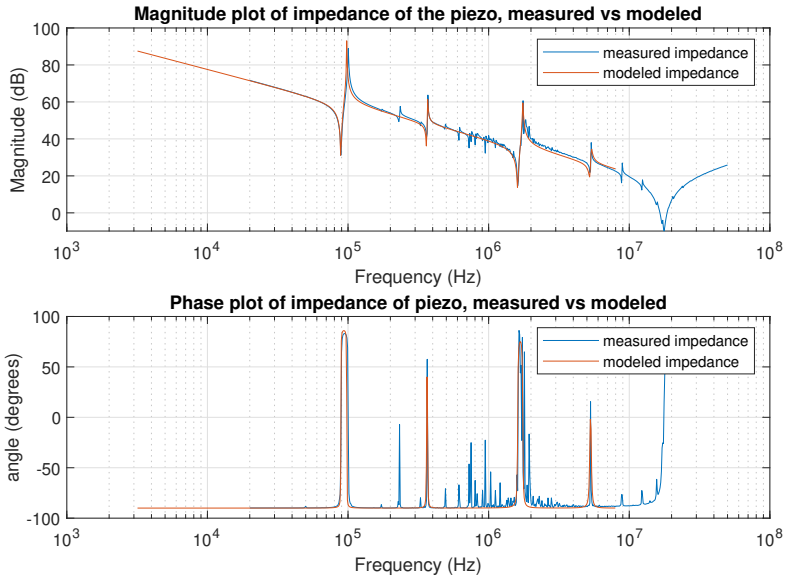


Figure 3.6: Measurement and equivalent model of the impedance of the piezo combined

From this figure, one can see that the model created resembles the actual behavior of the piezoelectric transducer and is thereby a reasonable model to be used for analyzing the amplifier in chapter 4.

4

Amplifier design

To control the piezoelectric transducer described in Chapter 3, an amplifier circuit is needed to drive the transducer. In this chapter, the design of the amplifier will be discussed and important elaborations on this design will be given. By using structured electronics design this chapter aims to achieve the following:

- Deriving specifications based on the design requirements.
- Different possible amplifier typologies will be discussed.
- Performance analysis will be done based on noise, dynamic behavior, and voltage & current drive capability.
- A design will be chosen based on the performance analysis.
- The design will be verified using SliCap[1].
- Frequency compensation will be implemented if needed.

4.1. Considerations and limitations for the amplifier system

Hysteresis in ultrasonic transducers

When making an amplifier an important aspect to consider is the load. The load needs to produce an amplitude response that is as flat as possible and this can be done best by driving the piezo with charge as output quantity of interest.
This is the case because piezos are non-linear[7], which brings parasitic effects to the displacement of the piezo such as hysteresis. An alternative way to drive a piezo is using charge as the output quantity to get a more linear response. This concept has already been studied by[8],[9] and 1.1.

A big difference between this thesis and recent research is the fact that charge driving is usually not done in the resonance mode of the piezo, this is the case because hysteresis is usually much lower near resonance.

This thesis aims to achieve this since the displacement of the piezo will not be in the same range as the maximum displacement near resonance and hysteresis will have a noticeable effect.

Simplifications to the piezo

Even though the impedance model of the piezo shows the correct response, the LRC circuit does not model the behavior correctly. All components are non-linear since they represent behavior in the mechanical domain. However, since the coupling is extremely low, the non-linear components are considered linear.

[1] Symbolic Linear Circuit Analysis Program. A program for setting up and solving design equations for electronic circuits

From digital to analog domain

In this project, the amplifier, transducer, and laser interferometer are all operating in the analog domain. The other operations are happening on an FPGA, microprocessor, and computer. With this implementation, one has to go from the digital to the analog domain. The DAC is used to interface with the FPGA. The DAC should have the right requirements, such as sufficient bit size and update rate for this application. Since requirements on a system level ensure this the DAC can be implemented as a source with a known source impedance, a configuration circuit, and a noise spectrum.

Noise in the system

As seen before in section 3.3, the minimum voltage over the transducer is $10V$. With the specification of the transducer of 220 For designing the amplifier, the output quantity is charge. To convert this minimum voltage to charge, the static capacitance of the piezo is used, The charge is then $Q_{min} = C_{Piezo} \cdot V_{min} = 13.5nC$.
Note that this piezoelectric coefficient has a tolerance of 20% and that this is a factor under a static electric field, and there is no behavior specified on its resonance point, which is the region of interest. These parameters make it difficult to give a reasonable and sensible specification for the displacement noise. It is reasonable to say that the piezoelectric coefficient of $220pm/V$ is not valid on its resonance point; the coefficient will be much higher because of the high Q factor. Since this is a path that is too unknown to be able to accurately say something about the noise, another approach can be taken. One other more reliable approach to thinking about the noise is to say that the noise of the amplifier should not contribute more than the noise of the source. There are some downsides to this approach:

- In case the input source is overly specified, the noise requirements for the amplifier may be impossible or very difficult to achieve.
- We still would not have an idea of how much displacement noise is present on the piezo.

However, when this requirement is met, then the amplifier is not the limiting factor contributing to the noise on the displacement. Therefore the choice was made to let the noise contribution from the amplifier design not be more than the input noise from the DAC, a noise figure of $3dB$.

Amplifier limitations

Typical commercially available amplifiers for these applications can have a maximal swing of approximately $\pm 20V$ and a maximum current of 1A. In this project, this is considered a limit to looking for commercially available circuitry. We can determine the maximum impedance on the frequency range with the measurement data. This is $Z_p = 21.03\Omega$ at $1.575MHz$, with the supply range of $\pm 20V$, we obtain:

$$Q_{out} = \int I\,dt = \frac{V}{sZ_p} = 96.4nC \tag{4.1}$$

where $s = j\omega$. This is the maximum possible output charge.

4.2. Requirements for the amplifier

The following list shows the requirements for the amplifier, based on the PoR, the chosen DAC and transducer, and other considerations in 4.1 and from other subgroups.

- The transducer must be driven with charge.
- To integrate the system in the complete design, a DAC is used as to comply with the FPGA with specifications outlined in 4.3.
- The output displacement of the transducer must be more than $2.2[nm]$.
- The total noise contribution of the amplifier has to be less than the input noise of the DAC. So a noise figure of $3dB$.
- This design is realized using commercially available circuitry.

4.3. From the program of requirements to specifications

To design a suitable amplifier system that drives the piezoelectric transducer (or to design any amplifier system for that matter) it is important to first outline the general specifications needed for the specific application. From the application related PoR specifications of the system can be made, this is done in appendix B, and the results are listed in table 4.1. Since the input and the output ports of the amplifier are defined, we will list their most important specifications in this list and consider other specifications as well.

Table 4.1: Table showing the specifications and their values for this design

specification	value
Input current range: I_s	$0 - 20mA$
Input impedance: Z_i	$12[pF]\|\|200[k\Omega]$
Input source referred noise of the amplifier: $I_{noise,max}$	$50[pA/\sqrt{Hz}]$
Output charge range: Q_o	$\pm 96.4[nC]$
Load impedance, near resonance: Z_l	$4.37[\Omega]\|\|1.35[nF]$
Output maximum offset charge: $Q_{off,max}$	$0.964[nC]$
Total current to charge gain: G_{total}	$\frac{Q_{o,pp}}{I_{s,pp}} = \frac{192.8*10^{-9}}{20*10^{-3}} = 9.64 \cdot 10^{-6}[s]$
Bandwidth: B	$50[kHz]$
Frequency range: f	$1.575 < f < 1.625[MHz]$

Figure 4.1 shows the conversion from different quantities used in this design.

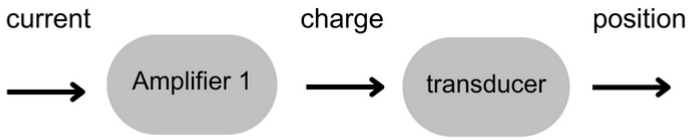


Figure 4.1: Figure showing the conversion from one quantity to the other in the system

4.4. Different amplifier typologies

To drive a piezoelectric transducer multiple circuit typologies can be discussed. An important thing to keep in mind however is the fact that simplicity and performance are the main aspects that need to be considered. To facilitate this two design options will be considered in this thesis. As discussed in 1.1 and 4.1, hysteresis is an important undesired problem. This is the reason for driving the transducer with charge. We will therefore not look at voltage amplification, but instead, look at charge amplifier typologies. The input source is a DAC, with the following specifications[23]:

- This DAC is used for high speed instrumentation and control, having a bit rate of 165 MSPS.
- The current source range is variable and best implemented by choosing a circuit from the application node, the possible current range is from 0 to $2mA$ to 0 to $20mA$. To minimize the gain needed in the amplifier stage, the choice for the highest possible current swing was made.
- It has a current source I_{out} and an inverting current source $\overline{I_{out}}$, where $I_{out} = 20mA$ and $\overline{I_{out}} = 0mA$. when all bits are 1, and vice versa when all bits are 0.
- The DAC has a parallel impedance of $12pF||200k\Omega$.

First of all, the applications are a good starting point, because you would be certain that the application is tested and that the DAC functions as it should in the corresponding circuit topology. Which application is then used? You could choose between using the 2 output sources, or use only one. When using

2 output sources, you would need 2 amplifier stages, which would increase noise levels, could affect stability and you would need additional requirements for the operational amplifiers. Since the designs need to be as simple as possible, the choice was made for only using one output source. Then there is only one application left in the user manual. It is in figure 4.2.

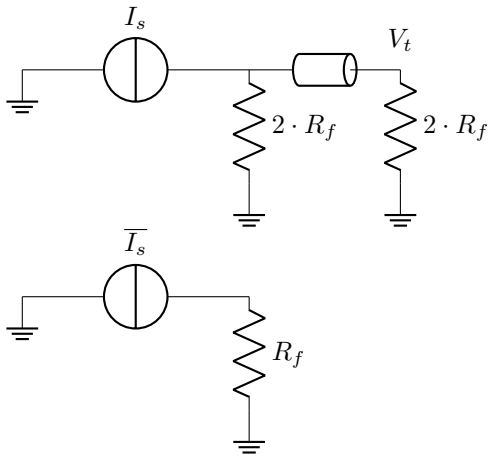


Figure 4.2: Application used in the final design

As only one source is used, $\overline{I_{out}}$ will not be of interest to the design and is thus left out from this point on. These current sources range from $0 - 20mA$, and with this typology, I_{out} is used to connect to the rest of the design. The DAC has an output compliance range between -1 and $1.25V$, a boundary for the voltage swing at V_t, and thus a boundary for R_f. The resistor combination in the figure should not exceed 225Ω. With $R_f = 100\Omega$ at V_t the range is $0 - 1V$. Then there are still 2 typology options for the rest of the circuit, presented in figures 4.3 and 4.4.

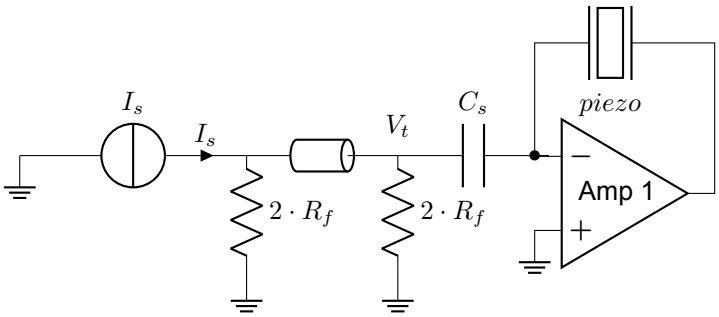


Figure 4.3: Charge amplifier design for driving the piezo. One amplifier stage is used.

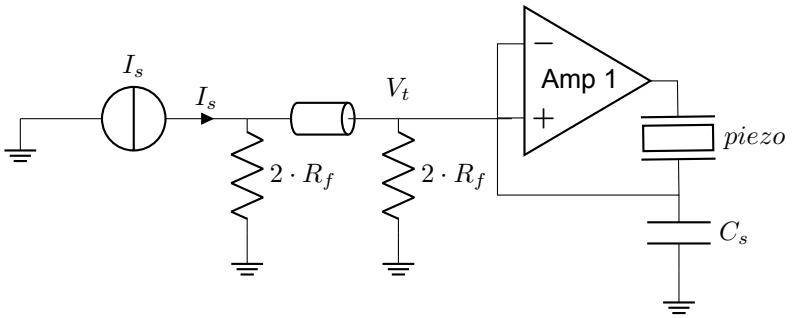


Figure 4.4: Charge amplifier design for driving the piezo with one amplifier stage.

The different typologies have in essence the same mechanism; the voltage V_t is set over a capacitor

C_s and because of the structure of the amplifier, the same charge introduced in C_s is set over the piezoelectric transducer.

4.5. Performance analysis

When looking at these amplifier configurations its functionality and the linearity of the transfer are the most important parts. The linear input quantity (current in this case) will be converted to a linear output quantity (charge in this case). In this design, the input and the output of the amplifier are specified.

In the entire system of figures 4.3 and 4.4, the two parallel resistors form an equivalent resistance of R_f. This is the feedback resistor used to set the gain of the first amplification stage. The current to voltage gain of the first amplification stage is $G_1 = R_f$ The sensing capacitor C_s is the capacitor at which the output voltage V_t of the first amplification is present. Using $q = CV$, the charge over the capacitor can be determined. This is the same charge that is present on the piezo. The input to output voltage gain of the amplifier is determined as $\frac{C_s}{C_p}$, so the voltage over the piezo V_p can be described by $V_p = V_i \cdot (\frac{C_s}{C_p})$, where we assume the piezo to behave as an ordinary capacitor. To convert to charge, we multiply by the capacitance of the piezo, C_p. The total voltage to charge gain of the second amplifier (when the operational amplifiers are perfect and the piezo is strictly capacitive) is $G_2 = C_s$. The total current-to-charge gain of the entire design is shown in equation 4.2.

$$G_{total} = \frac{R_f}{s} C_s \cdot s = R_f C_s \tag{4.2}$$

We will now consider the performance metrics for this amplifier structure. Possible configurations, noise analysis, as well as the dynamic behavior and voltage and current drive capabilities will be discussed.

Output current based on the maximum output charge

As mentioned in the specifications for the amplifier, the maximum output charge is $96.4nC$. The charge relates to the current as:

$$Q = \int I\, dt = \int Asin(2\pi ft)\, dt = -\frac{Acos(2\pi ft)}{2\pi f} + C \tag{4.3}$$

given that the current is a sinusoid with a certain frequency f. We look for the current amplitude A that will give the peak output charge. By rearranging the terms, and $cos(2\pi f_{max}) = 1$, you obtain a maximum current amplitude of $984mA$. This is a requirement for the amplifier.

4.5.1. Noise analysis

Considering the transducer as a capacitive load

In this derivation, we will assume the impedance of the piezoelectric transducer behaves as an ideal capacitor. Table 4.2 indicates all the show stopper values for each component to be designed. From this, a first lower bound on the gain distribution between the voltage divider and the charge driving stage can be made. The lowest possible value for $R_f = 13.256[\Omega]$. Next, the upper bound for the gain in the amplification stage can not be set easily since the source referred noise spectrum of the components after the amplifier does not add to the noise. Next to the the symbolic equation of the source referred noise spectrum can be found in equation 4.4.

$$S_{out} = \frac{1.657 \cdot 10^{-20}}{R_f} + \frac{S_{v_c}}{R_f^2} + \frac{S_{i_c}\left(C_s^2 R_f^2 f^2 + 0.02533\right)}{C_s^2 R_f^2 f^2} \left[\frac{\mathsf{A}^2}{\mathsf{Hz}}\right] \tag{4.4}$$

Considering the piezo with its equivalent BVD model

When not considering the piezo as having only a capacitive behavior, the entire analysis becomes a lot more complicated. However, the important question during this design is not what happens exactly but rather does it even matter. To answer this question the source referred spectral density can be evaluated by doing the analysis on paper or by letting the symbolic noise be calculated by a numerical program such as Python or Matlab. Since this method will always be correct and a comprehensive analysis prone to error is very time-consuming, the symbolic source referred noise spectrum can be

Table 4.2: Table showing the showstopper values based on the first gain distribution for the design. For R_f the limitation of the DAC is added as well (4.4)

component	showstopper[symbolic]	showstopper[numeric]
R_f	$\frac{8kT}{S_{dac}^2}$	$12.8[\Omega]$
S_{i_c}	$\frac{S_{DAC}}{\sqrt{1+\frac{1}{(\omega C_s R_f)^2}}}$	$40.25[\frac{pA}{\sqrt{Hz}}]$
S_{v_c}	$S_{DAC}R_f^2$	$125[\frac{nV}{\sqrt{Hz}}]$

considered the same as modeling the piezo as a purely capacitive load in equation 4.5. This equation is simplified by imposing boundaries on the frequency range.

$$S_{in} = 16\pi^2 C_s^2 R_f T f^2 k + 4\pi^2 C_s^2 S_{vc} f^2 + S_{ic}\left(4\pi^2 C_s^2 R_f^2 f^2 + 1\right)\left[\frac{\mathsf{A}^2}{\mathsf{Hz}}\right] \tag{4.5}$$

Detector Referred noise

It is important to specify the output noise spectral density of the amplifier since it indicates the quality of the charge driver. Equation 4.5 shows the source referred noise spectrum for both models.
where S_{ic} is the current noise power spectrum of the amplifier, S_{vc} is the voltage noise power spectrum of the amplifier, R_f and C_s are the gain factors of the amplifier design.

4.5.2. Dynamic behavior

Digital to analog converter

When connecting the DAC to two load resistances via a coax cable as shown in figure 4.2, it is important to realize that the coax cable is essentially a transmission line and needs to be modeled with its equivalent model. This can be done by making a lumped element network based on the coax cable itself. Before doing this let us first evaluate if the lumped element network is even needed. Lumped element networks are only needed when $\lambda < L_{cable}$ and since $\lambda = \frac{v_{wave}}{f_{max}} = \frac{1}{\sqrt{\epsilon\mu} f_{max}}$ this means $\lambda = 187.5[m]$ which is considerably larger than any coax cable that might be used. Therefore the lumped element network does not need to be considered.

Charge amplifier

To pick the proper amplifier two dynamic characteristics are of great importance, the slew rate (SR) and the gain bandwidth product (GBP). This subsection will calculate the minimum required SR and next to this the minimum required GBP will be derived. Firstly the slew rate is defined by equation 4.6 or in more popular terms the slew rate is defined by the maximum rate of change in the voltage over a capacitor or the current through an inductor. From equation 4.6 the minimum slew rate can be found as $204.2[\frac{V}{\mu s}]$ by assuming $V_{max} = 20[V]$ and the frequency range of interest.

$$SR_{min} = 2\pi V_{max} \cdot f_{max} \tag{4.6}$$

The second part of this subsection finds a way to calculate the minimum required GBP. The GBP is defined by the -3dB frequency of the controller gain and can be found by assuming a first-order low pass characteristic in the controller gain. From this, a first order estimation would suggest that it can be estimated by $G_b = G_{charge} \cdot f_{max}$. This would mean the requirement for G_b would be $59[MHz]$

A more elaborate way to find the minimal gain bandwidth product is by considering the loop gain poles product, as described in [24]. This method can then be used to determine the minimum required gain bandwidth product of the operational amplifier if the zeros of the loop gain are relativity far away from the poles of the loop gain. Due to the piezo and its series and parallel resonance modes this is not the case. Therefore the servo function (a parameter that indicates how much the ideal gain deviates from the actual gain) was determined in SLiCAP and from using the servo bandwidth an equivalent value for the gain bandwidth product of the amplifier can be found. This is the case because the gain should be such that the servo bandwidth is equal to the maximum frequency of interest. By using design equation

4.8 G_B can be found and it turns out that $G_b > 80.7[MHz]$, which is a significant difference compared to the first order estimation.

$$A_{f\infty}(s) \approx \frac{A}{1 + \frac{s \cdot A_0}{2\pi G_b}} \tag{4.7}$$

$$G(s) = A_{f\infty}(s) \cdot \frac{-L(s)}{1 - L(s)} = A_{G_B}(s) \cdot S(s) \tag{4.8}$$

In equation 4.8, $A_{f\infty}(s)$ is the asymptotic gain, $L(s)$ is the loopgain

4.5.3. Driving the digital to analog converter

When driving the digital-to-analog converter it is important to ensure the DAC drives in its proper operating range. This can be done by ensuring the operating voltage at the current source is between $-1 < V_{node_{DAC}} < 1.25[V]$. This can be ensured by limiting the resistor value. This limits the maximum possible voltage swing at the output of the voltage divider that drives the DAC to $V_{i_{max}} = 1.25[V]$. Because working within the compliance range of the DAC is needed, the gain distribution in section 4.5.1 is initially chosen. Later we will see that this gain distribution needs to be adjusted.

4.5.4. Biasing the charge amplifier

Biasing is important for each operational amplifier, since it ensures the amplifier is at the desired operating point. To evaluate a proper biasing solution for the amplifying circuit the desired operating point and the desired output swing of the amplifier needs to be determined. The operating point should be at $(0[A], 0[V])$ and the desired output swing should maximally be $+/-20[V]$.
This implies that from the initial gain distribution, the biasing should ensure a DC offset of $-0.625[V]$. From thinking about the lowest possible biasing error, the smallest noise effects, and considering bandwidth limitations circuit. figure 4.5 shows the full biasing circuit.

Determining design equations for biasing

Since all the theoretical aspects of significant importance to choosing an operational amplifier have been discussed the values of biasing components can be determined. When choosing these values the following design considerations need to be evaluated. (The derivations of these considerations and other less important or related considerations can be found in appendix B).

- Accuracy of biasing: $R_{b1} >> R_{b_2}||R_{b_3}$
- Accuracy of biasing: $|Z_{piezo}| << R_{p_{bias}}$
- Accuracy of biasing of resonance: $R_{b5}C_p = R_{b4}C_s$. These resistors refer to figure 4.6
- Noise: $C_b >> \frac{1}{(2\pi R_{b3} f_{min})}$
- Bandwidth : $|Z_{piezo}| < R_{p_{bias}}$
- Accuracy of biasing on resonance: $(R_{b4}||R_p)C_s = R_{b5}$These resistors refer to figure 4.6

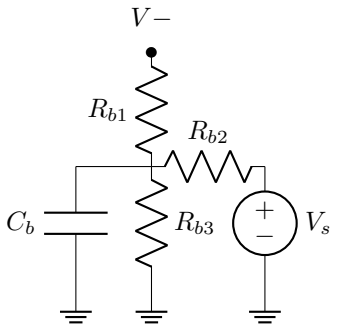


Figure 4.5: Circuit for biasing the inverting input of the amplifier.

4.5.5. Chosen design

With the design of figure 4.3, the inverting node is grounded, causing the common mode capacitance between the different inputs to be negligible. With the typology in figure 4.4, the output voltage of the amplifier is shared with C_s and the piezo, which causes the voltage over the piezo to be a certain fraction of the supply voltage. If the voltage gain of the amplifier is high however, the voltage over the piezo is roughly equal to the output voltage. With the typology in figure 4.3 the full supply range can be set over the piezo. However, in this configuration, the first amplifier is driving a low impedance load, which is undesired, because the majority of the current should go through R_f and not be shared with the low impedance load at V_t. This low impedance load is the path from C_s to the piezo to the output impedance of the load to ground. Also, C_s is floating between the output of one opamp and the inverting input of the other opamp, undesired effects can occur when implementing this structure since the load impedance of the voltage divider changes significantly. Therefore the amplifier structure of Figure 4.4 is selected.

Table 4.3: This table shows considerations for choosing one design over the other. You see the consideration and the checkmark shows for which amplifiers it is applicable.

Consideration for choosing a certain design	Is this desired?	Fig. 4.4	Fig. 4.3
Supply voltage is shared between the piezo and C_s	no	✓	✗
Differential mode capacitance of the amplifier is grounded	yes	✗	✓
source drives a low impedance load	no	✗	✓
C_s is floating	no	✗	✓

4.5.6. Choosing an op amp

By examining the commercially available op amps that satisfy the given requirements, it becomes evident that the selection criteria are exceedingly stringent.

Next to this, the required gain bandwidth product of $80.7[MHz]$ can be decreased by changing the gain distribution between the two stages. The gain in the first stage is set to the maximum gain within the compliance range of the DAC and the feedback resistor becomes $125[\Omega]$. This also benefits the noise since a larger value for R_f implies a lower source referred noise spectrum.

By using the maximum voltage swing of the chosen amplifier (a detailed discussion on the ADA4780 in section 4.6.1) the capacitor of the second amplification stage can be found as. $\frac{V_o}{V_i} = \frac{37}{1.25} = 1 + \frac{C_s}{C_p} \Rightarrow C_s = 38.61[nF]$. From the first order estimation, the required gain bandwidth product for the operational amplifier should now be $47.36[MHz]$. Doing the same estimation as in section 4.5.2 of the required gain bandwidth product with the servo bandwidth required a $G_b = 64.2[MHz]$, which is consistent with the previous determination since the values are only scaled by a certain factor.

By adjusting the gain distribution while maintaining the quality of the design the ADA4870 can be chosen as an operational amplifier to make the design.

- The ADA4870 is a high voltage high current output current feedback amplifier [25]
  - Gain bandwidth product: $52MHz$ large signal, $70MHz$ small signal.
  - input referred voltage noise density of $2.1nV/\sqrt{Hz}$.
  - Positive input current noise density of $4.2pA/\sqrt{Hz}$.
  - Negative input current noise density of $47pA/\sqrt{Hz}$.
  - slew rate: $2500V/\mu s$.
  - Maximum output current: $1A$.

With adjusting the gain distribution, the ADA4870 is suitable for the design that is to be created. Figure 4.6 shows the complete design including biasing.

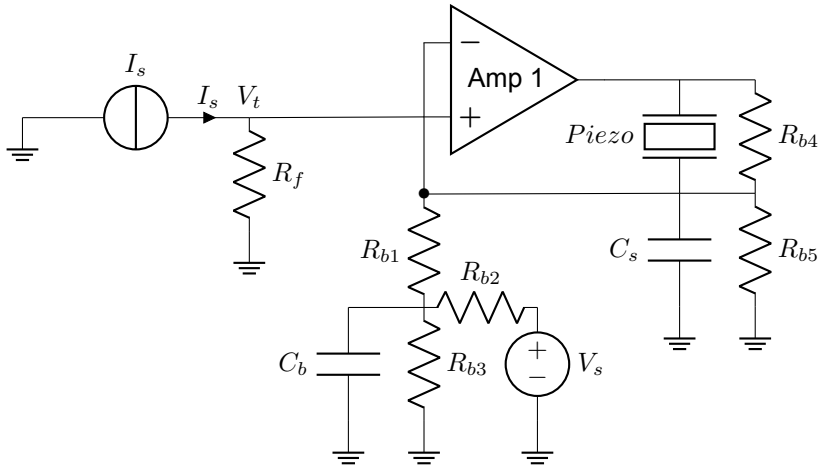


Figure 4.6: Charge amplifier design for driving the piezo with one amplifier stage. In this complete picture resistors R_{b1} until R_{b5} are used to properly bias the circuit and C_b is used to filter high frequency noise coming from the voltage source used for biasing

4.5.7. Determining suitable component values

Based on the showstoppers derived in section 4.2, considerations about the system with respect to the dynamic behavior in section 4.5.2, and the design equations of the biasing solution in section 4.5.4 the component values can be chosen.
Table 4.6 shows the selected component values.

Table 4.4: This table shows the component values of figure 4.6

Component	Value
V_s	$-1.25[V]$
R_f	$125[\Omega]$
R_{b1}	$100[k\Omega]$
R_{b2}	$500[\Omega]$
R_{b3}	$500[\Omega]$
R_{b4}	$4370[\Omega]$
R_{b5}	$152.7[\Omega]$
C_b	$31.8[\mu F]$
C_s	$38.61[nF]$

For the biasing part that is connected to the inverting input of the amplifier, at the inverting input, a voltage of $-0.625V$ is required for the biasing. R_{b1} should be very high, to ensure no voltage drop from the voltage divider created by R_{b2} and R_{b3}. It should also be higher than R_{b5}, because all the current should flow through R_{b5}. Choosing a much higher value for R_{b1} will allow less current to flow through this part of the circuit.

Then for determining the resistor values R_{b2} and R_{b3} and the voltage source V_s, R_{b2} and R_{b3} should be equal to each other, because of the tolerances the resistors may have. By choosing the same 2 resistances with a tolerance of 3%, you have less chance of deviating from the actual resistance, and thereby from the actual voltage divider.
The capacitor C_b behaves together with the resistor R_{b3} as a low-pass filter. This capacitor should behave as a short over the frequency range of interest, so its combined impedance should be low at

$1.6MHz$. The -3dB cutoff frequency of a low pass filter is defined as:

$$f_{-3dB} = \frac{1}{2\pi R_{b3} C_b} \tag{4.9}$$

With a -3dB frequency of $1kHz$, you obtain $C_b = 31.8[\mu F]$

Resistors R_{b4} and R_{b5} direct the bias current from the amplifier to the ground. They also serve as a DC gain for the amplifier. At resonance, the piezo behaves as a capacitor in parallel with a resistor. The error of the biasing component should contribute to 1% of the resistor in the piezo. Since the piezo resistor is 4.37Ω, $R_{b4} = \frac{4.37}{1\%} = 437\Omega$. R_{b5} is then determined by ensuring the same gain as the capacitor ratio, $\frac{C_s}{C_p}$. This results in $R_{b5} = 15.27\Omega$. However, as we will see in section 4.6.1 when modeling the amplifier, it can be seen that the transimpedance gain is very high at low frequencies. The DC loopgain is proportional to the transimpedance gain and inversely proportional R_{b5}. In order to decrease the loopgain at low frequencies, R_{b5} has to become larger. $R_{b5} = 152.7\Omega$. R_{b4} becomes 4370Ω.

4.6. Verification using simulation

4.6.1. Small signal model of operational amplifier

To verify if the chosen operational amplifier meets the specifications a full simulation with its LT-spice macro model can be done. However a macro model does not always capture instabilities caused by the internal functionality of the opamps. Because tiny variations in the system can cause massive differences in the poles and zeros of the model for the piezoelectric transducer and therefore also of the loopgain and the servo function the following paragraph gives small-signal modeling for the opamps used in the amplifying circuit.

To evaluate the functionality of an operational amplifier a large number of factors can be modeled (PSRR, CMRR, slew rate, temperature dependencies, or output impedance to name a few).

However, the functionality of making this small signal model is to ensure the system has a desired frequency response. Therefore the small signal models in this thesis consist of an input impedance, an output impedance, the controller gain and transconductance. These parameters will be tested and then a library file for the model will be made in SLiCAP. The ADA4780 is a current feedback amplifier. Figure 4.7 shows the model for a current feedback amplifier.

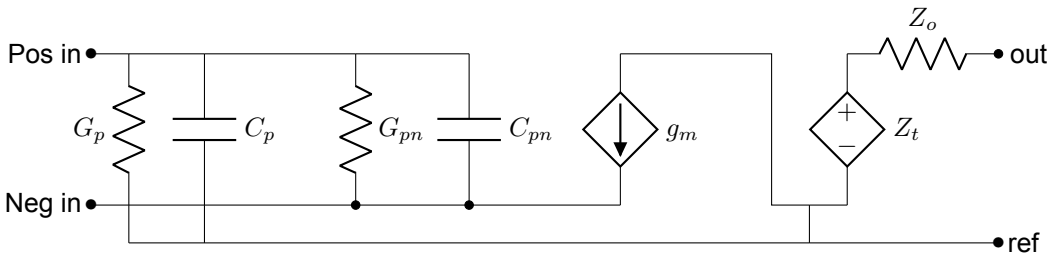


Figure 4.7: Small signal model of a current feedback amplifier for the ADA4780[26]. G_p and C_p are the input resistance and capacitance of the non-inverting input. G_{pn} and C_{pn} are the input conductance and capacitance. g_m is the input transconductance. Z_t is the output transimpedance. And Z_o is the output impedance.

The parameters for this model will be derived from the datasheet specifications and the LTSpice model.

Input impedance

By using the data sheet of the ADA4870 the input impedance of the the operational amplifier can be modeled. These are G_p, C_p, G_{pn}, and C_{pn}. G_p and C_p are listed in the datasheet and can be found in table 4.5. G_{pn} and C_{pn} are not known and are therefore by default 0.

Table 4.5: Table showing the input impedance values of the ADA4870 amplifier

Electrical element	Value
Non-inverting input capacitance C_p	$0.75[pF]$
Non-inverting input conductance G_p	$50[nS]$
Input capacitance C_{pn}	$0[pF]$
Input conductance G_{pn}	$0[nS]$

Transconductance

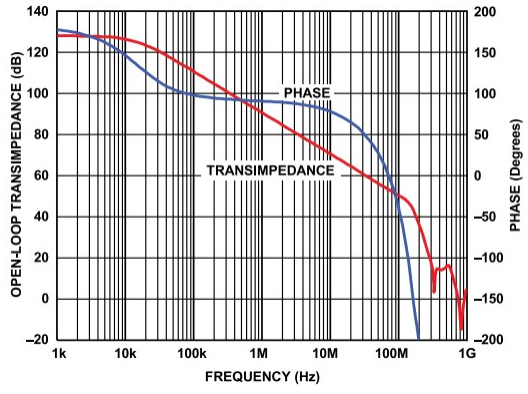
For determining the transconductance g_m, one needs the ratio of the current through and the voltage over the negative terminal of the amplifier in a certain feedback configuration. To estimate this parameter, in the model the non-inverting input is grounded. When the output and the inverting input are connected by a very high resistance, and you would apply $1V$ on the negative input, then the current that you measure is g_m. This current can only come from g_m in the model, since the feedback resistor, and G_p and G_pn are so large, that only a few μA run through it. The error created is small enough that g_m can be assumed to be correct.

Ideally, one would use the actual amplifier and do a test to obtain g_m. The time and effort it takes to do a test over the added accuracy you get would not make it worth to do this measurement in real life. In this case, the LTSpice model was used for estimating g_m by assuming the model is accurate and useful enough for this use case. From the LTSpice simulation, $g_m = 0.080029[S]$.

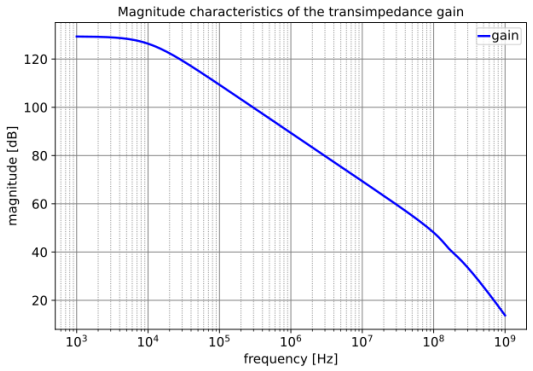
Trans impedance gain

In previous sections, the independent voltage source that acted as the controller of the operational amplifier could just be estimated by giving it a first-order low pass response such as in equation 4.7. In reality, this gain depends on the internal feedback structure (of current mirrors and resistors) in the current feedback amplifier and is therefore complex. The equivalent circuit of the small signal model is based on the measured trans impedance gain illustrated in figure 4.8a. Since this gain is an all-real pole function for the most part and the behavior at high frequencies has no visible phase response, the transimpedance gain will be modeled by only real poles. Equation 4.10 gives the Laplace function for the open loop trans impedance of the small signal model. In this equation $f_1 = 10[kHz]$, $f_2 = 180[MHz]$ and $Z_{t_o} = 30 \cdot 10^6$. Z_{t_o} was determined by measuring the macro model for two different load impedance and a known reference voltage V_i.

$$Z_t(s) \approx Z_{t_o} \frac{1}{(1 + \frac{s}{f1})(1 + \frac{s}{f2})} \tag{4.10}$$



(a) Measured open Open-Loop Trans impedance and Phase vs. Frequency



(b) simulation result of the model of Z_t

Figure 4.8: Comparison of measured and simulated trans impedance

Output impedance

The output impedance Z_o of the amplifier can be found by making an equivalent circuit for the measured output impedance plot data sheet[25]. The equivalent circuit can be found in figure 4.9. Table 4.6 shows the component values used to obtain the correct response. Figure 4.15 compares the measured impedance with the model of the ADA4780.

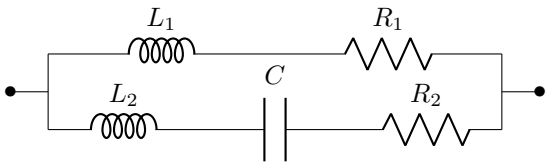
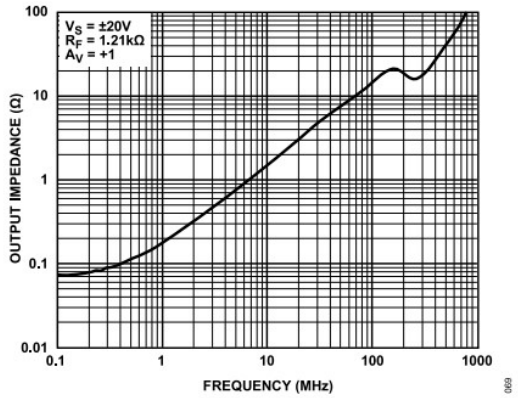


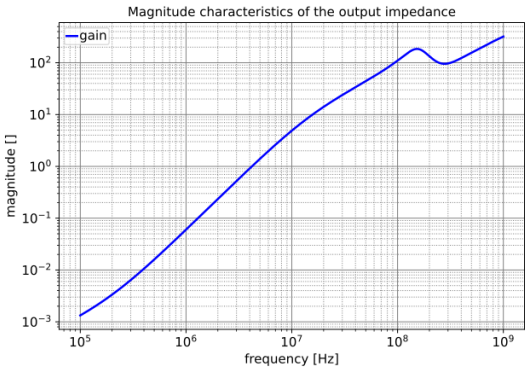
Figure 4.9: Output impedance of ADA4870

Table 4.6: Table showing the output impedance values of the ADA4870 amplifier

Electrical element	Value
C	$10.49pF$
L_1	$55.7nH$
L_2	$38.46nH$
R_1	0.07Ω
R_2	50Ω



(a) Measured closed-loop output impedance of the ADA4870, from the datasheet [25]



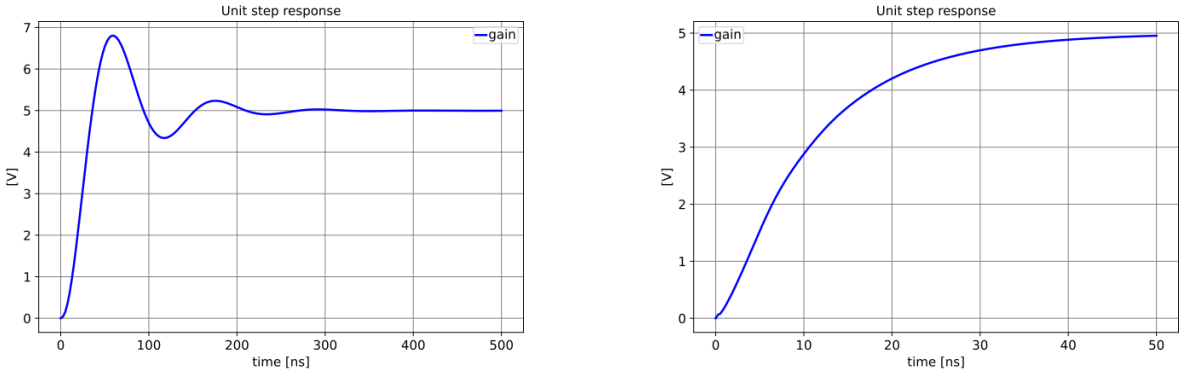
(b) closed loop simulation results of the model of Z_o

Figure 4.10: Comparison of the output impedance measurements using the electrical component values.

Important to note is the fact that these circuits merely represent a mathematical model of what is happening in the operational amplifier and do not represent the physical functionality.

Testing the small signal model

To ensure the small signal model functions as desired the system was tested with two of step responses. A figure of the simulation test circuit can be found in figures 4.11a and 4.11b. The difference between the two circuits is the load that is measured at the output; either resistive or capacitive. An important result of this test is the fact that capacitive load driving makes the model of the amplifier circuit oscillate more.



(a) Tested step response with a capacitive load

(b) tested step response for a resistive load

Figure 4.11: Testing the step response of the small signal model

4.6.2. Biasing of the amplifier

The biasing solution was verified by making use of a SliCap simulation. During this, the biasing values for the bias current and voltage of the ADA4870 were used to ensure the verification would be as accurate as possible. Next to this component tolerances of 3-sigma would be used (this is reasonable in applications such as this where component costs are not really of the essence). From doing the DC analysis a variance of $\sigma^2_{out} = 5.237 \cdot 10^{-9}[A^2]$ was achieved. This indicates the offset current of the output is $I_{ofsett} = 72.367[\mu A]$ which is well below the maximum specification of $1[mA]$.

4.6.3. Noise analysis

By filling in all the component values, an entire noise simulation can be made for the system. Based on this simulation a numerical higher-order source referred noise spectrum becomes evident. From this, the total RMS source referred noise can be calculated and an equivalent white noise spectrum can be determined. The verification result was a source referred noise spectrum $71.2[\frac{pA}{\sqrt{Hz}}]$. This corresponds to a noise figure of $3.85[dB]$ and does not meet the specification as set in 4.1

4.6.4. Dynamic response

Let us consider the gain A_f of a negative feedback amplifier, which is characterized by:

$$A_f = A_{f\infty}\frac{-L(s)}{1-L(s)} \tag{4.11}$$

Where $A_{f\infty}$ is the asymptotic gain, $L(s)$ is the loopgain, and the servo function is given by:

$$S(s) = \frac{-L(s)}{1-L(s)} \tag{4.12}$$

One can see that when the loopgain is high, the servo function reaches 1 (0 dB). When the loopgain is close to 1, the servo function increases beyond 1. When the loopgain is lower than 1, the servo function dips below 1. The servo function gives an indication of the stability of the system. By using the model of the chosen amplifier and using only the important components, the dynamic response of the system can be verified. Important about this is the fact that the amplifying system should be stable and that the amplifier should behave as desired especially around the frequency range of interest. In general, this means that:

- All poles of the loop gain should lie on the left half plane, to ensure stability.
- The servo function should be extremely close to 0 dB for: $f_{res} - \frac{B}{2} < f < f_{res} + \frac{B}{2}$. This means that the asymptotic gain equals the actual gain of the controller, and thus the controller behaves like a nullor.

These two requirements will be evaluated based on the initial amplifier structure and if needed frequency compensation will be used to enhance the performance. Obviously, there are more sophisticated methods to determine stability such as the Routh array or the Nyquist stability criterion.

4.6.5. Initial dynamic response

By making use of the model described in section 4.6.1, figure 4.12 gives the magnitude and phase plot of the entire system without compensation. These plots indicate that the functionality is as desired even though the loopgain at low frequencies is relatively high. When inspecting the gain two unstable poles at $18.5[MHz]$ were found. This means the system is unstable and it requires frequency compensation.

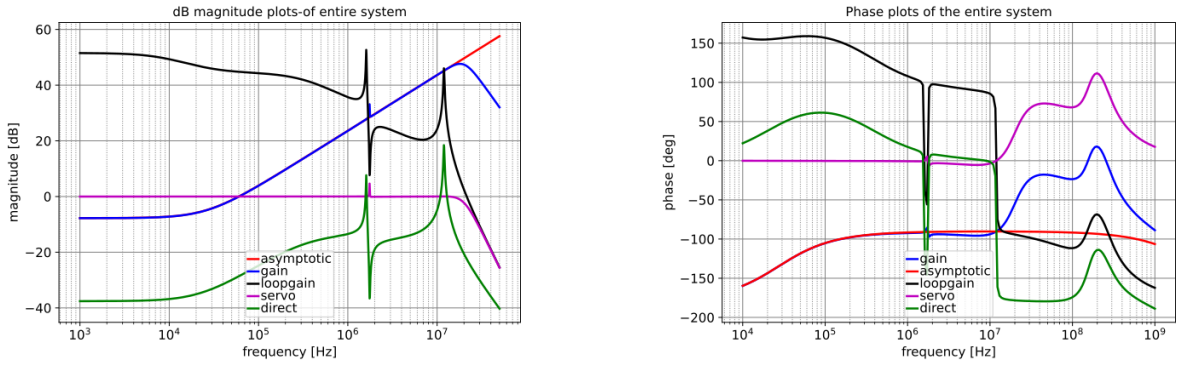


Figure 4.12: Magnitude and phase response for the asymptotic gain, the actual gain, the loopgain, the servo function, and the direct gain for the entire design without frequency compensation.

4.7. Frequency compensation

To ensure system stability and potentially enhance overall system response, frequency compensation can be implemented using techniques such as pole splitting, lead-lag compensation, or phantom zero compensation. Among these methods, phantom zero compensation offers the advantage of positively impacting system stability as it introduces only a pole in the source-to-load transfer function. Notably, phantom zero compensation is theoretically designed to leave the pole placement of other poles unaffected[24]. Therefore, in this case, phantom zero compensation will be employed to stabilize and improve the system.

4.7.1. Phantom zero compensation technique

In the circuit design, there are 3 plausible positions to implement the phantom zero compensation: at the source, at the load, or in the feedback network. Figure 4.13 shows the possible options. This type of compensation can be done by creating a short on the frequency at which the phantom zero needs to be implemented. In the feedback network, there is also a possibility for a complex conjugated phantom zero by implementing an LR circuit in the feedback network. The design equations for the possible phantom zeros are given in equations 4.13 until 4.16. In equation 4.16, the design equation for the LR phantom zero has the Q factor in its equation. The Q factor gives another degree of freedom to the implementation of the complex conjugated poles in the gain of the system.

$$C_{phz} = \frac{1}{2\pi R_f f_{phz}} \tag{4.13}$$

$$R_{phz,1} = \frac{1}{2\pi C_p f_{phz}} \tag{4.14}$$

$$R_{phz,2} = \frac{1}{2\pi C_s f_{phz}} \tag{4.15}$$

$$s^2 + \frac{R_{phz,2}}{L_{phz}}s + \frac{1}{L_{phz}C_s} = 0 \Rightarrow L_{phz} = \frac{1}{4\pi^2 f_{phz}^2 C_s}, R_{phz,2} = \frac{1}{2\pi f_{phz} Q C_s} \tag{4.16}$$

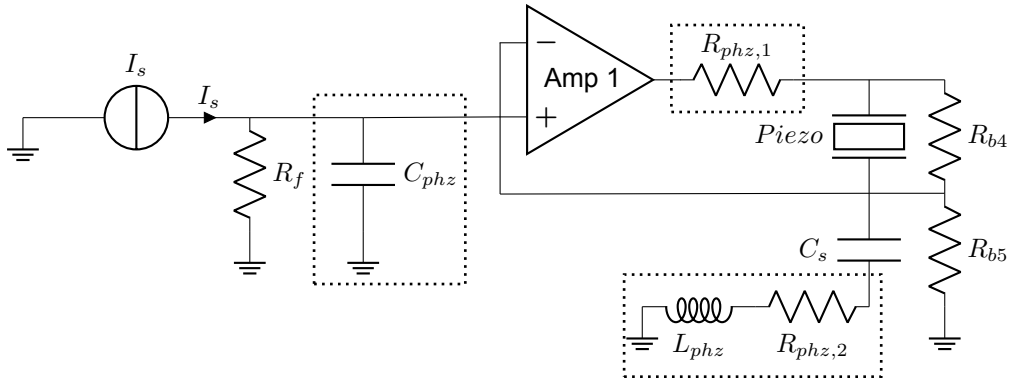


Figure 4.13: Possible phantom zero implementations in the design. C_{phz} at the source. $R_{phz,1}$ at the load. $R_{phz,2}$ and/or L_{phz} in the feedback loop.

4.7.2. Selection of frequency of phantom zero

First order phantom zero

The gain has a lot of poles and zeros. Ideally one would like to investigate the entire system by creating a root locus plot. By analyzing this plot, the proper selection for f_{phz} can be determined. Since placing a phantom zero requires a lot of complex mathematics, here a more straightforward way to select the frequency of the phantom zero is selected: one investigates the effects the zeros and poles of the loopgain have on the poles of the gain. Equation 4.17 and 4.18 show a more mathematical description of this process. The main objective is to make the set of new poles have a negative real part, because then the system becomes stable. Essentially this becomes an optimization problem where the frequency is the only degree of freedom. The implementation of a complex conjugated pole would add an additional degree of freedom. This will be discussed in section 4.7.2.

$$L(s) = \frac{N(s)}{D(s)} \Rightarrow S_{poles} : D(s) - N(s) = 0 \tag{4.17}$$

$$S_{new_{poles}} : -N(s)(1 + \frac{s}{f_{phz}}) + D(s) = 0 \Rightarrow S_{old}(s) - N(s)\frac{s}{2\pi f_{phz}} = 0 \tag{4.18}$$

A way to solve this optimization problem is by using hill climbing however the output of the function is also complex and therefore this would not work. Because of this, an estimation could be made: the servo function will be estimated by only the unstable poles at $f = 9.25[MHz]$ next to this there are no zeros in the loop gain this follows from the definition of the servo function(the derivation can be found in equation 4.19). Using this estimation it is still not possible to get equation 4.18 into root locus form and therefore a different procedure will be implemented. From inspecting the poles in the loop gain it becomes clear that a stable pole at $f_p = 11.9[MHz]$ with a relatively high Q factor($Q = 9.44$) will be shifted to the right half plane. This indicates that phantom zero compensation can still be applied on the pole that will become unstable. This phantom zero will be implemented at a frequency of: $f_{phz} = 5.95[MHz]$ since this should ensure the most movement of the pole. A root locus plot of the implementation of this compensation is depicted in figure 4.14 an important notion when making this locus plot is the fact that the loop gain will not exactly have this behavior since a lot of poles and zeros are not considered.

$$S(s) = \frac{1}{p(s)} = \frac{-L(s)}{1 - L(s)} \Rightarrow L(s) = \frac{-\omega_1\omega_2}{s(s + \omega_1 + \omega_2))} = -\frac{\omega_{pole}^2}{s(s + 2\Re(\omega_p))} \tag{4.19}$$

Complex conjugated phantom zeros

Implementing a complex conjugated phantom zero is also possible and there are two ways to do this: A phantom zero is inserted at approximately the same place as the first-order phantom zero. This means the frequency of the phantom zero does not change and the Q factor mentioned in 4.16 is relatively small, $Q < 10$. A root locus plot of this procedure is shown in figure 4.14.

A second way to implement the phantom zero would be by looking at all possible root loci that can

be created by placing the two poles. Even though this would be the best option, ideally speaking the influence of other poles and zeros would make this option significantly less attractive.

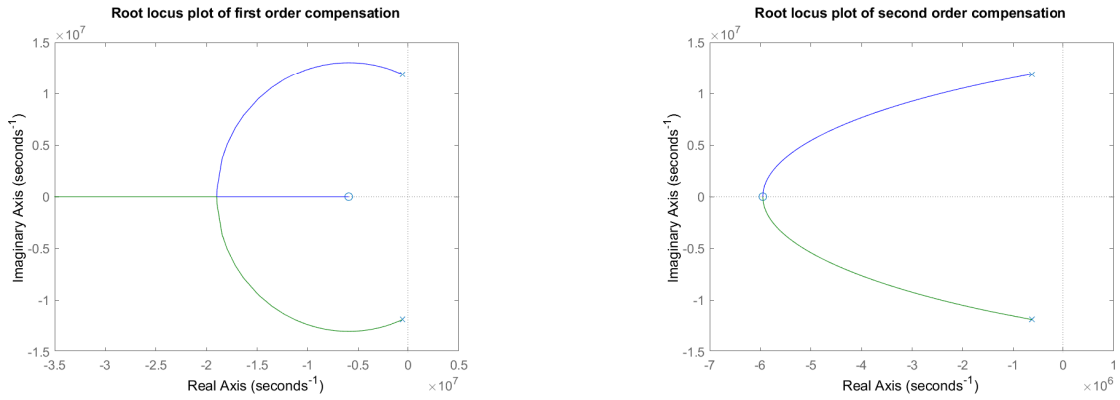


Figure 4.14: Root locus plot of a first order and second order compensation for phantom zero selection.

4.7.3. Implementing the phantom zero at the source

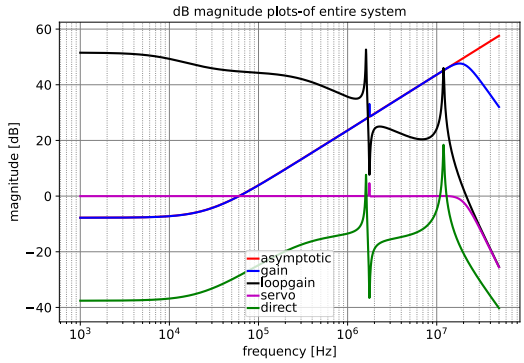
Implementing the pole at the source means $C_{phz} = 427.98[fF]$. By observing figure 4.15a the conclusion can be made that frequency compensation does not improve the system. Next to this, the system is still unstable.

4.7.4. Implementing the phantom zero at the load

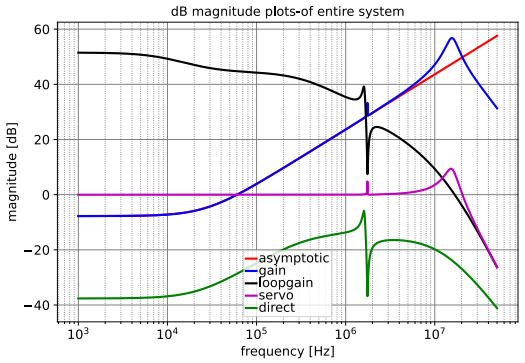
When implementing the phantom zero at the load the value of the resistor should be $R_{phz} = 19.81[\Omega]$. From this, the pole does not become stable. The magnitude response of the system is given in figures 4.15b. When implementing the phantom zero at the load the value of the resistor should be $R_{phz} = 0.689[\Omega]$. The implementation of this phantom zero does not change the placement of the unstable pole much. The system therefore is unstable.

The implementation of conjugated phantom zeros with a low Q factor can be done by setting $L_{phz} = 14.425[nH]$, by using 4.16 and by using the fact that Q should be small (smaller than 10) $R_{phz} > 0.539[\Omega]$. By inserting these values figures 4.15 become evident. Important about this implementation is the fact that all poles become stable but there is a large amount of loop gain and gain at frequencies above the desired frequencies.

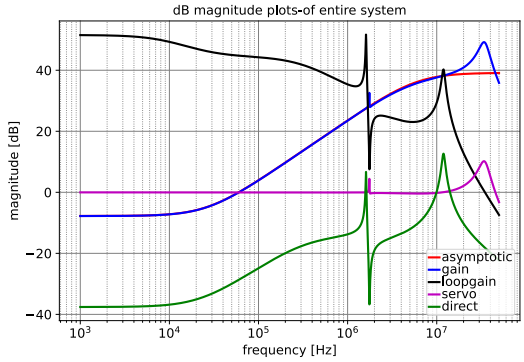
Another way to implement the complex zeros in the feedback loop with a similar Q factor comparable to the pole in the loopgain. This causes poles zero cancellation. This would mean $Lphz$ would be $L_{phz} = 4.63[nH]$ and $R_{phz} = 6.9[m\Omega]$. The results of this type of compensation are similar to the previous results. The only difference is the fact that the zeros of the asymptotic gain causes a large peak in the gain around the frequency range of interest and therefor the gain is greatly affected.



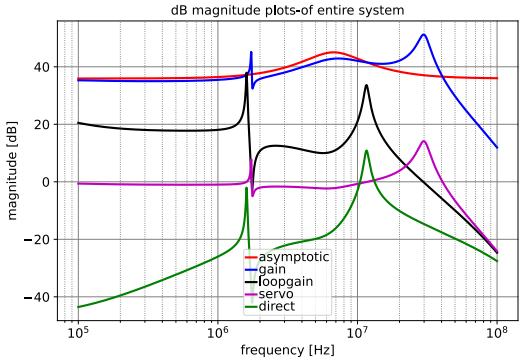
(a) Dynamic magnitude plot of the design using compensation at the source



(b) Dynamic magnitude plot of the design using compensation at the load



(c) Dynamic magnitude plot of the design using compensation at the feedback path



(d) Dynamic magnitude plot of the design using compensation at the feedback path, a second order phantom zero is used

Figure 4.15: Magnitude and phase response for multiple parameters in the asymptotic gain model.

4.7.5. Selection of compensation type

By inspecting table 4.7 it becomes clear that the options for compensation are limited. An option would also be to implement multiple different phantom zeros at the same time. From this, the decision can be made that applying two phantom zeros in the feedback network and one phantom zero at the load is the best option. Figure 4.17 shows the magnitude response

4.7.6. Dynamic voltage behavior

Since the option of implementing two conjugated phantom zeros in combination with one real phantom zero offers the most promising results it is important to consider if this option is possible when looking at the voltage-to-voltage gain of the amplifier. This can be done by making voltage the output quantity that needs to be measured and ensuring the current to voltage gain is smaller than $\frac{18.5}{10^{-2}} = 65[dB]$. By doing similar simulations as before figure 4.16 can be generated. These plots indicate that incoming signals need to be kept extremely small near the parallel resonance of the piezo at $f = 1.76[Mhz]$. Next to this, the system has an overall current-to-voltage gain near resonance that is too large so possible digital filtering needs to be applied to ensure a smaller incoming input signal near resonance.

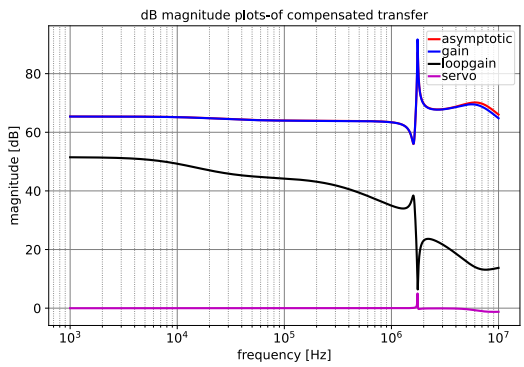


Figure 4.16: Magnitude response of amplifier output voltage v_{out} over the input current of the DAC I_{in}.

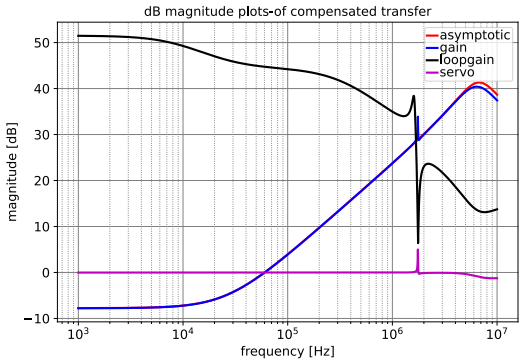


Figure 4.17: Magnitude response of chosen compensation, ie. the addition of $R_{phz,1}$, $R_{phz,2}$, and L_{phz}

Table 4.7: Table showing the location and stability of the phantom zero implementations in the system. For stability, the real part of the poles in the system should be negative. The second column shows the real part of the pole.

Location of compensation	$\Re(f_p)[MHz]$	Stable
No compensation	8.33	No
At the source	8.33	No
At the load	2.33	No
In the feedback network	4.53	No
Conjugated in the feedback network	-0.423	Yes
At load and in the feedback network	-2.95	Yes

4.7.7. Verification of the compensated system

Verification of dynamic behavior with additional resonances

In section 3.5.1 extra resonance peaks have been modeled and can be implemented in the complete simulation. The resonance peaks contribute to the magnitude and phase responses with the addition of their poles and zeros. Even though the frequency range of interest is quite small, the extra resonance peaks could lead to instability. Plots of the frequency response when adding additional resonance modes can be found in figure 4.18. With these plots, the assumption can be made that the poles and zeros of the additional resonance modes greatly influence the functionality of the entire system. Next to this, the system is still close to being unstable and parasitic effects, such as wiring inductances can greatly influence the stability of the amplifier with this implementation.

Verification of step response

Testing the entire compensation solution for a step response was done and the results can be found in figure 4.19. From this plot, the conclusion can be made that the system is still unstable. This can be caused by additional variations of the pole placement because of the biasing solution and the other resonance modes.

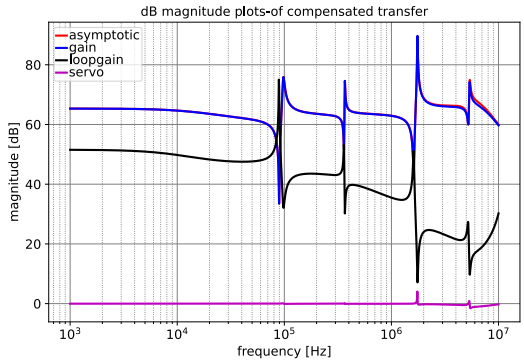


Figure 4.18: Magnitude response of $\frac{v_{out}}{i_{in}}$ when adding the additional resonance modes. v_{out} is the output voltage of the amplifier and i_{in} is the input current from the DAC

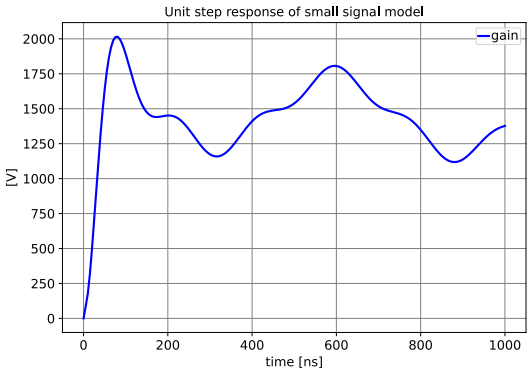


Figure 4.19: Not stable step response of the entire compensated system

4.7.8. Conclusion on frequency compensation

This section focused on improving the frequency characteristics by implementing frequency compensation. By doing this a large issue was disregarded: The initial feedback structure was not suited for a current feedback amplifier. This is the case because a capacitive feedback element causes a large loop gain for high frequencies, MHz range. Because of this, a better option for compensation is depicted in figure 4.20. In this option one of the main objectives is to follow the application node to ensure stable operation and therefor $R_f = 1.23[k\Omega]$. Due to time constraints, this design will be explained in more detail during the presentation.

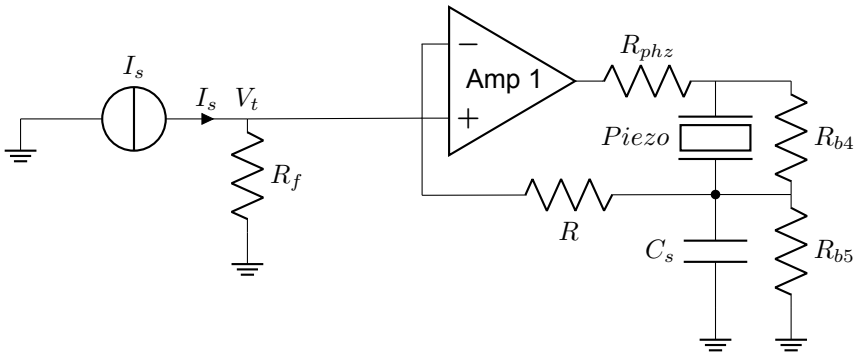


Figure 4.20: Different design prototype. R is the resistor used to stabilize the system.

5 Conclusion

The purpose of this project was to control the position of an ultrasonic transducer around its resonance region in the MHz range. In this report, an amplifier design for a piezoelectric transducer is developed. The specifications for the piezoelectric transducer are outlined in section 3.2, based on the program of requirements in chapter 2. Furthermore, the piezoelectric transducer is characterized using impedance measurement data and the BVD model, as depicted in figure 3.6, which accurately represents the four main resonance peaks. Subsequently, a structured electronics design is implemented for driving this amplifier, based on its specifications in table 4.1. A design is chosen and then verified using SliCap. The results obtained from this verification allow for an evaluation of the requirements. For the transducer, the following requirements are evaluated.

- The transducer has a resonance peak in the order of MHz, with a resonance peak at $1.6MHz$.
- The actual displacement of the piezo cannot be modeled with available information.
- The Q factor requirement could not be achieved due to the limited availability of suitable transducers.
- The minimum displacement requirement of $2.2[nm]$ is assumed to be met, based on the specifications from the manufacturer and the final implementation of the design.

In chapter 4, the specifications for the amplifier based on chapter 2, and other considerations are outlined. These requirements are evaluated:

- The transducer is driven with charge.
- The noise figure of $3dB$ is not met. The source referred noise figure is $3.85dB$.
- Commercially available circuitry and elements are used.

During simulation, the amplifier exhibits instabilities with poles located in the right half plane of the gain. This instability arises due to the interplay between the transimpedance gain and the impedance of the feedback path in the current feedback amplifier. When a low impedance is present, it results in a high loop gain, leading to the instability of previously stable poles. Even attempts to introduce phantom zeros do not rectify the instability. Consequently, it can be concluded that this amplifier configuration is unsuitable for simulation and, by extension, for real-life applications as well.
The PoR in chapter 2 that are relevant for this part of the project are evaluated here.

- The operating region of the signals is $1.6MHz$. This requirement is met, since the transducer is resonating in this region.
- The bandwidth cannot be guaranteed, because the Q factor of the transducer is 1000, which is higher than required.

5.1. Future work and recommendations

For future work, the following design considerations can be taken into account:

- To get a good estimation of the behaviour of the piezoelectric transducer, one would want to have a better model to relate the electrical and mechanical domain. Unfortunately. In many cases this is seldom specified, and therefore it is difficult to analyze the behaviour. One approach would be to measure the unknown parameters that are needed to create this elaborate model. This requires good measurement equipment, a correct testing setup, and one would have to measure many units to obtain reliable results. Another approach would be to look for another product that comes with accurate parameters.
- One of the design requirements was to use commercially available circuitry. The ADA4780 was one of the best available amplifiers in terms of voltage and current capabilities. For future work, one could consider a custom-made amplifier, capable of delivering a bigger voltage swing, because one of the limiting factor in this design is the voltage swing of the amplifier. Also, the difference between current feedback amplifiers and voltage feedback amplifiers has to be considered. Then instead of designing a transducer system over a small bandwidth, one could consider an application where the operating bandwidth of the design can be increased.
- To use the design on a more broadband level, a different filter implementation and a different transducer are needed, and there is much more voltage needed outside the resonance region of operation, since the displacement is significantly lower outside its resonance region.
- Consider a similar amplifier typology that not only ensures charge driving but also incorporates the necessary impedance feedback path of $1.23[k\Omega]$.

A

Digital to analog converter

The FPGA provides us with a 14-bit digital signal. In order for this to be used by the amplifier a Digital-to-analog converter is needed that is capable of meeting the specifications given by the amplifier.

- The DAC has to provide the amplifier with at least 1.65 MHz signals.
- In order to maintain signal integrity, the DAC has to provide at least 20 samples per period.
- The DAC has to have low glitch.

With these requirements the DAC904 from Texas instruments is used[23]. It is a high resolution 14 bit DAC, capable of delivering $200MHz$ at $100Msps$. It can deliver from 0 to $2 - 20mA$ sourcing output current. For this configuration, we will use the configuration for which the output current goes from 0 to $20mA$.

B

Derivation of specifications for the amplifier

This appendix will elaborate on some fundamental requirements for the amplifier and there will be some elaboration on associated specifications.

The current coming from the DAC is pretty self explanatory but the maximum driving current has been chosen since this requires the least amount of gain and this also favours the SNR.

The output offset charge was chosen in such a way that the DC offset corresponds to an acceptably error in displacement.

The total current to charge gain can be derived by combining the current to voltage gain, the voltage to output current gain and by using the fact that $Q(s)s = I(s)$: $G_{total} = R_f C_s$

By using the fact that commercially available operational amplifiers (usually) have supply voltages as high as $20[V]$, the bandwidth can also be defined: use the point where the maximum voltage is needed to determine the bandwidth. By using the fact that $I_{out} \approx 1[A]$ the impedance needs to be lower than 20 $[\Omega]$. This can be realized by driving from $1.575 < f < 1.625[MHz]$.

C

Derivation of biasing considerations

The first biasing consideration that can be made is one concerning accuracy. If the resistors of the voltage divider (R_{b2} and R_{b3}) in the biasing network are not the same, process variation will make the biasing less accurate. Additionally, the resistors should be as low as possible to minimize their noise contribution.

C_b should be chosen in such a way that it is a short over the frequency range of interest. This is wise since this ensures low pass filtering of the noise sources coming from the source and the two biasing resistors. The cutoff frequency of this filter is $f_{LPF} = \frac{1}{2 \cdot \pi R_{b3} C_b}$. The exact value was chosen based on the relation with respect to other biasing aspects.

R_{b1} was implemented to ensure the bias current from the voltage divider was limited. Additionally, it ensures that the biasing has no effect on the dynamic behaviour of the system.

Then the biasing resistors parallel to the sensing capacitor and to Z_{piezo} these resistors should have the property: $R_{b4} C_s = R_{b5} C_o$ any difference from this equation gives the DC gain a different gain than the gain of the amplifier outside of resonance. On resonance the story changes; the accuracy will be 1 when $(R_{b4} || R_p) C_s = R_{b5} \cdot C_o$. Since this thesis aims at driving from the first design equation to the second biasing this circuit is never fully possible.

Another consideration that is important when looking at R_{b4} and R_{b5} is the fact that the resistors also affect the dynamic response. This is the case because large resistor values damp the system and therefore the loop gain becomes smaller. A downside of this is the fact that the noise increases since I_{out} is directly affected by $S_{ii_{Rb4}}$.

References

[1] Antonio Arnau Vives. *Piezoelectric transducers and applications*. 2nd. Springer, 2004. ISBN: 978-3-540-77507-2. DOI: 10.1007/978-3-540-77508-9.

[2] Kenji Uchino. *fundamentals of piezoelectricity*. 2.3. 2023. ISBN: 978-012815733-6, 978-012815732-9.

[3] Pro-Wave Electronics corporation. *Piezoelectric Ceramic elements*. http://www.prowave.com.tw/english/item/download.htm. look for 'Piezoelectric products' Page 1, Accessed: 01/05/2023.

[4] Mark Hughes. *How Piezoelectric Speakers Work*. https://www.allaboutcircuits.com/technical-articles/how-piezoelectric-speakers-work/. Accessed: 27/04/2023. 2016.

[5] Danielle Collins. *How does hysteresis affect piezo actuator performance*. https://www.linearmotiontips.com/how-does-hysteresis-affect-piezo-actuator-performance/. 2021.

[6] Yanfang Liu et al. "Hysteresis and creep modeling and compensation for a piezoelectric actuator using a fractional-order Maxwell resistive capacitor approach". In: *Smart Materials and Structures* 22.11 (Oct. 2013), p. 115020. DOI: 10.1088/0964-1726/22/11/115020. URL: https://dx.doi.org/10.1088/0964-1726/22/11/115020.

[7] Mohsen Bazghaleh, Steven Grainger, and Morteza Mohammadzaheri. "A review of charge methods for driving piezoelectric actuators". In: *Journal of Intelligent Material Systems and Structures* 29.10 (2018), pp. 2096–2104.

[8] Texas Instruments. "Charge Amplifier Circuit". In: (2021).

[9] Piezodrive. "introduction to charge drives". In: ().

[10] Hanyun Zhou, S. H. Huang, and Wei Li. "Electrical Impedance Matching Between Piezoelectric Transducer and Power Amplifier". In: *IEEE Sensors Journal* 20.23 (2020), pp. 14273–14281. DOI: 10.1109/JSEN.2020.3008762.

[11] H.J.M.T.S. Adriaens, W.L. De Koning, and R. Banning. "Modeling piezoelectric actuators". In: *IEEE/ASME Transactions on Mechatronics* 5.4 (2000), pp. 331–341. DOI: 10.1109/3516.891044.

[12] Debojyoti Banerjee et al. "Deriving an electrical model of a two terminal piezoelectric buzzer from its impedance response". In: *2018 IEEE Applied Signal Processing Conference (ASPCON)*. 2018, pp. 114–118. DOI: 10.1109/ASPCON.2018.8748588.

[13] Jina Kim et al. "Electrical modeling of Piezoelectric ceramics for analysis and evaluation of sensory systems". In: *2008 IEEE Sensors Applications Symposium*. 2008, pp. 122–127. DOI: 10.1109/SAS13374.2008.4472956.

[14] G. Palumbo and S. Pennisi. "Current-feedback amplifiers versus voltage operational amplifiers". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 48.5 (2001), pp. 617–623. DOI: 10.1109/81.922465.

[15] Texas instruments. *Voltage feedback vs current feedback amplifiers, application report*. https://www.ti.com/lit/an/slva051/slva051.pdf.

[16] Erik Barnes. *Current Feedback Amplifiers I*. https://www.analog.com/en/analog-dialogue/articles/current-feedback-amplifiers-1.html. 1996.

[17] Anton Montagne. *piezo model*. unpublished confidential document. 2015.

[18] Gergely Csany, Michael Gray, and Miklos Gyongy. "Estimation of Acoustic Power Output from Electrical Impedance Measurements". In: *ACOUSTICS* 2.1 (Mar. 2020), pp. 37–50. DOI: 10.3390/acoustics2010004.

[19] Vytautas Dumbrava Linas Svilainis Andrius Chaziachmetovas. *Efficient high voltage pulser for piezoelectric air coupled transducer*. https://pdf.sciencedirectassets.com/271547/1-s2.0-S0041624X12X00076/1-s2.0-S0041624X12001114/main.pdf. 2012.

[20] wikipedia. *Q factor*. https://en.wikipedia.org/wiki/Q_factor. Accessed: 24/05/2023.

[21] Midas sensors. *Ultrasonic atomizing transducers*. https://www.farnell.com/datasheets/3094331.pdf. Accessed: 01/05/2023.

[22] Keysight. *E4990A Impedance Analyzer*. https://www.keysight.com/nl/en/assets/7018-04256/data-sheets/5991-3890.pdf.

[23] Texas Instruments. “DAC904 14-Bit 165-MSPS Digital-to-Analog Converter datasheet”. In: (2002). datasheet number: SBAS095C.

[24] Anton J.M. Montagne. *Structured electronic design*. 2.3. 2023. ISBN: 97890-6562-4277.

[25] Analog instruments. *High-speed, High voltage, 1 A Output Drive amplfier*. https://nl.mouser.com/datasheet/2/609/ada4870-3120105.pdf. Figure 54 on page 16 shows the closed-loop output impedance of this amplifier.

[26] Slicap development team. *SLiCAP Manual*. https://www.analog-electronics.eu/slicap/SLiCAP_python/docs/html/index.html. 2023.