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VACUUM ASSISTED LIQUIFIED METAL (VALM) TSV FILLING METHOD WITH SUPERCONDUCTIVE MATERIAL

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ABSTRACT

A novel, simple, low-cost method for the void-free filling of high aspect ratio (HAR) through-silicon-vias (TSVs) is presented. For the first-time pure indium, a type-I superconductor metal, is used to fill HAR vias, 300 to 500 µm in depth and 50 to 100 µm in diameter. The low electrical resistivity achieved without sintering, its reproducibility and straightforward processing steps, and the short time required to fill large arrays of vias at wafer scale—all make this method one of the simplest and quickest options for filling HAR TSVs for MEMS 3D integration. Moreover, the low melting point (~ 150 ˚C), malleability and superconductivity at 3.41 K make indium an interesting option in 3D interconnects for connecting quantum devices operating below 4 K.

INTRODUCTION

System downscaling, 3D integration and increasing functionalities are the main challenges that both integrated circuits (ICs) and MEMS technology have been dealing with in the past decade. Advanced packaging schemes, low-cost materials and reliable interconnect technologies are therefore required. The scope of these requirements is moreover being currently extended to the quantum realm. Particularly, microwave resonant structures that store and manipulate quantum information units called qubits are used as base for quantum computers. Contrary to classic bits, qubits can assume during the computation any superposition of 0 and 1 states, and can interfere or be entangled according to quantum mechanics, thus enhancing the computational power for specific stochastic algorithms [1]. Physically, the qubits can be realized by any two-level quantum system, such as e.g. excited states of an atom, nuclear and electron spins, positions of a crystalline defect, states of a quantum dot, or energy levels of a superconducting circuit [2]. To take full advantage of quantum computing, at least 10^4 qubits have to be integrated and interconnected on the same mm-sized platform [3], avoiding any thermal disturbance of their coherent states and operations. Compact superconductive interconnections are ideally suited to help achieve this goal, as they would produce negligible thermal noise. 3D device integration through superconductive vias can afford just that.

Through-silicon vias (TSVs) technology is at the core of the heterogeneous integration of ICs with MEMS and NEMS (Fig. 1). Although the TSV technology using copper or aluminum as vias filling material is quite established, it still presents reliability issues such as mismatch among the coefficient of thermal expansion of the materials involved. TSV filling by electroplating and electroless plating is typically time-consuming and is hardly void-free, especially for high aspect ratio (HAR) vias [4]. Silver inkjet printing [5] and magnetic assembly of Ni rods [6, 7] have been recently reported to improve vias filling. However, these filling methods show limitations in substrate choice, via depth, processing time or temperature budget. In addition, the TSVs should achieve superconductivity to be suitable for the operations of quantum devices at cryogenic temperatures [8].

Here we propose a new method based on the combination of a novel filling material for vias, Indium, and a straightforward via filling technique named Vacuum Assisted Liquified Metal (VALM). The method allows to keep the temperature of the via filling process below 160 ˚C, and achieves ~90% yield and low resistivity interconnects without the need of additional thermal treatments. The proposed method thus enables the effective use of In as TSVs filling material, which in turn allows 3D MEMS integration also for superconductive devices. Indium achieves superconductivity at higher temperatures in comparison with Aluminum [9]. This is important in quantum engineering to ease the realization of a prototype of a quantum computer.

TSV FABRICATION

The TSV fabrication starts with either 300 µm or 500 µm-thick 4 inches Si wafers. A 6 µm silicon dioxide layer is deposited on both wafer sides by a combination of thermal wet oxidation (1100 ˚C) and plasma enhanced chemical vapor deposition (400 ˚C). The silicon dioxide layer on the wafer frontside is used as hard mask during vias fabrication by deep reactive ion etching, DRIE. The SiO_2 layer is patterned with circular structures, 50 to 100 µm in diameter, by reactive plasma etching with landing on the Si substrate.

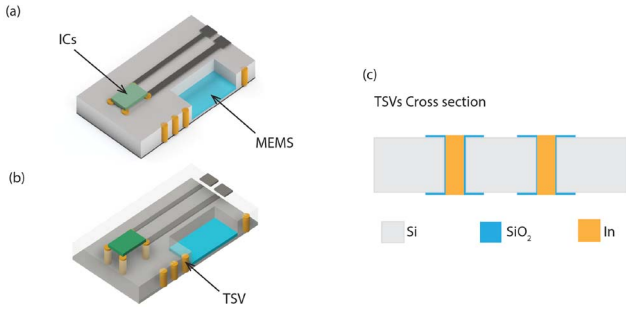

Figure 1. Sketches illustrating the heterogeneous integration concept including ICs and MEMS (a), TSVs integration (b) and schematic cross-section of the TSVs.

The TSVs are formed by DRIE of the silicon, landing on the silicon oxide at the wafer backside, and subsequent removal of the silicon dioxide left on both wafer sides by

immersion in a 40% HF solution for 20 minutes. To provide the vias with the electrical insulation necessary to avoid mutual cross-talk and fading of RF signals, a 2.8 µm-thick silicon dioxide layer is thermally grown on the surfaces of the vias, insulating the conductive core. Cross-section images of the achieved HAR TSVs for both 300 and 500 µm thick wafers are reported in Fig. 2, showing the smooth sidewalls and straight profile of the vias.

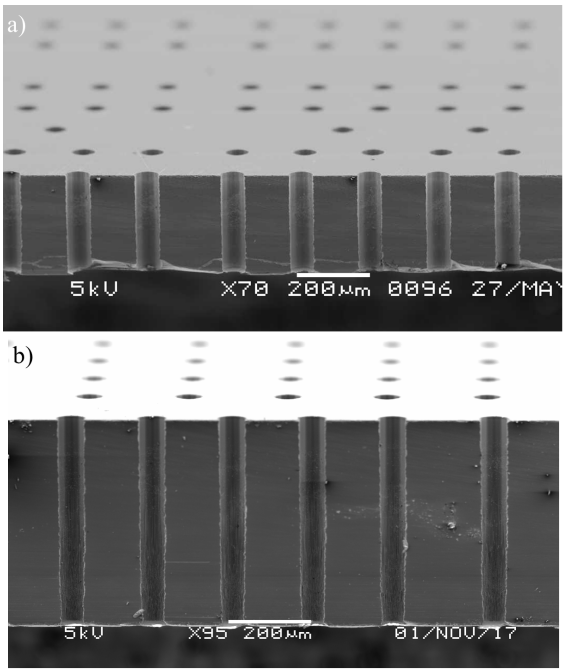

Figure 2: SEM images of TSVs cross-section after DRIE for a) 300 µm deep and b) 500 µm deep vias.

VALM PROCESS

The superconductive material used to fill the HAR TSVs is provided in the form of pure In beads (6.35 mm diameter, trace metal basis higher than 99.99%, Kurt J. Lesker Co. Ltd) with a melting temperature of ~156 °C.

The VALM method designed to fill the TSVs is based on the combination of vacuum and heat supply using a custom-made tool (Fig. 3). The vacuum is generated in the tool by the Venturi effect and reaches a maximum value of -0.85 bar with an induced air flow of 28 nl/min. The vacuum tool is placed on the hotplate which provides the heat to fully melt the In pellets and lower as much as possible its viscosity in the fluid state. The temperature shouldn't raise higher than 160 ˚C, although it lowers the viscosity, to avoid In oxidation. Then the wafer is placed on the chuck of the vacuum tool. After waiting for temperature stabilization, the In beads are deposited on top of the wafer (Fig. 4a), whereby the In melts and is spread across the wafer surface. Subsequently the vacuum is activated. As a consequence, a pressure difference between the opposite sides/openings of the vias causes the molten In to flow inside the vias in a laminar flux regime with a specific velocity pattern, which is higher at the center of the via and lower towards its contour. According to the Stokes flow law, such pressure difference is a function of the center liquid velocity, liquid density, via dimeter and via length [10].

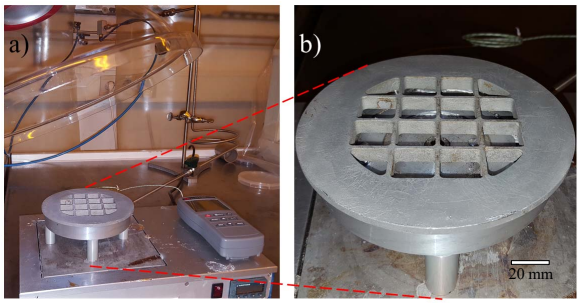

Figure 3: The custom-made setup for the VALM process (a), with close-up of the custom-made vacuum tool (b).

A blade, covered with a thin Kapton film, is then used to repeatedly scan the top wafer surface (Fig. 4b) to spread around the molten In into the vias until they are filled and a thin layer (few tens of □m-thick) is left on the surface (Fig. 4c). After blade coating, the vacuum is stopped, the wafer is covered with Kapton film for protection and turned upside down, so that the same procedure can be performed on the back side of the wafer (Fig. 4d). After complete filling of the vias, the In layer is patterned on both wafer sides using a conventional photolithographic process. A thick layer of photoresist is required to conformally coat the metal surface which presents topographical irregularities, caused by the manual blade coating and micrometric In oxide clumps which form upon exposure to air of the In surface. A ~35 µm-thick photoresist layer (AZ9260, Microchemical GmbH) was obtained by sequentially spray coating 32 layers of diluted photoresist (2 µL per layer). Finally, after resist exposure and development, the exposed In is etched in a solution of hydrochloric acid, hydrogen peroxide and water in a ratio of 8:1:1 for around 7 minutes. (Fig. 4e).

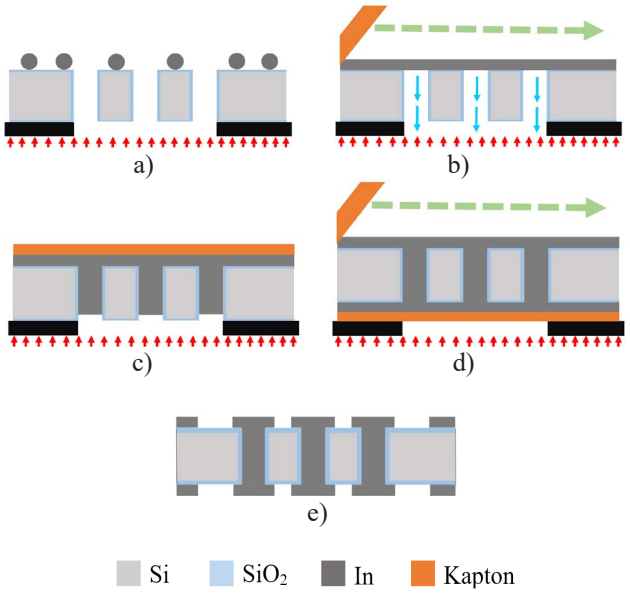

Figure 4: Key process steps for the fabrication of In-filled HAR TSVs: a) Application of In beads over the DRIE etched wafer placed over the heated vacuum tool. b) Blade coating of melted In with activated vacuum. c) Vias filling with In, and coverage of top wafer side with Kapton film. d) In blade coating on bottom wafer side. e) Patterning of top and bottom In layers after complete vias filling.

VIAS CHARACTERIZATION

To characterize the fabricated In-filled vias, electrical measurements were performed on the set of test structures shown in figure 5. A path of 200 µm width by 200 µm length was used for single via measurement. The same length was used for measurements with two vias in parallel and two vias in series with a separation between the vias of 180 µm. The width of the path was 445 µm for the parallel configuration and 945 µm for the TSVs in series.

The electrical resistivity of the achieved HAR TSVs In-filled through the VALM method was measured using an Agilent 4156C Semiconductor Parameter Analyzer and a Cascade probe station in a two-probe configuration. In particular, the measurements were performed by providing a stepwise voltage, from -15 mV to +15 mV, at three different vias configurations: single via, two vias in parallel, and two vias in series (Fig. 6).

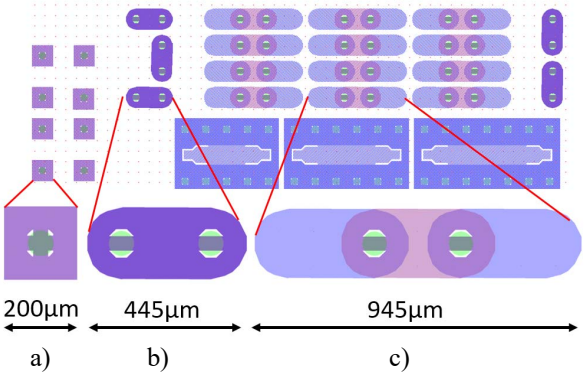

Figure 5: Layout of the test structures for the electrical characterization of the indium vias: a) one single via; b) two vias in parallel; c) two vias in series

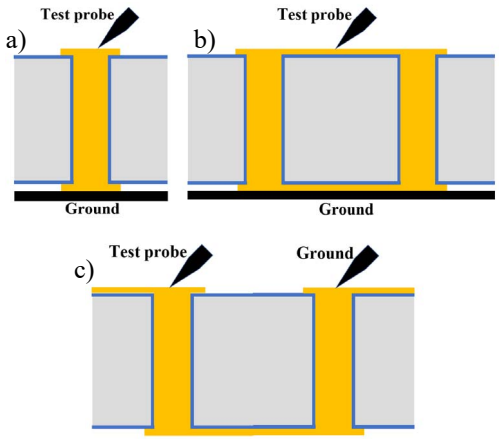

Figure 6: Configuration for the electrical characterization of the In-filled vias: a) single via; b) two vias in parallel; c) two vias in series.

RESULTS AND DISCUSSION

The VALM process allows to successfully fill HAR TSVs for both the 300 µm and 500 µm wafer thicknesses tested, as shown by the cross-section images reported in Figure 7. The voids-free filling of TSV has been obtained at wafer level in just 10 minutes, irrespective of the depth of the vias. In comparison, conventional via-filling methods such as electroplating and electro-less plating require around 20 hours and 2 hours, respectively [11]. The results achieved show the effectiveness of the proposed VALM method for filling HAR TSVs, and open up the possibility of applying the method to other low melting point metals such as gallium, tin, eutectic alloys for soldering, and micro/nano suspension pastes.

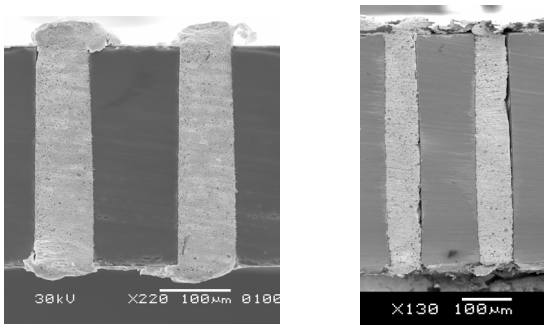

Figure 7: SEM images of TSVs cross section after filling with indium a) 300µm deep vias b) 500 µm deep vias. The voids and delamination in (b) were caused by the sawing used to obtain the cross-sections of the samples.

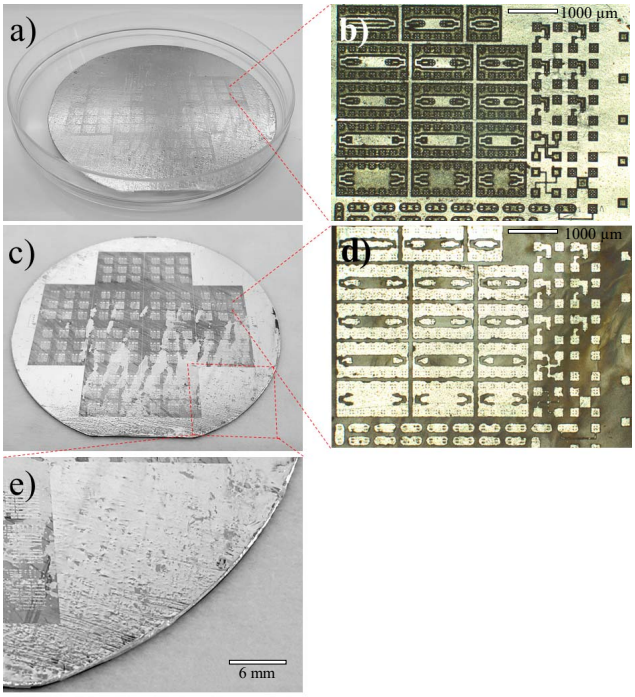

Figure 8: Patterning of indium after blade coating. Top view (a) and close-up (b) of the In-coated 4-inch wafer after photoresist patterning. Top view (c) and close-up (d) of patterned In test structures. e) Close-up of the surface roughness after In deposition.

Currently, the major challenge facing the fabrication process regards the etching of the In layers after via filling to define the interconnection lines and bondpads (Fig. 8). The challenge arises from the residual non-uniformity of the In layers after blade coating (Fig. 8c-e). It is crucial to achieve a good thickness uniformity after In spreading across the whole wafer surface to render the etching process more controllable. An ideal set-up would feature spin coating of molten In; a blade that could be actively heated, precisely aligned to the wafer surface and mechanical-

ly moved; and an oxygen-free or forming gas environment to avoid In oxidation, such as a glove box.

The measurements for 75 um diameter vias in the 300 um-thick wafer are reported in Fig. 9. A resistance of 0.16 Ω was measured for the parallel configuration, and 3.60 Ω for two vias connected in series (Fig 6). All the measured configurations show an ohmic behavior of the In-filled vias over the investigated voltage range. The obtained resistivity for a single via is as low as 593.6 μΩ•cm, which is in line with prior works [5, 6].

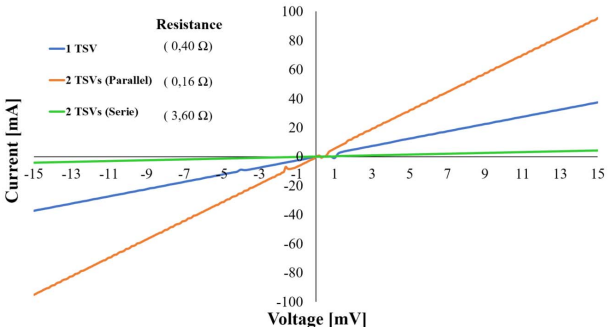

Figure 9: I-V curve of one TSV, two TSVs measured in parallel and two TSVs measured in series. An ohmic behavior is observed for the investigated voltage range.

CONCLUSIONS

We presented an effective and versatile method for filling high aspect ratio through silicon vias at wafer level with In, i.e. a low melting point and cryogenically superconductive material. HAR TSVs fabricated on both 300 and 500 μm-thick Si wafers have been used as test structures. The novel filling method, named Vacuum Assisted Liquified Metal (VALM), has been applied to fill void-free TSVs in only 10 minutes irrespectively of vias depth. The TSVs filling yield is ~ 90 % for all diameter vias tested. Moreover, filling of high density TSVs is not an issue for this method, though via surface density is inherently restricted by the DRIE process. Indium patterning is challenged by the current non-uniformity of the blade coated In layer at the wafer surface. A dedicated tool designed to guarantee a uniform thickness of the molten layer is currently under construction. Two-terminal In-filled TSV-based structures were fabricated and electrically characterized. A single via resistance of 0.40 Ω is measured for 300 μm deep TSV and 75 μm in diameter.

The simple and inexpensive method proposed to realize void-free, In-filled HAR vias is especially attractive for compact superconductive interconnects supporting quantum computing devices operating below 4 K.

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