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A Self-Matching Complementary-Reference Sensing Scheme for High-Speed and Reliable Toggle Spin Torque MRAM

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***Abstract*— While spintronic memories, for example, spin transfer torque magnetic random access memory (STT-MRAM), have shown huge potential for building next-generation memory due to their attractive characteristics, the relatively large write latency and deficient read mechanism preclude their further application for emerging concepts, such as in-memory-processing and neuromorphic computing. A toggle spin torque (TST) MRAM combining STT and spin orbit torque (SOT) has recently been proposed to alleviate the write issue. However, the sensing featuring a good balance between the reliability and speed has not been addressed. In this paper, we propose a self-matching complementary-reference (SMCR) sensing scheme, which provides not only a maximum sensing margin (SM) but also a high-speed read operation. Through applying it in the TST-MRAM, advantageous performance in terms of both write and read processes can be realized. To validate the functionality of our proposal, we design and evaluate an 8Kb TST-MRAM array, in which a read delay of 1 ns and a read bit error rate (BER) of 1.02 x 10^{-13} are achieved. Moreover, when being operated at 0.8 V supply voltage, it can reduce the read access energy by 7.5% and 20%, compared with conventional voltage sensing and dynamic reference sensing schemes, respectively.**

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***Index Terms*— MRAM, toggle spin torque, sensing margin, self-matching, read bit error.**

I. Introduction

SPIN transfer torque magnetic random access memory (STT-MRAM) is widely considered as a high potential candidate for future memory system designs, thanks to its intrinsic non-volatility, high endurance, low power consumption and good compatibility with existing complementary metal oxide semiconductor (CMOS) technology [1]–[3]. For example, a lot of STT-MRAM based cache designs have been brought out to address large bit cell size and static power dissipation issues of static RAM (SRAM) [4]–[6]. Recently, STT-MRAM is also gaining popularity in burgeoning big-data-driven applications. Various emerging computing concepts based on spintronic devices, such as in-memory-processing and neuromorphic computing, have recently been proposed to overcome Von-Neuman bottleneck and "memory wall" [7]–[10].

As shown in Fig. 1(a), STT-MRAM requires a rather long magnetization switching time and its write mechanism might cause the degradation of write endurance (e.g. 10^{12} cycles) [11]–[13], which have become an obstacle to further development of MRAM based computing concepts. Spin-orbit torque MRAM (SOT-MRAM) solves these two drawbacks by using three-terminal device structure, as shown in Fig. 1(b) [14]–[16]. However, as SOT effect suffers from the symmetric properties with respect to the perpendicular direction, it cannot achieve the deterministic switching of the magnetic tunnel junction (MTJ) with perpendicular magnetic anisotropy (PMA). An additional magnetic field is normally required, which is highly undesirable for the practical integration [17]–[19]. Some field-free solutions have thus been proposed, such as lateral structural asymmetry, antiferromagnetic (AFM) metal, voltage control magnetic anisotropy (VCMA) effect, etc. Recently, toggle spin torque MRAM (TST-MRAM) has been proposed to improve the write operation and realize field-free switching [20], [21], as depicted in Fig. 1(c). The write operation of TST-MRAM makes use of two currents: (i) one flowing through the heavy metal by T_{HM} transistor; (ii) the other injected into MTJ by T_{MTJ} transistor whose flowing direction determines the MTJ state,

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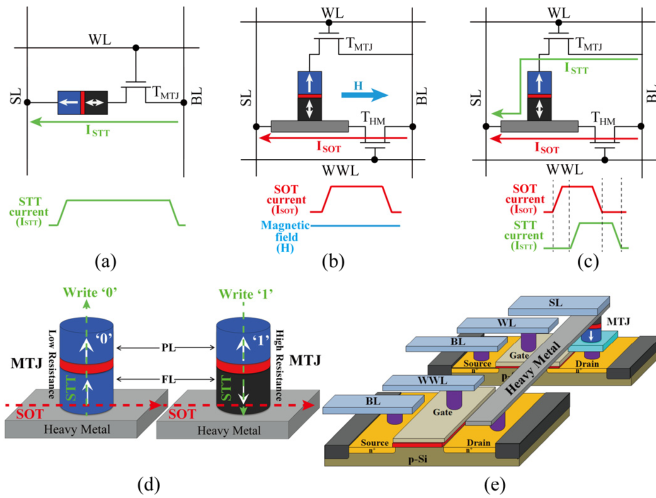

Fig. 1. (a) STT-MRAM. (b) SOT-MRAM. (c) TST-MRAM. (d) Principle of write operation for TST-MRAM. (e) Schematic diagram of TST-MRAM bit cell.

i.e., flowing from free layer (FL) to pinned layer (PL) to write '0' (low resistance, R_L) and from PL to FL to write '1' (high resistance, R_H), as shown in Fig.1(d). Fig. 1(e) shows the schematic diagram of a standard 2T1R bit cell in TST-MRAM. Although the integration density of TST-MRAM cannot be comparable to the two-terminal devices and the control process of write operation is relatively complex in TST-MRAM, theoretical studies and experimental data confirm that TST-MRAM can provide lower switching latency and smaller energy dissipation compared with STT-MRAM and SOT-MRAM [21].

However, as TST-MRAM read operation still adopts the mainstream approach of STT-MRAM, the read current can cause the possible unintentionally magnetization flipping during read operation due to the thermal fluctuation effect [22]. In addition, a part of current flowing through the heavy metal layer under the MTJ can also induce the torque on the FL [23], increasing the flipping probability during read operation. A small read current is conducive to reducing this read disturbance but will result in a lower sensing margin (*SM*) in sensing scheme. Hence, the tradeoff between read disturbance and *SM* makes the design of sensing scheme more challenging. Moreover, *SM* is reduced with feature size downscaling and process variations of device, which can seriously affect read operation and even cause read errors. Improving the tunneling magnetoresistance ratio (*TMR*) of MTJ is an effective method to increase *SM*, but the *TMR* value is only about 60% to 300% at room temperature owing to the limitations of materials, structures and process technologies [24].

To alleviate the above-mentioned issues, various sensing schemes have been introduced in [25]–[31]. [26] proposed a data-cell-variation-tolerant dual-mode sensing method to improve the fundamental read reliability while mitigating performance and energy overheads, however, it maintains read access time at around 8 ns. [27] introduced a time-based sensing scheme, which converts the bit line voltage into time-domain to discriminate the datum in bit cell. This effectively improves read reliability, but complex timing schedule extends the read access time. In [28], a continuous-recording-and-enhancement voltage (CREV) sense amplifier (SA) can tolerate smaller *SM* while enabling the read latency down to 1.3 ns at 0.9 V supply voltage. However, it requires two MTJs with complementary states to store a bit, which increases the write difficulties and degrades the storage capacity. In addition to the above approaches, the *SM* can be widened by single-cap offset-cancelled (SCOC) SA [29] and dynamically adjusting the reference voltage [30]. However, these methods sacrifice the read access time, for their reference voltage generation and the dispatch process are more complex compared with those of conventional schemes.

In this paper, we propose a self-matching complementary-reference (SMCR) sensing scheme to effectively reduce the read operation latency while improving the reliability for TST-MRAM. Beyond the efficient write operation, SMCR scheme can directly match a reference voltage complementing the sensed voltage (V_S) from two candidate reference voltages (V_{RL} and V_{RH}) instead of multiple comparisons, which can optimize the sense complexity and reduce the read access time. Besides, as voltage difference between V_S and the matched reference voltage is almost equal to V_{RH}-V_{RL}, a more reliable data sensing with large *SM* can be realized compared with the mainstream scheme of single reference. To validate the functionality of SMCR sensing scheme, we design and evaluate an 8Kb TST-MRAM array. The read access and reliability performance have been analysed by both theoretical calculations and simulations. Monte Carlo simulations have also been carried out to demonstrate the influence of manufacturing process on *SM*. Compared with state-of-the-art sensing scheme counterparts, the proposed SMCR scheme can offer a shorter read delay (1 ns), a lower read bit error rate (*BER*) (1.02×10^{-13}) and a lower read energy.

The remained part of this paper is organized as follows: Section II describes the SMCR scheme with its operation principle and the simulation framework. Read access time and reliability of SMCR scheme are analysed in Section III. Section IV presents simulation results and compares our proposal with previously reported sensing schemes of MRAM. Conclusions are presented in Section V.

II. SMCR Scheme and 8Kb TST-MRAM Array

In the conventional MRAM sensing scheme using a single reference resistance R_{ref}, the value of R_{ref} is normally the average of R_L and R_H. The reference voltage V_{ref} can thus be obtained as $(V_H + V_L)/2$, where V_H (V_L) is the sensed voltage when the MTJ in bit cell is R_H (R_L). *SM* is defined by the maximum deviation between the sensed voltage and the reference voltage, which can quantify the reliability of voltage sensing scheme [25]. Hence, the *SM* of conventional MRAM is invariably given as

$$SM = V_H - V_{ref} = V_{ref} - V_L = (V_H - V_L)/2 \quad (1)$$

In the proposed SMCR sensing scheme, V_{ref} can be dynamically adjusted to V_{RL} or V_{RH} according to the V_S value to enlarge *SM*. Here, $V_{RL} = V_L$ and $V_{RH} = V_H$. Consequently, *SM* of SMCR sensing scheme can be expressed as

$$SM = |V_S - V_{ref}| = V_H - V_{RL} = V_{RH} - V_L = V_H - V_L \quad (2)$$

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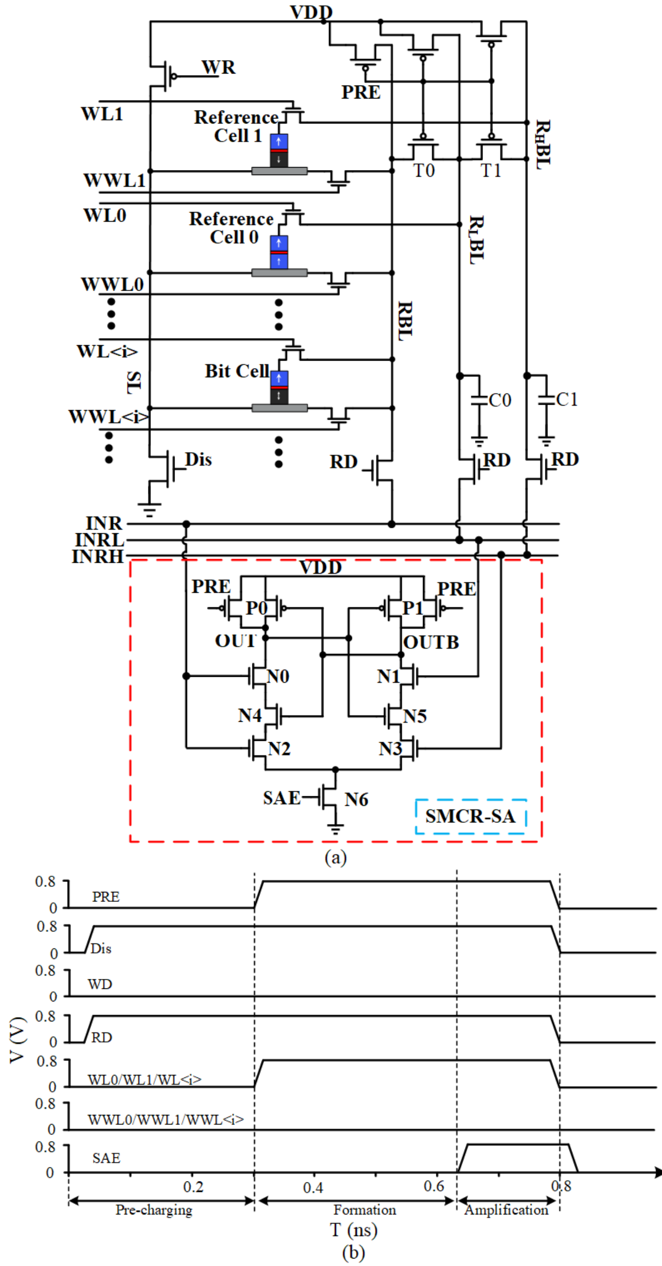

Fig. 2. (a) Schematic of the proposed SMCR sensing scheme. (b) Timing sequences of SMCR sensing scheme.

A. SMCR Scheme Design and Timing Analysis

Fig. 2(a) presents the schematic of SMCR sensing scheme, mainly including reference voltage generation circuit and SMCR-SA. Note that dual-reference bit cells are added on a column and connected to reference bit lines (i.e. R_HBL and R_LBL); the storage bit cells are connected to read bit line (i.e. RBL). Since the dual-reference cells have the same structure as storage bit cells and are located in same column, the resistive and capacitive variations are well tracked and compensated while reading '0' and '1' [29]. As there are more transistors connected to RBL compared with R_HBL and R_LBL, the parasitic capacitances of RBL is larger than those of R_HBL and R_LBL. To eliminate the large difference

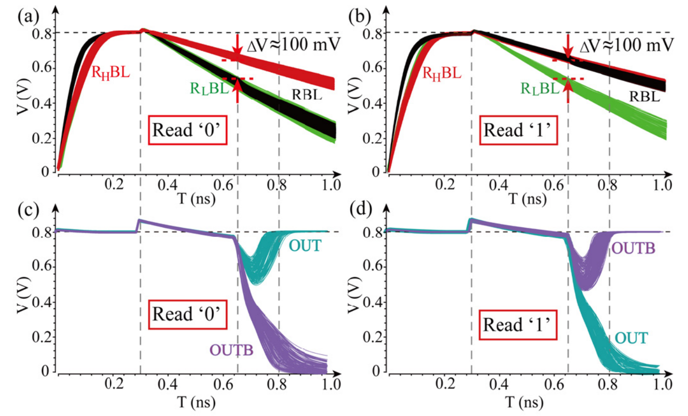

Fig. 3. Waveforms of RBL, R_HBL, R_LBL and SMCR-SA output in SMCR sensing scheme. (a) Read '0'. (b) Read '1'. (c) SMCR-SA output when reading '0'. (d) SMCR-SA output when reading '1'.

of parasitic capacitances, two load capacitances of C0 and C1 are added on R_HBL and R_LBL. Note that the sizes of the two load capacitances depend on the parasitic capacitances of RBL. Fig. 2(b) presents waveforms and timing sequences illustrating SMCR scheme basic operation principle, which includes three phases: (1) bit lines pre-charging, (2) voltages difference formation and (3) SMCR-SA amplification.

At the beginning of SMCR read operation, three bit lines RBL, R_HBL and R_LBL are pre-charged to read supply voltage VDDR, while the transistors T0 and T1 are applied to balance these voltages for getting the same voltage level at the end of phase (1). At the same time, the source line (SL) is connected to the ground by activating the Dis signal, and RD signal is set to VDDR for connecting RBL, R_HBL and R_LBL to the inputs of the proposed SMCR-SA, i.e. INR, INRH and INRL. Phase (2) is initiated by setting PRE signal to VDDR, which turns off the charging circuit while RBL, R_HBL and R_LBL preserve their status due to the parasitic capacitances of bit line. By activating WL0/WL1/WL<i> to turn on the transistors in dual-reference bit cells and datum bit cell, RBL, R_HBL and R_LBL voltages start to decrease and their drop speeds depend on the discharge channel parameters. After a period of time, variations among voltages of the three bit lines become obvious owing to the resistance differences. We carry out the Monte Carlo simulations of 10^5 samples to demonstrate the time-dependent variations of RBL, R_HBL, R_LBL and SMCR-SA output. In these Monte Carlo simulations, the process deviation of CMOS and the resistance of MTJ follow a Gaussian distribution with 5% variability [30], [32]. As depicted in Fig. 3(a) and (b), when the voltage difference reaches about 100 mV, the SMCR-SA is activated by the signal SAE. This voltage difference is defined as the *SM* of SMCR sensing scheme, which should be large enough for overcoming intrinsic PVT variation and the degradation on the flipping ability of latch (composing P0, P1, N4 and N5) and satisfying the requirement of amplification accuracy [33]–[35].

In the SMCR sensing scheme, SMCR-SA can implement the dynamically adjustment of V_{ref}. N1 and N3 gate voltages are V_{RL} and V_{RH}, respectively, and N0 and N2 gate voltages

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are both V_S. Note that the nodes OUT and OUTB have been pre-charged to VDDR at the end of phase (1). After the bit line voltages drop for a period of time in the phase (2), SMCR-SA begins to work by activating the enable signal SAE and phase (3) starts. OUT and OUTB voltages then discharge through N6, but their discharge rates are different because the transistor gate voltages on the corresponding discharge channels are different. Assume that the read datum is '0', and V_S is almost equal to V_{RL}. In this case, V_S and V_{RH} can form a pair of complementary voltages, which means that the V_{ref} is adjusted to V_{RH}. The N0 and N1 have the same gate voltages and the gate voltage of N3 is greater than that of N2. As a result, the current through N3 is larger than that through N2, which causes OUTB voltage to first decrease to $VDDR-|V_{THP}|$ (V_{THP} is PMOS threshold voltage). This turns on P0 and the initiates charging process of the OUT signal. As the discharge of OUT is still faster than its charge at that moment, its voltage continues to drop to $VDDR-|V_{THP}|$. Similarly, OUTB voltage continues to drop below V_{THN} (V_{THN} is NMOS threshold voltage), then N4 turns off and OUT voltage quickly rises through charging via the transistor P0 [33]. Subsequently, by leveraging the back-to-back inverters (i.e. P0, P1, N4 and N5) feedback, OUTB voltage decreases and OUT voltage rises until they reach '0' and '1' levels, respectively, as exhibited in Fig. 3(c). Similarly, when read datum is '1', V_S is almost the same as V_{RH}. V_S and V_{RL} then form a pair of complementary voltages, which means that the V_{ref} is adjusted to V_{RL}. N3 and N2 have the same gate voltages and the gate voltage of N0 is greater than that of N1. Fig. 3(d) shows the output of the SMCR-SA in this case, in which the OUTB will eventually be '1'. The above analysis demonstrates the self-matching capability of the SMCR scheme whose basics are to directly compare V_{RH}-V_S with V_S-V_{RL} and select the maximum between them. However, the achievement of self-matching capability causes the degradation on the flipping ability of latch due to the addition of the sampling transistors N0 and N1. In order to alleviate this degradation, we set a large enough input voltage difference and increase the size of transistors in SMCR-SA. Compared to conventional voltage SA, the input voltage difference and area of SMCR-SA increases 20 mV and 0.11 μm^2, respectively.

B. Design of the 8Kb TST-MRAM

Fig. 4(a) presents a detailed block diagram of an 8Kb TST-MRAM array, which contains 8 blocks, each with 128×8 cells. There are write and read drivers, row and column decoders, a level converter, a local timing control. To enhance the parallelism and avoid the affect between each column, each column is designed with an independent SMCR structure. In a read operation, a block of TST-MRAM can simultaneously read data from 8 bit cells. In addition, a voltage conversion from write supply voltage VDDW (1.5 V) to VDDR (0.8 V) can be realized through the level converter, which not only saves the energy during write and read operations but also alleviates read disturbance owing to the smaller current at low voltage.

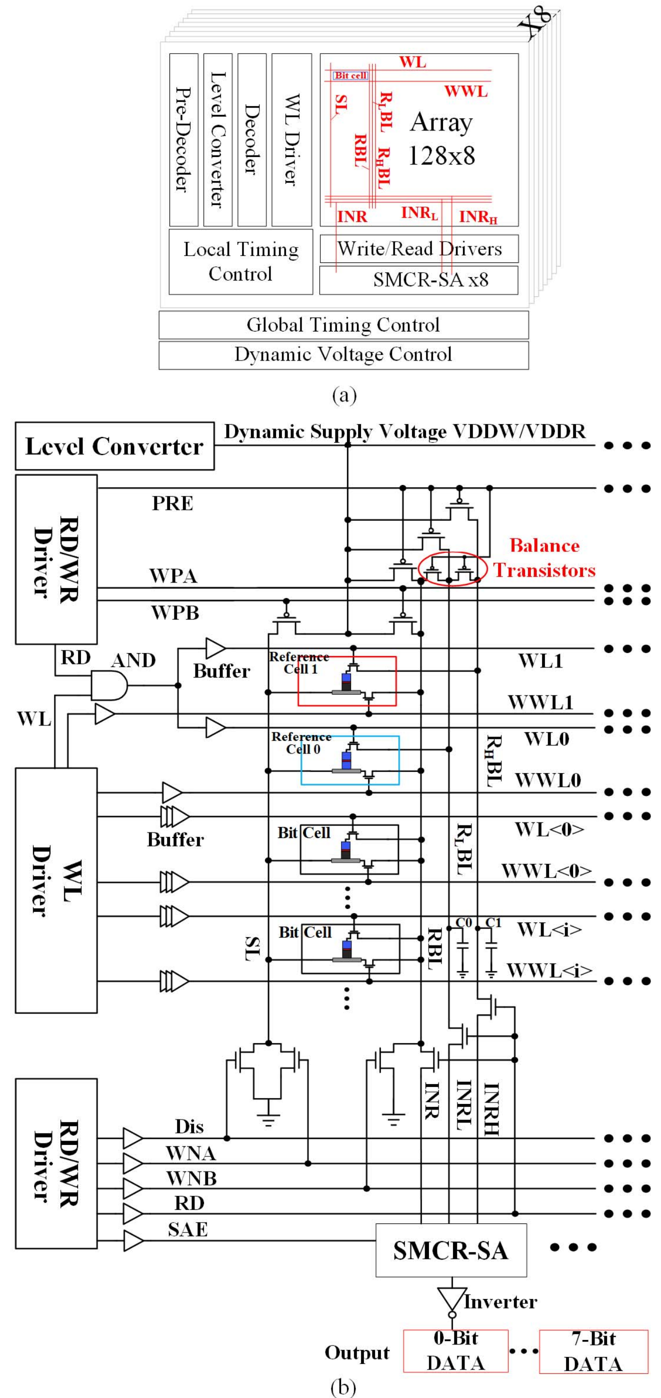

Fig. 4. (a) Detailed block diagram of an 8Kb TST-MRAM array with SMCR sensing scheme. (b) Schematic of the internal organization of a block.

The internal organization of the array is shown in Fig. 4(b). In the write operation, four control signals (WPA, WPB, WNA and WNB) are generated by the RD/WR driver to control two PMOS and two NMOS transistors, respectively. Following the timing sequence plotted in Fig. 5, for writing a datum '1', WPA drops to 0 V to turn on the connected PMOS transistor, and WNA rises to VDDW to open the connected NMOS transistor. The PMOS and NMOS transistors controlled by WPB and WNB signals are turned off. The signals

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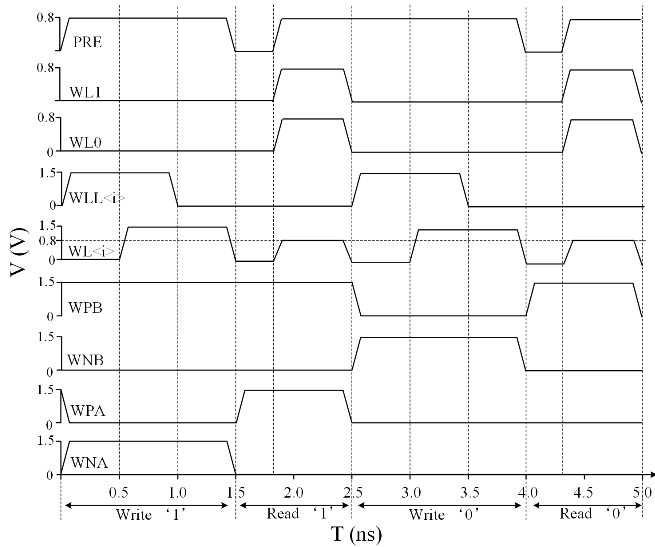

Fig. 5. Timing sequences of write and read operations for TST-MRAM array.

WWL<i> and WL<i> are activated according to the aforementioned switching mechanism of TST-MRAM. Similarly, for writing a datum '0', WPB and WNA are set to zero, WPA and WNB are set to VDDW. WWL<i> and WL<i> are then specially configured to induce reverse write currents flowing through the heavy metal and MTJ, respectively. The write operation is also performed for dual-reference cells to initialize their states. In the read operation, two PMOS and two NMOS transistors controlled by WPA, WPB, WNA and WNB are all shut, while the read control signals work as the timing sequence in Fig. 2(b).

Fig. 6 demonstrates the transient simulation results of entire write/read process for 1 bit among 8 bits in a block array. Through properly applying SOT and STT currents, the state of MTJ can be switched from '0' to '1' and then back to '0', as shown in Fig. 6(a). Here, the maximum current of SOT is 885 μA for writing '1' or 979 μA for writing '0' and STT maximum current is 121 μA for writing '1' or 266 μA for writing '0', as indicated in Fig. 6(b) and (c). Note that, although the SOT current flowing in the heavy metal is relatively large, the total power consumption will effectively be reduced due to the short time that it exists for, e.g. 1 ns.

The waveforms of the bit lines, namely RBL, R_HBL and R_LBL, are displayed in Fig. 6(d), (e) and (f). It is found that RBL provides different voltage levels according to the varied state of MTJ. In the read operation, the different voltage drops of these three bit lines can be observed. Based on them, the expected *SM* can also be obtained. Fig. 6(g), (h) and (i) illustrate the waveforms of the nodes OUTB, OUT and Output of a column in the array. The datum stored in the TST-MRAM array can successfully be read out within 1 ns.

III. Theoretical Analyses of Delay and Reliability

A. Delay Analysis

During the voltage difference formation phase, the discharges of R_HBL, R_LBL and RBL can be captured by the RC

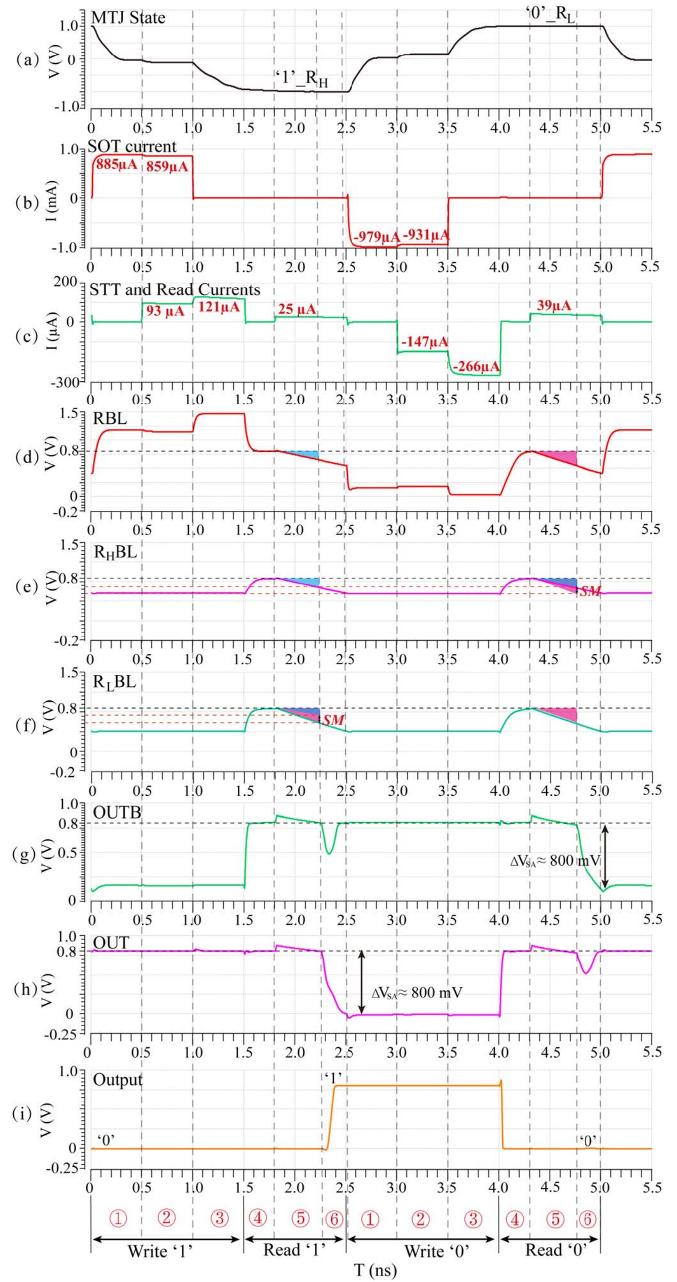

Fig. 6. Transient simulation results of TST-MRAM with SMCR sensing scheme. (a) MTJ states. (b) SOT current. (c) STT and read currents. (d)-(f) Waveforms of R_HBL, R_LBL and RBL. (g)-(h) Waveforms of OUT and OUTB of SMCR-SA output nodes. (i) Output of a column in the array. ① SOT write phase. ② SOT and STT write phase. ③ SOT write phase. ④ Bit lines and SMCR-SA pre-charge phase. ⑤ Voltage difference formation phase. ⑥ SMCR-SA amplification phase.

circuit model. The bit line voltage change can be expressed as

$$V_t = V_0 e^{-\frac{T_{dis}}{RC}} \tag{3}$$

where T_{dis} is the discharge time and V_0 is the initial voltage for the bit line. Note that the following discussion is based on the case of reading a datum '0', V_S and V_{RH} will thus form a pair of complementary voltages. For the RC circuit model, R is the total resistance of the discharge channel, including MTJ resistance, wire parasitic resistance (R_{WR})

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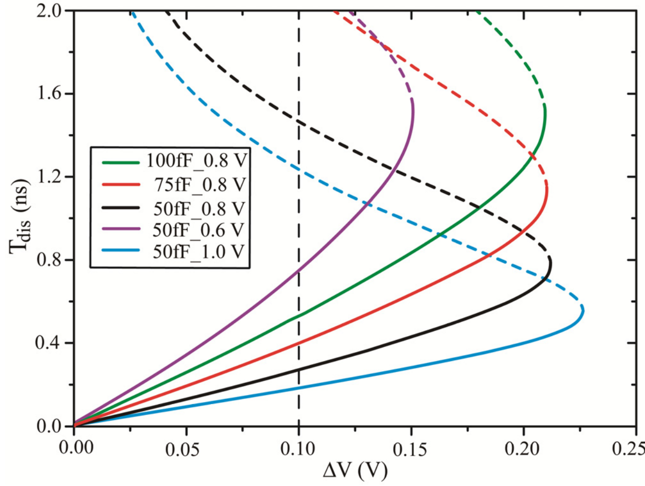

Fig. 7. Dependence of T_{dis} on ΔV with different V_0 and parasitic capacitances.

and the equivalent resistance of all transistors on discharge channel (R_{TR}). Similarly, C includes the parasitic capacitances of wire, MTJ and all transistors on discharge channel parasitic capacitance. In the simulation, according to CMOS and TST-MRAM processes technical documents, the R_{TR}, R_{WR} and R_L, are 0.05 KΩ, 0.72 KΩ and 3.98 KΩ, respectively. As the capacitance in a memory array increases when the number of bit cell increases, we evaluate T_{dis} for different capacitances, as shown in Fig. 7.

For ease of the calculation, we use the following notations: total resistance and capacitance on R_HBL discharge channel are R_{RH} and C_{RH}, respectively, and total resistance and capacitance on R_LBL discharge channel are R_{RL} and C_{RL}, respectively, and total resistance and capacitance on RBL are R_R and C_R, respectively. The voltage difference (ΔV) between V_{RH} and V_S can be expressed as

$$\Delta V = V_{RH} - V_S = V_0 e^{-\frac{T_{dis}}{R_{RH}C_{RH}}} - V_0 e^{-\frac{T_{dis}}{R_R C_R}} \tag{4}$$

indicating that the magnitude of ΔV is related to T_{dis}. On the basis of this assumption, the only factor influencing the discharge channel might come from the MTJs. Since the parasitic capacitance of MTJ is mainly affected by its feature size, we can assume that the parasitic capacitance keeps constant for the MTJs with the same feature size. The capacitance relationship of three discharge channels can be given as

$$C = C_{RH} = C_R = C_{RL} \tag{5}$$

For reading the datum '0', the MTJ connected to RBL is with low resistance. Considering the TMR ratio, that is $TMR = (R_H - R_L)/R_L$, R_{RH} and R_R can be expressed as

$$R_{RH} = R_{TR} + R_{WR} + (1 + TMR)R_L \tag{6}$$

$$R_R = R_{TR} + R_{WR} + R_L \tag{7}$$

Therefore, Eq. (4) can be rewritten as

$$\Delta V = V_0 \left(e^{-\frac{T_{dis}}{C}\frac{1}{R_{TR}+R_{WR}+(1+TMR)R_L}} - e^{-\frac{T_{dis}}{C}\frac{1}{R_{TR}+R_{WR}+R_L}}\right) \tag{8}$$

The dependence of ΔV on T_{dis} can be deduced via its inverse function as follows.

$$T_{dis} = f(\Delta V) \tag{9}$$

As Eq. (9) is difficult to analytically solve from Eq. (8), we demonstrate the relationship between T_{dis} and ΔV by utilizing the numerical solution. From the SMCR scheme read operation prospective, the T_{dis} is only meaningful before the change of ΔV reaches its maximum (solid curves in Fig. 7). Note that the maximum ΔV is almost constant for the same VDDR even with different parasitic capacitances, but the T_{dis} for achieving it heavily depends on the discharge channel parasitic capacitance. Furthermore, a larger V_0 not only widens ΔV, but also shortens the T_{dis} at which ΔV reaches its maximum value. However, increasing V_0 will enhance the read current, which could lead to unexpected magnetization switching. Hence, V_0 should be properly assigned.

In the pre-charging phase, as the charging time ($T_{charging}$) of bit line is determined by the parasitic capacitance, charging circuit and supply voltage, it can be regarded as a constant when these influencing factors are confirmed. In the proposed TST-MRAM structure, the simulation results show that $T_{charging}$ is about 0.3 ns, which makes the bit lines have enough time to be charged to VDDR. In addition, at the SMCR-SA amplification phase, the voltage amplification principle behind the SMCR-SA is similar to voltage latch SA, thus the SMCR-SA amplification phase delay can be given by [33], [34]

$$T_{SA} = \frac{2C_L V_{THP}}{I_0} + \frac{C_L}{g_{m,eff}} \ln\left(\frac{1}{V_{THP}}\sqrt{\frac{I_0}{2\beta}}\frac{\Delta V_{OUT}}{\Delta V}\right) \tag{10}$$

where C_L is the load capacitance (i.e. 5 fF) of SMCR-SA output, $g_{m,eff}$ is the effective transconductance of cross-coupled inverters, I_0 is the current flowing through N6, ΔV_{OUT} is the output of SMCR-SA and β relates to the transconductance parameter of N0, N1, N2 and N3. It is worth noting that there is a special case that N0, N1, N2 and N3 transistors are all turned off when V_{RH} voltage is reduced to V_{THN}, leading to malfunction for SMCR-SA. Hence, the bit line discharge time is limited to

$$T_{dis} \le -(R_{TR} + R_{WR} + (1 + TMR)R_L)C \ln \frac{V_{THN}}{V_0} \tag{11}$$

In summary, the total read operation delay T_{delay} of SMCR sensing scheme can be synthesized as

$$\begin{aligned} T_{delay} &= T_{charging} + T_{dis} + T_{SA} = 300ps + f(\Delta V) \\ &\quad + \frac{2C_L V_{THP}}{I_0} + \frac{C_L}{g_{m,eff}} \ln\left(\frac{1}{V_{THP}}\sqrt{\frac{I_0}{2\beta}}\frac{\Delta V_{OUT}}{\Delta V}\right) \\ &\quad \left(T_{dis} \le -(R_{TR} + R_{WR} + (1 + TMR)R_L)C \ln \frac{V_{THN}}{V_0}\right) \end{aligned} \tag{12}$$

It can be seen from Eq. (12) that T_{delay} is mainly influenced by ΔV. Fig. 8 demonstrates the relationship between T_{delay} and ΔV with different VDDR, i.e., a larger ΔV can be obtained by sacrificing the T_{delay}. Meanwhile, there are different delay times to get the same ΔV at different VDDR.

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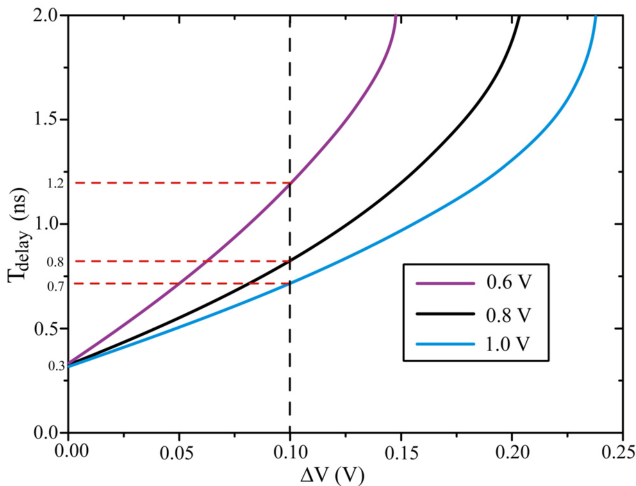

Fig. 8. Dependence of T_{delay} on ΔV with different VDDR.

For example, when ΔV is set to 100 mV to overcome intrinsic offset voltage and the voltage swing of bit line, the T_{delay} is calculated to be 0.7 ns, 0.8 ns and 1.2 ns at the supply voltage of 1 V, 0.8 V and 0.6 V, respectively.

B. Reliability Analysis

The capability of self-matching a complementary reference to the sensed voltage can effectively improve the sensing reliability. Here, we analyse the reliability of SMCR sensing through the *SM*, which is the maximum ΔV obtained under a constraint discharge time. According to the aforementioned delay analysis, a longer T_{dis} can produce a larger *SM*. There is thus a tradeoff relationship between the sensing delay and the reliability. However, even if the *SM* is determined by specifying the discharge time of the bit line, it is not a fixed value. There are fluctuations for *SM* due to the variation factors of bit-cell, SMCR and control circuit. The variation factors can be simulated by global Monte Carlo simulation which can span over different process corners [36], as illustrated in Fig. 9. It can be found that the voltage swing (V_{diff}) of bit lines will lead to about 10 mV reduction for *SM* in the SMCR sensing scheme when *SM* sets to 100 mV. On the other hand, the offset voltage (V_{offset}) of SA is also one of the major reasons behind *SM* degradation. In SMCR sensing scheme, the offset of SMCR-SA is restricted less than 15 mV at 0.8 V supply voltage. Despite the fact that the offset of SA can be further reduced by leveraging ancillary circuit and modifying the structure, it cannot be completely eliminated.

According to the above analyses, it is necessary to consider the V_{diff} and V_{offset} in the reliability discussion of SMCR sensing scheme. Hence, Eq. (2) is redefined as

$$SM = V_{RH} - V_{RL} - (V_{diff} + V_{offset}) \tag{13}$$

where V_{offset}, V_{diff}, V_{RH}, and V_{RL} are random variables, with 0, $\mu_{V_{offset}}$, $\mu_{V_{RH}}$ and $\mu_{V_{RL}}$ mean values, as well as σ_{offset}, σ_{diff}, $\sigma_{V_{RH}}$ and $\sigma_{V_{RL}}$ standard deviations, respectively [30]. The mean deviation and standard deviation of *SM*

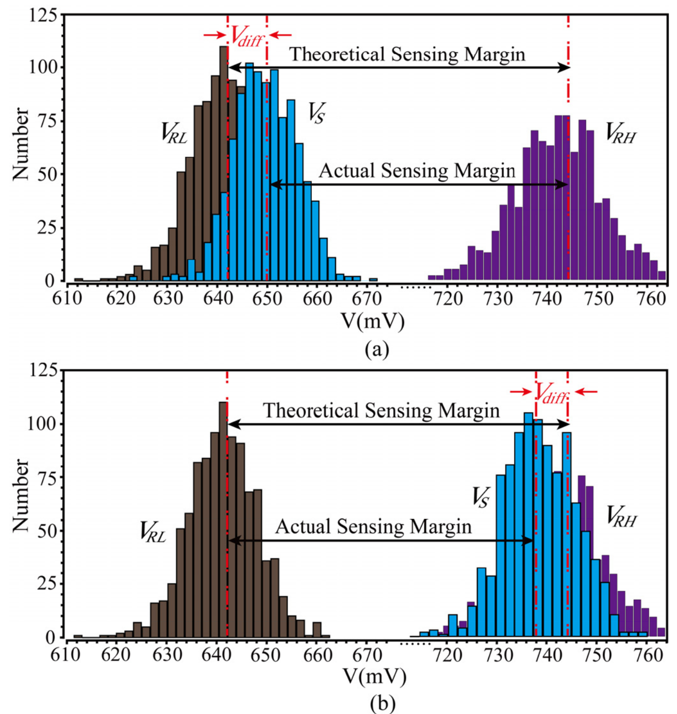

Fig. 9. Voltage statistical distributions of V_S, V_{RH} and V_{RL} when the *SM* is set to 100 mV. (a) Read '0'. (b) Read '1'.

are then deduced by

$$\mu_{SM} = \mu_{V_{RH}} - \mu_{V_{RH}} - \mu_{V_{diff}} \tag{14}$$

$$\sigma_{SM} = \sqrt{\sigma^2_{V_{RH}} + \sigma^2_{V_{RL}} + \sigma^2_{V_{diff}} + \sigma^2_{V_{offset}}} \tag{15}$$

where the variations contributed by V_{diff}, V_{offset}, V_{RH} and V_{RL} are assumed uncorrelated.

Hence, the read *BER* is given by [25]

$$BER = \frac{1}{2}(1 + erf(-\frac{1}{\sqrt{2}}\frac{1}{\sigma_{SM}/\mu_{SM}})) \tag{16}$$

where *erf(x)* is Gauss error function. The change trend of *BER* relying on different configurations of *SM* is shown in Fig. 10. It can be observed that the *BER* can be obviously improved by increasing the mean of *SM*.

IV. Performance Analyses and Discussion

To demonstrate the performance advantage of the proposed SMCR sensing scheme, including short latency and low *BER*, we compare it with conventional and recently-reported sensing structures. To this end, we embed the conventional single-ended voltage (CV) sensing and dynamic reference (DR) [30] sensing circuits into the 8Kb TST-MRAM array. This allows the above sensing schemes to be operated under the same peripheral circuits, which guarantees the comparison fairness. Hybrid CMOS/TST-MRAM simulations are conducted by applying 28 nm CMOS process technology and perpendicular-magnetic-anisotropy SOT-MTJ compact model [37]–[39].

Table I summarizes the fundamental parameters of TST-MRAM, which are dependent on physical models and

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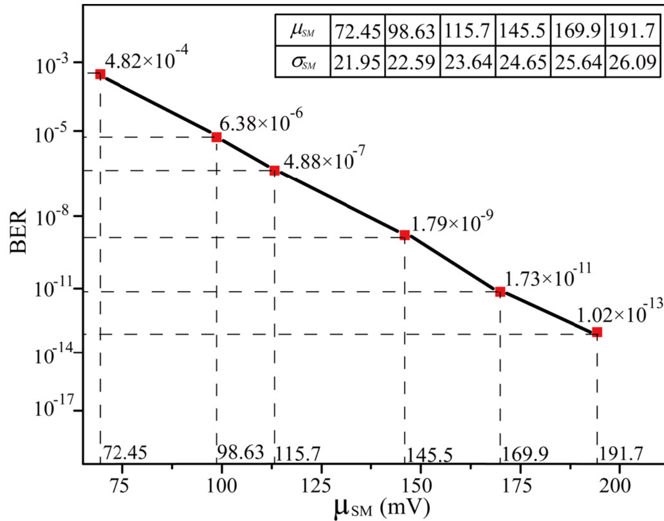

Fig. 10. *BER* of the SMCR sensing scheme with the different μ_{SM}.

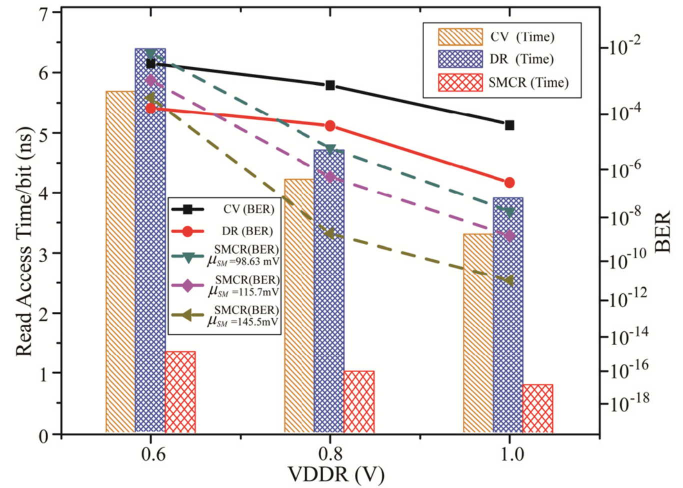

Fig. 11. *BER* and read access time per bit with different VDDR.

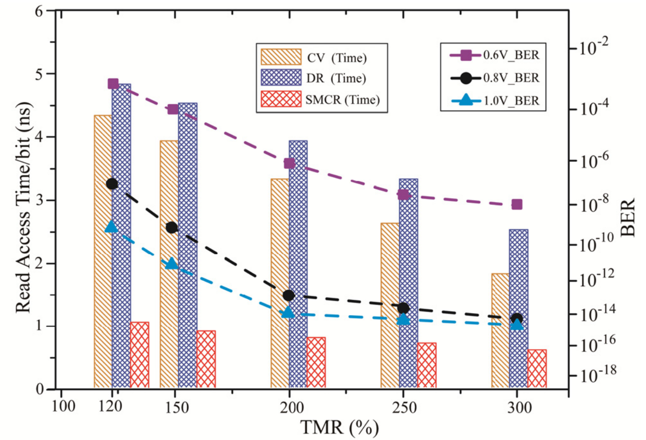

Fig. 12. *BER* and read access time per bit with different TMR.

TABLE I
KEY PARAMETERS OF TST-MRAM

Parameter	Value
MTJ area	25 nm x 25 nm x π
Oxide barrier height of MTJ	0.85 nm
free layer height of MTJ	0.7 nm
Length of heavy metal	120 nm
Width of heavy metal	100 nm
Thickness of heavy metal	3 nm
Resistivity of heavy metal	200 μΩ·cm
Temperature	300 K
Nominal R_{MTJ} at R_L (R_H) of MTJ	3.98 KΩ (8.75 KΩ)
Critical switching current R_H - R_L ($I_{c,H}$) of MTJ	45 μA
Critical switching current R_L - R_H ($I_{c,L}$) of MTJ	72 μA
Critical density of heavy metal	25 MA·μm^2
TMR	120%

experimental measurements [21], [37]. In Monte Carlo simulations for sensing circuits, the local and global variations are also taken into account. Meanwhile, assume that area and thickness following a Gaussian distribution indicate a 5% MTJ resistance variability in SOT-MTJ compact model, which is consistent with experimental data [38].

Fig. 11 shows the read access time of CV, DR and SMCR sensing schemes with different VDDR to obtain the same *SM* (e.g. 100 mV). The read access time of SMCR scheme is much shorter than the other two schemes. For example, with a voltage supply of 0.8 V, the read access time are 1 ns, 4.3 ns and 4.8 ns for SMCR, CV and DR schemes, respectively. Firstly, as the reference voltage of CV sensing scheme is typically generated by a single reference resistance (i.e. $(R_H + R_L)/2$), it thus takes longer discharge time of bit line to form the proper voltage difference. Secondly, the reference voltage in DR sensing scheme must be generated by a pseudo-PMOS inverter circuit, which additionally increases the read access delay. Moreover, the voltage difference between sensed voltage and reference voltage in DR sensing scheme develops slowly owing to the dynamic regulation mechanism. By contrast, the reference voltages are directly inputted into SMCR-SA via bit lines R_HBL, R_LBL and RBL in SMCR sensing scheme, allowing a compact read access process. Furthermore, Fig. 11 illustrates the *BER* performance of these three sensing schemes with different VDDR. The impact of *SM* on the *BER* of SMCR sensing scheme has also been analysed. We can find that SMCR sensing scheme outperforms its counterparts in term of *BER* when the mean value of *SM* is 98.63 mV and the supply voltage is 0.8 V. However, the advantage of SMCR scheme disappears at 0.6 V VDDR due to both the performance degradation of voltage SA and the reduction of *SM* at low voltage. When VDDR is increased up to 0.8 V or 1.0 V, the *BER* of SMCR sensing scheme significantly drops and will further decreases if the mean value of *SM* is raised from 98.63 mV to 145.5 mV.

In order to improve the *BER* of SMCR sensing scheme at a low VDDR (e.g. 0.6 V), an effective method is to enhance the *TMR* of MTJ. Fig. 12 exhibits the *BER* of the SMCR sensing scheme with different *TMR*. One can easily observe that the *BER* will be substantially reduced by increasing *TMR*. For example, *BER* can be reduced from 1.84×10^{-3} to 9.26×10^{-7} when *TMR* increases from 120% to 200% at 0.6 V VDDR. However, this improvement of *BER* will become weak and

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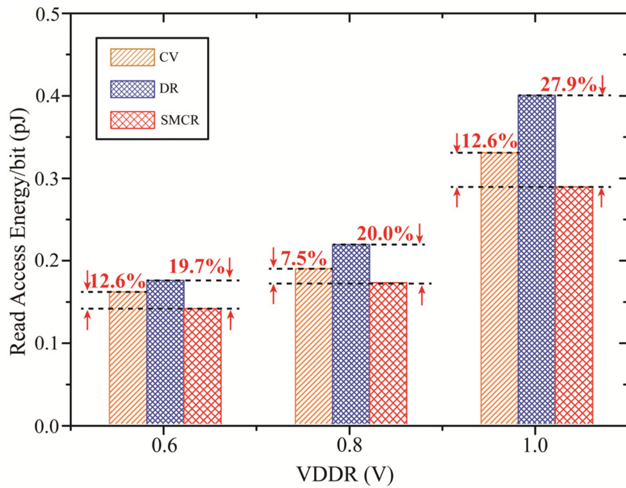

Fig. 13. Read access energy per bit with different VDDR.

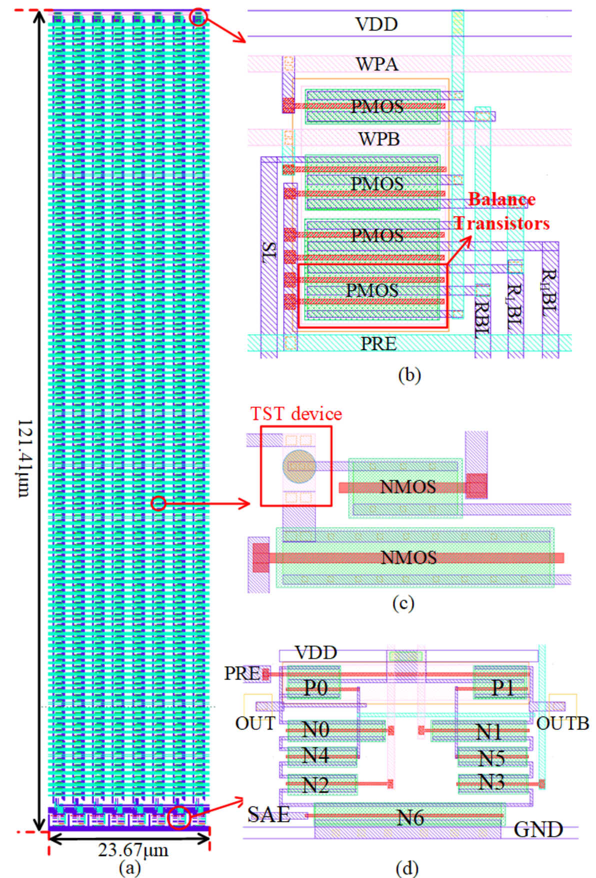

Fig. 14. Layout of a block of 8Kb TST-MRAM with SMCR sensing scheme. (a) Overall structure. (b) Write circuit part. (c) TST-MRAM bit cell. (d) SMCR-SA part.

approach to an equilibrium when *TMR* is larger than 200%. This change trend is more pronounced at the VDDR of 0.8 V and 1 V due to the intrinsic variability contribution of the bit cell [30]. *BER* can reach 1.02×10^{-13} with 300% TMR and 0.8 V VDDR. Fig. 12 also demonstrates the influence of *TMR* on the read access time. A larger *TMR* enables a faster formation of voltage difference on the bit lines. To achieve a fixed *SM*, the read access time in the case of larger *TMR* will be smaller. For example, read access time is decreased from 1 ns to 0.7 ns when *TMR* is increased from 120% to 300% at 0.8 V VDDR.

In addition to the read operation advantages in terms of speed and reliability for SMCR sensing scheme, there is also a reduction in energy consumption. Fig. 13 gives the comparison of read access energy per bit among SMCR, CV and DR sensing schemes under different VDDR. As SMCR sensing scheme makes use of dual-reference bit lines to read data, which at first glance may mean double power consumption compared to CV and DR sensing schemes, but it still outperforms them in energy consumption. The main reason is that SMCR sensing scheme can realize the faster read operation and requires smaller read current. Compared with CV and DR schemes, the read access energy per bit of SMCR sensing scheme can provide 7.5% and 20.0% reductions at 0.8 V VDDR, respectively.

With regard to the area, Fig. 14 depicts the layout of a block of 8Kb TST-MRAM based on the SMCR sensing scheme, including 128×8 bit cells, write and read circuits. The overall area is 2873.78 μm^2. The layout area is minimized by sharing the source and drain between multiple transistors. For instance, the layout of four transistors adopts the common source and drain structure, as shown in Fig. 14(b). In this way, although the number of transistors is augmented in the SMCR sensing scheme, the area overhead of it is less than 1% of the whole area. This common source and drain structure can decrease the parasitic capacitances and resistances, which is beneficial for improving the discharge speed of bit line. Besides, it can also minimize the mismatch between the transistors. It is worthy to note that this structure degrades the signal transmission performance of transistor due to the deteriorated capacitive coupling effect. However, in the SMCR sensing scheme, the transistors applying common source or drain structure are only used to transmit the supply voltage and balance these voltages. Therefore, the deterioration of capacitive coupling will not affect the SMCR performance significantly.

At last, to elucidate the overall performance advantages of the proposed SMCR sensing scheme in TST-MRAM, we compare it with various previously-reported MRAM systems in Table II. The different MRAM technologies are all simulated in the same technology node and with the same size of array. At the same power supply, TST-MRAM with SMCR sensing scheme exhibits superior overall performance compared with other existing MRAM systems. Moreover, the performance of SRAM is also added in Table II. It is commonly known that non-volatility and cell area are two advantages of MRAM systems compared with SRAM. Meanwhile, due to the intrinsic limitation of nowadays MRAMs, both write and read operations are still slower than SRAM [41]. But SMCR sensing scheme is beneficial for narrowing the read latency gap between MRAM and SRAM. In addition, we can find that the *BER* of TST-MRAM with SMCR scheme is lower than that of SRAM. This is because that the bit cell of SRAM is composed entirely of transistors, which makes the

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TABLE II
PERFORMANCE COMPARISON OF DIFFERENT MEMORY SYSTEMS

	TST-MRAM +SMCR	Single-port SOT-MRAM [40]	STT-MRAM +SCOC [29]	STT-MRAM +CREV [28]	SRAM [41]
CMOS Technology	28 nm	28 nm	28 nm	28 nm	28 nm
Array Size	8 Kb	8 Kb	8 Kb	8 Kb	8 Kb
Device Area	25 nm × 25 nm × π	60 nm × 120 nm	20 nm × 20 nm × π	20 nm × 20 nm × π	
TMR	120%	120%	120%	120%	
Cell Type	2T1TST	2T1SOT	1T1MTJ	2T2MTJ	6T
Non-Volatility	Yes	Yes	Yes	Yes	No
Power Supply	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V
BER	6.38×10^{-6}	4.72×10^{-5}	3.41×10^{-5}	8.68×10^{-5}	4.96×10^{-4}
Read Latency	1 ns	1.4 ns	1.85 ns	1.1 ns	0.5 ns
Read Energy	0.172 pJ/bit	0.679 pJ/bit	0.332 pJ/bit	0.245 pJ/bit	0.068 pJ/bit

read reliability of SRAM be significantly influenced by PVT variations [42], [43].

V. CONCLUSION

This paper presents an SMCR sensing scheme to provide high-speed and reliable read operation for TST-MRAM. This scheme can directly match a reference voltage from two candidate reference voltages to the sensed voltage, which reduces the read access time and forms a pair of complementary voltages to obtain a maximum *SM*. Theoretical analyses on delay and reliability of the proposed SMCR sensing scheme have firstly been implemented by considering the parasitic effect and manufacturing process mismatch. In order to confirm the advantageous performance, an 8Kb TST-MRAM array combining SMCR sensing scheme is designed and simulated. The mixed simulation results exhibit that our proposal can allow a read access time of 1 ns and a read *BER* of 1.02×10^{-13}. Moreover, compared with the previously published sensing schemes, SMCR sensing scheme can reduce the read access energy without significantly augmenting the area. In summary, this work offers a promising sensing solution for high-performance memories, and will be beneficial for building other emerging computing concepts.

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