Mitigation of Voltage Sags in Industrial Power Plants with Medium Voltage DC Distribution System

M.Sc. Thesis

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ABSTRACT

Unplanned downtime in industrial power systems causes high loss of revenues. These downtimes are often caused by voltage sags of durations up to 1 s. Currently many systems exist which can help to mitigate these voltage sags such as Dynamic Voltage Restorer, UPS and FACTS based devices. With the recent development in semiconductors the voltage-source-converter based high-voltage direct-current (VSC-HVDC) system has also become feasible to deal with power quality problems. With the Siemens Multifunctional Power Link (SIPLINK) also industrial customers can benefit from the advantages of the VSC technology. These benefits are due to the VSC making use of pulse width modulation (PWM) and are amongst others short circuit reduction and independent control of active and reactive power.

In this thesis the applicability of SIPLINK to mitigate voltage sags in an industrial power system is studied. Two different solutions are researched which make use of the VSC technology. One solution is based on the current rating of the converters such that the converter can continue to extract nominal power from the grid in an undervoltage situation. This method is called overrating of the system. The other is based on an auxiliary supply containing supercapacitors to replenish the grid power that is reduced during undervoltage. The research is carried on in Matlab/Simulink making use of the SimPowerSystems package. An industrial grid with three medium voltage induction motors serves as a base case for these two solutions. The important parameter to be monitored will be the speed of the motors during a sag with and without mitigation of any form.

To simulate the applicability of an overrated SIPLINK to mitigate sags a symmetrical voltage sag of 45% (i.e. 55 % remaining voltage) is applied to the grid that lasts 50 ms and another that lasts 1 s. The results will show that an 80% overrated converter is enough to mitigate these sags. To test the applicability of sag mitigation by supercapacitor, symmetrical voltage sags of 90% and 10% are applied to the grid each lasting 50 ms and 1 s. The results will show that fast mitigation can be accomplished this way.

Keywords: VSC-HVDC, vector controller, voltage sags, supercapacitor

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1. Introduction

1.1 Background

Unplanned downtime of industrial plants can be costly due to loss of production. A part of the unplanned downtime is caused by interruption of the power supply. Absence of power can be one of the reasons; however their frequency of occurrence is relatively low. Mostly the problems are caused by voltage sags of relative short duration, in the order of hundreds of milliseconds. These plants go down for instance because control systems reboot or because drives are switched off by an undervoltage protection system.
Voltage sags are defined as a momentary decrease in the RMS voltage, with a duration ranging from half a cycle up to 1 minute. These sags are caused by fault conditions within the power plant or power system, and last until the fault is cleared by a fuse or breaker. Typical causes for voltage sags on the utility side are lightning, wind, contamination of insulators, animals or accidents [1]. Also failures in the plant or the start up of large motors may lead to a sag. "The depth of the event that is seen by the industrial customer is determined by the magnitude of the fault current, stiffness of the grid, and how close the customer's facility is to the site of the fault. The duration of the event is related to the breaker-clearing time on the utility system."[2]
Because of their origin, the sags themselves are hard to avoid. However, avoiding these sags to penetrate to the plants could help to keep the plants alive during the sag and to reduce the unplanned down time. Typical sags are defined in terms of duration and magnitude (see Figure 1.1).

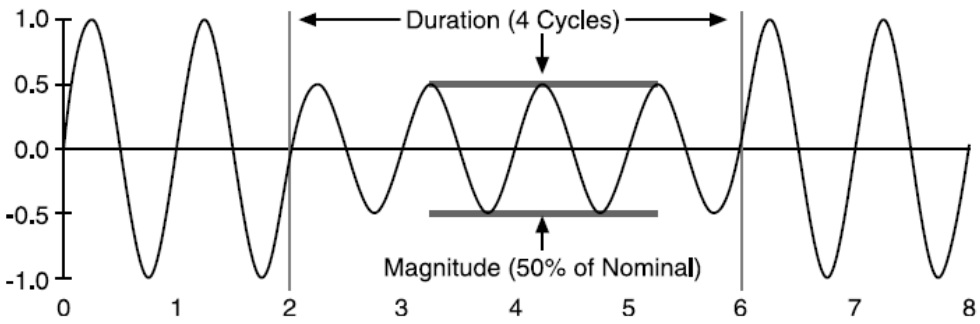

Figure 1.1: Voltage sags are described by Magnitude and Duration[2]

Industrial plants with great sensitivity to voltage sags and other power quality problems can choose from a variety of power-electronic solutions. An Uninterruptible Power Supply (UPS) can provide ride through capability against voltage interruptions and sags, depending on the storage capacity of the battery block, for several minutes or even hours. A Dynamic Voltage Restorer (DVR) can alleviate a range of dynamic power quality problems such as voltage sags and swells[3]. A static synchronous compensator (STATCOM) has the ability to either generate or absorb reactive power at a faster rate than classical solutions. This allows for the mitigation of flicker and alleviation of stability problems[3]. Application of a high voltage direct current (HVDC) system based on Insulated Gate Bipolar Transistors (IGBTs) (so called VSC-HVDC) could possibly also provide a solution. HVDC transmission is based on high power electronics and uses semiconductor technology to transport energy over long distances and also for the connection of non-synchronized grids. For a long time classic HVDC, which makes use of thyristors has been used. With newly developed semiconductors and control

equipment HVDC based on voltage source converters (VSCs) is now possible. This VSC-HVDC which is commercially available through the name HVDC Light[4] or HVDC^{PLUS} [5], is based on IGBTs and several commercial projects are already in operation. For medium voltage grids, Siemens' SIPLINK which is also based on VSCs is available on the market and can be considered when searching for a solution for power quality problems. With HVDC the AC voltage at the load side is isolated from the voltage at the supplying AC grid. Therefore the use of DC links can possibly provide new solutions to power quality related problems in industrial systems.

1.2 Objective of the thesis and method of approach

This master project focuses on how systems like SIPLINK can offer a solution for mitigation of voltage sags for industrial plants due to their ability to isolate the instantaneous power flow in the power grid from the power flow to the load. To achieve this task the use of computer simulations is needed. These computer simulations are made with Matlab/Simulink.

The objective is to investigate the applicability of an MVDC system that is equipped with proper ride through capabilities, in an industrial grid to solve power quality problems. In particular the mitigation of voltage sags is researched. To test the theories presented in this thesis a case study is done where the solutions for voltage sag mitigation with MVDC is tested. The case study involves modeling of the system which is carried on in three steps.

First a model for an industrial grid is needed. An industrial grid is a grid which contains several medium voltage levels each connected through transformers. The grid should supply several industrial size (several hundreds VA) motors with or without their corresponding drives. These motors can be a combination of induction and/or synchronous motors but mainly induction motors. A Simulink model is made of the industrial plant. This model will be used to verify the performance of the motors under a voltage sag with and without voltage sag compensation based on Siemens' SIPLINK and is the basis for the case study.

Second a model of SIPLINK is made in Simulink. This model is adapted from a model made by Siemens engineers in Erlangen, Germany. The adaptations include setting the proper voltage levels to be used, setting the controls of the system and upgrading the model to have higher power handling capabilities which coincide with the power from the industrial plant from the case study.

Third two methods for mitigation of voltage sags with an MVDC system are researched. The first method will determine how overrating of the MVDC system to handle higher currents can help mitigate sags. Second a method using an auxiliary supply in combination with a storage device is investigated. For the second method also a Simulink model will need to be derived and the performance tested in combination with the MVDC system and the industrial power plant under a voltage sag.

Based on a case study involving the model for the industrial grid and the SIPLINK model, the answer for the question of whether or not the two methods described in step 3 are possible solutions for the mitigation of a voltage sag in an industrial plant should be given.

1.3 Sags investigated

As mentioned before there are many causes to voltage sags in a power system. These causes are difficult to eliminate but nonetheless the effects can be great. Equipment mal-operation due to voltage sags and other disturbances can lead to high costs. An interrupted automotive assembly line cost one U.S. manufacturer $250000 a month until it was corrected. Interruptions to semiconductor hatch processing cost $30000 - $1 million per incident[3]. There are endless combinations of sag duration and magnitudes possible. This paragraph is dedicated to defining the types of sags that will be investigated. A voltage sag coming from the supplying high voltage AC network will be investigated. For the duration of the sag a survey done by UNIPEDE was consulted.

The Distribution Study Committee of UNIPEDE appointed a group of experts, DISDIP, to improve the knowledge of the rates of occurrence and severity of voltage dips and short interruptions in public electricity supply networks. This group arranged a coordinated series of measurements in nine countries (Austria, France, Italy, Netherlands, Norway, Sweden, Switzerland, United Kingdom, and Germany) which provide statistical information based on over 80 system-years of monitoring experience covering a wide range of environmental and geographical conditions.
The measurements were performed at 85 sites on medium voltage networks. Of these, 33 sites were cable systems and 52 sites were mixed overhead-cable systems[2]. The results from the measurements are shown in Table 1.1. From this table it can be seen that the majority of the sags (57 %) have a remaining voltage magnitude of 70 – 90 % and have a duration of up to 1 second. 19 % of the sags occur between 40-70 % remaining voltage and have a duration of up to 1 second. Sags of 10-40 % remaining voltage occur 7 % of the time with a duration between 100 ms up to 1 second. Complete interruptions of up to 1 second occurred 10 % of the time. Sags above 1 second occur only 5 % of the time for all sag magnitudes.

Remaining Voltage	10-100ms	100-500ms	500ms-1sec	1-3sec	3-20sec	20-60sec
70-90%	27%	27%	3%	1%	0%	0%
40-70%	3%	15%	1%	0%	0%	0%
10-40%	0%	6%	1%	0%	0%	0%
0% (Interruption)	0%	3%	7%	1%	1%	2%

Table 1.1: UNIPEDE DISDIP Survey, All Sites, Based on Events Per Site Per Year (84.6 total dip events per site per year between 10ms - 60 Sec)

From the above table a decision is made to design for the dimensioning of the sag compensation. Since most sags are under 1 second, this is chosen as the maximum sag duration. The most severe sag to be investigated will be 10 % remaining voltage for a duration of 1 second. Also the least severe, but more common sag of 90 % remaining voltage for 50 ms is investigated.
The sags enforced on the system are described in Table 1.2:

Remaining Voltage	**Duration (ms)**	
90%	50	1000
10%	50	1000

Table 1.2: Voltage Sags enforced on industrial system

The results of the sags enforced on the industrial system and the performance of the total system with an overrated SIPLINK and a SIPLINK with an auxiliary supply will be presented and compared in this thesis.

1.4 Existing solutions for sag mitigation

Paragraph 1.1 mentioned a UPS, DVR, STATCOM and HVDC as possible solutions for the improvement of power quality related problems like voltage sags. Common sags are described in the previous paragraph. This paragraph briefly explains the principles of the abovementioned solutions.

Uninterruptible Power Supply (UPS)

An uninterruptible power supply (UPS), is a device that maintains a continuous supply of electric power to connected equipment by supplying power from a separate source, most often a battery, when utility power is not available. It provides instant protection from a momentary power interruption and is often referred as an emergency power system. A UPS is typically used to protect computers, telecommunication equipment or other electrical equipment which are sensitive to power quality problems. UPS units come in sizes from a few hundred watts to several megawatts [6]. There are three types of UPS: off-line, line-interactive and double conversion or on-line. An off-line UPS remains in idle mode for most of the time and switches from utility power to its own power source almost instantaneously during a power failure, see Figure 1.3. In this figure the solid line represents the normal operation. Here the AC input feeds the load through an UPS switch which allows the load to be fed by normal AC or UPS power. The dashed line is the operation during a failure. The AC output is fed with power coming from the battery backup. The advantage of this topology is that it is low cost and lightweight. The disadvantages are the output voltage is not regulated, there is a transfer time or "dead" time when switching operating modes, there is no harmonic protection and the system does not protect against any other disturbances other than blackouts.

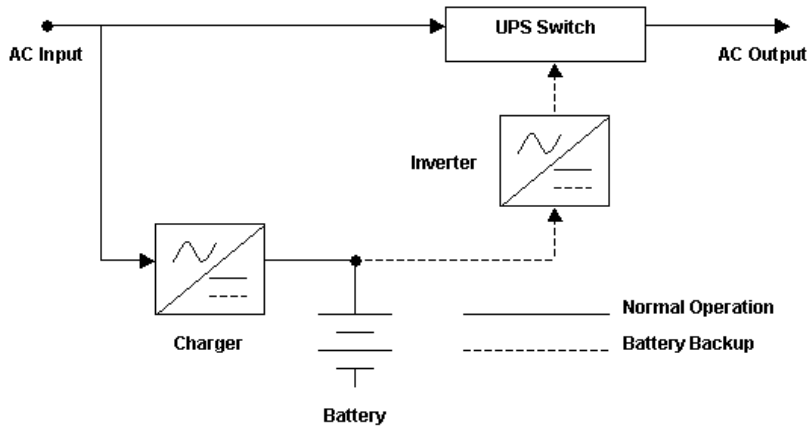

Figure 1.2: Simplified Off-line UPS[6]

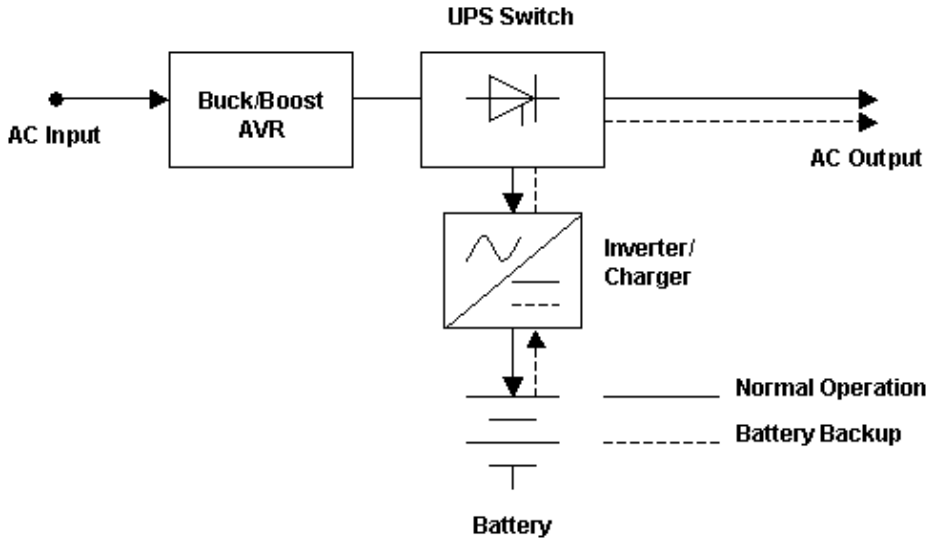

Figure 1.3: Simplified Line-Interactive UPS[6]

A line-interactive UPS is similar to an offline UPS but has a multi-tap variable-voltage autotransformer making it possible to tolerate sags and swells of the voltage without consuming the limited reserve battery power. An autotransformer is a one winding transformer in which the primary and secondary coils both have some or all of the windings in common. By changing to different power taps on the autotransformer the UPS is able to compensate for the occurring sags and swells. It does this by briefly switching to battery backup when a decrease in AC input is sensed. This is followed by the transformer tap switching and boosting the input and then turns the unit to off-line operation. During an overvoltage a similar response occurs but this time the AC is lowered. The advantages are the moderate costs, small and lightweight and it serves well during a brown-out operation. A disadvantage is the higher cost of the system.

An on-line UPS continuously powers the load from its energy reserve which can be stored in a battery or flywheel. These reserves are simultaneously being recharged from the AC supply. An on-line UPS absorbs the incoming AC supply, the filter removes the harmonics. The signal is then converted to DC then inverted to AC to supply critical power loads. An inverter supplies regulated AC power to loads at all times; either from rectified mains or a battery with an on-line UPS. In the event of a blackout, there is no transfer time or break in power supply. This configuration provides protection against all common power problems and is therefore known as a power conditioner and a line conditioner.

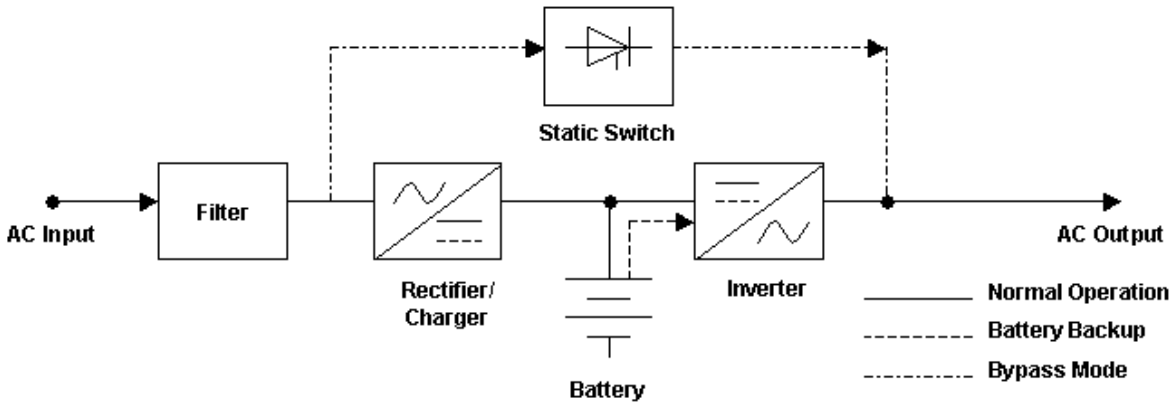

Figure 1.4: Simplified On-line UPS[6]

The advantages from this system are a stable AC voltage and frequency without harmonics to load. There is no switching between AC and battery so there is no transfer time or "dead" time. The disadvantages are the higher costs and the complexity of the system.

Dynamic Voltage Restorer (DVR)

A Dynamic Voltage Restorer (DVR) is a series compensator. It is comprised of a voltage source inverter (VSI), an energy storage (i.e. battery) supplying real power, a controller that provides gating signals for VSI control, three single-phase injecting transformers, capacitors that filter out inverter switching harmonics in the battery current and LC filters that functions to filter out switching harmonics in the injecting voltages. "The purpose of injection transformers is to accurately couple an oscillator signal into a feedback loop with minimum distortion and/or capacitive coupling." [7] For this reason, the transformers have a low magnetizing current and flat coupling over the specified frequency ranges. In normal power supply condition the DVR can be seen as in idle state. During a voltage sag the controller produces an error signal to control the DVR in such a way that a comparable amount of voltage is injected in series to the secondary side of the distribution transformers via the injecting transformers. Figure 1.5 shows the general structure of the DVR.

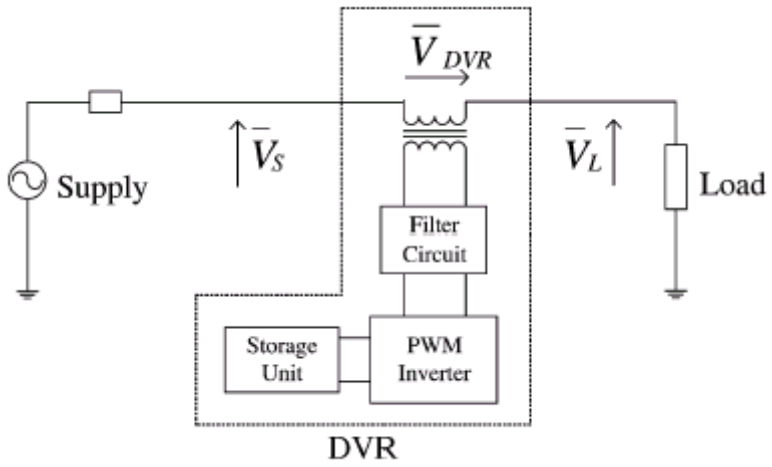

Figure 1.5: DVR structure[8]

STATCOM

The STATCOM is a shunt device of the Flexible AC Transmission Systems (FACTS) family using power electronics. It regulates voltage by generating or absorbing reactive power. When system voltage is low, the STATCOM generates reactive power. When system voltage is high, it absorbs reactive power.
Variation of the reactive power is performed by means of a Voltage-Sourced Converter (VSC) connected on the secondary side of a coupling transformer. The principle of operation is described in Figure 1.6. The power and reactive power are given by equations (1.1) and (1.2) respectively.

$$P = \frac{V_1 V_2 \sin\delta}{X} \tag{1.1}$$

$$Q = \frac{V_1(V_1 - V_2\cos\delta)}{X} \tag{1.2}$$

where
V_1 = line to line voltage of source V_1
V_2 = line to line voltage V_2
X = Reactance of interconnection transformers and filters
δ = angle of V_1 with respect to V_2

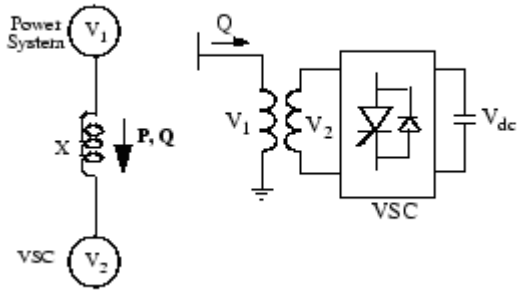

Figure 1.6: Operating principles of the STATCOM, adapted from [9]

In steady state operation the voltage V_2 which is generated by the VSC is in phase with V_1 i.e. $\delta = 0$. In this mode only reactive power is flowing since $P = 0$. If V_2 is lower than V_1, reactive power Q is flowing from V_1 to V_2 thus the STATCOM is absorbing reactive power. If V_2 is higher than V_1, Q is flowing from V_2 to V_1 making the STATCOM generate reactive power. The amount of reactive power during steady state operation. i.e. $\delta = 0$ is given by

$$Q = \frac{V_1(V_1 - V_2)}{X} \tag{1.3}$$

Depending on the power rating of the STATCOM, different technologies are used for the power converter. High power STATCOMs (several hundreds of Mvars [9]) normally use GTO-based, square-wave voltage-sourced converters (VSC), while lower power STATCOMs (tens of Mvars) use IGBT-based (or IGCT-based) pulse-width modulation (PWM) VSC.

High Voltage DC (HVDC)

HVDC technology is a high power electronics technology that make it efficient to transmit large amounts of power over long distances in electric power systems. This can be done using transmission lines or underground/submarine cables. With HVDC it is also possible to interconnect systems with differing frequencies.
There are two types of HVDC systems. Classic HVDC technology makes use of thyristors, while the newer family of HVDC makes use of Insulated Gate Bipolar Transistors (IGBTs) in a voltage source converter (VSC) topology. HVDC technology consists of a rectifier and an inverter with a DC link in between. Pulse width modulation (PWM) is used to create any voltage desired. With HVDC it is possible to separate the grid from the load, thus making it possible to isolate faults originating from the grid from penetrating to the load. For research on how HVDC can improve power quality the author refers the reader to [3] and [10].

1.5 Case Study: The Industrial Network

This paragraph deals with the specifications of the industrial grid which forms the basis for the case study. The industrial grid is needed to test the applicability of the sag mitigation solutions that are presented later on in this thesis. An industrial grid characterizes itself as having different levels of medium voltage, connected through transformers and having multiple motors. These motors can be synchronous or asynchronous (induction) motors. An example of this is the industrial grid from EdeA. EdeA is a company responsible for the exploitation of installations which produce steam, electricity and different kinds of water, air and technical gasses and distributes these to the plants of DSM and Sabic in Geleen. Substation PPF3 is part of the distribution network of Kerensheide and has different levels of medium voltage connected through transformers as well as several induction motors. It is for this reason that this substation is chosen to model an industrial grid and it will be used further in this thesis as the base case. Substation PPF3 is modeled in Matlab using Simulink with the SimPowerSystems toolbox.

1.5.1 The actual network

The network of Kerensheide starts at 150 kV which is provided by Essent B.V a utility company. It is then transformed down via 3 transformers, two of which are depicted in Figure 1.7, to 30 kV and then to 10 kV. A substation at 2 kV and one at 6 kV also exists. The substation PPF3 is connected to the 30 kV line via two three winding transformers 9m1 and 9m2. These transform the voltage down to 10 kV. At the 10 kV bus four asynchronous squirrel cage motors are directly connected, two for the use as cooling pumps, one as a compressor and one as an extruder. Also five transformers are connected. Three transform the voltage down to 0,69 kV and two to 0,4 kV. In Table 1.3 and Table 1.4 the data for the motors and transformers are summarized.

Transformers 150/30 kV					Transformers 30/10 kV	
Transf.		1 (2m1)	2 (2m2)	3 (2m3)	1 (9m1)	2 (9m2)
U_{prim}	**[kV]**	150,0	150,0	150,0	30,0	30,0
U_{sec}	**[kV]**	32,5	32,5	32,5	10,5	10,5
S_{rat}	**[MVA]**	70,0	70,0	70,0	25,0	25,0
U_k rat		14,28%	15,30%	14,28%	9,99%	10,06%
Vector group		YNd7	YNd7	YNd7	YNyn0 d	YNyn0 d
$U_{working}$	**[kV]**	31,5	31,5	31,5	31,5	31,5

Table 1.3: Transformers

Name	Motor	P[MW]	U_{rat}[V]	P_n[MW]	I_n[A]	I_a[A]	I_a/I_n	Remark
K3501	Compressor	0,530	10,000	0,530	39			Active
B3601-2	Extruder	6,000	10,000	6,000	402	1930	4,8	Active
P3001A	Cooling pump	0,525	10,000	0,525	38			50% in
P3001B	Cooling pump	0,525	10,000	0,525	38			50% in

Table 1.4: Motors

The low voltage transformers are summed together and result in S_{rat} = 12650 kVA with U_k = 6 %. Here S_{rat} is the rated apparent power and U_k is the short circuit voltage. Also the low voltage load equals a total of 3,2 MW of which 80 % is from motors and 20 % is ohmic. The total load of the system is P_{tot} =10.78 MVA. A schematic overview of substation PPF 3 is given in Figure 1.7.

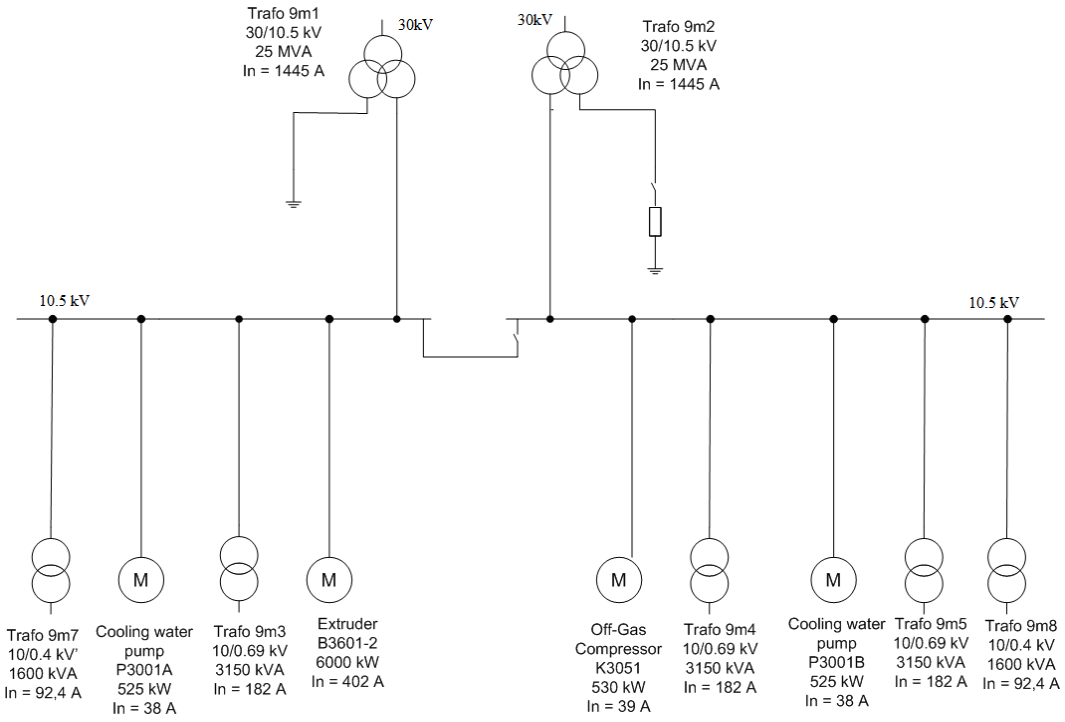

Figure 1.7: Schematic overview of substation PPF 3 of the EdeA network

1.5.2 The Simulink SimPowerSystems model

In this paragraph the Simulink model made with the SimPowerSystems toolbox is presented. This model will later be used as a case study to research the effects of voltage sags with and without sag mitigation. The reason for using the SimPowerSystems toolbox is because many elements such as transformers, motors, breakers and power electronics are readily available in individual blocks. For the model it was decided to only take one of the 150/30 kV transformers and one 30/10 kV transformer, 2m1 and 9m1 respectively. This was done because these two transformers are large enough to support the entire load on PPF3 and by leaving the non relevant transformers out also calculation time is saved. For the Simulink dynamic model of the asynchronous motors also values for rotor and stator resistances and inductances were needed along with values for the inertia, pole pairs and friction factor. These values are mostly only provided by the manufacturer upon request and are not available in this case. For this reason approximations for these values were sought. The correctness of these approximations were determined by looking at speed current, torque and voltage characteristics and compared to the values from Table 1.4. The motor and transformer parameters can be found in Appendix A.
For the pumps a quadratic mechanical torque characteristic was assumed. This is the most common characteristic for a pump. For the other motors a constant mechanical torque was assumed.

For final modelling the motors with quadratic mechanical torque characteristics on the same bus are aggregated as one motor and the motors with constant mechanical torque also. This is done to reduce simulation time.

1.6 Medium Voltage Direct Current

1.6.1 Introduction

This chapter presents general aspects of VSC-HVDC transmission. VSC-MVDC systems are based on the same principle but have lower power handling capabilities and lower voltages.

1.6.2 VSC-HVDC System Description

The classic HVDC, which makes use of thyristors is widely used all over the world. More recently a new type of HVDC has become available. It makes use of advanced semiconductor technology like Insulated Gate Bipolar Transistors (IGBTs) and Gate Turn-Off Thyristors (GTOs) for the conversion from AC to DC and vice versa. The converters are voltage source converters (VSCs) which operate with high switching frequencies (1-2kHz) utilizing pulse width modulation (PWM) [3]. Due to this use of PWM to create the desired waveform, it is possible to create any waveform, phase angle and magnitude of the fundamental frequency component.
A typical VSC-HVDC system consists of, converters, transformers, phase reactors, AC filters, DC capacitors and DC cables. This is shown in Figure 1.8.

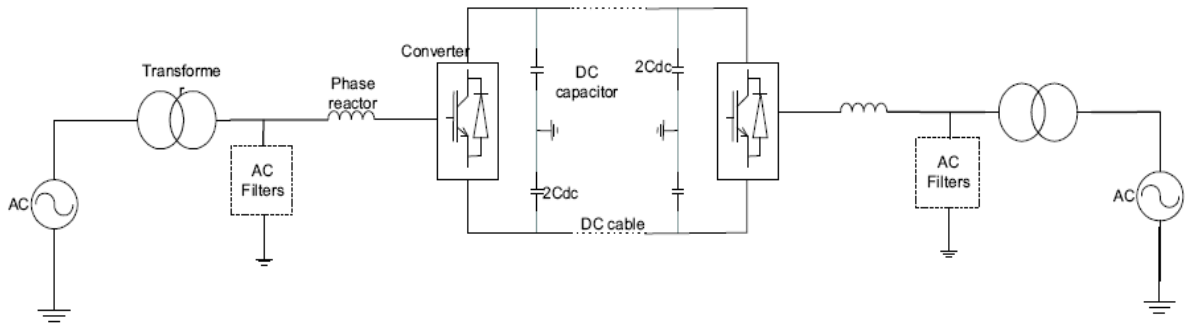

Figure 1.8: A VSC-HVDC system[10]

Converters

The converters are made with IGBT power semiconductors, one converter functions as a rectifier, the other as an inverter. The application of the VSC-HVDC system determines how the two converters are connected i.e. back to back or via a DC cable. Different rated powers can be achieved connecting the converters in series and parallel. The number of devices needed is determined by the rated power of the bridge and the power handling capabilities of the switching devices.

Transformers

Transformers are used to connect the converters to the AC system. They are responsible for providing the right voltage level to each converter. The leakage reactance of the transformer also acts as a phase reactor, used for the control of the active and reactive power. A good amount of harmonic filtering can also be achieved due to the reactors of the transformers.

Phase reactors

"The phase reactors are used for controlling both the active and reactive power flow by regulating currents through them"[3]. They also function as ac filters to filter out the harmonic contents of the AC currents which are caused by the switching action of the VSCs. The transformer leakage reactance together with the phase reactor allow the VSC output voltage to shift in phase and amplitude with respect to the AC system. Control of the converter active and reactive power output can be achieved in this manner.

AC filters

The switching action of the IGBTs produce ac voltages which contain high order harmonic components. These harmonic components need to be prevented from entering the ac system, causing malfunctioning of ac system equipment and/or radio and telecommunication systems. For this high-pass filters are needed. "With VSC converters there is no need to compensate any reactive power consumed by the converter itself and the current harmonics on the ac side are related directly to the PWM frequency" [10] . Usually second and third order filters are used for HVDC systems. These are shown in Figure 1.9.

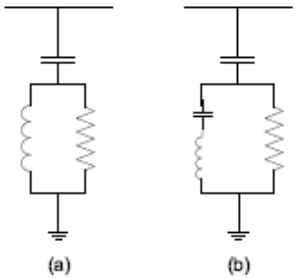

Figure 1.9: Passive high pass filter. (a) Second-order filter (b) Third-order filter, from [10]

DC capacitors

On the DC side there are capacitors, the size of these capacitors depends on the required DC voltage. During transients they act as an energy buffer to keep the power balance. The capacitors also reduce the voltage ripple on the DC side.

DC cables

The cables used in VSC-HVDC applications make use of insulation that is made up from extruded polymer. This material is resistant to DC voltage. “Polymeric cables are the preferred choice for HVDC, mainly because of their mechanical strength, flexibility, and low weight” [10].

1.6.3 Proposed MVDC Enhanced Industrial Network

For the research of the mitigation concepts to be proposed, the interconnection of the industrial grid from Figure 1.7 and the MVDC system of Figure 1.8 as shown in Figure 1.10 is proposed. As shown in Figure 1.7 there are two transformers 9m1 and 9m2 in the substation, both of which can sustain the entire load alone in case of failure of one transformer. The reason for the two transformers is to add redundancy in the case of a failure. Also during the startup of the motors, high amounts of current need to be drawn from the grid often times surpassing the capability of one transformer. Thus both transformers are needed. From Figure 1.10 it follows that the 10.5 kV bus will be connected through two MVDC systems. This is the topology that will be simulated. It is assumed that the transformer 9m1 on site can generate the 1100 V needed for the converter terminals. Other topologies exist and are described in paragraph 4.4.3. For redundancy a second branch with a transformer and SIPLINK converter can be added. This topology was not simulated to save calculation time. The system is modelled to be able to withstand normal overloads which include starting up of motors one at a time.

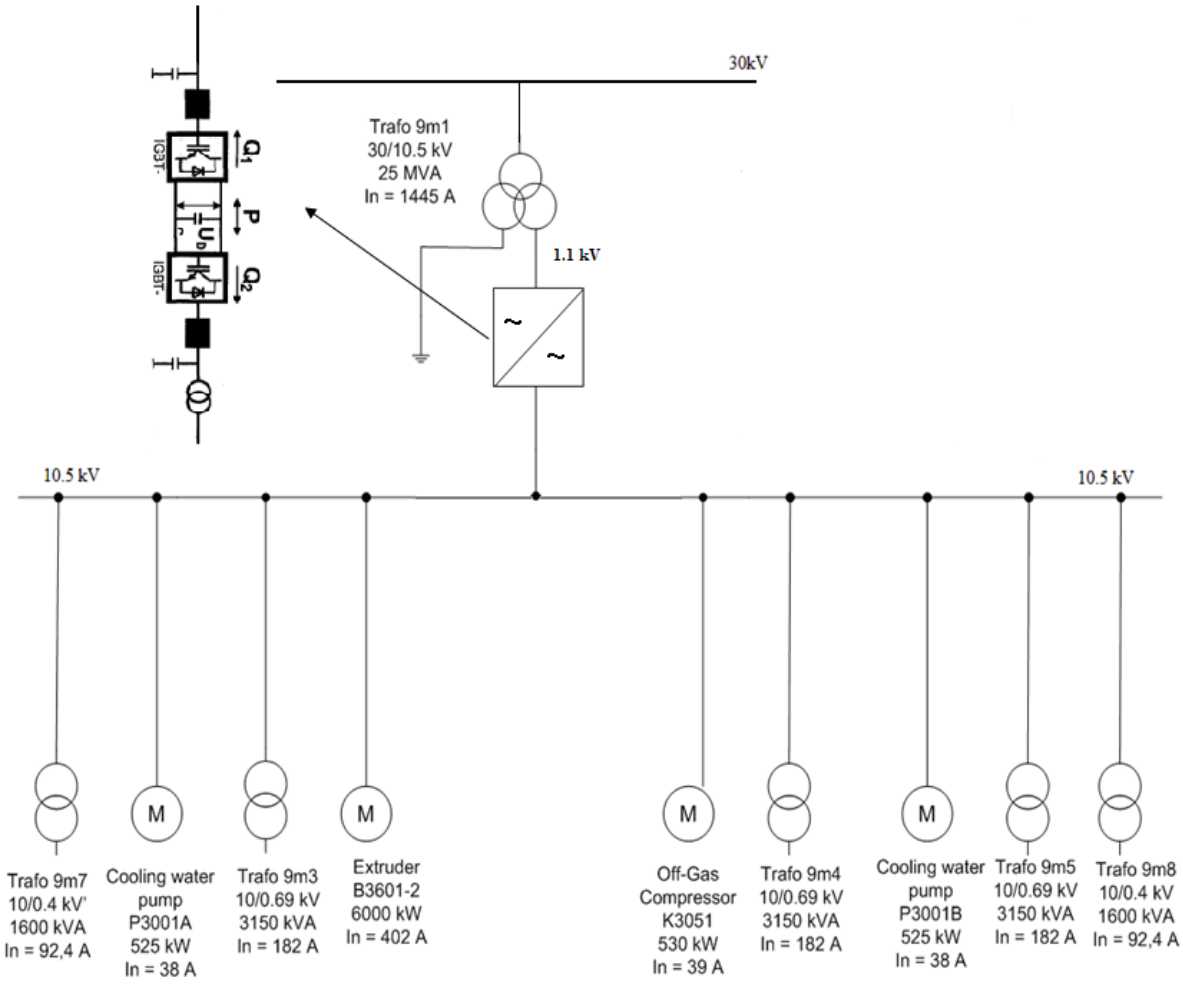

Figure 1.10: Proposed MVDC enhanced industrial grid

1.7 Mitigation systems concept

As previously noted, a voltage sag involves a decrease in voltage magnitude for a very short period of time. With an unaltered current magnitude, this voltage sag then also implies a temporary decrease in the transferred power to the load. This temporary decrease can be disastrous for equipment as motors and computers in an industrial plant. In order to mitigate these voltage sags, extra power needs to be injected into the system. The system in this thesis is an industrial plant which is connected to the grid through a Medium Voltage DC Link specifically Siemens' Multifunctional Power Link or SIPLINK. The valves in the converter limit the short circuit current. Faults in the AC grid will not propagate to the load because of the use of these current limiting converters. This increases plant availability because the load side can be protected from the grid side. In this system however the load is not protected from short dips in the voltage. For cost and converter response reasons, the DC link capacitor is designed to be small. This is explained later in chapter 4. The DC link capacitor thus can provide a buffer for when there are transients in the system, but is not large enough to provide ride through capability in the event of a voltage sag with durations of over a few tens of milliseconds. In order to increase the power that is being transmitted to the DC link in the event of a voltage sag, two methods have been chosen. The first is the overrating of the SIPLINK system and the second is increasing the power by adding an extra auxiliary supply to the link. A global representation of the power balance as well as the mitigation methods is given next.

1.7.1 Global Power Balance

During a voltage sag, the voltage drops in magnitude as given in Figure 1.1. This causes a sag in the power magnitude according to the power equation $P=VI$. The power balance for this equation is shown in Figure 1.11, where all quantities represent the converter grid side components.

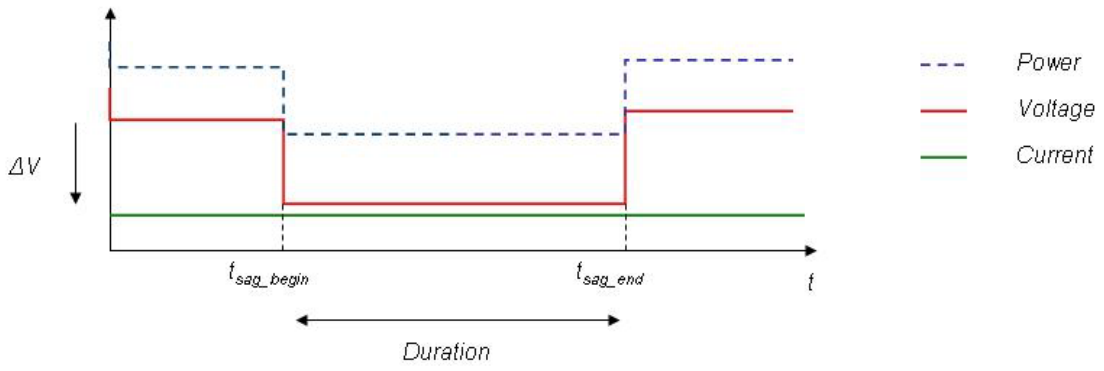

Figure 1.11: Power Balance during a voltage sag

In order to prevent equipment from malfunctioning, the power lost needs to be compensated for.

1.7.2 Converter overrating

By converter overrating it is meant that the grid current drawn by the converter is temporarily increased with respect to the load or working current in order to satisfy the equation $P=VI$, to maintain a constant power P. The power balance is then given by Figure 1.12.

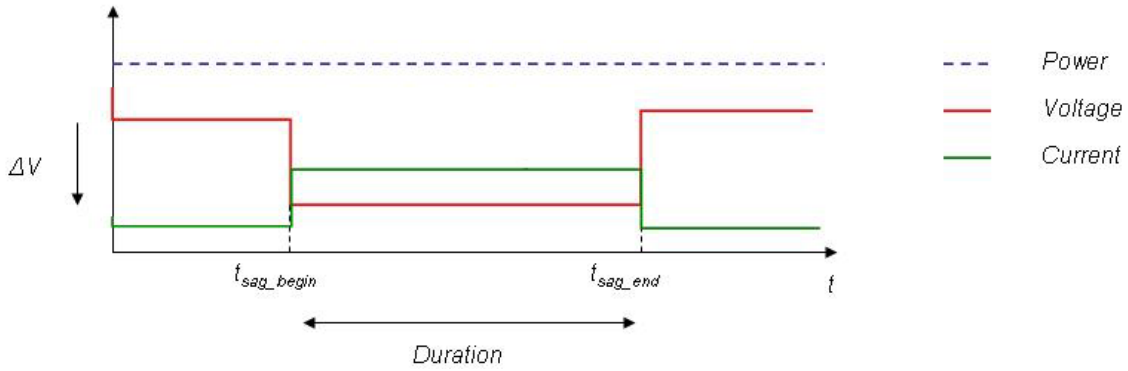

Figure 1.12: Power Balance during overrating of converters

The increase of the grid current drawn by the converter can be done in two ways.

1. The converter can be operated below its rated or nominal current. In this case in the event of a voltage sag, the current can be increased up to its maximum constant current $I_{conv,rat}$.
2. More converters can be connected in parallel to increase the current handling capability of the total system as in Figure 1.13. In all cases the extra current is drawn from the grid which is assumed to have a large short circuit power. In both cases the overrating percentage determine the costs. This percentage is determined by (1.4).

$$k_{or} = \frac{I_{conv,rat}}{I_{load,rat}} \tag{1.4}$$

Where $I_{conv,rat}$ is the nominal converter current and $I_{load,rat}$ is the rated load current.

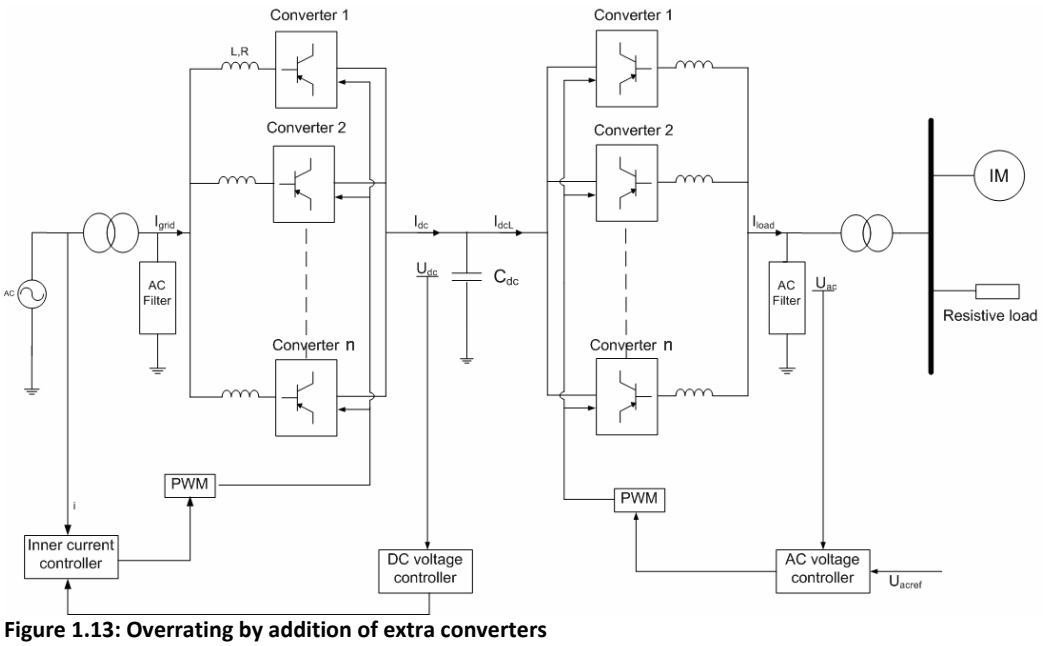

Figure 1.13: Overrating by addition of extra converters

1.7.3 Auxiliary supply

In this case mitigation of a voltage sag is done by stabilizing P_{dcL} (see Figure 1.15) during a voltage sag. Apart from increasing the operating current of the converter by drawing it from the grid, also extra current can be injected in the DC link through an auxiliary supply. The extra current comes from an extra storage device. In this case the power balance is represented by Figure 1.14.

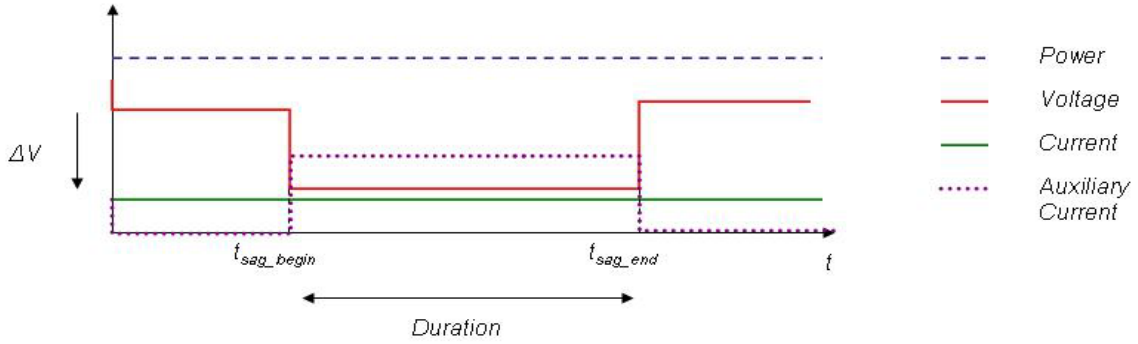

Figure 1.14: Power Balance with Auxiliary supply

The representation of the system with the auxiliary supply is given in Figure 1.15.

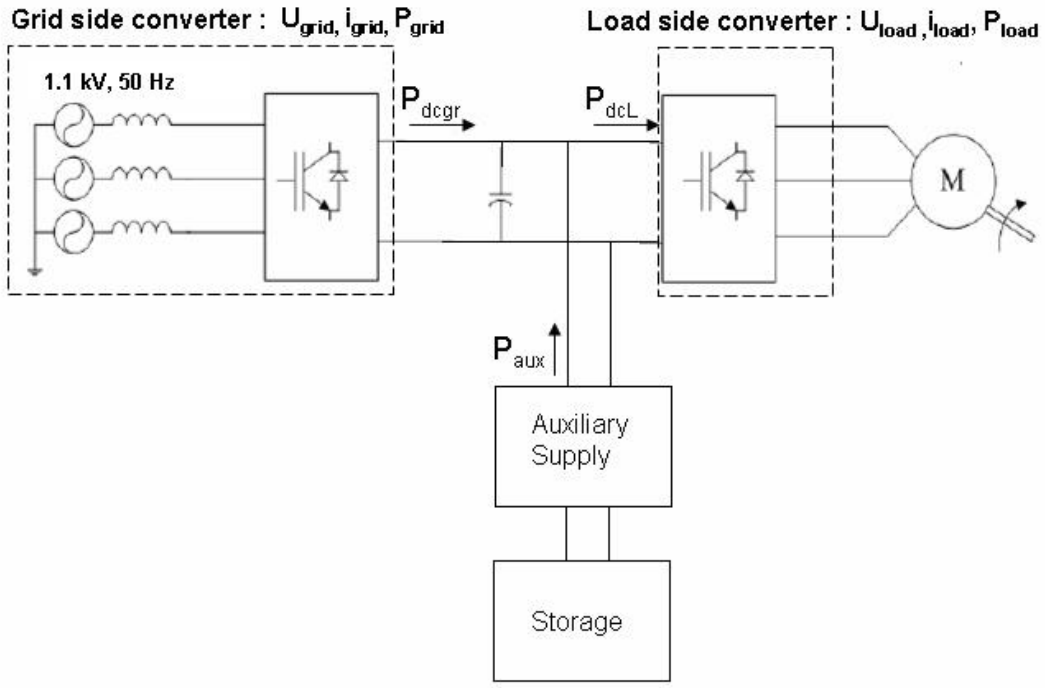

Figure 1.15 : MVDC system with auxiliary supply

The power balance for this configuration is given as

$$P_{dcL} = P_{dcgr} + P_{aux} \tag{1.5}$$

From the power balance it can be seen that the power transmitted to the load i.e. P_{dcL} remains unaffected because of the injection of extra current from the auxiliary supply.

1.8 Thesis Outline

Chapter 2 presents a quantitative analysis of the EdeA industrial plant. Actual values for power, voltage and currents will be given that will be used later in the research as a case study.
Chapter 3 focuses on the different storage methods and a comparison is given.
Chapter 4 will give an overview of the VSC-HVDC technology. The structure and the control system will be described in detail. A mathematical model of the control system is presented. The Siemens Power Link (SIPLINK) model will be presented and discussed. Also the current SIPLINK technology and practical information of the system as well as applications for it are presented in this chapter.
Chapter 5 will present the theory behind the interfacing of the storage method chosen in chapter 3.
Chapter 6 presents the case study and actual values for the used elements are calculated. Also the results of computer calculations of voltage sag mitigation by converter overrating and auxiliary supply are presented.
Chapter 7 will give simulation results for the designed SIPLINK system and industrial plant with different sags applied. Mitigation of these sags by converter overrating and by auxiliary supply is analysed.
Chapter 8 presents an overview of the costs involved in applying such an MVDC system to prevent power quality problems.
Finally, a summary is given and some suggestions for future research are pointed out in Chapter 9.

2. Quantitative analysis of EdeA industrial plant

Voltage sags are one of the most common occurrences in industrial power distribution systems. Although the duration of typical sags is between 10 – 500 milliseconds, and the depth of the sag is usually lower than 30% of the rated voltage value, this disturbance can trip the protections of an adjustable speed drive or introduce brief speed fluctuations which may damage the final product. This can lead to losses in revenue. With a system like SIPLINK in an industrial grid it will be possible to make use of the benefits like linking to a neighbouring network in the event of a load expansion or infeed failure. See chapter 4.4.3 for examples of SIPLINK applications. However with the adjustments described in chapter 1.7 it will also be possible to protect the load from voltage sags originating in the higher level supply grids. This chapter deals with two possible solutions for voltage sag mitigation. The first is the overrating of the converters. Usually the converter load current is close to the converter rated current. In case of a voltage sag there will be limited capability for the converters to supply the power necessary to the loads. By increasing the current limit i.e. overrating the system, it enables the converter to draw more current from the grid to try to maintain the power level of the load. The current limit setting is an important parameter in the design of an industrial power grid with VSC-HVDC links. There are three important parameters to be considered.

1. During steady state, the system should be able to supply any possible load
2. The starting of equipment should be supported i.e. normal overloads
3. The system must withstand internal and external faults which may lead to the interruption of the plant operation and/or damage to the equipment

Of course there is a limit to the overrating and this is defined in a great deal by the costs of the system. The second solution for voltage sag mitigation is increasing the rating of the DC link. This will be done by injecting extra current in the DC link from an auxiliary supply in the event of a voltage sag to maintain the DC link at its rated value. An appropriately sized energy storage device with proper interfacing will be used for that purpose. During a sag the storage device is used and the power is injected in the DC link. After the sag has cleared the storage device is to be charged back up to its initial state. To illustrate the actual power, voltage and current magnitudes that will be used for calculations further on in this thesis, an energy and power balance is given. The values for all components described in the previous paragraphs are calculated for the case of the EdeA substation. Voltage sag mitigation is introduced for the EdeA substation which is already described in chapter 1.5.1.
From Table 1.2 in section 1.3 it is clear that the most severe case to be investigated is that of a sag with 10 percent remaining voltage lasting 1 second. The maximum mitigation capability of any of the solutions provided is determined by this condition. To determine the power that is needed from the mitigation solution, the following parameters are introduced:

P_{grid} = The power supplied by the grid
$P_{grid,dip}$ = The power supplied by the grid during a voltage sag
P_{dc} = The power in the DC link
P_{aux} = The power provided by the mitigation solution
P_{load} = The power drawn by the load

These parameters are used in equations (2.1) to (2.5) for the calculation of the power supplied by the grid during a voltage sag. This ultimately leads to an equation for the power needed from any of the mitigation solutions.

During normal operation the power balance is given by

$$P_{load} = P_{grid} + P_{DC} \tag{2.1}$$

During a voltage sag the power balance is given by

$$P_{load} = P_{grid\_dip} + \frac{dE_{dc}}{dt} = V_{dip} I_{conv,rat} + \frac{\frac{1}{2} C_{DC} \Delta (V_{DC})^2}{\Delta t} \tag{2.2}$$

In this equation $P_{grid,dip}$ is defined by the remaining voltage during a voltage sag i.e. V_{dip} (Equation (2.3)) multiplied by the maximum current of the converter $I_{conv,rat}$.
ΔV_{DC} is the difference between the converter rated DC voltage and the minimum allowable DC voltage.

Remaining voltage during voltage sag V_{dip} is defined by:

$$V_{dip} = V_{grid} \times dip\% \tag{2.3}$$

Where *dip%* is the percentage of the remaining grid voltage and V_{grid} is given.

To determine the effect of overrating on the system, (2.2) can be rewritten, using (1.4) i.e.

$$P_{load} = P_{grid\_dip} + \frac{dE_{dc}}{dt} = V_{dip} k_{or} I_{load} + \frac{\frac{1}{2} C_{DC} \Delta (V_{DC})^2}{\Delta t} \tag{2.4}$$

For mitigation with an auxiliary supply, equation (2.2) is written as

$$P_{load} = P_{grid\_dip} + \frac{dE_{dc}}{dt} = V_{dip} I_{conv,rat} + \frac{\frac{1}{2} C_{DC} \Delta (V_{DC})^2}{\Delta t} + P_{aux} \tag{2.5}$$

where P_{aux} is the power originating from the auxiliary supply.

During this sag condition the power for the EdeA network connected by SIPLINK is given graphically by Figure 2.2. For this thesis it is chosen that the converters are overrated by 10 percent. This means that the rated current of the converter is 10 percent higher than the load current. During a voltage sag the converter operates at its maximum/rated current. This value is chosen in costs point of view. As mentioned in the previous chapter, the higher the system is overrated, the higher the costs because of the use of more and/or larger converters.

Figure 2.1 and Figure 2.2 illustrate graphically the voltage, current and power conditions that hold during a worst case voltage sag. The worst case voltage sag is defined as a 90 percent voltage sag during 1 second.

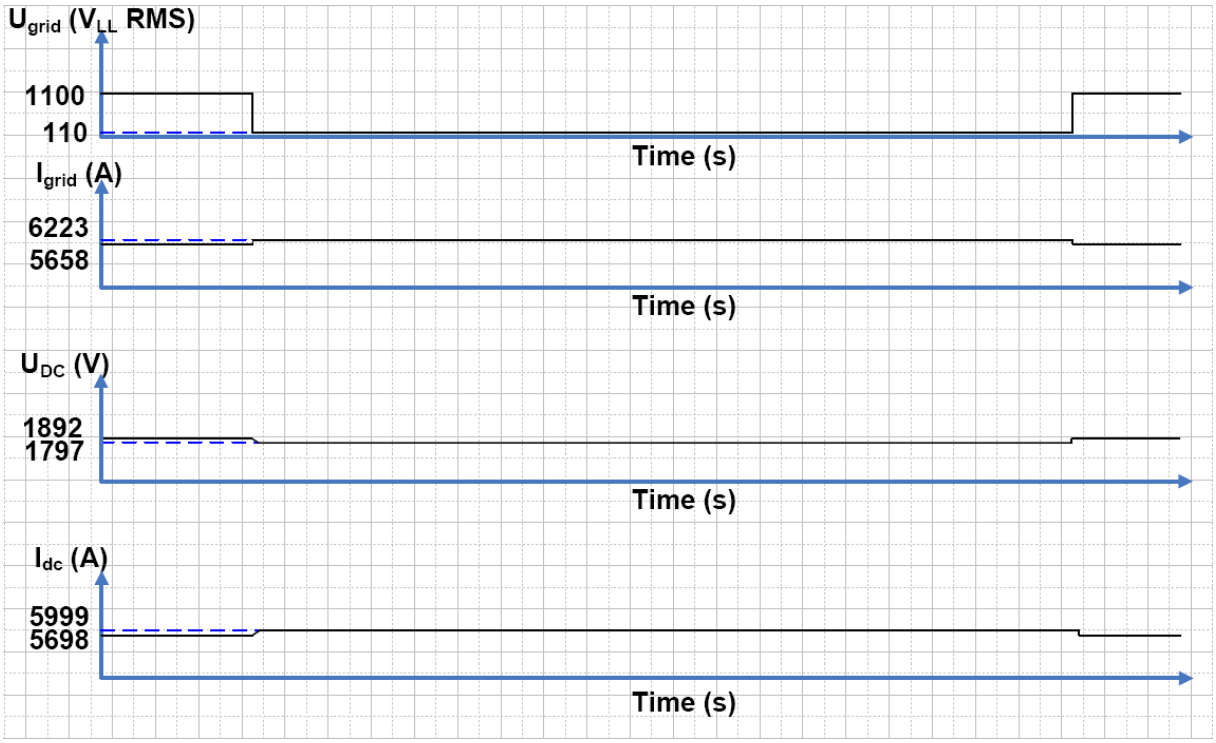

Figure 2.1: Voltages and currents during a worst case voltage sag

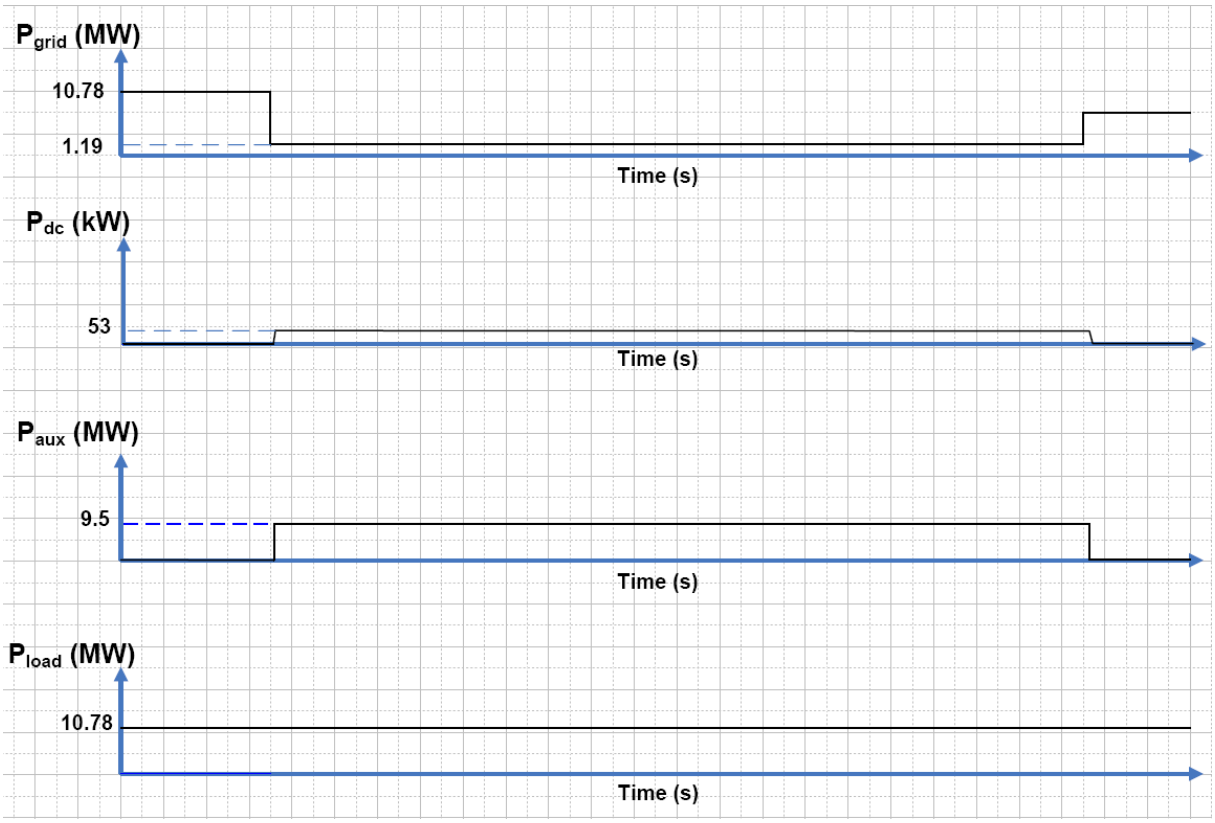

Figure 2.2: Power balance during a worst case voltage sag

From the above figures it is apparent that during the worst case voltage sag the power supplied to the grid is 1.19 MW. The power from the DC link is relatively small because of the small capacitor used. A small capacitor is needed for fast converter reaction times.

Using equation (2.5) different values for P_{aux} can be found by varying the voltage sag magnitude and the duration of the sag. The values are presented graphically in Figure 2.3. It is apparent from this figure that the longer and the deeper the sag, the more energy is needed to support the load.

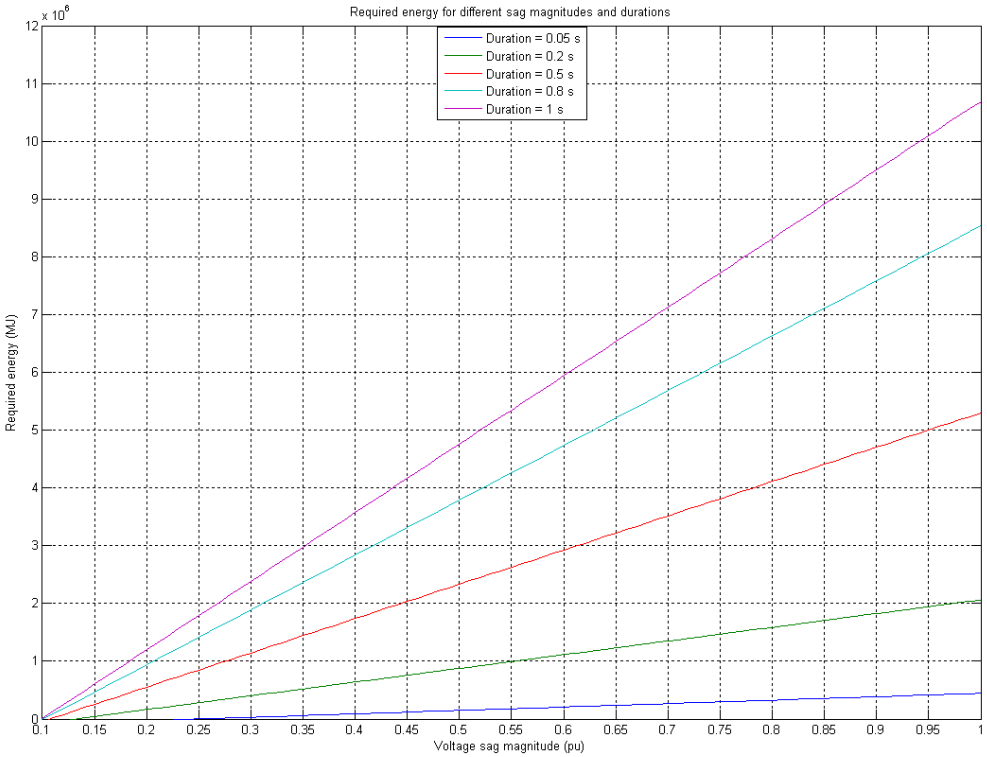

Figure 2.3: Required compensation energy for different sag magnitudes and durations

3. Storage Methods for Energy Compensation

3.1 Storage Devices

To store the energy that is needed for the boost converter compensation circuit a number of devices can be used. Each with their own advantages and disadvantages. The storage methods can be divided into direct and indirect storage methods. Indirect storage methods convert the energy from electrical to a different form. In direct storage devices the energy is stored without transforming the energy to a different form. Examples of indirect storage methods are compressed air, heat, hydrogen or rotating flywheels. Most of these storage methods are not very efficient because much of the energy is lost in the conversion process. The direct storage category can be divided in electrical and magnetic storage. The different energy storage methods available grouped by direct and indirect storage and by their specific storage reservoir is shown in Figure 3.1. The application of an energy storage technology is characterized by two factors. The first factor is typical to the storage method itself, and that is the amount of energy that can be stored in the device. The second factor is the rate at which the energy can be transferred into or out of the storage device.

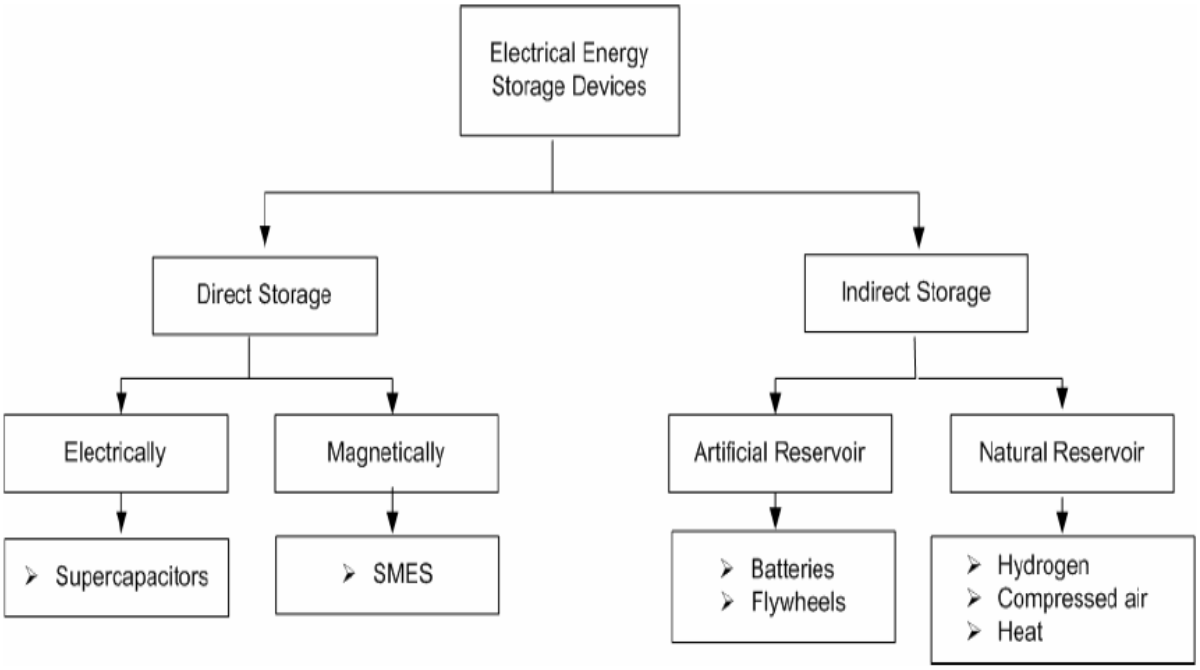

Figure 3.1: Electrical energy storage methods[11]

The "Ragone plot" from Figure 3.2 shows the power and energy classification of each storage method. This type of graph presents the power densities of the various energy storage devices, measured along the vertical axis is set against their energy density, measured along the horizontal axis.

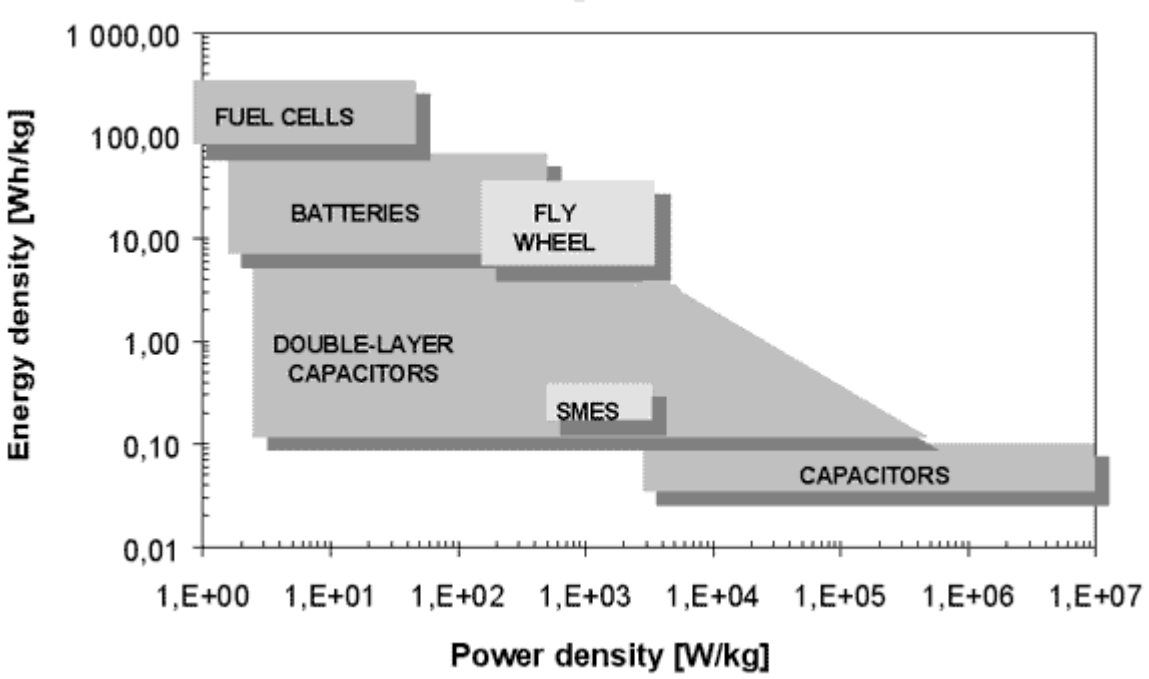

Figure 3.2 Ragone plot of energy storage devices, adapted from [12]

Next an elaboration on the more proven storage technologies i.e. battery, flywheel and supercapacitor follows.

1. **Battery**

   Energy is stored electrochemically in batteries. " All battery systems are made up of a set of low voltage/power cells connected in series to achieve the desired terminal voltage, and in parallel to provide the desired power rating" [11]. There are currently various battery technologies available. Lead acid batteries are the most common due to cost issues but currently lithium ion is becoming more popular every day. Batteries characterise themselves by their high energy density and high energy capability, life span and lower initial cost. The voltage profile of a battery is flat. This means that the voltage remains nearly constant until the battery is depleted. This has benefits for control of power electronics. Due to their chemical kinetics, batteries cannot handle high power levels for long time periods. Also rapid discharge cycles may shorten the battery life leading to early replacement. Because of increasing environmental awareness batteries, which contain hazardous materials and generate toxic gasses during the charge and discharge cycles, are becoming more costly in their use. This is due to the additional costs of disposal of the hazardous materials that are implied by ever stricter environmental regulations.

   Advantages: low cost

   Disadvantages: short cycle life, need maintenance and replacement, weight

2. **Flywheel**

   A flywheel works on the principal of a rotating mass being accelerated to a very high speed and maintaining the energy as rotational energy. The rotating mass is coupled to a motor-generator set through a shaft. A schematic of the flywheel components is shown in Figure 3.3. In many applications a power electronic converter is connected to the motor-generator s to provide power for a wide range of applications.

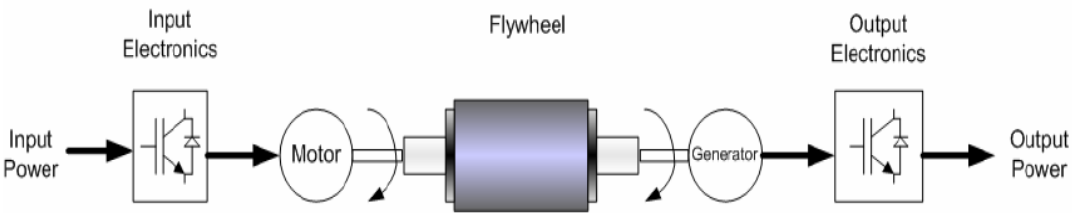

Figure 3.3: Flywheel system schematic[11]

The stored energy depends on the moment of inertia of the rotating mass and on the rotational velocity of the flywheel. See equation (3.1).

$$E = \frac{1}{2} J \omega^2 \tag{3.1}$$

In this equation E is the kinetic energy stored, J is the moment of inertia of the rotating mass and ω is the rotational velocity of the flywheel. When the mass has a cylindrical shape, which is usually the case, the moment of inertia can be calculated using equation (3.2).

$$J = \frac{r^2 ml}{2} \tag{3.2}$$

Where m is the mass of the cylinder, r is the radius and l is the length.

By decreasing the speed of the flywheel, the rotational energy stored can be converted back to electrical energy. In this case the motor-generator set operates as a generator and the power can then be transferred to the outside.
Charging of the flywheel occurs during acceleration of the rotational velocity. The motor-generator set then works as a motor. From (3.1) it follows that the energy storage capability of the flywheel can be improved by either increasing the moment of inertia, increasing the rotational velocity of the mass or a combination of both.

High power flywheels are being developed through the increase of the moment of inertia. This is achieved by increasing the radius of the spinning mass and constructing the mass using materials as iron or steel. In this manner rotational velocities of up to 10000 rpm can be achieved [11]. This approach is commercially attractive because standard electric motors, mechanical components and power electronics can be used making for easy implementation. The second approach is based on the constructing rotors with a smaller radius and constructing them from composite materials. This results in smaller moments of inertia but allow for rotational velocities as high as 100 000 rpm [11]. The second method produces lighter and smaller flywheels with equal or increased storage capability compared to the previous technology.

In the flywheel technology losses are mainly produced by air drag and bearing losses. These become more important with increasing velocity. To reduce the air drag losses, flywheels are mounted in near vacuum containers. Bearing losses are reduced by mounting the flywheels on magnetic bearings. With the rotational losses nearly eliminated, the flywheel can have high charge and discharge efficiency leaving the transfer of peak power dependant only on the design of the motor-generators and the converters.

Strong containment vessels are required as a safety precaution because of the chance for "flywheel explosion". Flywheel explosion means the flywheel shatters due to the tensile strength of the flywheel being exceeded because of the high centrifugal forces produced by the rotational mass. This of course increases the total mass of the system and the extra weight subsequently brings with it a reduction of the energy density [W/kg]

Advantages: Durable, not affected by temperature changes as batteries, less damaging to the environment because of the use of inert materials. The exact amount of stored energy can be determined by measuring the rotational velocity.

Disadvantages: Stationary, requires much safety precautions due to the forces produced by the rotating mass. This adds weight thus reducing the energy density [W/kg].

3. Supercapacitor

"Supercapacitors, also known as ultracapacitors or electrochemical capacitors, utilize high surface area electrode materials and thin electrolytic dielectrics to achieve capacitances several orders of magnitude larger than conventional capacitors." [13]
With these material properties the supercapacitor can have higher energy densities while keeping the high power density which is characteristic for conventional capacitors.

Standard capacitors are made of two conducting electrodes with in between an insulating dielectric material. They are governed by the following equations:
Capacitance C is defined as the ratio of stored (positive) charge Q to the applied voltage V:

$$C = \frac{Q}{V} \tag{3.3}$$

In a conventional capacitor, the capacitance C can also be described by (3.4). Here C is directly proportional to the surface area A of each electrode and inversely proportional to the distance D between the electrodes:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{D} \tag{3.4}$$

Where ε_0 is the dielectric constant or permittivity of free space and ε_r is the dielectric constant of the insulating material. The energy E stored in a capacitor is given by equation (3.5):

$$E = \frac{1}{2} C V^2 \tag{3.5}$$

"The internal components of the capacitor (e.g., current collectors, electrodes and dielectric material) also contribute to the resistance quantity which measured in aggregate by a quantity know as the equivalent series resistance (ESR)." [13]

The basic principles of a conventional capacitor given by the previous equations also hold for a supercapacitor. Supercapacitors have however larger surface areas and thinner dielectrics.

This increases the distance D between the electrodes leading to an increase in capacitance and energy according to (3.4) and (3.5).
A schematic of the supercapacitor is given in Figure 3.4.

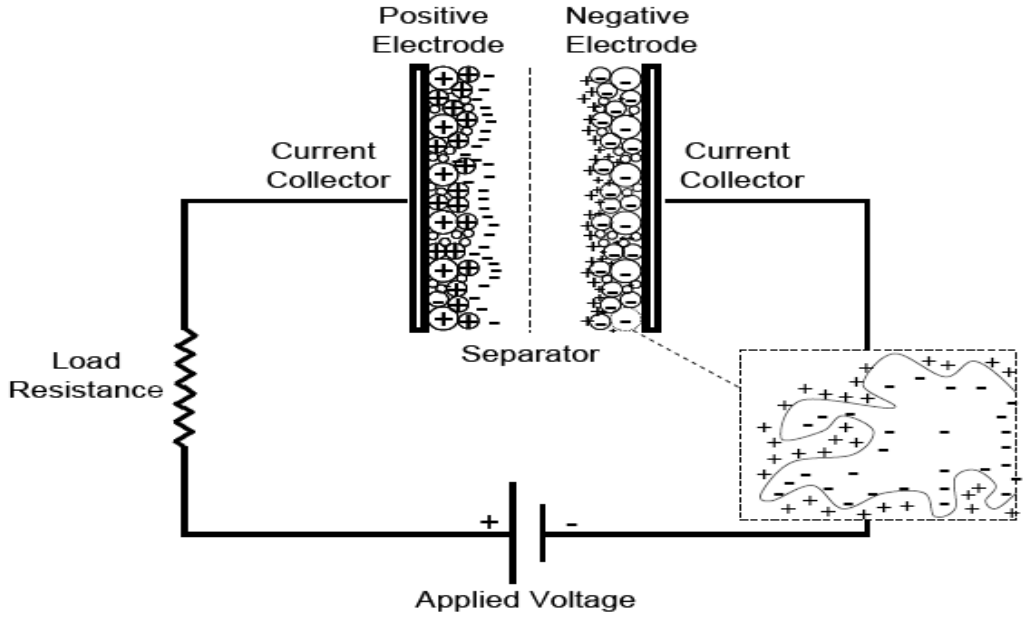

Figure 3.4: Schematic of an electrochemical double-layer capacitor, adapted from [13]

Advantages: Low impedance compared to battery, quick charge/discharge, high life cycle (up to 500000 cycled times), operating temperature range (-30˚ C - 70˚ C)
Disadvantages: Linear discharge voltage prevents use of the full energy spectrum because of the limited operating voltage, low energy density, cells have low voltages: 1-3 V for all technology, high self discharge, voltage balancing needed when connecting multiple capacitors in series.

3.2 Comparison and conclusion of energy storage technologies

From the previous discussion it follows that energy storage methods differ in their energy densities, power densities and other important parameters as equivalent series resistance and charge and discharge time. A comparison of the different technologies is therefore necessary in order to accomplish the highest performance for each application. From Figure 3.2 it is clear that there is a big difference between the different storage devices discussed. When energy density is an important factor, batteries appear to be the better choice compared to flywheels and supercapacitors according to Figure 3.2. Another important parameter to be considered is the power density, which measures the energy stored per unit of weight of the device. Here the supercapacitor seems to be the better option as it is better able to deliver pulsating currents due to its fast charge and discharge capabilities.
Also important to consider in the comparison of energy storage devices is the equivalent series resistance value. A high value means higher losses and more voltage drop at the moment when the load demands current. When comparing this parameter, the supercapacitor appears to be more convenient with ESR's in the range of 10 times lower than that of batteries and comparable to flywheels [13]. Size constraints presented by modern power electronic

applications make the volume and weight of the storage devices also an important parameter to take into consideration. Having a smaller volume and weight, supercapacitors offer a better alternative than batteries and flywheels. Flywheels are also lighter than batteries because of the use of composite materials, but their volume is bigger because of the use of different protective measures.
Costs are also important in the comparison between the different storage devices. In this case batteries appear to have the lowest initial cost because it is a proven technology. But this is not including the maintenance costs. Supercapacitors and flywheels have higher initial costs but require little maintenance during all their life span as compared to batteries. The life span of batteries is averaged to be at five years. But if subjected to extreme conditions such as low/high temperatures and pulsating current loads, the lifetime is estimated to be at three years [13]. Supercapacitors have a life span of about ten years but this depends on the actual charge discharge cycles it is subjected to. The normal charge discharge cycle of a supercapacitor can be over 1 million. This charge discharge cycle is independent of environmental conditions or because of pulsating loads. The life span of flywheels is also independent of the environmental conditions and of the type of load that is connected to its terminals [13]. Their life span is estimated to be around 20 years.
For this comparison it is imperative to consider that supercapacitors and flywheels are not mature technologies. Therefore their ongoing continuous improvement will lead to reduction of their costs and increase in energy density comparable to batteries. Though batteries are a proven technology and are widely used in power electronics, few improvements have been done to improve their power densities or reduce their size and weight. The chemical compositions also pose a limitation to the lowering of the ESR or to improve their transient response.
From this comparison supercapacitors appear to be suitable to be used in this thesis research in combination with power electronics to provide voltage sag ride through. Despite their low energy density it presents a good advantage over the two energy storage devices for this application. This advantage is due to the high power density. Voltage sags are in the order of seconds. The load requires then a pulsating burst of power and the supercapacitor is the best candidate to deliver the pulsating current needed. From the point of view of internal losses supercapacitors offer the better alternative because of their very low equivalent series resistance. See Table 3.1 for a comparison of the different storage devices if all the stored energy is needed in 60 seconds.

Storage device	peak power [W/kg]	power 60'' [W/kg]	life [number of deep discharges]	cost [€/kW$^{60''}$]	availability
Advanced battery	600	100	<300	50-100	commercial
Flywheel	300	130	>100.000	400-800	prototypes
Supercapacitor bank	3500	250	>10.000	100-120	pre-industrial

Table 3.1: Comparison of storage devices for complete discharge in 60 seconds [14]

4. Operation of VSC-HVDC and Siemens Multifunctional Power Link Design

This chapter will give an overview of the VSC-HVDC technology. The structure and the control system will be described in detail in Sections 4.1 up to 4.3. A mathematical model of the control system is presented in these sections. The Siemens Power Link (SIPLINK) model will be presented and discussed in Section 4.4. Also the current SIPLINK technology and practical information of the system as well as applications for it are presented in this section.

4.1 Operation of VSC- HVDC

"The fundamental operation of the VSC-HVDC may be explained by considering each terminal as a voltage source connected to an AC transmission network via series reactors" [10]. A DC link connects the two terminals as can be seen in Figure 1.8. One converter side is zoomed in and shown in Figure 4.1.

VSC converters are theoretically capable of producing any waveform depending only on the choice of the direct voltage level and the switching frequency. To generate these waveforms Pulse Width Modulation (PWM) is used.

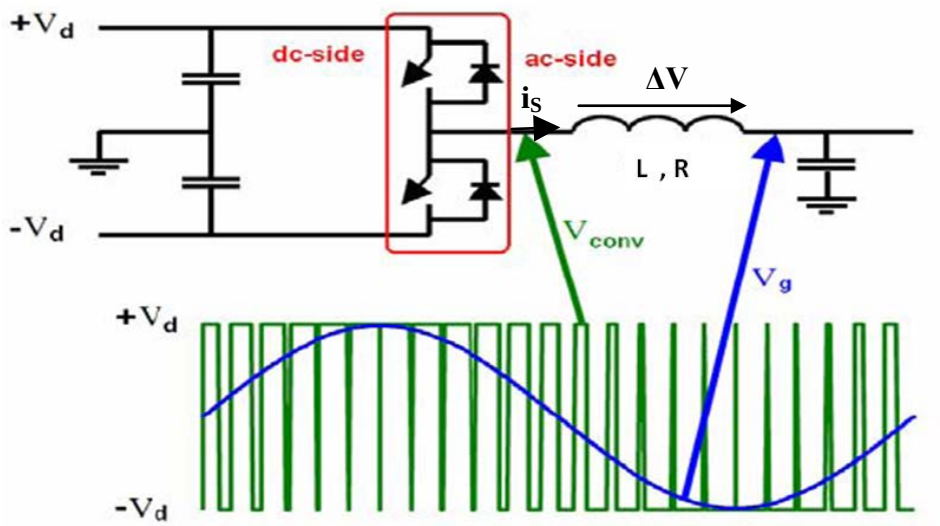

Figure 4.1: Schematic representation of one VSC converter[15]

The amplitude, the phase and the frequency of the VSC bridge can be controlled independently from each other. The instantaneous phase voltage which relates the aforementioned independently controlled parameters is described by the following equation.

$$V_{conv} = \frac{1}{2} V_{DC} m_a \sin(\omega t + \delta) + \text{harmonic terms} \tag{4.1}$$

where m_a is the modulation index, a number between 0 and 1, and is defined by the ratio of the peak value of the modulating wave and the peak value of the carrier wave; ω is the

fundamental frequency, δ is the phase shift of the output voltage depending on the position of the modulation wave[10].
By adjusting m_a and δ any combination of voltage magnitude and phase shift in relation to the fundamental-frequency voltage in the AC system can be created.
This is called direct control. The resulting voltage drop ΔV across the inductance L can be varied to control the active and reactive power flows. The phasor representation for the fundamental frequency for a VSC operating as an inverter is shown in Figure 4.2. Here the converter is supplying reactive power to the AC system.

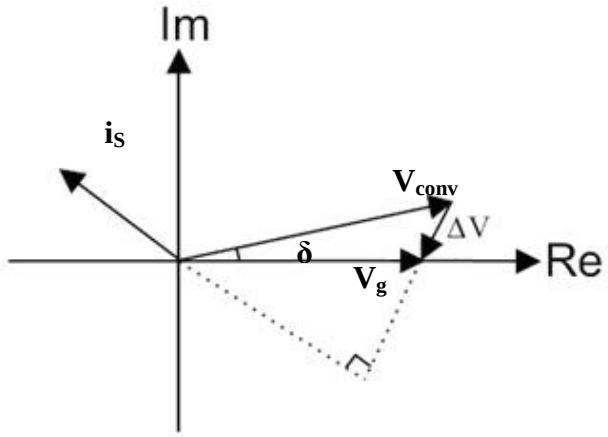

Figure 4.2: Phasor diagram of VSC inversion

By changing the phase angle δ between the fundamental frequency converter voltage V_{conv} and the grid voltage V_g, the active power flow between the converter and the AC system can be controlled.
The active and reactive power are calculated according to (4.2) and(4.3).

$$P = \frac{V_g V_{conv}}{\omega L} \sin \delta \tag{4.2}$$

$$Q = \frac{V_g (V_g - V_{conv} \cos \delta)}{\omega L} \tag{4.3}$$

From equation (4.3) it can be seen that the reactive power flow is controlled by the amplitude of V_g. The amplitude of V_g in turn is controlled by the width of the pulses of the converter bridge. The DC voltage determines the maximum fundamental-frequency voltage from the converter. The sign of the active and reactive power depend on the phase and the amplitude of the converter bridge voltage. Figure 4.3 represents the situation when the line voltage V_g is constant. The location of the V_{conv} phasor determines whether the converter is in rectifier or inverter mode.

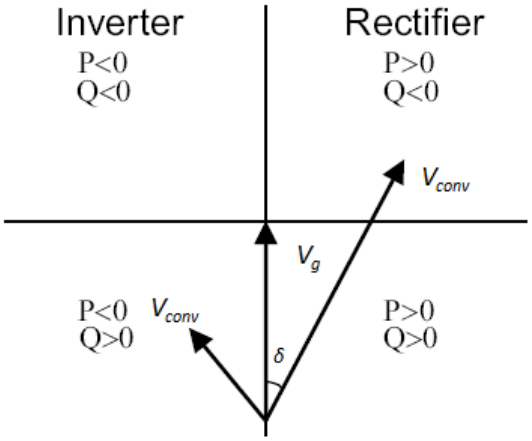

Figure 4.3: Phasor diagram (fundamental) and direction of power flows, adapted from [10]

In Figure 4.3, if the grid side voltage V_g leads the converter bridge voltage V_{conv}, the active power flows from the AC network to the converter. The converter is in rectifier mode.

With VSC-HVDC it is possible to transfer active power in both directions. This active power is equal on the AC side as well as the DC side in steady state. In order to accomplish this, one converter should control the DC voltage and the other should control the active power transmitted. Thus for proper operation of the system, there should always be DC voltage control and active power control done by either one of the converters. The controllable active power can be transferred in both directions equally and is only limited by the power rating of the converter. "The reactive power generation and consumption can be used for compensating the needs of the connected network."[10]

4.2 Design of DC capacitor

To control the input currents to be sinusoidal with a pulse width modulated signal with $m_a \leq 1$, the DC voltage should be appropriately chosen. PWM switching actions create harmonics in the current flowing to the DC link. Therefore care must be taken when designing the DC side capacitor. The harmonics in the currents cause a ripple in the DC voltage and the size of the DC side capacitor and the switching frequency determines the magnitude of this ripple. Apart from the steady state operation, the design of the DC capacitor should focus on the operation of the system during disturbances in the AC system. During disturbances large power oscillations may occur on the AC side which will in turn lead to oscillations in the DC voltage which could lead to overvoltages stressing the valves. The capacitor should thus provide an energy buffer to keep the power balance during transients. A small capacitor results in faster converter response. The DC side capacitor is characterized by a time constant given by equation (4.4) [3].

$$\tau = \frac{\frac{1}{2} C_{DC} U_{DCN}^2}{S_N} \tag{4.4}$$

Here U_{DCN} is the rated DC voltage and S_N is the nominal apparent power of the converter. "The time constant is equal to the time constant needed to charge the capacitor from zero to rated voltage U_{DCN} if the converter is supplied with a constant active power equal to S_N" [3].

Choosing a small time constant can satisfy small ripple and small transient overvoltages on the DC voltage. A relatively small time constant also allows for fast active and reactive control. Controller speed of less than 5ms is not practical because the connection will not react. This is true only for the control of the active power since the reactive power is generated locally and does not require the DC link [10].

4.3 Control system of the VSC- MVDC

The control system of the VSC-HVDC is a cascade control and typically consists of a faster vector controller. This vector controller is completed by additional controllers which supply the references for the vector controller. The vector controller is thus the inner loop and the additional controllers are the outer loop. The values being controlled are the direct axis "d" and the quadratic axis "q" components of the converters at both sides. The control modes are: in the "d" axis, either the active power flow at the PCC or the pole-to-pole DC voltage; in the "q" axis, the reactive power flow at the PCC [16]. Also an AC voltage control can be added. See Figure 4.4. To determine the "d" and "q" components first a Clark transformation is performed on the three-phase quantities. This transforms these quantities to space vector components α and β (real and imaginary part). Next the Park transformation is performed which computes the direct axis "d" and the quadratic axis "q" (two axis rotating reference frame) from the α and β quantities. These quantities are fed to the outer controllers which in turn calculate reference values for the inner current controller. The outer controllers include the DC voltage controller, the AC voltage controller, the active power controller, the reactive power controller or the frequency controller. The reference value for the active current can be derived from the DC voltage, the active and the frequency controller whereas the reference value for the reactive current can be obtained from the AC voltage and reactive power controller. In these controllers integrators can be used to eliminate steady state errors. Obviously not all controllers can be used at the same time but depending on the application different kinds of controllers can be chosen. In that case each of the controllers generates a reference value for the inner current controller and the inner current controller calculates the voltage drop over the converter reactor that will lead to the desired current. In Figure 4.4 an overview is given of the overall control structure of the VSC-HVDC.

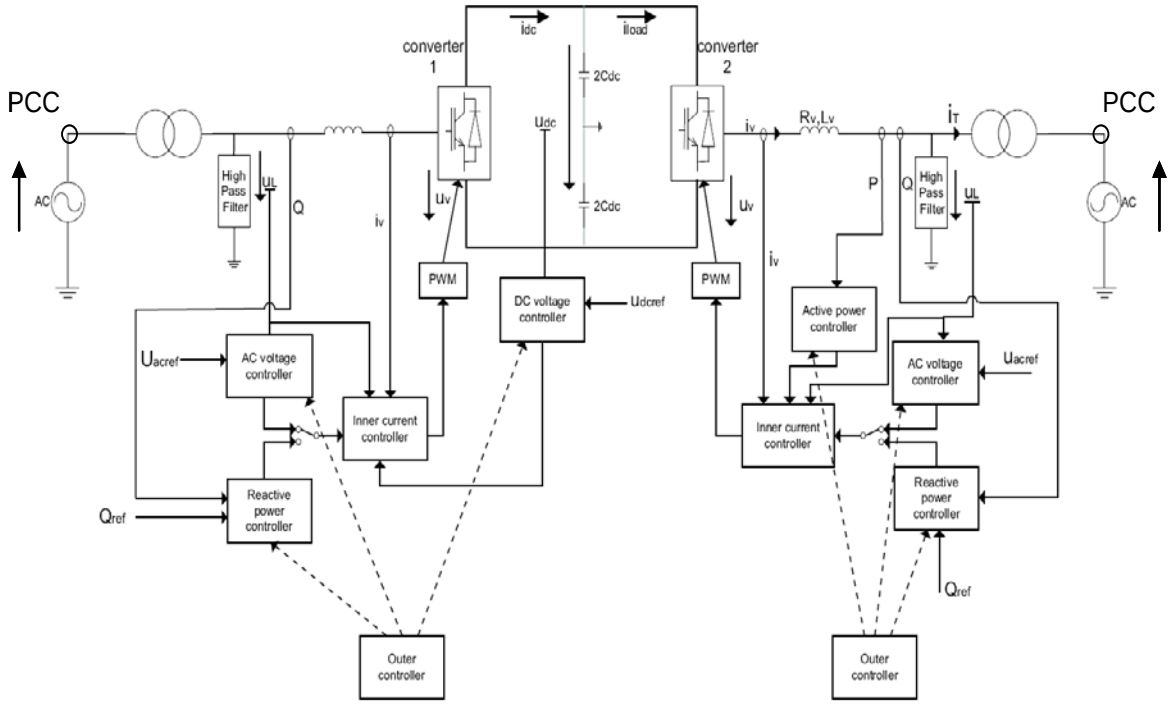

Figure 4.4: Overall control structure of the VSC-HVDC[10]

4.3.1 The inner current controller

To better explain the mathematics associated with the inner current controller, Figure 4.1 is used for illustrative purposes. This is part of Figure 4.4 zoomed in. The inner current controller loop is based on the basic relationships for this model and can be implemented in the *dq*-frame. The inner current controllers consist of a PI regulator, a feedforward control of the AC voltage and a decoupling factor which is current depending. When neglecting waveform distortion, simple control algorithms can be derived for balanced system operation because the *dq* voltages are constant.

The process shown in Figure 4.5 is followed to obtain reference values for the converters.

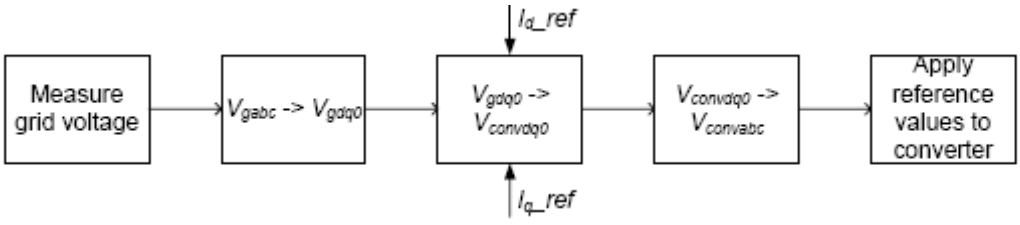

Figure 4.5: Schematic overview of current control[17]

For each of the phases a,b and c equation (4.5) holds:

$$V_g - V_{conv} = L\frac{di}{dt} + Ri \tag{4.5}$$

The voltages over the reactor $R+j\omega L$ are described by the differential equation:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} V_{conva} \\ V_{convb} \\ V_{convc} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix} \tag{4.6}$$

The transformation between the *abc*-components and the *dq0*-components is defined by [18]

$$V_{abc} = \mathbf{P}V_{dq0} \tag{4.7}$$

and

$$I_{abc} = \mathbf{P}I_{dq0} \tag{4.8}$$

In which the orthogonal Park transformation is used and is given by the matrix **P**

$$\mathbf{P} = \sqrt{\frac{2}{3}}\begin{pmatrix} \frac{1}{2}\sqrt{2} & \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \frac{1}{2}\sqrt{2} & \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \frac{1}{2}\sqrt{2} & \cos(\theta) & -\sin(\theta) \end{pmatrix} \tag{4.9}$$

with $\mathbf{P}^{-1} = \mathbf{P}^{T}$

The angle θ is measured by a phase-locked loop (PLL) system. In Simulink this is done by the Phase Locked Loop block. “The Phase Locked Loop block measures the system frequency and provides the phase synchronous angle θ (more precisely [sin(θ), cos(θ)]) for the dq Transformations block. In steady state, sin(θ) is in phase with the fundamental (positive sequence) of the α component and phase A of the PCC voltage (U_{abc}).”[16] The voltages v_{convd} and v_{convq} are calculated by the current controller after the transformation to *dq*-quantities. To do this first the network equations of the ac side will be derived with Kirchhoff’s laws. In the next section the following vector representations are used

$$V = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{4.10}$$

And

$$V' = \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \tag{4.11}$$

The transformation from three phase quantities to the *dq*-frame is given by

$$V = \mathrm{P}V' \tag{4.12}$$

The same holds for the current components. In the following equations the subscripts *conv* represent the converter side and g represents the grid side components.

Applying Kirchhoff's laws and applying the Park transformation as performed in [17] results in:

$$
\begin{aligned}
V_g &= RI + L\frac{d}{dt}(I) + V_{conv} \\
\mathbf{P}V_g^{'} &= R\mathbf{P}I^{'} + L\frac{d}{dt}(\mathbf{P}I^{'}) + \mathbf{P}V_{conv}^{'} \\
V_g^{'} &= \mathbf{P}^{-1}R\mathbf{P}I^{'} + \mathbf{P}^{-1}L\frac{d}{dt}(\mathbf{P}I^{'}) + V_{conv}^{'} \\
V_g^{'} &= R^{'}I^{'} + \mathbf{P}^{-1}L\frac{d\mathbf{P}}{dt}I^{'} + \mathbf{P}^{-1}L\mathbf{P}\frac{dI^{'}}{dt} + V_{conv}^{'} \\
V_g^{'} &= R^{'}I^{'} + L^{'}\mathbf{P}^{-1}\frac{d\mathbf{P}}{dt}I^{'} + L\frac{dI^{'}}{dt} + V_{conv}^{'} \\
\begin{bmatrix} v_{gd} \\ v_{gq} \\ v_{g0} \end{bmatrix} &= \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} 0 & -\omega L & 0 \\ \omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} v_{convd} \\ v_{convq} \\ v_{conv0} \end{bmatrix}
\end{aligned}
\tag{4.13}
$$

The VSC is connected to the grid through a ΔY-transformer with a grounded converter-sided Y- winding and ungrounded star point. The delta winding at the grid side makes it impossible for the zero-sequence current to flow and thus it is neglected. The remaining equations are as follows when choosing the *dq*-currents as state variables:

$$
\begin{aligned}
\frac{di_d}{dt} &= \frac{1}{L}v_{gd} - \frac{R}{L}i_d - \omega i_q - \frac{1}{L}v_{convd} \\
\frac{di_q}{dt} &= \frac{1}{L}v_{gq} - \frac{R}{L}i_q + \omega i_d - \frac{1}{L}v_{convq}
\end{aligned}
\tag{4.14}
$$

The terms ωi_q and ωi_d cause a cross coupling between the two state variables. These will be regarded as external disturbances and are fed forward in the current controller. Next two new control inputs are introduced as described by [17]:

$$
\begin{aligned}
x_d &= v_{gd} - \omega L i_q - v_{convd} \\
x_q &= v_{gq} + \omega L i_d - v_{convq}
\end{aligned}
\tag{4.15}
$$

Following from the original equations:

$$
\begin{aligned}
x_d &= (sL + R)i_d \\
x_q &= (sL + R)i_q
\end{aligned}
\tag{4.16}
$$

where s is the Laplace-operator. From equation (4.15) two independent first-order models are created which can be controlled using PI-regulators. The currents i_d and i_q from equation (4.16) are the input values to the current controller. These are measured values from the system. The currents are compared to the reference currents dictated by the outer controllers. The PI regulators regulate the error to zero and produce the values x_d and x_q from equation (4.16) which in turn are used to calculate v_{convd} and v_{convq}. The final result of the current controller is depicted in Figure 4.6.

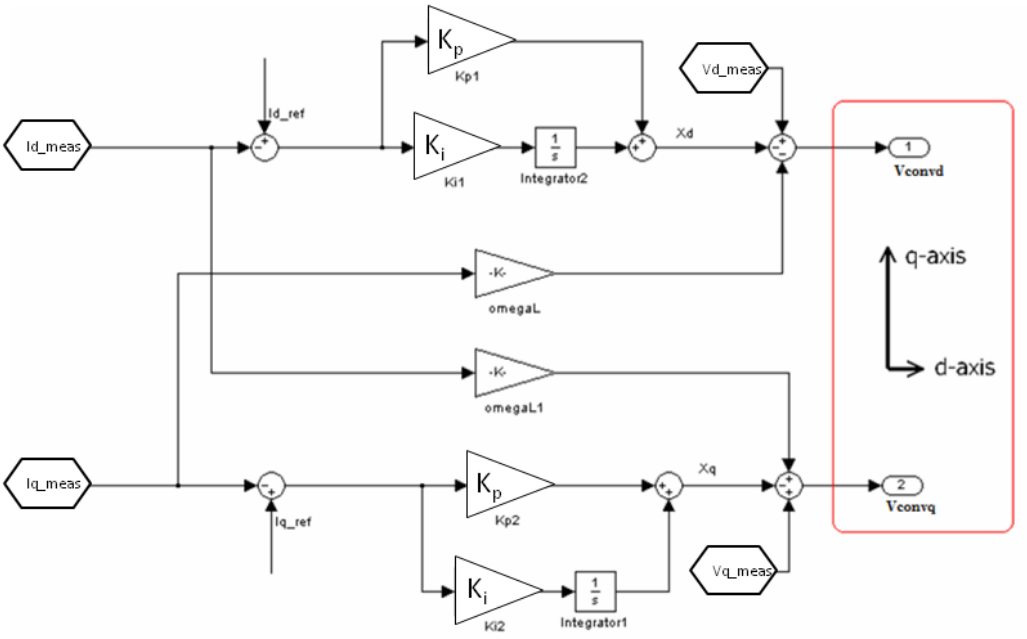

Figure 4.6: Inner Current controller, adapted from[17]

The total VSC with its corresponding inner and outer controllers is depicted in Figure 4.7.

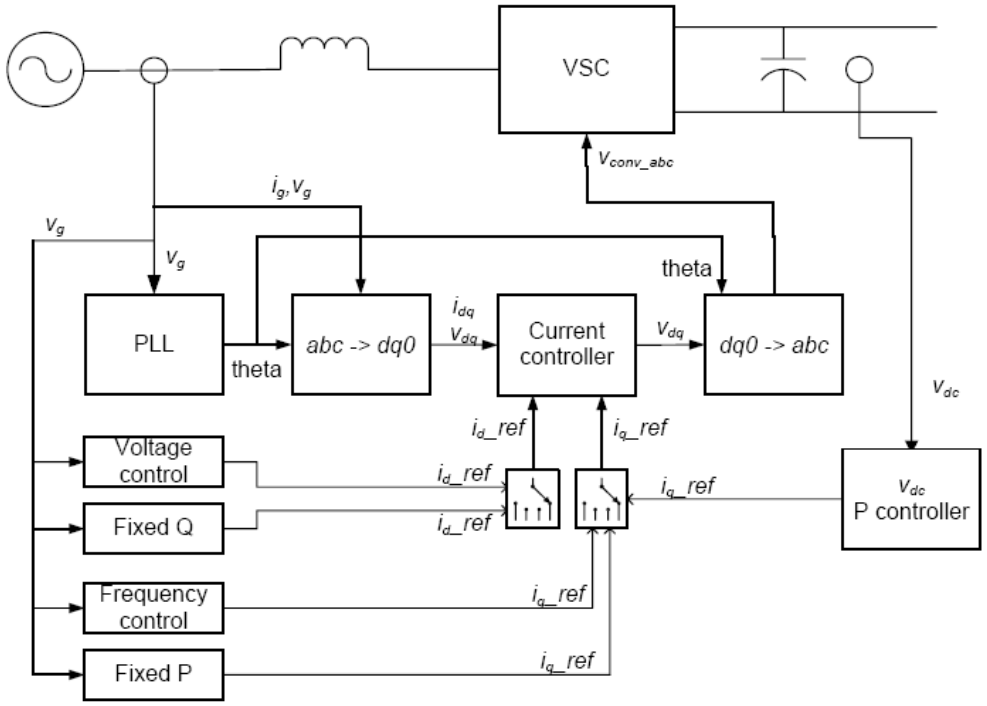

Figure 4.7: System and controller overview[17]

4.3.2 The outer controllers

This paragraph presents a brief summary of all outer controllers with their corresponding equations. For a more detailed explanation the author refers the reader to [10].

DC voltage controller

The phase values returned by the Simulink PLL block are

$$\begin{aligned} v_{gd} &= V \\ v_{gq} &= 0 \end{aligned} \tag{4.17}$$

Where V is the amplitude of the phase voltage. The instantaneous active and reactive power $P_{ac(dq)}$ and $Q_{ac(dq)}$ in the dq-frame are then given by:

$$\begin{aligned} P_{ac(dq)} &= v_{gd} i_{convd} + v_{gq} i_{convq} \\ &= v_{gd} i_{convd} \end{aligned} \tag{4.18}$$

$$\begin{aligned} Q_{ac(dq)} &= v_{gd} i_{convq} - v_{gq} i_{convd} \\ &= v_{gd} i_{convq} \end{aligned} \tag{4.19}$$

Also

$$P_{dc} = v_{dc} i_{dc} \tag{4.20}$$

The response of the inner current controller is very fast compared to the dc voltage controllers. The currents may thus be assumed to be equal to their reference values. The expressions for active and reactive power will then be:

$$P_{ac(dq)} = v_{gd} i^*_{convd} \tag{4.21}$$

$$Q_{ac(dq)} = v_{gd} i^*_{convq} \tag{4.22}$$

If the converter losses and the losses in the reactor can be neglected, the power transmitted is

$$P_{ac(dq)} = v_{gd} i_{convd} = P_{dc} = v_{dc} i_{dc} \tag{4.23}$$

Equating (4.23) gives:

$$i_{dc} = \frac{v_{gd} i^*_{convd}}{v_{dc}} \tag{4.24}$$

Unbalance between ac and dc power will lead to a change in voltage over the dc-side capacitor. The equation for the dc voltage over the capacitor is:

$$C_{dc} \frac{d}{dt} v_{dc} = i_{dc} - i_{load} \tag{4.25}$$

Where i_{load} is the current through the dc cable or line, that flows into the load side converter as shown in Figure 4.4. The resulting block diagram of the dc voltage controller is illustrated in Figure 4.8.

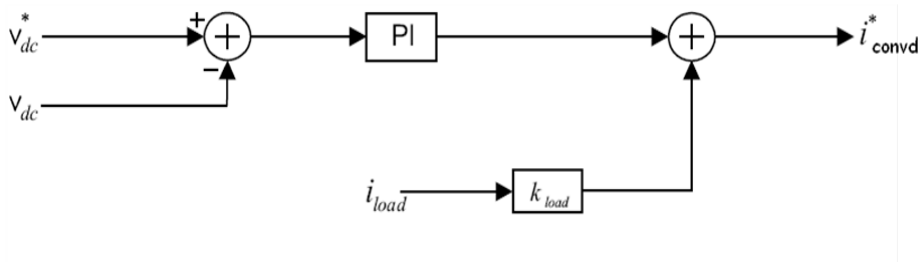

Figure 4.8: DC voltage controller, adapted from [10]

Here the controller measures the difference between the reference DC voltage and the actual DC voltage and controls the reference current via a PI controller. In this controller k_{load} is an extra feed forward term that allows for convergence of i^*_{convd} during faster disturbances and is defined as the ratio between v^*_{dc} and v_{gd}:

$$k_{load} = \frac{v^*_{dc}}{v_{gd}} \tag{4.26}$$

Active power controller

Figure 4.9 depicts the active power controller. This is the most simple method and is an open-loop controller. The reference current which is obtained from equation (4.21) and results in:

$$i^*_{convd} = \frac{P^*}{v_{gd}} \tag{4.27}$$

When more accurate control is needed, a combination of a feedback control and open loop control can be used.

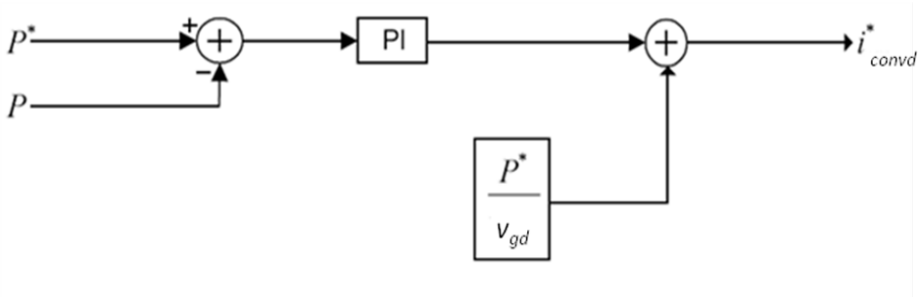

Figure 4.9: Active power controller, adapted from [10]

Reactive power controller

The reactive power controller is similar to the active power controller. Like the active power controller a combination of feedback and an open loop can also be used for more accurate control. The block diagram is given in Figure 4.10.

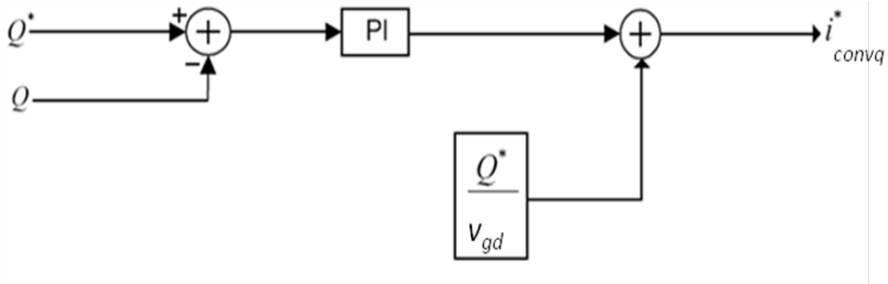

Figure 4.10: Reactive power controller, adapted from [10]

Where

$$i^*_{convq} = \frac{Q^*}{v_{gd}} \tag{4.28}$$

Frequency controller

The frequency controller keeps the frequency at its reference value. “The change in power for a given change in the frequency in an interconnected system is known as the stiffness of the system.”[19] Equation (4.29) gives the power frequency characteristic, which may be approximated by a straight line

$$\frac{\Delta P}{\Delta f} = K \tag{4.29}$$

Where ΔP is the power unbalance, Δf is the frequency drift and K is a constant. From this equation and equation (4.18) it is clear that the frequency can be controlled using a PI controller to reduce the control error to zero. The block diagram is shown in Figure 4.11.

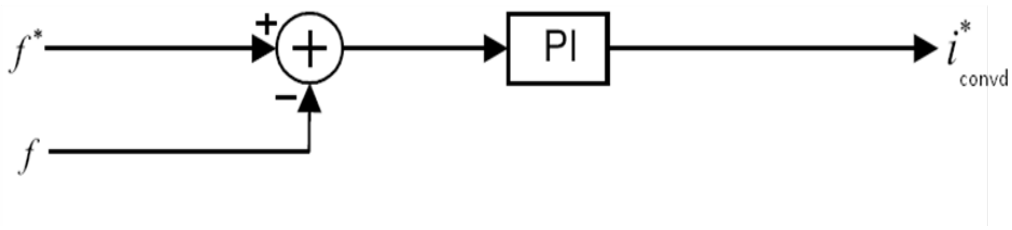

Figure 4.11: Frequency controller, adapted from [10]

AC voltage controller

From Figure 4.1 an equation for the voltage drop ΔV over the inductor L or reactor X can be derived as [10]:

$$\begin{aligned} \Delta V &= V_{conv} - V_g \\ &= \Delta V_p + j\Delta V_q \\ &= \frac{RP + XQ}{V_g} + j\frac{XP - RQ}{V_g} \end{aligned} \tag{4.30}$$

Assuming

$$\Delta V_q \ll V_g + \Delta V_p \tag{4.31}$$

leads to

$$\Delta V \approx \frac{RP + XQ}{V_g} \tag{4.32}$$

Most AC power circuits satisfy $X \gg R$, causing the voltage drop ΔV to only depend on the reactive power flow Q. Thus the variation of the AC voltage V_g depends only on the reactive power flow. Using equations (4.22) and (4.32) Figure 4.12 can be obtained where $|v_g|$ is the amplitude of the line voltage and $|v_g^*|$ is the reference amplitude of the line voltage.

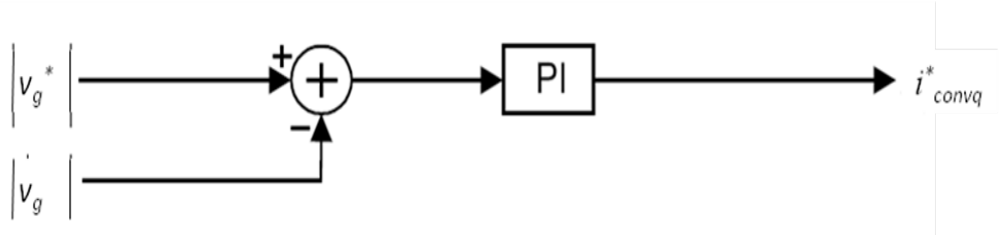

Figure 4.12: AC voltage controller, adapted from [10]

4.4 Siemens Multifunctional Power Link (SIPLINK)

A power distribution network making use of intelligent load-flow control allows for an efficiency-maximized and cost-optimized operation. Due to the liberalization of the market, power networks are subjected to increasing costs which may result in a reduction in supply quality. To cope with rapidly changing worldwide power distribution markets, organization of the network operation is needed. “Switching high currents and coping with short circuits remain the main tasks. High speed switches and HVDC transmission based on power electronics help to solve these problems”[20]. DC long-distance transmission and back-to-back links are not new for high voltage applications. The advancements in power electronics made in this sector make it also interesting for medium voltage applications.
With Siemens Multifunctional Power Link (SIPLINK), Siemens introduces the VSC-HVDC concept to be used for medium voltage applications. This section presents the system design for SIPLINK as well as possible configurations for it to be used in industry. The Simulink system design is discussed.

4.4.1 SIPLINK System Design

Like VSC-HVDC, SIPLINK has the same components but is designed to handle medium voltages. The AC side voltage of the converters is restricted to 1100 V. The DC link voltage is restricted to up to 2000 V. This makes long-distance power transmission not efficient because of higher losses due to the use of a lower voltage. The pulse-controlled power converters are operated at a frequency of 3 kHz for low power applications in the order of 1 to 5 MVA. For higher powers a converter frequency of 750 Hz is used. For electromagnetic compatibility (EMC) issues, the converters are connected via passive operating frequency filters and transformers to the networks to be linked. As stated in chapter 1.6.2, the phase reactors have a dual purpose, serving as EMC filters but also as a means to control the active and reactive power. “The pulse-controlled power converters form the link between the DC circuit and the three-phase networks [20].” The converters are designed with power ratings up to 1.2 MVA. To achieve higher system power ratings it is possible to connect converters in parallel to create what is called a multiparallel connection. For this multiparallel connection the limit is 5 MVA. Several of these SIPLINK systems can then be connected in parallel and a practical maximum of around 30 MVA can be achieved in primary distribution networks.

4.4.2 SIPLINK System Control

The control possibilities of SIPLINK are depicted in Figure 4.13.

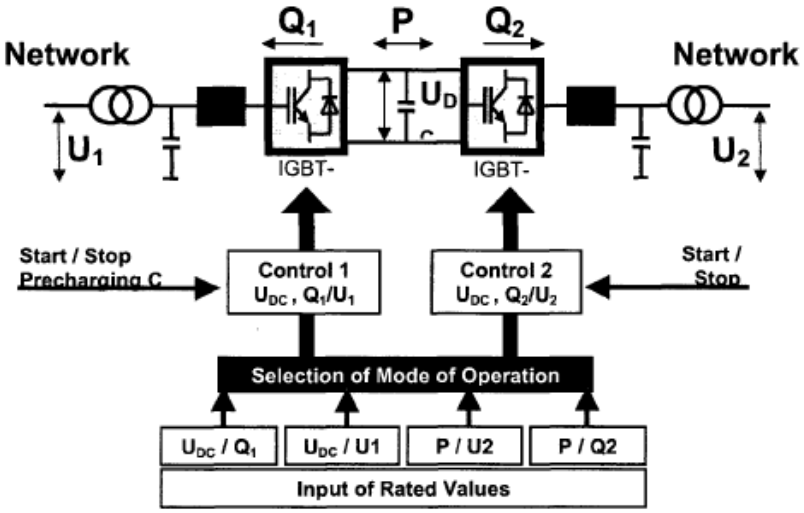

Figure 4.13: SIPLINK-Control: Active power transfer according to demand, dynamic reactive power supply to network 1 and 2 for voltage stability [20]

With SIPLINK power can be transmitted between two networks and reactive power can be generated at each converter end. For this Converter 1 controls the DC voltage and must be connected to a distribution network. Converter 2 can either be connected to a distribution network or may feed an islanded network. The reactive power at both converter ends can be generated independently. This makes it possible to control the power system voltage at both converter ends. Power system voltage regulation allows for compensation of deviations in stationary power system voltages. The recovery time is in the range of seconds. The voltage deviations that can be compensated for depend on the available reactive power of the converters and on the network impedance. In accordance with the client overrating of the converters up to 85 % of load current is possible to compensate for voltage deviations. The choice of overrating of the converters is done after an analysis of the costs and benefits.

SIPLINK has the following operating modes:
Islanded network mode
"The power system voltage is generated by SIPLINK at one network end. Load flow adapts to the active and reactive power demand in the subnetwork, within the framework of the system's power limit."[20]

Interconnected system mode
In this mode, power is being shifted between the two networks and no AC power system is created by SIPLINK.

4.4.3 SIPLINK configurations for industrial power grids

This paragraph illustrates some of the possibilities for a SIPLINK system to be used in an industrial grid to achieve higher plant availability.

Industrial Power Plant
Figure 4.14 represents an industrial grid which makes use of 3 SIPLINK converters. As stated before with a multiparallel connection a power of up to 5 MVA can be handled by the converters. 3 converters in parallel would thus be able to handle up to 15 MVA of power. The arrows indicate the direction of the powerflow. This configuration can be used to separate "dirty" grids (with high harmonics) from "clean" grids with the use of SIPLINK. Sensitive loads can be connected through SIPLINK. The upwards powerflow is useful if the SIPLINK converter is equipped with storage. During faults coming from the supplying grid, the energy stored can be directed towards the other loads connected to the bus. During voltage sags, the sensitive loads can be protected from ever noticing it due to the flow of energy from the storage to the load, and can continue to run undisturbed.

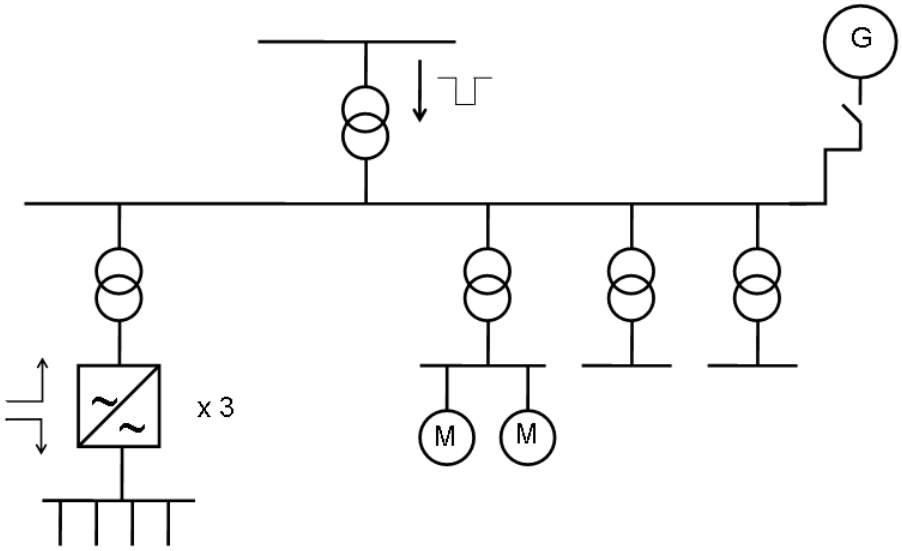

Figure 4.14: SIPLINK configuration with build in storage in Industrial Power Plant

Drilling Rig
The next configuration in Figure 4.15 is mostly used on a drilling rig. There are 2 independent busbars, each fed by 2 generators. The two busbars are closed by a breaker but at the event of a fault, the breaker is opened and the situation in the drawing ensues.
If the problems continue and a black-out occurs only one half of the power supply is lost. But all the thrusters, which are essential loads stay energized and the rig is able to manoeuvre.
The load of the thrusters can be distributed between the two grids and therefore stabilizing each grid. If problems occur in one busbar no power is drawn from that faulted busbar and it is able to recover. The load can be distributed from 100% left / 0% right to 0% left / 100 % right and anything in between. The loadflow can be changed during operation and can so help to balance the load on the busbars. A normal rig must be operated with 4 running generators for redundancy reasons, even if only the power of one generator is needed during low load situations. This will damage the diesel engines on the long run. The SIPLINK system allows

the busbar to be fed with only one diesel while maintaining full redundancy. This is due to the possibility of power exchange via the SIPLINK system from one grid to the other in the case of failure of one of the diesels. The operation of two generators with nearly optimized load saves fuel compared to four generators with nearly idle operation. The operation of only one busbar is not used because other consumers are connected to the busbars and they are not all redundantly fed. Figure 4.15 is only a small part of a complete power grid on the rig.

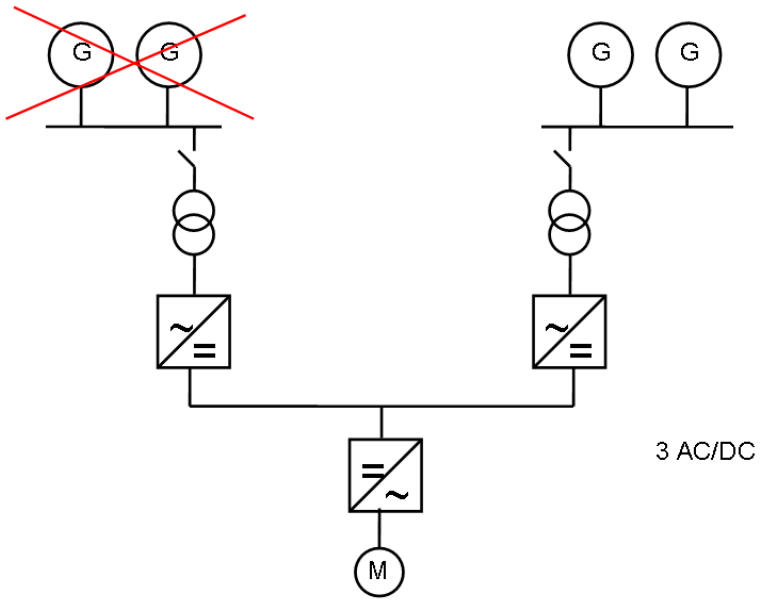

Figure 4.15: SIPLINK configuration on a drilling rig

Chemical Plant

Figure 4.16 is part of a power grid used for example in a chemical plant. It is fed with 150 kV and has its own distribution down to 6 kV where the process is connected. In case of a power failure in the distribution (for example a short) the power on the 6 kV busbars will go down halting the process. Instant feeding from another 6 kV busbar is not possible because that busbar would then also face the short and thus fail. Then before feeding from another source, the fault must be cleared selectively. This leads to waiting times of up to 300 ms until the second feeder from another 6 kV busbar may switch on. But only 70 ms of loss of power is allowed. By making use of SIPLINK, all 6 kV busbars can be connected and all AC/DC converters operate controlling the common DC voltage. At the same time the converters monitor their AC voltage. When the AC voltage goes down, that individual converter changes its operation mode to AC control. By doing this it supplies power to the busbar with the voltage going down. All other converters feed power into the DC link.

The SIPLINK can feed power directly into a faulted busbar because it is short circuit proof due to the current limitations in the converter. Although the SIPLINK feeds in, a short will pull the voltage down. At the same time when the converter changed its operation mode, an OPEN command was given to the feeding switch of the busbar. As soon as the contacts of the feeding switch are opened (after 50 ms) the short is decoupled from the busbar and the power from the SIPLINK will bring the voltage back up. So the process will not be lost. If the short should have occurred on that specific 6 kV busbar where the SIPLINK feeds to, then the process is lost in any case and nothing would have saved it. SIPLINK monitors the voltage and if it does not recover after the 50 ms it detects the short on the 6 kV busbar and stops the infeeding. This method allows for a safe power system with allowed voltage sags of 50 ms. It costs less than the version in Y connection as for the drilling rigs. On the other hand the more

expensive version for the drilling rigs would show NO voltage dip if a short occurs in a feeding system. The choice of which system to use is an economical one.

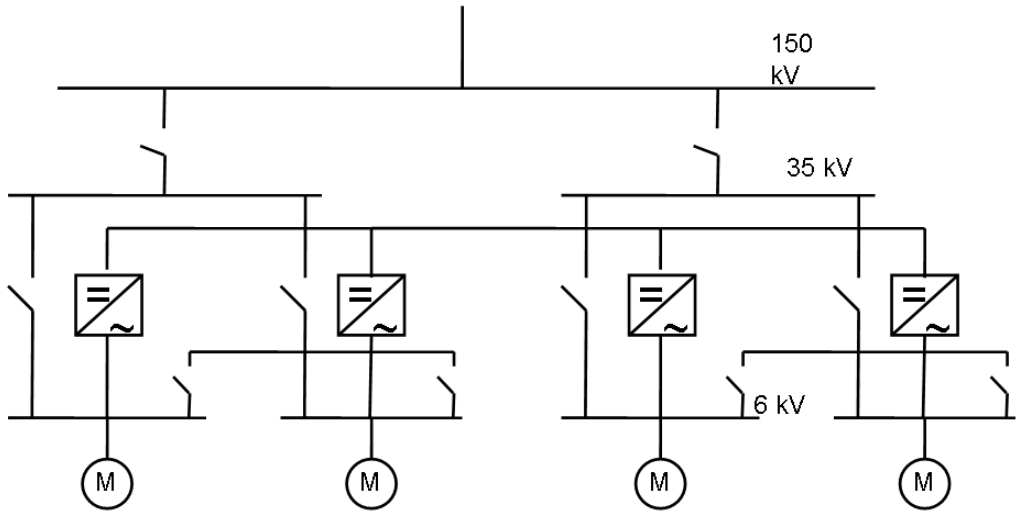

Figure 4.16: SIPLINK configuration on a chemical plant

Future Power Grid

The last configuration is a possibility for the very far future. Presently the power grids from generation to consumer have a tree like structure. But more and more consumers turn into generators – at least partly, by operating solar panels and wind turbines. So the generation is also made directly at the customer side and fed back to the grids. This can lead to instabilities. A future trend will be to organize grids as islands. These islands are the light blue bubbles in Figure 4.17. Each island contains its own consumers and generators (power generators at the local utilities, combined heat and power plants, solar, wind). Each island more or less balances its own loads and each island operates independently. The high voltage grids which now transport the energy will have another role. They will only make the overall balance between the island grids and move energy from one to the other and back. To avoid instabilities the island grids are connected to the high voltage grids by means of short couplings (SIPLINKS). So each grid can stay independent but can exchange energy via the high voltage grid.

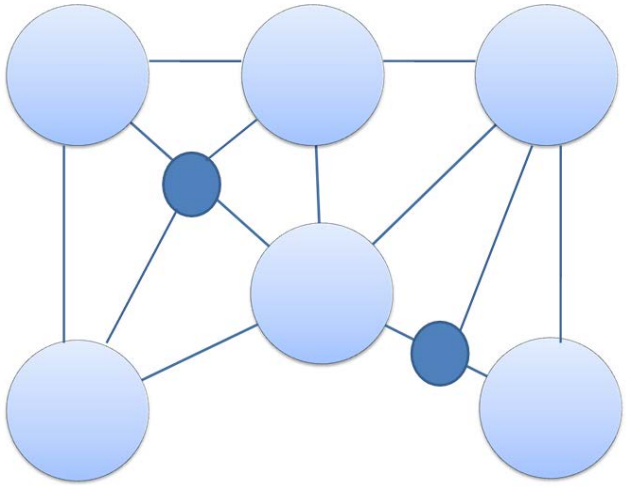

Figure 4.17: Future power grid

4.4.4 SIPLINK SimPowerSystems Model

To investigate the possibilities of voltage sag mitigation using a VSC-MVDC system, a model of SIPLINK was made in Simulink using the SimPowerSystems toolbox.
Each SIPLINK converter has a maximum voltage of 1100 V at the AC side. The current that it is able to handle is between 750 A and 900 A continuously. A peak current of 1800 A can be handled but for only 2 ms. Each converter comes with a 1 mH reactor and a 20 mF DC capacitance. The frequency of the converter is variable, but for high power applications a converter frequency of 750 Hz is used. To achieve higher power handling capabilities more converters need to be connected in parallel. For the use in the 20MVA EdeA substation PPF3, a custom made SIPLINK needs to be designed.

Since each converter has a power rating of 1.5 MVA and the EdeA substation has a power rating of 20 MVA, 14 converters are needed in parallel to handle this amount of power. But for economic purposes it is important to design the rating of the SIPLINK system as close to the load as possible in this case 10.78 MVA. With a 10 percent overrating factor, 8 converters are needed.

Next base value calculations of the one SIPLINK converter is given.

Base values SIPLINK converter
In this part the characteristics of the model made by Siemens Germany is given and the per unit calculations will be derived.

Rated power = 1.5 MVA
Rated voltage = 1100 V RMS line-to-line
Rated frequency = 50 Hz

The calculated base values are:

$$P_{base} = \frac{1.5e^6}{3} = 500\text{e}^3 \text{ VA/phase} \tag{4.33}$$

$$V_{base} = \frac{1100}{\sqrt{3}} = 635.1 \text{ V}_{\text{RMS}} \tag{4.34}$$

$$I_{base} = \frac{P_{base}}{I_{base}} = 787.3 \text{ A} \tag{4.35}$$

$$Z_{base} = \frac{V_{base}}{I_{base}} = 0.81 \ \Omega \tag{4.36}$$

$$L_{base} = \frac{Z_{base}}{2\pi f} = 0.0026 \text{ H} \tag{4.37}$$

$$C_{base} = \frac{1}{2\pi f Z_{base}} = 0.00395 \text{ F} \tag{4.38}$$

The converters at both ends are designed identical. Table 4.1 gives the SI and per unit values for the SIPLINK system designed.
The subscripts *r*, *f* and *dc* denote the values for the reactor, filter and dc circuit components respectively.

Description	Symbol	SI Value	Per Unit
Phase reactor converter 1	L_{r1}	0.0010 H	0.3895
Reactor resistance converter 1	R_{r1}	0.0060 Ω	0.00741
Filter capacitance converter 1	C_{f1}	$45e^{-6}$ F	0.0114
Filter damping resistance converter 1	R_{f1}	10 Ω	12.34
DC capacitor	C_{dc}	0.300 F	75.95
DC capacitor series resistance	R_{dc}		
Grid voltage	U_{grid}	1100 $V_{LL\ RMS}$	1
DC voltage	U_{dc}	1892	1
Output voltage	U_{load}	1100 V	1
Modulation index	m_a	0.95	

Table 4.1: Converter Parameters

These values are used to model a scaled version of SIPLINK. As stated before, 8 converters are connected in parallel. Each converter has its own 1 mH reactor but only one filter is used for all converters. In this model the DC voltage is being controlled by converter 1. This is done by a controller consisting of an inner current and an outer voltage controller. The SIPLINK designed in this thesis is used in an industrial grid. For the motors a reliable AC voltage is needed. Thus converter 2 should control the AC voltage. Because the motors in the industrial network need a reliable frequency to operate well, also a frequency controller is needed. However because of time constraints and because the design of a new SIPLINK model is not the core of the research for this thesis, rather to illustrate a possible solution for voltage dip mitigation with a boost converter in combination with an MVDC system, only a simple PWM AC voltage controller is designed, see Figure 4.18. All converters receive the same control input, thus only one controller is designed.

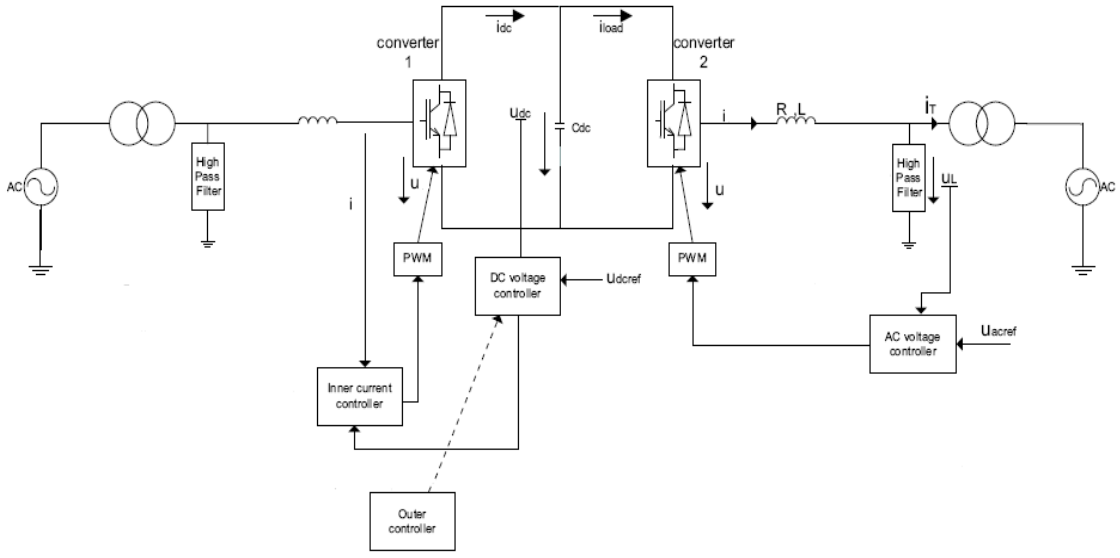

Figure 4.18: Designed SIPLINK model

The design and testing of the new SIPLINK was done in five steps:

1. Design and testing of rectifier with 1 converter block
    i. Inner current controller PI gains modified with fixed reference current, Figure 4.6, where *id_ref* and *iq_ref* are the reference dq-currents.
    ii. Outer DC voltage controller PI gains modified with changing load Figure 4.8, where v_{dc}^{*} is the reference dc voltage. k_{load} is determined by equation (4.26).
2. Adding 7 converters and connecting each with control output designed in step 1
3. Design and testing of inverter
    i. Controller consists of direct voltage controller PWM to achieve desired AC voltage. Modify PI gains with varying load.
4. Adding 7 converters and connecting each with control output designed in step 3.
5. Connect inverter and rectifier and test for different loads including motor load

The total system is depicted in Figure 4.19.

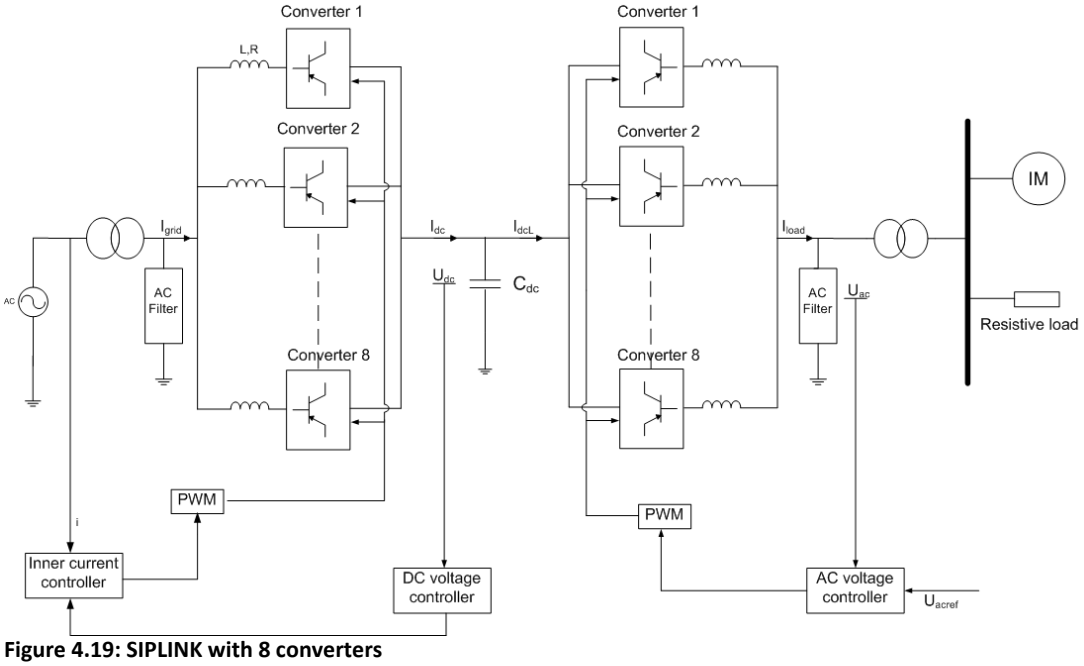

Figure 4.19: SIPLINK with 8 converters

5. Supercapacitor Interfacing

5.1 Bidirectional boost converter topology

To compensate for a brief voltage sag in the grid the supercapacitor based voltage sag compensator topology of Figure 5.1 is proposed. This compensator topology is based on the previously discussed SIPLINK system with the 8 converters and 10.78 MW power handling capability. The DC link of this SIPLINK system is enhanced by a converter with a supercapacitor storing element to compensate during brief voltage sags of up to 1 second of duration and as low as 10% of nominal voltage remaining. To charge and discharge the supercapacitor during and after a voltage sag respectively, a converter is needed. This because as mentioned before, the supercapacitor terminal voltage is only up to 5 V. A converter is needed to boost this voltage to a suitable level to feed into the DC link of the MVDC converter. After the voltage sag has cleared, the supercapacitor needs to be recharged in order for it to be ready for the next voltage sag. To increase the terminal voltage of the supercapacitor stack the well known boost converter can be used. The converter is a well proven technology and consists of an inductor, switch, diode and output filter. To recharge the supercapacitor stack after the sag has cleared, an extra switch and diode is added to the boost converter, making the power flow bidirectional. A schematic of the supercapacitor enhanced SIPLINK is shown in Figure 5.1.

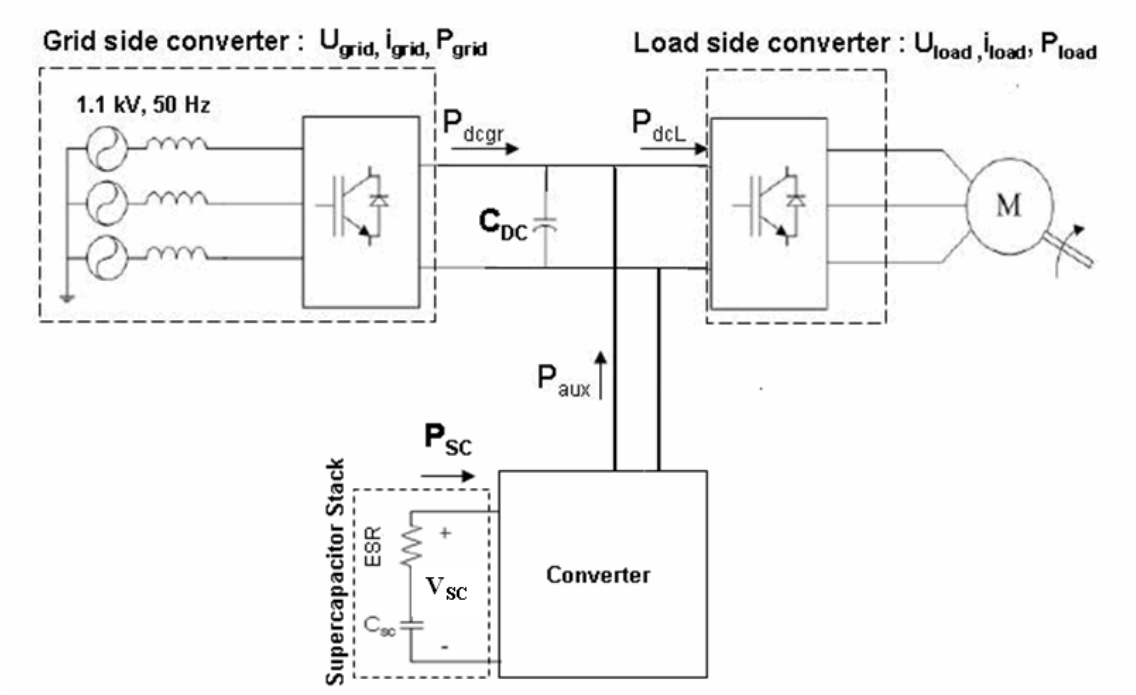

Figure 5.1: Supercapacitor enhanced mitigation topology

The bidirectional boost converter is based on a standard boost converter but it has an extra switch which makes it possible for the current to reverse and thus to recharge the supercapacitor after the sag has cleared. Figure 5.2 shows the basic boost converter circuit.

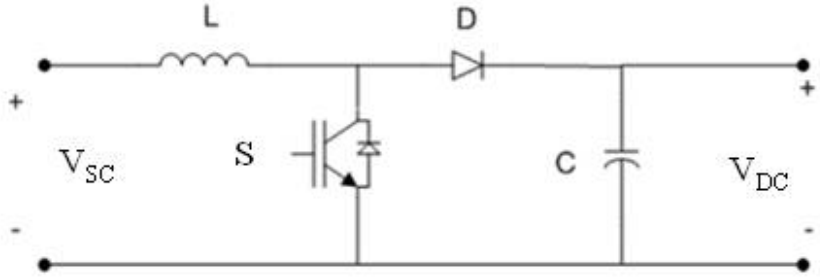

Figure 5.2: Boost converter topology

The basic principle of a Boost converter consists of 2 distinct states:

- In the On-state, the switch S is closed, the diode D is reverse biased thus isolating the output stage from the input stage of the converter. During this stage the input stage supplies energy to the inductor L resulting in an increase in the inductor current;
- In the Off-state, the switch is open and the inductor current flows through the diode D, the capacitor C and the load, thus transferring the energy accumulated during the On-state into the capacitor. In this state the output stage receives energy from the inductor as well as from the input source. The states are illustrated in Figure 5.3.

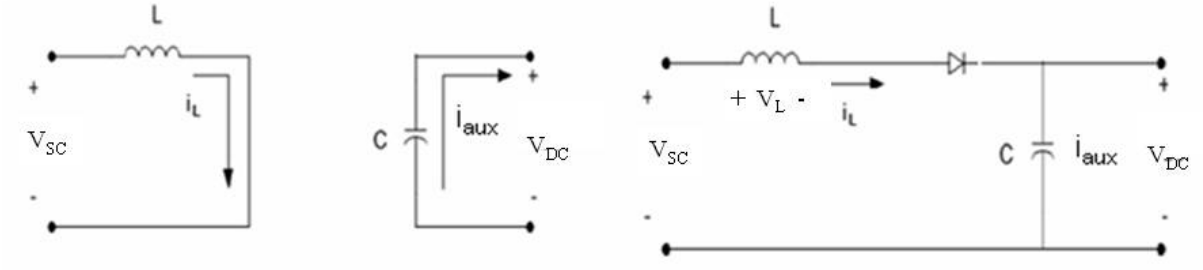

Figure 5.3: On and off states of the boost converter

When a boost converter operates in continuous mode, the inductor current (I_L) never falls to zero. See Figure 5.4 for the typical current and voltage waveform for this mode of operation. The output voltage can be calculated as follows, in the case of an ideal converter (i.e. using components with an ideal behaviour) operating in steady conditions:

$$V_{SC}t_{on} + (V_{SC} - V_{DC})t_{off} = 0 \tag{5.1}$$

where t_{on} is the time the switch S is on, and t_{off} is the time the switch is off.
Equation (5.1) can be rearranged as

$$\frac{V_{DC}}{V_{SC}} = \frac{T}{t_{off}} = \frac{1}{(1-D)} \tag{5.2}$$

where T is the period of the on-off switching action and D is the duty cycle.

For a lossless circuit the power balance ensures

$$\frac{I_{aux}}{I_{SC}} = (1 - D) \tag{5.3}$$

From the above expressions it can be seen that the output voltage is always higher than the input voltage (as the duty cycle goes from 0 to 1), and that it increases with *D*, theoretically to infinity as *D* approaches 1. This is why this converter is sometimes referred to as a *step-up* converter.

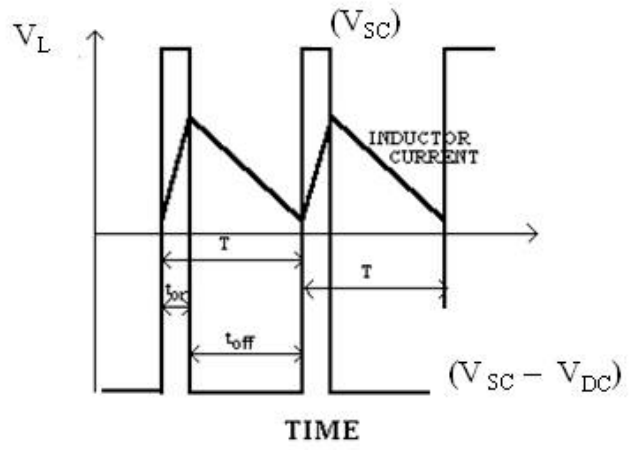

Figure 5.4: Voltage and current waveforms (Boost Converter)

Next by adding an extra switch to the boost converter a bidirectional boost converter is obtained. This allows for the supercapacitor to be charged back up after the voltage sag has cleared. A schematic for this converter is given in

Figure 5.5. The addition of the switch also implies that the converter does not have a discontinuous conduction mode as the current is always able to reverse through the extra switch.

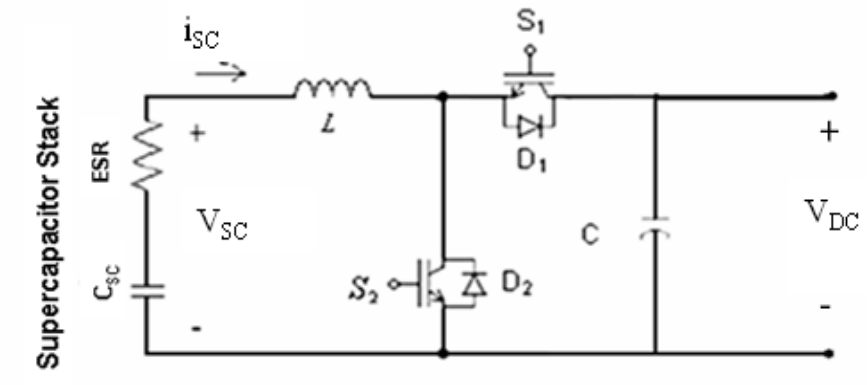

Figure 5.5 : Schematic bidirectional buck-boost converter

Using this converter, the supercapacitor topology of Figure 5.1 transforms into Figure 5.6. The bidirectional boost converter is added. Now during a voltage sag power from the supercapacitor is transferred to the DC link and back when the sag has cleared.

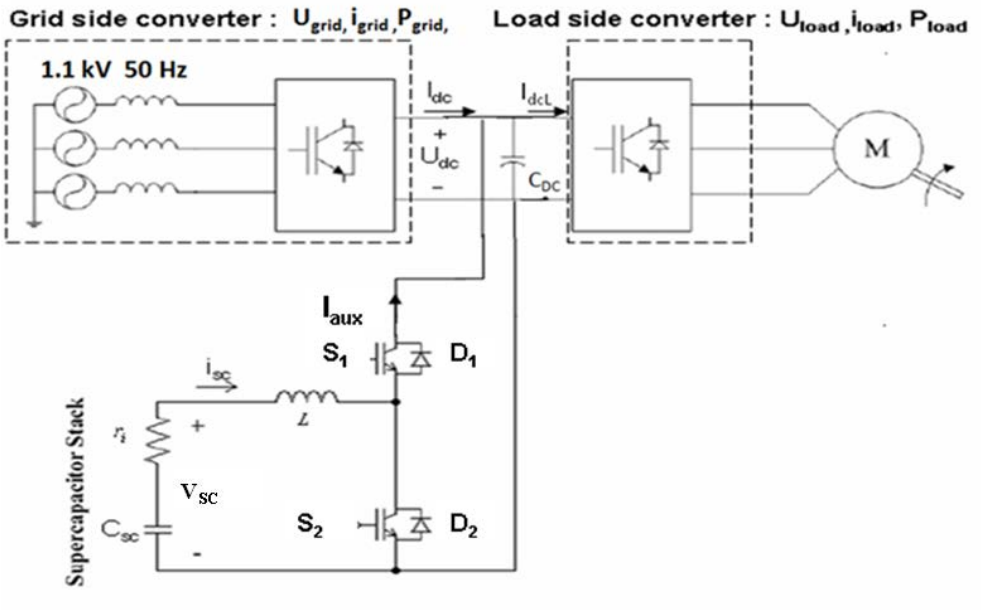

Figure 5.6: Proposed supercapacitor based voltage sag mitigation topology

5.2 Boost converter Inductor Design

In this paragraph the value of the inductor is determined. For economical purposes it is important to choose the components of the bidirectional boost converter as small as possible. To keep the stress on the supercapacitor and the switches low, also a small current ripple is desired. Taking these conditions into account, an expression is derived for the inductor with the equations following later in this section. Then graphically the minimum inductor value is determined.

The DC inductor current component of the boost converter is found by considering the output capacitor charge balance given by (5.4). This equation gives the net change in capacitor charge over one switching period by integrating the capacitor current $i_c(t)$. During the first subinterval the capacitor supplies the current to the load and is thus partially discharged. During the second subinterval the load is supplied by the inductor current and simultaneously recharges the capacitor.

$$\int_0^{T_s} i_c(t)dt = \left(-\frac{V_{dc}}{R}\right)DT_s + \left(I_{sc} - \frac{V_{dc}}{R}\right)(1-D)T_s \tag{5.4}$$

Where V_{dc} is the DC output voltage of the boost converter, R is the load impedance, D is the duty ratio, T_s is the switching period and I_{sc} is the inductor current DC component.
The steady state result is received by equating the result to zero. Solving for the inductor current DC component, equation (5.5) is obtained:

$$I_{sc} = \frac{V_{dc}}{(1-D)R} \tag{5.5}$$

To eliminate V_{dc}, equation (5.2) is substituted in the previous equation. This gives

$$I_{sc} = \frac{V_{SC}}{(1-D)^2 R} \tag{5.6}$$

From this equation it can be seen that the inductor current becomes large as D approaches 1.

Next an expression for the inductor current ripple Δi_{sc} is desired. During the first subinterval, when the switch is on, the slope of the inductor current is defined by

$$\frac{di_{sc}(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_{sc}}{L} \tag{5.7}$$

When the switch is off during the second subinterval, the slope of the inductor current is given by

$$\frac{di_{sc}(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_{sc} - V_{dc}}{L} \tag{5.8}$$

The inductor current waveform is illustrated in Figure 5.7.

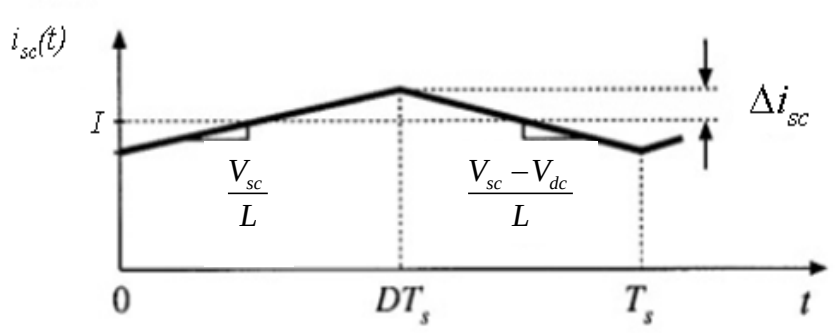

Figure 5.7: Boost converter inductor current waveform, adapted from [21]

During the first subinterval the change in the inductor current, $2\Delta i_{sc}$, is given by

$$2\Delta i_{sc} = \frac{V_{sc}}{L} DT_s \tag{5.9}$$

Solving for Δi_{sc} gives

$$\Delta i_{sc} = \frac{V_{sc}}{2L} DT_s \tag{5.10}$$

Using this equation a value for the inductor L can be found that satisfies the conditions for Δi_{sc}. When a value for Δi_{sc} is chosen, the maximum value of L is necessary in order for the converter to operate at every duty ratio. By varying D from 0 to 1, and determining the values of L, the maximum value is chosen. A similar analysis is done to confirm that the current ripple is as desired when the converter operates in buck mode.

5.3 Boost converter Output Capacitor Design

As in the previous section, the output capacitor voltage waveform can be given and the equation describing the output voltage ripple Δv_{dc} can be derived. The voltage waveform is given in Figure 5.8.

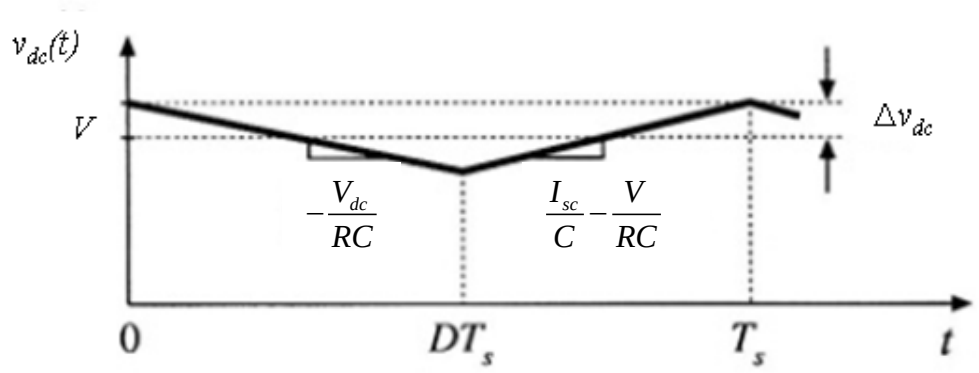

Figure 5.8: Boost converter output voltage, adapted from [21]

The change in the capacitor voltage, $2\Delta v_{dc,}$ is equal to the slope multiplied by the length of the subinterval. For the first subinterval this is given by equation (5.11)

$$-2\Delta v_{dc} = -\frac{V_{dc}}{RC} DT_s \tag{5.11}$$

Solving for Δv_{dc} gives

$$\Delta v_{dc} = \frac{V_{dc}}{2RC} DT_s \tag{5.12}$$

With $I_{aux} = \frac{V_{dc}}{R}$ equation (5.12) becomes

$$\Delta V = \frac{I_{aux}}{C} DT_s = \frac{P}{CV_{dc}} DT_s \tag{5.13}$$

With this expression a capacitor value C can be obtained which gives the desired output voltage ripple peak magnitude $\Delta v_{dc.}$

5.4 Boost converter Current mode controller design

A commonly used control method for power converters is current mode or current programmed control. In a current-mode control the control voltage directly controls the output inductor current that feeds the output stage and thus the output voltage.
Current mode control is a two-loop system, see Figure 5.9, in which the converter output is controlled by the peak transistor switch current. The inner loop or current loop controls the average current in one switching cycle, while the outer loop or voltage loop controls the output voltage and provides the inner loop with the reference current. The control input signal is current $i_c(t)$ and a control network switches the transistor on and off in a manner that the peak switch current $\hat{I}_s(t)$ follows $i_c(t)$. The control input signal $i_c(t)$ as well as the converter inductor currents, power input voltages and capacitor voltages determine the duty cycle $d(t)$.

The duty cycle is thus not directly controlled but is a function of the before mentioned parameters. Figure 5.10 illustrates the control signal $i_c(t)$ and the switch current $i_s(t)$. The clock sends a pulse to the Set input of the latch initiating the switching period by causing the latch output Q to be high thus turning on the transistor. While the transistor is on, the transistor current $i_s(t)$ is equal to the inductor current $i_{sc}(t)$. This inductor current increases gradually (see Figure 5.4) with slope m_1 given by equation (5.7). After some time, the switch current $i_s(t)$ equals the control signal $i_c(t)$ at which point the controller turns the transistor switch off, leading the switch current to drop to zero and the inductor current to gradually decrease with slope m_2 given by equation (5.8) during the remainder of the period.

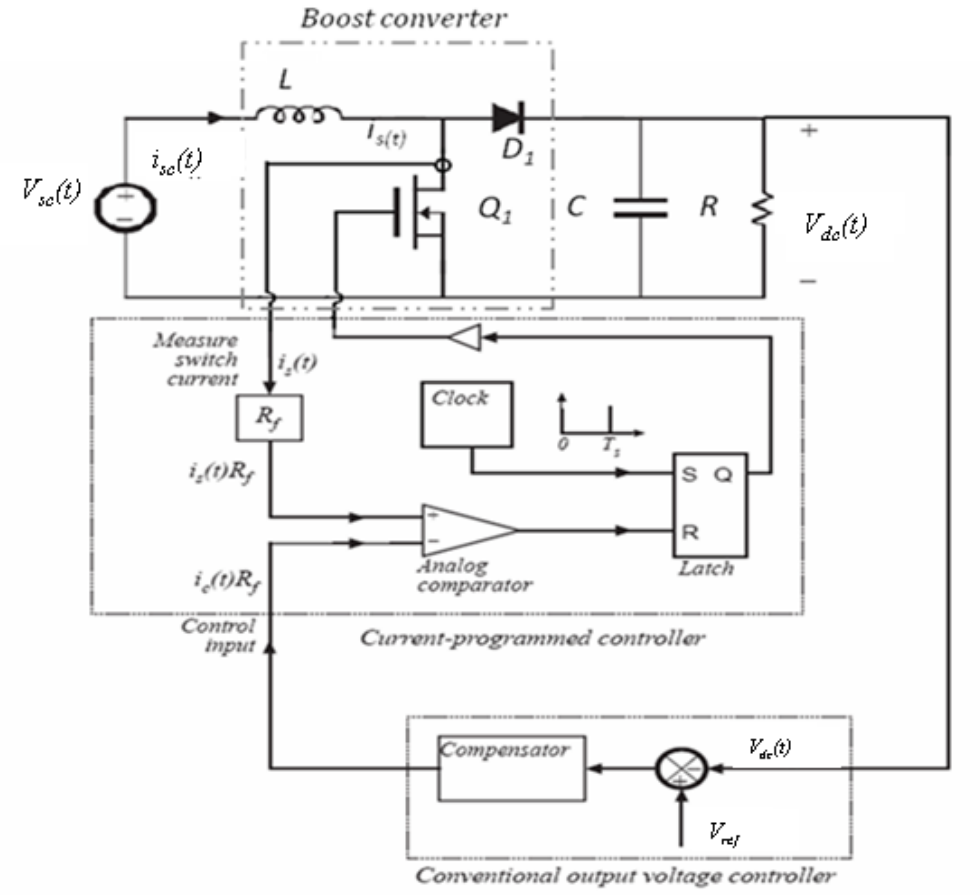

Figure 5.9: Boost converter with current mode control, adapted from [21]

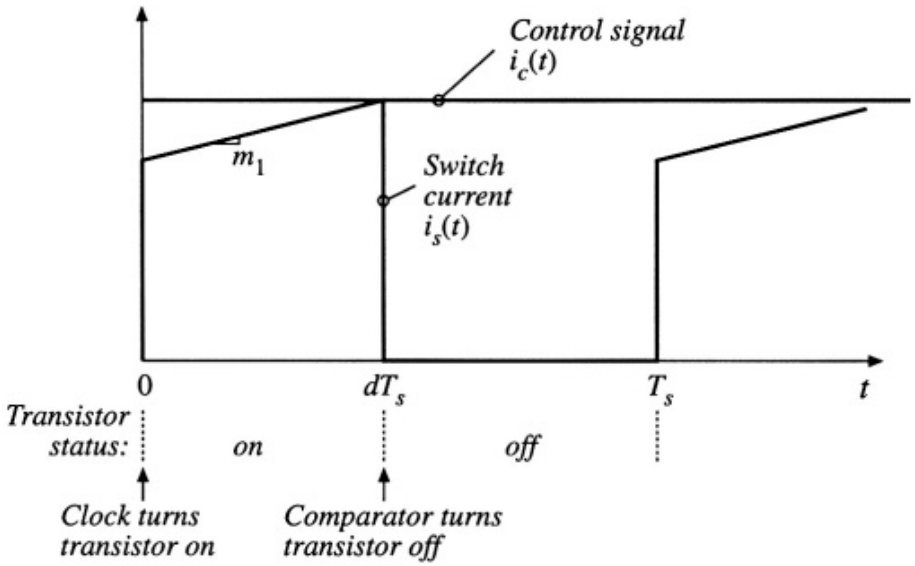

Figure 5.10: Switch current $i_s(t)$ and control input $i_c(t)$ waveforms [21]

In a practical circuit the controller current is measured with a current sensing circuit and then compared to the switch current with an analog comparator. Usually however voltages proportional to $i_s(t)$ and $i_c(t)$ are compared through a resistor R_f.
When a regulated output is desired, which is usually the case, a feedback loop is designed. The feedback loop compares the output voltage $v_{dc}(t)$ with a reference signal v_{ref} and generates an error signal. This error signal is fed to the input of a compensation network and the output of this network controls the signal $i_c(t)R_f$. A PI control scheme can be used for this outer voltage control. For this thesis research also a PI controller is designed. The main advantages of current-mode control are the simple dynamics. "A disadvantage of current programmed control is its susceptibility to noise in the $i_s(t)$ or $i_c(t)$signals. This noise can prematurely reset the latch, disrupting the operation of the controller." [21] Some amount of filtering is thus desired.

There are three basic types of current-mode controls:

1. Tolerance band control
2. Constant- "off"- time control
3. Constant-frequency control with turn on at clock time

For the current mode controller of the bidirectional boost converter, constant frequency control with a turn-on at clock time is simulated. The other two options have a variable frequency. The inductor impedance is dependent on the frequency, thus choosing a constant frequency means the circuit will always have constant impedance. A constant impedance benefits the prediction of the behaviour of the system and makes the design of an input filter simpler.
In the controller with constant-frequency and turn on at clock time, the switch is turned on at the beginning of each constant-frequency switching time period. The control voltage dictates $\hat{I}_{sc}$ which is the peak inductor current, and the instant at which the switch is turned off.

5.4.1 Slope compensation design

During the operation of the current-mode controller of Figure 5.9, with a duty cycle larger than 0.5, a perturbed inductor current is less able to converge to the desired steady state inductor current. Making the controller unstable whenever the steady-state duty cycle is greater than 0.5. “To avoid this stability problem, the control scheme is usually modified, by addition of an artificial ramp to the sensed switch current waveform.” [21] See Figure 5.11. In this section, the stability of the current-mode controller is analyzed.

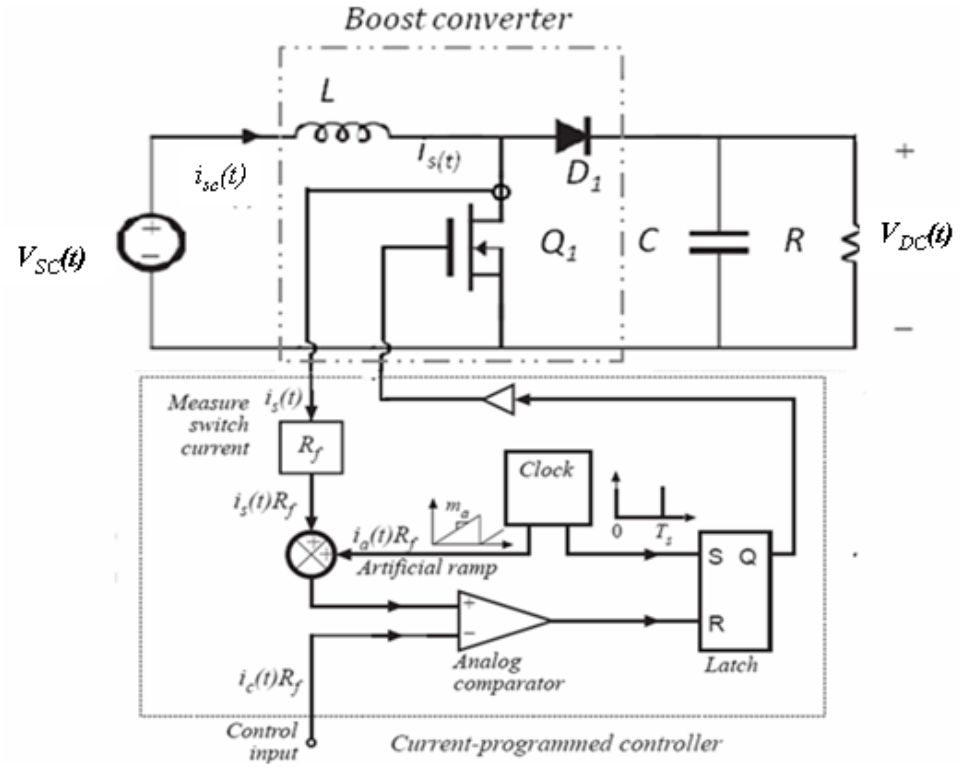

Figure 5.11: Current-mode controller with slope compensation, adapted from [21]

Figure 5.12 illustrates the inductor current during continuous conduction mode for a switching converter. During the first subinterval of the period T_s, the slope is equal to m_1 and equal to $-m_2$ during the second subinterval. For the boost converter the slopes m_1 and m_2 are given by (5.7) and (5.8).

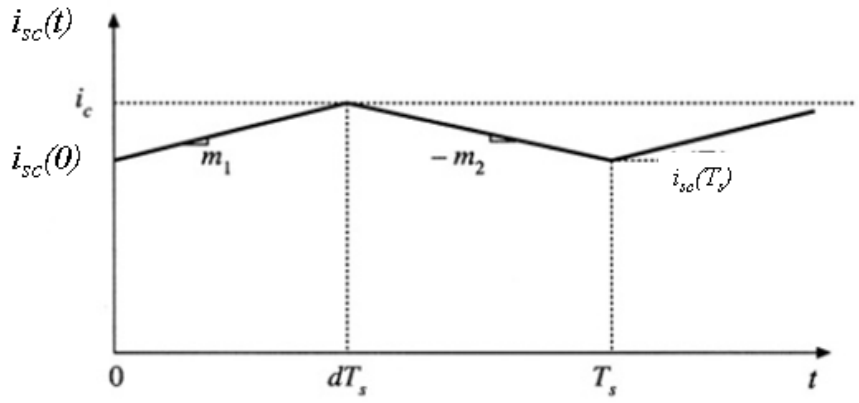

Figure 5.12: Inductor current waveform of current-mode controlled converter operating in the continuous conduction mode, adapted from [21]

Without slope compensation, a perturbation in the inductor current will lead to sub-harmonic oscillations. Here the pattern is often repeated at one half of the switching frequency. A 50 percent duty cycle is the theoretical limit for stable continuous conduction operation without any slope compensation. Without compensation, the inductor waveform looks like Figure 5.13.

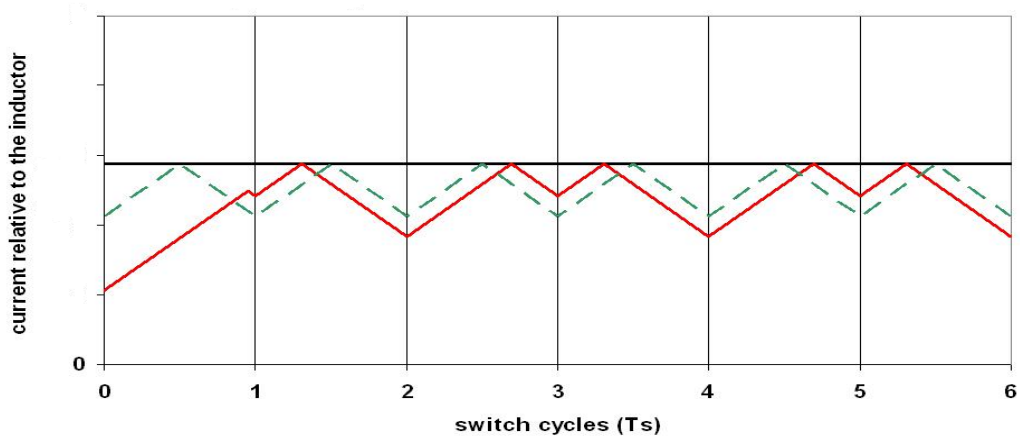

Figure 5.13: Perturbed inductor current (red), peak control current (black) and steady state inductor current (green) for D>0.5 [22]

"The controller can be rendered stable for all duty cycles by addition of an artificial ramp to the sensed switch current waveform" [21], as illustrated in Figure 5.14.

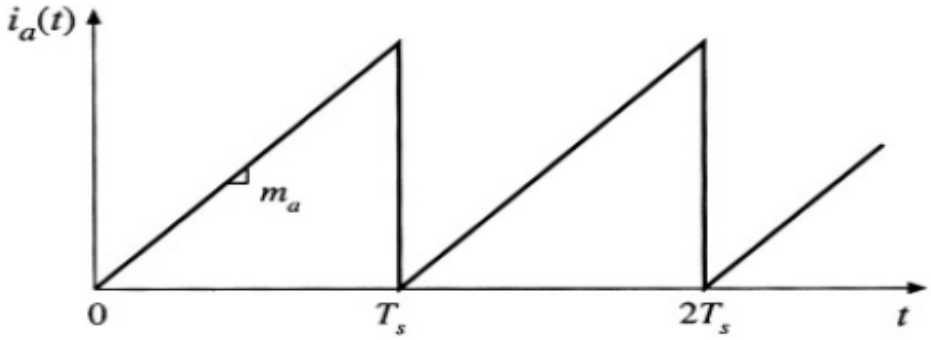

Figure 5.14: Artificial ramp waveform[21]

The artificial ramp reduces the gain of the inner switch-current sensing discrete feedback loop. The artificial ramp has slope m_a. The controller switches the transistor off at

$$i_a(dT_s) + i_{sc}(dT_s) = i_c \tag{5.14}$$

where $i_a(t)$ is the artificial ramp waveform. The transistor is switched off when the inductor current $i_{sc}(t)$ is given by

$$i_{sc}(dT_s) = i_c - i_a(dT_s) \tag{5.15}$$

Figure 5.15 illustrates the analog comparison of the inductor current waveform i_{sc} with the quantity $[i_c - i_a(t)]$.

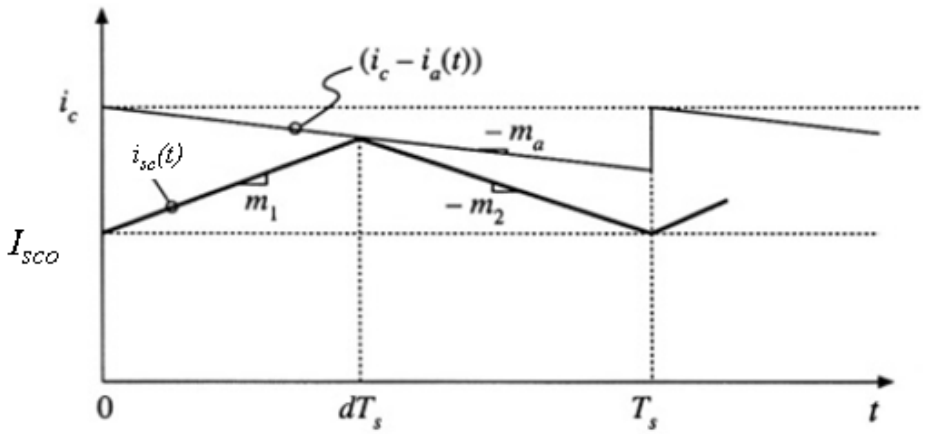

Figure 5.15: Addition of artificial ramp ,adapted from [21]

A common choice for the artificial ramp slope is [21]

$m_a = ½m_2$ (5.16)

Another common choice for the artificial ramp, known as *deadbeat control* or *finite settling time* is

$m_a = m_2$ (5.17)

The author refers the reader to [21] for an in depth mathematical deduction of equations (5.16) and (5.17).

5.5 Buck Mode or supercapacitor charging

While charging the supercapacitor the input voltage of the bidirectional boost converter is considered to be constant. It is after all the DC voltage provided by the SIPLINK converters. Since the supercapacitors are being charged in this mode, the output voltage does not need to be regulated and only a current loop is required. The current loop is necessary so a regulated current can be obtained to charge the supercapacitors so they will not get damaged. To disturb the operation of the SIPLINK converters as little as possible, only the 10 percent extra current that can be drawn by the 10 percent overrated converters will be used to charge the supercapacitors. This value is the current reference value for the Buck mode control in Figure 5.16.

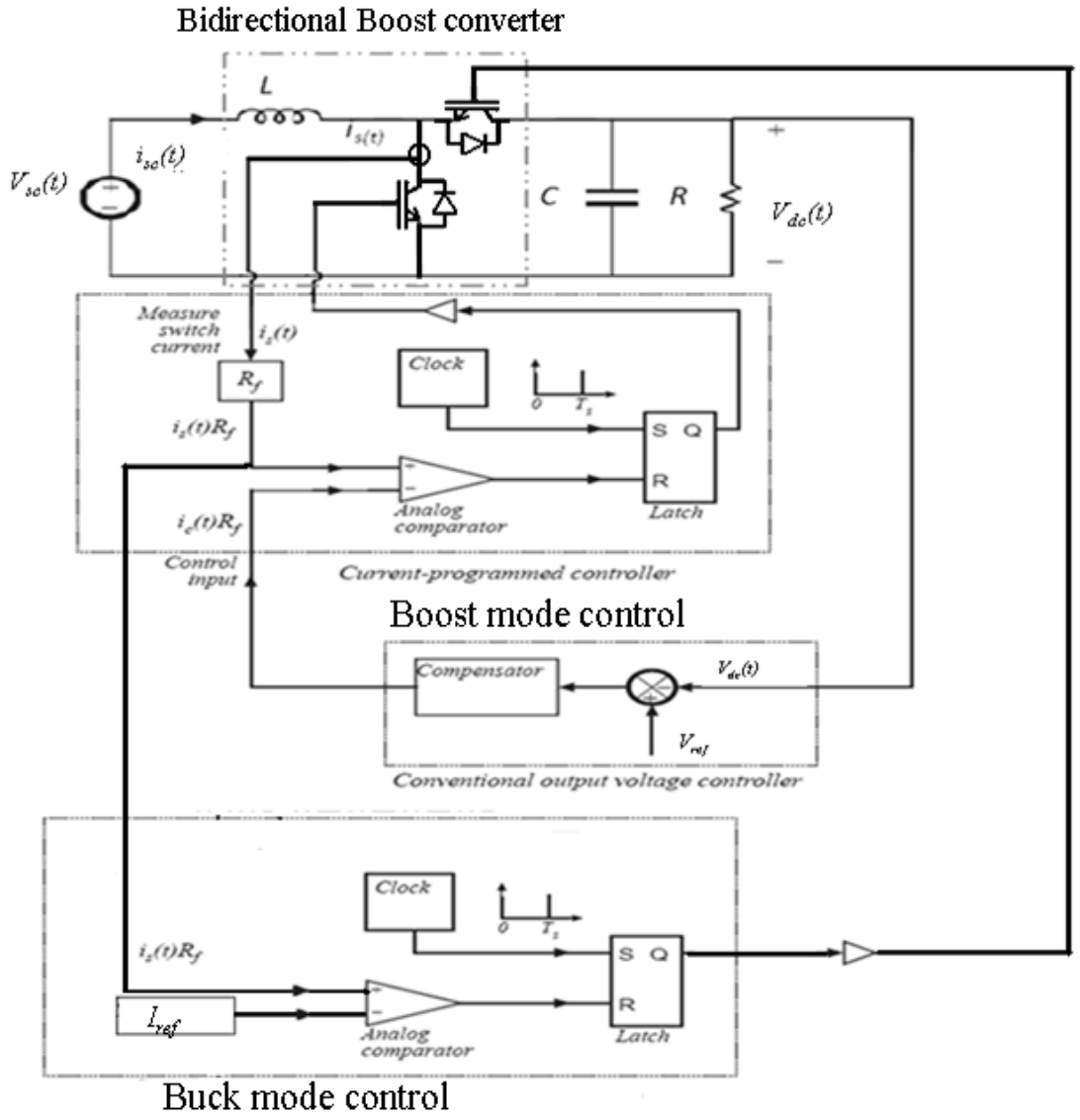

Figure 5.16: Supercapacitor charging circuit

5.6 Supercapacitor sizing

In this section the method to calculate the size of the supercapacitor needed to compensate for a voltage sag is described. During a voltage sag the important factor to consider is the power of the system. The converter currents are limited and the voltage decreases, thus decreasing the power delivered to the load. This power needs to be compensated for. Hence when sizing the capacitors one must consider calculations for a constant power discharge. Next equations for constant power discharge are presented and an iterative method to determine the minimum amount of supercapacitor cells is discussed. Figure 5.17 gives the equivalent circuit for a constant power application using supercapacitors with ESR.

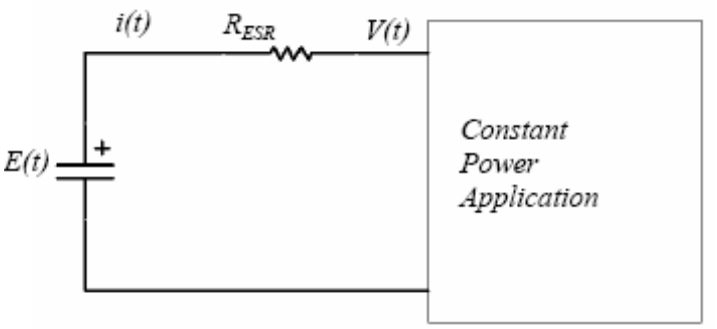

Figure 5.17: Equivalent circuit including the equivalent series resistance[23]

The system depicted in Figure 5.17 is governed by the following equations.

$$i(t) = -C\frac{dE(t)}{dt} \tag{5.18}$$

$$E(t) = -\frac{1}{C}\int i(t)dt \tag{5.19}$$

$$E(t) = i(t)R_{ESR} + V(t) \tag{5.20}$$

$$V(t)i(t) = p \tag{5.21}$$

$$E(t) = nE_{cell}(t) \tag{5.22}$$

$$C = \frac{n_p}{n_s}C_{cell} \tag{5.23}$$

$$R_{ESR} = \frac{n_s}{n_p}R_{cell} \tag{5.24}$$

where,
E(t) is the internal capacitor voltage,
V(t) is the terminal voltage,
I(t) is the current,
p is the constant power,
R_{ESR} is the equivalent series resistance.
n_p is the number of cells in parallel
n_s is the number of cells in series

Solving the equations results in equation (5.25)

$$\frac{dE(t)}{dt} = \frac{-CE(t) \pm \sqrt{C^2 E(t)^2 - 4R_{ESR}C^2 p}}{2RC^2} \tag{5.25}$$

The current waveform is given by

$$\frac{di(t)}{dt} = \frac{-i(t)}{C\left(R - \frac{p}{i(t)^2}\right)} \tag{5.26}$$

The iterative numerical method needed to solve this equation for a given power and time requires an initial value for the voltage *E(t)* and it needs a final target minimum voltage.
The maximum current is determined by the rating of the capacitor. When the current is at its maximum value, the terminal voltage *V(t)* will be a minimum. By adding the voltage drop over the ESR, the final value of *E(t)* can be found. The final value is used as the target for the numerical computations. The magnitude of the initial voltage is determined by the number of cells. By performing iterations, that is changing the value n_s (assuming n_p is 1), the final value of each voltage trajectory can be compared to the target voltage. If the final value is lower than the target voltage, the number of cells should be incremented until the voltage is greater than or equal to the target voltage. This way the minimum amount of cells required is found. All the while the current should be monitored so it does not exceed the maximum cell current.

Another approach is to design for the capacitor cells to reach the maximum current in the desired time instead of the minimum voltage. Then an initial current is needed which is given by (5.27).

$$I_i = \frac{E_i - \sqrt{E_i^2 - 4R_{ESR}p}}{2R} \tag{5.27}$$

By performing iterations on n_s the final value of the current can be set to be less than or equal to the maximum cell current. With iterations of n_p, thus more cells in parallel, more current can be supplied to the load.
The voltage and current waveforms for a constant power discharge are given in Figure 5.18.

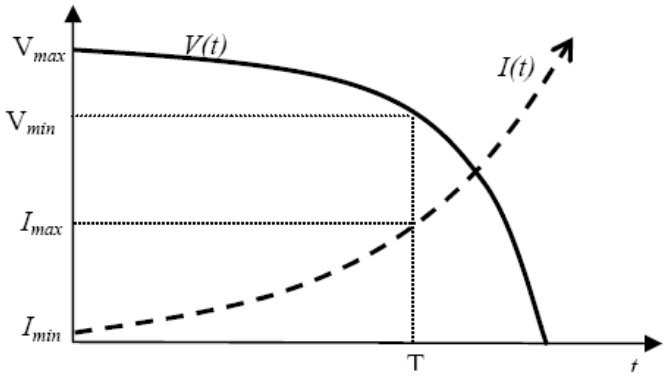

Figure 5.18: Voltage and current waveforms for constant power discharge[23]

By varying n_s and n_p an optimum solution can be found which yields the minimum amount of cells that can provide ride through for the given power and duration.

5.7 Control of supercapacitor based voltage sag mitigation system

Figure 5.6 shows the boost converter configuration for sag compensation. In this figure it appears that the boost converter is always on and boosting its input voltage. Of course in a practical situation this is not the case. Voltage sags occur only a few times a year, thus only a few times a year the boost converter should be operating to compensate for the voltage loss. After the voltage sag has cleared, the supercapacitor should be charged again for the next time a sag occurs. In this section a control scheme for the operation of the boost converter is presented.

The working window of the DC-link voltage of this version of SIPLINK is 1800 ~2100V. These values are chosen to correspond to a modulation index m_a of 0.86< m_a<1 according to (5.29). The ride-through system is set to start supporting the DC-link voltage when the DC-link voltage is below 1800 V, and to stop when the DC-link voltage is above 1850 V provided that the sag has cleared and the grid voltage has returned to normal. In Table 4.1 it was given that the modulation index m_a is 0.95. The modulation index is a function of the triangular waveform v_{tri} generated by the converter at a switching frequency $f_{s,}$ and the control signal $v_{control}$. The control signal is used to modulate the switch duty ratio and is at the desired fundamental frequency of the converter. The relation between these quantities is given in (5.28) [24]

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{5.28}$$

where $\hat{V}_{control}$ is the peak amplitude of the control signal. The amplitude of $\hat{V}_{tri}$ is kept constant. The line-to-line rms voltage of the system, V_{LL} is related to the modulation index m_a and the DC link voltage V_{DC} as [24]:

$$V_{LL} = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_{DC} \tag{5.29}$$

A linear relation exists between the line-to-line voltage and the DC voltage for $m_a \leq 1$. It is desirable to have a high modulation index so as to effectively make use of the available amplitude of the fundamental-frequency component. The converter is said to go into overmodulation when m_a>1. During overmodulation the linear relation is lost. For a DC voltage lower than 1797 V, the modulation index is higher than 1 according to (5.29). Hence the ride through system should start its support at a value higher than 1797 V. At 1850 V, the modulation index has returned to an acceptable value, and the converter is able to generate the required AC voltage independently. To have enough margin to distinguish between the supported DC-link voltage and the healthy DC-link voltage, the output voltage reference of the bidirectional boost converter is set to 1880 V. The working window of the supercapacitor stack is 1030~840 V. The derivation of this window follows in the next chapter. The flow chart of the control algorithm is shown in Figure 5.19. Here it follows that the auxiliary supply should start boosting the supercapacitor voltage when the DC voltage is below 1800 V and keep this mode until the DC link voltage is above 1850 V again. When the sag is cleared, the supercapacitor voltage is checked and if this is below 950 volts, the converter should go into buck mode.

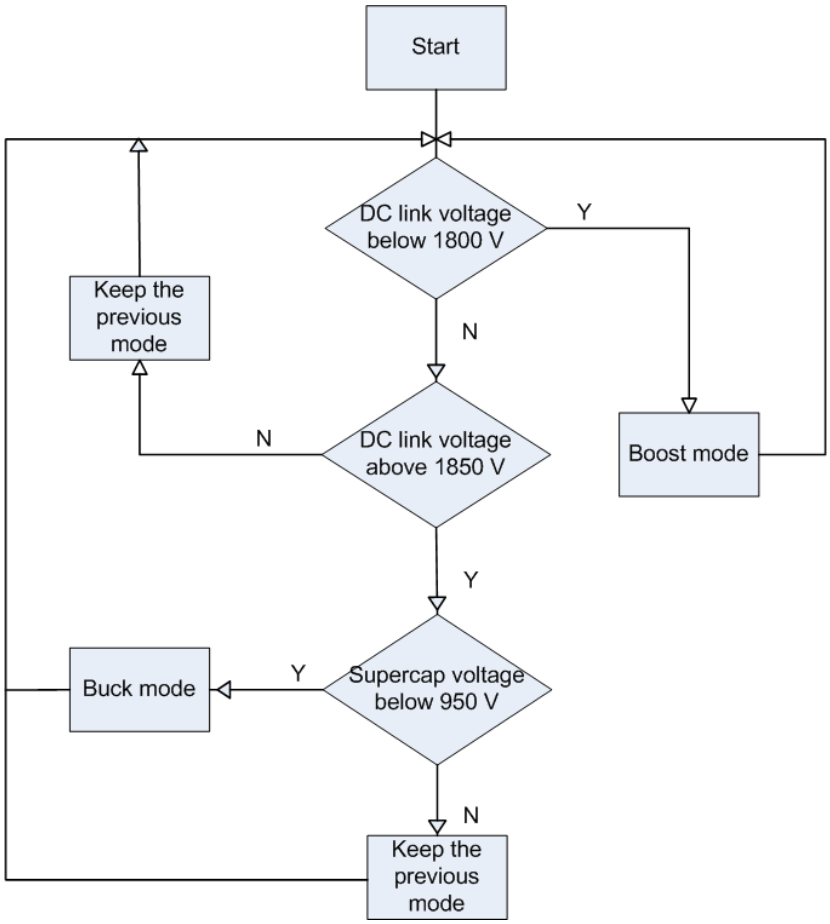

Figure 5.19: Flowchart of the control scheme

6. Case study for voltage sag mitigation solutions

In this chapter the methods and analysis that were described in previous chapters will be applied to a specific case. For this case all required component values will be calculated. The case in question concerns the EdeA network. This network contains three induction motors. Two motors, a 1.05 MVA motor with quadratic mechanical torque characteristic and a 6.53 MVA motor with constant mechanical torque characteristic, are connected to the 10,5 kV bus. The other motor, a 3.2 MW motor with constant mechanical torque characteristic is connected through a transformer on a 400 V bus. The total power of the system is 10.78 MVA. The motors are connected to the MVDC system through a 20 MVA transformer which transforms the converter voltage of 1100 V_{LL} to 10,5 kV_{LL} . Voltage sag mitigation shall be introduced for this EdeA subnetwork. The sags to be introduced have 10 and 90 percent remaining voltage, each during 50 ms and 1 second. Thus the maximum mitigation capability is required for 10 percent remaining voltage during 1 second.

In section 6.1 the required overrating that is necessary to mitigate these sags is analysed. Next mitigation of the given sags via a supercapacitor enhanced DC link is investigated in section 6.2. For this mitigation method, the steps given in section 5.6 are followed to determine the number of parallel and series supercapacitors needed for the supercapacitor bank. Also the inductor value and filter capacitor of the boost converter necessary for the supercapacitor interfacing are calculated in this section. Lastly the method for calculating the slope compensation given in section 5.4.1 is applied to calculate the necessary slope compensation using the newly calculated components. It should be noted that the overrating factor k_{or} for the MVDC system is initially set at 1.1 for the supercapacitor enhanced mitigation system. This value is chosen from cost point of view. As mentioned earlier, the higher the overrated system, the higher the costs because of the use of more and/or larger components.

6.1 Mitigation by overrated SIPLINK

In this section the required overrating factor to mitigate a sag as a function of sag magnitude and duration is investigated. With equations (2.3) and (2.4) which are repeated below the overrating factor k_{or} is calculated with varying sag magnitude, defined by *dip%,* and duration defined by Δt.

$$V_{dip} = V_{grid} \times dip\%$$

And

$$P_{load} = P_{grid\_dip} + \frac{dE_{dc}}{dt} = V_{dip} k_{or} I_{load} + \frac{\frac{1}{2} C_{DC} \Delta (V_{DC})^2}{\Delta t}$$

Table 6.1 give the definitions and values of the parameters of (2.3) and (2.4).

Parameter	*Description*	*Value*
V_{dip}	Remaining voltage	*Variable [V]*
V_{grid}	Grid phase voltage	$\frac{1100}{\sqrt{3}} V$
dip%	Sag magnitude	*Variable [pu]*
P_{load}	Power demanded by load	$10.78e^6\ W$
$P_{grid\ dip}$	Grid power during sag	*Variable [W]*
E_{dc}	DC link energy	*Variable [J]*
k_{or}	Overrating factor	*Variable*
I_{load}	Load phase current	*5658 A*
C_{DC}	DC link capacitor	*0.3 F*
V_{DC}	DC link voltage	*1892 V*
t	Sag duration	*Variable [s]*

Table 6.1: Parameter description and values of (2.3) and (2.4)

By varying the sag duration t and the sag magnitude *dip%* we obtain Figure 6.1. This figure gives the overrating factor k_{or} as a function of sag duration and magnitude.

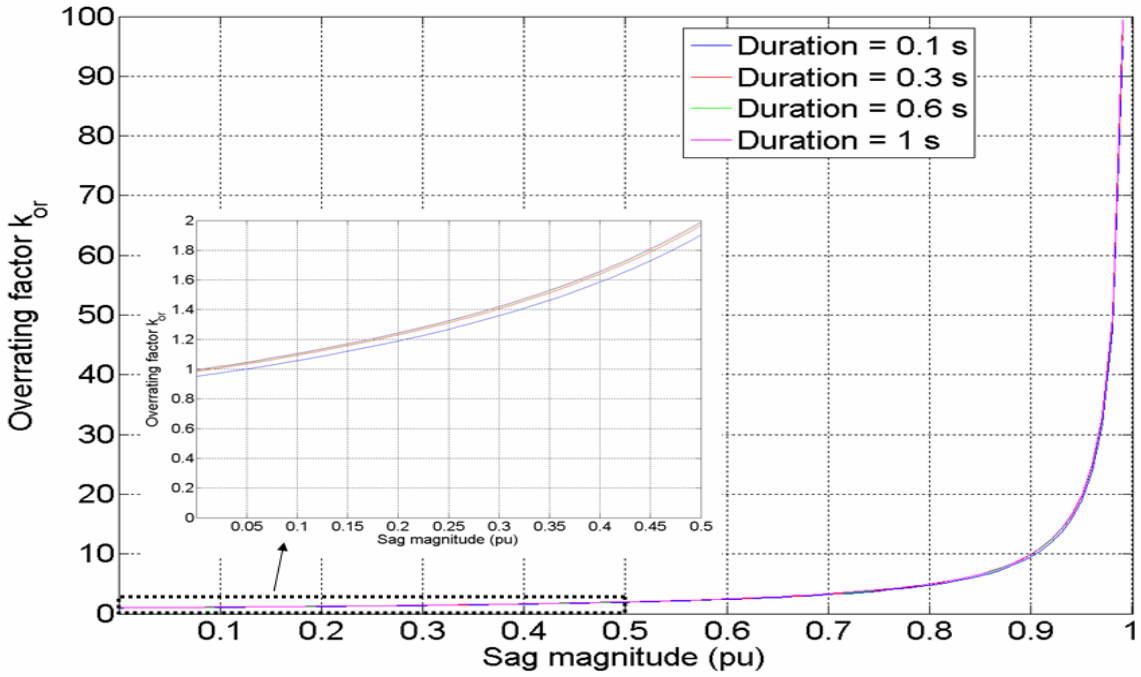

Figure 6.1: Overrating factors for different sag magnitudes and durations

As is visible from the figure, a very high overrating factor is needed for large sag magnitudes. This is of course not realistic from economic point of view. The inner picture gives more realistic values for the overrating factor. Here it can be seen that with an overrating factor of about 2, a 50 percent sag can be tolerated. Also at $k_{or}=1.1$ which is the value chosen for further computation a residual voltage of 90 percent can be tolerated. In the figure we can see that the lines are very close to each other indicating that the duration of the sag is not an important factor. This is to be expected because from (2.4) the sag duration is only important to determine the power available in the DC link capacitor. The capacitance value is very small, thus the contribution of the capacitor power to the total system during a sag is also very small. Therefore we can conclude that with a given overrating factor, the corresponding sag magnitude can be mitigated regardless of the duration of the sag.

6.2 Mitigation by supercapacitor enhanced SIPLINK

In this paragraph values for the boost converter components, i.e. inductor size, and supercapacitor size are calculated. The supercapacitor bank is sized so it can mitigate the worst case sag of 10 percent remaining voltage during 1 second.

6.2.1 Supercapacitor sizing

Paragraph 5.6 describes the steps necessary to size the supercapacitor bank. For this case study the Maxwell BMOD0018-P390 B01 supercapacitor module was considered. This module is chosen because of its high terminal voltage. Due to the high DC voltage of the MVDC system and the limited gain of the boost converter a high terminal voltage of the supercapacitor stack implies that fewer modules are needed to achieve the necessary voltage. The specifications of this module are given below. Up to three modules can be connected in series.

Item	Performance	
Nominal Operating voltage [Vdc]	390V	
Maximum Operating Voltage [Vdc]	394V	
Surge voltage [Vdc]	406V	
Nominal Capacitance [F]	17.8F	
Tolerance Capacitance [%]	+20% / -0%	
DC Series resistance [mΩ]	65.0	
Energy Available (Whr)	282	Energy Available equals 1/2C(Vnom^2–1/2Vnom^2) /3600
Self discharge [% of initial V]	50%	30 days RT 100V; 12 hours charge and hold
Maximum Continuous Current [A]	150A	Assuming 15 degree temperature rise above ambient temperature
Max current [A]	950A	
Lifetime 390V	150,000	End of life characterized as -20% C from nominal C, or increase of 100% in ESR
Cycles 390 to 62.5 Vdc, RT [cycles]	1,000,000	End of life characterized as -20% C from nominal C, or increase of 100% in ESR
Isolation Voltage [Vdc]	3500V	Maximum string operating voltage 1500V DC

Tabel 6.1: Supercapacitor module data

For the design of the boost converter a modular approach is desired. From a rough calculation the current flowing out of the converter is around 5000 A for the 9.5 MW compensation to a

DC bus voltage of about 1892 V. The input current i_i of the boost converter is larger than the output current i_o and is defined by $i_o = i_i(1-D)$. This means that the input current can become 10000 A for a duty ratio of 0.5. All components will have to be designed to be able to handle this high current, which could result in a bulky system. A non-modular approach implies also a lower reliability of the total compensation system. Failure of one component would take the whole converter offline. A modular approach implies that smaller converters are used that can each handle lower powers. By putting these converters in parallel more or less units can be added depending on the requirements for sag mitigation. This approach is more reliable because in the event of a converter malfunction only the broken converter needs to be taken offline while the rest continues to stand by for mitigation.

For the sizing of the capacitor bank the capacitor current is the important value that needs to be considered. The capacitor bank is sized such that it can handle the maximum current at the desired mitigation interval of 1 second. In order to find the minimal amount of parallel (n_p) and series (n_s) capacitor banks the steps described in section 5.6 are applied. By iterating n_p the current handling capability of the boost converter is changed. For the mitigation of voltage sags in this application, a constant power is desired. However the supercapacitor voltage decreases as the charge is depleted. Therefore more current needs to be delivered by the supercapacitor banks in order to uphold the power balance. The power delivered by the supercapacitor bank should be the same at the beginning of the sag, when the terminal voltage of the supercapacitors is the largest and the current is the smallest, and also at the end of the sag, when the terminal voltage is smallest and the current is largest. By iterating n_p also the capacitance value changes, therefore also changing the energy content of the supercapacitor banks. From Figure 2.3 it was deducted that 9.5 MJ is needed to compensate for a sag with 10 percent remaining voltage. Power not energy is the important factor however as the supercapacitor bank needs to be able to supply the 9.5 MJ of energy in 1 second, thus the sizing should be done such that 9.5 MW of power can be supplied. The steps taken below will iterate the amount of series connected supercapacitor banks $n_{s,}$ such that the maximum current is reached at 1 second and iterate the amount of parallel connected supercapacitor banks such that enough power is there to mitigate for a 90% sag during 1 second :

1. Assume a value for n_p. The maximum current that can be reached is then $I_f = n_p \times I_{\max}$ where I_f is the target final current for the numerical process and I_{max} is determined by the supercapacitor module.
2. Iterate n_s. This changes the initial voltage and thus also the initial current according to (5.27) i.e. $I_i = \dfrac{E_i - \sqrt{E_i^2 - 4R_{ESR}p}}{2R}$. Where E_i is the initial internal capacitor voltage, R_{ESR} is the equivalent series resistance of the supercapacitor, p is the delivered power and R is the load. By changing the initial current also the moment where the final target current is reached is changed.
3. Use (5.26) i.e. $\dfrac{di(t)}{dt} = \dfrac{-i(t)}{C\left(R - \dfrac{p}{i(t)^2}\right)}$ to find the current trajectory. Here C is the capacitance value of the supercapacitor. The current trajectory changes when n_s and n_p changes.
4. Compare the final value of each current trajectory to the target current. The correct current trajectory is determined when the maximum current that the supercapacitor bank can supply i.e. the final target current is reached after 1 second.

5. With each combination of n_s and n_p adjust the power p in step 3 to satisfy step 4. By varying p the maximum power that a given combination of n_s and n_p can deliver in 1 second is determined.

Once these steps are done and the correct values for n_s and n_p are found. Then using (5.25) :

$$\frac{dE(t)}{dt} = \frac{-CE(t) \pm \sqrt{C^2 E(t)^2 - 4R_{ESR}C^2 p}}{2RC^2}$$

the initial and final values of the terminal voltage can be calculated using the parameters from Table 6.1. When this is known, also the duty ratio of the converter is known.

The following table gives the results from the steps above.

n_p=1		E (Whr)	p_{max} (MW)	Converters parallel	Total modules	Weight(kg)	Power density (W/kg)
n_s	1	72.22	0.26	37	37	6105	42.27
	2	147.22	0.53	18	36	5940	89.23
	3	222.22	0.8	12	36	5940	134.68

Table 6.2: Supercapacitor sizing for n_p=1

n_p=2		E (Whr)	p_{max} (MW)	Converters parallel	Total modules	Weight(kg)	Power density (W/kg)
n_s	1	147.22	0.53	18	36	5940	89.23
	2	294.44	1.06	9	36	5940	178.45
	3	441.67	1.59	6	36	5940	267.68

Tabel 6.3: Supercapacitor sizing for n_p=2

From the tables above a decision cannot be made from the amount of modules needed. The decisive factor is determined by the power density. From this point of view a converter with n_p=2 and n_s=3 yields the best results.

The voltage characteristics for this combination determined by (5.25) and (5.20) is presented in Figure 6.2. From this figure it can be seen that the duty ratio D varies $0.46<D<0.55$. The current mode controller designed for the boost converter should thus vary the duty ratio between these values. Also because the duty ratio at one point increases above 0.5, also slope compensation must be designed to guarantee stable operation of the controllers.

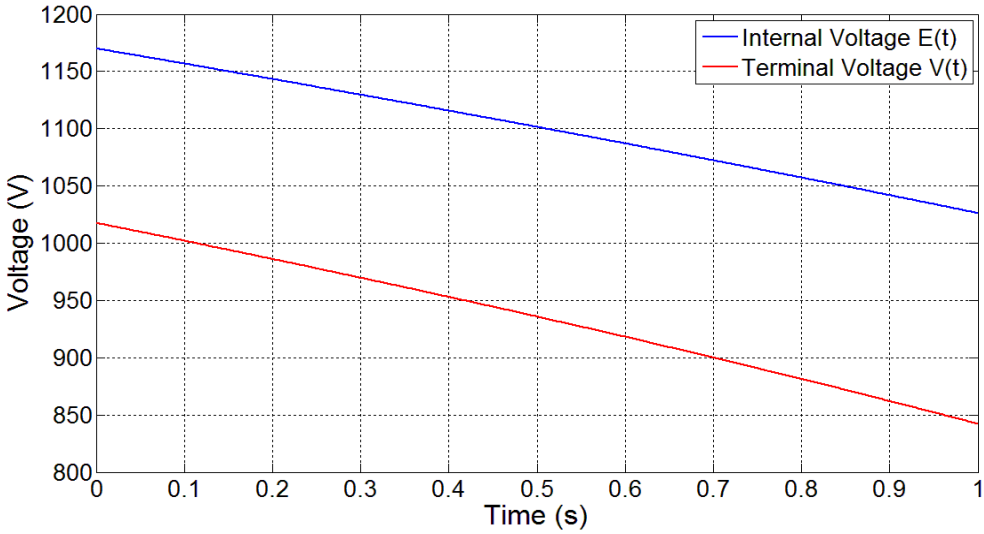

Figure 6.2: Terminal and internal voltage of the supercapacitor bank for $n_s = 3$ and $n_p = 2$

The current waveform which is calculated by equation 4.23 is given in Figure 6.3.

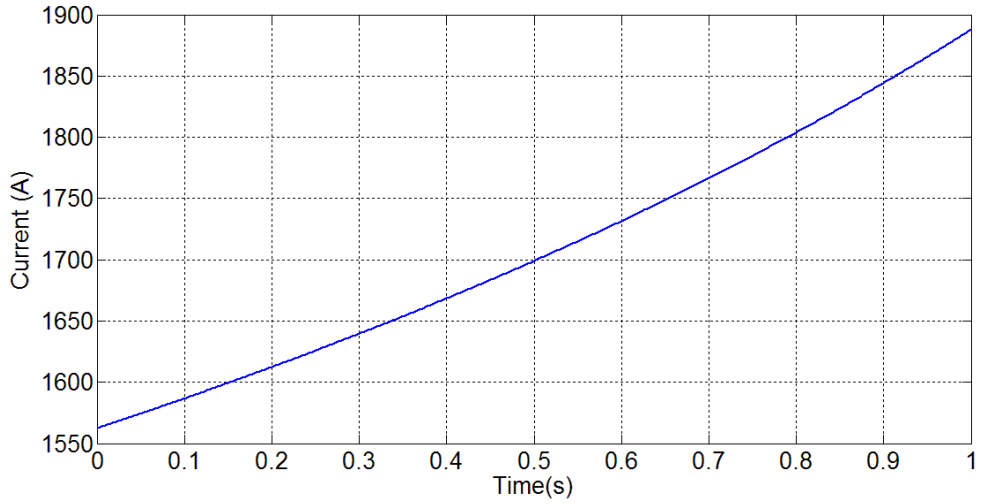

Figure 6.3: Capacitor current of the supercapacitor bank for $n_s = 3$ and $n_p = 2$

6.2.2 Inductor calculation

Next the inductor for each individual converter is calculated. From section 5.2 the inductor size is calculated using equations (5.4) through (5.10). To minimize the stress on the supercapacitor banks and the switches, a small inductor current ripple is desired. For this thesis the inductor current ripple is chosen to be 2% of the dc component of the inductor current. From (5.10) it follows that a high frequency gives smaller components. The converter frequency is thus chosen to be 3 kHz. Since the voltage of the supercapacitor will continuously decrease during the operation of the boost converter, the control will have to vary the duty ratio of the switch in order to keep the output voltage constant at 1892 V. Different values for the duty ratio give different inductor values according to (5.10) repeated below:

$$\Delta i_{sc} = \frac{V_{sc}}{2L} D T_s$$

Where V_{sc} is the terminal voltage and varies according to Figure 6.2., D is the duty ratio and varies in this case between 0.46 and 0.55 and T_s is the switching period and is equal to 1/3e^3. The ripple Δi_{sc} is required to be 2 percent of the DC component of the inductor current which is the same as the capacitor current given in Figure 6.3. Filling in (5.10) results in Figure 6.4. From Figure 6.4 the largest inductor value is chosen to guarantee the desired ripple at every duty ratio.

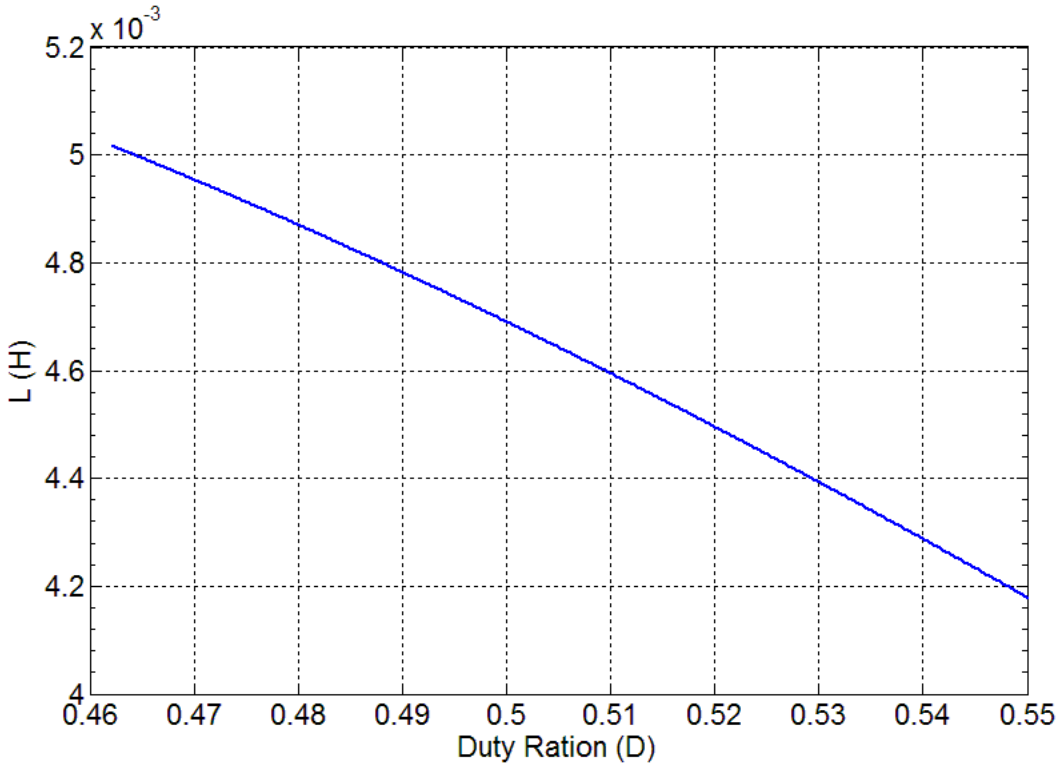

Figure 6.4: Inductor value with varying duty ratio

From this figure it is clear that a maximum inductor value of 5.05 mH is needed.

Now the output filter capacitor can be determined using equation (5.13) repeated below:
.

$$\Delta V = \frac{I_{aux}}{C} DT_s = \frac{P}{CV_{dc}} DT_s$$

To calculate the output capacitor, an output voltage ripple of at most 15 % is allowed. Rearranging we obtain:

$$C = \frac{pDT_s}{\Delta V V_{dc}} = \frac{9.5e^6 \times D \times \frac{1}{3e^3}}{0.15 \times 1892 \times 1892} \qquad (5.30)$$

Varying the duty ratio from 0.46 to 0.55 a capacitor value of 2.7 mF < C < 3.2 mF is obtained. Higher duty ratios result in larger output capacitor values.
Since the DC link capacitor, C_{DC} = 300 mF, this suffices as the output capacitor for the boost converter.

6.2.3 Slope compensation

As described in section 5.4.1 the boost converter circuit creates sub-harmonic oscillations in the inductor current for duty ratios over 0.5. This problem can be solved by adding an artificial ramp to the sensed switch current. The artificial ramp reduces the gain of the inner switch-current sensing discrete feedback loop. Using equation (5.2) with $D \geq 0.5$ and V_{dc} = 1880 V gives $V_{sc} \leq 940V$. Using equation (5.16) with *L=5.05 mH* gives $m_a = -9.31e^4 V/s = -31\ V/_{1/3e^3}\ s$. A triangular waveform with this slope will be added to the sensed switch current to remove the sub-harmonic oscillations in the inductor current.

7. Results Voltage Sag Mitigation Solutions

This chapter illustrates the results obtained from the Simulink SimPowerSystems models of the SIPLINK and industrial grid for the case study. Paragraph 7.1 gives the results obtained for an overrated SIPLINK. The results are to confirm that equations (2.3) and (2.4),which give the relation between the overrating factor k_{or} and the sag magnitude and duration, hold and that the graphical interpretation derived from these equations given in Figure 6.1 is correct. From Figure 6.1 it can be seen that endless combinations of sag duration, magnitude and overrating are possible, but only one is given. Specifically an 80% overrated SIPLINK is designed to prove the case that a 45% voltage sag lasting 1 second can be compensated for. To illustrate the results the following figures are illustrated:

1. Grid RMS line voltage V_{grid} RMS
2. Grid RMS phase current I_{grid} RMS
3. DC voltage V_{dc}
4. DC current I_{dc}
5. Load RMS line voltage V_{load} RMS
6. Load RMS phase current I_{load} RMS
7. Motor speed in per unit
8. Rectifying converter controller currents

Paragraph 0 shall illustrate the four cases representing different combinations of sag magnitude and duration given in Table 1.2 for a supercapacitor enhanced SIPLINK. The results that will be illustrated are equal to those from paragraph 7.1 and additional plots are given that illustrate the operation of the bidirectional boost converter. These plots are:

1. Converter output current I_{aux}
2. Converter output power P_{aux}
3. Inductor current I_L
4. Supercapacitor internal voltage V_{sc}

7.1 Results Sag Mitigation by Overrated SIPLINK

A voltage sag of 45 percent lasting 1 second is introduced in the grid side voltage. The results will show how the waveforms of the RMS grid side voltage, the RMS grid side phase current, the DC voltage, the DC current, the RMS load side voltage, the RMS load side phase current and finally the induction motor speeds react to this sag. The speeds shown are from an 1.05 MVA motor supplying a mechanical torque quadratic to its speed in p.u. and operating on the 10.5 kV bus, a 6.53 MVA motor supplying constant mechanical torque also at the 10.5 kV bus and lastly a 3.2 MVA motor supplying a constant mechanical torque and operating on the 400 V low voltage bus. In every figure three cases are shown, namely the normal operation (i.e. without a sag) a non-overrated SIPLINK and a 80% overrated SIPLINK. In all figures the sag starts at 0.25 seconds and ends at 1.25 seconds. The blue lines in every figure represent the normal operation, the red line represents a non-overrated system and the green lines represent an 80% overrated system.

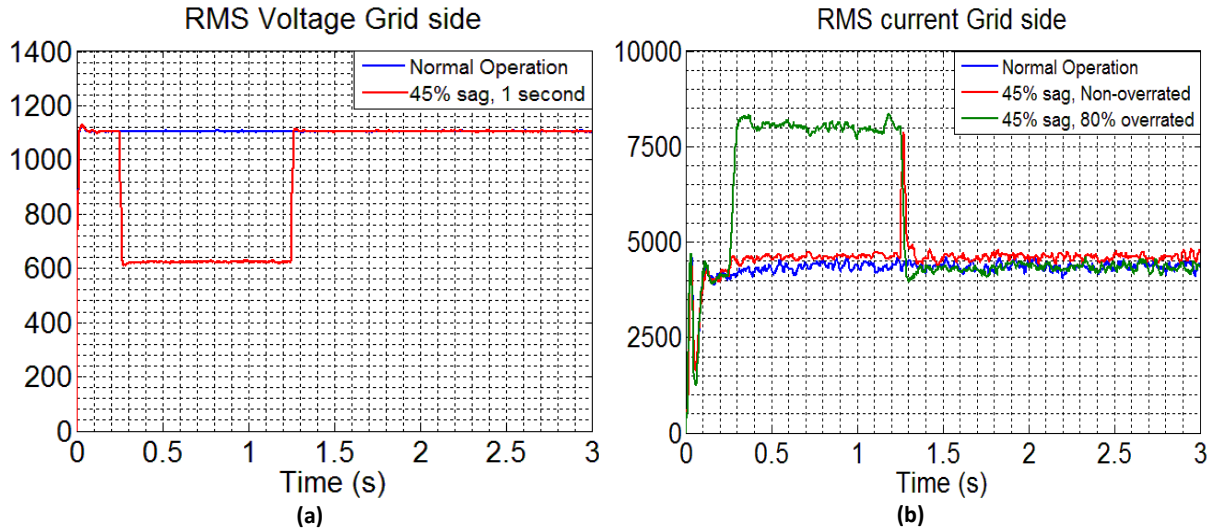

Figure 7.1: Grid side RMS voltage (a) and current (b) for normal operation and during a 45% sag for 1 second for an overrated and non-overrated system

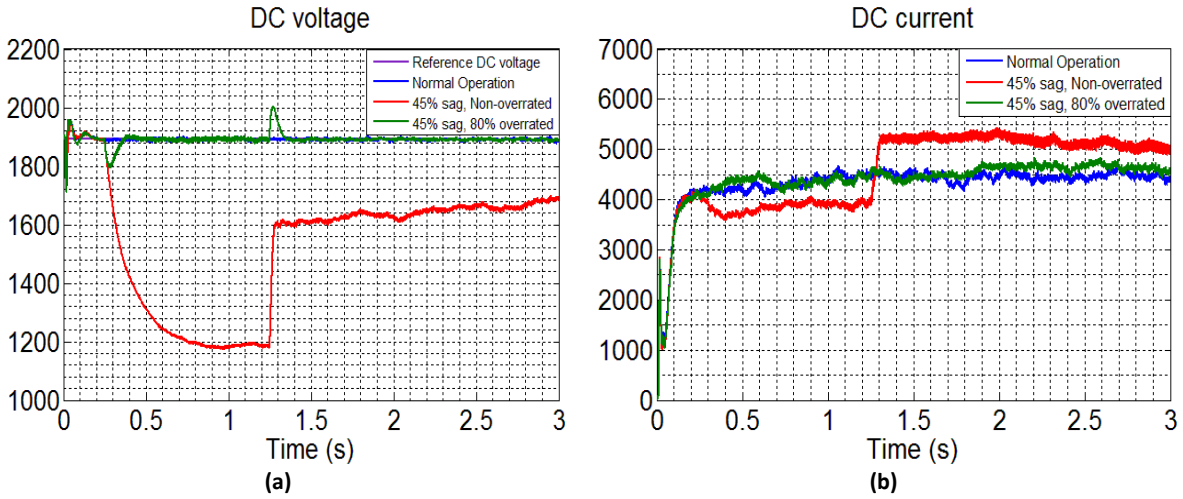

Figure 7.2: DC link voltage (a) and current (b)) for normal operation and during a 45% sag for 1 second for an overrated and non-overrated system

In Figure 7.1 (a) the 45% sag in the grid voltage is shown. Next in Figure 7.1(b), the current waveforms of each mode of operation is visible. It can be seen that during the sag, the converter that is 80% overrated draws extra current from the grid in order to uphold the power balance. The current for the non-overrated converter is slightly higher than in normal operation because the load current is slightly under the converter rated current. In the current waveform of the non-overrated converter a large peak occurs when the sag has been cleared. This is caused by the motors that have slowed down during the sag and that are now speeding back up because the sag has been cleared as is visible in Figure 7.4 (b). This speeding up of motors draws large currents. It is the task of the converter controllers to limit the current by setting a correct current reference value for the actual grid side currents to follow. However now there are two occurrences that counteract each other; the motors demanding very high currents on one side and the converter controller dictating a very low current as compared to the demanded current. The converter dynamics result in the converter initially supplying the demanded current before following the dictated reference current as it normally should. See Figure 7.6. This phenomenon does not happen at the beginning of the sag because the motors are already at their rated speed and do not demand high currents. The converter current is then perfectly able to follow the controller current.
The overrated converter does not encounter high current peaks as the non-overrated converter. When the sag occurs, the controllers very quickly dictate a higher reference current which makes the grid side converter draw extra current from the grid. An 80% higher current than the normal rated current is now drawn from the grid to uphold the power balance.

Next in Figure 7.2 (a) it is shown that the DC voltage of the non-overrated converter also shows a significant sag. After the sag, the DC voltage does not return to its original value again because of the large currents being drawn due to the motors starting up.
The overrated converter is however able to maintain its DC voltage (Figure 7.2 (a)) and only shows slight peaks at the start and end of the sag. This is caused again by the converter dynamics which do not allow instant state changes. The DC current in Figure 7.2 (b) for the overrated converter follows the current during normal operation closely. The current for the non-overrated system initially starts to drop and is higher than the converter current during normal operation at the end of the sag, again because of the large currents being drawn by the motors speeding back up.

From Figure 7.3 (a) it is clear that the overrated system is able to maintain the rated voltage almost as well as in the normal operation. The voltage for the non-overrated system is clearly dropping. The large currents drawn in Figure 7.3 (b) by the non-overrated system causes the drop in the load voltage after the sag has cleared. Remember that the load side converter does not have a current controller like the grid side converter, thus the currents are not limited. In such a case, a breaker would open causing the system to trip to avoid the whole system to be overloaded. With a current controller in the load side converter, the currents would be limited, making it impossible for the motors to draw such excessive currents and speeding up simultaneously. In this case the speed of the motors would continue to decrease until a stop.

This case has shown that the graphical interpretation of converter overrating versus sag magnitude in Figure 6.1 holds. The converter currents can be controlled quickly to a higher value leading to a minimal drop in speed for the overrated converter as compared to the non-overrated converter. One can conclude thus that converter overrating is an effective way of dealing with voltage sags. There were no requirements for the variation in speed of the motors during a voltage sag for an overrated converter. Figure 7.5 shows a speed variation of a few

tenths of a percent at the start and end of the sag. The magnitude of the speed variation depends on how fast the converter reacts to a voltage sag and how quickly the current can be controlled to the necessary value. In any case the overrated converter gives much better results than a non-overrated one. Also provided that the system is well designed to handle extra currents i.e. suitable valves, cabling, electronics and very important cooling, a sag of this magnitude can last indefinitely without causing problems in an overrated system.

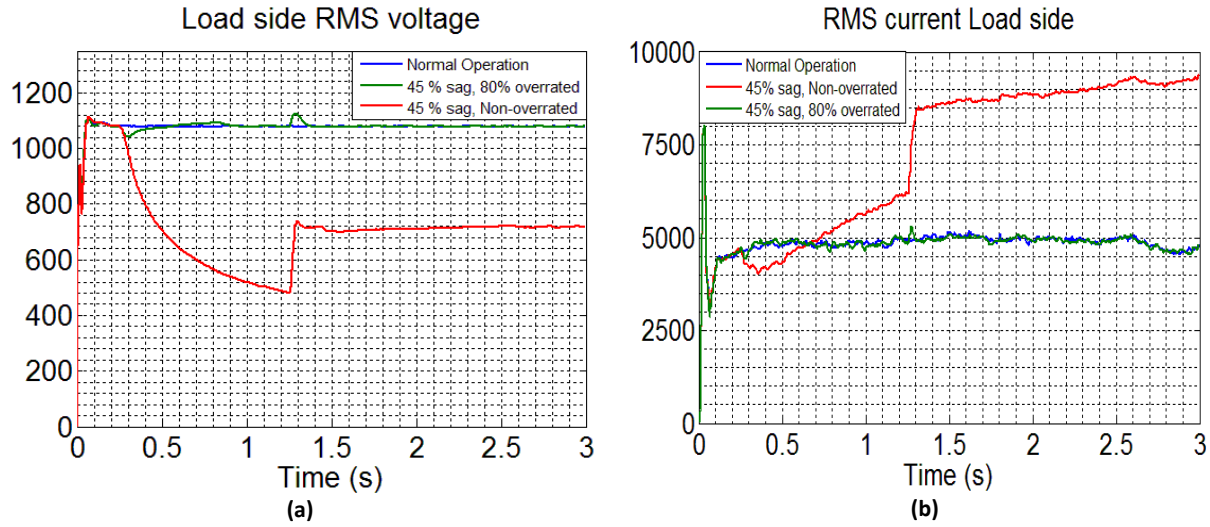

Figure 7.3: Load side RMS voltage (a) and current (b)) for normal operation and during a 45% sag for 1 second for an overrated and non-overrated system

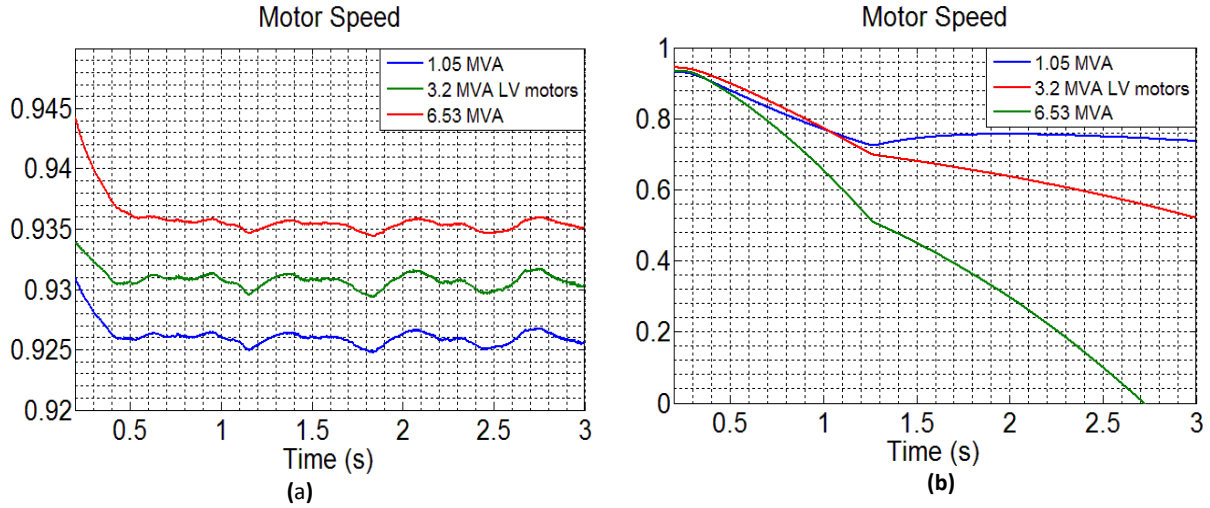

Figure 7.4: Motor speed during normal operation (a), 45 % sag non-overrated converter (b)

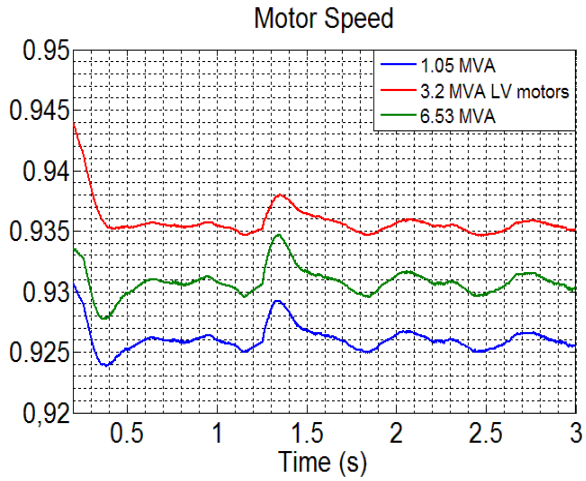

Figure 7.5: Motor speed during 45 % sag and 80% overrated converter

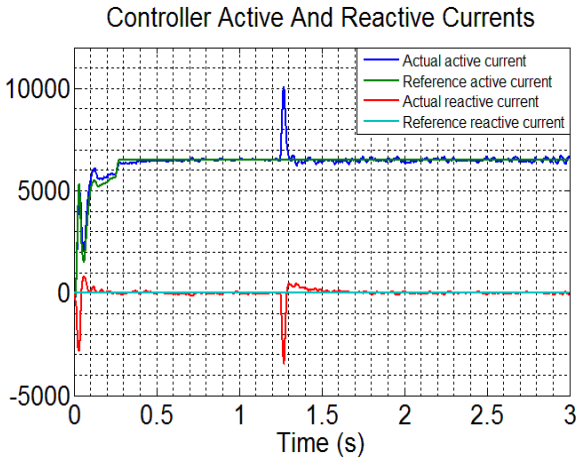

Figure 7.6: Rectifying converter controller current during 45% sag for a non-overrated system showing large peaks in the actual currents when the sag has cleared

Next the results for an overrated and non-overrated converter are shown for the case in which a 45 percent sag has occurred which lasts 50 ms. The purpose for the showing of these waveforms is to show if the overrated converter is fast enough in controlling the current to a higher value so the power balance is kept and the motor speed is not affected. Here the sag is introduced at t = 1 s and cleared again at t=1.05 s.
As can be seen in Figure 7.7 (b) the current for the overrated system is controlled quickly to its maximum value at t=1 s. The sag is cleared again very quickly after 50 ms. The DC voltage, Figure 7.8 (a) for the overrated system shows less drop in magnitude than the non-overrated system. This translates to a smaller variation on the load side RMS voltage of the overrated converter, Figure 7.9 (a).

Figure 7.10 (a) shows a 1 percent drop in speed of the motors for the non-overrated converter and a 0.2 percent drop in speed for the overrated converter. For this thesis there was no real requirement for the allowed drop in speed. But this author concludes that a 50 ms sag is not long enough to give a significant drop in speed for a non-overrated system and overrating of the converters should not be considered when one wants to deal with sags of such short duration.

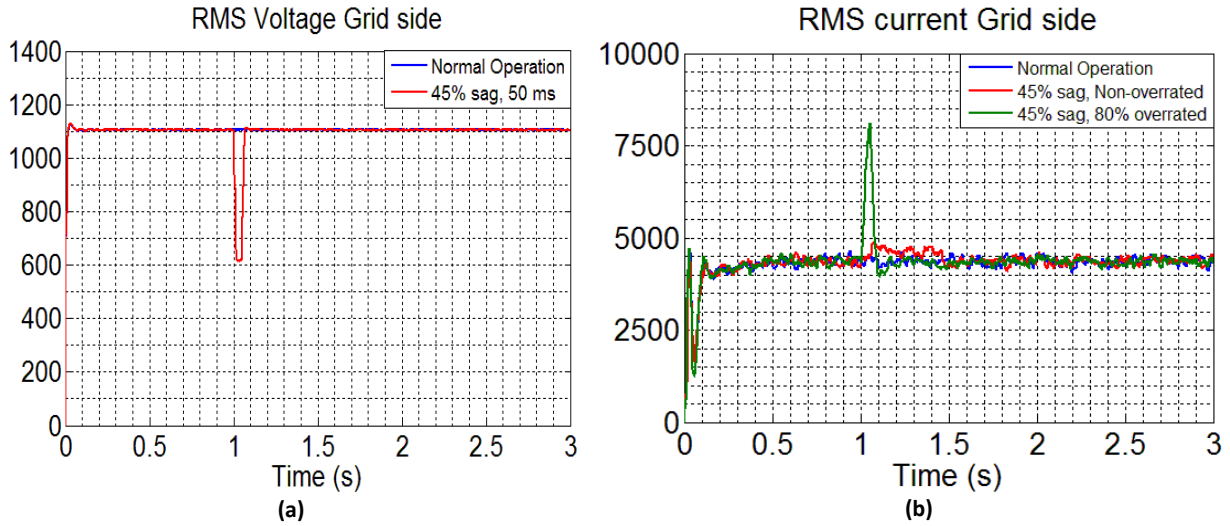

Figure 7.7: Grid side RMS voltage (a) and current (b) for normal operation and during a 45% sag for 50 ms for an overrated and non-overrated system

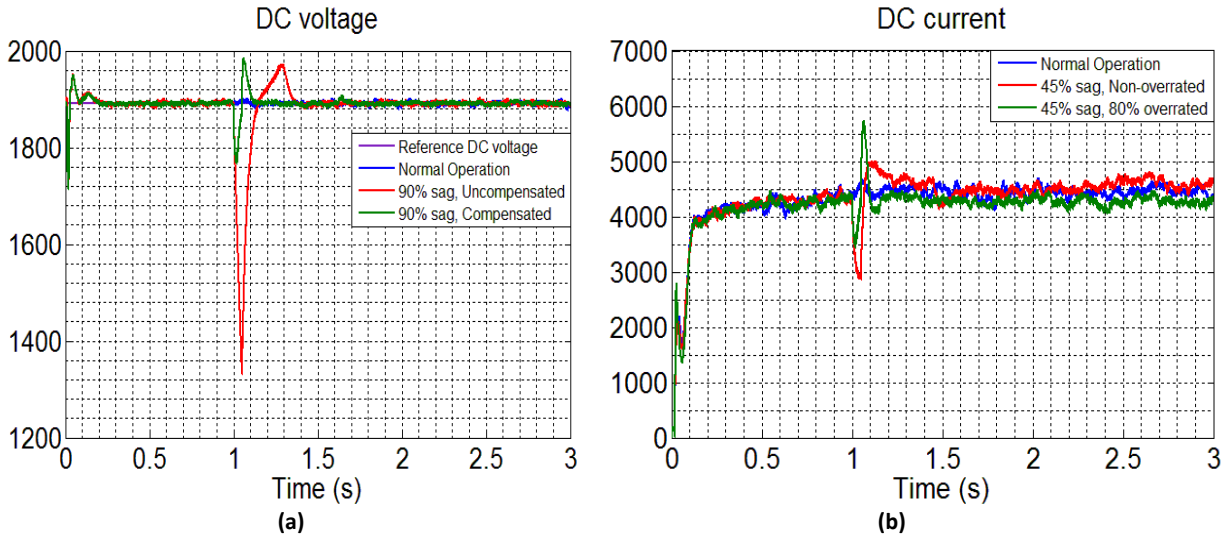

Figure 7.8: DC link voltage (a) and current (b) for normal operation and during a 45% sag for 50 ms for an overrated and non-overrated system

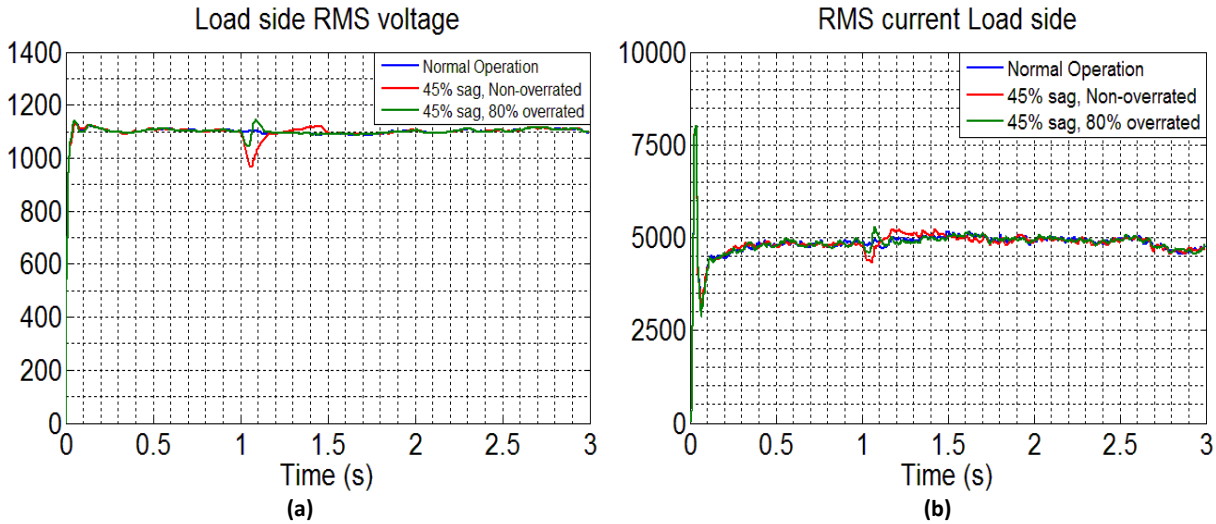

Figure 7.9: Load side RMS voltage (a) and current (b)

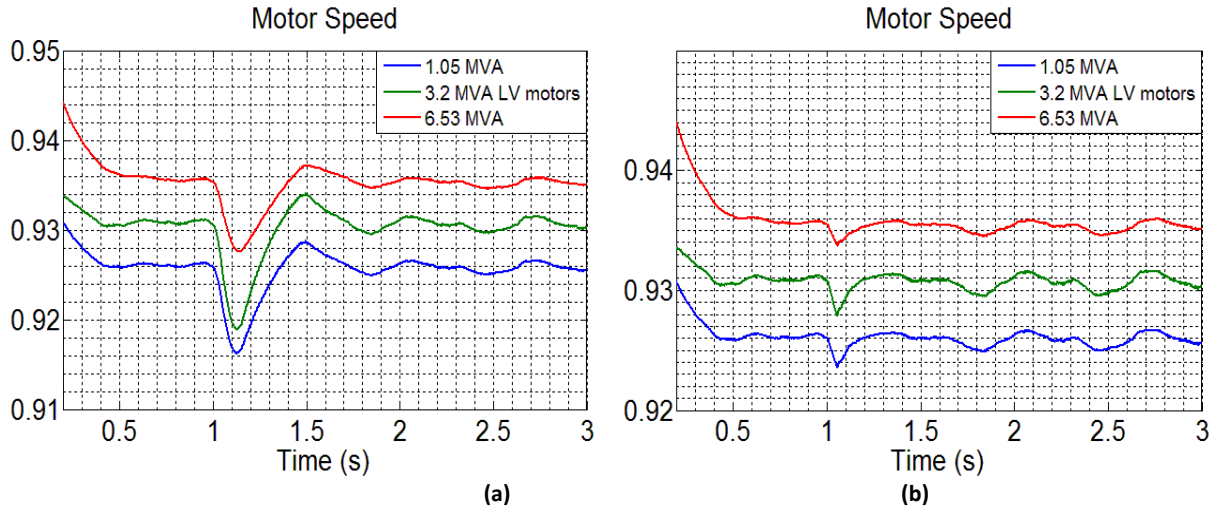

Figure 7.10: Motor speed during a 45 % sag for a non-overrated converter (a) and 80% overrated converter (b)

7.2 Results Sag Mitigation by supercapacitor

In this section sag mitigation is provided by a supercapacitor enhanced auxiliary supply. The sags that will be investigated are again summarized in Table 7.1. Recall that a 10 percent overrated converter will be used as a base case to test the applicability of a supercapacitor enhanced DC link. From the previous chapter we have already seen that an 80 percent overrated converter can mitigate a 45 percent sag as suggested by Figure 6.1. Thus we can assume that a 10 percent overrated converter is able to mitigate a 10 percent sag. For this reason, the cases in the second row of Table 7.1 will not be analysed in this section as it is assumed that the supercapacitor module is not needed to compensate for these sags. The two cases of the first row i.e. a 90 percent sag during 1 second and a 90 percent sag during 50 milliseconds remain to be analysed. For each case three waveforms are given in one figure namely the waveforms during normal operation with no sag (blue lines), the waveforms of a non compensated SIPLINK converter (red lines) and the waveforms with a supercapacitor enhanced auxiliary supply (green lines) both with the sag induced in the grid side voltage. The results will show the RMS line voltage and RMS phase current waveforms of the grid side converters as well as from the load side converters. Also the DC link voltage and current waveforms will be shown. The speeds of the induction motors which indicate the successfulness of the mitigation are also given. Also here the speeds shown are from an 1.05 MVA motor supplying a mechanical torque quadratic to its speed and operating on the 10.5 kV bus, a 6.53 MVA motor supplying constant mechanical torque also at the 10.5 kV bus and lastly a 3.2 MVA motor supplying constant mechanical torque and operating on the 400 V low voltage bus. In the cases where the sag is mitigated by a supercapacitor enhanced auxiliary supply, also the auxiliary current waveform, which is the total current of the auxiliary supply that flows into the DC link, is shown as well as the auxiliary power supplied. Lastly also the inductor current of one individual bidirectional boost converter is shown as well as the supercapacitor internal voltage.

Remaining Voltage	**Duration (ms)**	
90%	50	1000
10%	50	1000

Table 7.1: Voltage Sags enforced on industrial system

Next a 90 percent sag which starts at t=0.25 s and that lasts for 1 second is induced and the waveforms analysed. Figure 7.11(a) shows the effect of the sag on the RMS grid side voltage. For the both systems the current in Figure 7.11(b) is increased corresponding to the 10 percent overrating factor. At the end of the sag a peak occurs in the current from the uncompensated system which is explained by the converters initially drawing extra current due to the motors speeding back up, before following the controller dictated reference currents.
In this case with the non compensated system also the DC voltage is affected by the sag, Figure 7.12 (a) and drops significantly. The converters are not able to draw extra current from the grid to uphold the power because they are limited. Thus the DC voltage collapses. Because of the reduced DC voltage, the RMS voltage on the load side also has a significant reduction in magnitude Figure 7.13 (a). Obviously without some kind of compensation, the motors will be fed with a reduced voltage. Without enough power to feed them, the motors will slow down, Figure 7.14 (a). When the voltage returns, all motors will try to accelerate at the same time drawing large currents as can be seen in Figure 7.13 (b), and causing a voltage drop in the load side voltage. Again due to the current limitation of the rectifying converters, the amount of current that can be drawn is limited. The motors are not able to draw all the necessary current needed to start up, making them unable to speed up and finally this leads to

further reduction of the speed as can be seen in Figure 7.14 (a). Only the induction motors which operate as a pump do not slow down completely but keep operating at a greatly reduced speed. This is because the mechanical torque that the motor needs to deliver is quadratic to its speed, meaning that when the speed reduces, also a reduced torque is required. Though the field of the motor is weakened, the motor is still able to generate speed when a lower load is applied. The constant load of the other motors however reduces their speeds eventually to a standstill.

Next the compensated converter is discussed. The green lines everywhere in the figures show the waveforms with a supercapacitor enhanced SIPLINK. At the start of the sag current is injected from the supercapacitor enhanced auxiliary supply to the DC link. It is obvious that the compensation is fast enough to supply the DC link with the necessary current to uphold the DC voltage and RMS load side voltage and current. This ultimately leads to very small variation in motor speeds in the order of a few tenths of percentage, Figure 7.14 (b).

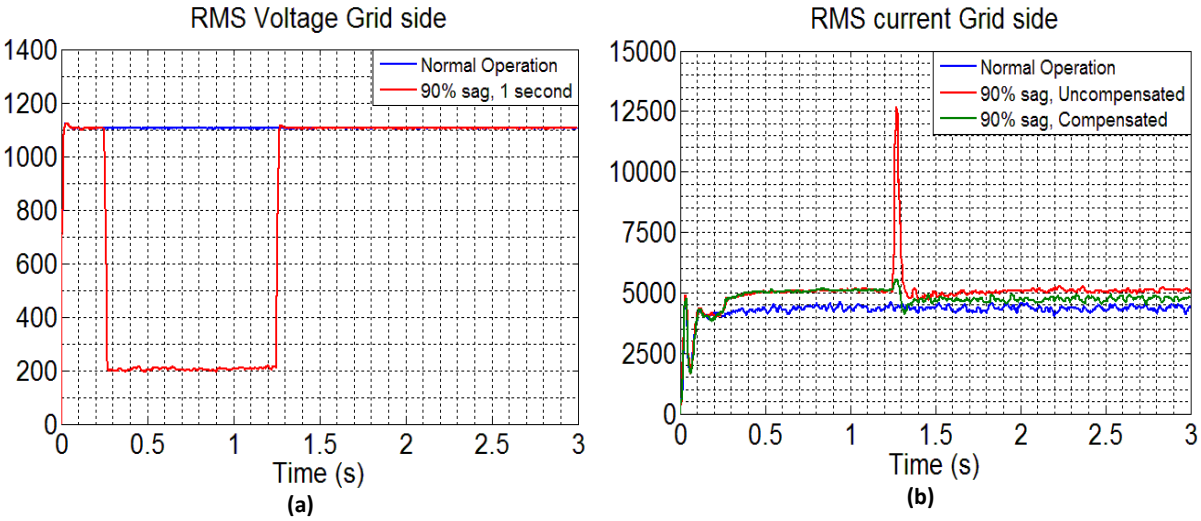

Figure 7.11: RMS Grid side voltage (a) and current (b) for a 90% sag lasting 1 second

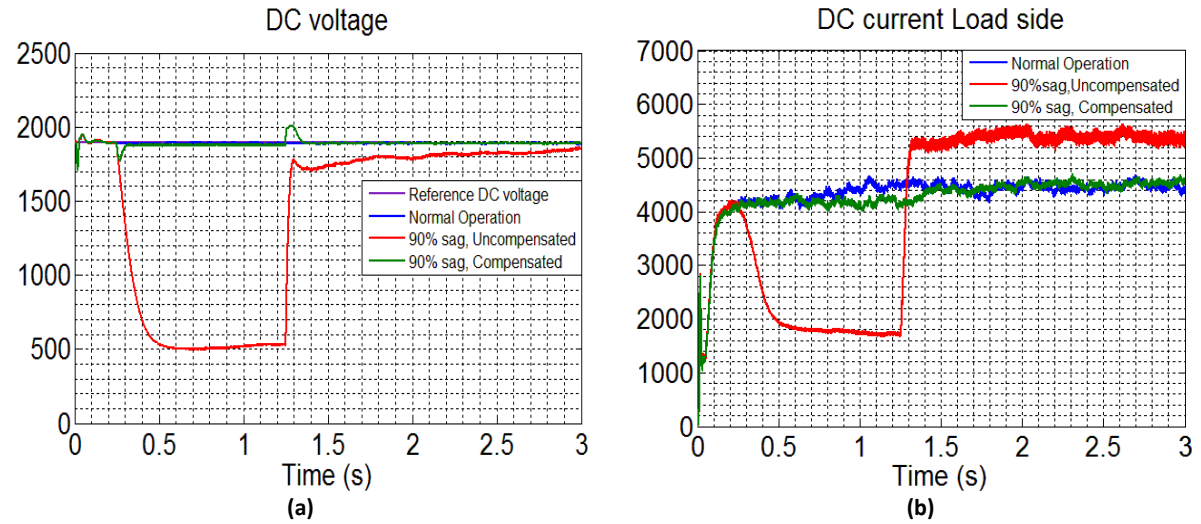

Figure 7.12: DC voltage (a) and current (b)

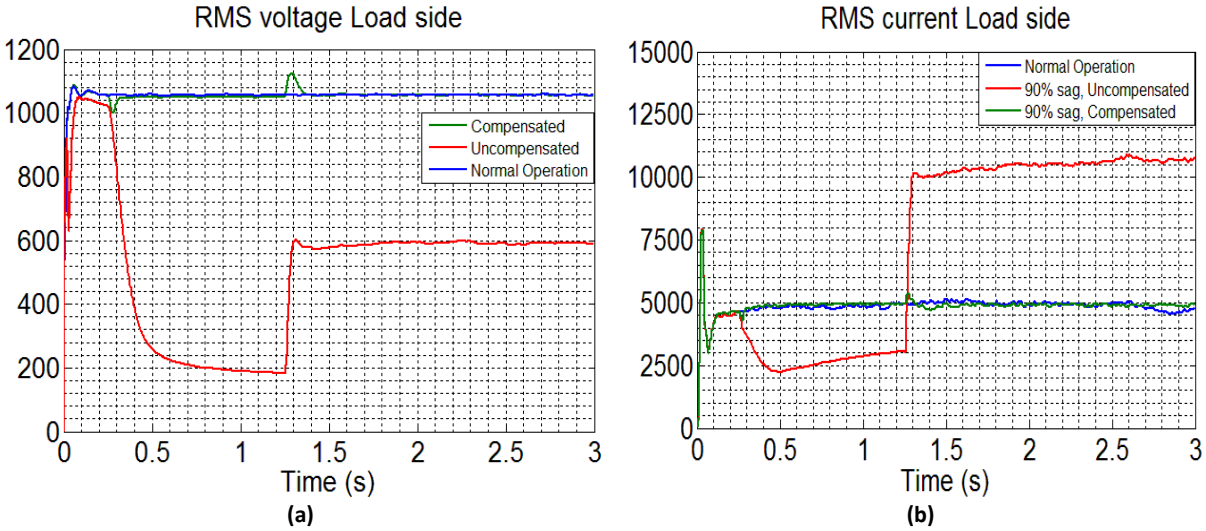

Figure 7.13: Load side RMS voltage (a) and current (b)

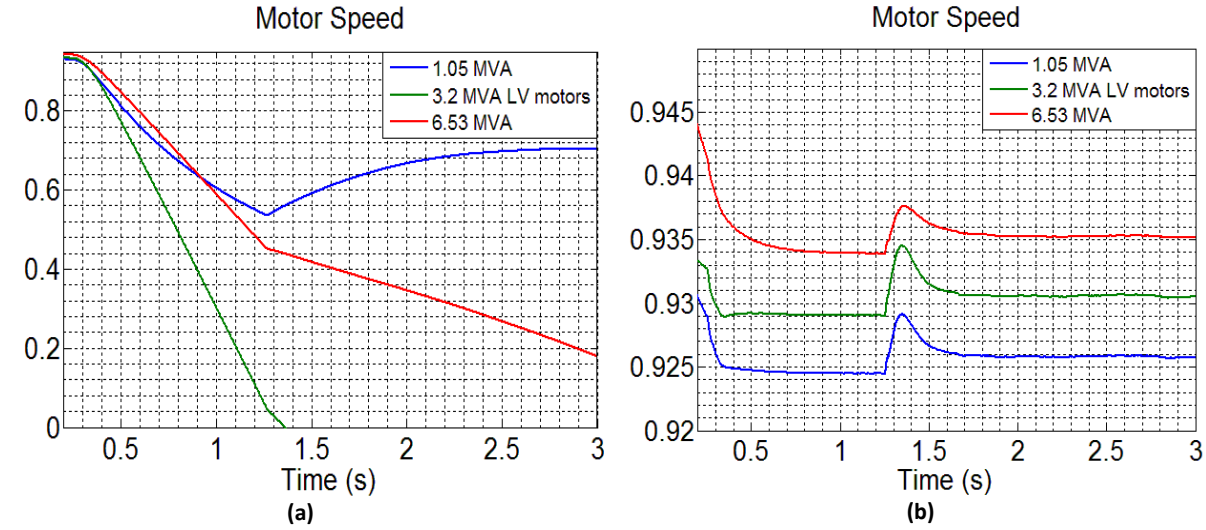

Figure 7.14: Motor speed during a 90% voltage sag for 1 second with an uncompensated SIPLINK network (a) and compensated SIPLINK network(b)

Next the waveforms for the compensating boost converter are shown. In Figure 7.15 (a) and (b) the auxiliary current and resulting power are shown. We can see that a mean current of 4000 A flows into the DC link at 1880 V. This corresponds to a power of about 7,5 MW which is shown in Figure 7.15 (b). Figure 7.16 (a) also shows the current through the inductor for one of the 6 boost converter compensating modules. This can be compared to the calculated waveform of Figure 6.3. The inductor current waveform has the same increasing form as from Figure 6.3 but with a lower value. The waveform of Figure 6.3 was calculated for one boost converter with its supercapacitor banks supplying 1.59 MW of power. It was calculated that 6 of these converters are needed to supply the necessary 9.5 MW of power in the case of a 90 percent sag. However the auxiliary supply needs to supply only about 7.5 MW of power. Thus each converter can supply less than the calculated current of Figure 6.3. The reduced necessary power is due to the motors drawing less than the 10.78 MW power in steady state mode than assumed for initial calculations.

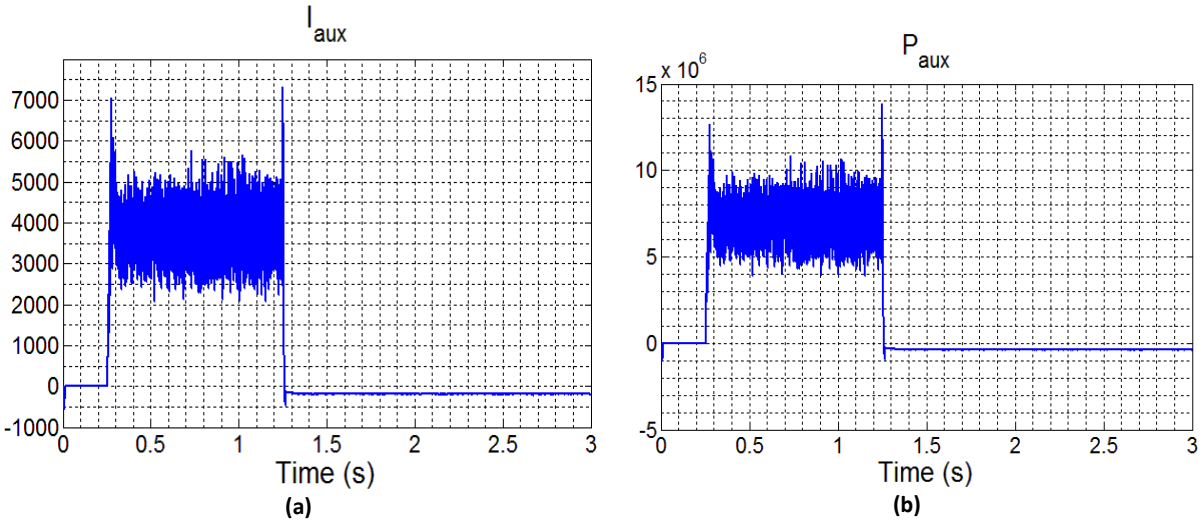

Figure 7.15: Auxiliary current (a) and power (b) from supercapacitor enhanced boost converters during a 90% voltage sag for 1 second

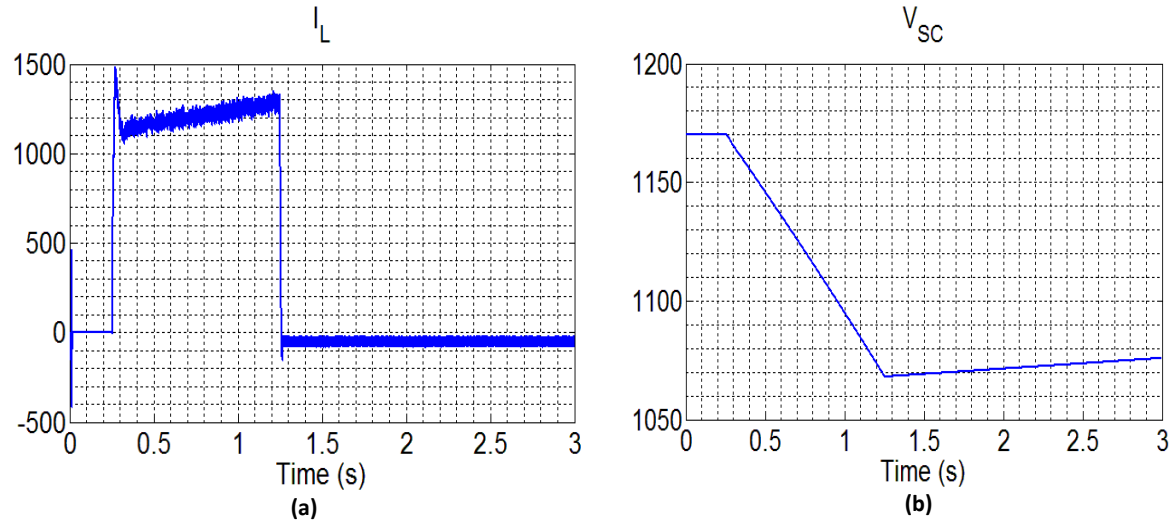

Figure 7.16: Inductor current of one boost converter module (a) and supercapacitor internal voltage (b) during a 90% voltage sag for 1 second

After the sag has been cleared the inductor current waveform is negative, meaning that now current flows into the supercapacitor banks charging them back up. The maximum charge current is 10 percent of the rated SIPLINK converter current as discussed earlier. See from Figure 7.15 (a) that about 200 A is drawn from the DC link of the SIPLINK converters to charge all six supercapacitor modules. The internal voltage of the supercapacitor during the discharge and charge of the module during the sag is given in Figure 7.16 (b). Compare this to the waveform given in Figure 6.2. At this charging rate, the supercapacitor modules are then fully charged in about 18 seconds. Due to computer memory constraints the full charge and discharge cycle cannot be shown. It is still clear though from the above given figures that the supercapacitor enhanced auxiliary supply charges and discharges according to the control scheme of Figure 5.19.

Next the waveforms are given for a sag of 90% lasting 50 milliseconds. The waveforms will show the effect that such a short voltage sag has on the total system while being compensated by an auxiliary supply. Also the non compensated system waveforms are shown. The speed of the induction motors with and without sag mitigation is the important parameter to watch as in the previous cases. First the grid side RMS voltage and current are given in Figure 7.17 (a) and (b). It can be seen that at t=1s a sag is applied and this sag is cleared at t=1.05s. In Figure 7.17 (b) it is clear that both the compensated and uncompensated converter start drawing extra current from the grid as soon as the sag is sensed. The extra current being drawn lasts longer for the compensated than for the uncompensated converter because of the charging back of the supercapacitors after the sag which is shown in Figure 7.22 (b).

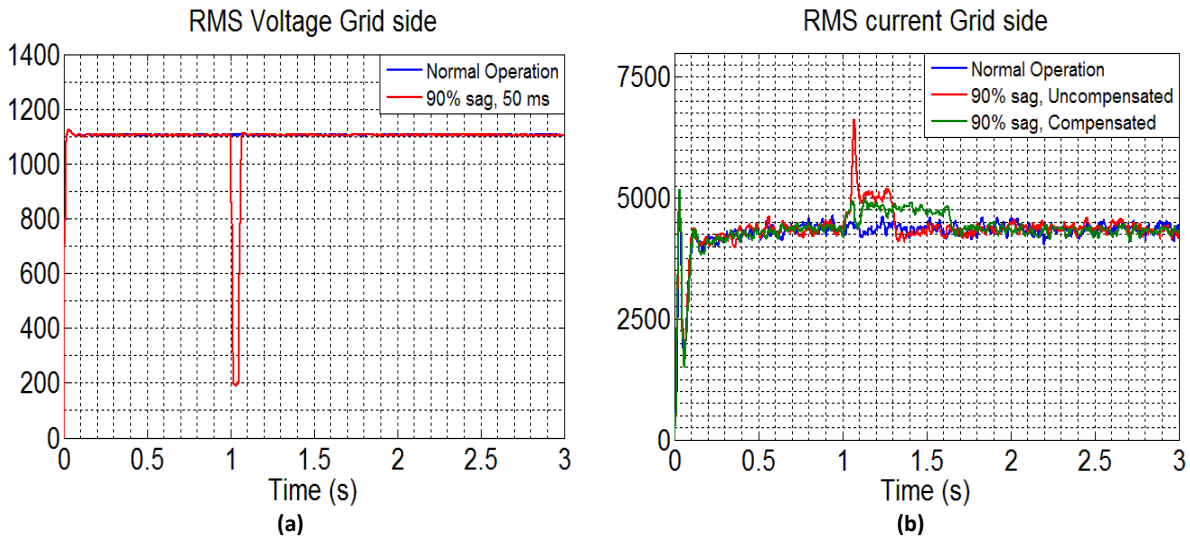

Figure 7.17: RMS Grid side voltage (a) and current (b) for a 90% sag during 50 ms

See from Figure 7.18 (a) that without compensation the DC voltage drops down almost to 1300 V, possibly tripping an undervoltage protection circuit. The DC voltage of the compensated circuit only sags until a little below 1800 V at which point the auxiliary circuit injects current in the DC link, Figure 7.18 (b) (red line) boosting the voltage back up.

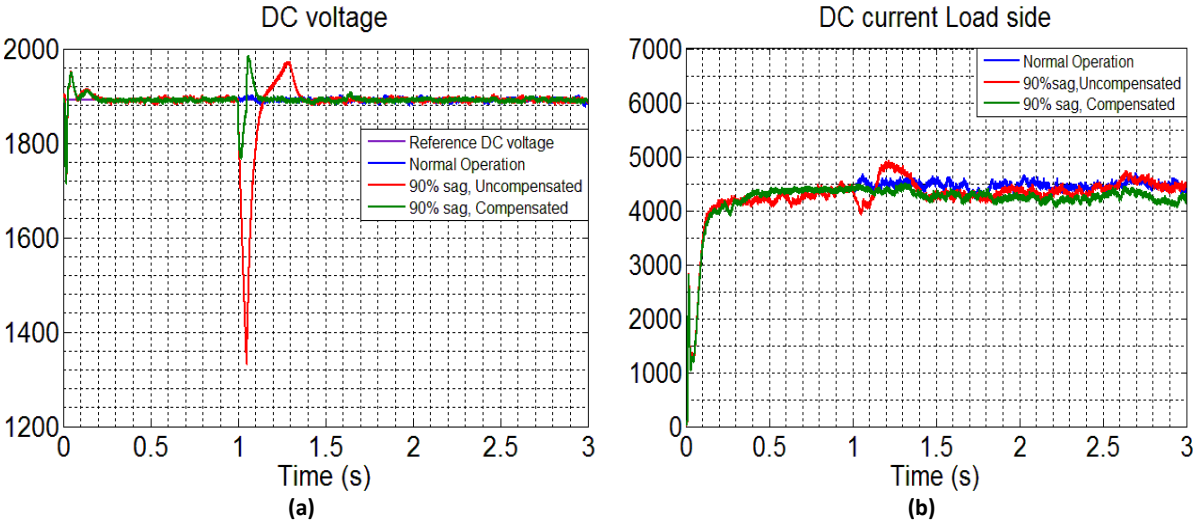

Figure 7.18: DC voltage (a) and current (b) for a 90% sag during 50 ms

Next Figure 7.19 (a) and (b) show the effect of the sag on the load side RMS voltage and current respectively. As expected the voltage for the uncompensated system drops deeper than for the compensated system. The effect this has on the speed is shown in Figure 7.20 (a) and (b) for an uncompensated and compensated SIPLINK system respectively. It can be seen that though the speed drop for the uncompensated system is not significant, about 2 percent, it is still greater than the speed drop for the compensated system. Whether this is acceptable depends on the specifications of the industrial grid.

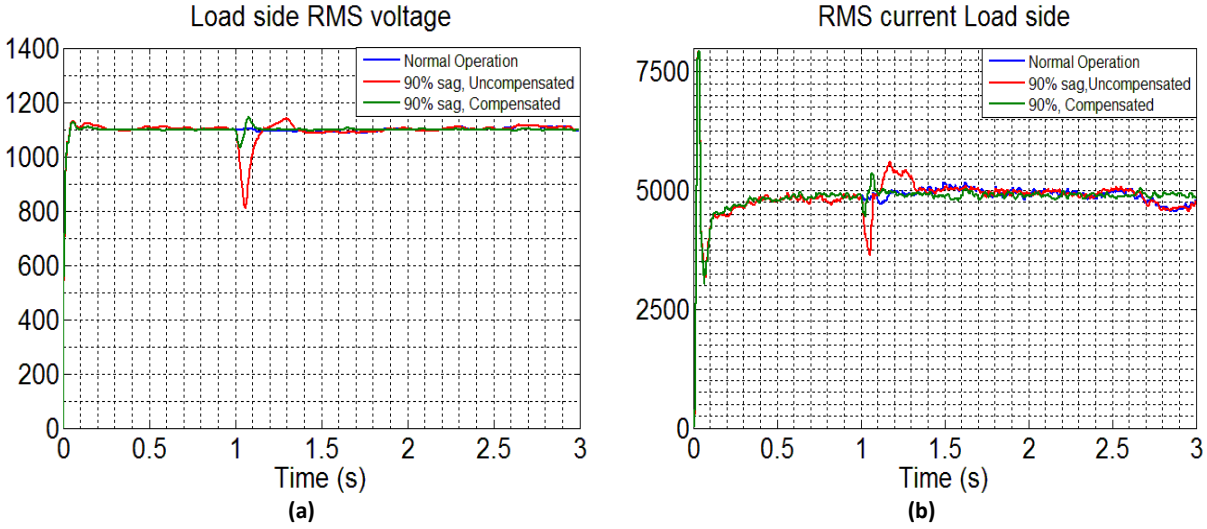

Figure 7.19: Load side RMS voltage (a) and current (b) for 90% sag during 50 ms

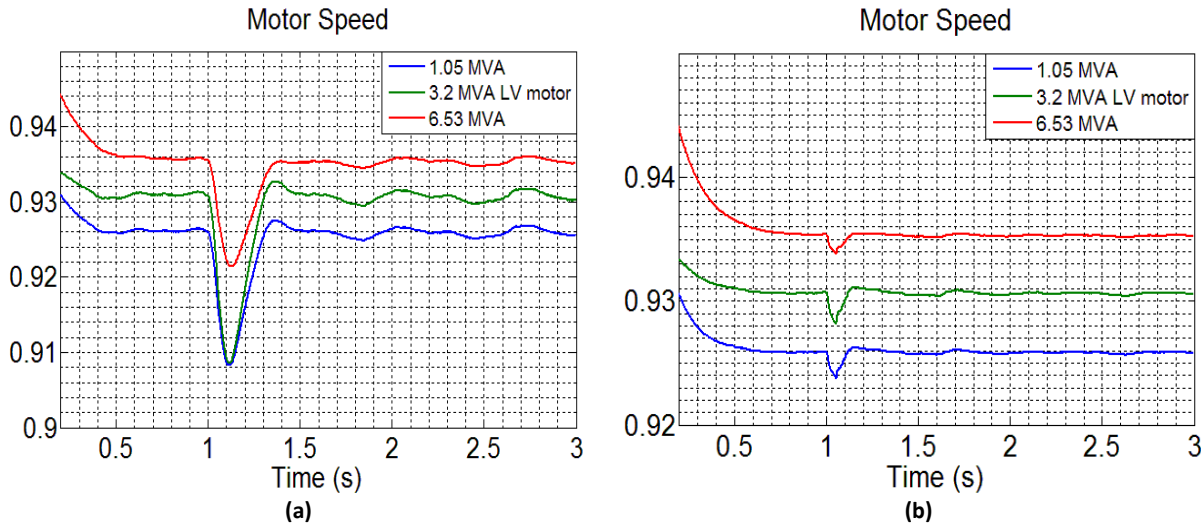

Figure 7.20: Motor speeds for uncompensated (a) and compensated (b) system for a 90% sag during 50 ms

Following are the waveforms from the auxiliary supply. Supercapacitors are especially suited to supply a burst of power for a short period of time. The short current pulse and power are shown in Figure 7.21 (a) and (b) respectively. After the sag has been cleared a constant current is drawn from the DC link. This current is used to charge the supercapacitor banks back up. This is not exactly according to the control scheme of Figure 5.19 because the supercapacitor terminal voltage has not dropped below 950 V, thus the supercapacitor banks do not need to be charged back up, but is given here to show a complete charge and discharge cycle of the supercapacitor banks. This could not be shown in the previous case due to simulation problems.

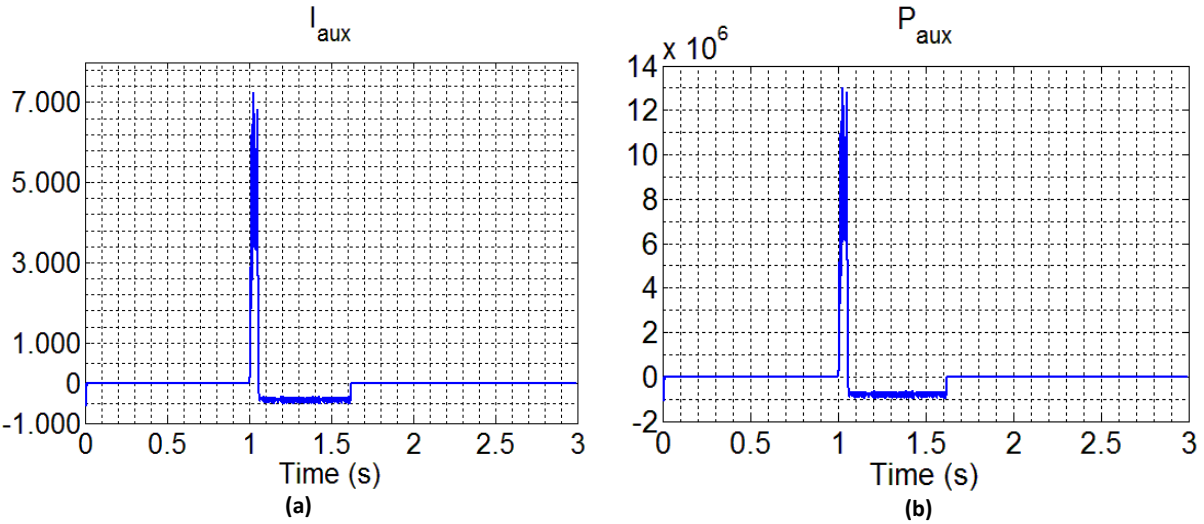

Figure 7.21 : Auxiliary current (a) and power (b) from supercapacitor enhanced boost converters for a 90% sag during 50 ms

Lastly Figure 7.22 (a) and (b) show the inductor current waveform for one of the six boost converter modules and the supercapacitor internal voltage respectively. The supercapacitors are recharged in about 0.45 seconds. Afterwards remaining standby for the next discharge cycle.

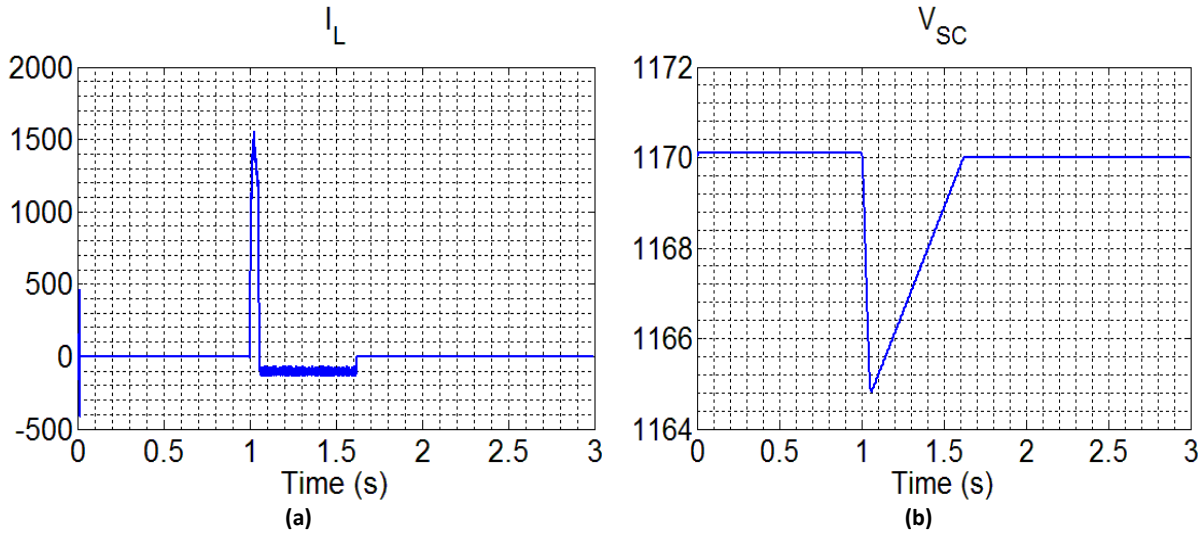

Figure 7.22: Inductor current of one boost converter module (a) and supercapacitor internal voltage (b) for a 90% sag during 50 ms

The above waveforms have shown that the supercapacitor enhanced SIPLINK converters are very useful when mitigating the effects of a voltage sag on the speed of the induction motors. The amount of supercapacitor banks as calculated in chapter 6.2.1 proved to be enough for the mitigation of a 90 percent voltage sag lasting 1 second. The control scheme of Figure 5.19 is followed charging and discharging the supercapacitor modules at the appropriate times. For a 50 ms sag the supercapacitor modules again seem fast enough but their necessity is questioned due to the small speed variation that occurs during such a short sag duration.

8. Economical and Implementation aspects of SIPLINK with Boost Converter Compensation

A standard SIPLINK comes equipped with water-cooled IGBT converters and either air- or water-cooled reactances with iron cores. The AC filters consist of air-cooled capacitors and water-cooled resistors. The DC capacitors are air-cooled and are self healing. The controllers are made by an external company called Integral Drive Systems-IDS. Signals are transmitted via fiber optics.

A 5 MW system fits in a 10 by 10 by 2,5 meter space. Excess space is needed to handle the waste heat. Although every SIPLINK system is custom made for each client, costs are about 3 million Euros for a 20 MW system.

The BMOD0018-P390 B01 supercapacitor module weights 165 kg and the dimensions are 1200x629x286 mm (LxWxH). Considerable space is thus needed to accommodate the 36 converters necessary for the compensation of the EdeA plant. Also as from august of 2007 the prices for these modules were 9 850 Euros when ordering between 1 and 15 modules, 7 390 Euros for 16 to 99 modules and 7 095 Euros for 100 to 500 modules. The 36 supercapacitor modules thus cost about 250 thousand Euros.

When assessing the costs of a voltage sag in an industrial plant several factors must be considered.

1. How sensitive is the process to various types of voltage sags?
2. What is the cost of a production outage due to the sag?
3. How effective are the solutions to mitigate the voltage sag?
4. What is the cost-benefit ratio of the particular solution?

When we speak of cost in this economic evaluation several elements can be used to quantify this.

1. Cost of Lost Production i.e. products that are not manufactured due to the disturbance and can therefore not be sold.
2. Cost of Damaged Products i.e. repair costs that are needed for damages sustained to a partially completed product.
3. Cost of Maintenance i.e. the cost of reacting to a voltage sag. This can be anything from cost of restoring production, cleanup and repair to environmental costs brought about by for example disposal of the damaged product.
4. Hidden Costs. This is the most difficult cost to assess as for in some cases the damage can only be detected once the product has fallen to consumer hands. This could lead to large product recall which is costly.

Since the cause for voltage sags are mostly random events, an effective way to assess the risk would be to conduct a statistical study of the total system and determine the expectations of events that can cause a voltage sag and that can be mitigated by a common solution. This is in no way an easy feat but historical data provide a good start for such a study.

9. Summary and Recommendation

9.1 Summary

Voltage sags yearly cause manufacturing companies thousands of dollars due to equipment shutting down or malfunctioning. This thesis has presented two methods of mitigating voltage sags in an industrial system. Both methods were based on the MVDC system SIPLINK developed by Siemens. This MVDC system makes use of IGBT switches for their converters. Vector control is used to transform the AC grid voltages and currents to DC values and back to AC to supply the industrial motor load. The first voltage mitigating method was based on overrating of the system meaning increasing the current rating of the system as compared to the steady state load which allows the converters to draw extra current from the grid during a voltage sag to keep the power constant. The second method was injecting extra current into the DC link from an auxiliary supply. This auxiliary supply consisted of supercapacitor banks interfaced by a bidirectional boost converter. To test the solutions an industrial grid consisting of 3 induction motors was modeled. Two motors are connected to a 10.5 kV busbar and one motor is connected to a 400 kV busbar. The motors on the medium voltage busbar are a 1.05 MVA motor that supplies a mechanical torque quadratic to its speed and a 6.53 MVA motor with constant mechanical torque. The motor on the low voltage busbar is 3.2 MVA and also has constant mechanical torque. The total rated power of the system is thus 10.78 MVA. The converters are rated 1.5 MVA each with terminal voltage of 1100 V and current of 750 to 950 A. A maximum current of 1800 A can be allowed for a maximum of 2 ms. The working window of the DC voltage is 1800 ~2100V and is set to operate at 1892 V. 8 converters are needed in parallel to supply the given load. The validity of the proposed models was investigated using Matlab and Simulink with the SimPowerSystems package.

9.1.1 Mitigation by converter overrating

Equation (2.4) allows one to derive the correct overrating factor to mitigate for a specified voltage sag. The results show that an 80% overrated system can mitigate a 45% voltage sag indefinitely. Without this overrating, the motors of the industrial plant would slow down and stop, except for the 1.05 MVA motor which would operate at a reduced speed. When the sag has cleared all motors want to accelerate back to their nominal speed drawing large currents. The system is usually designed to be able to support the load during steady state and during normal motor startup, in this case one at a time. Because the system is designed according to these criteria, it is not able to carry all the current demanded by all three motors speeding up simultaneously. The overcurrents thus lead to a shutdown of the entire system by overcurrent protection devices. To find the proper converter rating that is also able to mitigate for voltage sags apart from the three criteria necessary for normal operation mentioned in chapter 2, an in-depth stochastic study of the voltage at the plant area needs to be conducted similar to the study done by UNIPEDE DISDIP and presented in Table 1.1. From this study the occurrence of the most common sag magnitude and duration can be documented and the system can be designed to mitigate for these sags.

9.1.2 Mitigation by supercapacitor based auxiliary supply

The results have shown that a supercapacitor based auxiliary supply that supports the DC link of the MVDC system during a voltage sag is an effective way of mitigating voltage sags. These results were obtained for a 90% sag during 1 second and a 90% sag during 50 ms. For these tests a 10% overrated SIPLINK system was used as a starting point. The size of the supercapacitor banks depend on the depth of the sag and the duration. This thesis presented two cases to test the ability of the supercapacitors supporting the DC link. During all cases the support had to follow the control as given in the flowchart in Figure 5.19. This flowchart dictates when the support has to start and stop and when the supercapacitors need to be recharged after the sag has cleared. The auxiliary supply is to start supporting the DC link when the DC voltage is below 1850 V and as long as the sag has not cleared and the supercapacitor voltage has not dropped below 900 V. The working window of the supercapacitor voltage is between 1020 V and 840 V. When the sag has cleared and the DC voltage is above 1850 V, the supercapacitors are to be recharged with the 10 percent of the rated current (500 A) that the overrated converters can draw from the grid.

The supercapacitors are interfaced by a bidirectional boost converter that dictates the rate at which current is being transferred into and out of the system and with which magnitude. The converters also boost the voltage at the output to 1880 V. During discharge of the supercapacitors, current mode control was used to control the converter currents. During the charge mode a constant current is drawn from the DC link. This constant current stems from the extra 10% drawn by the overrated system. Care must be taken when designing the bidirectional boost converter components so as to not exceed the supercapacitor bank's maximum current and to supply the needed power during the specified time. During the most severe sag of 90 percent sag during 1 second, 9.5 MW of power should be supplied by the auxiliary supply. For this reason and also for reliability reasons the auxiliary supply was designed using a modular approach i.e. 6 bidirectional boost converters, each supplying 1.59 MW of power instead of 1 converter supplying 9.5 MW of power. This approach benefits the redundancy of the total system. All bidirectional boost converter modules operate on a 3kHz switching frequency in both the charge and discharge mode. A severe voltage sag of 90% during 1 second was taken as worst case scenario in this thesis research. In order to determine the right amount of compensation needed also an in-depth stochastic study of the voltages at the plant needs to be conducted.

9.2 Recommendation

For the design and simulation of the auxiliary supply, supercapacitor bank BMOD0018-P390 B01, manufactured by Maxwell was used. This supercapacitor module has a terminal voltage of 390 V. Unfortunately this module was discontinued during the writing of this thesis. Maxwell does provide a module with a terminal voltage of 125 V. This means that more modules need to be connected in series in order to make an acceptable input voltage for the bidirectional boost converter. As mentioned before, the gain of the boost converter should, due to the use of practical elements, not be larger than 2. To supply a DC voltage of 1892, thus the input voltage cannot be lower than 946 V. According to Maxwell data sheets, not more than 3 modules should be connected in series. Therefore 125 V modules cannot be used. A solution for this is to use isolated bidirectional boost converters. See Figure 9.1

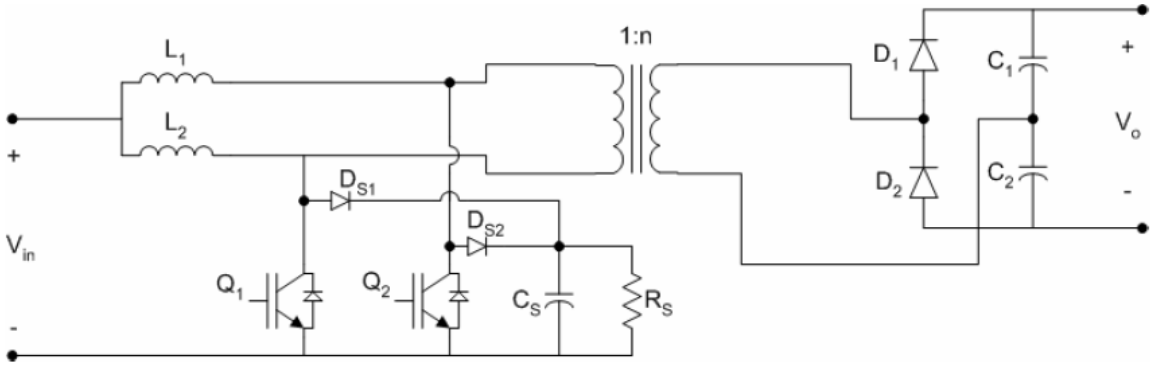

Figure 9.1: Isolated boost converter topology [11]

From Figure 9.1 it can be seen that the input and output sides are isolated by a transformer. This transformer isolates the grounds of the input and output and also provides most of the voltage gain of the converter. The converter consists of two boost converters connected in parallel. Where switches *Q1* and *Q2* operate alternating in order, inverting the input DC voltage to get a square wave voltage at the input terminals of the transformer. The transformer steps up this voltage which is then rectified by the half wave rectifier at the secondary part of the circuit. Though some gain is provided by the inductors *L1* and *L2*, most of the gain is provided by the transformer. The peak value of the input current is also reduced because these two inductors allow the converter to work in continuous conduction [11]. And though this topology has a higher component count, it makes it possible to use this topology for high power applications. Or in this case to provide more voltage gain from the low voltage supercapacitor modules.

For the bidirectional boost converter also a study should be done to select the proper converter switching frequency that will deliver the highest efficiency. For this thesis the author has chosen 3 kHz in order to achieve a small inductor size. Other factors such as the losses in the other elements of the converter should also be considered when choosing the proper converter frequency as proposed by [25]. Also a different switching topology can be used i.e. soft switching. Though hard switching has acceptable efficiency and power density, the Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) are not acceptable [25]. It is thus worthwhile to consider implementing the converters using resonant technology to not only reduce EMI but also switching losses. This can be realised by using Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). With these switching techniques switching losses which are mostly caused by overlapping voltages and currents in a switch can be reduced by creating a delay between them and smoothing out the voltages and currents in the switches.

Lastly the author recommends that instead of using the SIPLINK system to supply the load of an entire industrial plant or in this case an entire substation, to implement the system to protect only the most sensitive motors and processes of the industrial grid. In this way smaller, less expensive SIPLINK systems as well as auxiliary supply can be designed to guarantee the protection of the most critical loads.

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Appendix A. Motor and Transformer parameters

Components for the industrial system

Induction motor 1:

Rated power: 1.05 MVA
Rated RMS phase voltage: 6.062 kV
Rated RMS phase current: 57.735 A
Based angular frequency: 157.0796 rad/s

Induction motor 2:

Rated power: 3.2 MVA
Rated RMS phase voltage: 230.940 V
Rated RMS phase current: 4.162 A
Based angular frequency: 157.0796 rad/s

Induction motor 3:

Rated power: 6.53 MVA
Rated RMS phase voltage: 6.062 kV
Rated RMS phase current: 359.057 kA
Based angular frequency: 157.0796 rad/s

3 phase 2 winding transformer MVA: 20 MVA
Based operation frequency: 50Hz
Leakage inductance: 0.04 p.u.
Wind 1 line-to-line voltage (RMS): 11 kV
Wind 2 line-to-line voltage (RMS): 1100 V

3 phase 2 winding transformer MVA: 20 MVA
Based operation frequency: 50Hz
Leakage inductance: 0.04 p.u.
Wind 1 line-to-line voltage (RMS): 1100 V
Wind 2 line-to-line voltage (RMS): 10.5 kV

3 phase 2 winding transformer MVA: 12.65 MVA
Based operation frequency: 50Hz
Leakage inductance: 0.03 p.u.
Wind 1 line-to-line voltage (RMS): 10.5 kV
Wind 2 line-to-line voltage (RMS): 400 V