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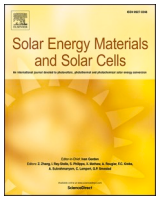

Understanding and mitigating resistive losses in fired passivating contacts: role of the interfaces and optimization of the thermal budget

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A B S T R A C T

This work presents a study of p-type passivating contacts based on SiC_x formed via a rapid thermal processing (RTP) step, using conditions compatible with the firing used to sinter screen-printed metallization pastes in industry. The contributions of the two interfaces (wafer/contact and contact/metal) to the contact resistivity are first decorrelated, identifying tunnelling at the wafer interface as the main contribution. We then investigate the influence of the active dopant concentration on the contact resistivity and the SiC_x sheet resistance and propose strategies to reduce both resistances by increasing the thermal budget applied during RTP. Lastly, we discuss potentials and limitations of implementing the investigated stacks as rear side contacts of p-type devices with localized metallization. We demonstrate that increasing the thermal budget during RTP can effectively mitigate resistive losses and enhance contact performance and we show that an oxide layer that can withstand high thermal budgets is the key factor for obtaining simultaneously high passivation quality and good electrical properties. We investigate three different oxide types grown by HNO_3 immersion, UV-O_3 exposure and N_2O plasma oxidation. The latter is demonstrated to be a promising candidate for an application in devices fabricated with high RTP thermal budget.

1. Introduction

Tunnel oxide passivating contacts (PCs) based on poly-Si layers have enabled solar cell conversion efficiencies above 26 % [1,2]. Formation of PCs normally starts with the growth of a thin silicon oxide (SiO_x) layer (~1–2 nm) at the c-Si wafer interface, followed by the deposition of a polycrystalline Si or amorphous Si layer. In the latter case, next, an annealing process is performed to crystallize the amorphous deposited layer, thereby providing stability to the poly-Si contact during the subsequent high-temperature processing steps. This annealing step is typically carried out at temperatures between 800°C and 900 °C [3,4] or sometimes up to 1050 °C [5,6] and for dwell times ranging from minutes to hours. Besides crystallization of the Si, this step also promotes the activation of dopants within the poly-Si layer. Moreover, it allows the dopants to diffuse through the SiO_x and into the wafer, thus creating a shallow highly doped region in the c-Si [7]. Lastly, the thin SiO_x also undergoes chemical and structural changes during this high temperature step [8–10].

Due to their compatibility with the high temperature processes that are routinely used by the photovoltaics industry, poly-Si contacts are now experiencing a growing popularity among industrial manufacturers, with industrial cell efficiencies that have been rapidly improving in recent years [11–13].

Using Earth-abundant, low-cost materials and fabrication conditions that are compatible with industrial processing is key to enable a smooth transition of poly-Si contact technology from research to industry. A possible simplification of this transition may be represented by the suppression of the long annealing at high temperature usually required for contact formation. As an alternative to long-annealed poly-Si contacts, p-type fired passivating contacts (FPCs) have been demonstrated, which make use of a shorter annealing to activate the dopants in the poly-Si layer [14]. This process, which consists of a rapid heating to a peak temperature around 800 °C and dwell times of only a few seconds, is compatible with the firing step employed in industry for the sintering of the metal paste. Thus, these FPC structures could provide an alternative to the localised rear-side contacts used in current p-type passivated emitter and rear cells (PERC) since they can be processed without the need for laser opening of the rear dielectric. In particular, previous work on FPCs has demonstrated their capability to achieve low saturation current density (J_0) values below 10 fA/cm^2 [15]. Replacing the

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partial rear contact scheme of PERC with this optimized FPC structure has the potential to improve the cell efficiency above 25 % [15].

In traditional poly-Si contacts, the presence of the shallow doped region promotes tunnelling through the SiO_x, thanks to a favourable band-edge alignment between the wafer and the doped poly-Si layer [16]. Additionally, the shallow doped region enhances surface passivation by reducing the presence of recombination centres for minority carriers. In contrast, due to the shorter thermal treatment applied to FPCs, dopant diffusion across the SiO_x is suppressed and surface passivation and charge carrier transport rely on the accumulation region formed at the wafer interface, as well as on a low defect density at the c-Si/SiO_x interface [14,17]. These, in turn, are strongly dependent on processing conditions that must be carefully tuned to ensure efficient charge transport and high passivation quality in these contacts.

Whereas previously reported FPC results often display these layers at the solar cell's rear side with a low-temperature, full-area metallization [15], integrating FPCs into industrial processing requires compatibility with high-temperature screen-printing and firing, where the use of localized metal fingers instead of full area contacts is the commonly chosen approach [18]. This introduces further challenges and requirements regarding contact resistivity and lateral conductivity compared to the case of a full-area metal contact; these parameters must be carefully optimized in order to minimize resistive losses that could negatively affect the fill factor (FF).

For long-annealed poly-Si contacts, the in-diffused region can promote low contact resistivity at the c-Si/SiO_x/poly-Si interface as well as provide a region with high lateral conductivity between the metal fingers. In the case of FPCs, satisfying these requirements solely through careful tuning of the poly-Si layer properties becomes essential; this, in turn, requires a thorough understanding and control of the interplay between the various process parameters and properties of the contacts.

In this contribution, we investigate FPCs based on p-type SiC_x layers, targeting their application as rear-side contacts in c-Si. We address the associated challenges and potential applications of the stacks in devices with localized metallization.

In particular, we focus on characterizing their electrical properties and optimizing them to minimize resistive losses. We study the dependence of the contact resistivity and lateral conductivity on processing temperature, separating the role of the wafer/PC and PC/metal interfaces. With the goal of reducing silver consumption (as used in silver paste screen printing), we compare the performance of various metals, namely an indium tin oxide/silver (ITO/Ag) stack, which was used to contact FPCs in previous publications [15,19] as well as aluminium and molybdenum contacts. These alternative metals possess suitable work functions that make them promising candidates for establishing low contact resistivity to p-type layers [20]. Additionally, we examine the impact of the thermal budget applied during firing on the passivation quality. We identify a range of processing parameters where high passivation quality and good electrical conductivity can be obtained simultaneously. This is accomplished by introducing an interfacial oxide layer that can withstand a higher thermal budget.

2. Experimental

The different processing steps for sample fabrication are shown in Fig. 1. Symmetrical test structures were fabricated on 200-μm thick shiny-etched (SE) float-zone wafers with (100) orientation, either p-type or n-type doped with a resistivity of 2 Ω cm. After etching and cleaning, a thin (~1.3 nm) interfacial oxide was grown chemically on all samples by immersion in HNO_3 (69 %, 80 °C, 10 min). For some samples, this chemical oxide was removed by a 1 min HF dip, and two other kind of oxides were tested, grown by UV-O_3 exposure for 2 min or by plasma enhanced chemical vapour deposition (PECVD). The thickness of the oxide layers obtained with these two techniques was found to be comparable with the thickness of the chemical oxide (~1.3 nm). For the PECVD oxide samples, the wafers were subjected to a plasma treatment using H_2 and N_2O as precursor gases, which resulted in the growth of an oxide layer at the wafer surface (referred to as "plasma oxide" in the following sections). After oxidation of the c-Si, a hydrogenated amorphous a-SiC_x(p):H layer (containing about 2.5 at% of C) was deposited by PECVD at 200 °C for all samples (KAI-M, Unaxis). The thickness of the a-SiC_x(p):H was ~40 nm on the p-type wafers and ~120 nm on the n-type substrates (denoted as p^+/p and p^+/n structures, respectively). The higher thickness of the SiC_x for p^+/n structures is chosen to ensure sufficient lateral conductivity for electrical characterization. Subsequently, rapid thermal processing (RTP) was used to crystallize the layers and activate their dopants (Jipelec 200). Temperatures between 770 °C and 920 °C and dwell times between 3 and 30 s were explored. More details on the experimental procedure can be found in Ref. [14].

Lastly, the samples were hydrogenated by growing a layer of hydrogen-rich silicon nitride (SiN_x:H) by PECVD (SINA, Meyer Burger) and then firing at a set temperature of 840 °C for a few seconds in a ceramic roller furnace (CAMINI, Meyer Burger). After hydrogenation, the SiN_x:H layers were removed by dipping the samples in a 5 % HF solution.

Minority carrier lifetime and implied open-circuit voltage (*iVoc*) were measured on unmetallized samples prior to SiN_x removal with a Sinton WCT-100 instrument.

For samples dedicated to metallization, after dipping in 5 % HF solution to remove the parasitic oxide at the SiC_x surface and sputtering Al, Mo, or an ITO/Ag bilayer (Leybold Univex-450B for Al and Mo and MRC P603, NIHON MRC Co. for ITO/Ag) through a shadow mask, the contact resistivity was measured using the transfer length method (TLM) on as-sputtered samples and after a 30 min curing at 200 °C carried out in air

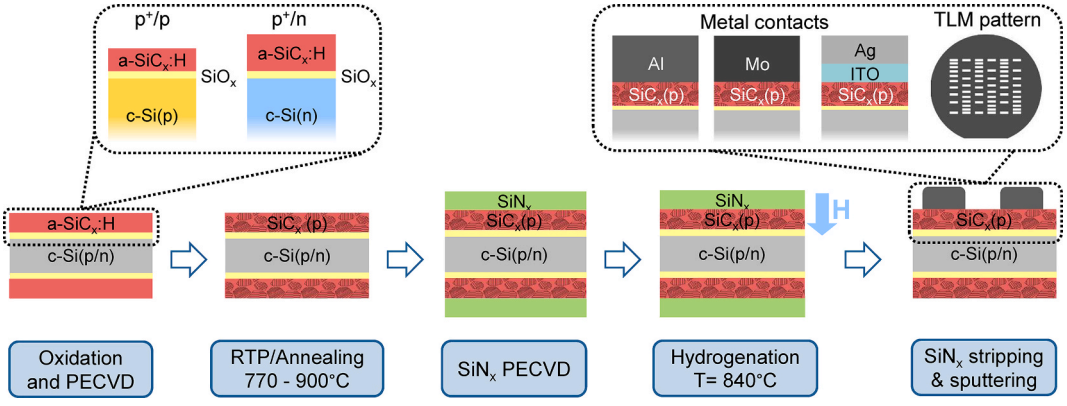

Fig. 1. Schematics of the process flow for fabrication of SiC_x passivating contacts. The two different sample configurations (p^+/p and p^+/n) are shown as well as the tested metal contacts. A top view schematic of the metallization pattern used for TLM measurements is also included.

atmosphere. The evaluation of the contact resistivity after curing was included in the study to test the compatibility with the process flow of our demonstrator solar cells, which includes a step at the end for curing the defects that could result from the sputtering of the metal contacts.

The samples were cleaved along the TLM pattern to avoid lateral current spreading. The true distances between the pads were measured by optical microscopy to account for deposition of material under the shadow masks. For the p^+/p structures, the current spreading into the wafer was corrected according to the 2D analytical method described in Ref. [21]. The SiC_x layer between the metal pads was not removed, as the lateral conductivity of this layer is much lower than the one of the wafer, as discussed below.

The contact resistivity characteristics expected for the tunnel junction were modelled according to Refs. [22,23]. For the metal/SiC_x contact resistivity, the contribution expected for thermionic field emission (TFE) was modelled according to Ref. [24]. The active carrier density was determined by combining ellipsometry (UVISEL, Horiba Jobin Yvon), UV–Vis spectrometry (Lambda 950 with integrating sphere, PerkinElmer), and IR transmission (Vertex 90 FTIR, Bruker) measurements following the method described in Ref. [19]. The sheet resistance of the layers was obtained from 4 point probe measurements on p^+/n structures.

X-ray photoelectron spectroscopy (XPS) measurements were performed with a ThermoFisher K-Alpha spectrometer equipped with a focused monochromatic Al Kα source (1486.6 eV) anode operating at 36 W (12 kV, 3 mA), a flood gun operating at 1 V, 100 μA and the pass energy of the analyser set to 150 eV. The base pressure in the analysis chamber was approximately $2{\cdot}10^{-9}$ mbar. For each sample, an area scan of 3000 × 3000 μm^2 was performed using a grid of 90 400 × 400 μm^2 points that are partially overlapping. The samples were transferred from the glove box to the spectrometer inside a dedicated ThermoFisher vacuum transfer module to avoid air-exposure. In the analysis, the binding energy was corrected for the 0.3 eV charge shift using the primary C1s hydrocarbon peak at binding energy BE = 284.8 eV as a reference. The data were fitted using 70 % Gaussian and 30 % Lorentzian line shapes (weighted least-squares fitting method) and nonlinear Shirley-type background using the ThermoFisher Avantage software.

3. Results and discussion

3.1. Contact resistivity for p^+/n and p^+/p structures

Fig. 2 shows contact resistivity data for three different metals measured on samples featuring n-type and p-type wafers (p^+/n and p^+/p, respectively), for RTP at 800 °C and a dwell time of 8 s (corresponding to the optimal conditions found in our previous publications for HNO_3 and UV-O_3 oxide [15,19]). In both cases, HNO_3 immersion was used to grow the thin interfacial oxide. The two types of sample structures are used for the following reasons: for the p^+/p samples, current flow between the TLM pads occurs mostly in the wafer, whose sheet resistance R_{sheet} is two orders of magnitude below the one of the SiC_x (~100 Ω/square for c-Si wafer compared to >10 kΩ/square for 40 nm SiC_x layer). The measured ρ_C is therefore a sum of the contributions coming from the wafer/SiO_x/SiC_x interface (ρ_C^{SiOx}) and the SiC_x/metal interface (ρ_C^{Met}). To assess the impact of lateral transport within the SiC_x layer on these structures, we conducted TLM measurements both before and after removing the material between the metal pads using reactive ion etching (RIE). Remarkably, our findings indicate comparable results for 40 nm layers, confirming the negligible contribution of current flow in the SiC_x. Detailed results can be found in the Supplementary Information.

In the case of p^+/n structures, transport occurs mostly in the SiC_x layer due to the blocking p/n junction at the wafer interface and thus only ρ_C^{Met} is measured. For these structures, the SiC_x layer has been deposited with a thickness of ~120 nm to ensure sufficient lateral conductivity to perform the contact resistivity measurements with enough accuracy. We verified that the different thicknesses of the SiC_x layers for the p^+/p and p^+/n structures do not create any additional difference in the measured contact resistivity by comparing the active doping concentration in the layer in the two cases, and we found them to be comparable within the measurement error. Furthermore, we compared the contact resistivities on p^+/p structures for 40 nm and 120 nm SiC_x layers and found no significant difference in the results, both layer thicknesses yielding values in the range 15–25 mΩ cm^2. The data relative to these additional experiments are reported in the Supplementary Information. The current flow in the two different sample structures is also illustrated in Fig. 2.

The data reveal that, for all the samples, the contact resistivity values are an order of magnitude lower for the case of p^+/n structures than for p^+/p. This indicates that the largest contribution to the resistivity originates from ρ_C^{SiOx}. The three tested metals all perform similarly, which points towards comparable values for their effective Schottky barriers. Nevertheless, the three metals show a different behaviour with respect to the changes in the contact resistivity after a thermal treatment. Aluminium contacts exhibit decreased contact resistivity in both p^+/p and p^+/n samples. This could be attributed to the reduction of a residual native oxide on the SiC_x surface, which improves the Al–Si contact [25,26]. Conversely, the samples metallized with ITO/Ag contacts show an increase in contact resistivity after curing; this effect has previously been explained with the effusion of O from the ITO, which

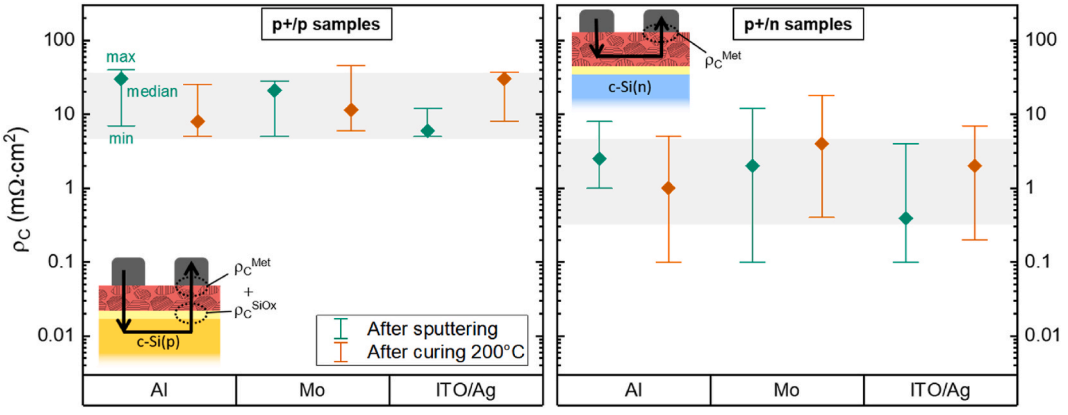

Fig. 2. Contact resistivity on c-Si(p)/SiO_x/SiC_x(p)/metal or c-Si(n)/SiO_x/SiC_x(p)/metal structures either directly after metal sputtering or after curing at 200 °C for 30 min. The chemical oxide was used for this experiment. The schematics illustrate the sample structures as well as the current path between TLM pads. The grey area corresponds to the range where the median values lie to highlight the difference between the p^+/p and p^+/n samples. For each conditions, 5 different samples were measured.

facilitates the growth of an oxide layer at the SiC_x/ITO interface [27]. The trend of Mo contacts is less clear, and contact resistivity values change little after curing. This behaviour appears to be consistent with previous observations reported in the literature, in which no reduction of the surface SiO_x by Mo was observed and the electrical properties of Si/Mo direct contacts were found to be unchanged after annealing up to 600 °C [28].

3.2. Influence of the active carrier concentration on the electrical properties of the contacts

The dependence of the active doping concentration on the RTP temperature and dwell time is depicted in the left panel of Fig. 3 and compared to literature data for the solubility of boron in crystalline silicon [29]. The data in Fig. 3 show increasing active carrier density towards higher firing temperatures and dwell times. For both dwell times of 3 and 30 s, the obtained concentrations follow closely the trends observed in the data from previous work [29]. We expect the concentration of active dopants to have an impact on the contact resistivity since the doping concentration controls the induced accumulation layer in the c-Si as well as the width of the space charge region at the metal interface.

3.2.1. Contact resistivity

The right panel of Fig. 3 presents the contact resistivity as a function of the carrier density for p^+/n and p^+/p structures, together with the predicted behaviour for thermionic field emission (TFE) and tunnelling (TO) dominated transport at the metal/SiC_x and c-Si/SiO_x/SiC_x interfaces, respectively [24]. For this experiment, contact resistivity was measured after sputtering of the metal contacts, and the curing step was not performed. The contact resistivity for p^+/n samples decreases towards higher carrier density (corresponding to a higher thermal budget applied during RTP), which agrees well with the predicted behaviour and indicates that increasing the RTP temperature can significantly reduce ρ_C^{Met}. For p^+/p samples, the contact resistivity appears to reach saturation at higher carrier densities; this behaviour can be explained by tunnelling-dominated transport across the c-Si/SiO_x/SiC_x interface, which is less sensitive to doping than TFE. This shows that the reduction in ρ_C^{SiOx} expected from increasing the RTP temperature is limited compared to ρ_C^{Met}. The data reported so far were measured on samples with a chemical oxide at the c-Si/SiC_x interface. On another batch of p^+/p samples where the thin oxide was obtained by UV-O_3 exposure (not shown here) no major differences were observed in the experiment in terms of contact resistivity compared to HNO_3 samples presented in this section. This suggests that the two processes result in oxide layers with similar thicknesses and with similar tunnelling probabilities for hole transport.

The contact resistivity data obtained from TLM measurements conducted on Al, Mo, and ITO/Ag contacts do not exhibit any preference for a specific Schottky barrier height. This observation is unexpected, considering that differences in the work function of these contact materials should show up particularly in the case of p^+/n samples. A possible explanation for this discrepancy could be the presence of a not fully etched parasitic oxide layer on the surface of the SiC_x. This could increase the measured contact resistivity and thus minimize the effect of the work function of the different tested metals. This topic will be addressed in a following section.

3.2.2. SiC_x lateral conductivity

Increasing the RTP thermal budget of p^+/n structures also changes the sheet resistance of the SiC_x layers as a consequence of the increased activation of dopants. Fig. 4 illustrates the dependence of R_{sheet} on the thermal budget during RTP (left) and on the concentration of active dopants (right). In contrast to what was previously observed for ρ_C^{SiOx}, the sheet resistance can be further decreased as carrier density increases, without limitation in the probed range. This demonstrates that, while a higher thermal budget may not result in a significant reduction in contact resistivity, it can substantially decrease R_{sheet}, a parameter of interest when applying localized metallization to the layers. This will be covered in greater detail in the following.

3.3. XPS analysis of SiC_x (p) surface

The contact resistivity data presented in Figs. 2 and 3 show a large spread, which could be tentatively explained by a residual oxide of variable thickness on top of the SiC_x that was not fully etched by the 1 min dip in 5 % HF used for these experiments. As previously mentioned, this could also explain why no dependence on the metal work function was observed for the data in the right panel of Fig. 3, especially for the p^+/n structures. To investigate this point, XPS measurements were performed on several samples that were subjected to different HF times. On each sample, 90 measurements were performed leading to acquire information on the uniformity across the sample. The data and fitted peaks are depicted in the left panel of Fig. 5. Data relative to samples with three different HF times are shown as an example (the complete dataset can be found in Supplementary information). The Si 2p signal was fitted with at least two pairs of peaks: one pair at BE ≈ 99 eV representing the Si signal (blue) and one or two pairs at BE ≈ 101–103 eV

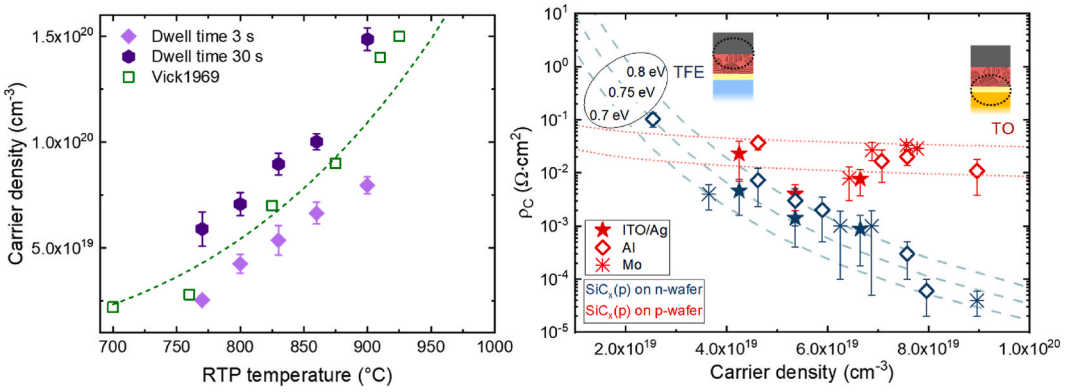

Fig. 3. Left: dependence of the active carrier concentration on the RTP temperature and dwell time. The error bars correspond to the uncertainty on the results of the fitting procedure. Literature data on the solubility of B in c-Si are shown with empty symbols, whereas the fit of the experimental data is shown in dashed lines. Right: Dependence of the contact resistivity on the active carrier concentration. Dotted lines show the modelled contribution for transport at the c-Si/SiO_x/SiC_x interface ("TO", red dotted line) for two different values of the band bending induced across the oxide. Dashed lines show the contribution at the SiC_x/metal interface ("TFE", light blue dashed line) for three values of the Schottky barrier. Contact resistivity data for p+/p (red) and p+/n structures (blue) are shown for the three chosen metals. Median values over three samples are shown, and the error bars represent the standard deviation. The chemical oxide was used for this experiment.

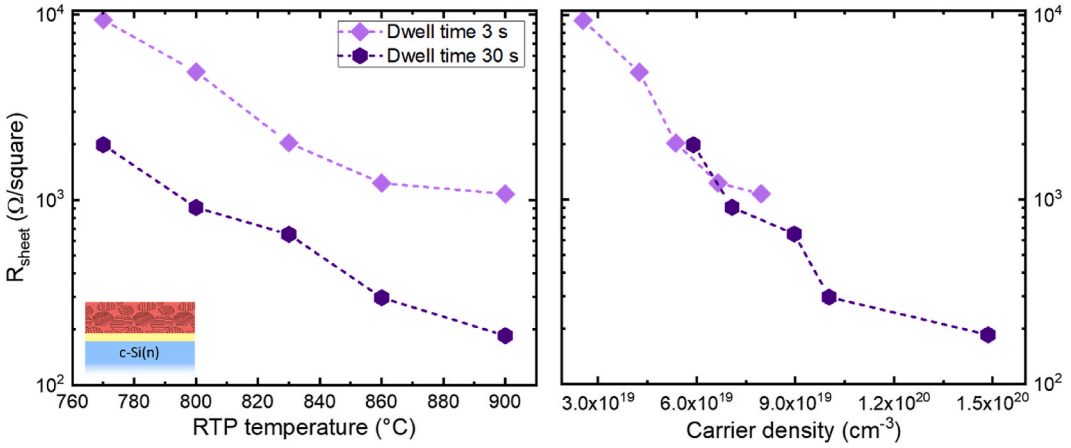

Fig. 4. Sheet resistance measured on p+/n structures for different RTP temperatures and dwell times (left). R_{sheet} as a function of the active carrier concentration (right).

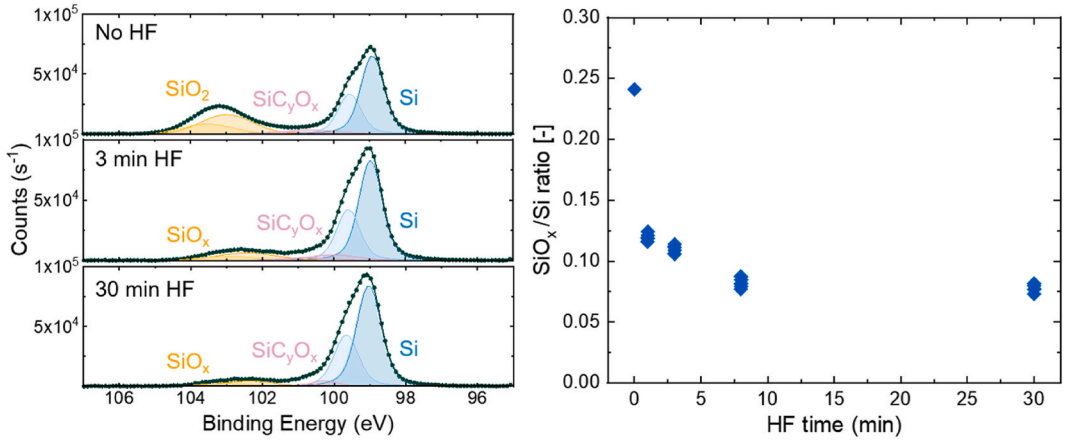

Fig. 5. Left: Detailed scan of the Si2p signal for three different HF times. The different colours highlight the pairs of peaks used for the fitting. Right: SiO_x/Si peak ratio from XPS scans, as a function of different HF times. On the samples, multiple measurements were performed leading to multiple values for each HF time.

representing the SiO_x peak (yellow). The intensity of the Si 2p peak was used to determine the ratio between the SiO_x to Si peak intensity to monitor the presence of SiO_x on the sample surface, and the results are shown in the right graph of Fig. 5. For each condition, 10 data points out of 90 are represented in the plot. The peak ratio shows a steep decrease from 0 to 1 min HF, and subsequently a slower decrease up to 8 min. For longer HF times, the peak ratio remains constant and never reaches zero.

The observation that the SiO_x/Si ratio never reaches zero could indicate that the parasitic SiO_x layer is never completely removed from the surface even after long HF dip duration. A possible explanation for this effect is that during the RTP, some boron from the SiC_x(p) layer may segregate into the surface oxide, leading to a B-rich SiO_x that is stable in HF for longer time compared to a pure native oxide. We speculate that the non-uniform etching of this oxide over the wafer surface could explain the large spreading observed in contact resistivity results. This hypothesis is also consistent with the observation that the largest spreading is found for p^+/n samples, where the contribution from the parasitic oxide layer would have a greater influence than in the case of p^+/p samples. These findings imply that improved surface control of the samples is required, and that additional techniques other than a simple HF dip may be needed to eliminate the parasitic oxide prior to metallization.

3.4. Application as rear side contact: impact on the series resistance

The contact resistivity data shown in Fig. 2 were obtained with a RTP temperature of 800 °C and dwell time of 8 s, which correspond to the optimum processing conditions used to produce SiC_x layers according to previous experiments. The obtained ρ_C values are mostly in the range of 10–40 mΩ cm^2, which is acceptable for full area metal contacts (leading to relative *FF* loss below 0.5 % [30]). However, the current industry standard for solar cells manufacturing involves localized metal contacts on both sides of the cells, which reduces paste usage and opens the possibility for bifacial cells. To minimize considerable series resistance losses, the contact resistivity requirements are more severe in this scenario than in the case of full area metallization. Nevertheless, the results presented earlier show that it is possible to slightly improve the contact resistivity by increasing the RTP thermal budget. Furthermore, this boosts considerably the lateral conductivity of the SiC_x layer (as seen in Fig. 4), allowing the current to laterally flow not only in the wafer, but also in the SiC_x layer. A more detailed investigation was therefore performed in order to understand the influence of these parameters on the series resistance in the case of localized metal contacts applied to the SiC_x layers. For this, the well-established description of the resistive losses occurring between two conductive layers coupled by a contact-resistivity was followed [31–33].

Fig. 6 depicts the effect of ρ_C^{SiOx} and R_{sheet}^{SiCx} on the series resistance in a p^+/p structure with localized metallization according to Ref. [32]. An example of the targeted cell structure, where the SiC_x contact is integrated at the rear side of a cell featuring the phosphorus emitter typical of PERC, is also shown on the left. In the right panel of Fig. 6, the dotted lines show separate contours for the series resistance, which correspond

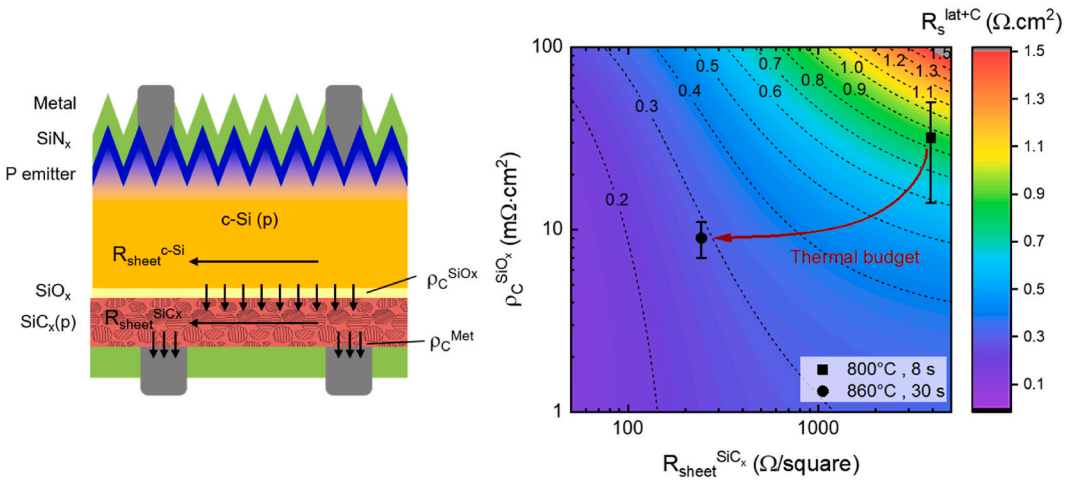

Fig. 6. Left: targeted cell structure where the SiC_x(p) is integrated on the rear side with localized metal contacts. Right: dependence of the series resistance contribution from the rear contact (R_s^{lat+C}) on the contact resistivity and sheet resistance of the SiC_x. Data corresponding to two different windows of RTP conditions are shown as an example. The model parameters are: ρ_C^{Met} = 1 mΩ cm^2, V_{mpp} = 630 mV, $N_{dop} = 7.2{\cdot}10^{15}$ cm^{-3}, finger pitch = 1.85 mm, finger width = 50 μm.

approximately to a change of 0.5 % in the *FF* [30]. The graph includes sheet resistance and contact resistivity data corresponding to "low" (800 °C for 8 s) and "high" (860 °C for 30 s) thermal budget. The graph shows two distinct parameter ranges where ρ_C^{SiOx} and R_{sheet}^{SiCx} influence R_s in different ways.

For the case of high R_{sheet}^{SiCx} (> 3 kΩ/square), current flow occurs primarily in the wafer, and ρ_C^{SiOx} must be as low as possible to maintain a small R_s. Thus, one would have to revert to a full area metal cover to provide sufficient lateral conductivity in the rear contact. Lower R_{sheet}^{SiCx} (300 Ω/square and below) allows current to flow laterally in both the SiC_x and in the wafer. In this case, R_s is less sensitive to changes in contact resistivity, which becomes less critical for the device performance and allows for local contacts. These results highlight the interest of working at high thermal budget, since in this range sufficient lateral conductivity can be provided by the SiC_x layer and requirements on the contact resistivity are relaxed.

3.5. Passivation quality

In addition to the electrical properties of the SiC_x layers, the applied thermal budget also influences the passivation. This topic has been extensively investigated by different groups, and similar trends for the evolution of the passivation as a function of the applied thermal budget have been observed [34–38]. Typically, two ranges are observed in which passivation initially improves with increasing thermal budget up to an optimum and subsequently decreases toward higher temperatures. The optimal thermal budget represents the compromise between two competing effects: on one hand, the increased dopant activation and shallow diffusion of dopants across the SiO_x obtained with higher temperature maximizes field effect passivation. On the other hand, too high thermal budget results in a damage to the thin interfacial SiO_x layer, causing a loss of chemical passivation. Furthermore, excessive dopant diffusion in the crystalline silicon has been also identified as a source of passivation loss at high temperatures, as it enhances Auger recombination.

For FPCs, very similar trends have been reported, with an initial improvement of the passivation as the thermal budget increases, followed by a drop above the optimum temperature [15,19,39]. Because the short dwell times of RTP do not allow for significant dopant diffusion across the oxide, these contacts primarily rely on dopant activation within the poly-Si layer to promote accumulations of holes or electrons in the c-Si, as well as on the integrity of the silicon oxide layer that provides chemical passivation.

The behavior of the passivation quality as a function of the applied thermal budget was investigated by using symmetrical p^+/p samples. Fig. 7 depicts the implied V_{oc} (iV_{oc}) values for various RTP temperatures and dwell times of 3 (left) and 30 (right) seconds. The two different oxides show very similar trends with respect to temperature and dwell time, with the UV-O_3 oxide outperforming the chemical one over most of the studied parameter range. The observed trends are consistent with other findings reported in literature for poly-Si based contacts. For the shorter dwell times, passivation improves initially with increasing temperature, reaches an optimum at 830 °C, and then declines towards higher temperatures. The initial improvement in passivation could be attributed to increased doping activation in the SiC_x, promoting hole accumulation at the wafer interface. For longer dwell times, the lowest temperatures of 770 °C and 800 °C show comparable performance, but at 830 °C the iV_{oc} already drops dramatically. The drop could be explained by the creation of interfacial defects across the oxide, which become detrimental for higher temperatures and longer dwell times [15], or even by the disruption of the oxide layer for the highest thermal budgets.

The iV_{oc} results shown in Fig. 7 demonstrate that HNO_3 or UV-O_3 oxides do not provide high enough surface passivation at high thermal budget. Therefore, a third oxide layer was developed with the goal of obtaining improved stability at high temperatures and longer dwell times, and thus accessing the high thermal budget range that was shown to be beneficial in terms of electrical conductivity. This oxide layer is based on N_2O plasma-assisted oxidation by PECVD, which has already shown improved resistance to high temperature processes compared to more commonly used oxide layers [40,41]. The data obtained with this oxide layer are depicted in Fig. 8 (left) in comparison with the HNO_3 and UV-O_3 results in the high temperature range (data reproduced from Fig. 7). The plasma oxide samples exhibit a completely different trend than the other layers included in this study. In particular, stable passivation quality up to 920 °C is shown, with the iV_{oc} remaining constant above 710 mV. The right panel of Fig. 8 displays the contact resistivity data obtained with the plasma oxide samples for an ITO/Ag metallization. The values lie in the same range as the results obtained with chemical and UV oxides, represented by the grey area. This makes the plasma oxide an excellent option to work in the high thermal budget range, enabling to maintain both high passivation quality and high electrical conductivity at the same time. We speculate that the improved stability at high thermal budget may originate from the higher density of this oxide layer compared to chemical and UV-O_3 ones. The superior performance of this oxide layer could also be related to a composition closer to that of stoichiometric SiO_2, which was shown to have a positive impact on thermal stability of oxide layers [9,42]. Moreover,

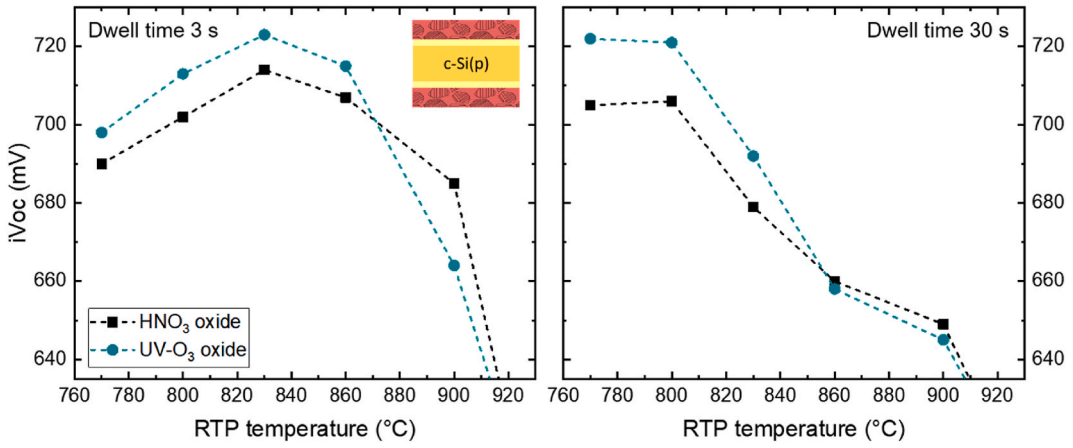

Fig. 7. Implied V_{oc} data measured on symmetrical samples featuring a chemical (black squares) and a UV-O_3 (blue circles) oxide, for a RTP with 3 s (left) and 30 s (right) dwell time.

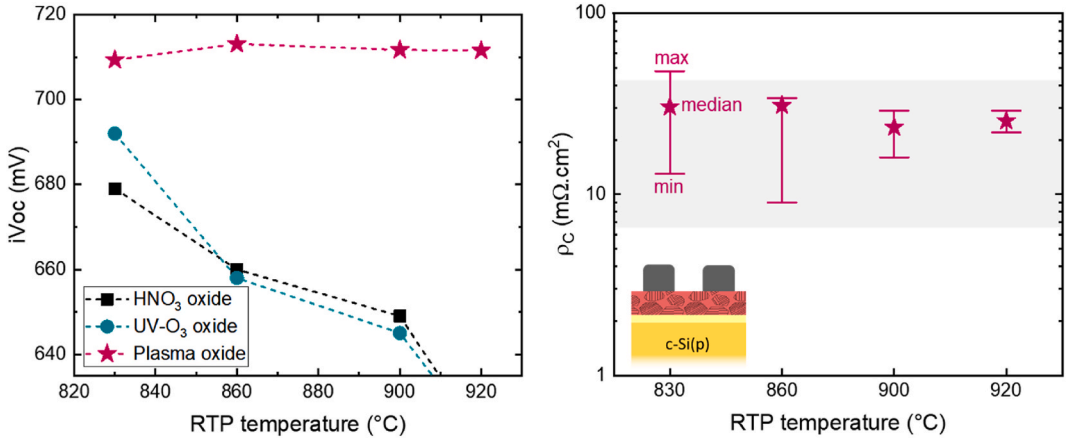

Fig. 8. Left: implied V_{oc} data measured on symmetrical samples for chemical (black), UV-O_3 (blue) and plasma (pink) oxides, for a RTP with dwell time of 30 s in the higher temperature range. Right: contact resistivity data measured for the plasma oxide samples for different RTP temperatures. The grey area represents the range of values that was obtained with chemical and UV-O_3 oxides, corresponding to the data reported in Figs. 2 and 3.

accumulation of N at the c-Si interface has been reported in previous studies, where strong Si–N bonds substitute the weaker ones normally present at the interface [43]. The presence of the stronger bonds may also explain the improved stability of the N_2O oxide at high thermal budget. The investigation of this topic is beyond the scope of this work and will be treated in a follow-up publication.

4. Conclusions

By separating the impact of ρ_C^{SiOx} and ρ_C^{Met} on charge transport performing TLM measurements on p^+/p and p^+/n structures, we have shown that the results did not strongly depend on the chosen metallization, which opens the interesting possibility of Ag-free contacts to the poly-Si layers. Increasing the RTP temperature can significantly reduce ρ_C^{Met}, whereas the contribution from the tunnel oxide can only be lowered to a lesser extent. Nonetheless, an increased thermal budget improves the lateral conductivity of the SiC_x layer, which is important when using localized metallization. We showed that using a high thermal budget for the RTP is critical for limiting the influence of the rear contact on the series resistance. We investigated an alternative oxidation process based on N_2O plasma treatment of the wafer surface, which demonstrated improved stability in the high thermal budget range compared to the other oxide layers studied in this work. The introduction of this oxide layer did not have significant effect on the contact resistivity of the stacks. Therefore, we identify the plasma oxide layer as a promising candidate to allow for successful integration of the studied layers into devices with localized metallization.

CRediT authorship contribution statement

S. Libraro: Writing – original draft, Visualization, Methodology, Investigation, Data curation. **A. Morisset:** Writing – review & editing, Supervision, Investigation, Funding acquisition, Data curation. **J. Hurni:** Writing – review & editing, Investigation, Data curation. **E. Genç:** Writing – review & editing, Investigation, Data curation. **L. Antognini:** Writing – review & editing, Investigation, Formal analysis, Data curation. **L.J. Bannenberg:** Writing – review & editing, Investigation, Data curation. **T. Famprikis:** Writing – review & editing, Investigation, Data curation. **C. Ballif:** Writing – review & editing, Project administration, Funding acquisition. **A. Hessler-Wyser:** Writing – review & editing, Supervision, Conceptualization. **F.-J. Haug:** Writing – review & editing, Supervision, Funding acquisition, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The supplementary information and data underlying this contribution are available on the Zenodo repository under the following https://doi.org/10.5281/zenodo.7982438.

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