A MHz Switching Active Clamp Fly-back Converter as a Power Factor Correction Stage for Lighting

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Challenge the future

A MHz Switching Active Clamp Flyback Converter as a Power Factor Correction Stage for Lighting

BY

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PREFACE

This thesis is submitted for the degree of Master of Science at TU Delft.The research described herein was conducted under the supervision of Professor.dr.J.A Ferreira in the Department of Electrical Sustainable Energy, the Facility of Electrial Engineering, Mathematics and Computer Science, TU Delft and and Reinhold Elferich in the Electronics and Sensing Group, Philips Lighting.

Nowadays, the LED drivers have to becomesmaller and more efficient in order to be suitable for more and new lighting applications. However, these drivers still have to comply with the strict regulations for lighting equipment like a high power factor or safety isolation. The miniaturization of a power factor correction stage that incorporates the safety isolation would be helpful for the whole driver's size down.

This master thesis project investigates the active clamp flyback converter as an miniaturized and high efficient power factor correction stage for lighting .Allthough this topology has been known for more 25 years it only recently has gained wider interest a.o. for power adapter applications. The upcoming GaN power transitors allow mastering substantially increased switching frequencies while keeping the power losses low and therefore offer the desired miniaturization potential.

Chapter 1: outlines the motivation, objectives and approaches of this project

Chapter 2: introduces the power factor correction background and solutions;

Chapter 3: describes the operation characteristics of the active clamp flyback converter and a summary of benefits and drawbacks of this topology;

Chapter 4: presents the step by step design process: The control method for the transistors; The choice of the conduction mode; The design of the components; The design of the dead times as well as the transformer design;

Chapter 5: describes the experimental results.

Chapter 6: contains the conclusion and proposes future work.

Due to confidentiality, the dead time design is shown seperately in appendix.

I am very grateful that Philips Lighting could offer me this opportunity to work on this promising project.I feel really proud that I could work with those talent person in this group.This project has been challenging, but inspiring, and has given me great insight

within power electronics and provided me an opportunity to know myself better.

Ruyu Li
Eindhoven, August 2017

ABSTRACT

A Driver with a high power factor, small size and safety isolation is desired in a number of lighting applications. Regarding topologies for isolated power factor correction (PFC) stages. the flyback converter is the common choice due to its ability to cover large gain ratios and is simplicity.

Regarding the miniaturization however, the conventional flyback is of limited use. One difficulty is related to the energy stored in its transformer's leakage inductance which typically is dissipated in apassive clamp network to avoid an excessive voltage stress at the switching transistor.. Since further hard switching cannot be avoided the switching frequency is limitedand the transformer of the passive clamp flyback is bulky particularly for a wide mains PFC application.

The aim of this project is to investigate high switching frequency active clamp flyback converter with GaN transistor as a power factor correction stage. By means of the active clamp loop the leakage inductance energy and snubber loss could be utilized properly to allow for ZVS on both switches under all line and load conditions. So high switching frequency and high efficiency are both achievable.

In this project a specific control method, dead time length and conduction mode are designed for active clamp flyback converter as PFC in the lighting application. The implementation of a closed loop control is not included. A 50W (75V) prototype of an active clamp flyback PFC front end converter operating at around 1MHz with GaN transistors e is developed to validate the analysis.

Keywords – Active clamp flyback, ZVS, high switching frequency, e-mode GaN transistor, power factor correction, Lighting

ACKNOWLEDGEMENTS

This is a very fabulous two years experience.The first year, I lived in Delft to study in TU Delft. The second year, I moved to Eindhoven to start my internship and master thesis in Philips Lighting.

On the submission of my master thesis report of "**A MHz Switching Active Clamp Flyback Converter as a Power Factor Correction Stage for Lighting**",I would like to give my most sincere thanks to all the people I known in these two years. Without them, it is impossible for me to grow into a better person than two years ago.

First and foremost, I would like to express my sincere thanks to Dr.ir.Reinhold Elferich, my thesis supervisor at Philips Lighting. His responsible guidance, patient explanation and instructive suggestions helped me to break through all the difficulties in this project.

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Special thanks to Dr.ir.Yi Wang, who is my internship mentor in Philips lighting.He introduced me to the fantastic electronics world and taught me how to work in a company. He gave me so much precious comment during my thesis project.Without his help, this project could not finish on time.

Another special thanks to Ir.Binghong Wang, my another thesis mentor in Philips Lighting.When I met any problem, he was always be with me to solve it.He gave me many supports during this project and encouraged me to break through all the fairs.

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Last but not least, I want to express my love to my parents and my friends.It is their understanding, support and encouragement that drive me forward.

Ruyu Li
Eindhoven, August 2017

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1

Introduction

In this chapter, the motivation, the objectives and approaches of this project are discussed.

1

1.1. MOTIVATION

Recently, the lighting industry consumes 25% of the electrical energy produced in the world [1]. The improvement of the energy utilization rate in lighting could have significant effect in energy saving and ease energy shortage.

LEDs are low voltages device.So it always requires a driver to transfer the main AC power supply to a low DC voltage which LEDs could work on.

Figure 1.1: An example of LED and its driver

The size and shape of LED lamps and tubes are various for different applications, power level and other specifics of the application. Nowadays, in order to be suitable for more lighting products, a LED drivers with high power factor, small size,high efficiency and safety isolation front end is more attractive.

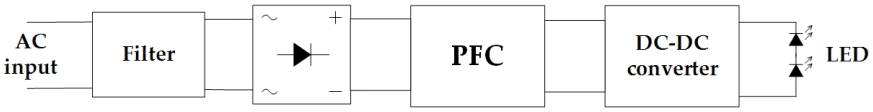

Figure 1.2: Simplified LED driver circuit

A typical LED driver contains several parts as shown in Fig1.2. Power factor correction stage is an essential part in LED drivers, which has two major functions.The first one is to force the input current to be in phase with input voltage, in order to achieve a higher power factor and lower THD to meet the requirement in IEC 61000-3-2 standard [2]. The other function is to regulate its output DC voltage to be flat with less e.g. than 10% peak to peak ripple, which will be the input voltage for the DC-DC converter in the next stage.A miniaturization of power factor correction stage would be helpful for the whole driver's size down.

This master thesis project is to investigate a smaller size and high efficiency power factor

correction stage for the lighting application.

1.2. PROJECT OBJECTIVES

This project is to built a converter to achieve the four objectives:

1. Smaller size
2. Isolation
3. High efficiency
4. PFC

The flyback topology is suitable for combining power factor correction, isolation and output voltage regulation into one power converter step. So this is an ideal topology for this project.

But the major problem of flyback converter is the voltage ringing on the transistor.The transformer in flyback topology contains leakage inductance. The energy stored in leakage inductance will cause large voltage spike on transistor when it turns off. So there is a risk for transistor to be broken down.

Generally, a clamping circuit is needed for flyback converter to overcome this problem.For passive clamp flyback converter, its clamping circuit is formed by passive components – resistance, capacitance and diode. The leakage inductance energy is dissipated as heat on resistance.This part of loss is proportional to switching frequency. So the switching frequency of passive clamp flyback converter could not go up to $500kHz$ and the transformer size stays bulky.

So the active clamp flyback converter is chosen as the topology for this project.In 1992, active clamp flyback converter was published in [3].Allthough this topology has been known for more 25 years,it only recently has gained wider interest i.e. for power adapter applications. The upcoming GaN power transitors allow mastering substantially increased switching frequencies while keeping the power losses low and therefore offer the desired miniaturization potential.

1.3. APPROACHES

The approaches to achieve objectives in this project:

1. The converter will be designed to work at a high switching frequency to reduce the required inductance value.So the transformer's size could be reduced.
2. The transformer in flyback converter could provide an electric isolation for the circuit.

3. The actively clamping circuit and GaN transistor would be utilized to achieve high efficiency.

   Actively clamping circuit could provide a loop for leakage inductance energy to recycle to input source. And the negative inductance current could discharge the output capacitance of both transistors to achieve zero voltage switching on both transistors.[3][4]

4. A proper control method would be designed to shape the input current to be in phase with input voltage and regulate the output voltage.

   Because this project is focusing on size and efficiency, the implementation of closed control loop is not included. A open loop prototype will be built to verify the design

2

POWER FACTOR CORRECTION

In this chapter, the power factor correction background and solutions are introduced.

2.1. POWER FACTOR

THE definition of Power Factor is the ratio of real power to apparent power[1]

$$PowerFactor = \frac{Average\ Power}{RMS\ Voltage * RMS\ Current}$$

Average power is the amount of power used by the load. The apparent power is defined as the product of the rms voltage and rms current. It indicates the power transmitted from the source into the load circuit. The value of power factor is between 0 to 1.A low power factor value indicates that more current is drawn from the power supplier into the circuit.

When the power factor is unity, the load could be considered as a resistance. [5][6] So the voltage and current are in same shape and in phase with each other.

When the power factor is low, there are two main disadvantages. First, the amount of reactive power is increased,which the electricity supplier needs to provide. But this extra part is useless, just a small portion is used by the load. The utilization of energy is low and customers need to pay extra money on it. Second, there will be large harmonic component in the distorted input current. Those harmonics would have effect to the operation of power grid and affect the performance of other equipment on the same line.[5][6]

2.2. POWER FACTOR CORRECTION

THE purpose of power factor correction circuit is to shape the input current to be in phase with input voltage and minimize the harmonic distortion on input current.

2.2.1. WITHOUT POWER FACTOR CORRECTION

The rectifier bridge is followed by a storage capacitor. This capacitor could maintain the output voltage near a constant value. But this will cause that the diodes will only conduct when the input voltage is higher than the capacitor voltage. So the conduction angle is limited by the desired output voltage.

$$V_{desired} = \sqrt{2} * V_{in} * sin(\theta_c)[1]$$

Where:
$V_{desired}$ is the desired output voltage of the rectifier bridge
V_{in} is the input RMS voltage
θ_c is the conduction angle

A higher and flat output voltage would lead to a short conduction period. So the input current is drawn from the power supply only at the peak of the input waveforms, like a pulse. In order to transfer enough energy to the circuit, the peak of the magnitude of the current pulse must be several times higher than the average current needed.[5][6]

2.2.2. PASSIVE POWER FACTOR CORRECTION

A passive PFC uses extra passive components in the circuit. There are several ways to construct a passive PFC: an AC side inductor; a DC side inductor; L-C filter.[5][7]

Although the passive PFC has advantages, such as simplicity, robustness, low EMI and low high switching frequency losses, it has several drawbacks.it should be noted that the input line power frequency is 50Hz or 60Hz, the passive components needs to work under the same frequency. This will cause heavy and bulky components.[8][9]

2.2.3. ACTIVE POWER FACTOR CORRECTION

An active PFC circuit employs active components, e.g. MOSFETs, and a switch mode power converter with a much higher switching frequency than line the frequency [7].Different DC/DC con- verter topologies could be used in this application with proper control method.

The main functions of the active power factor correction:

1. Shape the input current
2. Control the output voltage via feedback loop

Comparing with Passive PFC circuit, active PFC circuit is more light and effective. Furthermore, it can stabilize the output voltage by a feedback loop and allow a wide input voltage range. However, because of the additional components, the cost of the circuit increases.

Here, the power factor correction has two functions.

For safety reason, isolated PFC is more attractive in commercial lighting application. In switching power supply, the electrical isolation is provided by a high-frequency isolation transformer. With this electrical isolation, if the transistor or diode is broken, the load will be separated from the high voltage input.[8]

2.3. FLYBACK CONVERTER AS PFC

There are several isolated converter topologies – e.g. Forward converter, Flyback converter, Push-pull converter, Half bridge and Full bridge.[5]

The advantages of using the flyback topology:

1. Simplest isolated topology and least components needed among other isolated topologies.
2. It is appropriate for wide input voltage range. Because the output voltage is easily controlled by adjust turns ratio and duty ratio.

3. Simple control schemes.

But the major disadvantage of the flyback converter is the voltage stress on the transistor.

Because there is energy stored in the leakage inductance of the transformer, when the main switch is turned off, in order to remain the unchanged of inductance current, the leakage inductance will release the energy and this can cause an excessive overvoltage across the switch. This overvoltage can exceed the breakdown voltage of the transistor. So the requirement of voltage rating should be relatively high.[8][9]

In order to solve the overvoltage problem on switch, a clamping circuit needs to be used to absorb the leakage energy. There are two types of clamping circuit could be used to limit the voltage spike on the transistor – **Passive clamp** and **Active Clamp**.[7]

2.3.1. PASSIVE CLAMP FLYBACK CONVERTER

Passive clamping circuit is using a RCD circuit or a Zener across the primary inductance to provide another loop for leakage inductance energy dissipation and suppress the voltage spike on the main switch.[9][10]

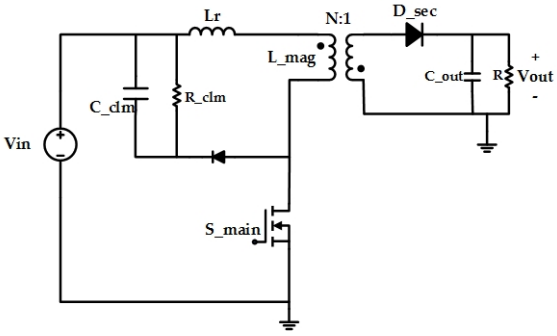

Figure 2.1: Passive Clamp Flyback Converter

The passive clamp circuit is very simple and effective. But the leakage energy will just be dissipated as heat.[8][9] Generally, the leakage inductance will be designed as small as possible to reduce the energy loss. In every switching cycle, the leakage energy will be dissipated once. At MHz switching frequencies, the leakage energy loss will be very considerable. This limits the passive clamp flyback converter in high frequency application. [10][11]

Another drawback of Passive clamp Flyback converter is the high current stress and bigger transformer size. In order to reduce the switching loss on main switch and secondary side rectifier, the passive clamp flyback converter is always designed to work in BCM and DCM. So ZCS could be achieved at Turning On of main switch and Turning off on secondary rectifier. But the peak and ripple of inductance current value are relatively high.

This will cause the transformer loss goes higher. So when design the transformer, the volume of it will be bigger.

2.3.2. ACTIVE CLAMP FLYBACK CONVERTER

Active clamp circuit uses an extra active component – a transistor and an extra capacitor to form an extra loop.[3][4] With this loop, the voltage stress between drain and source is clamped and the leakage energy could be recycled back to power source. Also, with proper design of control method and timing, the main switch Smain and Auxiliary switch S2 could achieve ZVS to further minimize the switching loss.[4][12]

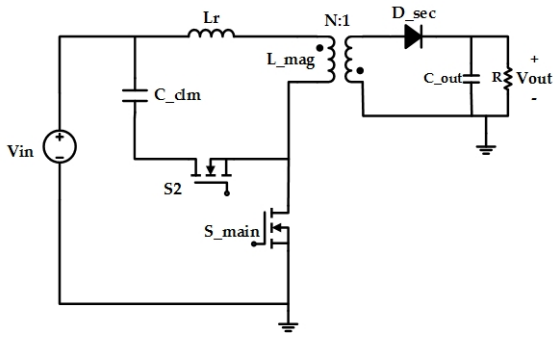

Figure 2.2: Active Clamp Flyback Converter with main switch S_{main} and auxiliary switch S2 (both MOSFETs)

Because of the low switching loss and leakage inductance energy utilization, active clamp flyback converter is very suitable in higher switching frequency application. More recently its application in power adaptors has been considered. By the combination of GaN switches and AC flyback converter, a high efficiency could be achieved[13] [14]. However, these adapters of up to 70W do not require a high power factor. The prototype efficiency of the state of are AC flyback converter is becoming very popular in adapter application.

3

Active Clamp Flyack Converter

This chapter describes the operation characteristics of the active clamp flyback converter and a summary of benefits and drawbacks of this topology;

3.1. THE DEFINITION OF CONDUCTION MODE IN ACTIVE CLAMP FLYBACK CONVERTER

WITH the auxiliary switch S2, there is an extra loop for circuiting primary side current. This causes two main differences of the waveforms in Active Clamp flyback converter from it in Passive Clamp flyback converter.

The magnetizing current in passive clamp flyback converter has three different shapes, which causes the converter has three different conduction modes – **Continuous conduction mode**; **Boundary conduction mode**; **Discontinuous conduction mode**.[5]

But in active clamp flyback converter, the magnetizing current could become negative because of the auxiliary switch loop. So the magnetizing current is always continuous, but it could go negative. According to this characteristic, the conduction mode of AC flyback converter could be defined as two modes according to the direction of magnetizing current.

3.1.1. UNIDIRECTIONAL CONDUCTION MODE

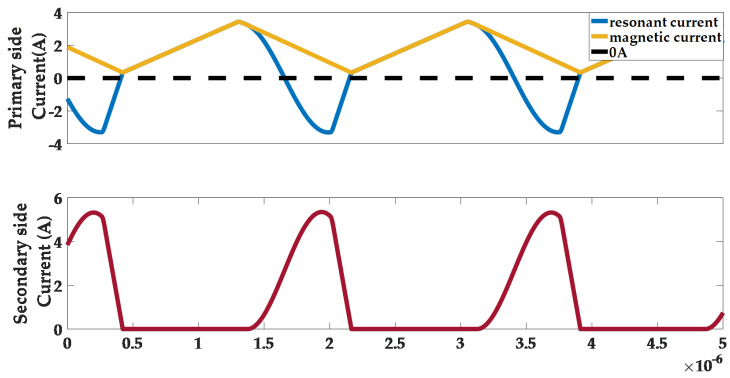

Figure 3.1: The current waveforms in Unidirectional conduction mode (85V peak, 50W)

In unidirectional conduction mode, the magnetizing current will be always positive. Meanwhile, the primary side current will go negative as shown in figure3.1.

3.1.2. BIDIRECTIONAL CONDUCTION MODE

In bidirectional conduction mode, the magnetizing current will be both positive and negative as shown in Figure 3.2.

3.2. THE OPERATION OF ACTIVE CLAMP FLYBACK CONVERTER

Seven operation stages can be distinguished for AC flyback converter in steady state as shown in figure 3.3. The first 5 stages are independent of the operation mode.

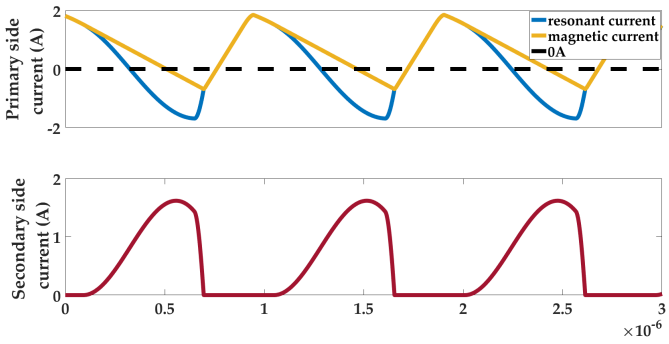

Figure 3.2: The current waveforms in Bidirectional conduction mode (230V peak, 25W)

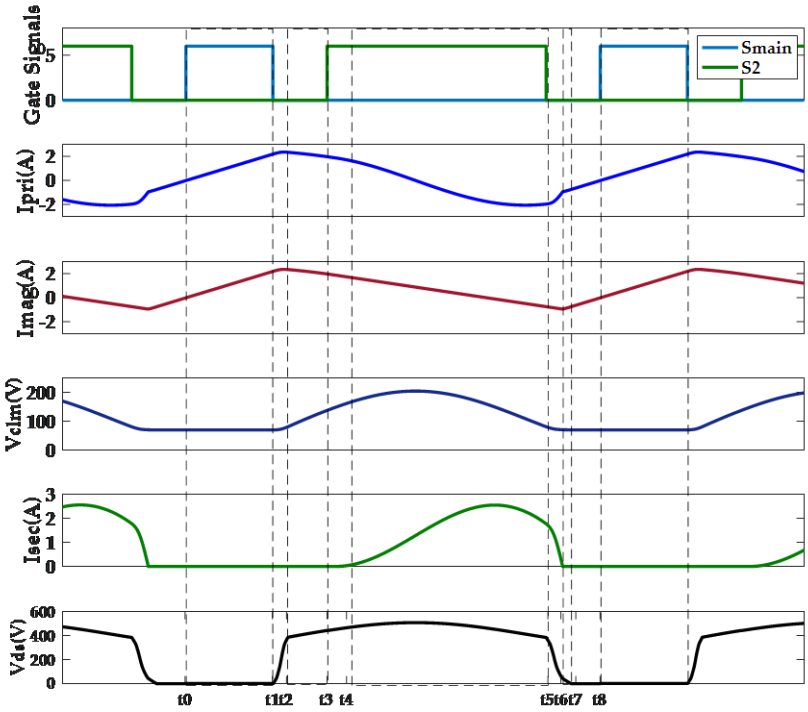

Figure 3.3: waveforms of the Active Clamp Flyback Converter

3.2.1. THE FIRST 5 STAGES

- Stage 1:Magnetizing stage t_0 - t_1

In this stage, the main switch Smain is on and the auxiliary switch S2 is off. The voltage on magnetizing inductance L_{mag} and resonant inductance L_r are positive, so the magnetizing current increases linearly.

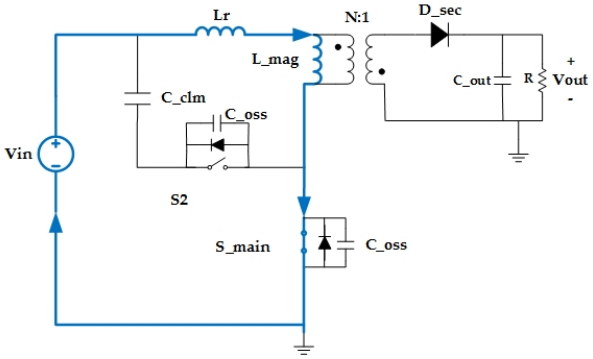

Figure 3.4: Stage 1 – Magnetizing stage

The magnetizing current and primary current are the same.

$$i_{Lmag} = i_{Lr} = i_{Lmag}(0) + \frac{V_{in}}{L_{mag} + Lr} * (t - t_0)$$

- Stage 2: Dead time stage t_1 - t_2

  At t1, the main switch is turned off, the inductance current splits into two parts to charging the output capacitance of S_{main} and discharging the output capacitance on S_2.

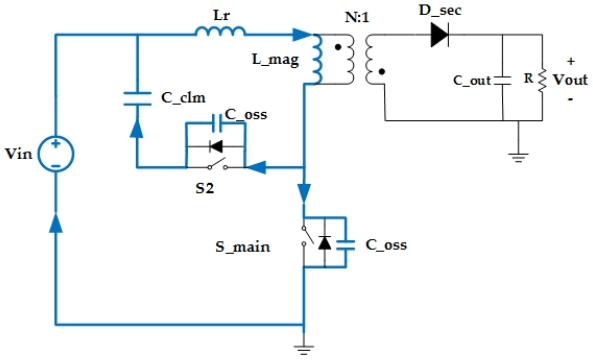

Figure 3.5: Stage 2 – Dead time stage

It should be noted that the value of output capacitance is a non-linearly function of the drain - source voltage V_{ds}.[15] Here in order to simplify the calculation process, the capacitance value of the C_{oss} is approximated as

$$C_{oss} = \frac{C_{oss}(0V) + C_{oss}(V_{ds})}{2}$$

Firstly, this simplification however is roughly appropriate only for the GaN transistors under consideration. Due to the absence of a body diode the nonlinearity of these devices is less pronounced as compared to e.g. recent super-junction MOSFETs. More details can be found in [16]. Secondly, regarding the PFC context, Vds is not a constant but varies according to the instantaneous line voltage.

Another fact needs to be pointed out is that the two transistors are the same.Meanwhile, the starting and ending V_{ds} across them are reversed. So the equivalent capacitance of this two C_{oss} could be expressed as

$$C_{oss_{equ}} = 2 * \frac{C_{oss}(0V) + C_{oss}(V_{ds})}{2} = C_{oss}(0V) + C_{oss}(V_{ds})$$

The circuit could be simplified to a resonant circuit formed by L_r, L_{mag} and C_{oss}.So the equations for this stage are:

$$i_{Lmag} = i_{Lr} = i_{Lr}(t_1) * cos(\omega_1 * (t - t_1)) + \frac{V_{in}}{Z_1} * sin(\omega_1 * (t - t_1))$$

$$V_{cout} = V_{in} - V_{in} * cos(\omega_1 * (t - t_1)) + Z_1 * i_{Lr}(t_1) * sin(\omega_1 * (t - t_1))$$

Where:

$$\omega_1 = \frac{1}{\sqrt{(L_{mag} + L_r) * C_{oss_{equ}}}} \qquad Z_1 = \sqrt{\frac{L_{mag} + L_r}{C_{oss_{equ}}}}$$

This time interval is very short because of high discharging/charging current.

- Stage 3: Dead time stage t_2 - t_4

  The voltage on the clamping capacitor has been charged to $V_{in} + V_{clm}$, so the body diode across S_2 is turned on. As already mentioned, the preferred devices for his converter are enhancementmode GaN HEMTs, which do not have the intrinsic body diodes of MOSFETs. They however, show a similar third quadrant conduction behavior (at a higher source-to-drain voltage though). Therefore, and in the interest of simplicity, the concept of a 'body diods' is used throughout this explanation of the operation states.

  In this time interval, the inductive current charges the resonant capacitor $Cclm$.

$$i_{Lmag} = i_{Lr} = i_{Lr}(t_2) * cos(\omega_1 * (t - t_2)) + \frac{V_{in}}{Z_2} * sin(\omega_1 * (t - t_2))$$

$$V_{cout} = V_{in} - V_{in} * cos(\omega_1 * (t - t_2)) + Z_2 * i_{Lr}(t_2) * sin(\omega_1 * (t - t_2))$$

Where:

$$\omega_2 = \frac{1}{\sqrt{(L_{mag} + L_r) * C_{clm}}} \qquad Z_2 = \sqrt{\frac{L_{mag} + L_r}{C_{clm}}}$$

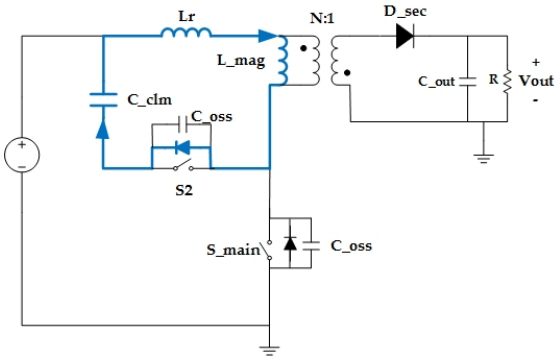

Figure 3.6: Stage 3 – Dead time stage

At the end of t_4, the auxiliary switch S_2 is on and the voltage on the resonant capacitor C_{clm} is charged to

$$V_{clm} = n * V_o * \frac{L_r + L_{mag}}{C_{clm}}$$

So the voltage on the magnetizing inductance has reached the reflected output voltage $n * V_o$ and the secondary side rectifier becomes forward biased and begins to conduct. The current difference between the magnetizing current and the current is the reflected output current.

It should be noted that the auxiliary switch S2 should be turned on when the body diode is conducting to achieve ZVS.

- Stage 4:Resonant Stage t_4 - t_5

  The secondary side diode is conducting, so the voltage on the magnetizing inductance is clamped to $-n*V_O$ and a primary side circuit on the primary side is formed by resonant inductance L_r and resonant capacitance C_{clm}.

$$i_{Lr} = i_{Lr}(t_4) * cos(\omega_4 * (t - t_4)) + \frac{n * V_o - n * V_o * \frac{L_{mag}+L_r}{L_{mag}}}{Z_4} * sin(\omega_4 * (t - t_4))$$

$$V_{clm} = n*V_o-(n*V_o-n*V_o*\frac{L_{mag}+L_r}{L_{mag}})*cos(\omega_4*(t-t_4))+Z_4*i_{Lr}(t_4)*sin(\omega_4*(t-t_4))$$

$$i_{Lmag} = i_{Lmag}(t_4) - \frac{n * V_o}{L_{mag}} * (t - t_4)$$

$$i_{diode} = n * (i_{Lr} - i_{Lmag})$$

Where:

$$\omega_4 = \frac{1}{\sqrt{(L_r * C_{clm})}} \qquad Z_4 = \sqrt{\frac{L_r}{C_{clm}}}$$

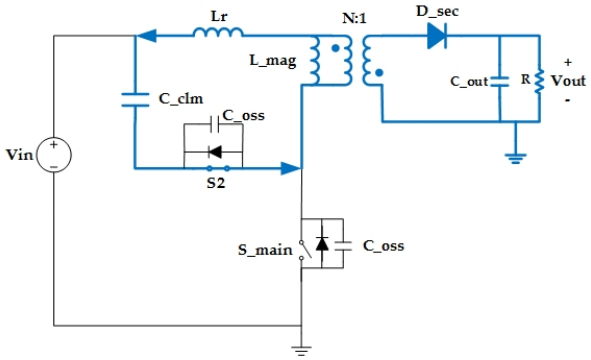

Figure 3.7: Stage 4 – Resonant stage

- Stage 5:Dead time t_5 - t_6

  The auxiliary switch S2 is turned off. The resonant current splits into two parts. discharging the output capacitance of S_{main} and charging the one of S2.

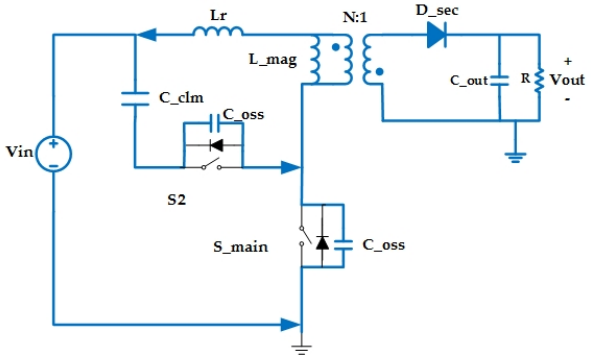

Figure 3.8: Stage 5 – Dead time stage

$$i_{Lr} = i_{Lr}(t_5) * cos(\omega_5 * (t - t_5)) + \frac{V_{in} + n * V_o - V_{coss}(t_5)}{Z_5} * sin(\omega_5 * (t - t_5))$$

$$V_{clm} = V_{in} + n * V_o - (V_{in} + n * V_o - V_{coss}(t_5)) * cos(\omega_5 * (t - t_5)) + Z_5 * i_{Lr}(t_5) * sin(\omega_5 * (t - t_5))$$

$$i_{Lmag} = i_{Lmag}(t_5) - \frac{n * V_o}{L_{mag}} * (t - t_5)$$

Where:

$$\omega_5 = \frac{1}{\sqrt{(L_r * C_{oss_{equ}})}} \qquad Z_5 = \sqrt{\frac{L_r}{C_{oss_{equ}}}}$$

3.2.2. THE FOLLOWING STAGES

The next two intervals are depend on the operation Three cases can be distinguished:

1. The output stops conducting (at t6) before the voltage at the switch node has been commutated (at t7)

2. The output stops conducting (t7) after the voltage at the switch node has been commutated (t6).

3. The output stops conducting (t8) after the voltage at the switch node has been commutated (t6) and the main switch has been turned on again (t7).

CASE 1: THE OUTPUT STOPS CONDUCTING BEFORE THE SWITCH NODE COMMUTATION

This situation is under bidirectional conduction mode.

The magnetizing current will be negative at t7.So it will take a short time for the primary side current reaching the magnetizing current.

After the two current equaling to each other, the voltage on the magnetizing inductance Lm will not be clamped any more. The magnetizing inductance Lm will also help to discharge/charge output capacitors.

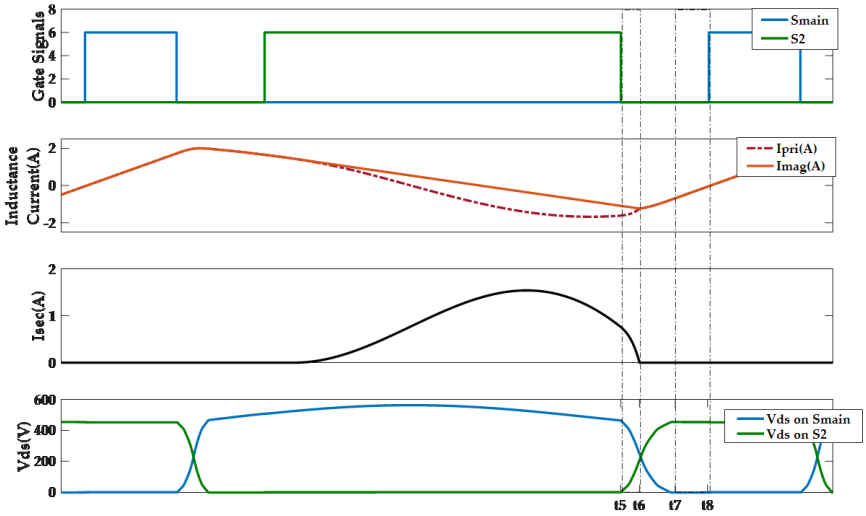

Figure 3.9: Case 1:The equaling time is before the fully discharging time

- Stage 6:Dead time t_6 - t_7

At the end of t6, the difference between primary side current and magnetizing current is 0. So the current on secondary side is 0A and the rectifier stops to conduct.

The voltage on the magnetizing inductor is not clamped at –n*Vo any more. So the magnetizing inductance will participate in discharging/ charging output capacitors in each transistor.

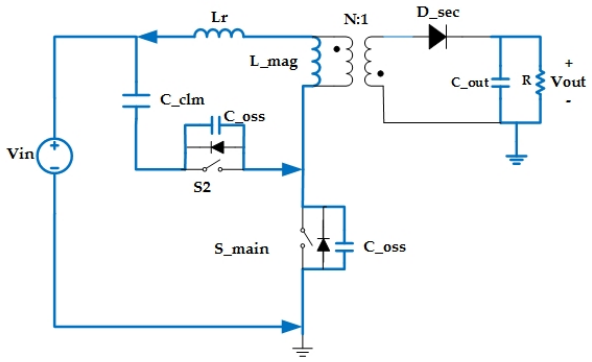

Figure 3.10: Stage 6 (Case1) – Dead time stage; the output does no longer conduct

$$i_{Lmag} = i_{Lr} = i_{Lr}(t_6) * cos(\omega_1 * (t - t_6)) + \frac{V_{in} - V_{clm}(t_6)}{Z_6} * sin(\omega_6 * (t - t_6))$$

$$V_{coss} = V_{in} - (V_{in} - V_{clm}(t_6)) * cos(\omega_6 * (t - t_6)) + Z_6 * i_{Lr}(t_6) * sin(\omega_6 * (t - t_6))$$

Where:

$$\omega_6 = \frac{1}{\sqrt{(L_{mag} + L_r) * C_{oss_{equ}}}} \qquad Z_6 = \sqrt{\frac{L_{mag} + L_r}{C_{oss_{equ}}}}$$

- Stage 7: Main switch reverse conducting t_7 - t_8

  In this stage, the direction of primary side current is still negative. The voltage on magnetizing inductance and resonant inductance are both positive. So the inductance current increases linearly.

  Main switch should be turned on in this stage before the inductance current being positive again. So the dead time should not be longer than the ¾ of resonant period.

$$i_{Lmag} = i_{Lr} = i_{Lmag}(t_7) + \frac{V_{in}}{L_{mag} + L_r} * (t - t_7)$$

CASE 2: THE OUTPUT STOPS CONDUCTING AFTER THE SWITCH NODE COMMUTATION

This situation is mostly under unidirectional conduction mode, i.e. lower input voltage and high output power. The required average input current is relatively high. So the peak inductance current value is also high.

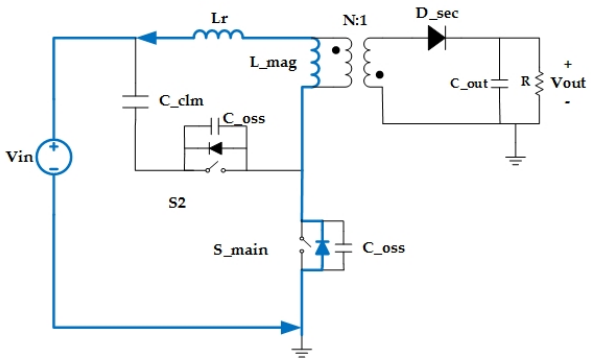

Figure 3.11: Stage 7 – Main switch reverse conducting

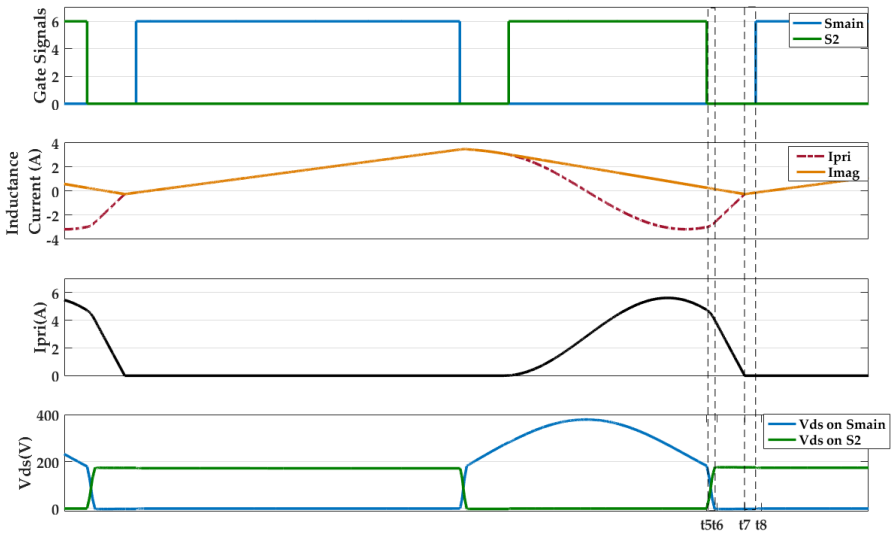

Figure 3.12: Case 2:The equaling time is between the fully charging time and Smain turning on time

- Stage 6 (case 2):Dead time t_6 - t_7

  At time t6, the output capacitors are fully charged and discharged respectively. Meanwhile, the current difference between magnetizing current and resonant current has not reached 0. There is energy transferred to the secondary side. So the voltage on the magnetizing inductance is still clamped at $-n * V_o$.

  The voltage on the resonant inductance L_r is positive and the value is relatively high.

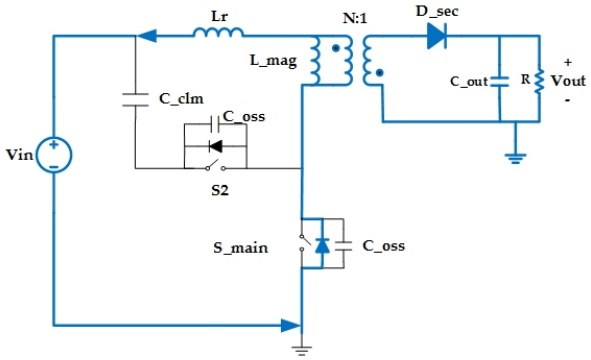

Figure 3.13: Stage 6 (Case 2)– Dead time stage

$$V_{Lr} = V_{in} + n * V_o$$

So the current on the resonant inductance will increase linearly in a high rate.

$$i_{Lr} = i_{Lr}(t_6) + \frac{V_{in}}{L_r} * (t - t_6)$$

$$i_{Lmag} = i_{Lmag}(t_6) - \frac{n * V_o}{L_{mag}} * (t - t_6)$$

- Stage 7: Main switch reverse conducting t_7 - t_8 In this stage, the direction of reso-

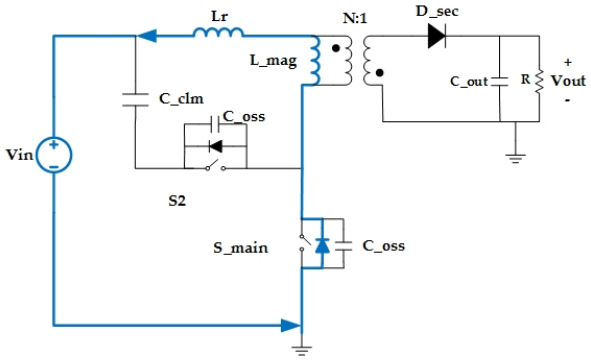

Figure 3.14: Stage 7 (Case 2)– Main switch reverse conducting

nant current is still negative. The voltage on magnetizing inductance and resonant inductance are both positive. So the inductance current increases linearly.

$$i_{Lmag} = i_{Lr} = i_{Lmag}(t_7) + \frac{V_{in}}{L_{mag} + L_r} * (t - t_7)$$

Main switch should be turned on in this stage before the inductance current being positive again. So the dead time should not be longer than the ¾ of resonant period.

CASE 3

This situation is under lower input voltage and high output power. The required average input current is relatively high. So the peak inductance current value is also high.

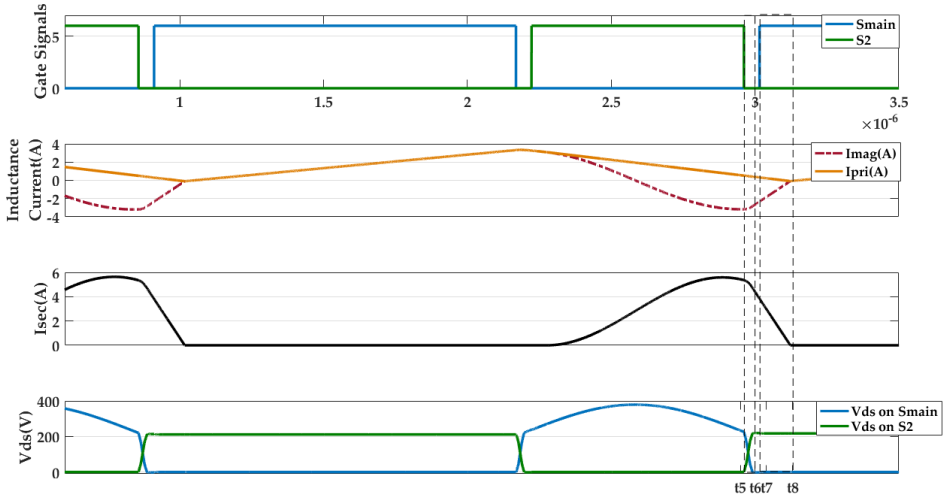

Figure 3.15: Case 3:The equaling time is after Smain turning on time

If the dead time is shorter than the required equaling time, the secondary side rectifier would still conduct even after the main switch is turned on again.

- Stage 6:Dead time t_6 - t_7 This time interval is the same as previous conduction mode.

$$i_{Lr} = i_{Lr}(t_6) + \frac{V_{in}}{L_r} * (t - t_6)$$

$$i_{Lmag} = i_{Lmag}(t_6) - \frac{n * V_o}{L_{mag}} * (t - t_6)$$

- Stage 7: Non-effective Duty ratio stage

  At t7, the Smain is turned on again. But because the dead time is too short for this operation point, the current difference between magnetizing current and resonant current has not reached 0. There is still current conducting through the secondary side rectifier.

  So the voltage on the magnetizing inductance is still clamped at $-n * V$o. The magnetizing inductance will start to re-magnetize until the secondary side rectifier is

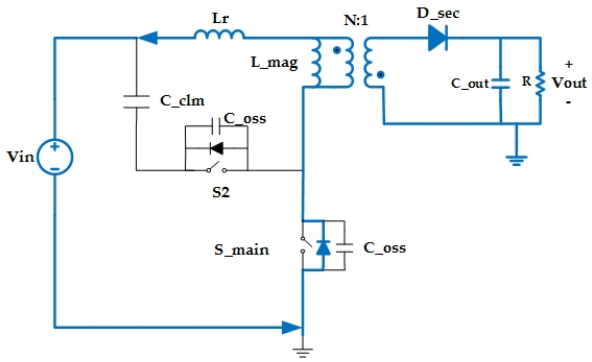

Figure 3.16: Case3:Stage 6 – Dead time stage

blocked.

$$i_{Lr} = i_{Lr}(t_7) + \frac{V_{in}}{L_r} * (t - t_7)$$

$$i_{Lmag} = i_{Lmag}(t_7) - \frac{n * V_o}{L_{mag}} * (t - t_7)$$

In passive clamp flyback converter, the leakage inductance value is quite small, so the current on the leakage inductance will equal to the magnetizing current very fast. But in active clamped flyback converter, the resonant (leakage) inductance value is relatively high, so the time needed is longer.

This will cause the effective duty ratio is less than the actual one. Here not sure if this will influence the efficiency or else. This will cause problem when the switching frequency is fixed. But in this project, the on time of Smain is controlled by the average input current, so the energy transferred into this system will not be influenced by this effective duty ratio problem.

3.3. THE ADVANTAGES AND DISADVANTAGES OF ACTIVE CLAMP FLYBACK CONVERTER

3.3.1. ADVANTAGES

- The utilization of leakage inductance

  The major problem of flyback converter is the energy in leakage inductance. If without clamp circuit, those energy will be released on the transistor. There will be large voltage spike on drain source voltage. A clamp circuit is needed here. In

passive clamp ,this part of energy is dissipated as heat. But in active clamp flyback converter, this part of energy will be recycled to the input source. And also it is used as discharging current to discharge output capacitance of both switches and to help them achieve zero voltage switch. [3][4]

- Virtually No Switching Losses

  In active clamp flyback converter, with the help of resonant current and active clamp loop, the main switch and auxiliary switch could be turned on in ZVS if the dead time is set properly. With the advantage, AC flyback converter is very suitable in high switching frequency application.

- High switching frequency is feasible

  As the snubber loss is proportional to the switching frequency, so passive flyback converter typically runs below 500kHz. [9][10]It sets a hard ceiling to power density and converter's size. But active clamp has the advantage of reclaimed leakage energy and ZVS, it could run at high switching frequency, so it is an ideal topology.

3.3.2. DISADVANTAGES

- The control system will be complex

  First, there are two transistor in this system, so two sets of control loops are needed. Second, if a higher efficiency is pursued, the dead time between two switches will be different at different operation points. The control system needs to detect the operation points and adjust the dead time to the corresponding value. Third, if the switching frequency is relatively high, the time scale is in nanosecond. This requires the responding speed of the control system is also very fast and the controlling should be very precise.

- Higher cost

  Comparing to passive flyback converter, AC flyback converter has an extra transistor as the auxiliary switch. This transistor needs extra gate driver and control circuit, so the cost of active clamp flyback converter will be higher.

3.4. CONCLUSION

In this chapter, the operation of active clamp flyback is explained in detail.The whole operation in one switching period has been divided into 7 stages.The first 5 stages are independent of the operation mode.The next 2 stages are dependent on the operation. Mathematical models are built for each stages. And the benefits and drawbacks of the active clamp flyback converter are summarized.

4

Choice of Control method, Conduction mode and Design of components

This chapter presents the step by step design process: The control method for the transistors; The choice of the conduction mode; The design of the components; The transformer design.

Due to confidentiality, the dead time design is shown seperately in appendix.

4.1. PFC SPECIFICATIONS

Input voltage range	$85V--265Vrms$ (Universal Line)
Output voltage	$75V$
Output Power	$50W$ Average

Table 4.1: PFC specifications

4.2. THE PRINCIPLE OF A PFC

POWER factor correction (PFC) controls the input current of power supply to be in phase with the input voltage, i.e. idealy, the only difference between input current and input voltage waveform is just amplitude.Therefore, the whole PFC converter could be treated as a pure resistance if looking from the input side.[5][6]

$$I_{in}(t) = \frac{V_{in}(t)}{R_{PFC}}$$

Where:
$Vin(t)$ is the instantaneous value of input voltage of the PFC converter.
$Iin(t)$ are the instantaneous value of input current of the PFC converter.
R_{PFC} is the equivalent resistance of the PFC converter.

$$R_{PFC} = \frac{\eta * V_{in_{rms}}^2}{P_{out_{ave}}}$$

Where:
$V_{in_{rms}}$ is the RMS value of input voltage.
$P_{out_{ave}}$ is the average output power in one switching cycle.
η is the efficiency of the PFC system.

$$\eta = \frac{P_{out_{ave}}}{P_{in_{ave}}}$$

Where:
$P_{out_{ave}}$ is the average output power in one switching cycle.
$P_{in_{ave}}$ is the average input power in one switching cycle.

Combine the previous three equations, the expression for required instantaneous input current is:

$$I_{in}(t) = \frac{V_{in}(t) * P_{out_{ave}}}{\eta * V_{in_{rms}}^2}$$

4.3. THE CHOICE OF CONTROL STRATEGY

The control strategy of active clamp Flyback Power Factor Correction circuit could be separated into two parts: the control of main switch and the control of auxiliary switch.

4.3.1. MAIN SWITCH CONTROL

Based on the operation principle of Flyback converter, the power is transferring into the converter when Smain is on and the stored power will be transferred to the output when Smain is off. So the control of main switch is shaping the input current of the system.

There are several choice for current shaping control: peak current control; average current control and hysteresis control.[5][17]

Peak current control is widely used in PFC controller, e.g. L6562A.[18] The magnitude of inductor current will be sensed by sensing resistors. When its value of reaches the reference current value, the main switch Smain will be turned off.

This method is very suitable for Boost converter, because the input current of Boost converter is continuous. But for Flyback converter, it is not ideal enough.

In flyback converter

$$I_{in} = D * I_{L_{ave}}$$

The relationship between average input current and inductance current has a ratio of D, which is dependent on input voltage, output voltage and turns ratio. Although the peak current follows the desired sine wave current shape, the average input current does not.

Hysteresis Current control: which is also called threshold control of tolerance control, shapes the current within a band. [19]This control method is widely applied in different converter because of its simply implementation and limiting the peak current inherently. But this also has the peak to average current error.

Average Current control:controls the average input current by introducing a high gain integrating current error amplifier into the current loop, which is with very high accuracy.And it overcomes the peak to average current error in the other two control method.[18]

So here, the average current control will be applied on main switch to achieve a high power factor and low distortion.

4.3.2. AUXILIARY SWITCH CONTROL

In order to achieve ZVS at the both transistors, three critierias need to be met. The first criteria is the energy stored in resonant inductance Lr should be large enough to fully discharge the energy stored in output capacitor. This could be achieved by a large size of resonant inductance and a large enough primary side current when *S*2 is turned off. The second criteria is that the direction of the primary side current should be anti-clockwise in order to be the discharging current of main transistor S_{main}. The third criteria is the dead time should be long enough to allow the C_{oss} to be fully discharged.

The first two criterias are controlled by the timing when the auxiliary switch S2 is turned off. In order to meet the two requirements:

1. When the auxiliary switch S2 is turned off, the direction of the resonant circuit should be anti-clock wise, i.e. it just reverses its direction once. This will make the primary side current to be the discharging current of C_{oss} on Smain.

2. When the auxiliary switch S2 is turned off, the magnitude of the resonant circuit should be a relatively large value to ensure the energy in resonant inductor L_r higher than the energy stored in C_{oss}.

When the S2 is on, the circuit is in the resonant stage as described in Chapter 2, the equations describes this stage is

$$i_{res} = i_{Lr} = i_{Lr}(t_4) * cos(\omega_4 * (t - t_4)) + \frac{n * V_o - n * V_o * \frac{L_{mag}+L_r}{L_{mag}}}{Z_4} * sin(\omega_4 * (t - t_4))$$

$$V_{res} = V_{clm} = n*V_o-(n*V_o-n*V_o*\frac{L_{mag}+L_r}{L_{mag}})*cos(\omega_4*(t-t_4))+Z_4*i_{Lr}(t_4)*sin(\omega_4*(t-t_4))$$

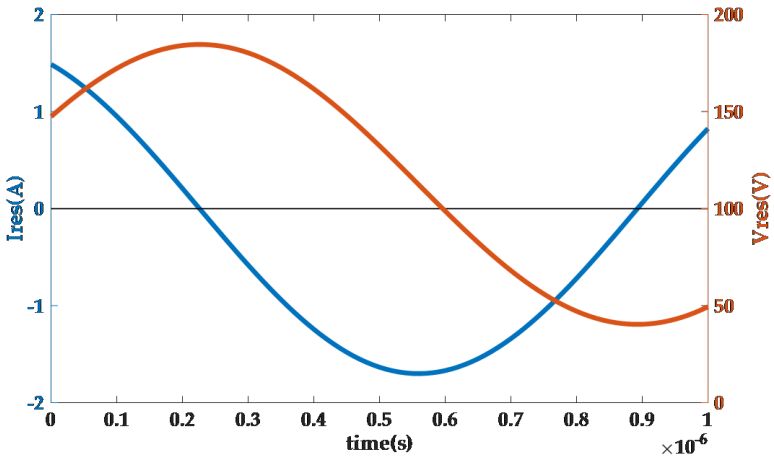

Figure 4.1: Resonant current and voltage when S2 is ON

The figure4.1 illustrates the waveforms for primary side current on L_r and resonant voltage on C_{clm}. If the auxiliary switch could be switched off near the negative peak of the resonant current. This could ensure the magnitude of the primary side current is relatively high and the direction of it is reversed once.

It should be noted that this stage is just the resonant circuit formed by L_r and C_{clm}. So the time when the primary side current reaches valley point is very clear – half of the resonant period.

$$T_{resonant} = 2 * \pi * \sqrt{L_r * C_{clm}}$$

$$T_{ON_{S2}} = \frac{T_{resonant}}{2} = \pi * \sqrt{L_r * C_{clm}}$$

It will be an easy way to set the On time of auxiliary switch as a constant value. So the constant On time control is chosen here to guarantee the primary side current could meet the two requirements.This results the switching switching frequency is variable.

Because the dead times between Smain and S2 are very short compared with the ON time of the other two switches, here just ignore them to have an approximate volt- second balance on magnetizing inductance L_{mag}.

$$T_{ON_{Smain}} * V_{in} = T_{ON_{S2}} * n * V_o$$

So the switching frequency is

$$T_{SW} = T_{ON_{Smain}} + T_{ON_{S2}} = T_{ON_{S2}} * (1 + \frac{n * V_o}{V_{in}})$$

Combine the previous two equations, the switching frequency could be expressed as

$$T_{SW} = \pi * \sqrt{L_r * C_{clm}} * (1 + \frac{n * V_o}{V_{in}})$$

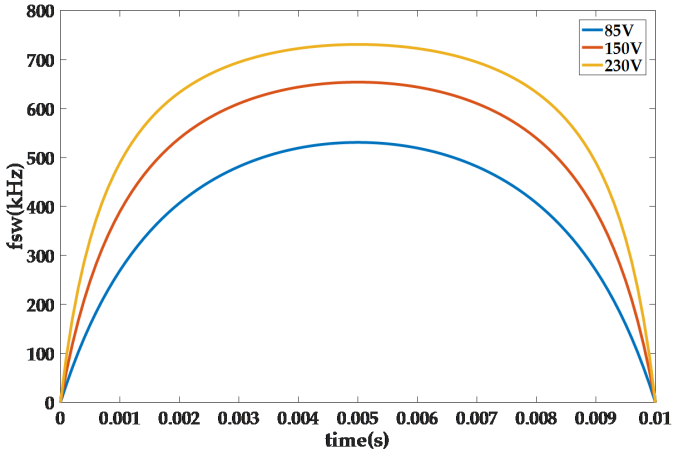

Figure 4.2: fsw under different input voltage

As showed in the equation and Fig4.2, if the output voltage stays constant, the switching frequency is just depended on the input voltage V_{in}, output voltage V_{out} and turns ratio N. But the output voltage also has significant voltage ripple at twice of the line frequency. The ripple is depended on the output load.

illustrated in figure 4.3, the switching frequency will be distorted because of the output voltage ripple.

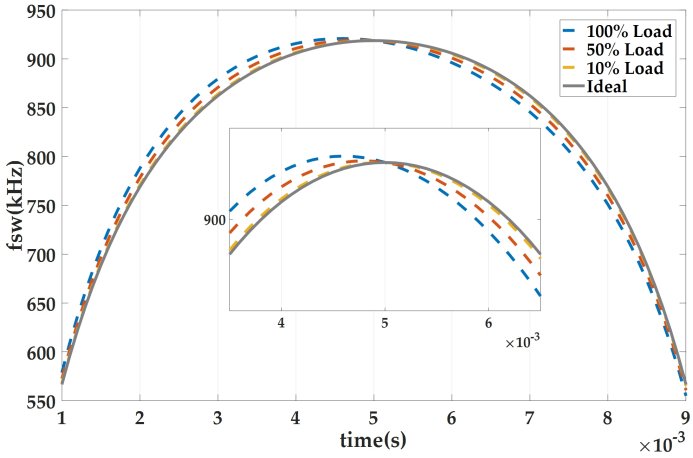

Figure 4.3: fsw under different Output Load

4.4. CHOOSE THE CONDUCTION MODE

This converter will work in both Bidirectional conduction mode and unidirectional conduction mode depended on different operation points.

Due to the constant turn ON of auxiliary S2, the current ripple of magnetizing current is nearly constant. So at different operation points, the DC offset of magnetizing current is different. With a constant ripple, it will cause different peak and valley inductance current value

This converter will work in unidirectional conduction mode when the output load is heavy and input voltage is low. Meanwhile, it will work in bidirectional conduction mode when the output load is light and input voltage is high.

Under low input voltage and heavy load condition, the required input current is relatively high. The energy stored in leakage inductance is high enough to fully discharge the energy on the output capacitance.

Under high input voltage and light load condition, the required input current is relatively low. So there may not be enough energy in leakage inductance to fully discharge the output. But the reversed magnetizing current could help to discharge the output capacitors.

So a mixed conduction mode is designed.

4.5. DESIGN OF COMPONENTS

4.5.1. TURNS RATIO

The transformer's turns ratio will mainly influence the voltage stress on primary and secondary switches. The voltage stress on primary side switch:

$$V_{ds} = V_{in} + V_{clm}$$

$$V_{clm} = V_{clm_0} + V_{res}$$

Where:
V_{ds} is the drain source voltage on transistor;
V_{clm} is the clamping voltage on clamping capacitor C_{clm};
V_{clm_0} is the initial value of clamping voltage;
V_{res} is the voltage ripple on clamping capacitor because of resonant with L_r

The stead state voltage value for Cclm is

$$V_{clm_0} = n * V_o + V_{in} * \frac{L_r}{L_r + L_{mag} * \frac{D}{1-D}} \approx n * V_o$$

Combine the previous equations:

$$V_{ds} = V_{in} + n * V_o + V_{res}$$

The value of the resonant voltage is depended on the clamping capacitor.The general voltage rating of GaN transistors is $650V$ and set 10% margin of the maximum value.

$$n_{max} = \frac{V_{breakdown} * 0.9 - V_{in_{max}} - V_{clmpeak}}{V_o}$$

Here, the resonant voltage is approximated as $n * V_o$. So the maximum turns ratio is 1.4.

4.5.2. MAGNETIC INDUCTANCE L_{mag}

The design of magnetic inductance in active clamp flyback is the same as in general flyback converter. Generally, the design of L_m is depended on which conduction mode the converter would work in.Here, the converter will work in mixed conduction mode. The worst point is at the lowest input rms voltage and full load. At this operation point, the converter will work in Unidirectional conduction mode, i.e. continuous conduction mode.

For CCM conduction mode: the design of the L_{mag} is dependent on $I\%$, the ratio of allowable peak – peak ripple current to peak current in the inductor. [19]

$$I\% = \frac{\Delta I}{I_{peak}}$$

The current ripple ΔI of a flyback converter over one switching cycle is

$$\Delta I = \frac{V_{in}(t)}{L_{mag}} * D * \frac{1}{f_{sw}}$$

Where:
$V_{in}(t)$ is the instantaneous input voltage;
L_{mag} is the magnetic inductance value;
D is the duty cycle;
f_{sw} is the switching frequency.

The relationship between average input current I_{in} and inductor current in Flyback converter is

$$I_{in} = \frac{1}{2} * D * (I_{peak} + I_{peak} - \Delta I)$$

Combine the equation and equation, the relationship between average input current and peak – peak ripple current is:

$$I_{in} = \frac{1}{2} * D * (\frac{2}{I\%} - 1) * \frac{V_{in}(t)}{L_{mag}} * D * \frac{1}{f_{sw}}$$

So the expression for magnetic inductance Lm could be get:

$$L_{mag} = \frac{V_{in_{rms}}^2 * \eta}{2 * P_{out_{ave}}} * (\frac{nV_o}{V_{in}(t) + nV_o})^2 * \frac{1}{f_{sw}} * (\frac{2}{\Delta I} - 1)$$

Here the I% could be chosen higher than the typical value, because in active clamp flyback converter, the resonant (leakage) inductance is much higher than general value. So it will influence the ripple current to be lower than the expected value.

4.5.3. RESONANT INDUCTANCE L_r

According to general papers which describe the design of resonant inductance L_r , the basic rule is to ensure that the energy stored in L_r is sufficient of to completely commutate the switch node's capacitance -as given by the output capacitance of the two switches- prior to turning on the main switch.[12][20] But this approach does not take into account the third operation mode, in which the energy stored in magnetic inductance L_{mag} also helps to discharge C_{osseq} . So that rule will result in a relatively large L_r which is not needed.

The value of L_r will influence three operation parameters in the converter: the switching frequency f_{sw}, the current ripple in magnetic inductance and the ZVS.

- Switching frequency

  The On time of the auxiliary switch S2 is determined by the resonant period of L_r and C_{clm}.

  $$T_{ON_{S2}} = \frac{T_{resonant}}{2} = \pi * \sqrt{L_r * C_{clm}}$$

Because the dead times between Smain and S2 are very short compared with the ON time of the other two switches, here just ignore them to have an approximate volt- second balance on magnetizing inductance L_{mag}.

$$T_{SW} = \pi * \sqrt{L_r * C_{clm}} * (1 + \frac{n * V_o}{V_{in}})$$

- ZVS

In order to guarantee the energy stored in resonant inductance Lr is large enough to fully discharge the output capacitor of transistors, two factors could be optimized. First, the magnitude of primary side current value should be high enough. This is achieved by the Constant Ton control on S2. Second, the value of resonant inductance should also be large enough.

When S2 is turned off, the energy stored in resonant inductance is:

$$E_{L_r} = \frac{1}{2} * L_r * I_{L_r}^2$$

Meanwhile, the energy stored in output capacitor is:

$$E_{C_{out}} = \frac{1}{2} * C_{oss} * V_{ds}^2$$

In general published papers, these two equations will be combined to have a expression for L_r:

$$L_r > \frac{C_{oss} * (V_{in} + nV_o)^2}{I_{t5}^2}$$

Where:
C_{oss} is the output capacitance of transistor;
I_{t5} is the primary side current when S2 is turned off.

This calculation will cause a relatively high resonant inductance value. Because in this equation, it doesn't take into account that the energy stored in the magnetic inductance Lm will also help to discharging the output as the third case described in Chapter 3.

A high resonant inductance will not only store energy, but also will give rise to oscillation with (unwanted) capacitances in the circuit (transformer capacitances, output rectifier capacitance). Also, it will be more difficult to design a transformer which has a large leakage inductance with a minimized volume. So the resonant inductance should also not too big.

- Current ripple Based on the previous design, the Ton time length of auxiliary switch S2 is fixed, so the current ripple on magnetic inductance is fixed.

$$I_{mag_{ripple}} = \frac{nV_o}{L_{mag}} * \pi * \sqrt{L_r * C_{clm}}$$

There are many criteria should be met when design the L_r. Also, the equations of T_{sw}, D, and I_{Lr} are functions of L_r.It makes L_r very difficult to solve and find an accurate value to strictly meet all the requirements.

Here, a resonant inductance is 1/3 of the main inductance would be a proper value.

4.5.4. CLAMPING (RESONANT) CAPACITOR

The same as resonant inductance, the value of clamping capacitance will influence the switching frequency, the inductance current ripple and the voltage ripple on the main transistor Smain.

The On time of the auxiliary switch S2 is determined by the resonant period of L_r and C_{clm}. So the switching frequency and current ripple are both determined by L_r and C_{clm}, as described in Section 3.4.3.

$$V_{clm_{peak}} = nV_o + Z_4 * I_{peak}$$

Where:
$V_{clm_{peak}}$ is the peak voltage value on clamping capacitor.

Although a larger C_{clm} could release the voltage stress on the main switch, the ON time of S2 also increases. As a consequence, the switching frequency will decrease and current ripple will increase.A larger magnetic inductance would be needed. The design of C_{clm} and L_r are very difficult to find an accurate value of strictly meet all the requirements.A proper C_{clm} should be chosen to achieve a limited voltage ripple and proper resonant period.

4.6. DESIGN OF MAGNETIC COMPONENT

The design of transformer in this project is based on the simulation result in MagTool, which could give an accurate estimation of core loss, winding loss and temperature change.

4.6.1. LAYOUT OF COIL FORMER

In active clamp flyback converter, the leakage inductance in a transformer could be used as the resonant inductance, which will help to discharging the output capacitance of

transistors to achieve ZVS. So the leakage inductance should be much higher than it in passive clamp flyback converter.

As shown in figure 4.4, the two windings are seperated into two parts: the primary winding is at the blue part; the secondary winding is at the green part. The gap between them could help to reduce the coupling coefficient between the two windings, which could result in a large leakage inductance.

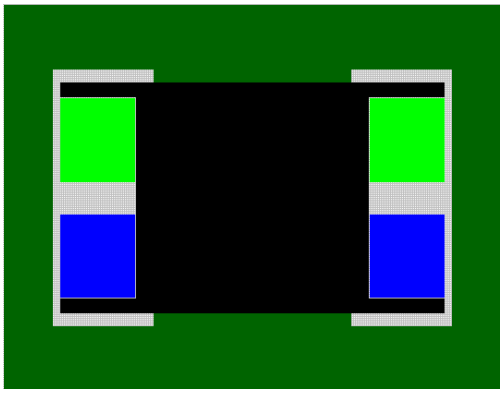

Figure 4.4: The layout of transformer coil former

4.6.2. MAGNETIC MATERIAL

The maximum switching frequency in this design is nearly 1MHz, the availability of magnetic materials and cores which is suitable for this operation range is limited. Recently, the available magnetic materials are 3F36, 3F4, and 3F46. [23]

3F36 is the optimum solution for the design operation range. Its general purpose transformer is working within $0.5MHz$ to $1MHz$.But due to long delivery time and further improvement possibility, 3F46 is using instead here.[23]

4.6.3. TRANSFORMER DESIGN RESULT

Magnetic material	3F46
Core	RM6S/I
Primary winding	17 turns 120*0.03mm
Secondary winding	13 turns 180*0.03mm
Mutual inductance	$26.66\mu H$
Leakage inductance	$10.93\mu H$
$N_p : N_s$	1.28:1

Table 4.2: Transformer design result

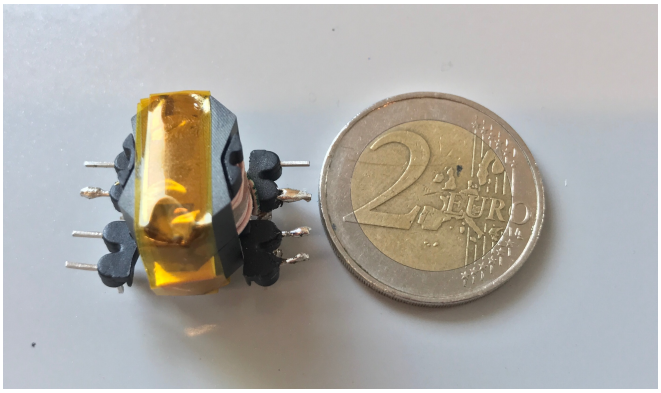

Figure 4.5: The design result of transformer

In the state of art passive clamp flyback converter in PFC application, the PQ25/20 [24] and PQ25/26 [25] transformer cores are used for 60W output requirement. Comparing with the design result in this project, the transformer's size has been reduced 6 times.As shown in fig 4.5, it is even less then a 2 euro coin.

4.7. CONCLUSION

This converter is designed to work in a mixed conduction mode depending on the line and load condition.And the two transistors have different control strategies. The main switch is working under average current control to shape the input current to be in phase with input voltage. The auxiliary switch is working under constant ON control to achieve ZVS at two transistors and recycle leakage inductance energy to input.The components in the converter are designed properly. Comparing with the state of art flyback converter in PFC application, the size of the transformer has been reduced 6 times.

5

Experimental Results

This chapter firstly describes the experimental set up and the validation method.Then, it presents how the secondary side diode influences the converter's performance;The following is overall efficiency of the designed converter and loss breakdown.Finally, the achievement of ZVS at different line and load condition is illustrated.

5.1. DESCRIPTION OF THE SET UP

THE basic measurement set up is based on n a GaN E-HEMT half bridge evaluation. This board contains two GaN 650V E-HEMTs, half bridge gate drivers, gate drive power supplies and heat sink.[26]

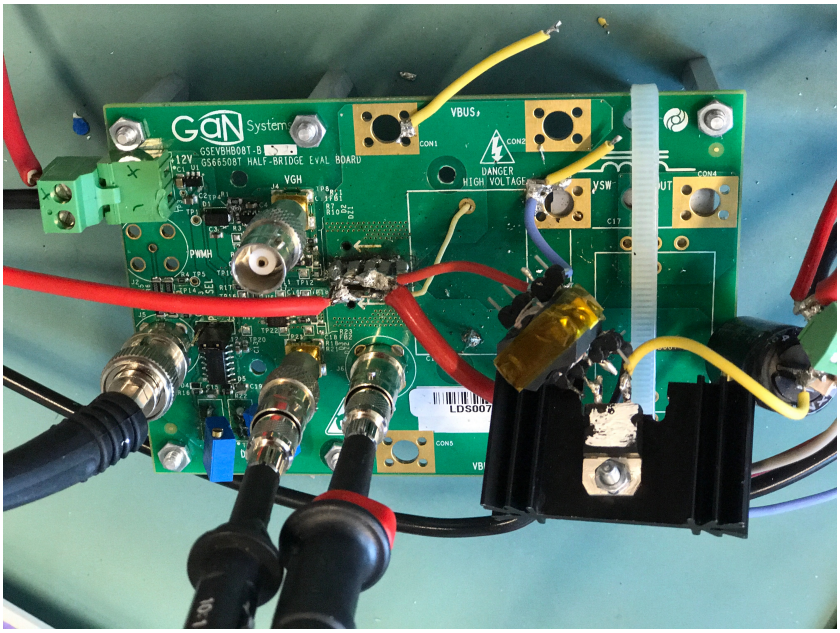

Figure 5.1: Basic set up for test

The list of equipment used in measurements:

Equipment	Brand and Type	Basic technical parameters
Oscilloscope	LeCroy Wavepro 940	500MHz
DC power supply (for test board)	Power supply ES 030-5	0-30V; 0-5A
DC power supply	Power Supply SM3004-D	0-300V ; 0-4A
Power analyzer	YOKOGAWA WT3000	
Signal Generator	Agilent B1104A	80MHz
Electric Load	Chroma 63100A	0.6A/2A; 100V/500V;100W

Table 5.1: List of experimental equipments

5.2. SYSTEM PARAMETERS OF DESIGNED CIRCUIT

The selected resonant period by L_r and C_{clm} is $1468ns$ ($681kHz$).So the Ton time of auxiliary switch $S2$ is $734ns$.

Input ac voltage range	$85V--265Vrms$ (Universal Line)
Output voltage	$75V$
Output Power	$50W$ Average
Maximum Switching frequency	$980kHz$
Magnetic inductance L_m	$26.66\mu H$
Resonant(Leakage) inductance L_r	$10.93\mu H$
Resonant capacitance C_{clm}	$5nF$
Output capacitance C_{out}	$220\mu F, 100V$

Table 5.2: System Parameters of designed circuit

5.3. VALIDATION METHOD

The scope of this project is focusing on investigate power factor correction of active clamp flyback converter. To achieve high efficiency and smaller size are the main targets of this project.The control method will be designed, but the implementation of closed control loop as shown in fig 5.2 is not included in this project.

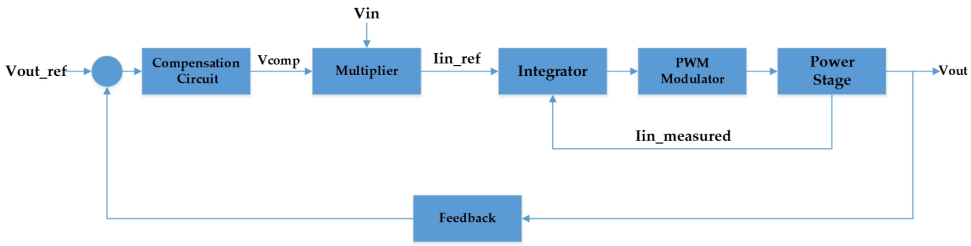

Figure 5.2: Closed Control Loop diagram for Power Factor Correction

In order to test the prototype, a number DC-DC points are chosen representing the line cycle.

As shown in fig 5.3 and fig5.4, 5 points are chosen from half a mains cycle. At each DC-DC operation point, the corresponding duty ratio and switching frequency will be get from simulation result. Those two data will be used to set the signal generator to create PWM signals directly to the low side and high side switch. Due to parasitic inductance/capacitance in real circuit and time delay within circuit, the duty ratio and switching frequency will be slightly adjusted to make sure that the output voltage could reach desired value.

The input current value will be record to check if its waveform over 50Hz could be in phase with input voltage and be sinusoidal. Meanwhile, the power loss on each point will be recorded.In order to have a more accurate average loss value over a 50Hz cycle,the

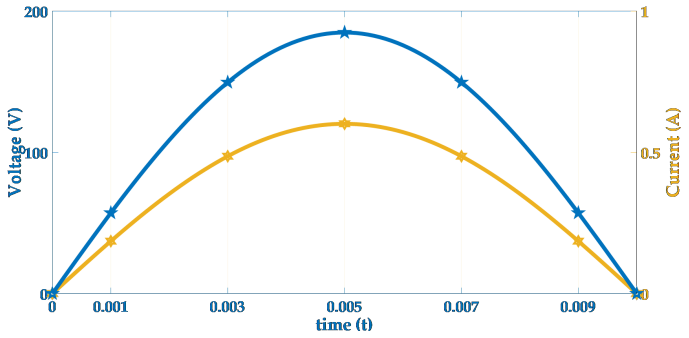

Figure 5.3: DC-DC test points on V and I waveform

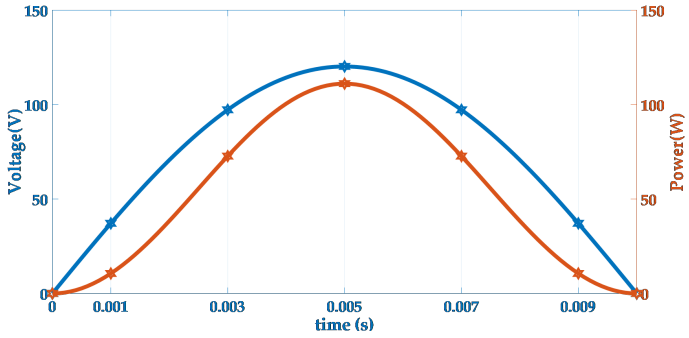

Figure 5.4: DC-DC test points on V and P waveform

loss on each operation point would be weighted by the corresponding switching period.

$$P_{loss_{ave}} = \frac{\sum T_{sw} * P_{loss}}{\sum T_{sw}}$$

Where:
$P_{loss_{ave}}$ is the average power loss over half a main cycle;
T_{sw} is the switching period at each DC-DC points;
P_{loss} is the power loss at each DC - DC points.

It should be noted that the load value is set not as usual. Generally, with a closed control loop, the load is simply set as a constant value.But here, in DC-DC points verification, the instantaneous output power is variant as input power. So the load value should be adjusted at different operation points.

$$R_{load} = \frac{V_{out}^2}{P_{out}}$$

Where:
V_{out} is the instantaneous output voltage;
P_{out} is the instantaneous output power.

5.4. THE INFLUENCE OF THE OUTPUT RECTIFIER

5.4.1. WAVEFORM

The output capacitance and reverse recovery charge on secondary side rectifier will have a significant influence on waveforms.

1. The reverse recovery charge of the diode

   The diode must have a very low reverse recovery charge, otherwise it will have significant effect of the waveform and operation.

   Here, in order to have a low forward voltage and low output capacitance on the diode, the body diode of the MOSFET – STD3NK60ZT4 is used as secondary side rectifier. But, the reverse recovery charge in this diode is relatively high – 948nC as shown in its datasheet [27].

   At this operation point, the switching frequency is 500 kHz but the reverse recovery time of this diode is 300ns. So the influence from the reverse recovery process is very significant, as shown in red box in Fig 5.5. The primary side and secondary side current wave shape is distorted.

   The peak of the reverse recovery current is even higher than forward current, the conduction loss of diode and transformer's winding loss will increase because of this current "dip". [22] With a high loss, the temperature of the diode will increase. Meanwhile, the minority charge concentration will increase with temperature. [5] So the situation will become worse and worse.

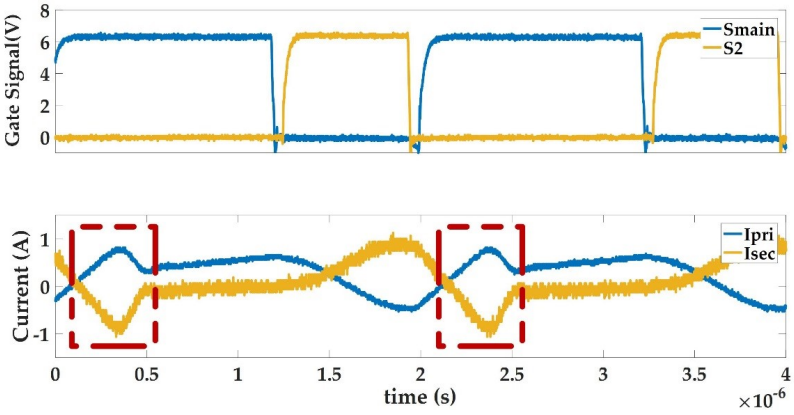

Figure 5.5: The current waveform using the body diode of a MOSFET (STD3NK60ZT4) as the output rectifier

2. The output capacitance of the diode

   The output capacitance of the secondary side rectifier will have a significant influence on waveforms. This capacitor will form a resonant circuit with the inductance on the primary side. So there will be oscillations superimposed to the ideal current and voltage waveforms.

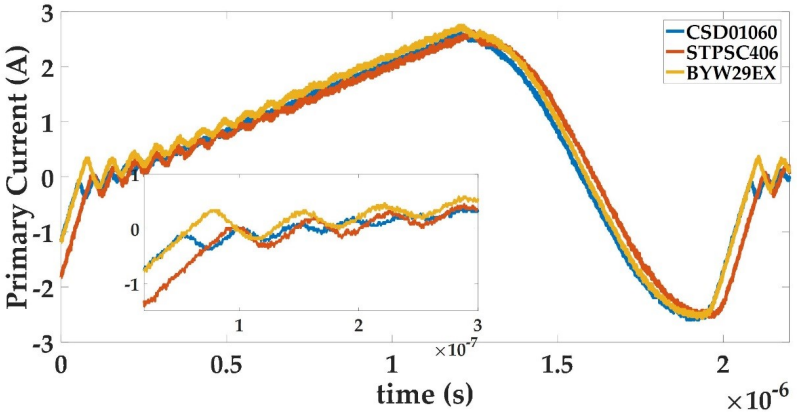

Figure 5.6: The influence of diode's output capacitance on primary current

Those three diodes are with very low recovery charge – 3.3nC, 3nC and 11nC respectively. So the reverse recovery charge as shown in previous section does not influence too much. Here, the output capacitance dominate the distortion on primary side current. As shown in fig5.6 and fig5.7, there are oscillations on both primary and secondary side current.

The oscillations on inductance current is from the resonant circuit formed by the

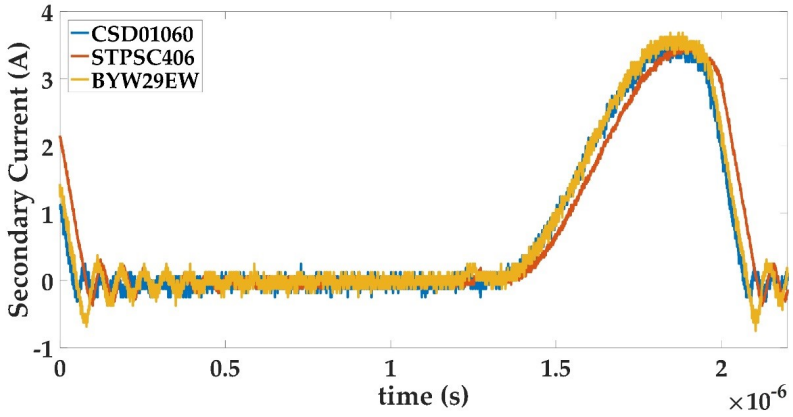

Figure 5.7: The influence of diode's output capacitance on secondary current

primary inductance and secondary side diode output capacitance. As shown in Fig5.6, the oscillation's period and amplitude are proportional to the size of the diode output capacitance.

5.4.2. TRANSFORMER LOSS

Due to this high frequency oscillation, the transformer's core loss and winding loss will increase. First, the oscillation's variation trend under different input and output level will be illustrated. The diode in the test circuit will remain the same and the operation point is the peak on the 50Hz cycle.
As shwon in Fig5.8 and fig5.9, the current oscillation on inductance current is proportional to the input voltage and output power. Those ripple are generated from the resonant circuit formed by primary inductance and diode output capacitance.

The current expression in a series resonant circuit is :

$$i_L(t) = I_{L0} * cos(\omega_0 * (t - t_0)) + \frac{(V_d - V_{c0})}{Z_0} * sin(\omega_0 * (t - t_0))$$

As expressed in the equation, two variables will domain the magnitude of resonant cur-

	Output capacitance	Oscillation frequency	Oscillation Magnitude
CSD01060–SiC Schottky 600V 2A	12pF[28]	21MHz	0.25A
STPSC406–SiC Schottky 600V 4A	25pF[29]	16.67MHz	0.4062A
BYW29EX–Ultrafast Diode 200V 8A	50pF[30]	13MHz	0.5312A

Table 5.3: List of experimental equipments

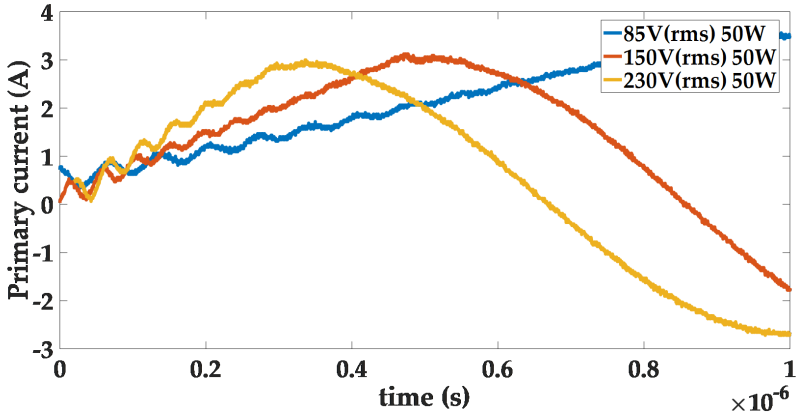

Figure 5.8: Comparison of current oscillation under different input voltage

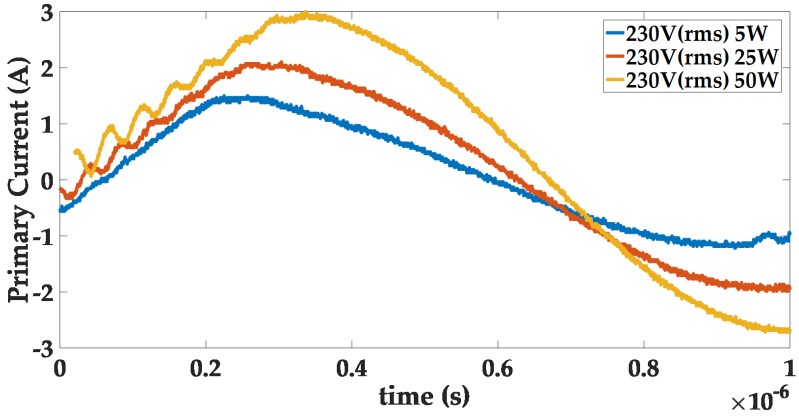

Figure 5.9: Comparison of current oscillation under different output load

rent – the initial value of inductance current and the input voltage.

When the output load power remains the same, but the input voltage changes, the difference of initial value of inductance current under different operation point is not so much, so, the input voltage will domain the magnitude of current oscillation. In the similar way, when the input voltage remains the same, but the output load changes, the initial value of inductance current will domain the magnitude of current oscillation, i.e. the output load power will domain.

Here, in order to invest how the output capacitance influences the transformer loss, a comparison experiment of transformer loss between two different diode is processed. Here CSD01060 [28] and STPSC406 [29] are chosen as candidates.

	Output capacitance	Forward voltage drop
CSD01060–SiC Schottky 600V 2A	12pF	1.6V
STPSC406–SiC Schottky 600V 4A	25pF	1.1V

Table 5.4: List of experimental diode basic data

In order to minimize the influence from the diode forward voltage and intensify the influence from the current oscillation, an operation point with high input voltage and low output power is chosen here – $V_{in} = 230V$, $P_{out} = 25W$.

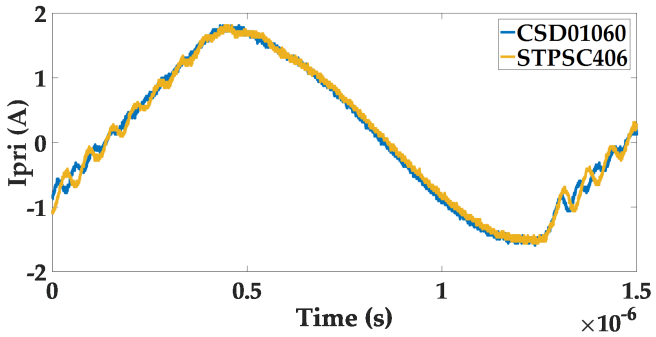

Figure 5.10: Comparison of primary current oscillation under different diode

As shown in table 5.5, the experimental result and simulation result are matching with each other. Because of the ringing on inductance current, the total transformer loss has 0.17W difference in simulation and 10°C temperature difference in experimental result.

With a larger output capacitance, the frequency of inductance current will decrease, but the amplitude of inductance current will increase.

1. Core Loss: With a larger amplitude oscillation, the voltage oscillation on magnetic

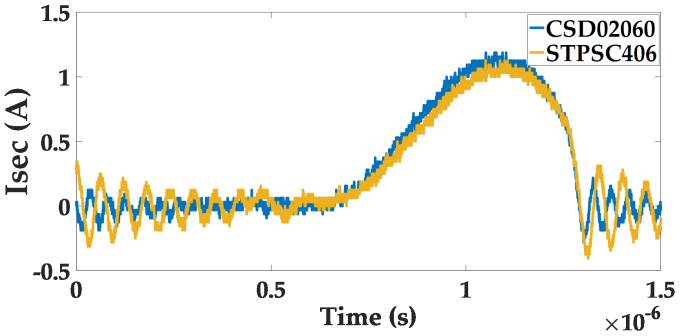

Figure 5.11: Comparison of secondary current oscillation under different diode

		CSD01060	STPSC406
Experiment result	Power loss	2.187W	2.334W
Experiment result	Efficiency	91.251%	90.664%
Temperature	Core	83.6°C	96°C
Temperature	Winding	73.5°C	83.4°C
Temperature	Diode	42.5°C	41°C
Simulation result	Core Loss	1.115W	1.326W
Simulation result	Winding Loss	0.387W	0.295W
Simulation result	Eddy Current	0.263W	0.312W
Simulation result	Total Transformer Loss	1.765W	1.933W
Calculate result	Diode Loss	0.4W	0.3667W

Table 5.5: Comparison of experimental results and magnetic component simulation results between two diodes (V_{in}=230V, P_{out}=25W)

inductance would also be larger.

$$P = V_{core} * k * f^{\alpha} * (\frac{B}{2})^{\beta} [5]$$

A larger voltage oscillation on magnetic inductance would cause a wider range of magnetic force at high frequency.A wider hysteresis loop at high frequency will cause a higher hysteresis loss. So the core loss will increase with larger current oscillation,i.e. higher input voltage, larger output capacitance or heavier load.[23][31][32]

2. Winding Loss:

$$P_{winding} = R_{DC} * i_{rms}^2 + R_{\omega_1} * i_{\omega_1}^2 + R_{\omega_2} * i_{\omega_2}^2 + R_{\omega_3} * i_{\omega_3}^2 + ... + + R_{\omega_n} * i_{\omega_n}^2$$

Where:
R_{DC} is the DC resistance of each winding;
i_{rms} is the RMS current value over one switching cycle on each side;
R_{ω_n} is the high frequency resistance of each winding;
i_{ω_n} is the high frequency component in inductance current.

The high frequency resistance of winding wire increases exponentially with frequency. With a lower switching frequency, even the current oscillation amplitude is higher,but the high frequency resistance decreases dramatically. So the winding loss at lower switching frequency, i.e. smaller output capacitance, will be less.

To sum up, the experimental result and simulation result are matched. Both of them show that a larger inductance current ripple would cause a higher transformer loss. Even though winding loss would be less, but that can not compensate the increase part of core loss and eddy current.

5.4.3. THE CHOICE OF SECONDARY RECTIFIER

- Schottky diode:

  The reverse recovery charge of Schottky diode is very low and its switching speed is much faster than other types. But the repetitive peak reverse voltage of Schottky diode is restricted. There are just a few commercial models which is upper than 400V. It should be noted that due to the other wide bandgap semiconductor material, SiC, the limit of break-down voltage of Schottky diode has been overcome. But one of the drawback of SiC Schottky diode is its high forward voltage. This will cause a higher conduction loss.[5]

- Standard-recovery diode

  They are intended for low switching frequency operation, i.e. 50Hz to 60Hz. The reverse recovery time of them is even higher than the switching period of this project. Also, standard recovery diode has very low output capacitance, but its reverse recovery parameters are not suitable in high switching frequency converter.[5]

- Ultra-fast recovery diode

  Its characteristic is between Schottky diode and standard recovery diode. It has a short reverse recovery time and low reverse recovery. Meanwhile, its output capacitance is low and forward voltage is acceptable. Due to The lower current rating, the lower output capacitance.

- Synchronous Rectifier

  In order to achieve lower conduction loss and less output capacitance effect, another transistor could be used as secondary side rectifier [13] [33]. But an extra signal and driving circuit needs to be applied to turn on/off this SR.

Based on the analysis of effect from secondary side, in order to achieve high efficiency and less current distortion of active clamp flyback converter, a diode with short reverse recovery time, low reverse recovery charge, low output capacitance and low forward voltage should be chosen here.

After comparing several between different types of diode, STPSC406 (600V Power Schottky silicon carbide diode) is applied in this project.

1. The voltage rating is higher than the maximum reverse voltage – 390V. Also it could stand for the voltage ringing due to resonant oscillation between primary inductance and diode output capacitance.

2. The reverse recovery charge is just 3nC.

3. The output capacitance at 100V is 30pF.

4. The forward voltage is less than 1.5V when the forward current is under 2A

This diode has a good balance of all the requirements, so the converter gives a better efficiency performance with it.

5.5. EFFICIENCY

The highest efficiency could get is 94% at 85Vrms input and full load.In the state of art Flyback converter in PFC application, the highest efficiency of CRM flyback converter is 89.5% [24][25]. Here if the power loss on rectifier bridge is included, the efficiency would be 92% for different input voltage level.

5.6. LOSS BREAKDOWN

The loss of this converter could be divided into several parts: **Transistor loss**; **Diode loss**; **Transformer Loss**; **Others**.

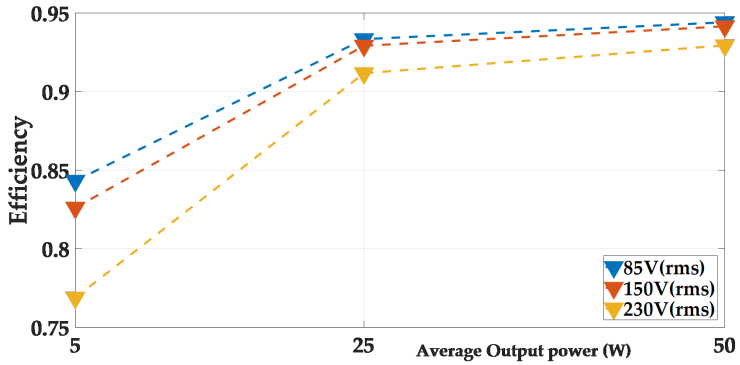

Figure 5.12: The Efficiency performance of the designed AC flyback converter

5.6.1. TRANSISTOR LOSS

SWITCHING LOSS

- Turn On Loss

  Because of the advantage of Active Clamp flyback converter, the Drain – Source voltage across the two transistor are fully discharged before the gate signal is on. So there is no switching ON loss of those two transistors.

- Turn Off Loss

  The turn off loss is assumed virtually zero here due to the low impedance gate drivers and low capacitances.

CONDUCTION LOSS

When the transistor is turned on, the on-state resistance $Rds(on)$ of GaN transistor is lower than $70m\Omega$[15]. So the conduction loss is much lower than Si mosfet.

$$P_{cond(HS)} = R_{ds(on)(HS)} * I^2_{rms(HS)}$$

$$P_{cond(LS)} = R_{ds(on)(LS)} * I^2_{rms(LS)}$$

Where:
$I_{rms(HS)}$ and $I_{rms(LS)}$ are the RMS current over one switching cycle through the high side and low side MOSFET, respectively.
$R_{ds(on)(HS)}$ and $R_{ds(on)(LS)}$ are the Drain to Source On resistance for the MOSFET on the high side and low side, respectively.

REVERSE CONDUCTION LOSS

GaN E_HEMT reverse conduction has a "diode" like characteristics.[26]

$$P_{reverse} = (V_{sd} * I_{sd} + R_{rev(on)} * I^2_{sd}) * t_{reverse} * f_{sw}$$

Where:
V_{sd} is the forward voltage drop cross the Drain to Source;
I_{sd} is the current through them when the transistor is reversed conducting.
$t_{reverse}$ is the time length when the transistor is reversed conducting during the dead-time stage.
f_{sw} is the switching frequency;
$R_{rev(on)}$ is the channel resistance.

5.6.2. DIODE LOSS

The conduction loss model of a diode is as following:

$$P_{cond} = V_f * I_{f_{ave}} + R_D * I_{f_{rms}}^2$$

Where:
P_{cond} is the diode conduction loss over one switching period;
V_f is the forward voltage drop when the diode is forward biased;
$I_{f_{ave}}$ is the forward average current;
R_D is the dynamic resistance;
$I_{f_{rms}}$ is the forward root mean square current flowing through the diode.

It should be noted that V_f and R_D are thermal dependent values. It will be not accurate to use this equation to estimate the loss in diode. Here a simple test is utilized to find out the relationship between temperature and loss in any specific diode.

Small test: Connect a DC current source with a diode, measure the voltage across the diode and the current through it. And record the diode temperature after it goes into thermal balance.

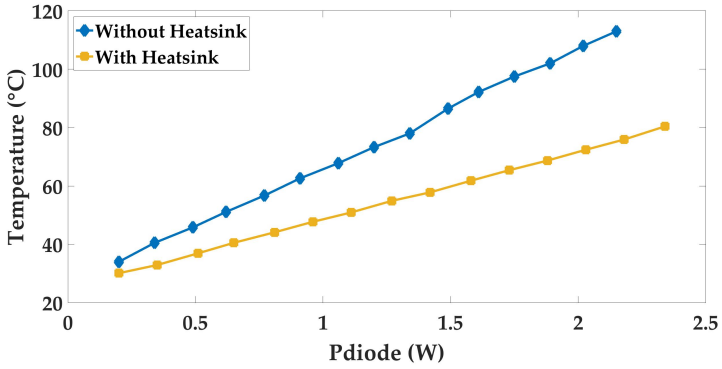

Figure 5.13: The relationship between diode loss and its temperature

5.6.3. TRANSFORMER LOSS

The estimation of transformer loss is based on a magnetic design software – Magtool.The analysis of transformer loss has been discussed in Section 4.3.2.

5.6.4. OTHERS

The clamp capacitor and output capacitor also have series resistance.And in real circuit, as the switching frequency is relatively high, the influence from parasitic capacitance and parasitic inductance are more obvious.Wire resistance will also introduce some loss.

5.6.5. TOTAL LOSS

The total loss breakdown is based on the same output load level and different input voltage level.Here three operation points are chosen – $V_{in} = 85V, P_{out} = 25W; V_{in} = 150V, P_{out} = 25W; V_{in} = 230V, P_{out} = 25W$.

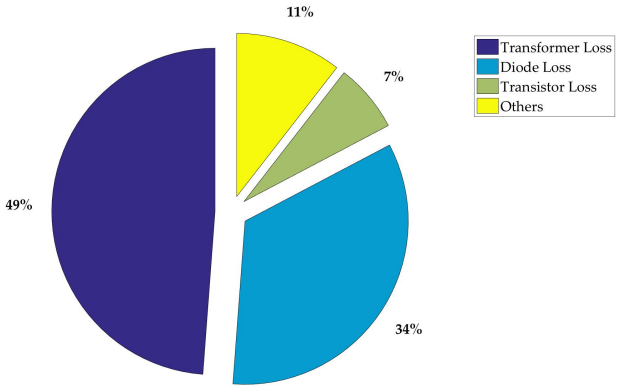

Figure 5.14: Loss Breakdown at 85Vrms

As shown in Fig5.14 – Fig 5.16, the proportion of transformer loss has a dramatic increase.The reason is when the input voltage level increases, the oscillation on inductance current would also increase. As analysis in 5.4.2, the transformer loss will increase with a higher input voltage.

5.7. ZVS

Based on the experimental validation, the zero voltage switching could be achieved in operation points within this range: Input RMS voltage range: 85V - 230V; Average output power range: 5W – 50W.

Those figures 5.17 - 5.22 show the drain – source voltages of the two transistors when the corresponding gate signal go to positive. The operation points are chosen at the peak of each 50Hz voltage cycle. Because at the peak point, the drain – source voltage stress is

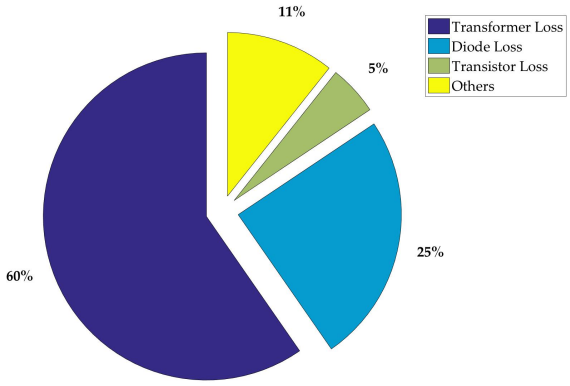

Figure 5.15: Loss Breakdown at 150Vrms

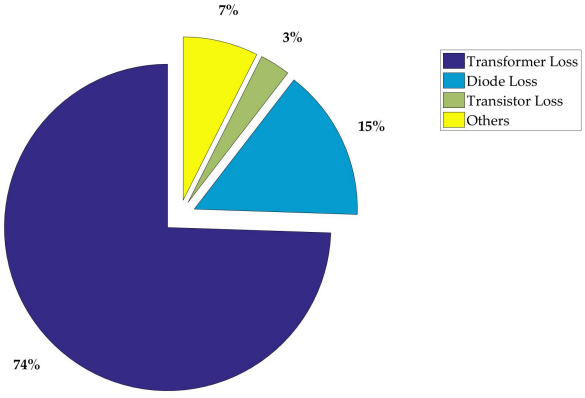

Figure 5.16: Loss Breakdown at 230Vrms

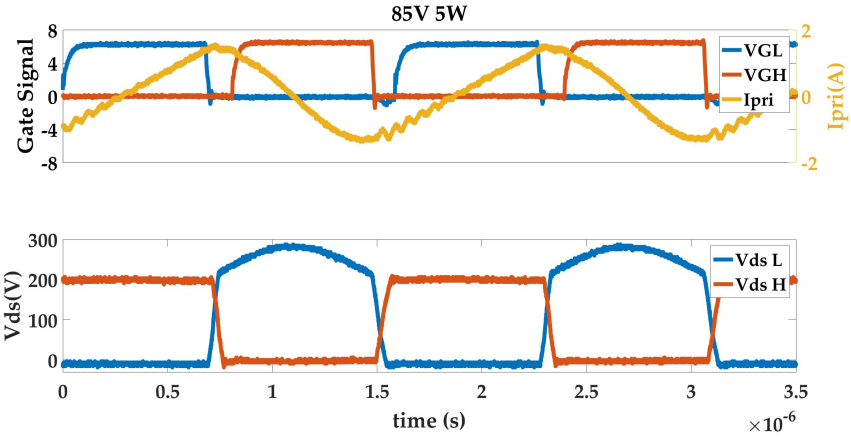

Figure 5.17: The peak of Vin_{rms}=85V and $Pout_{ave}$ = 5W

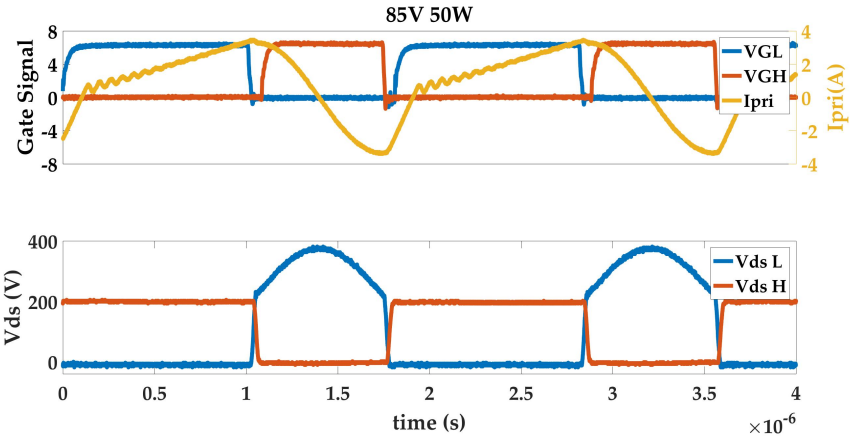

Figure 5.18: The peak of Vin_{rms}=85V and $Pout_{ave}$ = 50W

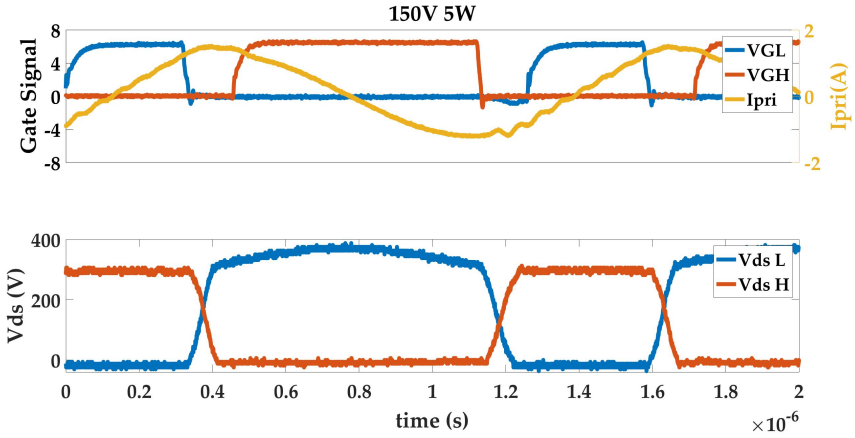

Figure 5.19: The peak of Vin_{rms}=150V and $Pout_{ave}$ = 5W

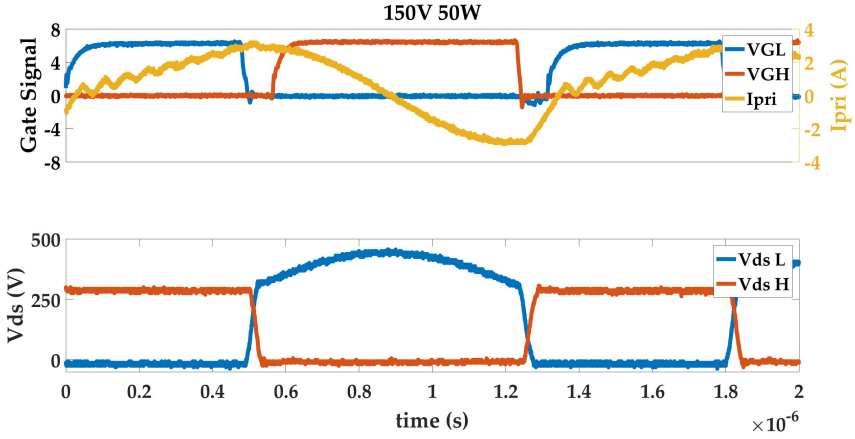

Figure 5.20: The peak of Vin_{rms}=150V and $Pout_{ave}$ = 50W

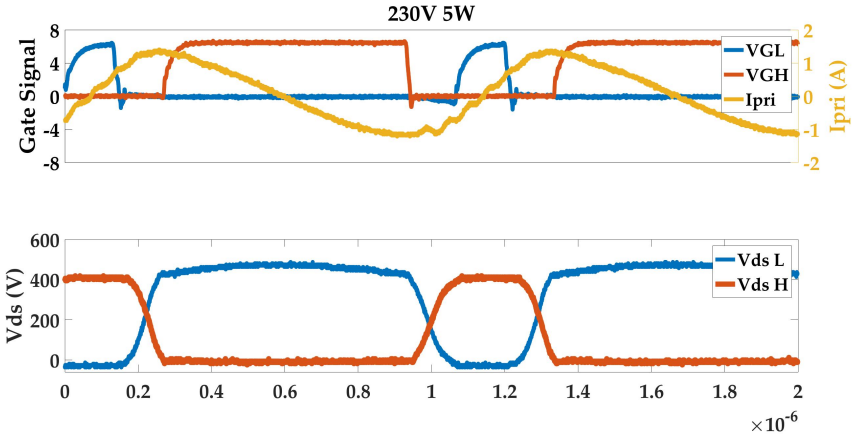

Figure 5.21: The peak of Vin_{rms}=230V and $Pout_{ave}$ = 5W

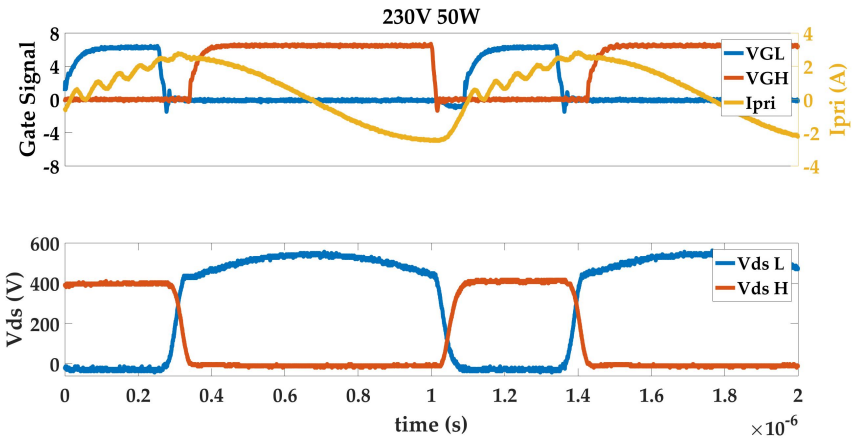

Figure 5.22: The peak of Vin_{rms}=230V and $Pout_{ave}$ = 50W

maximum. It is the worst case to achieve fully discharging.

For the average output power under 5W part, the required input current is relatively low. So the energy stored in both resonant inductance and magnetic inductance may not be enough to fully discharging the output capacitance. But the output voltage would be also decreased. Meanwhile, the current through the transistor is very low due to the low output power. So the switching loss at those operation points are acceptable.

If the ZVS needs to be achieved at very light average output power, the value of resonant inductance needs to be further increased. The gap between primary winding and secondary wingding will be increased. But the window of the present transformer is full. In order to meet both the requirement of enough magnetic inductance and enough gap, a bigger size core will be used.

5.8. CONCLUSION

According to experimental result, the output capacitance and reverse recovery charge on secondary side rectifier will have a significant influence on waveform and transformer loss. Here, a SiC diode has been employed to minimize those influence.At present, the efficiency achieved at full load and the minimum AC voltage (85Vrms) is 94.4% excluding the loss of the input rectifier and EMI filter.The zero voltage switching of the two transistors are achieved at different operation points.

6

CONCLUSION AND FUTURE WORK

6.1. CONCLUSION

IN this project, the active clamp flyback converter has been analysed and designed targeting 50W front end stage for am LED driver that covers a universal mains input and renders a high power factor. A demonstrator has been built that shows zero voltage under all relevant line and load conditions.

Using e-mode GaN switches, the highest switching frequency in the converter reaches $980kHz$ and the transformer's size has been minimized to a volume of less than 1/6 compared to an optimized state-of-the-art flyback PFC converter. The active clamp limits the drain-to-source voltage of the transistors to below the maximum device rating of 650V at the peak mains voltage (265Vac). As output rectifier a SiC diode has been employed to minimize the parasitic capacitance of the output. At present, the efficiency achieved at full load and the minimum AC voltage (85Vrms) is 94.4% excluding the loss of the input rectifier and EMI filter. The estimated efficiency of the complete front end is therefore about 92% under all line conditions at full load, which is well above conventional PFC flyback converters.

(A specific control method, dead time and conduction mode are decribed for the active clamp flyback converter as PFC.)

6.2. FUTURE WORK

The performance of this converter strongle depends on the on the type of output rectifier.

The secondary side diode could be replaced by a synchronous rectifier to solve the high forward voltage drawback of the present SiC schottky diode. So the power efficiency could be increased further.

But the control of this SR should be carefully designed. Because the forward bias of secondary side rectifier is determined by the voltage of the clamping capacitor. The turning ON/OFF time of the rectifier would also depend on the operation point. In addition, the output capacitance of such SR has to be minimized as well.

1. At present, the dead time is set based on input rms voltage and output average power. At some operation points, this is still much longer than needed. So the dead time could be further optimized. This would help to decrease the reverse conduction loss in transistor and further increase efficiency.

2. As analyzed in section 4.4.2, the inductance current oscillation would introduce more loss on transformer, so the temperature increase on transformer is higher than expected. At low line input and heavy load condition, the temperature would go up to $100°C$. The transformer design should be optimized.

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