A 14-b BW /Power Scalable Sensor Interface with a Dynamic Bandgap Reference

Tang, Zhong; Liu, Yuyan; Chen, Pengpeng; Wang, Haining; Yu, Xiao Peng; Makinwa, Kofi A.A.; Tan, Nick Nianxiong

DOI
10.1109/JSSC.2024.3471820

Publication date
2024

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A 14-b BW /Power Scalable Sensor Interface With a Dynamic Bandgap Reference

Zhong Tang, *Member, IEEE*, Yuyan Liu, *Member, IEEE*, Pengpeng Chen, Haining Wang, Xiao-Peng Yu, *Member, IEEE*, Kofi A. A. Makinwa, *Fellow, IEEE*, and Nick Nianxiong Tan, *Senior Member, IEEE*

***Abstract*— This article presents a 14-bit fully dynamic sensor interface that consists of a switched-capacitor (SC) ΔΣ modulator and a dynamic bandgap reference (BGR). The BGR is implemented by summing the proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) outputs of two PNP-based capacitive DACs. At the sampling rate, the DAC capacitors are pre-charged to the supply and then discharged for a fixed period via PNPs, thus biasing them and simultaneously sampling their base–emitter voltages. By using the modulator's first integrator to sum the DAC outputs, a dynamic BGR can be realized, which does not need additional reference buffers or decoupling capacitors. To make the system fully dynamic, the modulator itself is based on capacitively biased (CB) floating inverter amplifiers (FIAs). Implemented in a standard 130-nm CMOS process, the sensor interface occupies an area of 0.2 mm^2. It achieves an SNDR of >84.5 dB over a scalable bandwidth (BW) ranging from 98 Hz to 5.9 kHz while consuming 1.7–50.8 μW. Furthermore, by employing a time-domain temperature-compensation scheme, it achieves a batch-trimmed gain error of ±0.26% from −40 °C to 125 °C.**

***Index Terms*— ΔΣ ADC, analog-to-digital converter, bandgap reference (BGR), capacitively biased (CB) BJT, floating inverter amplifier (FIA), poly-phase filter (PPF).**

I. Introduction

IoT applications employ a wide range of sensors. To accommodate different use cases, the bandwidth (BW) and power dissipation of the associated sensor interfaces should be scalable. For example, in battery management applications, Coulomb counting is often used to estimate the battery state of charge. This requires always-on current sensors with low BW, high resolution, and microwatt power consumption for extended battery life [1]. On the other hand, the ac impedance measurements used to monitor battery state of health require current sensors with much wider BW but less demanding power requirements [2]. There is, thus, a need for high-resolution sensor interfaces that are BW/power scalable.

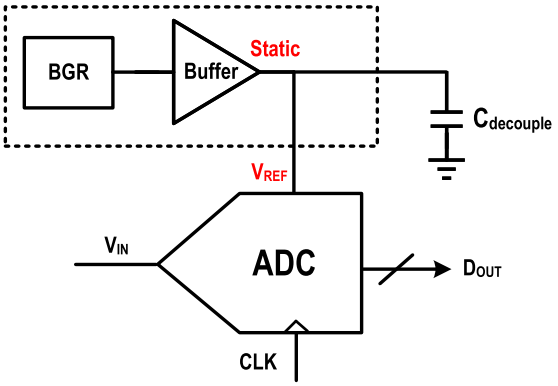

Fig. 1. Block diagram of the conventional ADC with an external reference and reference buffer.

Since they are key components, the ADCs used in such interfaces should themselves be BW/power scalable. Although successive-approximation-register (SAR) ADCs can be easily scaled by changing their sampling frequencies, they typically only have a moderate resolution (<14 bits) [3]. High-resolution BW/power scalable ΔΣ ADCs have also been reported [4], [5]. However, as shown in Fig. 1, such ADCs typically employ external bandgap references (BGRs), which then require power-hungry reference buffers and/or large decoupling capacitors.

Conventional BGRs are based on BJTs biased at fixed currents to generate proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) signals, which can then be combined to generate a temperature-independent output [6]. To achieve a low-temperature coefficient (TC < 20 ppm/°C), they typically consume tens of microwatts of static power [6], [7]. Although nanowatt BGRs have been reported, they typically have larger TCs (>20 ppm/°C) and limited driving capacity [8], [9].

To achieve both low power dissipation and good accuracy, dynamic BGRs based on the capacitively biased (CB) "diode" technique have been proposed [10]. This involves discharging a pre-charged capacitor across a diode for a fixed period and then sampling the resulting voltage. By combining the outputs of a number of CB diodes, a bandgap voltage can be generated. Although this approach only consumes dynamic power, it also has limited driving capacity because the output voltage is stored on a capacitor. To drive an ADC, a reference buffer is

Received 12 May 2024; revised 17 July 2024; accepted 24 September 2024. Date of publication 11 October 2024; date of current version 25 November 2024. This work was supported by the National Key Research and Development Program of China under Grant 2023YFB4405000. This article was approved by Associate Editor Drew Hall. *(Zhong Tang and Yuyan Liu contributed equally to this work.) (Corresponding author: Zhong Tang.)*

Zhong Tang, Yuyan Liu, Haining Wang, and Nick Nianxiong Tan are with Vango Technologies, Inc., Hangzhou 310053, China (e-mail: tangzhong@vangotech.com).

Pengpeng Chen was with Vango Technologies, Inc., Hangzhou 310053, China. He is now with Shaoxing Devechip Microelectronics Company Ltd., Hangzhou 310051, China.

Xiao-Peng Yu is with the School of Integrated Circuits, Zhejiang University, Hangzhou 310027, China (e-mail: yuxiaopeng@zju.edu.cn).

Kofi A. A. Makinwa is with the Electronic Instrumentation Laboratory, Microelectronics Department, Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS), Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: k.a.a.makinwa@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2024.3471820.

Digital Object Identifier 10.1109/JSSC.2024.3471820

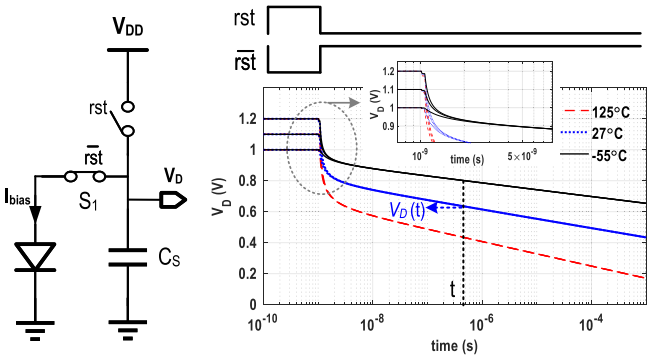

Fig. 2. Operating principle of the CBD structure.

required, which will then consume static power. In both cases, either the BGRs or the reference buffers will limit the power scalability of the overall system. Moreover, to supply dynamic currents and filter noise, external decoupling capacitors are often needed, thus increasing the system's bill of materials [3].

In this article, which is an extended version of [11], the design of a fully dynamic sensor interface with a dynamic BGR and ADC is presented. The BGR is realized by using the first integrator of a switched-capacitor (SC) $\Delta\Sigma$ modulator to sum the outputs of a number of CB PNPs, thus avoiding the need for extra reference buffers. The modulator itself is based on CB floating inverter amplifiers (FIAs). As a result, the sensor interface is fully dynamic and achieves an SNDR of greater than 84.5 dB over a scalable BW ranging from 98 Hz to 5.9 kHz while consuming 1.7–50.8 μW. Furthermore, by employing a time-domain temperature-compensation scheme, it achieves a batch-trimmed gain error of $\pm 0.26\%$ from -40 °C to 125 °C.

The rest of this article is organized as follows. Section II describes the proposed dynamic BGR and how it can be merged with the first integrator of an SC $\Delta\Sigma$ modulator. A detailed circuit implementation of the sensor interface is then described in Section III. In Section IV, the measurement results of the sensor interface are presented and compared to the state-of-the-art. Finally, conclusions are drawn.

II. Proposed Dynamic BGR

In this section, the detailed design of the proposed dynamic BGR is presented.

A. CB Diode

As shown in Fig. 2, the CB "diode" technique involves pre-charging a capacitor C_S to the supply voltage V_{DD} and then discharging it via a diode. After a short time (tens of nanoseconds), the voltage V_D on C_S will be fully determined by the diode's I/V characteristic and will be a supply-independent logarithmic function of time [12]. For a certain discharge time t, the diode's bias current I_{bias} is given by

$$I_{bias} \propto \frac{kT}{q} \cdot \frac{C_S}{t} \tag{1}$$

where k is Boltzmann's constant, T is the absolute temperature, q is the charge of an electron, and C_S is the sampling capacitor in Fig. 2. If the discharge time t is constant, the resulting V_D will be CTAT. A PTAT voltage ΔV_D can then be generated by subtracting the outputs of two CB diodes operated at different current densities, which can be done by adjusting either the discharge time or the area ratio of the two diodes. As in [13], the diode can also be replaced by a diode-connected BJT.

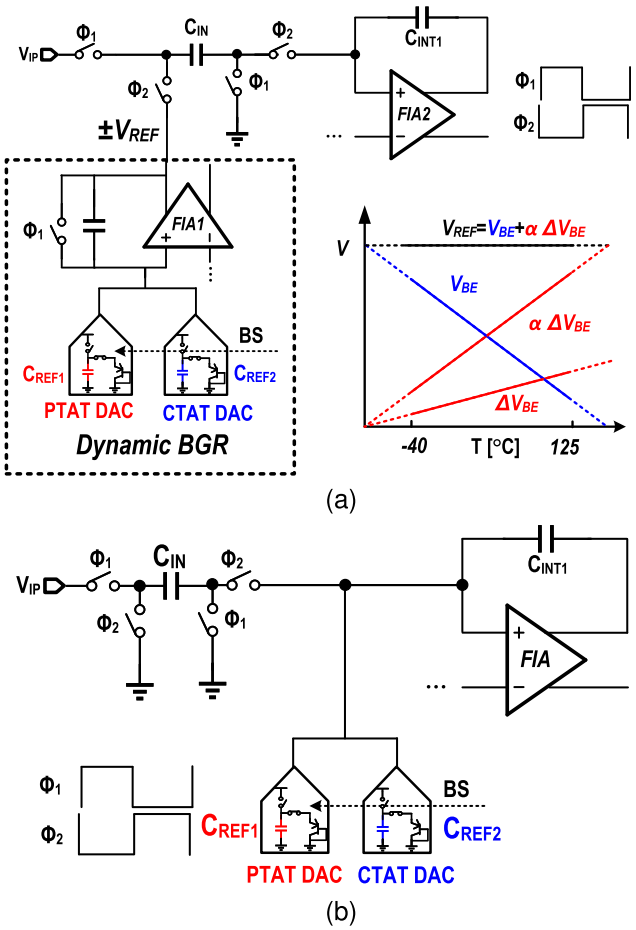

Fig. 3. (a) Separate dynamic BGR and SC integrator. (b) Embedded dynamic BGR in an SC integrator.

B. Dynamic BGR in an SC Integrator

Fig. 3(a) shows one way of combining a fully dynamic BGR with an SC $\Delta\Sigma$ modulator. The outputs of two CB-PNP-based PTAT and CTAT DACs can be summed by an SC amplifier, generating an output voltage V_{REF}

$$V_{REF} \propto V_{BE} + \alpha \Delta V_{BE} \tag{2}$$

where $\alpha = C_{REF1}/C_{REF2}$. To the first order, the TC of the resulting reference voltage V_{REF} can be balanced by choosing an appropriate DAC capacitance ratio α. Controlled by the feedback bitstream (BS), the output of the amplifier can then be used to drive the sampling capacitor of the SC $\Delta\Sigma$ modulator with the proper polarity. To achieve fully dynamic operation, the amplifiers can be implemented by FIAs. In this approach, the amplifier in the BGR must have low offset and high gain to make V_{REF} accurate, which increases design complexity.

Alternatively, the outputs of the PTAT and CTAT DACs can be directly summed by dumping the charge on their sampling

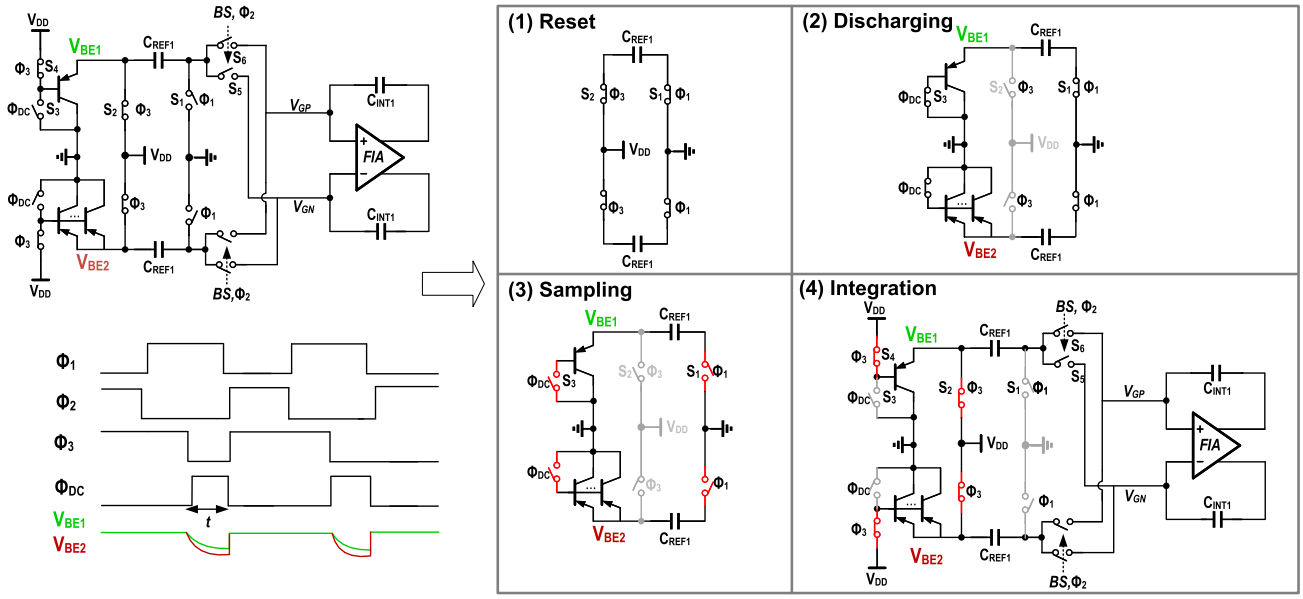

Fig. 4. Block and timing diagrams of the PTAT DAC.

capacitors into the virtual ground of the $\Delta\Sigma$ modulator's SC integrator, as shown in Fig. 3(b) [14], [15]. Compared to Fig. 3(a), this approach only requires one amplifier, resulting in a smaller area and higher accuracy.

C. PTAT and CTAT DACs

Fig. 4 shows the block and timing diagrams of the PTAT DAC and how it is combined with the SC integrator. At the start of the sampling phase Φ_1 (Reset), the capacitors C_{REF1} are pre-charged to V_{DD} by closing the $S_{1,2}$ switches. During the discharging phase Φ_{DC}, they are separately discharged through two diode-connected PNPs with a fixed area ratio p by turning off the S_2 switches and turning on the S_3 switches. Compared to the use of a time ratio [10], [13], [15], the use of an area ratio to define ΔV_{BE} allows the same timing control signals to be used for all the CB PNPs, thus simplifying the on-chip timing generation logic. At the end of Φ_{DC}, ΔV_{BE} ($=V_{\mathrm{BE1}} - V_{\mathrm{BE2}}$) is sampled by turning off the $S_{1,3}$ switches.

During the succeeding integration phase Φ_2, the PNPs are completely off by connecting their bases to V_{DD}. Simultaneously, the left plates of C_{REF1} are connected to V_{DD} via the S_2 switches, thus transferring a differential charge proportional to ΔV_{BE} to the SC integrator. The associated common-mode charge shifts the common-mode voltage (V_{CM}) of the integrator's virtual ground from zero to V_{DD}-V_{BE}. With the standard 1.2-V supply of the target 130-nm CMOS, V_{DD}-V_{BE} is close to $V_{\mathrm{DD}}/2$, which can be readily handled by the integrator's FIA.

The block diagram of the CTAT DAC is shown in Fig. 5. Here, V_{BE} is generated in one branch, while the other branch samples ground, thus generating a differential charge proportional to V_{BE}. As in the PTAT DAC, this charge is also transferred to the SC integrator during the integration phase Φ_2. Depending on the BS state, the $S_{5,6}$ switches transfer the outputs of the PTAT and CTAT DACs to the integrator with the appropriate polarity.

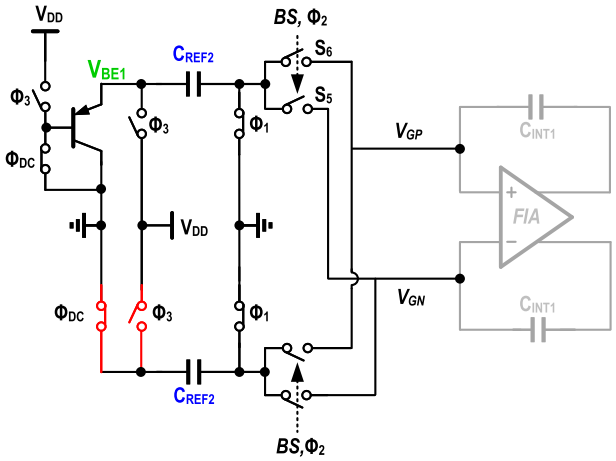

Fig. 5. Block diagram of the CTAT DAC.

D. Time-Domain Temperature Compensation

To realize a temperature-independent bandgap voltage V_{REF}, the TCs of the PTAT and CTAT DACs must cancel each other out exactly. To first order, this is achieved by setting the BJT's emitter area ratio p (=15) and the capacitor ratio α ($=C_{\mathrm{REF1}}/C_{\mathrm{REF2}} = 8$, with $C_{\mathrm{REF1}} = 6.4$ pF and $C_{\mathrm{REF2}} = 0.8$ pF). These choices facilitate the use of common-centroid layouts for good matching. To mitigate the effect of process spread, however, the TC of V_{REF} should be tunable. Doing this in the analog domain, e.g., by trimming the sampling capacitors, would require extra switches, whose on-resistance would then cause errors in the sampled voltages. In this work, a time-domain compensation scheme is proposed.

From (1), adjusting the discharge time t (the pulsewidth of Φ_{DC} in Fig. 4) will change the bias current of the BJTs, thus changing their emitter-base voltage V_{BE} according to

$$V_{\mathrm{BE}} = \frac{kT}{q} \cdot \ln \frac{I_{\mathrm{bias}}}{I_{\mathrm{S}}}. \tag{3}$$

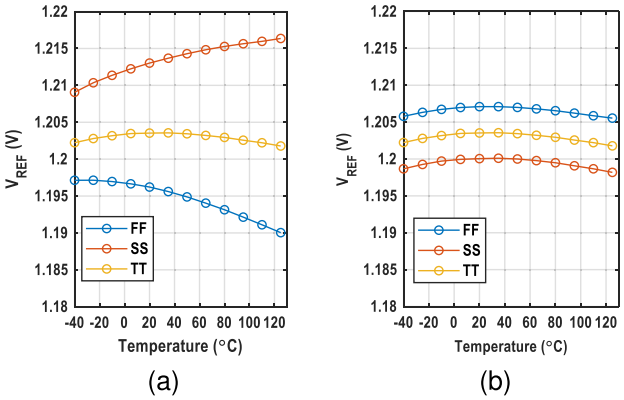

Fig. 6. (a) Simulated V_{REF} at different temperatures and corners without trimming. (b) Simulated V_{REF} at different temperatures and corners after batch calibration (t is 200 ns at the TT corner, 140 ns at the FF corner, and 300 ns at the SS corner).

Note that adjusting the discharge time will have a negligible effect on ΔV_{BE} since this is mainly determined by the BJT's emitter area ratio. The same discharge time can then be used in both the PTAT and CTAT CDACs. In this work, instead of setting this time with an external sampling clock [10], [13], [15], an on-chip RC delay generator is used. This ensures that the bias currents of the BJTs and the resulting V_{REF} do not depend on the ADC's scalable sampling clock. Moreover, the logarithmic relationship between I_{bias} and V_{BE} makes the BGR insensitive to PVT variations in the RC delay. From simulations, the BGR can be tuned in steps of 1 mV (~0.1%) by tuning the discharge time in steps of 5 ns (~2.5%) around a nominal value of 200 ns.

E. Simulated Results

Fig. 6(a) shows simulations of the ideally summed outputs of the PTAT and CTAT DACs over corners and over temperature. The simulated V_{REF} has a TC of 9 ppm/°C at the TT corner, increasing to 36 ppm/°C at the FF and SS corners without trimming. This corresponds to an absolute inaccuracy of about 2.2%. Adjusting the discharge time reduces the TC to less than 10 ppm/°C over corners [see Fig. 6(b)]. The residual error (~0.7%) in the nominal value can then be mitigated by digitally trimming the ADC's gain.

Fig. 7 shows the simulated V_{REF} at different supply voltages. Thanks to the intrinsic supply rejection of the CBD technique, the V_{REF} variation is less than 0.06% as the supply changes from 1.1 to 1.4 V, corresponding to a supply sensitivity of 0.2%/V.

F. Noise Analysis

Similar to other SC circuitry, the proposed dynamic BGR suffers from kT/C noise. Since the on-resistance of the various switches is much smaller than the impendence of the BJTs, the BJTs are the major noise contributors during the discharging phase Φ_{DC}. In addition, since their bias currents are quite small (nAs) at the sampling moment, their short noise is much higher than the thermal noise contributed by their base resistances. Therefore, the noise power spectral density (PSD) expression

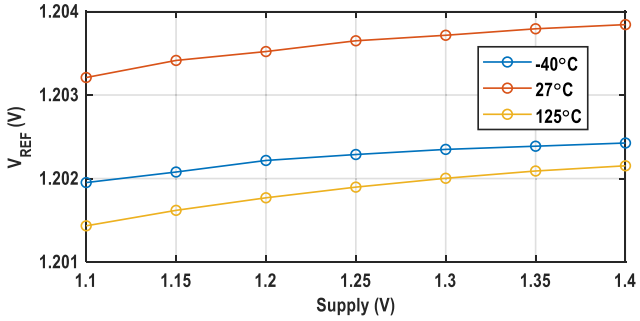

Fig. 7. Simulated V_{REF} when the supply changes from 1.1 to 1.4 V over temperature.

$S(f)$ of the output voltage V_{BE} can be simplified as follows:

$$S(f) = \frac{I_{n,c}^2}{g_m^2} = \frac{2kT}{g_m} \tag{4}$$

where $I_{n,c}^2$ ($=2qI_c$) is the BJT's shot noise density and g_m ($=qI_c/kT$) is the BJT's transconductance. The noise power of $V_{BE1,2}$ is then

$$v_{n,BE}^2 = \frac{2kT}{g_m} B_n = \frac{kT}{2C_{REF1,2}} \tag{5}$$

where B_n is the noise BW. In the differential implementation, the noise power in the PTAT DAC is given as

$$v_{n,\Delta BE}^2 = \frac{kT}{C_{REF1}}. \tag{6}$$

In the CTAT DAC, since one branch samples ground during the sampling phase, its noise is the same as that of a conventional SC circuit. Therefore, the noise power in the differential CTAT DAC is

$$v_{n,BE}^2 = \frac{kT}{2C_{REF2}} + \frac{kT}{C_{REF2}} = \frac{3kT}{2C_{REF2}}. \tag{7}$$

Including the input sampling noise, the total noise charge of the SC integrator during the sampling phase is expressed as follows:

$$q_n^2 = 2kTC_{IN} + kTC_{REF1} + \frac{3}{2}kTC_{REF2}. \tag{8}$$

The input referred noise power in the sampling phase is

$$v_{n,in}^2 = \frac{2kT}{C_{IN}}\left(1 + \frac{C_{REF1}}{2C_{IN}} + \frac{3C_{REF2}}{4C_{IN}}\right). \tag{9}$$

To achieve an input swing around ±1.2 V, the input capacitor C_{IN} (=0.64 pF in this work) is about the same size as C_{REF2} and is much smaller than C_{REF1}. Therefore, compared to a single $\Delta\Sigma$ modulator, the presence of the PTAT and CTAT DACs results in a noise penalty. In other words, there is a tradeoff between power/BW scalability and energy efficiency. A similar noise penalty also occurs in the architecture in Fig. 3(a), in which a separate dynamic BGR is realized. However, the proposed combination of an SC integrator with an embedded BGR is much simpler.

III. Circuit Implementation

The circuit design of the proposed dynamic BGR and the SC $\Delta\Sigma$ modulator is presented in this section.

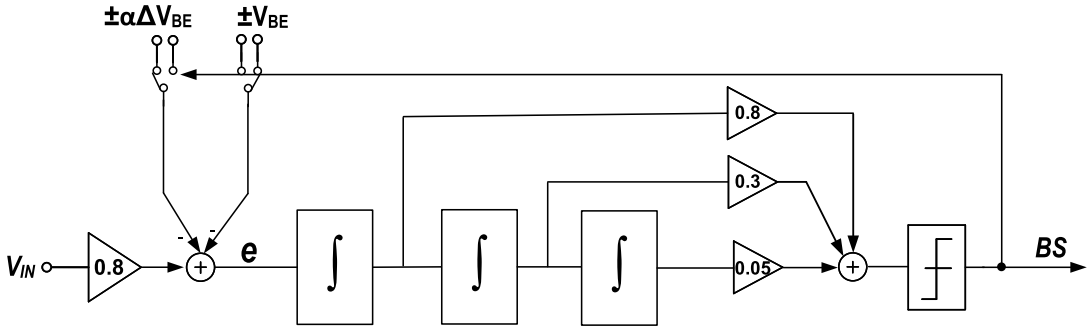

Fig. 8. Block diagram of the 1-bit third-order ΔΣ modulator.

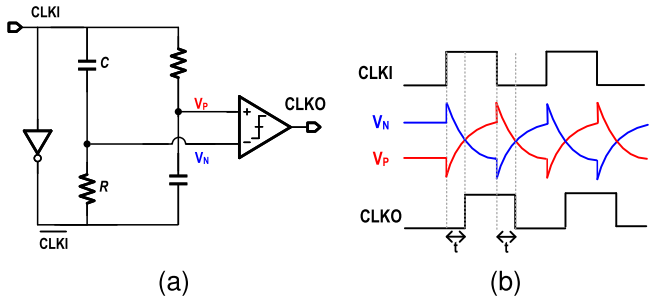

Fig. 9. (a) Delay generator based on the conventional *RC* PPF. (b) Timing diagram of the conventional *RC* PPF.

A. 1-Bit Third-Order ΔΣ Modulator

As shown in Fig. 8, the sensor interface in this work employs a 1-bit third-order SC ΔΣ modulator with a feed-forward topology. The choice of a 1-bit DAC minimizes the number of switches in the CB PNP pairs, thus maximizing their accuracy. As shown in the timing diagram of Fig. 4, the minimum period of the ΔΣ cycle must be larger than the required discharge time t (∼200 ns). This limits the maximum sampling frequency F_S of the ΔΣ modulator to about 1.5 MHz. With a third-order loop filter and an oversampling ratio (OSR) of 128, its BW can be scaled up to 5.9 kHz and its SQNR is about 100 dB, which are both sufficient for many sensors used in IoT applications.

B. On-Chip RC Delay Generator

As discussed in Section II-C, the discharge time t is set by an on-chip delay generator. This can be implemented by detecting the zero-crossing of an *RC* poly-phase filter (PPF), as shown in Fig. 9(a) [16], [17]. The PPF is driven by anti-phase clocks CLKI and $\overline{\text{CLKI}}$. As shown in Fig. 9(b), a comparator is then used to detect when its *RC* delayed outputs V_P and V_N cross, which defines the delay t. Due to the PPF's differential structure, t is supply-independent. However, the fact that V_P and V_N periodically exceed the supply rails poses reliability issues for the input pair of the comparator.

To solve this issue, a modified *RC* PPF is proposed in this work. As shown in Fig. 10(a), two extra capacitors C_2 ($=C_1 = 500$ fF) are added in parallel with the resistors. These capacitors limit the output swing of the PPF and prevent the occurrence of beyond-the-rail spikes. This allows the input pair of the comparator to be implemented by core devices without any reliability issues.

In this work, to achieve fully dynamic operation, an inverter-based comparator with a latched output is employed, as shown in Fig. 10(a) (right). The delay of the comparator should be minimized to ensure that t is defined by the *RC* PPF. Due to its inverter, the comparator's supply current peaks when its inputs V_P and V_N are close to $V_{DD}/2$, which reduces its switching delay (<5 ns), at the expense of power dissipation. To reduce power, an extra pair of reset switches are used to pull V_P/V_N up/down to V_{DD}/ground, respectively, shortly after the comparator switches. This quickly reduces the supply current after an output transition. Moreover, since the comparator is not used when CLKI is low, V_P and V_N are directly tied to ground or V_{DD} in this state. This further reduces the comparator's dynamic power consumption and ensures that the initial voltages of the next cycle, and thus the *RC* delay, are independent of the input clock frequency. The p-poly resistors R (190 kΩ) are 6-bit tunable to adjust t from 100 to 350 ns in steps of 5 ns. This compensates for *RC* spread and also fine-tunes the BGR's TC.

Fig. 11 shows the simulated delay time t at different supply voltages and temperatures after normalization. Thanks to the differential structure, the variation of t is less than ±2% when the supply changes from 1.1 to 1.4 V, corresponding to a V_{REF} error of less than ±0.1%. Due to the negative TC of the p-poly resistor, t decreases over temperatures. Thanks to the logarithmic relationship between I_{bias} and V_{BE}, this ±5% temperature dependence only has a small systematic impact on the curvature of V_{REF}.

C. Cascoded FIAs

To achieve BW/power scalability, all the integrators are based on FIAs [18]. As shown in Fig. 12, during the sampling phase Φ_1, a reservoir capacitor C_{RES} is pre-charged to the supply voltage V_{DD}. In the amplification phase Φ_2, the differential inverter is powered by the reservoir capacitor C_{RES}, and differential charges are transferred to the load capacitors. Thanks to the floating reservoir capacitor C_{RES}, only a differential path exists for the currents to flow in or out from C_{RES}. Therefore, the FIA provides excellent common-mode rejection without any common-mode feedback (CMFB) circuitry [18]. To suppress the offset of the following stages, a cascoded FIA with a dc gain >60 dB is employed. To simplify the bias network, the input pair is implemented with IO devices, while the cascode transistors are core devices

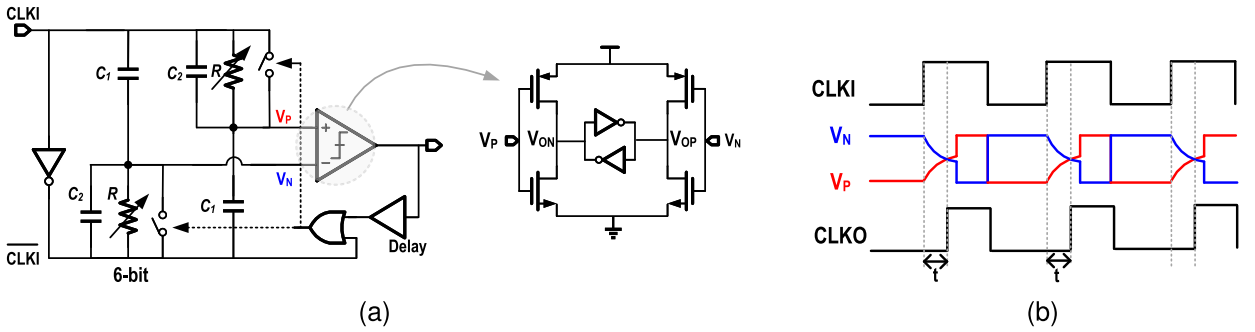

Fig. 10. (a) Delay generator based on the proposed *RC* PPF. (b) Timing diagram of the proposed *RC* PPF.

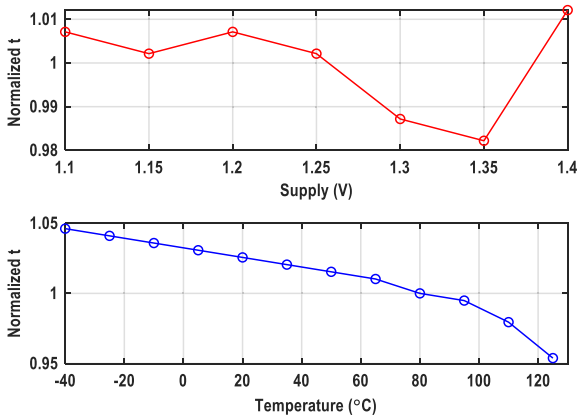

Fig. 11. Simulated delay time t (normalized to 200 ns) at different supply voltages (top) and temperatures (bottom).

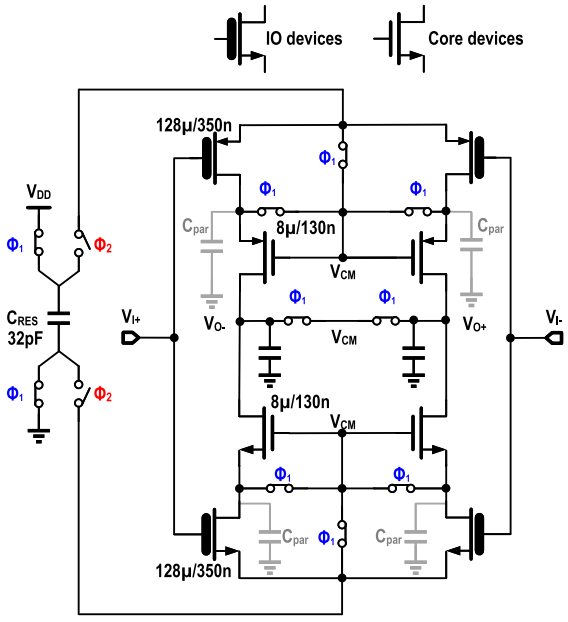

Fig. 12. Circuit diagram of the proposed cascoded FIA with internal nodes resetting.

and so can share the common mode voltage as the gate bias voltage ($V_{CM} = V_{DD}/2$) [19]. However, due to the added cascode transistors, more intermediate nodes are involved. All of them have their parasitic capacitances C_{par}, as shown in Fig. 12, which will hold the residual charge from the previous cycle, causing a signal-dependent error. Compared to the conventional cascoded FIA [19], extra switches are added to reset these floating nodes to V_{CM} during the sampling phase Φ_1, thus mitigating signal-dependent errors. Compared to a self-cascoded FIA [20], this topology reduces the parasitic capacitance at the virtual ground, thus improving energy efficiency. For flexibility, V_{CM} is provided off-chip in this prototype. However, it can be readily generated by an on-chip SC divider, which is also all-dynamic. The value of C_{RES} (=32 pF) and the transistor sizes used in the first stage FIA are shown in Fig. 12. The rest of the stages are the scaled versions of this with reduced loading capacitors.

D. Top-Level Implementation

Fig. 13 shows the block diagram of the proposed sensor interface. All the building blocks consume only dynamic power, allowing their operating frequency and power to be scaled flexibly. To reduce the $1/f$ noise and offset of the amplifiers, the amplifier of the first integrator is chopped at half of the sampling frequency $F_S/2$. Residual offset is further suppressed by applying nested low-frequency chopping (CHL) to the first and second integrators at $F_S/128$ (not shown). The CHL frequency is chosen such that the ripple is out-of-band and can be suppressed by the notches of the decimation sinc^3 filter. To compensate for the reduced maximum stable signal amplitude of a third-order $\Delta\Sigma$ modulator, the input sampling capacitor C_{IN} (0.64 pF) is set to $0.8C_{REF2}$ (in the CTAT DAC). Bootstrapped switches are employed for the input voltage sampling, thus achieving a rail-to-rail input range while maintaining good linearity.

IV. Measurement Results

The proposed sensor interface was fabricated in a standard 130-nm CMOS process with a core area of 0.2 mm^2. No external decoupling capacitor is needed for the on-chip reference. Fig. 14 shows the die photograph of this sensor interface. From a 1.2-V supply voltage, it realizes an equivalent BGR voltage ($\sim$1.22 V) and can tolerate a maximum input voltage of 1.5 V. For flexibility, the sinc^3 decimation filter was implemented off-chip.

A. Dynamic BGR and Gain Error

Since the ADC digitizes the ratio between the input voltage and the reference voltage, with a fixed 1-V dc input, the

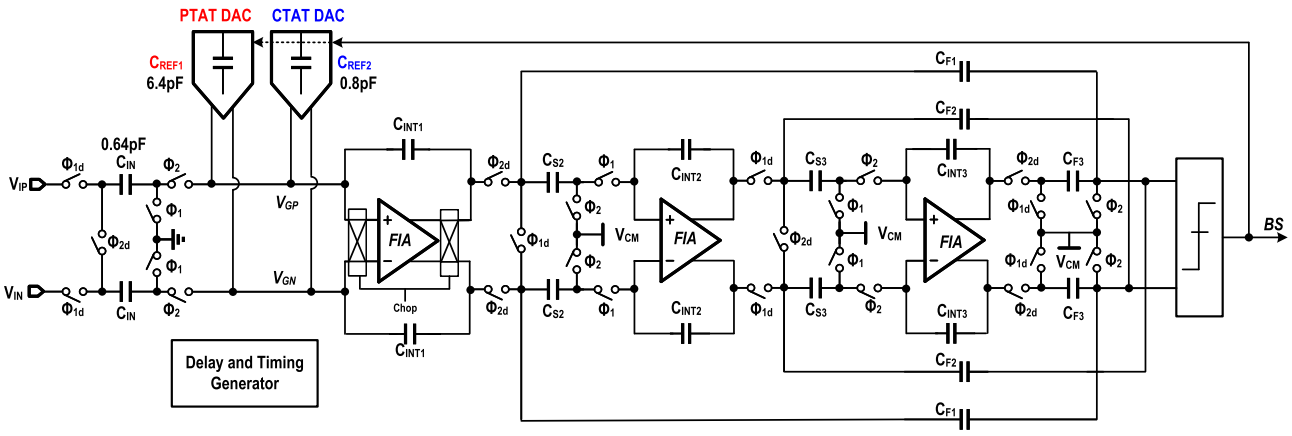

Fig. 13. Circuit diagram of the simplified 1-bit third-order $\Delta\Sigma$ modulator.

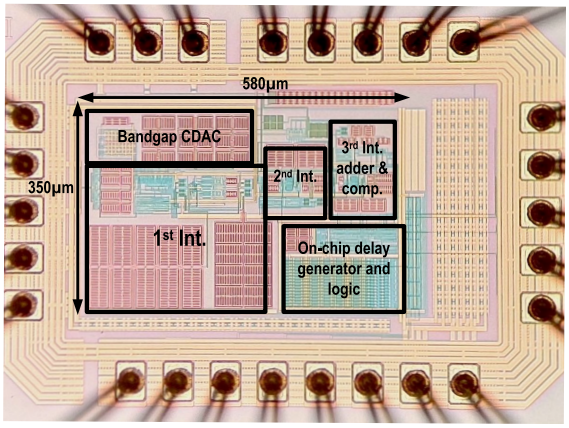

Fig. 14. Die photograph of the proposed sensor interface.

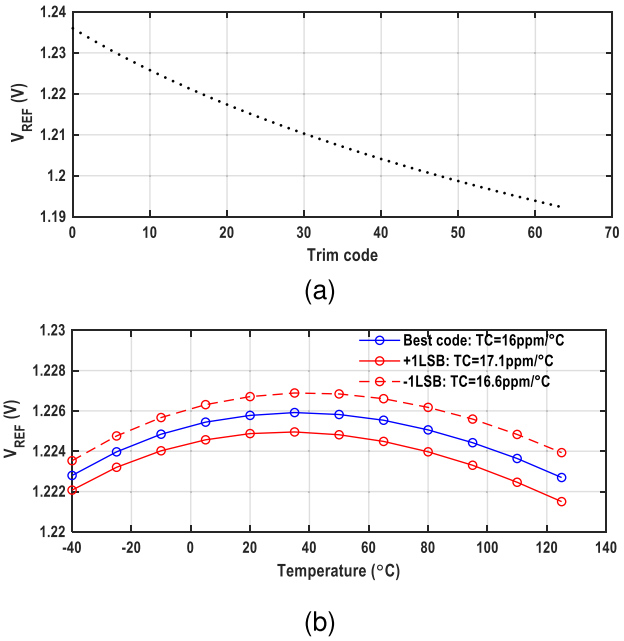

Fig. 15. (a) Measured time-domain trim of one sample: equivalent BGR V_{REF} versus trim codes at room temperature. (b) Equivalent BGR V_{REF} versus temperature.

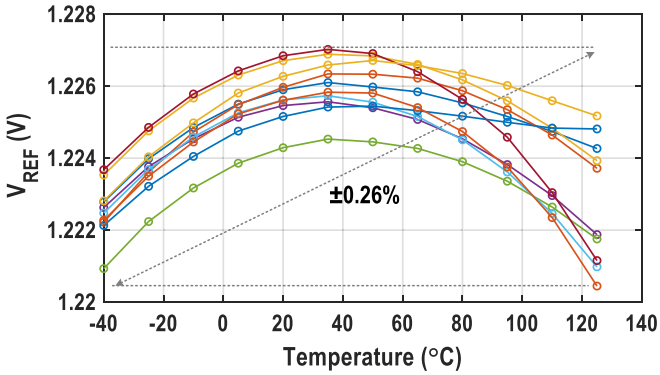

Fig. 16. Measured V_{REF} of ten samples over temperatures with a fixed 1-V dc input and identical trimming code obtained from batch calibration.

equivalent BGR voltage V_{REF} ($=\alpha V_{\mathrm{BE}} + V_{\mathrm{BE}}$) can be extracted from the ADC's decimated output. In Fig. 15, the measured equivalent V_{REF} of one exemplary sample is plotted as the 6-bit resistor in the *RC* PPF is adjusted. It shows a tuning step of about 1 mV atroom temperature. Fig. 15(b) shows the measured V_{REF} over temperature with an optimal trimming code. Using the box method, it shows a residual TC of about 16 ppm/°C. The residual TC is mainly limited by the high-order TC of the BJTs.

To verify the gain accuracy of the sensor interface, ten samples from one batch were measured from −40 °C to 125 °C. All the samples used the same *RC* trimming code obtained from batch calibration. With a fixed 1-V dc input, the extracted V_{REF} from the ADC's decimated output also reflects the gain accuracy of the entire interface. As shown in Fig. 16, the interface achieves a gain error of ±0.26% from −40 °C to 125 °C using the box method. The residual TC of ten samples varies from 16 ppm/°C to 29 ppm/°C after batch calibration. The error sources are the high order TC of V_{REF} due to the base–emitter voltage V_{BE} curvature, the spread of V_{REF} caused by the BJT emitter area mismatch, and the mismatch between the input sampling capacitor C_{IN} and the reference capacitors $C_{\mathrm{REF1,2}}$.

B. FFTs and Dynamic Range

Fig. 17(a) shows the measured output spectra when the $\Delta\Sigma$ modulator operates at $F_{\mathrm{S}} = 1$ MHz. Chopping significantly

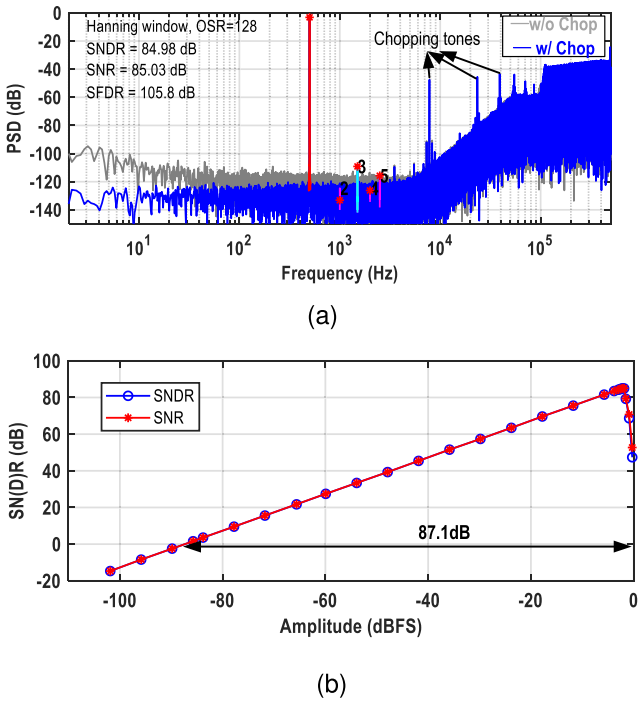

Fig. 17. (a) FFTs of the proposed sensor interface with an ac input w/wo chopping. (b) Dynamic range measurement of the proposed sensor interface.

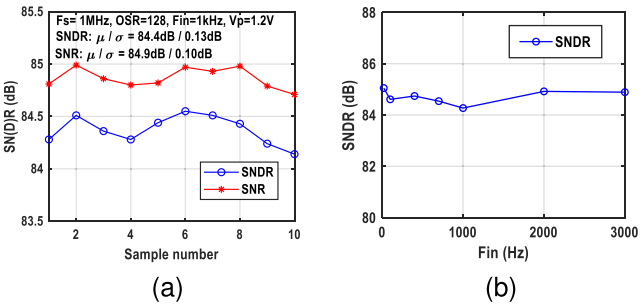

Fig. 18. (a) SN(D)R of ten samples at room temperature with $F_S = 1$ MHz, $f_{IN} = 1$ kHz, $V_p = 1.2$ V, and OSR = 128. (b) SNDR versus input frequency with $F_S = 1$ MHz, Vp = 1.2 V, and OSR = 128.

suppresses its in-band $1/f$ noise and offset. Measurements on ten samples show that the latter is reduced from 25 mV to 100 μV. With a 500-Hz 1.2-V-Vp sinusoid input signal and an OSR of 128, the modulator achieves 84.9-dB SNDR and 105.8-dB SFDR in a 3.9-kHz BW. As shown in Fig. 17(b), the modulator achieves a dynamic range (DR) of 87.1 dB. Operating at $F_S = 1$ MHz, it consumes 35.8 μW (including the BGR), which corresponds to a Schreier $\text{FoM}_{\text{SNDR/DR}}$ of 165.3/167.5 dB. Compared to a stand-alone SC $\Delta\Sigma$ modulator [4], the energy efficiency of this work is moderate due to the kT/C noise penalty of the embedded dynamic BGR.

To verify its robustness over samples, Fig. 18(a) shows the measured SNDR/SNR of ten samples. The variation (σ) is only about 0.13 and 0.1 dB, respectively. With $F_S = 1$ MHz, $V_p = 1.2$ V, OSR = 128, and the SNDRs of different signal frequencies are also measured, as shown in Fig. 18(b), whose variation is less than 0.5 dB.

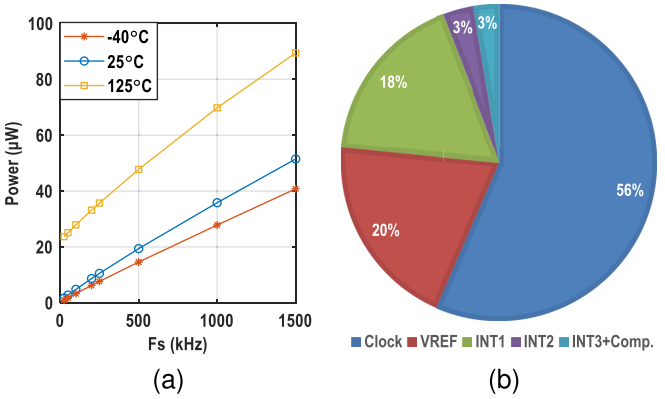

Fig. 19. (a) Measured power consumption at different sampling frequencies. (b) Power breakdown at room temperature with $F_S = 1$ MHz.

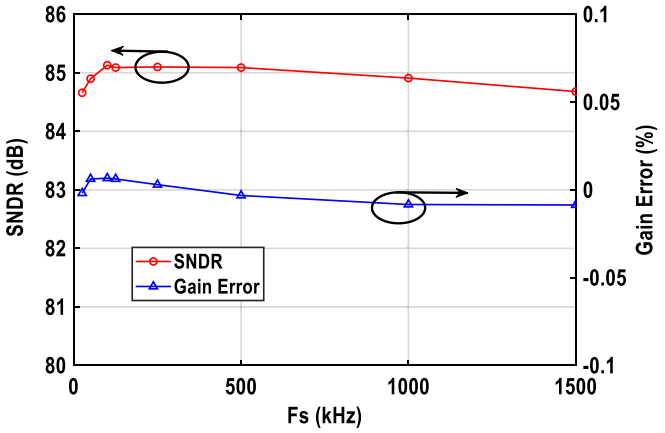

Fig. 20. Measured SNDR and gain variations with different sampling frequencies at room temperature.

C. Power and BW Scalability

Fig. 19(a) shows the measured power dissipation over temperature as the sampling frequency F_S varies from 25 kHz to 1.5 MHz. With a fixed OSR of 128, the scalable F_S corresponds to a tunable BW from 98 Hz to 5.9 kHz. Thanks to the all-dynamic design, the power consumption of the sensor interface can be scaled from 1.7 to 50.8 μW and from 1 to 40.8 μW at 25 °C and −40 °C, respectively. Due to the PTAT bias current and the leakage current, the scalable power increases at 125 °C (from 23.7 to 89.5 μW). Fig. 19(b) shows the power breakdown of the sensor interface at room temperature. More than half of the power is dissipated by the on-chip delay and clock generator.

Fig. 20 shows the measured SNDR and gain error of the sensor interface as the sampling frequency F_S varies from 25 kHz to 1.5 MHz. It keeps a consistent SNDR of larger than 84.5 dB as F_S varies. Owing to the on-chip RC delay generator, the proposed dynamic BGR is independent of the variable F_S. The measured gain variation is less than ±0.01% as F_S changes by 60 times.

D. PSRR and CMRR

The sensor interface is also measured at different dc supply voltages, as shown in Fig. 21. With a supply ranging from

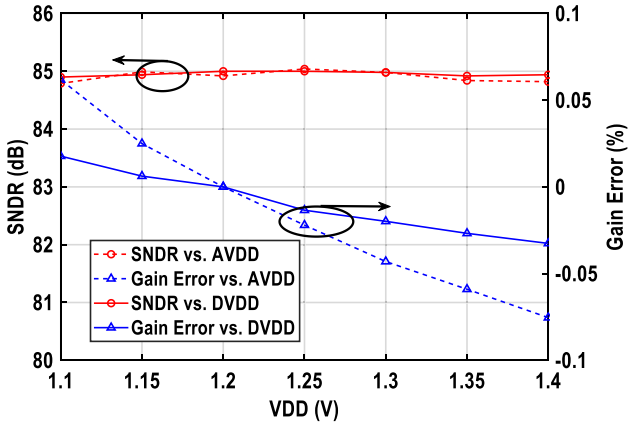

Fig. 21. Measured SNDR and gain variations at different supplies with a 500-Hz 1.2-V-Vp input, $F_S = 1$ MHz, and OSR $= 128$.

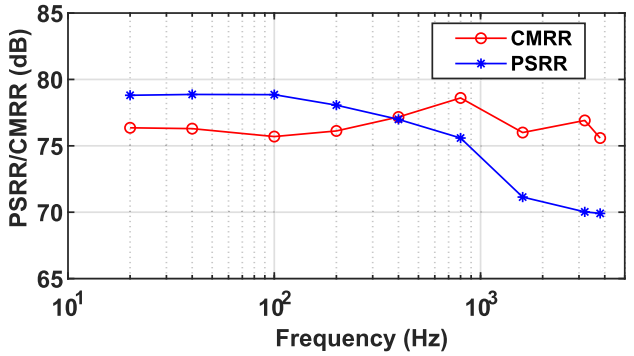

Fig. 22. Measured CMRR and PSRR of the interface at different frequencies with $F_S = 1$ MHz.

1.1 to 1.4 V and a fixed 500-Hz 1.2-V-Vp input, it consistently achieves 14-bit linearity (SNDR $>$ 84.5 dB). Thanks to the stable BGR, the measured gain variation is less than $\pm 0.1\%$ when both the analog supply (AVDD) and the digital supply (DVDD) change from 1.1 to 1.4 V. Similar to [13], the residual analog supply sensitivity is mainly limited by the CB PNPs, while the digital supply sensitivity is mainly limited by the residual supply dependence of the on-chip RC delay generator.

Fig. 22 shows the measured ac power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) of the sensor interface when working with $F_S = 1$ MHz. A 100-mVpp sinusoid wave is added to the 1.2-V supply and 0.6-V common mode voltage, respectively. It achieves a PSRR of 78 dB at low frequencies and is larger than 70 dB in the 3.9-kHz BW without external decoupling capacitors. The CMRR is larger than 75 dB, thanks to the nested CHL.

E. Comparison With the State-of-the-Art

Table I summarizes the performance of this work and compares it to state-of-the-art sensor interfaces/ADCs with a similar BW. Compared to the low-TC sensor interface in [21], this work achieves 60 times BW/power scalability and 7.5-dB better FoM_{DR}. Compared to an SAR ADC that includes a BGR [3], it achieves $>$10 times better accuracy without external decoupling capacitors.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

	This work	JSSC'21 [4]	JSSC'16 [3]	ISSCC'23 [21]
Technology	**130nm**	180nm	65nm	180nm
Architecture	**DTDSM +VREF**	DTDSM	SAR +VREF	CTDSM +VREF
Area (mm^2)	**0.20**	0.75	0.26	0.38
BW/Power Scalable	**Yes**	Yes	Yes	No
Include Reference	**Yes**	No	Yes	Yes
External Capless	**Yes**	-	No	Yes
Supply (V)	**1.1-1.4**	1.5	0.8	1.8
Fs (Hz)	**25k-1.5M**	100k-400k	80k	5.12M
Power (μW)	**1.7-50.8**	2.2-7	0.106	477
BW (Hz)	**98-5.9k**	400-1.6k	40k	10k
SNDR (dB)	**84.9**[2]	89.3	56.6	-
DR (dB)	**87.1**[2]	94.1	-	75.3
FoM_{SNDR}/ FoM_{DR}(dB)[1]	**165.3/ 167.5**[2]	172.3/ 177.1	172.4	-/160
Temperature range (°C)	**-40-125**	-	-25-110	-40-125
TC (ppm/°C)	**16-29** [3]	-	44-248 [3]	-
Inaccuracy	**$\pm$0.26%** [3]	-	$\pm$3% [3]	$\pm$0.2% [4]
Samples	**10**	1	15	10

[1] FoM_{SNDR} =SNDR + 10 log(BW/Power), FoM_{DR}= DR + 10 log(BW/Power);
[2] measured at Fs=1MHz, OSR=128, and room temperature
[3] Batch calibrated, max-min error
[4] 1-point individual trim

V. CONCLUSION

A 14-bit fully dynamic sensor interface including a dynamic BGR and $\Delta\Sigma$ modulator is proposed in this work. It employs CB PNP-based PTAT and CTAT DACs, which are summed by the first integrator of the modulator, thus realizing a dynamic BGR with additional reference buffers. To achieve fully dynamic operation, the integrators are built around cascoded FIAs. A time-domain temperature-compensation scheme is also proposed to minimize the temperature dependence of the sensor interface. Implemented in a 0.13-μm CMOS process, the sensor interface achieves an SNDR of greater than 84.5 dB over a scalable BW from 98 Hz to 5.9 kHz with a dynamic power ranging from 1.7 to 50.8 μW. It shows a batch-trimmed gain error of $\pm 0.26\%$ from -40 °C to 125 °C. Due to its easy scalability and high accuracy, it is suitable for sensors in IoT applications.

ACKNOWLEDGMENT

The authors would like to thank Chunjuan Sui, Junjie Hung, Ling Lin, Xiangyang Jiang, Guangyin Yan, and Yangfan Zhou for their technical discussion and support.

REFERENCES

[1] S. Heidary Shalmany, D. Draxelmayr, and K. A. A. Makinwa, "A $\pm$36-A integrated current-sensing system with a 0.3% gain error and a 400-μA offset from -55 °C to $+85$ °C," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1034–1043, Apr. 2017.

[2] Z. Tang, R. Zamparette, Y. Furuta, T. Nezuka, and K. A. A. Makinwa, "A versatile ±25-A shunt-based current sensor with ±0.25% gain error from −40 °C to 85 °C," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3716–3725, Dec. 2022.

[3] M. Liu, K. Pelzers, R. van Dommele, A. van Roermund, and P. Harpe, "A 106 nW 10 b 80 kS/s SAR ADC with duty-cycled reference generation in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2435–2445, Oct. 2016.

[4] M. Zhao et al., "A 4-μW bandwidth/power scalable delta–sigma modulator based on swing-enhanced floating inverter amplifiers," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 709–718, Mar. 2022.

[5] Y. Zhao, M. Zhao, and Z. Tan, "Fully dynamic zoom-ADC based on improved swing-enhanced FIAs using CLS technique with 1250x bandwidth/power scalability," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 6, pp. 1901–1905, Jun. 2023.

[6] G. Ge, C. Zhang, G. Hoogzaad, and K. A. A. Makinwa, "A single-trim CMOS bandgap reference with a 3σ inaccuracy of ±0.15% from −40 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2693–2701, Nov. 2011.

[7] J.-H. Boo et al., "A single-trim switched capacitor CMOS bandgap reference with a 3σ inaccuracy of +0.02%, −0.12% for battery-monitoring applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1197–1206, Apr. 2021.

[8] J. M. Lee et al., "A 29nW bandgap reference circuit," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2015, pp. 1–3.

[9] Y. Ji, C. Jeon, H. Son, B. Kim, H.-J. Park, and J.-Y. Sim, "A 9.3nW all-in-one bandgap voltage and current reference circuit," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 100–101.

[10] M. Eberlein, G. Panagopoulos, and H. Pretl, "A 40 nW, sub-IV truly 'digital' reverse bandgap reference using bulk-diodes in 16 nm FinFET," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2018, pp. 99–102.

[11] Z. Tang et al., "A 14b 98Hz-to-5.9 kHz 1.7-to-50.8 μW BW/power scalable sensor interface with a dynamic bandgap reference and an untrimmed gain error of ±0.26% from −40 °C to 125 °C," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 60–62.

[12] E. H. Hellen, "Verifying the diode–capacitor circuit voltage decay," *Amer. J. Phys.*, vol. 71, no. 8, pp. 797–800, Aug. 2003.

[13] Z. Tang, S. Pan, M. Grubor, and K. A. A. Makinwa, "A sub-1 V capacitively biased BJT-based temperature sensor with an inaccuracy of ±0.15 °C (3σ) from −55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3433–3441, Dec. 2023.

[14] S. H. Shalmany, D. Draxelmayr, and K. A. Makinwa, "A micropower battery current sensor with ±0.03% (3σ) inaccuracy from −40 to +85 °C," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 386–387.

[15] Z. Tang, Y. Fang, X.-P. Yu, N. N. Tan, Z. Shi, and P. Harpe, "An energy-efficient capacitively biased diode-based temperature sensor in 55-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 210–213, 2021.

[16] W. Choi, J. Angevare, I. Park, K. A. A. Makinwa, and Y. Chae, "A 0.9-V 28-MHz highly digital CMOS dual-*RC* frequency reference with ±200 ppm inaccuracy from −40 °C to 85 °C," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2418–2428, Aug. 2022.

[17] W. Choi et al., "A compact resistor-based CMOS temperature sensor with an inaccuracy of 0.12 °C (3σ) and a resolution FoM of 0.43 pJ·K^2 in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3356–3367, Dec. 2018.

[18] X. Tang et al., "An energy-efficient comparator with dynamic floating inverter amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1011–1022, Apr. 2020.

[19] Y. Liu et al., "A fully dynamic 4-channel 13b simultaneous sampling incremental $\Delta\Sigma$ ADC using cascoded floating-inverter-amplifier and code division multiplexing technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 10, pp. 3737–3741, Oct. 2023.

[20] X. Tang et al., "A bandwidth-adaptive pipelined SAR ADC with three-stage cascoded floating inverter amplifier," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2564–2574, May 2023.

[21] Z. Tang, N. G. Toth, R. Zamparette, T. Nezuka, Y. Furuta, and K. A. A. Makinwa, "A 40A shunt-based current sensor with ±0.2% gain error from -40 °C to 125 °C and self-calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 56, Feb. 2023, pp. 348–350.

Zhong Tang (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2015 and 2020, respectively.

From 2019 to 2020, he was a Visiting Ph.D. Student with EEIC Group, Eindhoven University of Technology, Eindhoven, The Netherlands. From 2020 to 2023, he was a Post-Doctoral Researcher at the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands. He is currently an Analog IC Designer with Vango Technologies, Inc., Hangzhou. His research interests include precision analog and mixed-signal integrated circuits. This has led to over 35 technical articles, including seven from the IEEE International Solid-State Circuits Conference (ISSCC) and six from IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC).

Dr. Tang was a recipient of the Outstanding Doctoral Thesis Award of Chinese Institute of Electronics in 2022.

Yuyan Liu (Member, IEEE) received the B.E. and Ph.D. degrees from Zhejiang University, Hangzhou, China, in 2018 and 2023, respectively.

In August 2023, he joined Delft University of Technology, Delft, The Netherlands, as a Post-Doctoral with the Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS). His research interests include low-power data converters and mixed-signal circuits and systems.

Pengpeng Chen received the B.S. and Ph.D. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2009 and 2017, respectively.

He is currently a Senior Engineer with Shaoxing Devechip Microelectronics Company Ltd., Hangzhou, China. His research interests include radio frequency (RF) transceiver design, low-power circuit design for wireless body area networks, and high-accuracy analog front-end design for sensors.

Haining Wang received the B.S. degree in communication engineering from Hangzhou Dianzi University, Hangzhou, China, in 2015.

He is currently an Electronics Engineer with Vango Technologies, Inc., Hangzhou.

Xiao-Peng Yu (Member, IEEE) received the B.Eng. degree in optical engineering from Zhejiang University, Hangzhou, China, in 1998, and the Ph.D. degree from the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore, in 2006.

From 2000 to 2002, he was an Engineer at MOTOROLA's Global Telecom Solutions Sector, Hangzhou, and a Research Staff Member at NTU, from 2005 to 2006. Since 2006, he has been affiliated with the Institute of VLSI Design, Zhejiang University, where he holds the position of a Qiushi Distinguished Professor. He further expanded his academic horizons as a Visiting Scholar at Eindhoven University of Technology (TU/e), Eindhoven, The Netherlands, from 2008 to 2010, and a Marie Curie Fellow at the Mixed Signal Microelectronics Group, TU/e, a role co-hosted with Philips Research, Eindhoven. His research is primarily focused on the design and development of analog, mixed-signal, and radio frequency integrated circuits.

Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from the Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven. Since 1999, he has been with Delft University of Technology, where he is an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors. This has led to more than 20 books, more than 350 technical papers, and more than 30 patents.

Dr. Makinwa is a member of the Royal Netherlands Academy of Arts and Sciences. He was the Analog Subcom Chair of ISSCC from 2018 to 2021 and has served on the program committees of several other IEEE conferences. He has also been a Distinguished Lecturer of the Solid-State Circuits Society and an Elected Member of its Adcom. He is currently a member of the Executive Committee of the VLSI Symposium and the Co-Chair of the Advances in Analog Circuit Design (AACD) Workshop and the IEEE Sensor Interfaces Meeting (SIM). He was a co-recipient of 18 best paper awards, from IEEE JOURNAL OF SOLID-STATE CIRCUITS, ISSCC, and VLSI Symposium, among others. In 2023, at the 70th anniversary of ISSCC, he was recognized as its top contributing author.

Nick Nianxiong Tan (Senior Member, IEEE) received the B.Eng. and M.Eng. degrees from Tsinghua University, Beijing, China, in 1988 and 1991, respectively, and the Ph.D. degree from Linköping University, Linköping, Sweden, in 1994.

He is currently a Full Professor with Zhejiang University, Hangzhou, China, and the Chairperson of Vango Technologies, Inc., Hangzhou, China, a fabless semiconductor company for the Internet of Energy. Prior to starting up Vango Technologies, Inc., he was the Founder and the CEO of AnaLutions, Inc., Laguna Niguel, CA, USA, a chip design service company. He also worked as a Design Director at GlobeSpan (a Bell lab spinoff), Red Bank, NJ, USA, and worked at the Ericsson's Research and Development Center, Stockholm, Sweden. He taught mixed-signal chip design and supervised Ph.D. students at Linköping University. He is an accomplished chip designer and a researcher with an interest in mixed-signal chip design and agile design methodologies. He holds 32 U.S. patents and numerous Chinese patents. In addition, he has written three books and book chapters and published over 100 papers.