Sparsity-Aware Hardware: From Overheads to Performance Benefits

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DOI
10.1109/MSSC.2025.3549709

Publication date
2025

Document Version
Final published version

Published in
IEEE Solid-State Circuits Magazine

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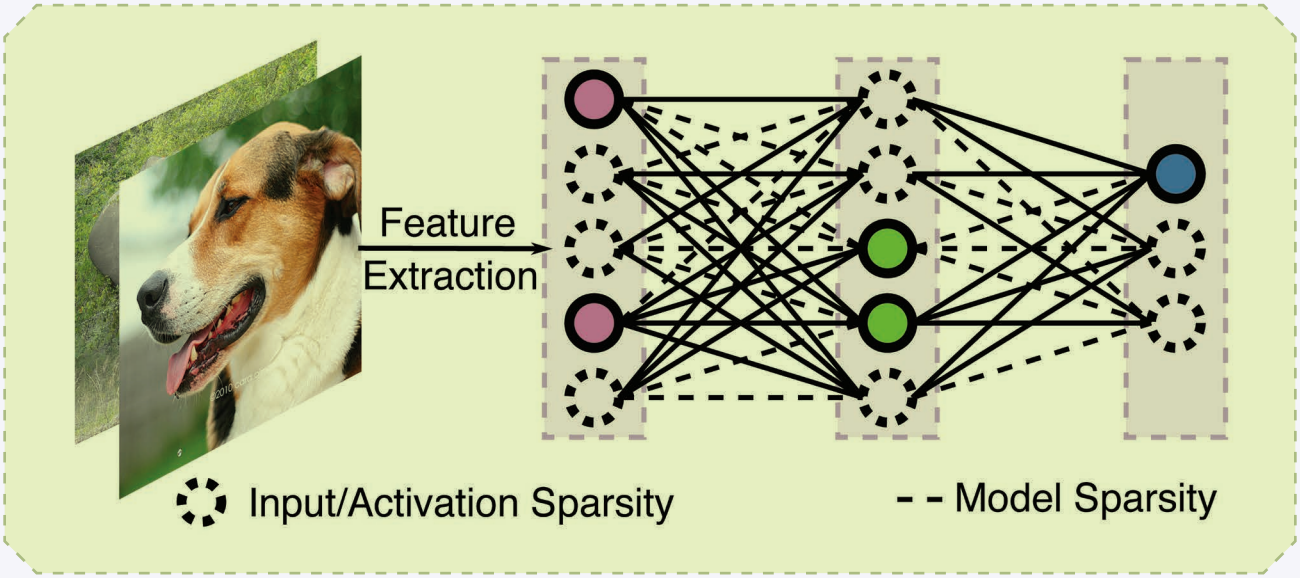
From Overheads to Performance Benefits



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As artificial intelligence (AI) continues to transform multiple sectors, its exponential growth in computational demands presents significant challenges for hardware infrastructure. This article examines sparsity, the prevalence of zeros in AI workloads, as a promising approach to address these challenges. While sparsity offers potential efficiency gains, its practical implementation requires careful consideration of hardware constraints and computational overheads. Therefore, this article cooperates with a virtual performance roofline model to analyze various sparsity techniques and their associated tradeoffs, aiming to bridge the gap between theoretical potential and practical implementation in AI accelerator design.

Digital Object Identifier 10.1109/MSSC.2025.3549709
Date of current version: 20 June 2025

Introduction: Sparsity in AI Workloads

AI systems exert a transformative impact across numerous fields, reshaping our modern world [1], [2], [3], [4]. However, this rapid growth comes at a significant cost: The computational demands of AI infrastructure are doubling approximately every 100 days [5]. This skyrocketing trend poses performance concerns for the supporting AI computing hardware, which struggles to scale at a comparable pace. This challenge has prompted hardware architecture designers to seek solutions off the beaten path.

One particularly promising strategy leverages an intriguing characteristic of AI workloads: their sparsity [6]. Sparsity represents the fraction of operands in AI workloads that consist of zero values (whether weights or activations), and thus do not contribute any useful information to the output However, leveraging sparsity in AI accelerators is not trivial and requires a detailed understanding of the

This tight codesign process requires a good understanding of the various existing types of algorithmic sparsity that can be exploited at the hardware level.

underlying hardware constraints and computational overheads. To bring sparsity from a theoretical concept into a practical efficiency technique, the key lies in strategically balancing computational performance gains and the hardware overheads induced by sparsity handling.

In this article, we revisit the hardware roofline model to take sparsity into performance consideration, thereby sketching the landscape of sparsity techniques, their opportunities, as well as their related overheads.

Hardware Implications of Sparsity

Whether sparse or not, AI workloads, such as deep neural networks (DNNs) usually consist of simple yet numerous tensor operations, mainly matrix–vector or matrix–matrix multiplications (denoted MVMs and MMs, respectively), which dominate the workload's latency and energy per inference. These workloads are thus typically executed on specific tensor accelerators optimized for dense MMs/MVMs, with large computational parallelism, excellent data reuse, and a resulting 100 to 1,000× lower energy per operation than conventional CPUs or GPUs (without tensor cores) [7]. These hardware accelerators [8], [9] typically consist of three parts [Figure 1(a)]: a *datapath* formed by an array of processing elements (PEs) that compute parallel multiply-accumulate (MAC) operations to yield the MM/MVM result, a local *memory* connected to the datapath through a high-bandwidth interface to store the DNN's weights and input/output activations, and a *controller* orchestrating the accelerator's dataflow.

To minimize the latency and energy footprint of DNN inference, one aims to utilize 100% of the accelerator's computing resources at all times. Under such peak utilization, each PE performs a MAC operation at each clock cycle, and the memory bandwidth utilization matches the processing rate of the datapath. These conditions leverage the peak computational efficiency of the accelerator, commonly described by two performance metrics: its throughput (GOPS) and energy efficiency (TOPS/s/W). Nonetheless, the actual performance of the accelerator is in practice affected by the arithmetic intensity of the DNN workload, as described by its *roofline model* (see "Visualizing Computational Performance: The Virtual Roofline Model").

Yet, dense DNN accelerator cores are optimized for dense DNN workloads: They process MACs regardless of the presence of zero operands. These zero-valued MACs do not contribute to the final result, and therefore result in wasted computing time and energy. As such, sparsity effectively leads to an underutilization of either the datapath, memory bandwidth,

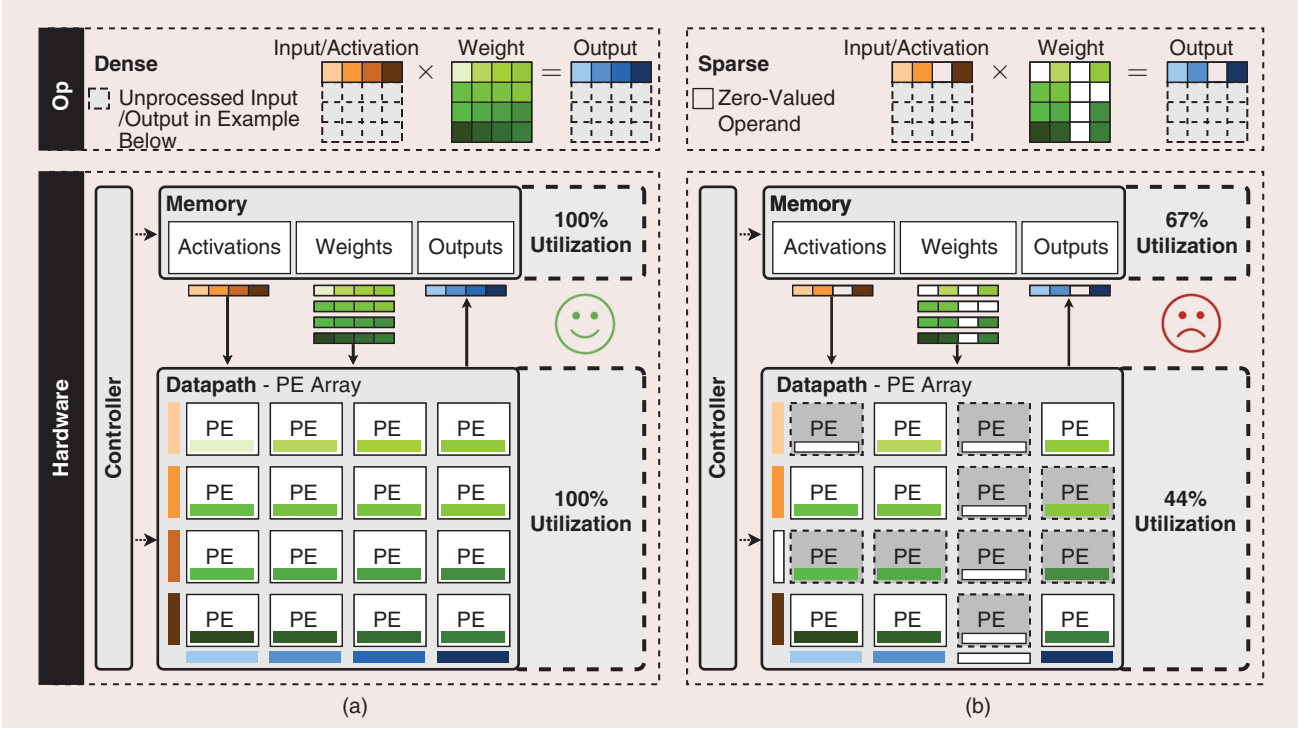

FIGURE 1: Hardware architecture of a dense DNN accelerator, running (a) a dense and (b) a sparse matrix-matrix multiplication, typically consisting of several MAC operations. Reported hardware utilization is illustrative.

and/or memory content, as shown in Figure 1(b). To overcome these, sparsity-aware techniques have been investigated to account for sparse operands directly at the hardware level. Their impact on performance can be captured in a virtual roofline model (see "Visualizing Computational Performance: The Virtual Roofline Model") reflected by a change in the roofline boundary as a function of the density level (= 1 – sparsity). At low sparsity, sparsity-aware accelerator cores generally suffer from a drop in virtual peak throughput compared to dense cores due to the introduced hardware overheads to handle sparsity. As the sparsity level rises, benefits from sparsity increase the virtual throughput: The gap between dense and sparsity-aware performance narrows down, eventually disappearing at the sparsity turning point, beyond which virtual throughput gains start to be leveraged. Yet, doing so requires matching the supported sparsity technique(s) with the nature of the sparsity present in the workload at hand. This tight codesign process requires a good understanding of the various existing types of algorithmic sparsity that can be exploited at the hardware level.

The Many Faces of Sparsity

Sparsity in DNNs can be classified into different categories (Figure 2) based on the organization of zeros in operands (i.e., whether structured or not), as well as on the underlying granularity of the zero elements (i.e., from individual bits to full values). While sparsity can be inherently present in DNN operands, it often needs to be induced in the software pipeline to reach significant levels [10]. It usually relies on adjusting or retraining a model prior to deployment [11], or on setting activations to zero based on known statistics [12]. This often leads to an accuracy penalty, which will typically be more severe for structured than for unstructured sparsity [13].

Along the first categorization axis, *unstructured sparsity* corresponds to the absence of clear patterns in an operand's sparsity, with the zero-valued elements irregularly scattered across a tensor. Unstructured sparsity inherently arises at the bit level in binary data representations. Yet, it can also occur at the value level as a result of weight pruning or regularization

VISUALIZING COMPUTATIONAL PERFORMANCE: THE VIRTUAL ROOFLINE MODEL

The virtual roofline model is derived from the traditional roofline model, commonly used to benchmark the performance landscape of CPU or GPU architectures [S1], [S2], [S3]. It allows assessing the maximum achievable throughput of a processor with a given memory bandwidth and peak performance, as a function of a workload's arithmetic intensity. The *virtual* roofline extends it to include the first-order dependence of a core's performance on the sparsity-aware characteristics (Figure S1):

- The *arithmetic intensity* ❶ is the workload-dependent number of (zero and nonzero) operations performed per virtually transferred (zero and nonzero) byte of data (OPs/byte).
- The *virtual throughput* ❷ is the ratio between the total number of (zero and nonzero) operations and their total effective execution time (GOPS).
- In the *memory-bound regime* ❸ at low arithmetic intensity, *peak throughput* is limited by the *virtual memory bandwidth* ❹. In the *compute-bound regime* ❺ at high arithmetic intensity, it is limited by the datapath's parallelism. The resulting roofline curve corresponds to performance with a 100% utilization of the core's resources. The region above it is unreachable, while that below means under-utilization.
- While dense-optimized processors have a fixed roofline (black line in Figure S1), that of sparsity-aware processors changes with the sparsity level. At 0% sparsity (i.e. 100% density), the roofline drops below the dense processor performance (red area in Figure S1) due to hardware overheads for handling sparsity. At high sparsity levels, gains from virtual memory and compute throughput increases kick in (green area in Figure S1).
- The *sparsity turning point* ❻ is the sparsity level at which hardware overheads brought by sparsity-aware hardware techniques are overcome by virtual throughput gains. The memory- and compute-bound regimes can have different turning points depending on the supported sparsity-aware hardware techniques.

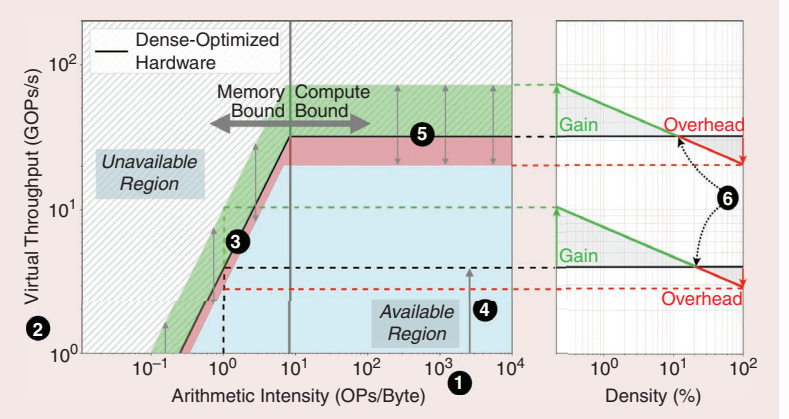

FIGURE S1: (a) The virtual roofline model and (b) corresponding tradeoffs in the memory- and compute-bound regimes as a function of density (= 1 – sparsity).

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> ***Altogether, the structured nature of these sparsity types results in a much higher regularity and determinism in the processing of the sparse workload.***

techniques during training [14], or due to thresholding functions during inference which zero out operands over ranges of input values [e.g., the conventional rectified linear unit activation function] [15]. However, the irregularity of the zero element locations entails fine-grained hardware and control overheads.

In contrast to unstructured sparsity, *structured sparsity* is characterized by a clear pattern of the zero elements within operand tensors. These patterns can also appear at a bit-level granularity, or at a value-level one. Moreover, at both granularities, the structure can present itself in different ways. First, in block sparse tensors, zeros are clustered together into subtiles of the tensor. At the bit level granularity, zero bits are packed together within one word or even across adjacent words [10]. At value-level granularity, such a tile can be a complete tensor row, column, 2D or 3D subset of the tensor [16], [17]. Alternatively, zero-valued operands can be structured based on *density bounding*, in which case every block of M tensor elements can have at most N nonzero elements, also denoted as N:M sparsity [18]. This form of structured sparsity is also possible at the value or at the bit level, as done in bit-balance [19], where the latter limits the number of "1" bits in each element. Quantization [20], [21] represents a specialized form of structured bit-level sparsity. Unlike previously discussed approaches that permit distributed nonzero bits, quantization typically mandates consecutive bit placement. This design choice eliminates index storage overhead and simplifies hardware implementation, although it imposes a more severe tradeoff between training effort and bit reduction while maintaining model accuracy [10], [20].

Altogether, the structured nature of these sparsity types results in a much higher regularity and determinism in the processing of the sparse workload. This in turn simplifies encoding/decoding schemes, run-time scheduling, or workload balancing complexity. The benefits this brings in terms of reducing hardware overheads can, however, be overshadowed by the inferior tradeoff between sparsity levels and task accuracy compared to unstructured sparsity.

Exploiting Unstructured Sparsity in Hardware: High Cost, High Reward?

To harness the potential benefits of sparsity, various accelerators and techniques have been developed in recent years, with some examples provided in Table 1. Among these techniques, those exploiting unstructured sparsity were the earliest to emerge [11], [24]. Unstructured sparsity can be leveraged in two distinct ways: From the memory perspective, it offers compression opportunities, while from the datapath perspective, it allows gating or skipping zero-valued operations, as visualized in Figure 3.

Compression techniques, on the one hand, are commonly used to compact sparse activations/weights into a dense representation, primarily aiming for a reduced memory footprint. Yet, these methods are typically penalized with an index overhead associated with indicating nonzero elements and ensuring accurate data decoding during the computational processes. The critical challenge lies in identifying an optimal sparsity turning point that strategically balances compression efficiency with indexing overhead, as discussed in [25]. Consequently, researchers have proposed diverse compression techniques to optimize

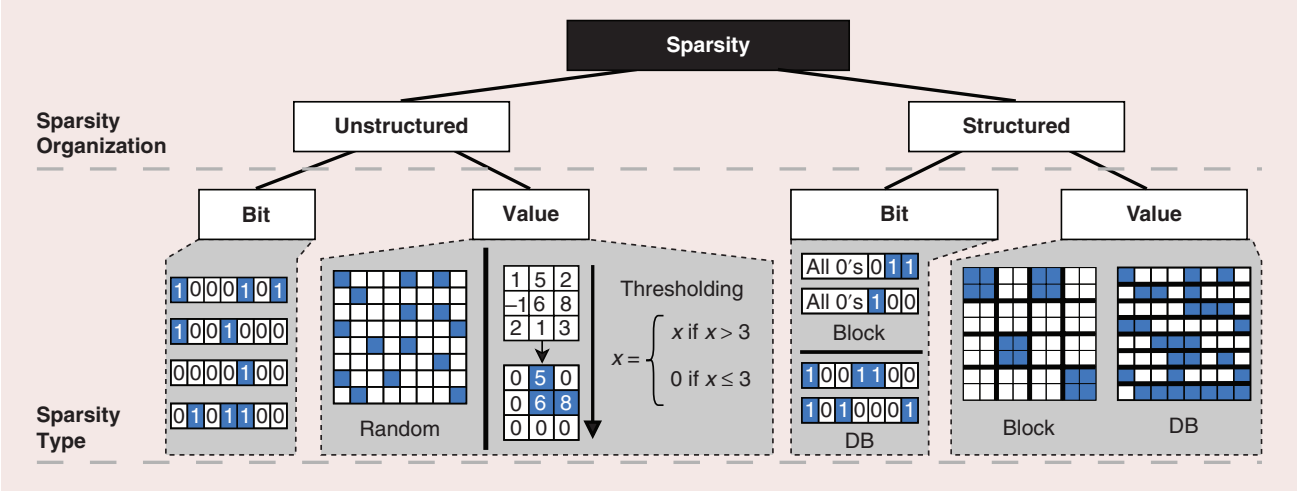

FIGURE 2: Classification of sparsity types appearing in DNN operands. DB: density bounded.

sparse data representations. Bit-masking (BM)-based compression [Figure 3(a)], for example, used in SparTen [26], employs "1" to indicate the locations of nonzero values within tensors, which has proven to be particularly advantageous for scenarios with lower sparsity (<30% sparsity [27]). In contrast, the compressed sparse row or column (CSR/CSC) representation emerges as a prominent technique for high-sparsity scenarios (>70% sparsity [27]), and is widely adopted in existing work [11], [23]. As illustrated in Figure 3(b), this method encodes nonzero element locations into coordinates, which are then stored consecutively in memory. In addition, recent advances [28], [29] leverage the abundant bit-level sparsity present in AI workloads to conduct data compression. For instance, as shown in Figure 3(c), the compact canonical signed digit is able to compress an N-bit data element into N/2 bits by encoding data in common 2's complement format with dedicated encoder/decoder support [28].

Sparsity-aware datapaths, on the other hand, typically involve MAC gating and/or skipping techniques to save computational energy and increase the throughput of the datapath. As illustrated in Figure 3(f), MAC gating introduces an additional signal and/or clock gating cell to each MAC, reducing computational energy consumption by freezing the inputs and disabling the MAC whenever a zero is detected. Envision [24] applies this gating technique at the value level for both activations and weights, leading to a standalone 1.6× energy saving for 30%–60% sparsity. Such gating techniques bring energy benefits and only come with small hardware overheads, yet they fail to provide any improvement in system throughput.

Alternatively, the sparsity-driven MAC skipping techniques skip the computation whenever a zero is detected at the MAC inputs [34]. As shown in Figure 3(g), online value-level activation-sparsity detectors are introduced to squeeze out zero activations, hence streaming only nonzero activations into the PE array and increasing the temporal utilization. Similarly, the technique can also be applied at the bit level, by skipping the ineffective bit-level operations to enhance the datapath efficiency in a more fine-grained manner. Bit-pragmatic [35] skips the zero-bit–associated computation by only processing nonzero activation bits in a bit-serial manner, as shown in Figure 3(h). In contrast to MAC gating, MAC skipping brings both energy savings as well as throughput benefits, making it an attractive target. However, a naive implementation of MAC skipping entails a risk for compute resources underutilization, due to uneven workload allocations to the different MACs, as shown in Figure 3 (g) and (h). State-of-the-art hardware implementations further incorporate advanced runtime load-balancing techniques to improve utilization, yet at the expense of increased complexity and hardware overhead. These additional hardware costs can be attributed to control logic overhead to dynamically parse the sparse data elements, manage nonzero value routing, and balance computational resources online to maintain efficient processing. Practical implementations underline the significant challenges: Both sparse convolutional neural networks (SCNN) [23] and SIGMA [27] dedicated more than 30% of their hardware area to their online data scheduler. These routing and compilation overheads can potentially negate the intended performance benefits, worsening the sparsity turning point for such accelerators.

Adapting the formalism of the virtual roofline model (see "Visualizing Computational Performance: The Virtual Roofline Model") to the above hardware techniques allows estimating this overhead-performance tradeoff. The virtual roofline of Figure 4(a) illustrates the typical sparsity turning point of accelerator cores concurrently supporting CSR compression and operand skipping in the presence of unstructured activation sparsity.[1] Such sparsity is notably exploited by spatial approaches, which leverage activation sparsity within individual tensor frames. In the compute-bound regime, initial overheads arise from the complex cycle-skipping control circuitry and the distribution of nonsparse operands across PEs, resulting in a turning point around a density of 60% for cycle skipping to become effective [23]. In the memory-bound regime, the virtual bandwidth utilization is originally degraded by the additional transfer of the compression metadata (i.e., encoding indices) compared to the dense case. Figure 4(a) highlights that in the typical range of activation

[1]The rooflines are drawn by assuming 128 parallel PEs in the datapath running at a 125-MHz clock, with a 4-Gb/s maximum memory bandwidth (1 MAC = 2 OPs) for each accelerator core.

TABLE 1. STATE-OF-THE-ART SPARSITY-AWARE AI ACCELERATORS.

ARCHI.	SCNN [23]	STICKER [11]	S2TA [30]	E-LLM [31]	BITLET [32]	BSAA [28]	SIBIA [33]	BitWAVE [10]
SPARSITY TYPE	UNSTRUCTURED VALUE SPARSITY		STRUCTURED VALUE SPARSITY		UNSTRUCTURED BIT SPARSITY		STRUCTURED BIT SPARSITY	
Gating	✗	✓	✗	✗	✗	✗	✗	✗
Skipping	✓	✓	✓	✓	✓	✓	✓	✓
Compression	✓	✓	✓	✓	✗	✓	✓	✓

BSAA: Bit-sparsity aware acceleration; LLM: large language model; SCNN: sparse convolutional neural networks.

sparsity harnessed in mainstream spatial DNN models, the dense-optimized core always outperforms its sparsity-aware counterpart under the given assumptions. Therefore, the turning point lies in the unavailable region of the sparsity-aware core. Altogether, the gains of unstructured sparsity seem limited, unless very high sparsity levels can be achieved. The graph neural networks (GNNs) can be a concrete example, as GNN sparse hardware still yields substantial gains due to extreme sparsity [36], [37] despite requiring complex memory controllers and schedulers to handle irregular connectivity patterns [38], [39].

Increasing input sparsity is also pursued by spatiotemporal approaches, which exploit activation

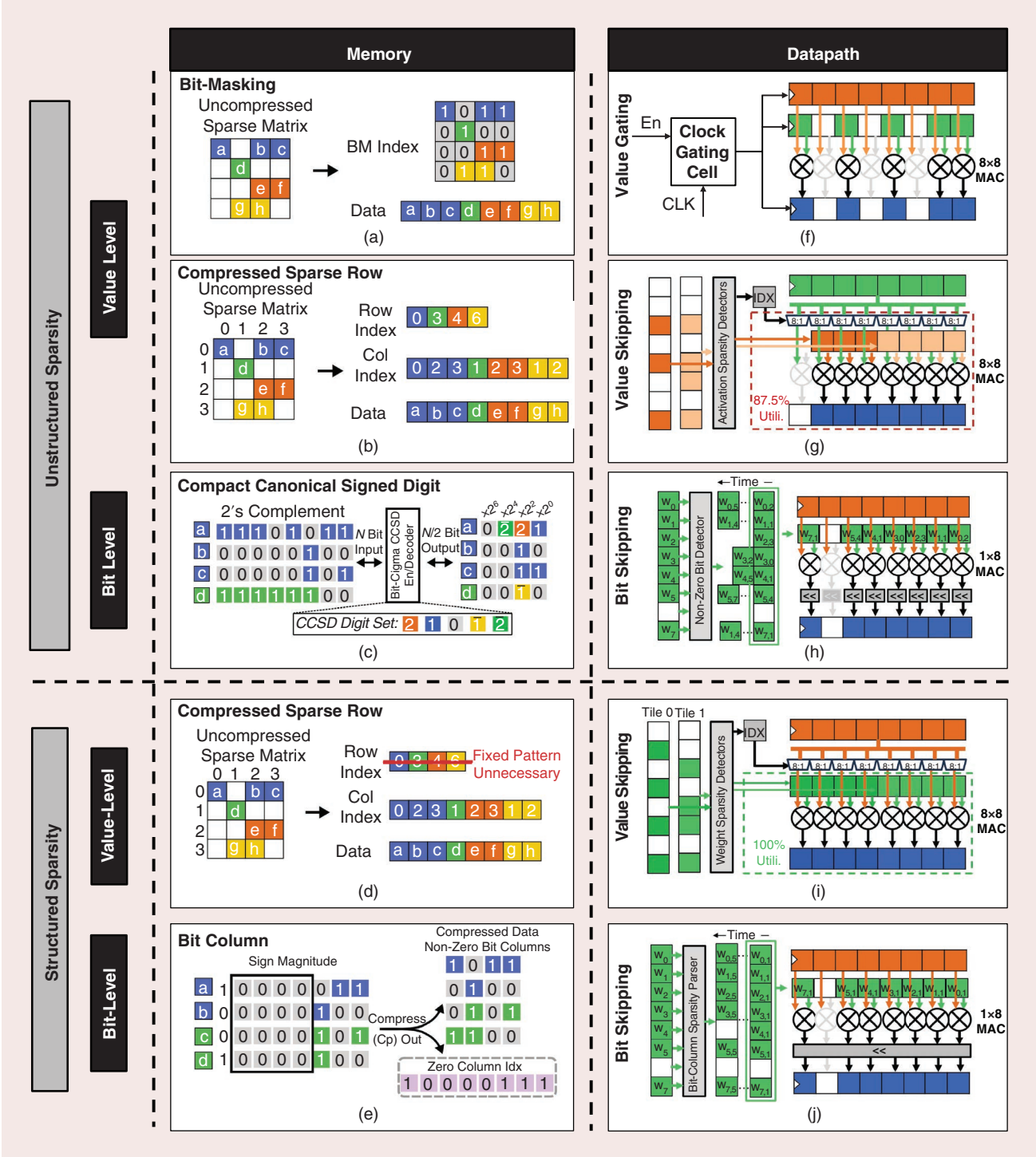

FIGURE 3: (a)–(j) Examples of hardware techniques suiting different sparsity types, from the memory and datapath perspectives. BM: bit masking.

sparsity along the time dimension. For example, deltaCNN and deltaRNN skip the processing of static elements between successive frames [41], [42], [43], enabling up to 98% unstructured activation sparsity. However, they both require computing the frame-to-frame difference on the fly, involving a latency penalty as well as a significant memory overhead to store the previous frame. Instead, event-based approaches can leverage the inherent sparsity of event cameras to bypass the latency bottleneck, processing events either in time-windowed batches using accumulated bin histograms [44], or in a fully event-driven fashion [22], [37], [45]. As the level of sparsity is purely dependent on the activity in the observed scene, extreme sparsity levels can be leveraged when moving from frame-based to pure event-driven processing. Nonetheless, leveraging temporal activation sparsity implies a memory overhead to store additional neuron states, needed to keep track of the evolution of information in time. These extra states also translate into increased data transfers that further pressure the available memory bandwidth.

The virtual roofline of such a spatiotemporal processing of unstructured sparse inputs and activations is compared to the previously discussed roofline in Figure 4(b). In the compute-bound regime, overheads from cycle-skipping are similar and the turning point likewise lies around a 60% density [23]. In contrast, in the memory-bound region, the increased data transfer overhead stemming from storing and communicating the neuron state information [22] brings the sparsity turning point down below the 10% density mark [Figure 5(b)]. As a result, the transition between the compute- and memory-bound regimes moves toward a higher arithmetic intensity. Despite this, the high sparsity levels unlocked by the spatiotemporal approaches outline order-of-magnitude throughput gains, especially when striving toward event-driven processing in the compute-bound regime.

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Leveraging Predeployment Model Knowledge for Structured Sparsity Hardware

Previous discussions showed that, to exploit unstructured sparsity, a complex online scheduler or encoders/decoders are required to retain a high utilization of the PE array or memory bandwidth. Such burdens can be alleviated if the sparsity patterns are regular and known beforehand, which are exactly the properties of structured sparsity in a DNN model [46], [47]. For instance, NVIDIA's support for 2:4 density-bounded structured sparsity in the Ampere architecture offers a more regular workload mapping with fewer overhead losses compared to unstructured sparsity [47]. The impact on processor performance can again be assessed from a memory and from a datapath perspective.

From the memory side, when exploiting the value-level sparsity as shown in Figure 3(d), the indexing cost of the CSR format under structured sparsity can be reduced by removing the row (or tile) indices, and only indicating the nonzero positions within each tile [30]. The compressed data can moreover be organized in a regular pattern for efficient storage and access. Both of these are attributed to the known number of nonzero elements per tile. In contrast, as shown in Figure 3(e), the bit-level

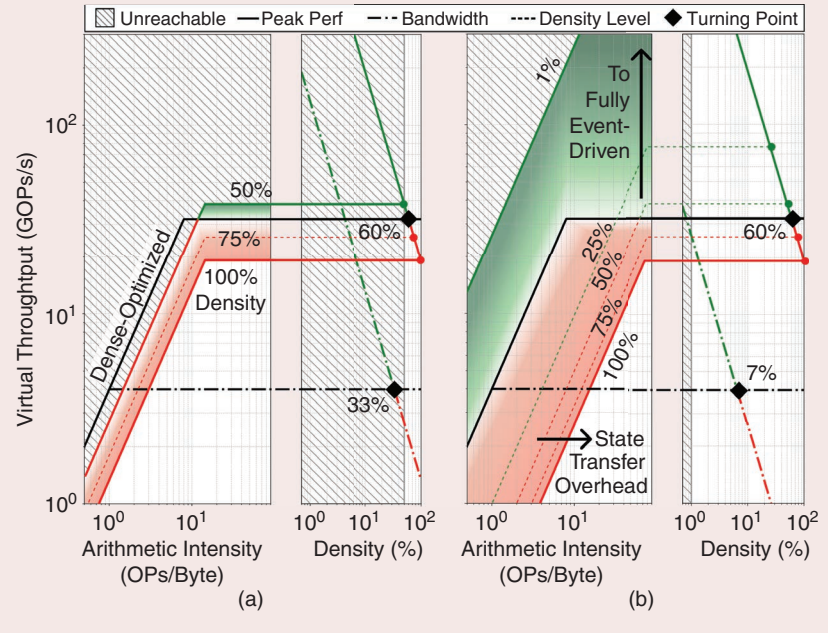

FIGURE 4: Virtual roofline representation of two different accelerator cores, respectively exploiting (a) spatial-only and (b) spatiotemporal unstructured activation sparsity. The 33% memory-bound turning point in (a) results from the compression of 8-b values into a CSR format, bringing a 200% overhead over a dense representation [18]. The 7% memory-bound turning point in (b) relates to the additional neuron state information [22]. The compute-bound turning points derived from hardware overheads in [23].

Nevertheless, the conclusion remains valid: At a fixed level of sparsity, DNN cores exploiting structured sparsity outperform those supporting unstructured sparsity for a same array size.

sparsity can be exploited by reorganizing weights into structured bit vectors that share zero-bit positions in each bit column [10].

From the datapath side, when applying the skipping technique on the value level, structured sparsity patterns allow for a full utilization of the MAC arrays with little control overhead, as the nonzero positions and MAC availability follow strict structured patterns. Specifically, comparing the skipping techniques for unstructured and structured value sparsity, as in Figure 3 (g) and (i), a 1-to-8 MUX is required for each MAC in both cases. Yet, in contrast to unstructured sparsity, structured sparsity can easily maintain high utilization by combining multiple processing tiles with fixed sparsity levels, without the need for intricate load-balancing techniques. Similarly, as shown in Figure 3(j), bit-level structured sparsity enables simpler hardware implementation than those for unstructured sparsity, as bit-column sparsity parsers can skip zero bits vector-wise.

The performance impact of the above techniques can again be reflected in the virtual throughput roofline, and compared to that of cores optimized for unstructured sparsity (Figure 5). The baseline shown in Figure 5(a) represents the roofline for unstructured weight sparsity processed on an accelerator optimized for this sparsity type. Compared to the unstructured activation sparsity roofline in Figure 4(a), the predeployment knowledge of the model's sparsity enables a lower compute overhead. Indeed, the load-balancing challenge in the compute-bound regime can be attenuated by extracting the sequence of weights to skip directly at compile time. Moreover, higher sparsity levels can be attained in some classical models through weight pruning techniques without incurring a significant accuracy degradation (e.g., down to a 10% density in VGG-16's or ResNet50's last layers [13]). Nonetheless, the initial overhead on virtual throughput remains significant, especially in the memory-bound regime.

Structure-optimized DNN processors leverage the better regularity of structured sparsity to mitigate the initial overhead of their unstructured counterpart, as shown in Figure 5(b). In the memory-bound regime, the use of *N:M* compression techniques pull the sparsity turning point significantly up at constant bandwidth. In the compute-bound regime, improvements are also observed at constant PE array size. Although lesser here, their absolute value depends on the underlying implementation of the zero-skipping and load-balancing techniques (Figure 3). Nevertheless, the conclusion remains valid: At a fixed level of sparsity, DNN cores exploiting structured sparsity outperform those supporting unstructured sparsity for a same array size. Moreover, the much lower design complexity of structured approaches allows the ability to drastically scale up the size of their MAC array without dramatically raising the hardware complexity. This makes structured-optimized processors especially appealing to handle low-to-moderate sparsity levels with very high parallelism [18], [30] . While unstructured-optimized processors remain a suitable choice to leverage high model sparsity in models and layers that show this property, one must realize that the high-throughput benefits of a few sparse layers can end up being masked by the significant overheads of denser layers. Altogether, these points suggest that structured-optimized processors make a more complete and reliable compromise.

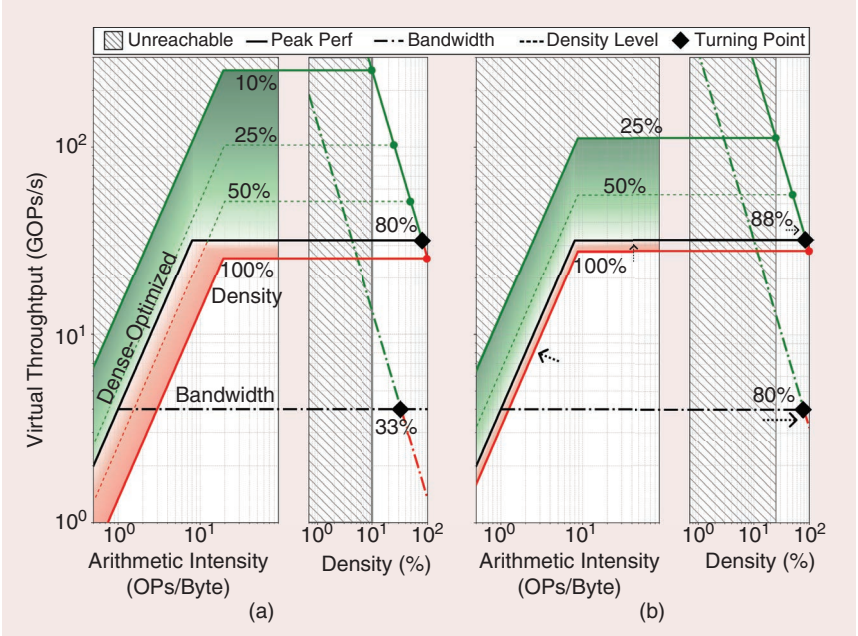

FIGURE 5: Virtual roofline representation of two different accelerator cores, respectively exploiting (a) unstructured spatial and (b) structured spatial model sparsity. The 33% memory-bound turning point in (a) is identical to that in Figure 4(a), as the same CSR compression is assumed. The 80% memory-bound turning point in (b) results from the 25% overhead of using a 2:4 sparse storage format over a dense representation [18]. The compute-bound turning points are derived from hardware overheads in [40].

WHAT ABOUT TRANSFORMER MODELS?

Hardware implications of sparsity in transformers:

- *Unstructured sparsity:* In contrast to DNNs, transformer-based models, among which large language models (LLMs), initially demonstrated minimal activation sparsity, primarily due to the adoption of Gaussian error linear units [S4] or Sigmoid-weighted linear units [S5] activation functions. Yet, recent research [12] has unveiled significant potential for sparsity by reintroducing rectified linear units in the transformers architectures. Remarkably, more than 90% activation values exhibit sparse characteristics in the feed-forward layer. As illustrated in Figure S2(a), once the activation (A) is zero, it can effectively skip the associated computation and transmission of the entire weight (W) chunk (in grey), directly translating to computational efficiency. Additionally, transformer-based LLMs showcase weight sparsity through unstructured parameter pruning techniques. Methods like Wanda [S6] employ sophisticated algorithms to estimate model weight importance, strategically removing noncritical weights to enhance random value-level sparsity up to 50% with minimal accuracy drop.
- *Structured sparsity:* Contemporary research extends beyond unstructured approaches, exploring structured sparsity to optimize transformers deployment efficiency [S7]. This involves implementing sparsity-aware training methodologies. Notably, the 2:4 density-bound sparsity can be introduced for LLMs as well [S8], achieving a 50% reduction in computational complexity while preserving model performance. Recent literature has also investigated structured bit-level sparsity to further minimize memory and datapath costs during transformers deployment. For instance, Anda [S9] leverages activation redundancy to bypass more than 50% ineffectual bit-block computations and memory footprints.

The exploration of unstructured/structured activation and weight sparsity in transformers, whether at the value or bit level, presents a promising avenue for optimization. These techniques can be synergistically combined with various hardware approaches, illustrated in Figure 3 and Table 1, to significantly enhance transformer performance and computational efficiency.

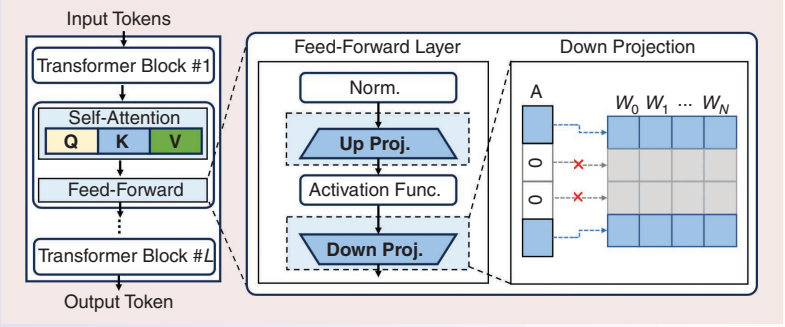

FIGURE S2: (a) Transformer-based architecture and (b) activation sparsity in down projection.

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While the discussion in this article focused mainly on vanilla multilayer perceptrons and DNNs, the same classes of sparsity techniques can also be exploited in modern transformer-based AI workloads (see "What About Transformer Models?"), such as large language models.

Conclusion and Perspectives

Sparsity is a powerful and intrinsic characteristic of AI workloads that offers potential for enhancing computational efficiency through specialized hardware architectures. While the promise of performance gains is compelling, careful assessment is still crucial to understand the actual benefits under a given sparsity level and associated hardware overheads. The introduced virtual roofline model enables such a holistic view toward an effective hardware–software codesign. In addition, an emerging research direction focuses on sparsity-aware hardware modeling and design space exploration [48], [49], aiming to analyze the complex tradeoffs in more detail and develop new computational strategies. Going forward, we observe a growing trend of increasingly combining multiple types of structured and unstructured weight/activation sparsity within flexible architectures, aiming to maximize utilization in large MAC arrays to sustain the scaling laws of modern AI workloads.

Acknowledgment

This work was cofunded by the European Research Council under Grant Agreement 101088865, the Flanders AI Research Program, KU Leuven, Prophesee, and by the Dutch government as an High-Tech Systems and Materials-TKI project. Man Shi, Adrian Kneip, Nicolas Chauvaux, and Jiacong Sun are co-first authors, with equal contributions. Man Shi is the corresponding author.

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