Systematic Distortion Analysis for MOSFET Integrators with Use of a New MOSFET Model

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Abstract— **Distortion in MOSFET-based (fixed-capacitance) continuous-time integrators is analyzed. To make the analysis general, the integrators are subdivided into four classes. Almost all the possible MOSFET integrators fall into one of these classes, the rest is mixed class. It is shown that integrators from the same class have the same distortion characteristics. A new method to describe and measure distortion is introduced. Measurement results for the four classes are presented, and for some classes they are explained with a simple MOSFET model. As not all results can be explained this way, a new, highly accurate MOSFET model is introduced. A hint at designing optimal MOSFET's is given. Finally, it is explained how the distortion characteristics of stages with different MOSFET's that all contribute to distortion can be determined.**

I. Introduction

SINCE the very beginning of active RC-filter design, these filters were used in situations where coils—or inductances—were to be avoided. First, in discrete realizations, this happened if very low pole frequencies were wanted [1], [2]. Nowadays, in integrated realizations, inductances are so badly realizable that they are practically not used at all.

An early application of integrated filters was video circuits [3], [4], and it still is [5]. Other applications are audio circuits [6], intermediate-frequency filters [7], and disk-drive read channels [8], [9].

Especially in audio and intermediate-frequency applications it appears that the dynamic range of integrated continuous-time filters is barely sufficient or even insufficient. The dynamic range of a circuit is defined as the ratio of the maximal and minimal signal level it can handle without clipping effects. In high-quality audio circuits, a dynamic range of 80–100dB is wanted, while in intermediate-frequency filters of high-quality radio circuits a dynamic range of 120dB is wanted [10]. This implies that it is difficult, if not impossible, to meet the requirements of audio and intermediate-frequency circuits with integrated filters.

The same problem exists for another measure of dynamic range, namely *distortion-free dynamic range*. This measure is based on the observation that a high-level signal can cause the filter to generate distortion products, while the signal level still falls within the dynamic range of the filter. This is especially unwanted in intermediate-frequency filters because it is possible that, via intermodulation distortion, two strong signals just outside the passband of the filter are responsible for a distortion product within the passband, which can interfere with a weak signal present there to be processed. The distortion-free dynamic range is the ratio of the largest and the smallest signal level the circuit under consideration can handle, where the distortion products are to remain below the noise level. The smallest signal level the circuit can handle is usually also taken to be equal to the noise level.

To maximize the distortion-free dynamic range, the noise level, as well as the distortion level, must be minimized. In this article we only handle the distortion aspect of distortion-free dynamic range.

An important, although indirect, reason why integrated filters suffer from distortion is that it is necessary to make these filters electronically tunable in order to be able to cope with component tolerances by an on-chip automatic tuning system [11], [12]. For that end, the integrators are made tunable, so that they should contain at least one tunable component. In practice it appears that tunable components for integrators inherently are non-linear and thus give rise to distortion.

There are many techniques available to cope with the non-linearities of tunable components. Many modern techniques to realize integrated linearized tunable integrators are based on MOSFET technology. But as, even within the restrictions of this category, a large amount of different tunable integrator circuits that have different distortion characteristics have been proposed, and nowhere has a clear statement on the relative merits of these proposals been made, it is unclear which technique gives the best results. Therefore we opt for a systematic approach, in which it is possible to determine what type of integrator can best be used for a maximal distortion-free dynamic range in a specific situation.

For that end, we first show how integrators can be realized and classified into four classes, such that circuits of the same class have similar distortion properties. Subsequently, we discuss how distortion can be characterized and measured, and measurement results are given. On the basis of these results one can choose for one of the four integrator classes for use in conjunction with an IC-process. The measurements are compared to the results from existing MOSFET models, and a new, more accurate model is introduced. We draw some conclusions, in which a hint is given at the design of optimal low-distortion MOSFET's with use of the new model and applications in high distortion-free dynamic range integrators. We end with showing how the distortion of more complex circuits can be determined from the characteristics of the

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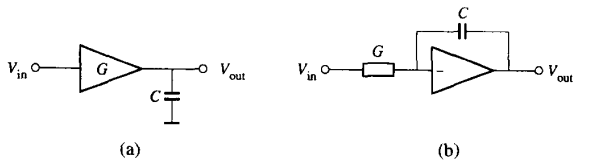

Fig. 1. Integrators consist of a capacitor that is driven by an admittance part. In (a) the admittance part is a transadmittance stage; in (b) it is a conductance, and the capacitor is situated in the feedback path of an opamp.

basic circuits. In this way, also multiple-class circuits can be handled.

In order to save space, lengthy mathematical proofs are omitted. These are included in a Ph.D. thesis [13], where also noise is taken into consideration.

II. Integrators

In another article [14] it is shown that an integrator always consists of an admittance part and a capacitance part. This is demonstrated in the examples of Fig. 1.

The admittance part realizes a voltage-to-current conversion. In the frequency domain, it ideally has a real-valued transfer function G. In Fig. 1(a) the admittance part of the integrator is realized as a transadmittance stage. In Fig. 1(b) it is realized as a conductor. We will call a transadmittance stage as used in Fig. 1(a) an *active* admittance, and an admittance as used in Fig. 1(b) a *passive* admittance. The examples of this figure are representative for all possible integrators. If the capacitor value is C, the time constant of these integrators is C/G.

If the integrator must be tunable, it must have a tunable time constant, so C or G must be tunable. In a modern MOS process, high-quality MOS capacitances with a high linearity can be realized, but these capacitances are not tunable, so the admittance factor G must be tunable. Some MOSFET configuration is then used as a tunable admittance stage, and this configuration is inherently non-linear, because the MOSFET's are non-linear.

Therefore, in practice, the admittance part of an MOS integrator is responsible for all the distortion which is produced by this integrator. For that reason we will focus on the realization of tunable MOSFET admittance stages. Because, in principle, even-order distortion can be canceled by balancing [12], we will only regard odd-order distortion in comparing the stages. In the next section we make a classification of practically all possible admittance stages into four classes.

III. MOSFET Admittances And Integrators

In a MOSFET transadmittance stage there are some devices (or one device) that do the real job of converting a voltage to a current. We refer to these devices as the *kernel devices* of the stage. The other devices are generally meant for biasing or buffering. According to how the kernel devices are used, the stage can be classified. We assume that the frequencies of interest are low, so that the drain current and the source current differ only by sign, and that the gate current is zero. We also assume that the devices under discussion are of the n-channel type, unless stated otherwise.

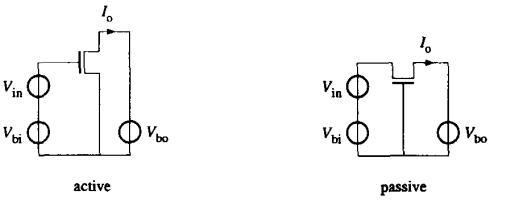

Fig. 2. MOSFET admittance stages can be classified as active or passive stages.

Since the admittance stage must deliver a current at its output, the output node of the kernel device must be the drain or the source, but not the gate. The input node of this device is one of the remaining two nodes. If the input node is the drain or the source, the output current is delivered by the input voltage source (possibly via a voltage buffer), and therefore the device is used passively, as explained in Section II. If, on the other hand, the input node is the gate, the output current enters the drain or the source from the power supply, and the device is used actively. In this way, we can classify the admittance stages as active or passive. Fig. 2 shows examples of stages of these classes, where only the kernel device is shown.

In this figure, V_{in} is the input signal voltage, and V_{bi} and V_{bo} are the input and output bias voltages.

Another classification is as to whether the kernel device is biased in the triode region or in the saturation region. The device is said to be biased in the triode region if

$$V_g > V_d + V_t \tag{1}$$

and

$$V_g > V_s + V_t \tag{2}$$

where V_g, V_d, and V_s are the gate, drain, and source voltages, respectively, and V_t is the threshold voltage—otherwise the device is biased in the saturation region. In Fig. 2, the bias region is dependent on the values of V_{bi} and V_{bo}.

The above-mentioned two classifications give rise to four classes of MOSFET admittance stages, and in that way to four classes of MOSFET integrators. In the rest of this section we discuss some examples of these four classes of integrators, in order to offer an idea of how these look like, and to discuss some properties.

A. Passive-Triode Integrators

In passive-triode integrators the MOSFET is used as a tunable resistor. An equivalent resistor is present between the source and the drain connection of the transistor. The voltage at the gate is used to tune the resistor. A very simple MOSFET model for the triode region is [15]

$$I_d = \frac{W}{L}\mu C'_{ox}\left[(V_{gs} - V_t)V_{ds} - \frac{1}{2}V_{ds}^2\right] \tag{3}$$

in which W and L are the effective width and length of the device, μ is the effective electron mobility, C'_{ox} is the gate capacitance per unit area, and V_{gs} and V_{ds} are the gate and drain voltages with respect to the source. From this model, it

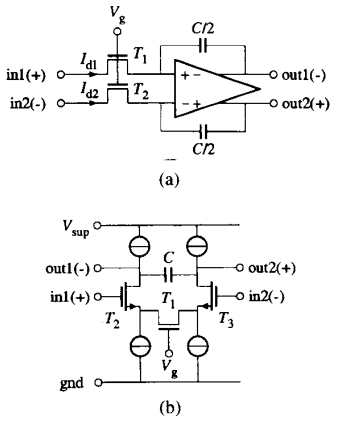

Fig. 3. Two examples of passive-triode integrators. Integrator (a) has been realized around an opamp.

can be seen that the equivalent resistor is non-linear, and that the non-linearity is second order. Therefore the resistor can be linearized by balancing. Two examples of a thus linearized passive-triode integrator are shown in Fig. 3.

The integrator of Fig. 3(a) is realized around an opamp and has been used by Banu and Tsividis [6]. The integrator of Fig. 3(b) was used by Tsividis *et al.* [16], Kaiser [17] and Gopinathan *et al.* [5]. The kernel devices in Fig. 3(a) are T_1 and T_2. In Fig. 3(b) the kernel device is T_1, provided that the transconductance parameter of T_2 and T_3 is very large compared to the conductance of T_1. Under this assumption, it can be proved that the distortion characteristics of these two integrators are identical. An outline of the proof is given below, for a more accurate proof, see [13].

Due to the high gain of the opamp, one can assume that its two inputs have the same voltage. It can be proved that the non-linear transfer function of this integrator is independent of this voltage [18]. Therefore, T_1 and T_2 act as if they were connected in series. They effectively form one transistor, which behaves similar to the kernel device in Fig. 3(b). The non-linear behavior of the two integrators of Fig. 3 is therefore identical.

A similar argument holds for other balanced passive-triode integrators. Therefore we may state that *all balanced passive-triode integrators have the same distortion characteristics, provided that the kernel devices are similar.* Similar kernel devices means that they have the same device parameters and bias voltages.

B. Active-Triode Integrators

Active-triode integrators have been proposed by Pennock [19] and Wong [20]. These two propositions have the same principle of operation and distortion characteristics, so that it is sufficient to discuss the circuit of Fig. 4, which represents a single-ended version of the differential implementation by Wong. The kernel device of this integrator is T_1. This device is biased by a current source I_b and a voltage source V_b. This voltage can be used to tune the stage. The device is to be biased in the triode region. By (3) with $V_{ds} = V_b$, the drain current

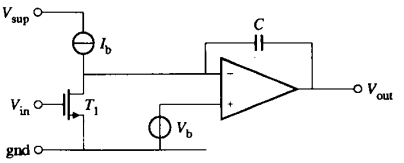

Fig. 4 An opamp-based implementation of an active-triode integrator.

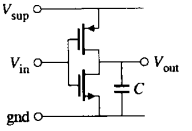

Fig. 5. A simple active-saturation integrator.

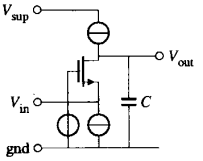

Fig. 6 A simple unbalanced passive-saturation integrator. The current source in the source of the transistor is necessary if the input signal source cannot handle the input bias current.

has a linear dependence on the input voltage, so according to this model there is no distortion. Distortion enters the picture if mobility reduction is regarded, as we will see shortly.

C. Active and Passive Saturation Integrators

A simple MOSFET model for the saturation region is [15]

$$I_d = \frac{1}{2}\frac{W}{L}\mu C'_{ox}(V_{gs} - V_t)^2. \tag{4}$$

The transfer of this stage is quadratic of nature, and therefore distortion products are mainly second order. In order to cancel this type of distortion, saturated integrators must be balanced.

An example of an active-saturation integrator is shown in Fig. 5. This type of integrator is used by Nauta and Seevinck [21].

In a *passive*-saturation integrator, on the other hand, the input node is the source of the kernel device. The drain end of the channel is saturated. This type of transconductor has been proposed by Wang [22]. A simple example of an unbalanced version of a passive-saturation integrator is shown in Fig. 6.

Now that we have classified MOSFET integrators by their admittance stages, we proceed by considering the distortion properties of these admittance stages.

IV. Distortion

In this section we characterize the distortion of admittance stages that belong to one of the classes described in Section III, and as a first step we describe the distortion of stages with only one kernel device. From these results it is possible to determine the properties of admittance stages with more than one kernel device, which is discussed in Section VIII.

First, a figure of merit, which we use to characterize the distortion of integrators, is introduced. Then a distortion measurement setup is described, and measurement results for each of the four integrator classes are given.

A. Measures

Only second and third order distortion is handled because in practice these two are the most important to determine the distortion-free dynamic range. The integrator is modeled as a distortion-free integrator with a distorted signal at its input. If the input signal voltage of the integrator is V_{in}, the distorted input signal V'_{in} is modeled as

$$V'_{\text{in}} = V_{\text{in}} + k_2 V_{\text{in}}^2 + k_3 V_{\text{in}}^3. \tag{5}$$

This equation defines the second and third order distortion coefficients k_2 and k_3 that play a central role in this work. From this equation it can also be made clear how one can intuitively interpret these coefficients. The dimension of $|k_2|^{-1}$ and $|k_3|^{-1/2}$ is Volt. $|k_2|^{-1}$ and $|k_3|^{-1/2}$ are the input signal amplitudes for which the second and third order distortion products have the same magnitude as the input signal. Therefore we call these voltages the (second and third order) intercept voltages. The higher these voltages, the less distortion the stage produces. In this way, $|k_2|^{-1}$ and $|k_3|^{-1/2}$ give a very direct idea of the distortion properties of a circuit.

If the output current of the transadmittance part of the integrator is I_{out}, its transadmittance factor is $G = dI_{\text{out}}/dV_{\text{in}}$ for $V_{\text{in}} = 0$. This gives with (5):

$$I_{\text{out}} = G(V_{\text{in}} + k_2 V_{\text{in}}^2 + k_3 V_{\text{in}}^3). \tag{6}$$

Differentiating this equation two, respectively three times yields

$$k_2 = \frac{\dfrac{d^2 I_{\text{out}}}{dV_{\text{in}}^2}}{2\dfrac{dI_{\text{out}}}{dV_{\text{in}}}} \tag{7}$$

$$k_3 = \frac{\dfrac{d^3 I_{\text{out}}}{dV_{\text{in}}^3}}{6\dfrac{dI_{\text{out}}}{dV_{\text{in}}}}. \tag{8}$$

These equations can be used to determine distortion from measurements, as described in Section IV-C.

B. Harmonic Distortion

In practice, distortion is often described with harmonic distortion measures. The second and third order harmonic distortion measures HD_2 and HD_3 can be determined with elementary trigonometry from (5). If V_{in} is a sine wave with amplitude V_{A}, we get:

$$\text{HD}_2 = \frac{1}{2} k_2 V_{\text{A}} \tag{9}$$

$$\text{HD}_3 = \frac{1}{4} k_3 V_{\text{A}}^2. \tag{10}$$

From these expressions, we see what we already knew, namely that the harmonic distortion is dependent on the signal amplitude. This is one of the reasons why harmonic distortion is a measure that does not suit our methods very well, and we prefer to use k_2 and k_3 instead. With (9) and (10), it is easy to calculate the harmonic distortion figures from k_2 and k_3. The numerical values of $k_2/2$ and $k_3/4$ can be thought of as the HD_2 and HD_3 for a 1V-amplitude input signal.

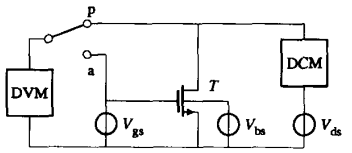

Fig. 7 The distortion measurement setup for MOSFET's. The gate voltage (for an active configuration) or the drain voltage (for a passive configuration) is measured with a digital voltage meter (DVM). The drain current is measured with a digital current meter (DCM).

C. Measurements

The determination of the distortion figures k_2 and k_3 of a transadmittance stage from measurements is straightforward. A programmable DC-voltage source is connected to its input, and a DC-current meter is connected to its output. The input voltage is stepped over the range of interest, and for each value of the input voltage the output current is measured. Then by numerical differentiation, and by (7) and (8), k_2 and k_3 are obtained. This method is much simpler, and gives much more information about the stage than the conventional AC-based methods do, as we will see further on.

Because in first instance we look at transadmittance stages with only one kernel device, it is sufficient to characterize only one MOSFET that is biased in one of the classes of Section III.

Fig. 7 shows the essence of the measurement setup. The reference node is the source, and with programmable voltage sources the voltages at the drain, gate, and the bulk can be controlled. In this way the MOSFET can be biased into any of the classes. One of the voltage sources is used as input source and is swept over the range of interest. The input voltage and the output current are measured with digital meters. A central computer controls the sources and reads the meters.

The measurements that are presented here are done on an n-channel MOSFET with $W = 10\mu\text{m}$ and $L = 20\mu\text{m}$. The results apply to a situation where the supply voltage is 8V. Fig. 8 shows the intercept voltages $|k_2|^{-1}$ and $|k_3|^{-1/2}$ for the active-triode case with $V_{\text{ds}} = 0.5\text{V}$. The peaks in the third-order plot indicate bias points where k_3 is zero. In these regions there is no third-order distortion. This phenomenon can be utilized to realize very low distortion integrators, but for the device under consideration the gate-source voltage must be about 6V to bias it in this region, so that the supply voltage must be approximately 12V, which may not be practical.

The intercept voltages for the active and passive saturation case are plotted in Fig. 9. The differences between these cases arise from the body effect.

The measured intercept voltages for the passive-triode case, with $V_{\text{gs}} = 4\text{V}$ and $V_{\text{bs}} = -4\text{V}$ are shown in Fig. 10.

Comparing the stages for normal bias conditions ($V_{\text{gs}} = 4\text{V}$ in all cases, and $V_{\text{ds}} = 0\text{V}$ for the passive-triode case), we

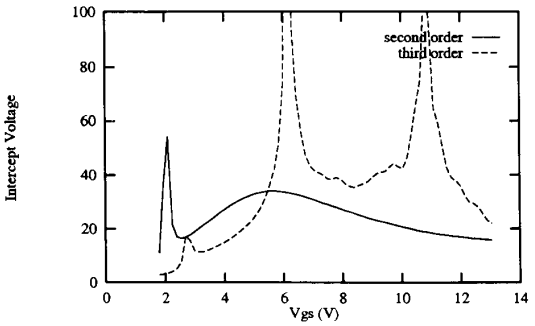

Fig. 8 Measured active-triode second and third order intercept voltages plotted against the gate-source voltage.

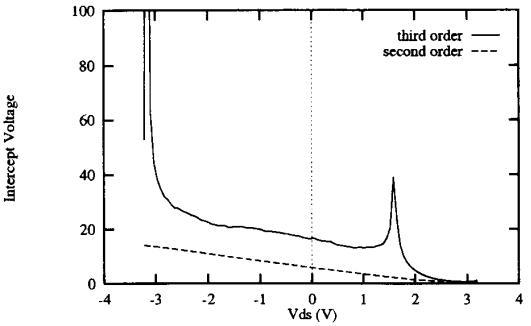

Fig. 10. The measured intercept voltages for the passive-triode configuration.

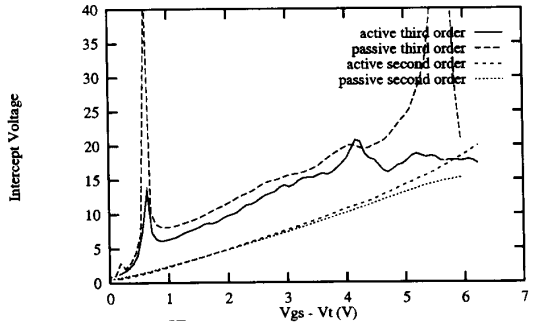

Fig. 9. Intercept voltages for the active and passive saturation case, plotted against $V_{gs}-V_t$. For the passive configuration, $V_{gb} = V_{db} = 8$V was chosen.

see that the active-triode stage has the least distortion with $|k_3|^{-1/2} = 17.4$V. For the passive-triode class, the active-saturation class, and the passive-saturation class, this is 16.5V, 14.9V, and 10.0V, respectively. These values are not very different from each other, except for the latter. Differences can get much larger for other supply voltages, as we saw for instance in the active-triode case with a supply voltage of 12V, or if the MOSFET is optimized, a possibility that is discussed later.

V. Improving Model Accuracy

When the MOSFET models of (3) and (4) are used to determine k_2, one obtains

$$|k_2| = \frac{1}{2(V_{gs} - V_t)} \tag{11}$$

for the saturation classes,

$$k_2 = \frac{-1}{2(V_{gs} - V_t - V_{ds})} \tag{12}$$

for the passive-triode class, and

$$k_2 = 0 \tag{13}$$

for the active-triode class. Except for the last one, these values are fairly accurately in accordance with measurement results. Therefore we will not discuss these values any further in connection with more accurate models.

For k_3 one finds zero for all the classes. This is not in accordance with the measurements, so we try to find more accurate models that enable us to predict third-order distortion for all classes and second-order distortion for the active-triode class. As a first step, we extend the simple model of (3) and (4) with two important phenomena that give rise to distortion, namely the body effect and mobility reduction.

The body effect is incorporated by substituting a bias-dependent threshold voltage

$$V_t(V_{sb}) = V_{t0} + \gamma(\sqrt{V_{sb} + \phi_b} - \sqrt{\phi_b}) \tag{14}$$

into (3) or (4). In this expression, V_{sb} is the source-to-bulk voltage, V_{t0} is the zero-backgate-bias threshold voltage, γ is the body-effect coefficient, and ϕ_b is the surface potential for strong inversion.

The electron mobility μ in (3) and (4) is not constant, but dependent on the normal gate-induced electric field in the channel, which is dependent on the gate-source voltage V_{gs}. The following empirical model for the dependence of the mobility on the gate-source voltage is often used (see, for instance [23]).

$$\mu(V_{gs}) = \frac{\mu_0}{1 + \theta(V_{gs} - V_t)} \tag{15}$$

In this equation, θ is an empirical constant with dimension V^{-1}.

To include both the body effect and mobility reduction, (14) and (15) are substituted into (3) or (4), whichever appropriate. This model is very similar to the one Patterson and Shoucair [24] used, and we will see later that the results obtained with our model are similar to the results they obtained, as far as we can compare them. An optimal fit of our model to the above measurements on an n-channel MOSFET gave $\mu_0 C'_{ox} = 5.6 \cdot 10^{-5}$A/V^2, $\gamma = 0.355\sqrt{\text{V}}$, $V_{t0} = 0.766$V, and $\theta = 0.0503\text{V}^{-1}$. With these parameters, this model can be used for a fairly accurate prediction of the drain current. We will determine now if distortion can be characterized with this model.

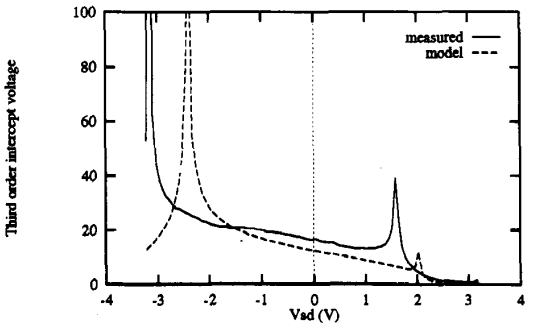

Fig. 11. The third-order intercept voltage for the passive-triode configuration, as a function of V_{sd}, with $V_{gd} = 4V$ and $V_{db} = 4V$, determined from measurements and from a standard model.

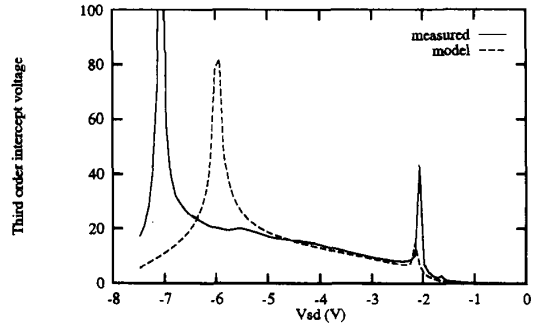

Fig. 12. Third-order intercept voltages for the passive-saturation class with $V_{db} = V_{gb} = 8V$.

A. Passive Triode

If the above-derived model is used for the passive-triode case, with the source as input node, the drain current is predicted with an inaccuracy of 3%. With this model and (8), k_3 is found:

$$k_3 \approx \frac{-1}{V_{gs} - V_t}\left(\frac{\theta}{2} - \frac{\gamma}{12(V_{sb} + \phi_b)^{3/2}}\right). \tag{16}$$

From this equation it can be seen that distortion due to the body effect and due to mobility reduction tend to cancel. This is visible in Fig. 11 where $|k_3|^{-1/2}$ as determined numerically from measurements and the model are compared with $V_{gd} = 4V$ and $V_{db} = 4V$. It appears that, according to the measurements and the model, there is a peak in this plot, where $k_3 = 0$ and the two distortion mechanisms cancel. At the left side of the peak the body effect is dominant, and at the right side of the peak mobility reduction is dominant.

Usually, it is desired to bias the transistor at $V_{sd} = 0$, for that yields a maximal signal sweep and a minimal $1/f$-noise level [15]. If this is done, the transistor is biased in a region where the dominant distortion mechanism is mobility reduction. The distortion due to this mechanism is partially canceled by the body effect. This observation leads us to a very important conclusion, namely that it is unwise to use configurations in which distortion due to the body effect is annihilated [25], for this will *increase* the total distortion level.

The other peak at $V_{sd} = 1.7V$ marks the transition from the triode region into the saturation region.

B. Passive Saturation

The measurements and simulations for the passive-saturation class were performed with $V_{gb} = V_{db} = 8V$. Discrepancies between the measured and predicted drain current were mainly due to a 0.6V mis-estimation of the threshold voltage at $V_{sb} = 8V$, and this has no influence on the predicted distortion. The third-order intercept voltages from measurements and the model are shown in Fig. 12 as a function of V_{sd}.

It can be proved from the model that

$$k_3 \approx \frac{1}{2(V_{gs} - V_t)}\left(-\theta + \frac{\gamma}{6(V_{sb} + \phi_b)^{3/2}}\right) + \frac{\gamma}{16(V_{sb} + \phi_b)}. \tag{17}$$

From Fig. 12 and from (17) we see that, just as in the passive-triode case, distortion effects due to the body effect and due to mobility reduction tend to cancel. Complete cancellation occurs if $V_{sd} = -7V$, or $V_{sb} = 1V$. At lower values for V_{sb} the body effect is dominant, but such a low value for this voltage limits the maximal signal level at the source of the MOSFET and thus results in a very low dynamic range. Therefore, at practical values for the bias voltages, mobility reduction is dominant in third-order distortion.

C. Active Triode

The model has been compared for the active-triode region with measurements, with $V_{sb} = 0V$, $V_{db} = 0.5V$, and $0\,V < V_{gs} < 15\,V$, so that also a small trajectory in the saturation region was covered. In the triode region the inaccuracy with which the drain current was predicted was 1%. In the small saturation part of the trajectory the inaccuracy was 3%.

As in the active-triode region the voltages at the drain and the source are constant, the body effect has, at least according to the model under consideration, no influence on the distortion that is produced by the stage. The distortion originates from mobility reduction only. Via (7) and (8), one obtains

$$k_2^{-1} = -\theta^{-1} - (V_{gs} - V_t) \tag{18}$$

$$k_3^{-1} = (\theta^{-1} + (V_{gs} - V_t))^2. \tag{19}$$

A remarkable result is that, according to this model, $|k_2|^{-1}$ and $|k_3|^{-1/2}$ are equal. In Fig. 13, these values are compared with corresponding values from measurements, as a function of V_{gs}. It is clear from this comparison that the model is inadequate to foretell the distortion, especially the third-order distortion, for the active-triode class.

D. Active Saturation

The inaccuracy of the model for the active-saturation class is about 4% for values of V_{gs} above 2V. Below this value the inaccuracy is higher. Fig. 14. shows a comparison of the third-order intercept voltages from measurements and from the model, for $V_{sb} = 0V$ and $V_{db} = 8V$. It must be rated a piece of

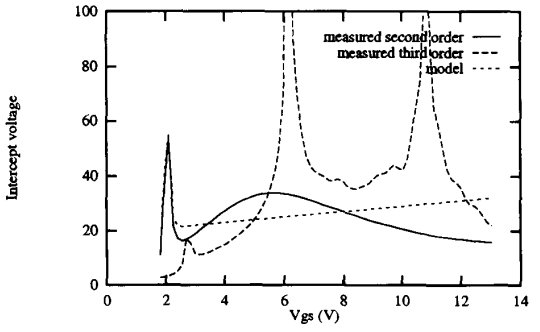

Fig. 13. Second and third order intercept voltages for the active-triode class as a function of V_{gs}, according to a standard model and measurements, with $V_{sb} = 0V$ and $V_{db} = 0.5V$. According to the model, the second and third order intercept voltages are equal, so as far as the model is concerned, only one value is shown.

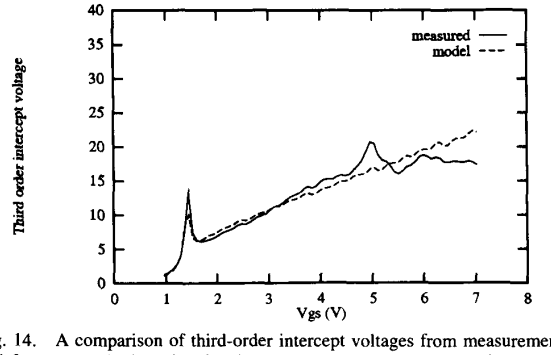

Fig. 14. A comparison of third-order intercept voltages from measurements and from a standard model, for the active-saturation class, as a function of V_{gs}. These data refer to a situation with $V_{sb} = 0V$ and $V_{db} = 8V$.

chance that with a simple model like this, third-order distortion for this class can be determined in a reasonably accurate way.

For the same reason as for the active-triode class, distortion cannot originate from the body effect, and is mainly due to mobility reduction. With the model and (8), it can be shown that for this class

$$k_3 = \frac{-\theta}{(2+\theta(V_{gs}-V_t))(1+\theta(V_{gs}-V_t))^2(V_{gs}-V_t)} \approx \frac{-\theta}{2(1+\theta(V_{gs}-V_t))^2(V_{gs}-V_t)}. \quad (20)$$

E. Discussion

In this section we modeled distortion with a relatively simple model with an inaccuracy of typically 3%. We saw that even with this simple model second and third order distortion for MOSFET stages with one kernel device can be reasonably accurately determined, except for the active-triode class.

The most important conclusion of this section is that in all cases mobility reduction is the dominant distortion mechanism. This is a remarkable result, for it is often assumed that the body effect is the main cause of distortion in MOSFET integrators [12], [18], [25]. In active stages mobility reduction is even practically the only distortion mechanism. In passive stages, the body effect also plays a role, but it tends to cancel distortion due to mobility reduction, and therefore one should *not* use a configuration in which body-effect distortion is annihilated.

These results seem to be consistent with results from Patterson and Shoucair [24], who used a model that is very similar to the one we used in this section. It was extended for short-channel devices, which we will not do. They applied their model to the passive-triode case and found distortion levels that compared favorably to measurement results. Their result also indicate that mobility-reduction distortion is stronger than body-effect distortion, and that the two tend to cancel.

Because the model we used up to now, as well as Patterson and Shoucair's, is inadequate to describe distortion for the active-triode case we will develop in the next section a new and more accurate model with which distortion in this class can be accurately modeled, and with which the distortion for the passive classes is also modeled more accurately.

VI. More Accurate MOSFET Models

The model that was developed in Section V was in a number of cases adequate to determine second and third order distortion levels, and to offer an insight into the relative importance of different distortion-producing mechanisms. However, with this model the distortion of an active-triode stage could not be predicted correctly, and that is why we develop a better model in this section.

A. Charge-Sheet Model

An accurate model is obtained when the charge distribution in a MOSFET is taken into consideration. In the so-called charge-sheet model, it is assumed that the charge regions in the transistor are infinitesimally thin. The drain current is found as follows [15].

$$I_d = \frac{W}{L}\int_{V_{sb}}^{V_{db}} \mu\,|Q_i'|\,dV_{cb} \quad (21)$$

The inversion charge per unit area Q_i' that appears in the integral is a function of the channel-to-bulk voltage V_{cb}, and can be modeled as [15]

$$Q_i' = -C_{ox}'\left(V_{gb} - V_{fb} - \phi_b - V_{cb} - \gamma\sqrt{\phi_b + V_{cb}}\right) \quad (22)$$

where V_{fb} is the flat-band voltage, which is dependent on the fabrication details of the MOSFET, but not on the bias conditions.

Apart from the (mobile) inversion-layer charge, there is an immobile depletion-layer charge, usually referred to as the bulk charge. The total amount of bulk charge per unit area is denoted as Q_b', and equals:

$$Q_b' = -\gamma C_{ox}'\sqrt{\phi_b + V_{cb}}. \quad (23)$$

The bulk charge and the inversion-layer charge give rise to a normal electric field in the inversion layer. The effective absolute value of this electric field is [15]

$$|E_{eff}| = \frac{1}{\epsilon_0\epsilon_{Si}}\left|\frac{1}{2}Q_i + Q_b\right| \quad (24)$$

where ϵ_0 is the vacuum permittivity, and ϵ_{Si} is the relative permittivity of silicon. The electron mobility in the inversion layer is reduced by the existence of this electric field. In this way the following empirical relation between the electron mobility in the inversion layer and the charge densities in the transistor is found:

$$\mu = \frac{\mu_0}{1 + \frac{\theta}{C'_{ox}}|Q'_i + 2Q'_b|} \tag{25}$$

where μ_0 is the inversion-layer mobility in absence of an electric field, and θ is an empirical constant. (25) is more accurate than (15); it especially reflects the dependence of the mobility on the bulk voltage correctly [26]. Still, when the above model is used, the distortion that is predicted with it for the active-triode case is essentially the same as shown Fig. 13, so for this case this model is not better than the model of Section V. The dependence of the mobility on the terminal voltages or the charge densities in the transistor still needs to be better modeled.

B. Mobility-Reduction Mechanisms

Several mechanisms that reduce the electron mobility in the inversion layer can be distinguished. If each mechanism, when considered on its own, gives rise to a mobility μ_i, the mechanisms can be combined to obtain the effective mobility μ_{tot} with Mathiessen's rule [27]:

$$\frac{1}{\mu_{tot}} = \sum_i \frac{1}{\mu_i}. \tag{26}$$

In the first instance, there are two mobility-reduction mechanisms that need to be considered at room temperature, namely due to surface roughness and phonon scattering [28].

The phonon-scattering mobility can be approximated as [28]:

$$\mu_{ph} = \beta |E_{eff}|^{-1/3} \tag{27}$$

and due to surface roughness:

$$\mu_{sr} = \nu |E_{eff}|^{-2.1} \tag{28}$$

where β and ν are constants, and $|E_{eff}|$ is given by (24). When these mobility-reduction mechanisms are combined with the zero-field bulk mobility μ_0 by (26), and the resulting effective mobility is substituted with (23), (22) into (21), a MOSFET model is obtained, but it still appears that with this model the distortion characteristics shown in Fig. 8 can not be explained. Therefore, a new feature is to be added to the model.

C. A Semi Charge-Sheet Model

In modern MOS processes a channel-implant step is done to adjust the threshold voltage. This step gives rise to a nonuniform doping concentration in the substrate: the doping concentration is dependent on the depth below the silicon surface. If this is to be taken into account, the assumption underlying the charge-sheet model, namely that the inversion layer has infinitesimal thickness, can not be used anymore. Instead, the measure in which the inversion layer extends below the silicon surface must be taken into account. The results that are obtained in this way can be condensed into some effective parameters of an equivalent charge-sheet model. Because this model has been obtained by departing from the charge-sheet assumptions, we denote it as a semi charge-sheet model. To develop it, we first revisit mobility reduction.

Mobility: Let us agree on calling the coordinate axis that points from the silicon surface perpendicularly into the silicon the y-axis, and on making $y = 0$ coincide with the silicon surface, and let us assume that the implantation doping profile is Gaussian, so that the implantation doping concentration as a function of y is expressed as

$$N_{ii}(y) = N_{iip} e^{-\frac{(y-y_0)^2}{2\rho^2}} \tag{29}$$

where y_0 is the mean implantation depth, ρ is the standard deviation of the implantation depth, and N_{iip} is the peak implantation concentration.

The electron mobility is dependent on the doping concentration, and therefore, with a nonuniform doping concentration as described above, the mobility is dependent on the depth y. The dependence of the mobility on the doping concentration can be quite complex, but because the variations in the doping concentration are not very large, we can use a first-order approximation:

$$\mu_{ii} = \frac{\mu_N}{N_{ii}} \tag{30}$$

where μ_N is a constant, and μ_{ii} is the mobility-reduction term due to the implanted impurity concentration N_{ii} alone. This term is infinite in absence of implanted impurities.

To find the effective mobility-reduction term $\mu_{ii,eff}$ due to implanted impurities, we approximate the channel as an abrupt channel. That is, we assume that the inversion charge is distributed uniformly between the silicon surface ($y = 0$) and the deepest point of the channel ($y = y_c$). Then $\mu_{ii,eff}$ is found by taking the mean of μ_{ii} over the channel depth:

$$\frac{1}{\mu_{ii,eff}} = \frac{N_{iip}}{y_c \mu_N} \int_0^{y_c} e^{-\frac{(y-y_0)^2}{2\rho^2}} dy. \tag{31}$$

The inversion-layer depth y_c (in meter) can be obtained from the combination of the classically and the quantum-mechanically estimated inversion-layer depth [29]:

$$y_c = 3.9 E_{eff}^{-1} + 5.76 \cdot 10^{-5} E_{eff}^{-1/3}. \tag{32}$$

With this equation, $\mu_{ii,eff}$, as given in (31), has become a function of E_{eff}.

Suppose that the mobility in a uniformly doped substrate with doping concentration N_A in absence of an electric field is μ_A, then by Mathiessen's rule, the total effective mobility can be found from (27), (28), and (31) as follows.

$$\frac{1}{\mu_{tot}(E_{eff})} = \frac{1}{\mu_{ph}(E_{eff})} + \frac{1}{\mu_{sr}(E_{eff})} + \frac{1}{\mu_{ii,eff}(E_{eff})} + \frac{1}{\mu_A} \tag{33}$$

Thus μ_{tot} has become a function of E_{eff} and the fabrication details of the MOSFET. E_{eff} is the only parameter that represents the bias condition in this expression.

TABLE I
PARAMETERS FOR THE MOSFET MODEL OF SECTION VI-C .

fitted			others		
parameter	value	unit	parameter	value	unit
γ	0.3125	$\sqrt{\text{V}}$	W	$1.0 \cdot 10^{-5}$	m
β	$3.0101 \cdot 10^{4}$	$\text{C}^{2/3}\text{m}/(\text{N}^{2/3}\text{s})$	L	$2.0 \cdot 10^{-5}$	m
ν	$2.3943 \cdot 10^{15}$	$\text{N}^{1.1}\text{m}/(\text{C}^{1.1}\text{s})$	ϵ_0	$8.8542 \cdot 10^{-12}$	F/m
y_0	$4.190 \cdot 10^{-8}$	m	ϵ_{Si}	11.9	
ρ	$2.503 \cdot 10^{-7}$	m	C'_{ox}	$6.9 \cdot 10^{-4}$	F/m^2
$\mu_{\text{N}}/N_{\text{iip}}$	0.18927	Cm/Ns	V_{fb}	-0.03	V
μ_{A}	$9.284 \cdot 10^{-2}$	Cm/Ns	ϕ_{b}	0.55	V

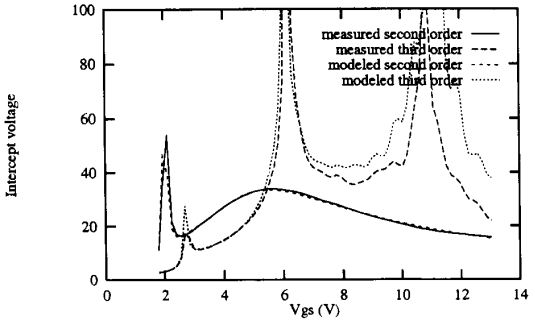

Fig. 15. The second and third order distortion figures from the model of Section VI-C for the active-triode class, compared to results from measurements. $V_{\text{ds}} = 0.5\text{V}$ and $V_{\text{bs}} = 0\text{V}$.

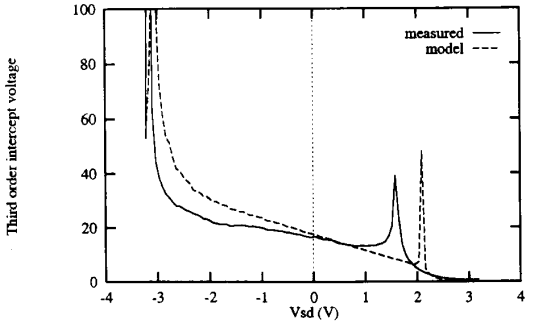

Fig. 16. Third-order distortion for the passive-triode case, according to measurements, and predicted by the model of Section VI-C. $V_{\text{gb}} = 8\text{V}$ and $V_{\text{db}} = 4\text{V}$.

Model: The drain current now is given by (21) with field-dependent mobility:

$$I_{\text{d}} = \frac{W}{L} \int_{V_{\text{sb}}}^{V_{\text{db}}} \mu_{\text{tot}}(E_{\text{eff}}) \, |Q'_{\text{i}}(V_{\text{cb}})| \, dV_{\text{cb}}. \tag{34}$$

$\mu_{\text{tot}}(E_{\text{eff}})$ is given by (33), E_{eff} by (24), and $Q'_{\text{i}}(V_{\text{cb}})$ by (22). Via (22) and (23), E_{eff} is a function of the gate voltage and V_{cb}. The model is in first instance meant for triode-region operation, but can be extended to the saturation region by substituting zero for Q_{i} if by (22) its value would become positive.

The model was fitted to the measurements for active-triode operation, and the parameter values that were obtained are shown in Table I.

The inaccuracy of this model was very low in the active-triode class: 0.03%, for $2.8\text{V} \leq V_{\text{gs}} \leq 15\text{V}$ with $V_{\text{ds}} = 0.5\text{V}$. A comparison of the second and third order distortion figures, as predicted by the model and as obtained from measurements, is shown in Fig. 15.

From these results it is clear that with this model distortion for active-triode stages can be predicted quite accurately. With this model, also the distortion figures of passive stages can be predicted more accurately than with the model of Section V. Only in the case of active-saturation stages, the distortion results are less accurate than with the model of Section V. The results for the passive-triode, the passive-saturation, and the active-saturation case are shown in the Figs. 16, 17, and 18, respectively.

Conclusion: From the comparison of the measurements with the simulations with this model we conclude that the model we developed in this section is accurate enough to predict distortion with it for all our four classes of MOSFET integrators.

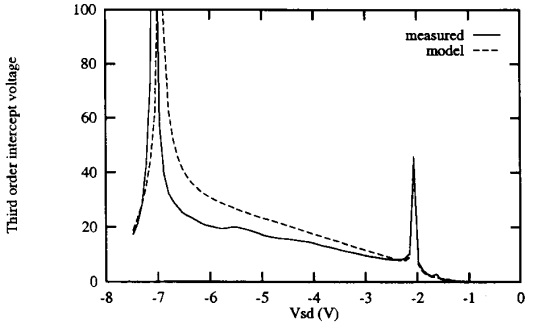

Fig. 17. A comparison of third-order distortion for the passive-saturation case, according to measurements, and to the model of Section VI-C with $V_{\text{gb}} = 8\text{V}$ and $V_{\text{db}} = 8\text{V}$.

VII. DESIGNING OPTIMAL MOSFET'S

The models we presented into Sections V and VI give insight into the various mechanisms that give rise to distortion. This insight can be used to design optimal MOSFET's for low-distortion integrators.

For example, in Section V we saw that in passive-saturation and in passive-triode integrators, the body effect and mobility reduction are the mechanisms that give rise to distortion. It appeared that mobility reduction is dominant, and that the distortion from the body effect partly cancels the distortion

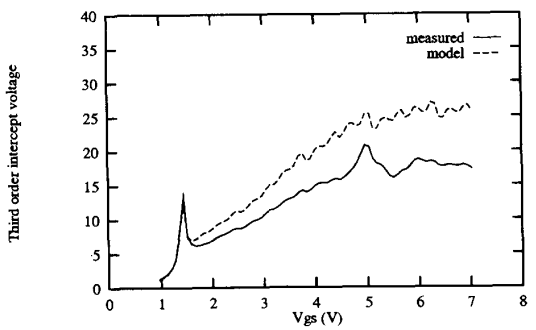

Fig. 18. Measurements of the third-order intercept voltages for the active-saturation case, compared to simulations with the model of Section VI-C , with $V_{ds} = 8V$ and $V_{bs} = 0V$.

from mobility reduction. If these two effects would cancel each other completely, there would be no third-order distortion. We saw in Section V that cancellation can occur, but under unfavorable bias conditions. In the case of passive-triode integrators, we would like to achieve cancellation if $V_{ds} = 0V$. This is possible by decreasing mobility reduction or, if this is not possible, even by *increasing* the body effect. In this way, a MOSFET can be designed to produce no third-order distortion in a passive configuration.

In Section VI we saw that in an active-triode configuration the doping profile has a profound influence on the distortion that is produced by the MOSFET. Due to this effect, there are bias conditions for which there is no third-order distortion. A practical problem is that these conditions occur at relatively high bias voltages. But it can be imagined that there is a possibility to design a doping profile that yields a distortion-free operation at more favorable bias voltages.

These are interesting possibilities that seem well worth exploring.

VIII. Multiple Kernel Devices

Up to now, we mainly handled transadmittance stages that contain only one kernel device. An exception occurred in Section III-A, where it was shown that a balanced combination of two passive-triode kernel devices behaves as one balanced device.

In general, from the behavior of one kernel device, which is more or less known by now, the behavior of stages that contain more than one kernel device can be determined. As an example, we discuss in this section the series connection of active devices.

Fig. 19 shows two combinations of two active-saturation devices. The circuit of Fig. 19(b) is a series connection, the circuit of Fig. 19(a) is added for comparison. The series stage has been used by Khorramabadi and Gray [30], and with use of junction FET's by Tan and Gray [11]. For both circuits of Fig. 19, it can readily be seen that

$$k_2 = 0 \tag{35}$$

so that there is (ideally) no second-order distortion. Because the stage of Fig. 19(a) can handle an input amplitude that is

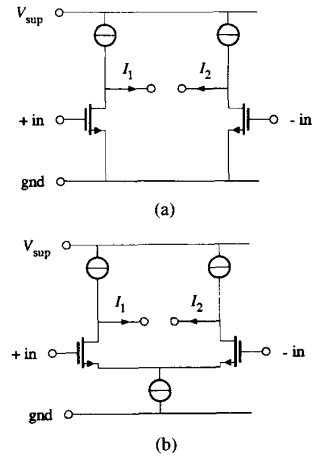

Fig. 19. Two combinations of two active-saturation devices. Circuit (a) is a balanced combination, (b) is a series connection.

twice as much as would be possible with a single device, its k_3 is only a quarter of the k_3 of one single device. Denoting the k_i of one single device with k_i', we have for this stage

$$k_3 = \frac{k_3'}{4}. \tag{36}$$

For the stage of Fig. 19(b) it can be proved that

$$k_3 = \frac{k_3' - 2k_2'^2}{4}. \tag{37}$$

If the transistors would not exhibit second-order distortion by themselves, and would be identically biased, these two stages would have the same third-order distortion characteristics, but if the transistors by themselves produce second-order distortion, this distortion is canceled in the configuration of Fig. 19(a), while it gives rise to third-order distortion in the circuit of Fig. 19(b). Loosely speaking, the stage of Fig. 19(b) converts the second-order distortion of a single transistor to third-order distortion.

Equations (35) to (37) are also valid if other transconductance stages, which may be complete circuits, are substituted for the transistors in Fig. 19, so these equations also apply to the series connection of active-triode stages or linearized active-saturation stages. The latter has been proposed by Wang and Guggenbühl [31], and by Czarnul and Fujii [32]. Because we saw that in a series connection the second-order distortion of one single substage is converted to third-order distortion of the whole stage, a substage with much second-order distortion, such as an unbalanced saturation stage, can better not be used if a low distortion level is wanted. A stage with a low level of second-order distortion—such as an active-triode stage—can give rise to an increase in linearity if the converted third-order distortion cancels the third-order distortion of the substage itself.

The situation gets more complicated if the circuits that are connected in series are no longer identical, as is the case with the transconductance stage of Fig. 20, which has been patented by Fernandez [33], and used by Park, Tan, and Schaumann [34], [35]. It can be thought to consist of

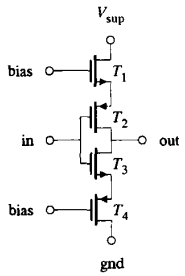

Fig. 20. A transconductance stage that consists of a parallel connection of two parts that in turn consist of a series connection of two active-saturation devices. The stage is balanced if transistors of the same type match and the quiescent input voltage is the arithmetic mean of the two bias voltages.

a balanced parallel connection of two identical subcircuits, each consisting of a series connection of an NMOS transistor and a PMOS transistor. These transistors are used as active-saturation devices, and are all kernel devices.

If $k_{i,j}$ denotes the k_i of transistor T_j, and T_1 and T_3, as well as T_2 and T_4 are identical, and g_{mi} is the transconductance factor of T_i, and $g_{m1} = \alpha_g g_{m2}$, one can prove that the k_3 of the whole stage is

$$k_3 = \frac{k_{3,1} - 2k_{2,1}^2 + \alpha_g^3(k_{3,2} - 2k_{2,2}^2)}{(1+\alpha_g)^3} + 2\frac{(k_{2,1} - \alpha_g^2 k_{2,2})^2}{(1+\alpha_g)^4}. \quad (38)$$

Equation (38) reduces to (37) if the properties under consideration of all the MOSFET's are equal.

Along the same lines, a series connection of devices that do not belong to the same class can be handled. If for instance in the circuit of Fig. 3(b), T_2 and T_3, as well as T_1 should be considered to be kernel devices, the circuit is a multiclass circuit, it belongs to the active-saturation class and to the passive-triode class at once. The intercept voltages $|k_2|^{-1}$ and $|k_3|^{-1/2}$ of this circuit can be obtained from the intercept voltages of the devices by handling the circuit as a series connection of the three devices.

IX. Conclusion

In this paper we handled the distortion generation of MOSFET integrators. By doing this in a systematic way, nearly all integrator possibilities are covered. It was shown that at least for the specific MOSFET type under consideration, in all cases distortion due to mobility reduction is dominant over distortion due to the body effect. Because we saw that body-effect distortion tends to cancel mobility-reduction distortion, we came to the surprising conclusion that we should *not* try to mitigate body-effect distortion, for instance as described in [25], because that would actually *increase* total distortion. In Section IV we saw that in normal situations all the configurations have very much the same distortion figures. With help of insights into the distortion mechanisms, obtained from the models we presented, however, we were able to point out that optimal MOSFET's can be designed. These MOSFET's can give rise to a much larger distortion-free dynamic range than conventional MOSFET's do.

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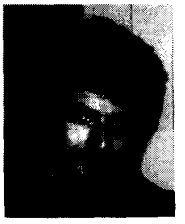

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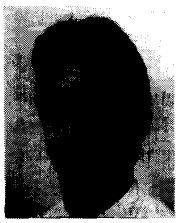

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