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28 GHz Quadrature Frequency Generation Exploiting Injection-Locked Harmonic Extractors for 5G Communications

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***Abstract* — This paper proposes a mm-wave quadrature frequency generator using injection-locked harmonic extractors (HEs) incorporated with quadrature class-F oscillators. While maintaining high output levels at 28 GHz, the utilization of injection locking technique improves the effective quality (Q)-factor and helps to achieve a fundamental harmonic suppression of 60 dB. This results in an FoM of the entire frequency generation system reaching -184 dB. The consideration of quadrature phase mismatch induced by electromagnetic coupling between quadrature buffers is also discussed.**

***Index Terms* — Injection locking (IL), harmonic extraction (HE), quadrature (I/Q) frequency generation.**

I. Introduction

The commercialization of 5G communications has spurred interests in the development of 28 GHz mm-wave transceiver systems. To save cost and battery life, typical CMOS transceiver usually adopts a direct conversion architecture thanks to its lower complexity. High-speed communication, supported through complex modulation schemes, requires low phase noise (PN) from frequency synthesizers. Moreover, quadrature phase mismatch should be minimized in the local oscillator (LO) in order to suppress interference in the image band.

For low PN, the degradation of quality (Q)-factor of a tank at mm-wave should be avoided. Sub-harmonic injection locking can be used but it is susceptible to PVT variations and typically requires an additional calibration loop [1]. An alternative approach is to use a third-harmonic extraction technique which extracts the desired third harmonic component from high-Q class-F oscillator, achieving low PN with high reliability [2]–[4]. A typical quadrature signal generation can be achieved through coupling of two oscillators. However, if used in a transmitter (TX), the oscillator may suffer from the pulling effect of output drivers. Exploiting harmonic extractions can benefit from the mitigation of TX's pulling effect on oscillators. Therefore, we propose to couple two class-F oscillators and extract the 3rd harmonic to generate the quadrature signal, as shown in Fig. 1. The quadrature class-F oscillators [3] and coupling diode ring [5] are adopted to achieve low PN and accurate quadrature phase.

This paper focuses on design considerations of the quadrature harmonic extractor (HE) exploiting the injection locking technique to enhance Q-factor that results in an improvement in fundamental harmonic rejection while consuming relatively lower power. As a proof of concept, the proposed HE, operating at 28 GHz, has been designed and electromagnetically simulated using EMX with post-layout extraction in TSMC 28-nm technology. Section II discusses the design consideration and detailed implementation. Section III provides simulation results and Section IV draws the conclusions.

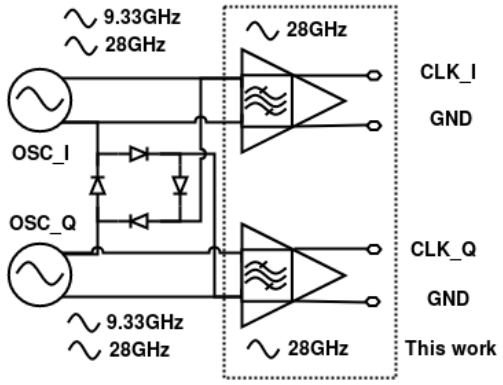

Fig. 1. Proposed mm-wave quadrature frequency generation.

II. Design Considerations and Implementation

In order to improve performance of the proposed frequency generation scheme (see Fig. 2), the design of HE plays an important role in maintaining the 3rd-harmonic output levels with the accurate in-phase/quadrature (I/Q) phase. These should be achieved while consuming minimum additional power to reach high figure-of-merit (FoM) of mm-wave frequency generation traditionally defined as:

$$\mathrm{FoM} = L(\Delta f) - 20\log(\frac{f_0}{\Delta f}) + 10\log(\frac{P_{osc}}{1\mathrm{mW}}). \quad (1)$$

where P_{osc} usually includes power consumption of both the oscillator and HE. Additionally, layout parasitics and electromagnetic coupling between quadrature paths should be carefully taken care of. Even though phase mismatch may be compensated by detuning frequency of locked oscillator [1], the PN of locked oscillator may degrade due to reduction of injection efficiency [6]. To avoid such dilemma, phase inaccuracy introduced by HE should

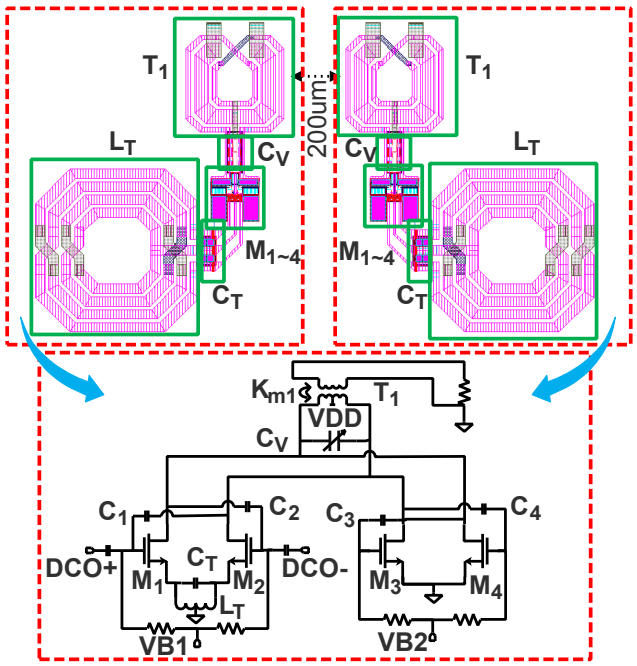

Fig. 2. Proposed harmonic extractor (HE): (top) layout of I/Q HEs; and (bottom) schematic of a single injection-locked HE.

be minimized. Apart from the above concerns, the TX may suffer from a strong fundamental residue at the HE output. Even though such fundamental spur can be attenuated by the HE's band-pass filtering characteristics, a strong residual fundamental component may still appear, consequently degrading the receiver's blocker tolerance and causing spurious output in the TX spectrum [2]. Thus, it should be suppressed to a sufficiently low level. In this section, these three considerations will be discussed for the proposed architecture.

A. Fundamental Suppression

In order to improve suppression of the component at fundamental frequency (f_0), we adopt a source-degenerated parallel LC tank, comprising C_T and L_T in Fig. 2, which resonates at f_0. As mentioned in [4], this tank exhibits high impedance at f_0, thus the input's fundamental component will be followed well at the source of the input differential pair, M_1 and M_2. Consequently, f_0 will be suppressed at V_{gs}. On the other hand, since the signal amplitude at V_{gs} is attenuated, the input transistor will not be saturated by the large fundamental component. Thus, the gain at 3rd-harmonic can be larger when compared with a counterpart without the LC source degeneration. All these contribute to a lower fundamental component relative to the 3rd-harmonic at HE output. In addition, the proposed HE is assisted by the cross-coupling differential pair M_3 and M_4 which

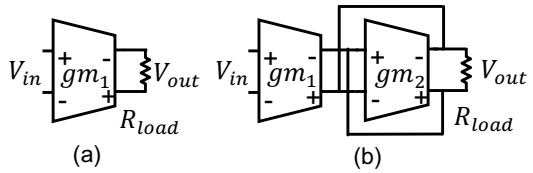

Fig. 3. Simplified diagram of: (a) traditional one-staged amplifier; (b) proposed one-staged injection-locked amplifier.

further helps improving the fundamental suppression. It functions as a negative resistance and is placed in parallel with the load to boost the effective Q of the output tank. For an LC tank resonating at frequency $3f_0$, signal at f_0 can be filtered by:

$$10\log\frac{1}{1+Q^2(\frac{f_0}{3f_0}-\frac{3f_0}{f0})^2}\approx -20\log Q-20\log\frac{7}{3} \quad (2)$$

It can be observed that the more Q is boosted, the better fundamental suppression is achieved.

B. Efficiency Boosting

In the past, the harmonic extraction has usually adopted a two-stage architecture [2]–[3]. The first stage would amplify the 3rd-harmonic signal and the second stage would drive the external $50\,\Omega$ load. While considering the limited chip area and relatively high load resistance in practical on-chip applications, only one stage should be utilized in SoC applications. Thus, in the proposed design, a single-stage amplifier is adopted and the cross-coupling differential pair, M_3 and M_4, is added to boost efficiency. This may look similar to an injection-locked power amplifier [7] but here it is done with different considerations. To clarify the energy efficiency improvement in the proposed system, Fig. 3(b) shows a simplified diagram of the proposed HE. g_{m_1} represents the transconductance of input differential pair, M_1 and M_2, whereas g_{m_2} represents the transconductance of the cross-coupled differential pair, M_3 and M_4. The load impedance at resonant frequency f_0 is simplified to R_{load}. Thus, the voltage gain of this amplifier can be expressed as:

$$\frac{V_{out}}{V_{in}}=g_{m_1}\cdot\frac{R_{load}}{1-g_{m_2}R_{load}} \quad (3)$$

If the target gain is A, g_{m_1} and g_{m_2} should satisfy:

$$g_{m_2}=\frac{1}{R_{load}}-\frac{g_{m_1}}{A} \quad (4)$$

Thus, the total transconductance used in this amplifier can be expressed as:

$$g_{m_1}+g_{m_2}=\frac{1}{R_{load}}+\frac{(A-1)g_{m_1}}{A} \quad (5)$$

Its lower limit is $1/R_{load}$. It can be approached when $g_{m_1}\approx 0$. Substituting it into Eq. (4) yields $g_{m_2}\approx 1/R_{load}$.

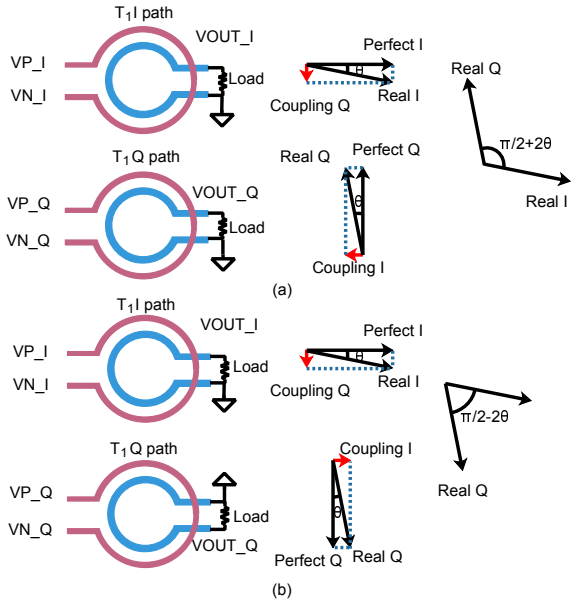

Fig. 4. Coupling phase diagram between I/Q buffers. (a) Layout configuration inducing positive I/Q phase mismatch. (b) Layout configuration inducing negative I/Q phase mismatch.

In that case, the load resistance seen by g_{m_1} can be expressed as:

$$-\frac{R_{load}\cdot\frac{1}{g_{m2}}}{R_{load}-\frac{1}{g_{m_2}}}\approx-\frac{R_{load}^2}{R_{load}-R_{load}}, \tag{6}$$

which is theoretically infinite. Thus, an extremely small signal current coming from g_{m_1} can be amplified to any desired level. Although this lower limit cannot be achieved in practice, it is viable to achieve a total transconductance much lower than A/R_{load}, which is the upper limit. In contrast, the gain of a traditional a general one-stage HE, whose block diagram is shown in Fig. 3(a), is $A = g_{m_1} \cdot R_{load}$. Thus, its total transconductance should be equal to A/R_{load}. Assuming a maximum achievable current efficiency, defined as transconductance over its current consumption, for g_{m_1} and g_{m_2} being identical, lower total transconductance indicates lower power consumption. Therefore, for a one-stage HE, the injection locking structure is much more power efficient when compared with the traditional approach. However, the bandwidth is greatly narrowed down in the injection locked amplifier. Thus, a 2-bit capacitor bank C_v is added in parallel with the output transformer T_1. By digitally tuning C_v, the resonant frequency can track the desired output frequency. Consequently, a high gain over the relative wide tuning range will be maintained.

C. Quadrature Phase Inaccuracy

Compared with the traditional quadrature oscillators, HE is beneficially added in this architecture. Electromagnetic (EM) coupling between the I/Q outputs of HE could result in extra phase mismatch. As shown in Fig. 4, the signal generated by the Q path could couple to the I path and slightly shift its phase. Similarly, the signal in the Q buffer could experience similar mechanism. Unfortunately, this phase shift would not be cancelled or compensated for by itself. Therefore, the phase difference between the I/Q LO signal can grow and result in excessive phase inaccuracy.

A popular strategy to mitigate the EM coupling from nearby environment is to construct an 8-shape coil [8]. In order to verify the coupling mechanism and the 8-shape coil solution, a two-stage transformer-based buffer mentioned in [3] is modified and simulated. The I/Q buffers are spaced 200 um away. Their EM coupling is modeled by EMX. Simulations suggest that if all the transformers adopt the 8-shape, phase inaccuracy can be reduced from 10° to 0.01°. However, this does not exactly apply to the proposed design. In the two-stage buffer case, greater influence is observed from the EM coupling coming from the second stage of the I/Q buffer to the first stage. Since the current in second stage is much larger than that in first stage, it could generate stronger magnetic field and exert greater influence. Note that in the proposed design there is only one stage. Therefore, the phase inaccuracy induced by EM coupling is not that strong. Further, according to EM simulations, ring-shaped transformers can guarantee 0.1° phase inaccuracy if the I/Q transformers are properly spaced. As a result, the ring-shaped transformer is still chosen in the proposed design in a consideration to balance the phase inaccuracy with degradation of Q factor introduced by the 8-shape coil.

III. Simulation Results

Simulation results of the proposed HE are shown in Fig. 5. According to Fig. 5(a), which illustrates the voltage gain at the 3rd-harmonic band, peak gain of 12 dB is achieved. As mentioned previously, a 2-bit capacitor bank with control code (SW) is utilized to compensate the bandwidth degradation caused by the cross-coupled differential pair. By tuning it, the gain could be maintained with less than 5 dB fluctuation across the frequency range of 26–30 GHz. Fig. 5(b) demonstrates the voltage gain $20\log(A_{f_0})$ at fundamental and Fig. 5(c) gives the fundamental suppression, which is defined as $20\log(A_{3f_0}) - 20\log(A_{f_0})$, versus output frequency. In Figs. 5(a)–(c), the corresponding performance for the case in which the negative resistance is turned off is shown in dashed lines. The comparisons suggest the proposed injection-locked HE contributes a 10 dB improvement in the fundamental suppression. Fig. 5(d) shows the output power when HE is cascaded with oscillator. At 29.2 GHz, an output level of -1.2 dBm can be achieved. Across

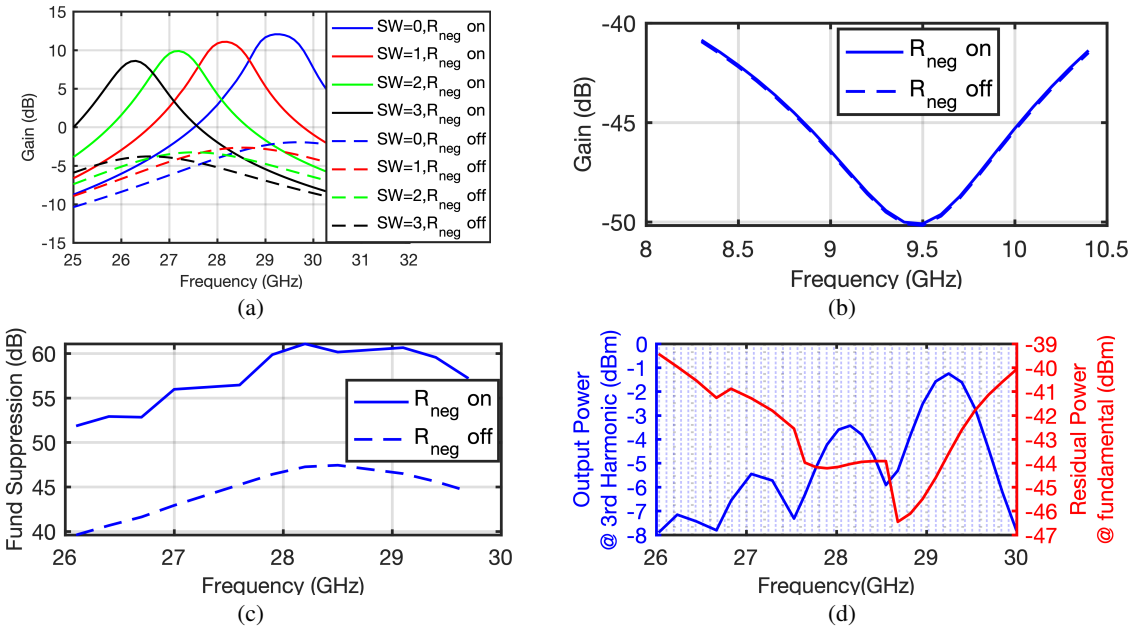

Fig. 5. Simulation results of the proposed buffer. (a) Voltage gain at 3rd harmonic, (b) voltage gain at fundamental, and (c) fundamental suppression. (d) Output power at 3rd harmonic and fundamental when the buffer is cascaded with oscillator.

TABLE I
COMPARISON TABLE WITH STATE-OF-THE-ART MM-WAVE FREQUENCY GENERATION SYSTEMS

	This work	[4]	[3]	[1]
Technology (nm)	28	28	28	65
Quadrature	Y	N	N	Y
Output frequency (GHz)	29.2	66.9	27.3	60
P_{osc} (mW)	12[1]	17	11.58	18.9[1]
P_{buf} (mW)	20.4[1]	22[2]	20[2]	7.8[1]
P_{out} (dBm)	1.8[3]	1	0	-7[3]
PN @ 1MHz (dBc/Hz)	-110.4	-98	-106	-93
FoM (dB)	-184.6	-178.6	-179.7	-174.3

[1] Total power consumption of the two blocks in I/Q path.
[2] Total power consumption of the two stage buffer.
[3] Total output power of I/Q path.

26–30 GHz band, the minimum output power is -8 dBm. Within this band, the residual fundamental component is below -39 dBm, which is also shown in Fig. 5(d). Table I compares performance of the quadrature frequency generation system utilizing the proposed HE with prior works. It can be observed that the proposed HE is the most energy-efficient and helps the whole clock generation system achieving competitively high FoM. In addition, phase inaccuracy introduced by this I/Q HE is merely 0.1°.

IV. Conclusion

A 28 GHz quadrature frequency generation system exploiting injection-locked harmonic extraction (HE) is proposed. Effective Q-factor of HE is boosted by cross-coupled differential pair which not only helps improving the fundamental suppression by 10 dB but it also helps achieving lower power consumption at the same output power level. This contributes to better FoM. The cause and solution for quadrature phase inaccuracy due to electromagnetic coupling have been discussed, which is beneficial in designing accurate quadrature clock generation system.

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