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RESEARCH ARTICLE

Design and Analysis of a Novel Two-Switch Transformerless High Step-Up DC–DC Converter for Grid-Connected Renewable Energy Sources

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ABSTRACT Renewable Energy Sources (RESs), particularly Photovoltaic (PV) systems, inherently produce variable DC voltages that often cannot meet load or grid requirements directly. Consequently, a reliable and efficient DC-DC converter is required to interface RESs with downstream converters and loads. This paper proposes a non-isolated, high-gain, transformerless step-up DC-DC converter that provides continuous input current and a non-inverting output voltage. The proposed topology is designed to minimize switching losses and to maintain a low component count, thereby improving conversion efficiency while containing cost and implementation complexity. A comprehensive analytical model that includes parasitic elements is developed to derive the converter voltage gain. Comparative analyses of device voltage and current stresses against recently reported topologies are presented. The results demonstrate that the proposed converter achieves high voltage gain with reduced voltage and current stresses on switching devices, while preserving acceptable component current levels. Conduction intervals of switches and diodes, as well as switching loss contributions, are analyzed and quantified. Experimental validation is provided by a $100W$ prototype, and measured results corroborate the theoretical predictions and simulation outcomes. The proposed converter thus represents an effective and practical solution for high-gain DC–DC conversion in renewable energy applications, offering an advantageous trade-off between efficiency, component simplicity, and cost.

INDEX TERMS DC–DC converter, high-gain, photovoltaic, renewable energy sources (RESs), transformerless, voltage and current stresses.

NOMENCLATURE

ABBREVIATIONS

CCM	Continuous Current Mode.
DCM	Discontinuous Current Mode.
EMI	Electromagnetic Interference.
ESR	Equivalent Series Resistance.
PV	Photovoltaic.
RES	Renewable Energy Source.
RMS	Root-Mean-Square.
SSA	State Space Averaging.
VMC	Voltage Multiplier Circuit.

NOMENCLATURE

A_2	A matric for $(1-D)$ time interval.
A_1	A matric for Dtime interval.
B_2	B matric for $(1-D)$ time interval.
B_1	B matric for Dtime interval.
C_2	C matric for $(1-D)$ time interval.
C_1	C matric for Dtime interval.

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R_c	Capacitor ESR.
$P_{C,ESR}$	Capacitors ESRs loss.
V_f	Diode forward voltage.
r_D	Diode resistance.
t_{rr}	Diode reverse recovery time.
$P_{Con,D}$	Diodes conductions loss.
P_{rr}	Diodes reverse recovery loss.
E_2	E matric for *(1-D)* time interval.
E_1	E matric for D time interval.
η	Efficiency.
r_L	Inductor wire resistance.
$P_{Con,L}$	Inductors conduction loss.
P_{in}	Input power.
$i_c(t)$	Instantaneous capacitor current.
$v_L(t)$	Instantaneous inductor voltage.
I_{Ci}^{avg}	i^{th} capacitor average current.
I_{Ci}	i^{th} capacitor current.
I_{Ci}^{RMS}	i^{th} capacitor RMS current.
V_{Ci}	i^{th} capacitor voltage.
ΔV_{Ci}	i^{th} capacitor voltage ripple.
I_{Di}	i^{th} diode current.
I_{Di}^{RMS}	i^{th} diode RMS current.
I_{Li}^{avg}	i^{th} inductor average current.
V_{Li}^{avg}	i^{th} inductor average voltage.
I_{Li}	i^{th} inductor current.
ΔI_{Li}	i^{th} inductor current ripple.
V_{Li}	i^{th} inductor voltage.
L_i^{min}	i^{th} minimum inductance to operate in CCM.
I_{Qi}	i^{th} switch current.
I_{Qi}^{RMS}	i^{th} switch RMS current.
P_{out}	Output power.
y	Output variables vector.
R	Resistive load.
U	Sources vector.
X	State variables vector.
$R_{DS(ON)}$	Switch ON-state resistance.
r_s	Switch resistance.
t_{off}	Switch transition to OFF-state time.
$P_{Con,Sw}$	Switches conduction loss.
$P_{S,Sw}$	Switches switching loss.
f_s	Switching frequency.
P_{Loss}	Total power loss.
G	Voltage gain.

I. INTRODUCTION

Fossil-fuel-based power plants are major contributors to environmental degradation through emissions of greenhouse gases and other pollutants, exacerbating climate change and jeopardizing both ecosystems and human health [1], [2]. As a result, the adoption of Renewable Energy Sources (RESs)—including wind turbines and Photovoltaic (PV) modules—has increased markedly over recent decades [3], [4]. The performance of PV systems is highly dependent on environmental conditions such as solar incidence angle, irradiance level, and cloud cover, which directly affect the irradiance incident on PV panels [5]. These variations often produce substantial fluctuations in PV output voltage, highlighting the importance of site selection and local weather patterns for system optimization. A stable voltage supply is essential to ensure efficient operation and longevity of electrical loads, since voltage fluctuations can cause reduced efficiency, operational faults, and even component damage. To mitigate these effects, DC–DC converters are routinely employed to convert the variable output of RESs into a regulated and reliable voltage suitable for downstream converters and loads [6]. In particular, high step-up DC–DC converters are required to elevate the typically low PV voltages to the higher levels needed by the DC link or grid-side converters [7], [8], [9]. Therefore, a high step-up DC-DC converter serves as a critical interface between RESs and the DC link, as illustrated in Fig. 1.

The DC-DC converters are generally classified as isolated and non-isolated topologies. Isolated DC–DC converters provide several important advantages, including electrical isolation, a wider achievable voltage-regulation range, enhanced reliability, and improved electromagnetic noise immunity [10], [11]. These features make isolated converters particularly suitable for safety- and performance-critical applications such as medical equipment, industrial automation, avionics, and telecommunications, where protection of loads from electrical faults and galvanic coupling is essential [12]. However, isolated topologies also entail disadvantages: they typically incur higher cost, larger physical size and weight, and can introduce significant Electromagnetic Interference (EMI). Techniques commonly used to obtain high voltage gain in DC-DC converters include coupled inductors, switched-inductors, switched-capacitors, built-in transformers, VMCs, and multi-stage arrangements [10]. Designs based on coupled inductors or built-in transformers often face challenges associated with leakage inductance, which can degrade performance and increase device stress [13]. Switched-capacitor topologies rely on rapid capacitor switching and therefore generate high *di/dt*, which can impose substantial electrical and thermal stress on switching components and passive elements, increasing the risk of failure. Consequently, the selection of an appropriate converter topology and boosting technique depends on the specific application requirements and trade-offs among cost, size, efficiency, reliability, EMI performance, and component stress.

In light of the foregoing discussion, non-isolated DC–DC converters that do not employ coupled inductors or transformers are increasingly preferred in PV systems. Consequently, considerable research has focused on such converters. A novel single-switch non-isolated DC-DC topology inspired by the conventional boost and self-lift SEPIC converters has been proposed; this topology imposes minimal voltage stress on the switching devices [14]. Banaei and Bonab introduced an innovative transformerless single-switch buck–boost converter that attains high efficiency while providing both step-up and step-down conversion. The proposed design achieves higher voltage gain than classic topologies such

as conventional buck-boost, Cuk, SEPIC, and Zeta converters; however, it produces an inverted output polarity [15]. Reference [16] presents a two-switch input-parallel/output-series architecture that uses input-stage interleaving to reduce current ripple and attains high gain by series-connecting output capacitors. Notably, the voltage stress on each switch in this topology is limited to half the output voltage. A different buck-boost converter proposed in [17] offers low-ripple input current such that an input filter is rendered unnecessary, making it particularly suitable for the RES and fuel-cell applications. The key advantage of this converter is its non-inverting output polarity, which is often absent in many buck–boost variants. Elsayad et al. investigated a single-switch, transformerless DC-DC converter based on an L2C3D2 network, reporting low-ripple input voltage and soft output characteristics that satisfy fuel-cell requirements [18]. Karthikeyan et al. proposed a hybrid high-gain converter with a low component count, continuous input current, and non-inverting output polarity; this topology parallels conventional boost and Cuk converters while employing a single active switch and achieves 92.2% efficiency at full load with a voltage conversion ratio of 5.116 [19]. A two-switch high-gain converter introduced in [20] features a symmetric and simple structure that charges passive components in parallel and discharges them in series. Nevertheless, this topology requires strict parameter matching: deviations can cause elevated voltage stress on semiconductor devices due to parasitic capacitances and inductor resonance. Shayeghi et al. studied a non-isolated buck–boost converter that combines high efficiency with a simple control scheme, though it requires multiple inductors, which increases size and weight [21]. Sadaf et al. presented a modification to the switched-inductor boost converter wherein a diode is replaced with a switch and particular connections are revised to reduce switch current stress; the authors report efficiencies approaching 94% [22]. A two-switch high-gain variant based on an enhanced SEPIC topology is reported in [23]; it offers higher gain, reduced voltage stress across semiconductors, and improved efficiency, with measured efficiencies above 92% across a range of power levels. Prajapati and Chaudhary proposed a high-gain topology inspired by conventional boost and Luo configurations, capable of achieving efficiencies near 95% [24]. Another single-switch high-gain converter described in [25] attains a voltage gain approximately six times that of the traditional boost converter by combining a modified Voltage-Multiplier Cell (VMC) with switched-inductor and switched-capacitor cells. A comparable gain is achieved in [26] using two improved voltage-lift cells together with a switched-inductor cell and a single active switch; this design can be extended to further stages to realize higher voltage gains.

This paper proposes a novel two-switch, transformerless, high-gain step-up DC-DC converter designed for the RESs. The converter operates in two distinct modes, and a comprehensive steady-state analysis is presented to characterize its performance. Detailed examinations of the voltage gain and of the voltage and current stresses on semiconductor devices are provided, together with a comparative evaluation against existing topologies in the literature. The proposed topology achieves substantially lower voltage stress on both diodes and switches while delivering high voltage gain; current stresses remain within acceptable limits, indicating robust device operation. These characteristics contribute to superior overall performance and enable high conversion efficiency. Under the stated test conditions (V_{in} = 30V, V_{out} = 150V, duty cycle D = 0.5, and rated power = 100W, excluding capacitor losses), the converter attains an efficiency of 96.78%.

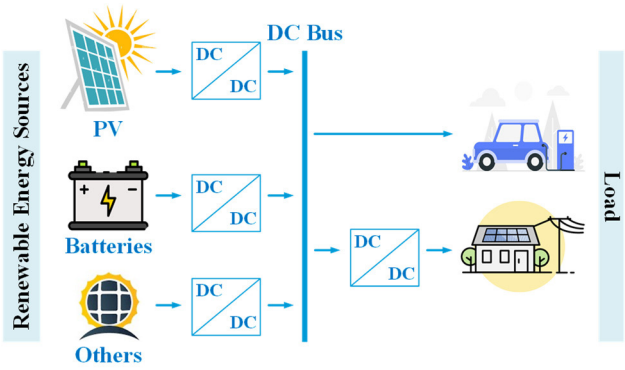

FIGURE 1. The schematic of grid-connected RESs, utilizing DC-DC converters.

II. PROPOSED HIGH-GAIN DC-DC CONVERTER

A. CONVERTER TOPOLOGY DESCRIPTION

Inductors and capacitors are the principal passive elements responsible for voltage boosting in the proposed topology; they achieve this by storing energy during charging interval and releasing it during discharging interval. Semiconductor switching devices—including diodes, MOSFETs, and IGBTs—enable and control the required interconnections among circuit components to realize the intended energy transfer. The proposed topology is shown in Fig. 2. The key features of the proposed high-gain DC-DC converter are as follows:

1. The non-isolated configuration,
2. The continuous input current,
3. The non-inverting output voltage polarity,
4. High voltage conversion ratio,
5. Acceptable volume,
6. Low Switching Loss,
7. Low voltage and current stresses across switching components.

This topology comprises two switches ($Q1$, $Q2$), three inductors ($L1$, $L2$, and $L3$), five capacitors ($C1$, $C2$, $C3$, $C4$, and $C5$), and four diodes ($D1$, $D2$, $D3$, and $D4$). The voltage-boosting elements are $L1$, $L2$, $L3$, $C1$, $C2$, and $C3$. The switches operate with a simultaneous switching pattern. To simplify the steady-state circuit analysis, the following assumptions are adopted:

- Equivalent Series Resistance (ESR) of capacitors winding resistance of inductors, and diodes resistance have been neglected.
- All capacitors have been assumed sufficiently large to maintain approximately constant voltages during each switching period.
- The ON-state resistance $R_{DS(ON)}$ and other parasitic components of switches are ignored.
- Diode forward voltage drops are neglected (i.e., diodes are treated as ideal switches).

The operating modes of the proposed high-gain DC-DC converter are analyzed in the following sections.

B. OPERATING MODES

The typical waveforms of the proposed converter under Continuous Current Mode (CCM) are shown in Fig. 3. The plotted waveforms indicate the polarities (biased directions) of the currents and voltages throughout the switching period. The converter operates in two primary modes, which are described in the following sections.

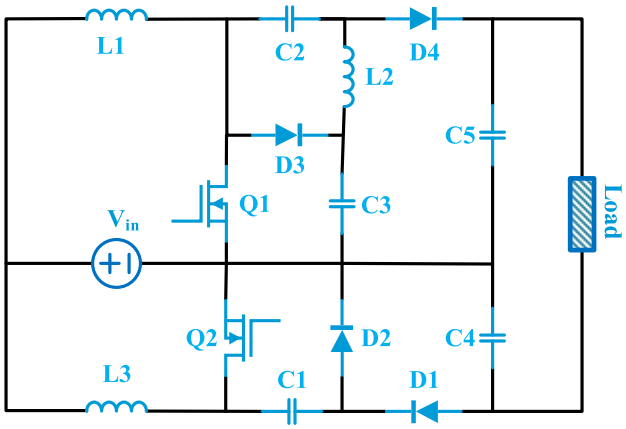

FIGURE 2. The proposed high-gain DC-DC converter layout.

1) MODE I

The active and inactive elements during mode I are depicted in Fig. 4 (a). As noted above, the switches operate simultaneously, alternating between their ON and OFF states. When the switches are in the ON state, the input DC source supplies energy to inductors *L1* and *L3*. In this interval, only diode *D1* is forward-biased. Capacitors *C2* and *C3* discharge, thereby transferring energy to inductor *L2*; as a result, *C2*, *C3*, and *L2* carry equal current amplitudes. Additionally, capacitor *C1* discharges to charge capacitor *C4*. The corresponding relationships, based on Figs. 2 and 3, are given as follows:

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_{C2} - V_{C3} \\ V_{L3} = V_{in} \\ I_{in} = I_{L1} + I_{L3} \\ I_{L2} = I_{C2} = I_{C3} \\ I_{C4} = I_{C1} + I_{C5} \\ I_{out} = I_{C5} \\ V_{out} = V_{C4} + V_{C5} \end{cases} \tag{1}$$

The capacitors currents during this mode are given by:

$$\begin{cases} I_{C1} = -\dfrac{I_{L2}}{D} \\ I_{C2} = -I_{L2} \\ I_{C3} = -I_{L2} \\ I_{C4} = \dfrac{1-D}{D} I_{L2} \\ I_{C5} = -I_{L2} \end{cases} \tag{2}$$

The current through the diodes and switches during this mode are given by:

$$\begin{cases} I_{D1} = -I_{C1} \\ I_{D2} = 0 \\ I_{D3} = 0 \\ I_{D4} = 0 \\ I_{Q1} = I_{L1} + I_{C2} \\ I_{Q2} = I_{L3} + I_{C1} \end{cases} \tag{3}$$

Furthermore, the voltages to be applied to the diodes and switches are as follows:

$$\begin{cases} V_{D1} = 0 \\ V_{D2} = \dfrac{V_{in}}{1-D} \\ V_{D3} = \dfrac{V_{in}}{1-D} \\ V_{D4} = \dfrac{V_{in}}{1-D} \\ V_{Q1} = 0 \\ V_{Q2} = 0 \end{cases} \tag{4}$$

2) MODE II

The active and inactive branches in mode II are illustrated in Fig. 4(b). In this mode both switches are turned off and all diodes except *D1* are conducting. As a result, the inductors are discharged while capacitor *C2* is charged. Capacitors *C3* and *C1* are charged predominantly by inductors *L1* and *L3*, respectively. In addition, capacitor *C5* is charged mainly through the combined effect of capacitor *C2* and inductor *L2*. The corresponding relations are:

$$\begin{cases} V_{L1} = V_{in} - V_{C3} \\ V_{L2} = -V_{C2} = V_{C3} - V_{C5} \\ V_{L3} = V_{in} - V_{C1} \\ I_{in} = I_{L1} + I_{L3} \\ I_{L2} + I_{C2} = I_{L1} + I_{C3} \\ I_{L3} = I_{C1} \\ I_{out} = I_{L2} + I_{C2} - I_{C5} \\ V_{out} = V_{C4} + V_{C5} \end{cases} \tag{5}$$

The currents through the capacitors during this mode are given by:

$$\begin{cases} I_{C1} = I_{L3} \\ I_{C2} = \dfrac{D}{1-D} I_{L2} \\ I_{C3} = \dfrac{D}{1-D} I_{L2} \\ I_{C4} = -I_{L2} \\ I_{C5} = \dfrac{D}{1-D} I_{L2} \end{cases} \tag{6}$$

The currents flowing through the diodes and switches are given below:

$$\begin{cases} I_{D1} = 0 \\ I_{D2} = I_{L3} \\ I_{D3} = \dfrac{I_{L2}}{1-D} \\ I_{D4} = \dfrac{I_{L2}}{1-D} \\ I_{Q1} = 0 \\ I_{Q2} = 0 \end{cases} \tag{7}$$

The voltages across the diodes and switches are given by:

$$\begin{cases} V_{D1} = \dfrac{V_{in}}{1-D} \\ V_{D2} = 0 \\ V_{D3} = 0 \\ V_{D4} = 0 \\ V_{Q1} = \dfrac{V_{in}}{1-D} \\ V_{Q2} = \dfrac{V_{in}}{1-D} \end{cases} \tag{8}$$

III. STEADY-STATE ANALYSIS

It is essential to derive the current and voltage characteristics of the components to obtain a comprehensive understanding of the proposed converter. In this section, the converter is analyzed under CCM.

A. VOLTAGE GAIN

Based on the volt-second balance, the average voltage across each inductor must be zero. In addition, the amp-second principle is also applicable. These principles are stated below:

$$V_L^{avg} = \frac{1}{T_s} \int_0^{T_s} v_L(t)dt = 0 \tag{9}$$

$$I_c^{avg} = \frac{1}{T_s} \int_0^{T_s} i_c(t)dt = 0 \tag{10}$$

Thus, to derive the voltage gain, the capacitor voltages must first be determined. By applying the volt-second balance to the inductors, the capacitor voltages are

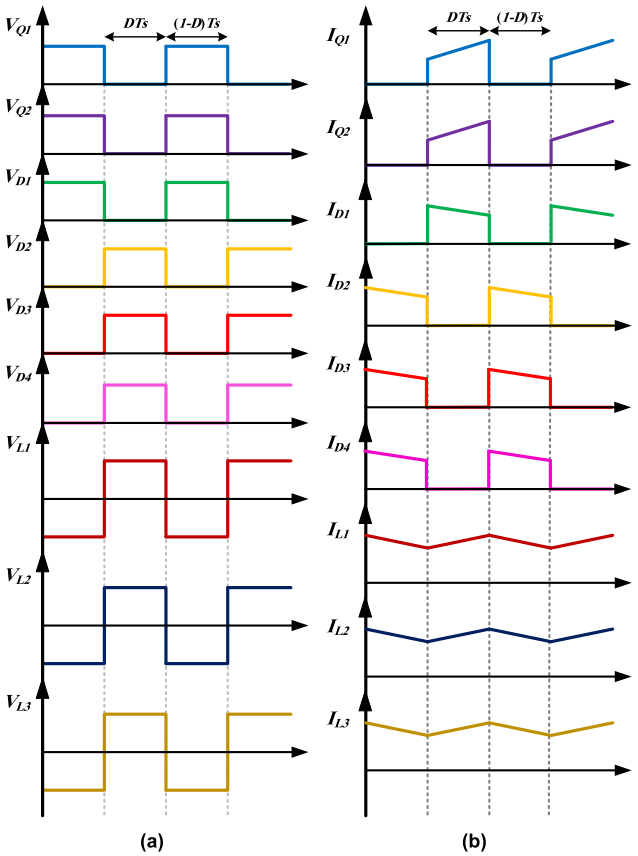

FIGURE 3. The key waveforms of the proposed converters components (a) voltages (b) currents.

obtained as follows:

$$\begin{cases} V_{C1} = V_{C3} = V_{C4} = \dfrac{1}{1-D} V_{in} = \dfrac{1}{2+D} V_{out} \\ V_{C2} = \dfrac{D}{1-D} V_{in} = \dfrac{D}{2+D} V_{out} \\ V_{C5} = \dfrac{1+D}{1-D} V_{in} = \dfrac{1+D}{2+D} V_{out} \end{cases} \tag{11}$$

The output voltage is the sum of the voltages across *C4* and *C5*. Therefore, the voltage gain of the proposed converter in the CCM is:

$$G = \frac{V_{out}}{V_{in}} = \frac{2+D}{1-D} \tag{12}$$

B. CAPACITORS CURRENTS

It is crucial to calculate the converter efficiency precisely. Many published works neglect capacitor losses; therefore, the Root-Mean-Square (RMS) currents of the capacitors must be determined.

$$I_{C1}^{RMS} = \frac{I_{out}}{\sqrt{D(1-D)}} \tag{13}$$

$$I_{C2}^{RMS} = I_{C3}^{RMS} = I_{C5}^{RMS} = \frac{\sqrt{D} I_{out}}{\sqrt{1-D}} \tag{14}$$

$$I_{C1}^{RMS} = \frac{\sqrt{1-D}}{\sqrt{D}} I_{out} \tag{15}$$

C. INDUCTORS CURRENTS

To determine the design parameters, the inductor currents must be established. The average inductor currents, derived from the input and output currents, are given by

$$I_{L1}^{avg} = \frac{1+D}{2+D} I_{in} = \frac{1+D}{1-D} I_{out} \tag{16}$$

$$I_{L2}^{avg} = \frac{1-D}{2+D} I_{in} = I_{out} \tag{17}$$

$$I_{L3}^{avg} = \frac{1}{2+D} I_{in} = \frac{1}{1-D} I_{out} \tag{18}$$

The maximum inductor currents play a crucial role in component selection and in computing RMS currents. Therefore, it is essential to determine the inductor current differentials. The inductor current variations are given below:

$$(\Delta I_{L1})_{Closed} = \frac{D}{L_1 f_s} V_{in} \tag{19}$$

$$(\Delta I_{L2})_{Closed} = \frac{D\,(1+D)}{L_2 f_s (1-D)} V_{in} \tag{20}$$

$$(\Delta I_{L3})_{Closed} = \frac{D}{L_3 f_s} V_{in} \tag{21}$$

Equations (19)-(21) are used to calculate the inductor values and to size the components. In many studies, the inductor current ripple is assumed to be sufficiently small to simplify the mathematical modeling.

D. DIODES AND SWITCHES CURRENT AND VOLTAGE STRESSES

The voltage stress represents the maximum voltage applied to switching devices while they are in the non-conducting (off) state. The current stress denotes the peak current that flows through a device during its operating cycle. It is recommended to select diodes and switches whose voltage and current ratings exceed the calculated stresses by a suitable safety margin; a common practice is to choose components with ratings at least twice the expected stress values. The voltage stresses for the diodes and switches are as follows:

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{Q1} = V_{Q2} = \frac{V_{out}}{2+D} = \frac{V_{in}}{1-D} \tag{22}$$

It can be inferred that the proposed converter's diodes and switches experience relatively low voltage stresses, each being less than one half of the output voltage. This stress ratio can be further reduced by increasing the duty cycle, thereby lowering the peak voltages imposed on the switching devices.

The average currents for the diodes and switches, expressed as multiples of the output current, are as follows:

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{out} \tag{23}$$

$$I_{Q1} = \frac{2D}{1-D} I_{out} \tag{24}$$

$$I_{Q2} = \frac{1}{1-D} I_{out} \tag{25}$$

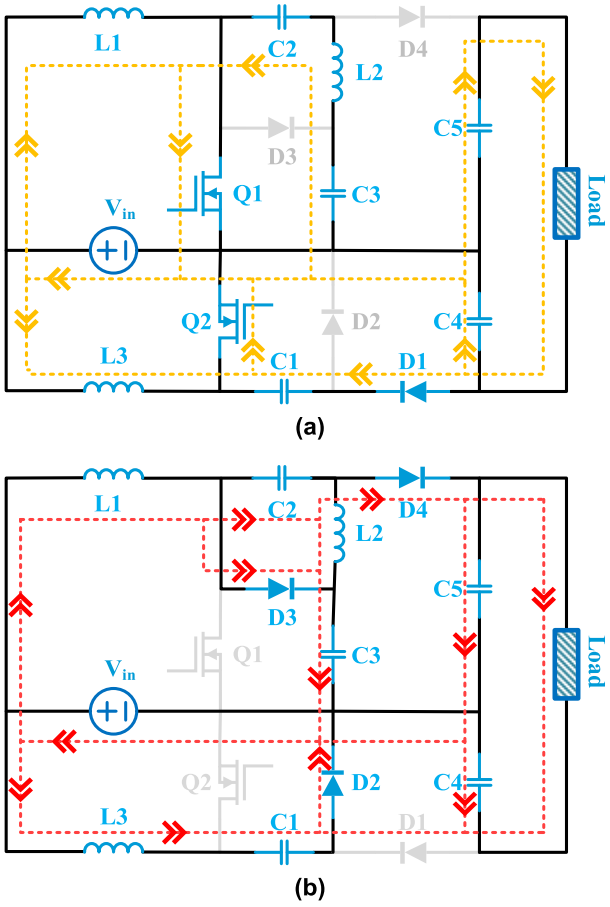

FIGURE 4. The operating modes of the proposed converters (a) Mode I (b) Mode II.

The current stress experienced by the diodes is independent of the duty cycle, indicating that the proposed converter's diodes benefit from a substantially reduced peak current burden. Consequently, the diodes maintain lower peak currents across the full operating range of the duty cycle, improving device reliability and reducing conduction losses.

The RMS current of switching components are:

$$I_{D1}^{RMS} = \frac{I_{out}}{\sqrt{D}} \tag{26}$$

$$I_{D2}^{RMS} = I_{D3}^{RMS} = I_{D4}^{RMS} = \frac{I_{out}}{\sqrt{1-D}} \tag{27}$$

$$I_{Q1}^{RMS} = \frac{2\sqrt{D}}{1-D} I_{out} \tag{28}$$

$$I_{Q1}^{RMS} = \frac{\sqrt{D}}{1-D} I_{out} \tag{29}$$

IV. DESIGN PARAMETERS

To design an optimal converter, all components—particularly the inductors and capacitors—must be selected with care; this meticulous selection leads to a more compact and cost-effective design.

A. INDUCTORS

Based on current ripple, inductors value can be determined from (19)-(21) as follow:

$$L_1 = \frac{D}{\Delta I_{L1} f_s} V_{in} = \frac{D(1-D)}{\Delta I_{L1} f_s (2+D)} V_{out} \tag{30}$$

$$L_2 = \frac{D(1+D)}{\Delta I_{L2} f_s (1-D)} V_{in} = \frac{D(1+D)}{\Delta I_{L2} f_s (2+D)} V_{out} \tag{31}$$

$$L_3 = \frac{D}{\Delta I_{L3} f_s} V_{in} = \frac{D(1-D)}{\Delta I_{L3} f_s (2+D)} V_{out} \tag{32}$$

It is evident that if the inductance values fall below a certain threshold, the converter transitions into Discontinuous Conduction Mode (DCM). The minimum inductances required to maintain the CCM are as follows:

$$L_1^{min} \geq \frac{RD(1-D)^2}{2f_s(2+D)(1+D)} \tag{33}$$

$$L_2^{min} \geq \frac{RD(1+D)}{2f_s(2+D)} \tag{34}$$

$$L_3^{min} \geq \frac{RD(1-D)^2}{2f_s(2+D)} \tag{35}$$

Therefore, the average inductor currents must exceed half of the peak-to-peak current ripple to avoid entering the DCM. If the converter operates in DCM, the inductor current falls to zero for part of the switching period, degrading converter performance.

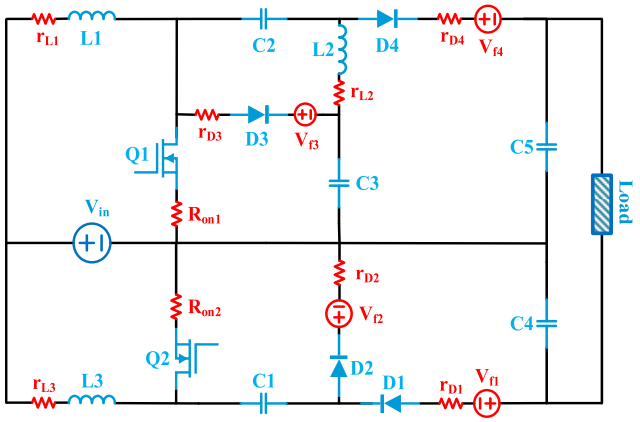

FIGURE 5. Equivalent circuit of the proposed converter with parasitic components.

B. CAPACITORS

The capacitor values can be determined from (2) and (6) based on the switching frequency, duty cycle, allowable voltage ripple, and output current, as follows:

$$C_1 = \frac{I_{out}}{f_s \Delta V_{C1}} \tag{36}$$

$$C_2 = \frac{DI_{out}}{f_s \Delta V_{C2}} \tag{37}$$

$$C_3 = \frac{DI_{out}}{f_s \Delta V_{C3}} \tag{38}$$

$$C_4 = \frac{(1-D)I_{out}}{f_s \Delta V_{C4}} \tag{39}$$

$$C_5 = \frac{DI_{out}}{f_s \Delta V_{C5}} \tag{40}$$

V. NON-IDEAL MODE VOLTAGE GAIN

The voltage gain given in equation (12) was derived under the assumption of ideal components; however, the actual voltage gain observed in practice is typically lower. This discrepancy arises from several non-ideal effects, including component limitations, inductor de-energization times, control instabilities, and reduced converter efficiency.

To clarify these effects, the principal parasitic elements that influence performance are included in the analysis: the winding resistances of the inductors, the forward voltage drops of the diodes, and the MOSFETs' on-state resistances. The capacitors' ESR is neglected. The equivalent circuit of the proposed converter with the considered parasitic elements is shown in Fig. 5.

To derive the non-ideal voltage gain of the proposed converter, volt-second method may be utilized. However, in order to have a systematic vision, it is preferred to employ the state space averaging (SSA) method. The SSA is based on state space equations as follows:

$$x = AX + BU \tag{41}$$

$$y = CX + EU \tag{42}$$

Then, the outputs are obtained as below:

$$Y = \left(-CA^{-1}B + E\right) U \tag{43}$$

Since the converter has a single output and the output voltage is the quantity of interest, the Y vector corresponds to V_{out}. The matrices A, B, C, E, and U are defined as follows**:**

$$A = A_1 D + A_2(1-D) \tag{44}$$

$$B = B_1 D + B_2(1-D) \tag{45}$$

$$C = C_1 D + C_2(1-D) \tag{46}$$

$$E = E_1 D + E_2(1-D) \tag{47}$$

$$U = [V_{in} V_f]^T \tag{48}$$

To derive the $A1$, $A2$, $B1$, $B2$, $C1$, and $C2$ matrices, the converter is analyzed in its two switching states (ON and OFF). The matrices are then obtained as follows:

It should be noted that the E_1 and E_2 matrices are zero. Substituting as in (49)–(54), shown at the bottom of the next page, into (44)-(47), and then using the resulting A, B, and C matrices in (43), yields the expanded form of (43) as in (55), shown at the bottom of page 9. Consequently, after simplification, the non-ideal voltage gain of the proposed converter is obtained as in (56), shown at the bottom of page 9..

The ideal and non-ideal voltage gains of the proposed converter are compared in Fig. 6 for an input voltage of $10V$. The non-ideal gain is consistently lower than the ideal gain for all duty cycles. Beginning at a duty cycle of approximately D=0.7, the discrepancy increases, and it becomes

particularly pronounced near D=0.8. At D=0.92, the maximum non-ideal voltage gain is 17.18, whereas the ideal voltage gain reaches 36.5 at the same duty cycle; beyond this point the gain decreases markedly. The device parameters used in the comparison are: diode forward voltages V_f=0.7V, inductor resistance R$_L$=0.05Ω, diode resistance R_D =0.02Ω, MOSFET on-resistance $R_{DS(on)}$ =0.1Ω, and load R_{load} =100 Ω.

To investigate the effect of parasitic components on voltage gain, these elements were varied over typical ranges and their influence on the output voltage was analyzed. Because diode series resistance had a negligible effect, it was held constant

$$A_1=\begin{bmatrix} \frac{-(r_s+r_L)}{L_1} & \frac{-r_s}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{r_s}{L_2} & \frac{r_s+r_L}{L_2} & 0 & 0 & \frac{-1}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ 0 & 0 & -\frac{r_s(r_L+r_D)+r_Lr_D}{L_3(r_s+r_D)} & \frac{-r_s}{L_3(r_s+r_D)} & 0 & 0 & \frac{r_s}{L_3(r_s+r_D)} & 0 \\ 0 & 0 & \frac{r_s}{C_1(r_s+r_D)} & \frac{-1}{C_1(r_s+r_D)} & 0 & 0 & \frac{1}{C_1(r_s+r_D)} & 0 \\ 0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_3} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-r_s}{C_4(r_s+r_D)} & \frac{1}{C_4(r_s+r_D)} & 0 & 0 & \frac{-(r_s+r_D+R)}{RC_4(r_s+r_D)} & \frac{-1}{RC_4} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{RC_5} & \frac{-1}{RC_5} \end{bmatrix} \tag{49}$$

$$A_2=\begin{bmatrix} \frac{-r_L}{L_1} & 0 & 0 & 0 & \frac{-1}{L_1} & 0 & \frac{-r_D}{RL_1} & -\frac{r_D+R}{RL_1} \\ 0 & \frac{r_L}{L_2} & 0 & 0 & 0 & \frac{-1}{L_2} & \frac{r_D}{RL_2} & \frac{r_D+R}{RL_2} \\ 0 & 0 & \frac{-(r_L+r_D)}{L_3} & \frac{-1}{L_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 & \frac{-1}{r_DC_2} & \frac{1}{r_DC_2} & \frac{-1}{RC_2} & \frac{-(r_D+R)}{Rr_DC_2} \\ 0 & \frac{-1}{C_3} & 0 & 0 & \frac{1}{r_DC_3} & \frac{-1}{r_DC_3} & \frac{1}{RC_3} & \frac{r_D+R}{Rr_DC_3} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{RC_4} & \frac{-1}{RC_4} \\ \frac{1}{C_5} & \frac{1}{C_5} & 0 & 0 & \frac{-1}{r_DC_5} & \frac{1}{r_DC_5} & \frac{-2}{RC_5} & \frac{-(2r_D+R)}{Rr_DC_5} \end{bmatrix} \tag{50}$$

$$B_1=\begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{r_s}{L_3(r_s+r_D)} & \frac{1}{C_1(r_s+r_D)} & 0 & 0 & \frac{-1}{C_4(r_s+r_D)} & 0 \end{bmatrix}^T \tag{51}$$

$$B_2=\begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_3} & 0 & 0 & 0 & 0 & 0 \\ \frac{-1}{L_1} & \frac{1}{L_2} & \frac{1}{L_3} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{52}$$

$$C_1=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \end{bmatrix} \tag{53}$$

$$C_2=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \end{bmatrix} \tag{54}$$

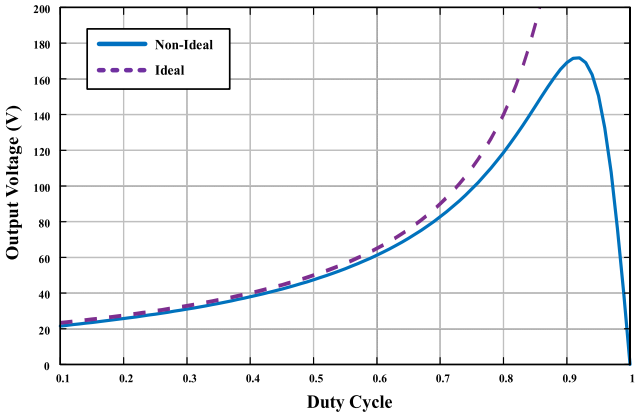

FIGURE 6. The ideal and non-ideal output voltage of the proposed converter in accordance with the duty cycle.

throughout the study. The resulting output-voltage variations for different diode forward voltages, inductor resistances, and MOSFET on-resistances are presented in Fig. 7. As shown in Fig. 7(a), changing the diode forward voltage from $0.7V$ to $2.0V$ produced output voltages of $172V$ and $17.7V$, respectively, indicating a limited effect under the tested conditions. In contrast, inductor and MOSFET resistances exhibit more pronounced effects. Fig. 7(b) shows that the MOSFET on-resistance $R_{DS(on)}$ strongly affects voltage amplification: for $R_{DS(on)}$=0.1, 0.4, 0.7, and 1.0Ω, the maximum achievable output voltages are $171.8V$, $98.64V$, $75.91V$, and $63.92V$, respectively. Increasing $R_{DS(on)}$ also reduces the allowable maximum duty cycle to approximately D=0.92, 0.86, 0.83, and 0.8 for these resistances. Thus, MOSFET on-resistance notably influences both the attainable output voltage and the maximum operational duty cycle.

Regarding inductor resistances, Fig. 7(c) shows that the output voltages are $191.7V$, 171.8 V, $149.0V$, and $133.4V$ for r_L=0.02, 0.05, 0.10,and 0.15Ω, respectively. The corresponding maximum operational duty cycles for these resistances are approximately D=0.92, 0.92, 0.90, and 0.89. Thus, the influence of inductor series resistance on the maximum operational duty cycle is minor. Of the parasitic components considered, the MOSFET on-resistance presents the greatest limitation to achieving the converter's optimal performance.

The non-ideal voltage gains for various output power levels are shown in Fig. 8. Fig. 9 provides a more detailed view, illustrating the combined effects of output power and duty cycle. The results indicate that the voltage gain of the proposed high-gain DC-DC converter decreases as output power increases; equivalently, for a fixed duty cycle, increasing the load reduces the output voltage. For example, Fig. 9 shows that the maximum voltage gain decreases by 52.78% when the output power falls from $40W$ to $20W$. This finding highlights that the non-ideal voltage gain is strongly dependent on the load, unlike the ideal converter model.

VI. COMPARATIVE ANALYSIS OF THE PROPOSED CONVERTER

Numerous factors must be considered when designing a DC–DC converter, including input and output voltage and current ripple, wide-range voltage regulation, power density, EMI, control strategy, voltage gain, protection features, and stability. It is important to recognize that very high voltage gain is not always desirable: an efficient converter must strike an appropriate balance among these performance metrics according to the target application. For high and ultra-high step-up converters, minimizing the ratio of voltage stress to voltage gain is preferred. Moreover, maintaining a proportional relationship between the voltage and current stresses on switching components is recommended to improve reliability and simplify thermal and protection design.

The component counts for the proposed converter and the converters used in the comparative study are summarized in Table 1. Most designs show a similar total number of components and therefore lie within the same range. Table 2 lists the normalized voltage stresses on the switches and diodes as well as the voltage gains. To ensure a fair comparison, two measures were applied: (1) all switch and diode voltage stresses were normalized to the output voltage, and (2) the voltage gain was fixed at 5 for every converter, with the corresponding duty cycles adjusted accordingly.

$$V_{out} = \left(-\begin{bmatrix} 0\\0\\0\\0\\1\\1\\0 \end{bmatrix}^T \begin{bmatrix} -\frac{r_L+r_sD}{L_1} & \frac{-r_sD}{L_1} & 0 & 0 & 0 & 0 & \frac{r_D(D-1)}{RL_1} & \frac{(r_D+R)(D-1)}{RL_1} \\ \frac{r_sD}{L_2} & \frac{r_L+r_sD}{L_2} & 0 & 0 & \frac{-D}{L_2} & \frac{-1}{L_2} & \frac{r_D(1-D)}{RL_2} & \frac{(r_D+R)(1-D)}{RL_2} \\ 0 & 0 & -\frac{r_D^2D+r_sr_D+r_Lr_D+r_Lr_s}{L_3(r_s+r_D)} & \frac{r_DD-r_s-r_D}{L_3(r_s+r_D)} & 0 & 0 & \frac{r_sD}{L_3(r_s+r_D)} & 0 \\ 0 & 0 & \frac{r_s+r_D-r_DD}{C_1(r_s+r_D)} & \frac{-D}{C_1(r_s+r_D)} & 0 & 0 & \frac{D}{C_1(r_s+r_D)} & 0 \\ \frac{1-D}{C_2} & \frac{-D}{C_2} & 0 & 0 & \frac{D-1}{r_DC_2} & \frac{1-D}{r_DC_2} & \frac{D-1}{RC_2} & \frac{(r_D+R)(D-1)}{Rr_DC_2} \\ 0 & \frac{-1}{C_3} & 0 & 0 & \frac{1-D}{r_DC_3} & \frac{D-1}{r_DC_3} & \frac{1-D}{RC_3} & \frac{(r_D+R)(1-D)}{Rr_DC_3} \\ 0 & 0 & \frac{-r_sD}{C_4(r_s+r_D)} & \frac{D}{C_4(r_s+r_D)} & 0 & 0 & \frac{-(r_s+r_D+RD)}{RC_4(r_s+r_D)} & \frac{-1}{RC_4} \\ \frac{1-D}{C_5} & \frac{1-D}{C_5} & 0 & 0 & \frac{D-1}{r_DC_5} & \frac{1-D}{r_DC_5} & \frac{-2}{RC_5} & \frac{(r_D+R)D-(2r_D+R)}{Rr_DC_5} \end{bmatrix} \begin{bmatrix} \frac{1}{L_1} & \frac{D-1}{L_1} \\ 0 & \frac{1-D}{L_2} \\ \frac{1}{L_3} & \frac{r_s+r_D-r_DD}{L_3(r_s+r_D)} \\ 0 & \frac{D}{C_1(r_s+r_D)} \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-D}{C_4(r_s+r_D)} \\ 0 & 0 \end{bmatrix} \right) \begin{bmatrix} V_{in} \\ V_f \end{bmatrix} \tag{55}$$

$$G = \frac{RD(1-D)\left(2V_{in}-2V_f+2DV_f+DV_{in}\right)}{V_{in}\left(r_D+r_s+D\left(r_D+3r_l+R\right)+D^2\left(4r_s-3r_D-2R\right)+D^3\left(2r_l+r_D+R\right)\right)} \tag{56}$$

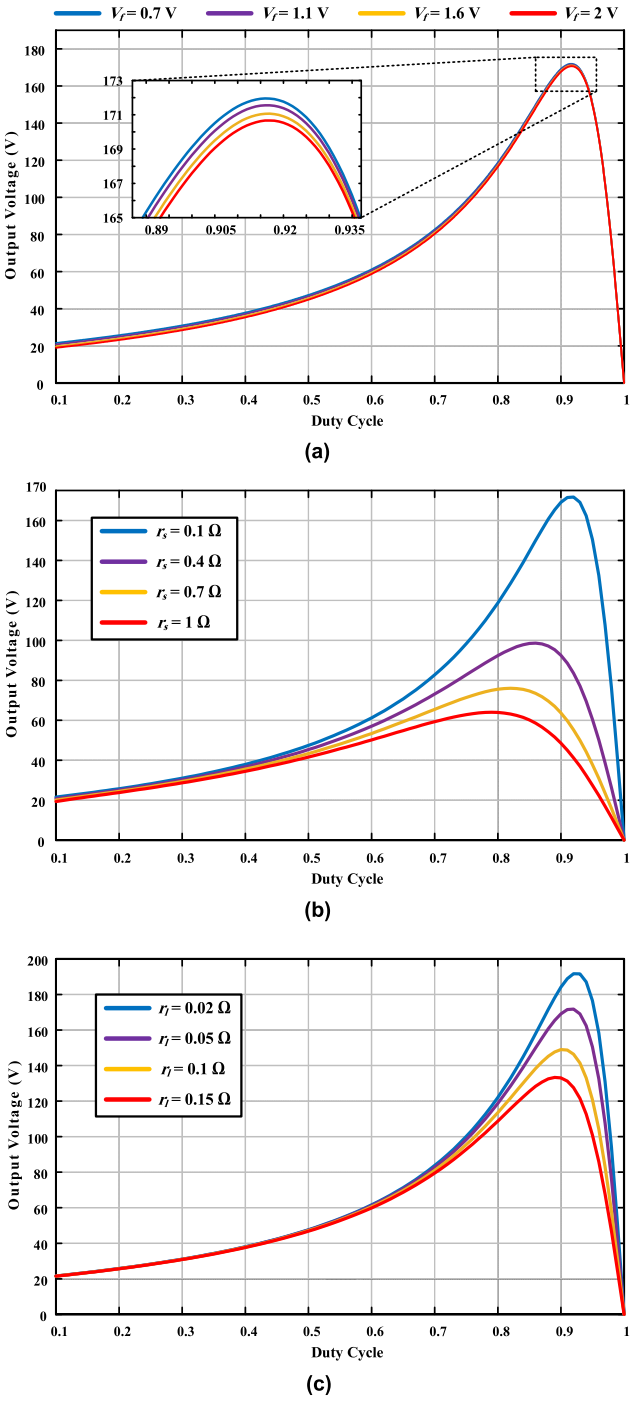

FIGURE 7. The output voltage variations of the proposed high-gain DC-DC converter across different duty cycles influenced by (a) diode forward voltages, (b) MOSFET turn-on resistances, and (c) inductor resistances.

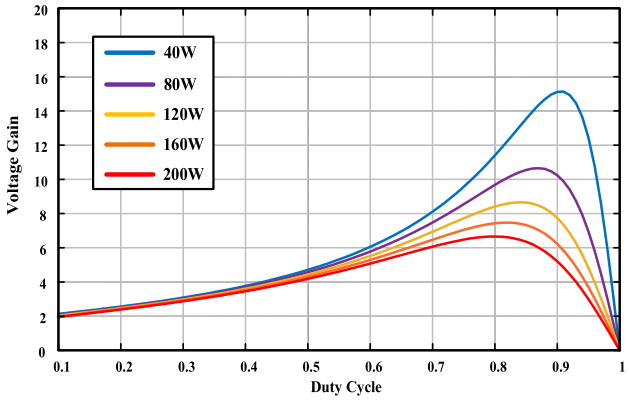

FIGURE 8. The output voltage variations in accordance with the various output power values.

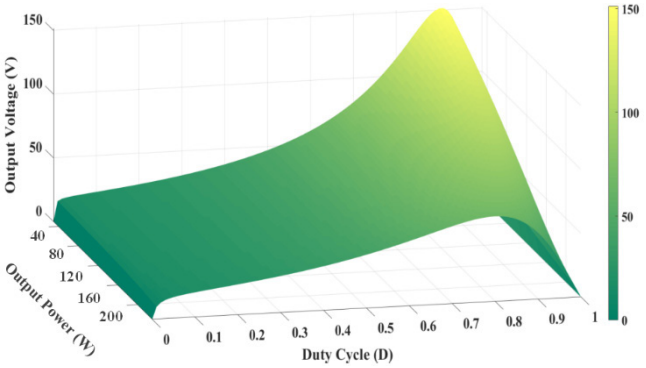

FIGURE 9. The non-ideal output voltage of the proposed converter versus duty cycle and output power variations.

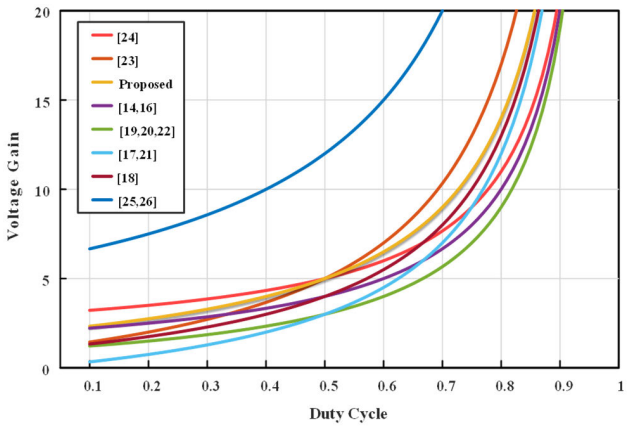

FIGURE 10. Voltage gains versus duty cycles.

For clarity, the results are presented in Figures 10 and 11. Comparison of Table 2 and Figure 10 indicates that the converter proposed in this paper achieves the highest voltage gain among the surveyed topologies, with the exception of the converters reported in [23], [24], [25], and [26]. Although the converter in [24] exhibits a larger gain at low duty cycles, the gain of the proposed converter surpasses it for duty cycles greater than 0.5. A similar behavior is observed with respect to the converter in [23]. The converters in [25] and [26] deliver substantially higher voltage gain; however, these topologies use a greater number of diodes, which increases component count and construction cost. Moreover, capacitive loops appear in all operating modes of those converters, which may introduce additional implementation challenges.

Figure 11 reports the maximum voltage stress experienced by the switches and diodes of each converter. In the duty-cycle range examined, the proposed converter exhibits switch and diode voltage stresses that are lower than or equal to those of the other topologies. Furthermore, all switches and diodes in the proposed converter share the same voltage stress level. Among the compared converters, the topology of [17] shows the highest voltage stress within the considered duty-cycle range. Although the switch voltage stresses of [23] match those of the proposed converter, the diodes in [23] endure approximately twice the voltage stress.

For duty cycles below 0.5, the proposed converter yields lower switch voltage stresses than most alternatives; for duty cycles above 0.5, its switch stresses become larger than some competitors. As specific examples, at duty cycles of 0.2 and 0.8 the switch voltage stresses in [23] are 37.51% higher and 21.43% lower, respectively, than those of the proposed converter. The diode stresses in [23] are comparatively worse: at the same duty cycles they are 75.02% and 42.86% higher, respectively. Overall, the proposed converter consistently maintains lower diode voltage stress than the other examined topologies.

The switch voltage stresses of the converters in [14] and [16] remain essentially constant across the duty-cycle range. Notably, the proposed converter's switch voltage stresses remain below 0.5 (normalized) for all considered duty cycles. The converters in [15], [17], and [21] present the highest stresses on both switches and diodes when the duty cycle is below 0.33; nevertheless, their stresses remain higher than those of the proposed converter across the entire duty-cycle span. The converter of [24] exhibits marginally lower switch and diode voltage stresses for duty cycles below 0.5, but the difference relative to the proposed converter is small.

Finally, the non-isolated converters reported in [18], [19], and [20] experience greater voltage stresses than the proposed topology throughout the duty-cycle range examined. For example, their switches and diodes show approximately 83.34% and 22.2% higher voltage stresses, respectively. The normalized maximum voltage stress for the topology in [22] equals 1, which is greater than that of the proposed converter.

Fig. 12 compares the maximum current stresses of the studied converters, and Table 3 lists the individual current stresses of switches and diodes. In the proposed converter, diodes *D2*, *D3*, and *D4* share the same current stress, while *D1* carries a substantially higher current. Similarly, switch *Q2* experiences higher current stress than *Q1*.

The converter in [24] exhibits larger maximum current stresses for both switches and diodes than the proposed topology. Its diode currents fall below those of *D2-D4* only for duty cycles above 0.73, which are generally impractical. The converters in [15] and [17] present critically high maximum current stresses, considerably exceeding those of the proposed converter's switching components.

In [16], the diodes endure much higher peak currents than *D2-D4* and are slightly higher than *D1*. For switches, [16] shows greater maximum current stress up to a duty cycle of

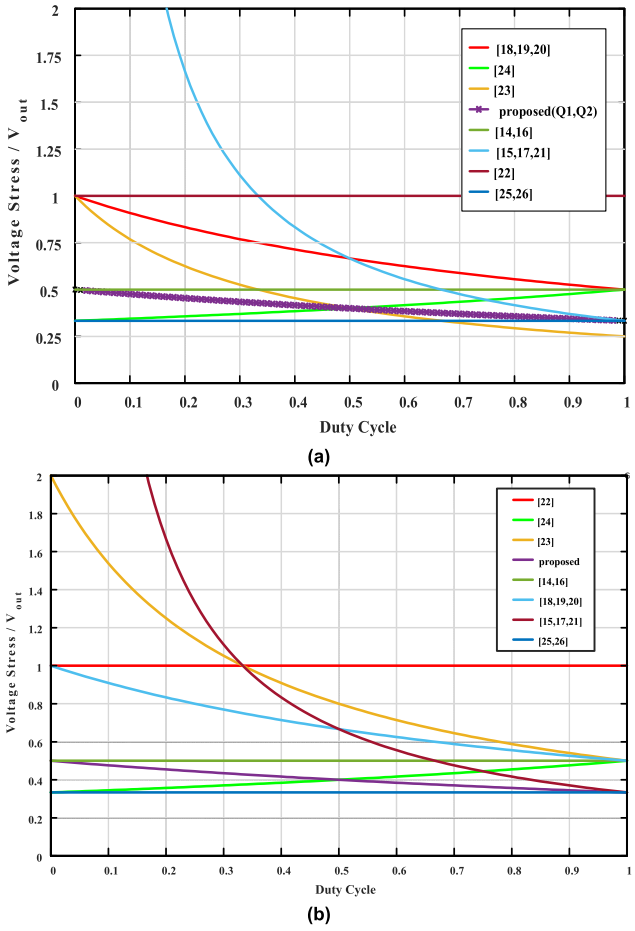

FIGURE 11. Maximum voltage stresses of (a) switches and (b) diodes.

0.66, but lower stresses beyond 0.73 when compared to *Q2* and *Q1*, respectively. The converter in [22] demonstrates a similar switch-current behavior; its diodes, however, consistently draw less current than *D1* for all duty cycles and exceed *D2-D4* only for duty cycles below 0.41.

The topology in [21] exhibits diode behavior that resembles *D1*, but its overall maximum current stress is substantially higher than *Q1*, *D2*, *D3*, and *D4*; additionally, it presents increased stresses relative to *Q2* for duty cycles above 0.7. In contrast, the converters in [25] and [26] subject switches to relatively low current stress across most duty cycles, with magnitudes remaining below I_{in}. Even so, the proposed converter offers a more favorable current-stress profile for *Q2*. For duty cycles above 0.45, *Q1*'s current stress in the proposed converter also decreases.

Regarding diode currents in the proposed topology, they are subject to a constant stress of $I_{in}/2$. This value exceeds the currents of *D2-D4* only for duty cycles below 0.9; *D1*, however, experiences lower current for duty cycles greater than 0.45. The converter in [14] maintains lower diode maximum currents at all duty cycles but shows higher switch maximum currents in practically important ranges (higher than *Q1* for duty cycles below 0.9 and higher than *Q2* for duty cycles above 0.38).

TABLE 1. The proposed and other selected converters components count for the comparative analysis.

Components	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	Proposed
Inductors No.	2	3	2	4	3	2	2	4	2	3	1	2	2	3
Capacitors No.	4	5	3	6	5	3	4	6	1	3	4	6	6	5
Diodes No.	3	3	3	3	3	2	2	3	3	2	4	7	7	4
Switches No.	1	1	2	1	1	1	2	1	2	2	1	1	1	2
Total	10	12	10	14	12	8	10	14	8	10	10	16	16	14

TABLE 2. Voltage stresses of the switches and diodes of various DC-DC converters.

Converter	$\frac{V_{Q1}}{V_{out}}$	$\frac{V_{Q2}}{V_{out}}$	$\frac{V_{D1}}{V_{out}}$	$\frac{V_{D2}}{V_{out}}$	$\frac{V_{D3}}{V_{out}}$	$\frac{V_{D4}}{V_{out}}$	$\frac{V_{D5}}{V_{out}}$	$\frac{V_{D6}}{V_{out}}$	$\frac{V_{D7}}{V_{out}}$	$\frac{V_{out}}{V_{in}}$	D
[14]	$\frac{1}{2}$	-	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	-	-	-	-	$\frac{2}{1-D}=5$	0.6
[15]	$\frac{1}{3D}=0.53$	-	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	-	-	-	-	$\frac{3D}{1-D}=5$	0.625
[16]	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	-	-	-	-	$\frac{2}{1-D}=5$	0.6
[17]	$\frac{1}{3D}=0.53$	-	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	-	-	-	-	$\frac{3D}{1-D}=5$	0.625
[18]	$\frac{1}{1+D}=0.64$	-	$\frac{1}{1+D}=0.64$	$\frac{1}{1+D}=0.64$	$\frac{1}{1+D}=0.64$	-	-	-	-	$\frac{1+2D}{1-D}=5$	0.571
[19]	$\frac{1}{1+D}=0.6$	-	$\frac{1}{1+D}=0.6$	$\frac{1}{1+D}=0.6$	-	-	-	-	-	$\frac{1+D}{1-D}=5$	0.67
[20]	$\frac{1}{1+D}=0.6$	$\frac{1}{1+D}=0.6$	$\frac{1}{1+D}=0.6$	$\frac{1}{1+D}=0.6$	-	-	-	-	-	$\frac{1+D}{1-D}=5$	0.67
[21]	$\frac{1}{3D}=0.53$	-	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	-	-	-	-	$\frac{3D}{1-D}=5$	0.625
[22]	$\frac{1}{1+D}=0.6$	1	$\frac{D}{1+D}=0.4$	$\frac{1-D}{1+D}=0.2$	1	-	-	-	-	$\frac{1+D}{1-D}=5$	0.67
[23]	$\frac{1}{1+3D}=0.4$	$\frac{1}{1+3D}=0.4$	$\frac{2}{1+3D}=0.8$	$\frac{2}{1+3D}=0.8$	-	-	-	-	-	$\frac{1+3D}{1-D}=5$	0.5
[24]	$\frac{1}{3-D}=0.4$	-	$\frac{1}{3-D}=0.4$	$\frac{1}{3-D}=0.4$	$\frac{1}{3-D}=0.4$	$\frac{1}{3-D}=0.4$	-	-	-	$\frac{3-D}{1-D}=5$	0.5
[25]	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{6}{1-D}=5$	0.2
[26]	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{6}$	$\frac{1}{6}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{6}{1-D}=5$	0.2
Proposed	$\frac{1}{2+D}=0.4$	$\frac{1}{2+D}=0.4$	$\frac{1}{2+D}=0.4$	$\frac{1}{2+D}=0.4$	$\frac{1}{2+D}=0.4$	$\frac{1}{2+D}=0.4$				$\frac{2+D}{1-D}=5$	0.5

The converters reported in [18] and [19] perform poorly in terms of peak currents: [19] yields higher maximum currents than *Q1*, *D2-D4* for all duty cycles and exceeds *Q2* for duty cycles above 0.28; [18] produces higher currents than the diodes and *Q1* across the entire duty-cycle range and is lower than *Q2* only up to a duty cycle of 0.22. In [20], diode peak currents are lower than *D2-D4* only up to a duty cycle of 0.42; its maximum currents remain approximately lower than *D1* and *Q2*. For [23], at low duty cycles (e.g., 0.48) the maximum current is lower than *D1* but higher than *D2-D4*; at duty cycles of 0.4 and 0.85, the switches' maximum current is lower than *Q2* and higher than *Q1*, respectively.

Overall, considering both switch and diode currents across the practical duty-cycle range, the proposed converter exhibits a superior and more balanced current-stress profile compared with the majority of the examined topologies.

VII. EFFICIENCY EVALUATION

The parasitic elements introduce losses that reduce the converter's efficiency. In this analysis, we account for conduction losses of switches, diodes, and inductors; power dissipated in capacitor ESR; diode reverse-recovery losses; and switching losses of the semiconductor devices. Eddy-current and hysteresis losses in the inductors are neglected. The conduction losses, computed from the RSM currents, are expressed as follows:

$$P_{Con.L}=\frac{P_{out}}{R}\left(r_{L1}\left(\frac{1+D}{1-D}\right)^2+r_{L2}+r_{L3}\frac{1}{(1-D)^2}\right) \tag{57}$$

$$P_{Con.Sw}=\frac{P_{out}}{R}\left(r_{S1}\frac{4D}{(1-D)^2}+r_{S2}\frac{D}{(1-D)^2}\right) \tag{58}$$

TABLE 3. Current stresses of the switches and diodes of various DC-DC converters.

Converter	$\frac{I_{Q1}}{I_{in}}$	$\frac{I_{Q2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	$\frac{I_{D3}}{I_{in}}$	$\frac{I_{D4}}{I_{in}}$	$\frac{I_{D5}}{I_{in}}$	$\frac{I_{D6}}{I_{in}}$	$\frac{I_{D7}}{I_{in}}$	D
[14]	$\frac{3-2D}{2}=0.9$	-	$\frac{1-D}{2}=0.2$	$\frac{1-D}{2}=0.2$	$\frac{1-D}{2}=0.2$	-	-	-	-	0.6
[15]	$\frac{1}{D}=1.6$	-	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	-	-	-	-	0.625
[16]	$\frac{1}{2}$	$\frac{1}{2D}=0.83$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1-D}{2D}=0.33$	-	-	-	-	0.6
[17]	$\frac{1}{D}=1.6$	-	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	$\frac{1}{3D}=0.53$	-	-	-	-	0.625
[18]	$\frac{3}{1+2D}=1.4$	-	$\frac{1}{1+2D}=0.47$	$\frac{1}{1+2D}=0.47$	$\frac{1}{1+2D}=0.47$	-	-	-	-	0.571
[19]	$\frac{2}{1+D}=1.2$	-	$\frac{1}{1+D}=0.6$	$\frac{1}{1+D}=0.6$	-	-	-	-	-	0.67
[20]	$\frac{1-D}{1+D}=0.2$	$\frac{1-D}{1+D}=0.2$	$\frac{1-D}{1+D}=0.2$	$\frac{1-D}{1+D}=0.2$	-	-	-	-	-	0.67
[21]	1	-	$\frac{1-D}{3D}=0.2$	$\frac{1-D}{3D}=0.2$	$\frac{1-D}{3D}=0.2$	-	-	-	-	0.625
[22]	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{D}{1+D}=0.4$	$\frac{1-D}{1+D}=0.2$	$\frac{1-D}{1+D}=0.2$	-	-	-	-	0.67
[23]	$\frac{2+D-D^2}{1+3D}=0.9$	$\frac{2+D-D^2}{1+3D}=0.9$	$\frac{1}{1+3D}=0.4$	$\frac{1}{1+3D}=0.4$	-	-	-	-	-	0.5
[24]	$\frac{D(1+D)}{3-D}=0.3$	-	$\frac{1-D}{D}=1$	$\frac{1}{3-D}=0.4$	$\frac{1-D}{D(3-D)}=0.4$	$\frac{1-D}{D(3-D)}=0.4$	-	-	-	0.5
[25]	$\frac{5+D}{6}=0.87$	-	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	0.2
[26]	$\frac{5+D}{6}=0.87$	-	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	$\frac{1-D}{6}=0.13$	0.2
Proposed	$\frac{2D}{2+D}=0.4$	$\frac{1}{D(2+D)}=0.8$	$\frac{1-D}{D(2+D)}=0.4$	$\frac{1}{2+D}=0.4$	$\frac{1}{2+D}=0.4$	$\frac{1}{2+D}=0.4$	-	-	-	0.5

$$P_{Con.D}=\left(V_{f1}+V_{f2}+V_{f3}+V_{f4}\right)I_{out}+\frac{P_{out}}{R}\left(r_{D1}\frac{1}{\sqrt{D}}+\left(r_{D2}+r_{D3}+r_{D4}\right)\frac{1}{\sqrt{1-D}}\right) \tag{59}$$

The total switching loss of the semiconductor switches is calculated as follows:

$$P_{S.Sw}=P_{out}t_{off}f_s\frac{1+2D}{(2-2D)(2+D)} \tag{60}$$

Generally, reverse recovery denotes the diode's transition from the conducting (ON) state to the blocking (OFF) state. During this interval a reverse current flows before the diode can fully block the voltage, giving rise to reverse-recovery losses. In the present analysis, all diodes are assumed to share the same reverse-recovery time, i.e., t_{rr1}=t_{rr2}=t_{rr3}=t_{rr4}=t_{rr}.

$$P_{rr}=\frac{(1+2D)}{D(1-D)(2+D)}t_{rr}f_sP_{out} \tag{61}$$

To compute the power dissipated in the capacitors' ESRs, all ESRs are assumed equal, i.e., r_{c1}=r_{c2}=r_{c3}=r_{c4}=r_{c5}=r_c. Under this assumption, the total ESR losses of the capacitors can be expressed as follows:

$$P_{C.ESR}=\frac{P_{out}}{R}r_c\frac{4D^2-2D+2}{D(1-D)} \tag{62}$$

Thus, the total loss of the converter is given by the sum of all considered loss components:

$$P_{Loss}=P_{Con.L}+P_{Con.Sw}+P_{Con.D}+P_{S.Sw}+P_{rr}+P_{C.ESR} \tag{63}$$

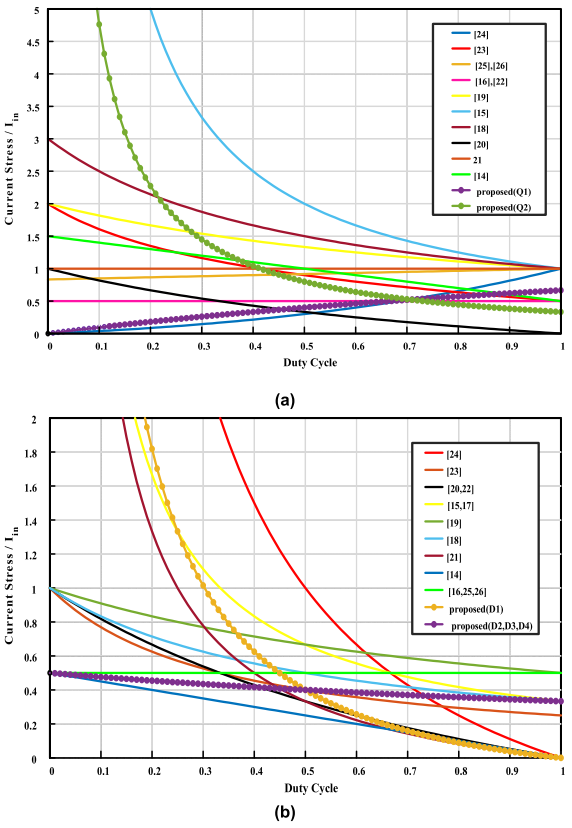

FIGURE 12. Maximum current stresses of (a) switches and (b) diodes.

Then, using, (57)–(62), efficiency may be defined as below:

$$\eta=\frac{P_{out}}{P_{out}+P_{Loss}} \tag{64}$$

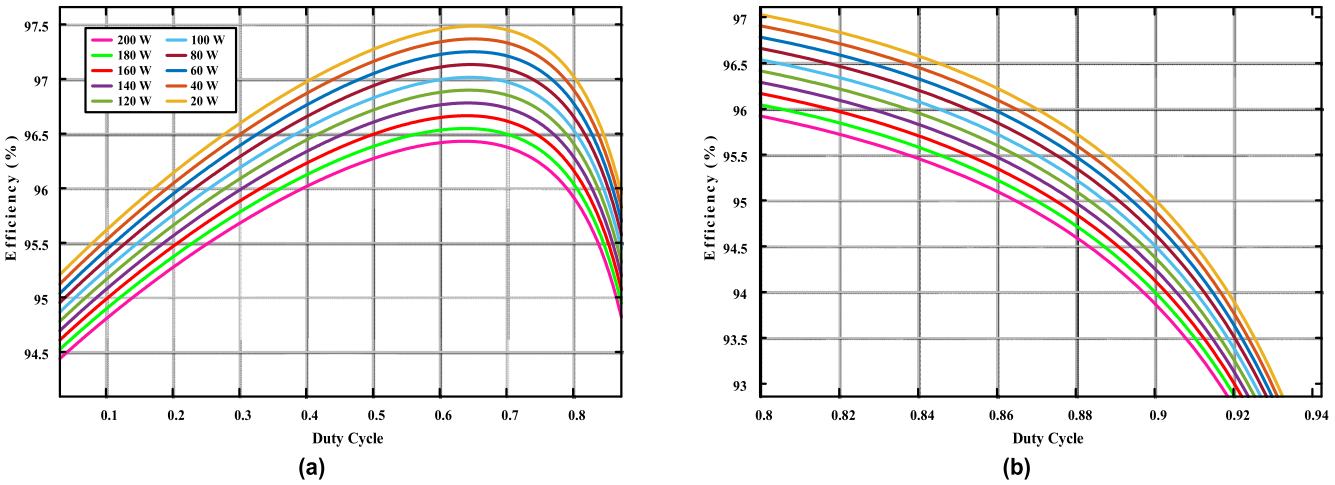

FIGURE 13. Efficiency of the proposed converter in accordance with various duty cycles.

The proposed converter efficiencies under various duty cycles are shown in Fig. 13. Efficiency decreases as output power increases, although it remains above 90% up to duty cycles of 0.92. For lower output-power levels, efficiency exceeds 97% over certain duty-cycle ranges. Increasing the output power shifts the duty-cycle threshold at which efficiency begins to decline to lower values. Efficiency was evaluated for output powers from $20W$ to $200W$ in $20W$ increments. A notable efficiency drop occurs beyond a duty cycle of approximately 0.7. For an output power starting at $20W$, the efficiencies at a duty cycle of 0.5 are 97.27%, 97.16%, 97.05%, 96.94%, 96.83%, 96.71%, 96.60%, 96.49%, 96.38%, and 96.27%, respectively.

The losses and efficiency of the proposed converter are compared with those of the referenced converters in Table 4 . For a fair comparison, the output power, output voltage, and input voltage are fixed at $100W$, $150V$, and 30 V, respectively, and a switching frequency of 100 KHz is used. Under these conditions, the proposed converter exhibits the highest efficiency among the compared topologies.

As noted, eddy-current and hysteresis losses of the inductors were neglected; only conduction losses were considered. These conduction losses scale with both the inductance value and the number of inductors. The proposed converter demonstrates lower inductor conduction loss than most referenced converters, except for those in [16], [20], [23], and [24]. It should be noted, however, that the converters in [16], [20], [23], and [24] generally achieve this lower inductor loss at the expense of reduced voltage gain and/or increased voltage stress. Although the converters in [16], [20], [24], [25], and [26] use fewer inductors than the proposed topology, they do not achieve overall superiority in system performance. Moreover, the proposed converter's inductor conduction loss is lower than that reported in [15] and [18] (with the same number of inductors) by 63% and 44.5%, respectively.

Diode losses are separated into conduction losses and reverse-recovery losses. Reverse-recovery loss is neglected here because Schottky diodes are assumed. Diode conduction loss comprises the forward-voltage drop and any series resistance; in practice, the resistance contribution is negligible compared with the forward-voltage contribution. Diode conduction loss represents the largest single component of the total converter loss. Most converters listed in Table 4 exhibit diode conduction losses within a similar range. However, the converters in [15], [19], [24], [25], and [26] experience substantially higher diode conduction losses—approximately 2.00, 1.51, 1.75, 3.12, and 3.12 times that of the proposed converter, respectively.

Switch losses include both conduction and switching components. In hard-switched converters, switching losses typically dominate. The proposed converter has among the lowest switch conduction losses, surpassed only by the converters in [20], [23]. By contrast, converters in [15], [17], [21], [25], and [26] exhibit the highest switch conduction losses, roughly four times that of the proposed topology. The proposed converter also shows lower conduction loss than single-switch alternatives listed. Switching loss is proportional to switching frequency and to the time required for the device to transition between states. The converter in [17] exhibits the highest switching loss among the compared designs. Overall, the proposed converter achieves the lowest switching loss except for the designs in [19] and [24]; its switching loss is 63% and 25% higher than those two, respectively. Compared with the remaining referenced converters ([14], [15], [16], [17], [18], [20], [21], [22], [23], [25], [26]), the proposed converter's switching loss is lower by 13.3%, 292%, 166.7%, 104%, 433%, 280%, 67%, 41.3%, 153.3%, 170.67%, and 170.67%, respectively.

Figure 14 presents the detailed loss breakdown for the proposed converter under the stated operating conditions. Total losses comprise diode conduction losses, switch

conduction losses, switching losses, inductor conduction losses, and capacitor losses. The total converter loss, including capacitor losses, is $4.77W$, corresponding to an overall efficiency of 95.23%. Inductor conduction losses amount to $0.31W$, representing 6.5% of the total loss. Switch conduction and switching losses are $0.24W$ (5.03% of total) and $0.75W$ (15.72% of total), respectively. Diode conduction losses are $1.87W$ (39.2% of total), and capacitor losses are $1.60W$ (33.55% of total). These results indicate that the proposed converter benefits from low switching loss and achieves high overall efficiency, while diode conduction loss is the dominant contributor to total loss.

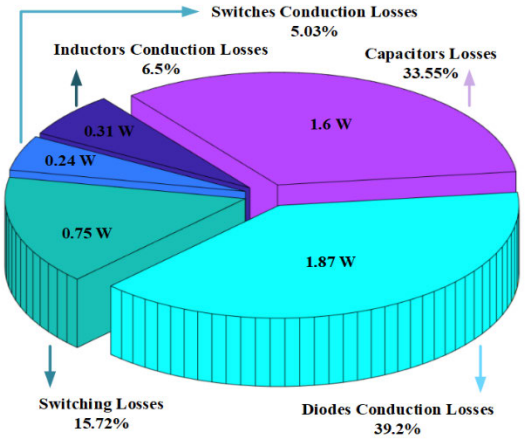

FIGURE 14. The losses distribution of the proposed converter.

VIII. THE PROTOTYPE AND EXPERIMENTAL RESULTS

To validate the theoretical analysis and simulation results, a $100W$ prototype was constructed. The switching frequency and duty cycle were set to 100 KHz and 0.5, respectively, as specified in the comparative analysis. Detailed converter specifications are provided in Table 5. The prototype is designed to operate from a $30V$ input and deliver a $150V$ output.

The $100W$ prototype of the proposed converter and the test setup are shown in Fig. 15 and Fig. 16, respectively. For accurate measurements, a GWInstek GDP-050 50 MHz high-voltage differential probe and a PINTEK PA-677 1 MHz current probe were used. HCPL-316J optocouplers were employed to generate the MOSFET gate-drive pulses. Measured voltage and current waveforms are presented in Fig. 17 and Fig. 18.

Fig. 17(a)–(c) show the inductor voltages, while the corresponding inductor currents are shown in Fig. 18(a)–(c). With the duty cycle set to 0.5, the energizing and de-energizing intervals and their slopes are symmetric. Measured inductor peak, minimum, and average currents are:

- Inductor 1: $I_{max} = 2.34A$, $I_{min} = 1.61A$, $I_{avg} = 1.98A$
- Inductor 2: $I_{max} = 0.79A$, $I_{min} = 0.49A$, $I_{avg} = 0.64A$
- Inductor 3: $I_{max} = 1.68A$, $I_{min} = 0.96A$, $I_{avg} = 1.32A$

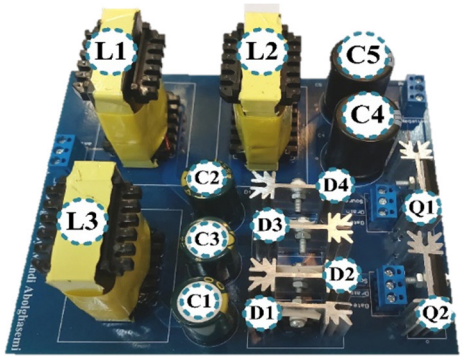

FIGURE 15. The proposed DC-DC converter prototype.

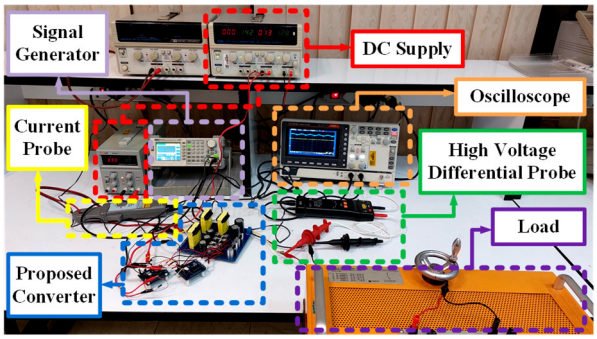

FIGURE 16. The test setup of the proposed DC-DC converter prototype.

All inductors are energized and de-energized simultaneously, as expected. Fig. 17(d)-(g) present the diode voltage waveforms. All diodes experience identical voltage stress of $58.45V$, consistent with the theoretical prediction. The diode current waveforms are shown in Fig. 18(d)-(g). As predicted, diodes *D2*, *D3* and *D4* conduct during the inductors' de-energizing interval, while *D1* conducts during energizing. Measured diode current stresses are approximately $1.51A$, $1.54A$, $1.48A$, and $1.45A$ for *D1*-*D4*, respectively. MOSFET voltage waveforms are given in Fig. 17(h)-(i) and show the same voltage stress as the diodes, in agreement with the previously derived relations. MOSFET current waveforms (Fig. 18(h)-(i)) indicate currents of approximately $3.1A$ and $2.7A$, respectively. Both switches operate simultaneously during the inductors' energizing interval, as with *D1*. The dynamic response is presented in Fig. 19. The duty cycle was increased from 0.5 to 0.6 to observe transient behavior. Under this change, the output voltage and current moved from approximately $150V$ and $0.66A$ to $193V$ and $0.50A$, respectively.

To validate the voltage conversion ratio and measure efficiency, input and output voltages and currents were recorded (Fig. 17(j)-(k) and Fig. 18(j)-(k)). With $V_{in} = 30V$, $D = 0.5$, and rated output power $= 100W$, the measured efficiency is 93.95%, which closely matches the theoretical prediction. The small discrepancy is mainly attributed to capacitor ESR losses that were not included in the theoretical loss model. Figure 20 compares theoretical and experimental

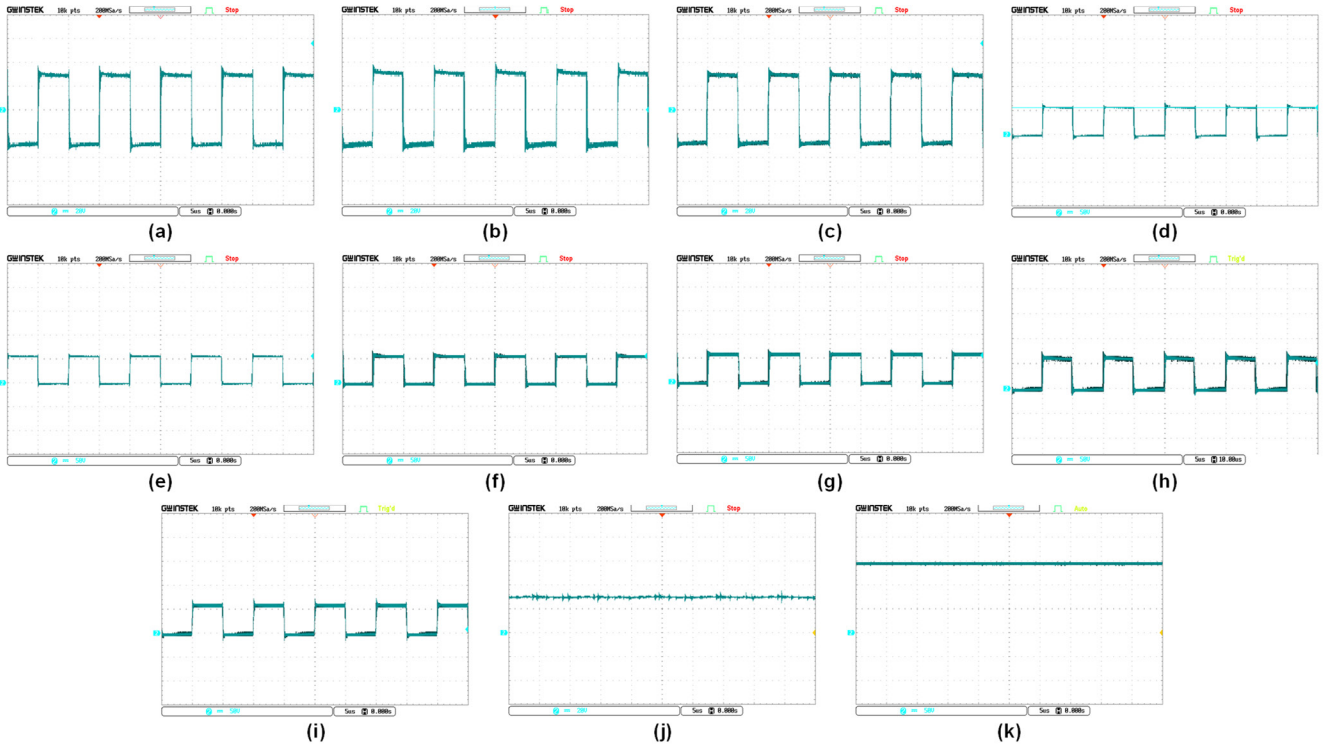

FIGURE 17. The voltages waveforms of the proposed converter components when the input voltage, duty cycle, and rated power are set to 30 V, 0.5, and 100 W, respectively. (a) *L1* (b) *L2* (c) *L3* (d) *D1* (e) *D2* (f) *D3* (g) *D4* (h) *Q1* (i) *Q2* (j) input (k) output.

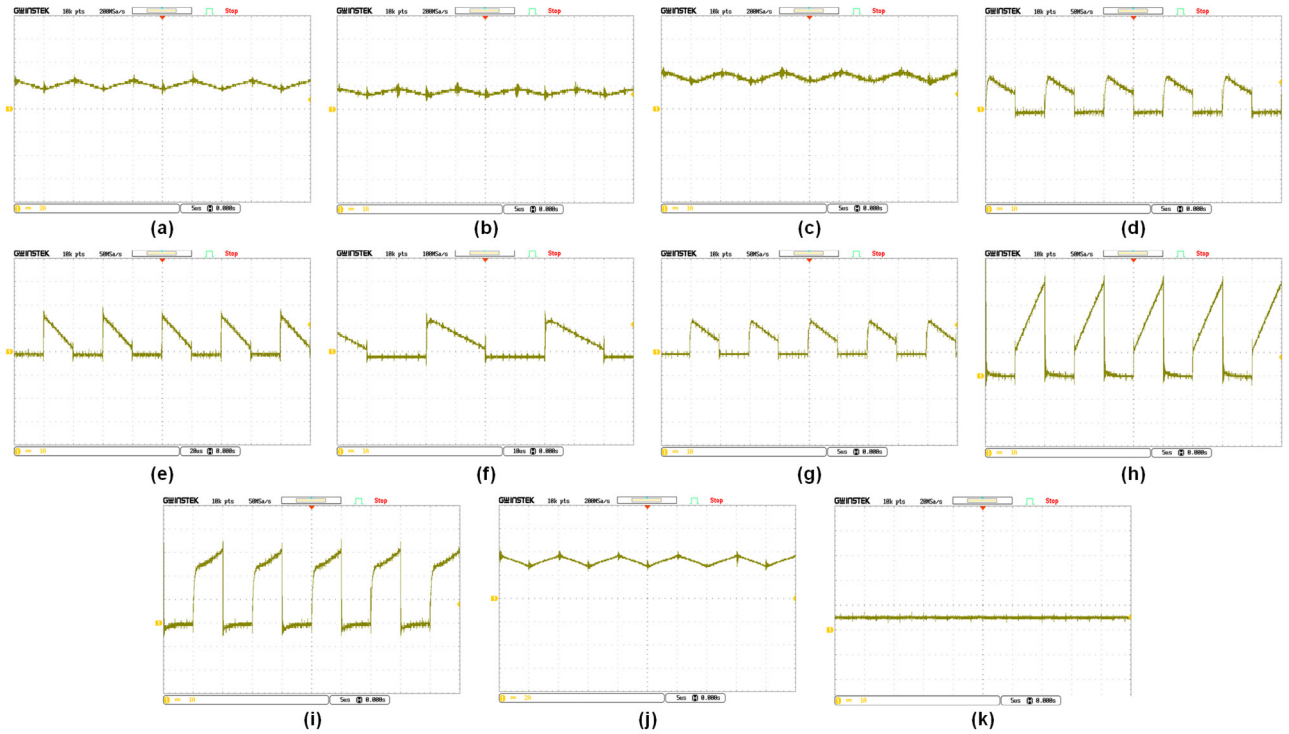

FIGURE 18. The voltages waveforms of the proposed converter components when the input voltage, duty cycle, and rated power are set to 30 V, 0.5, and 100 W, respectively. (a) *L1* (b) *L2* (c) *L3* (d) *D1* (e) *D2* (f) *D3* (g) *D4* (h) *Q1* (i) *Q2* (j) input (k) output.

TABLE 4. The loss analysis of various DC-DC converters.

Converter	Inductors Conduction Loss	Switches Conduction Loss	Diodes Conduction Loss	Switches Switching Loss	Duty Cycle	Efficiency (%)
[14]	$\frac{P_{out}}{R} r_L \frac{4}{(1-D)^2} = 0.55$	$\frac{P_{out}}{R} r_S \frac{(3-2D)^2}{(1-D)^2} = 0.49$	$3V_f I_{out} = 1.4$	$P_{out} t_{off} f_s \frac{3-2D}{2(2-2D)} = 1.06$	0.6	96.5
[15]	$\frac{P_{out}}{R} r_L \frac{6D^2+3}{(1-D)^2} = 0.84$	$\frac{P_{out}}{R} r_S \frac{9D}{(1-D)^2} = 0.98$	$\frac{3}{(1-D)} V_f I_{out} = 3.73$	$P_{out} t_{off} f_s \frac{1}{2D(1-D)} = 2$	0.625	92.45
[16]	$\frac{P_{out}}{R} r_L \frac{2}{(1-D)^2} = 0.28$	$\frac{P_{out}}{R} r_S \frac{1+D^2}{D^2(1-D)^2} = 0.58$	$\frac{1+D}{(1-D)} V_f I_{out} = 1.87$	$P_{out} t_{off} f_s \frac{1+D}{2D(1-D)} = 2.94$	0.6	94.33
[17]	$\frac{P_{out}}{R} r_L \frac{12D^2-6D+3}{(1-D)^2} = 0.62$	$\frac{P_{out}}{R} r_S \frac{9D}{(1-D)^2} = 0.98$	$3V_f I_{out} = 1.4$	$P_{out} t_{off} f_s \frac{2}{2D(1-D)} = 4$	0.625	93
[18]	$\frac{P_{out}}{R} r_L \frac{5D^2+3}{(1-D)^2} = 0.56$	$\frac{P_{out}}{R} r_S \frac{9D}{(1-D)^2} = 0.68$	$3V_f I_{out} = 1.4$	$P_{out} t_{off} f_s \frac{3}{(2-2D)(1+2D)} = 1.53$	0.571	95.83
[19]	$\frac{P_{out}}{R} r_L \frac{2D^2+2}{(1-D)^2} = 0.59$	$\frac{P_{out}}{R} r_S \frac{4D}{(1-D)^2} = 0.6$	$\frac{2}{(1-D)} V_f I_{out} = 2.83$	$P_{out} t_{off} f_s \frac{1}{(1+D)} = 0.56$	0.67	95.42
[20]	$2\frac{P_{out}}{R} r_L \frac{1+D}{1-D} = 0.2$	$2D \frac{P_{out}}{R} r_S = 0.15$	$2V_f I_{out} = 0.93$	$P_{out} t_{off} f_s \frac{1}{(1-D)} = 2.85$	0.67	95.87
[21]	$\frac{P_{out}}{R} r_L \frac{5D^2+2D+2}{(1-D)^2} = 0.82$	$\frac{P_{out}}{R} r_S \frac{9D}{(1-D)^2} = 0.98$	$\frac{3-3D}{1-D} V_f I_{out} = 1.4$	$P_{out} t_{off} f_s \frac{1}{(2-2D)} = 1.25$	0.625	95.55
[22]	$\frac{P_{out}}{R} r_L \frac{2}{(1-D)^2} = 0.41$	$\frac{P_{out}}{R} r_S \frac{D(1+D)^2}{(1-D)^2} = 0.42$	$\frac{(1+D)(2-D)}{2(1-D)} V_f I_{out} = 1.57$	$P_{out} t_{off} f_s \frac{2+D}{(4-4D)} = 1.9$	0.67	95.7
[23]	$\frac{P_{out}}{R} r_L \frac{(1+2D-D^2)^2}{(1-D)^2} = 0.27$	$\frac{P_{out}}{R} r_S \frac{D(2+D-D^2)^2}{(1-D)^2} = 0.22$	$\frac{2}{1-D} V_f I_{out} = 1.87$	$P_{out} t_{off} f_s \frac{2+D-D^2}{(2-2D)(1+3D)} = 0.85$	0.5	96.79
[24]	$\frac{P_{out}}{R} r_L \frac{(1+2D-D^2)^2}{(1-D)^2} = 0.27$	$\frac{P_{out}}{R} r_S \frac{(3-D^3+3D^2-3D)^2}{D(1-D)^2} = 0.88$	$\frac{2D^2-8D+7}{1-D} V_f I_{out} = 3.27$	$P_{out} t_{off} f_s \frac{D(1+D)}{(2-2D)(3-D)} = 0.28$	0.5	95.3
[25]	$\frac{P_{out}}{R} r_L \frac{18}{(1-D)^2} = 0.625$	$\frac{P_{out}}{R} r_S \frac{(5+D)^2}{D(1-D)^2} = 0.94$	$\frac{11-5D}{1-D} V_f I_{out} = 5.83$	$P_{out} t_{off} f_s \frac{5+D}{3(1-D)} = 2.03$	0.2	90.58
[26]	$\frac{P_{out}}{R} r_L \frac{18}{(1-D)^2} = 0.625$	$\frac{P_{out}}{R} r_S \frac{(5+D)^2}{D(1-D)^2} = 0.94$	$\frac{11-5D}{1-D} V_f I_{out} = 5.83$	$P_{out} t_{off} f_s \frac{5+D}{3(1-D)} = 2.03$	0.2	90.58
Proposed	$\frac{P_{out}}{R} r_L \frac{2D^2+3}{(1-D)^2} = 0.31$	$\frac{P_{out}}{R} r_S \frac{5D}{(1-D)^2} = 0.24$	$4V_f I_{out} = 1.87$	$P_{out} t_{off} f_s \frac{1+2D}{(2-2D)(2+D)} = 0.75$	0.5	96.82

efficiencies for output powers from $47W$ to $115W$. Both theory and measurements show efficiencies above 90%; efficiency decreases as output power increases. The maximum difference between theoretical and experimental efficiency under the tested conditions is 2.87%, again primarily due to not modeling the capacitor ESR. The trend in Fig. 20 indicates a larger efficiency reduction at higher output powers.

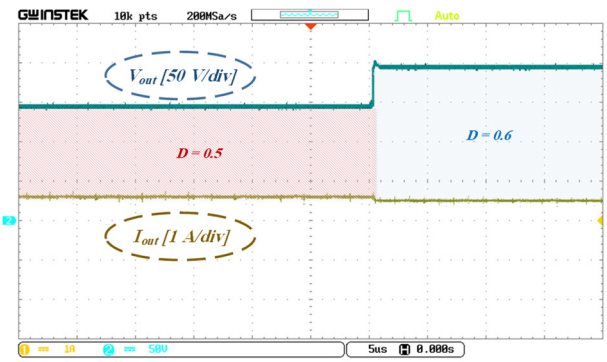

FIGURE 19. Dynamic performance of the proposed converter under the duty cycle variation.

Closed-loop control was implemented using a type-3 PID controller. The voltage-control block diagram is shown in Fig. 21. Controller design was based on the open-loop Bode plot of the converter (Fig. 22). The design targets were a phase margin between 45° and 55° at the 0 dB gain crossover. However, the measured open-loop response exhibited a phase of −259° and a magnitude of −45.14 dB at the intended crossover, indicating that a type-2 controller would be insufficient. Therefore, a type-3 controller was selected. The implemented controller circuit and component values are detailed in Fig. 23, and the controller prototype is shown in Fig. 24.

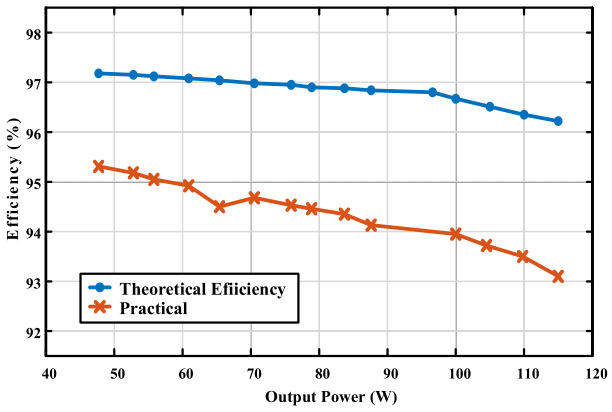

FIGURE 20. The theoretical and practical efficiencies of the proposed converter across various output powers.

Experimental closed-loop tests are reported in Fig. 25. The input voltage was stepped from $30V$ to $25V$ and $35V$; the output voltage tracked these changes and remained regulated, confirming controller effectiveness. A load step from 225Ω to 150Ω (output current increase from $0.667A$ to $1A$) was

TABLE 5. Specifications of the prototype.

COMPONENT	SPECIFICATION
Diode part number	MUR860
MOSFET part number	IPW60R190P6
Inductors (*L1* and *L3*)	200 µH
Inductor (*L2*)	500 µH
Input voltage	30 V
Output voltage	150 V
Output power	100 W
Switching frequency	100 KHz
MOSFETs turn-on resistance	190 mΩ
Diodes forward voltage (max)	1.5 V
Capacitors (*C1*,*C2*, and *C3*)	100 µF – 400 V
Capacitors (*C4* and *C5*)	220 µF – 400 V

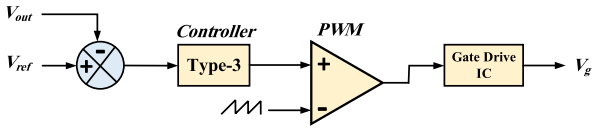

FIGURE 21. The voltage control loop diagram.

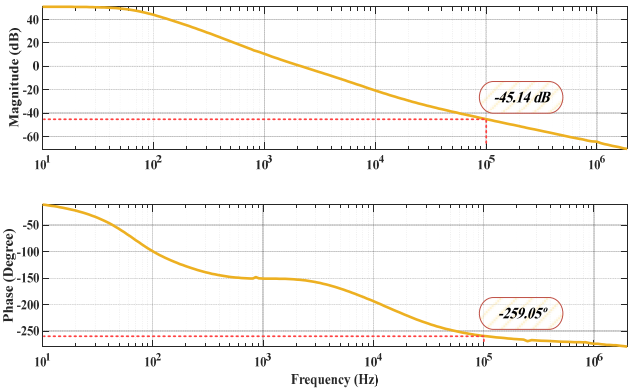

FIGURE 22. The open loop Bode plot of the proposed high gain DC-DC converter.

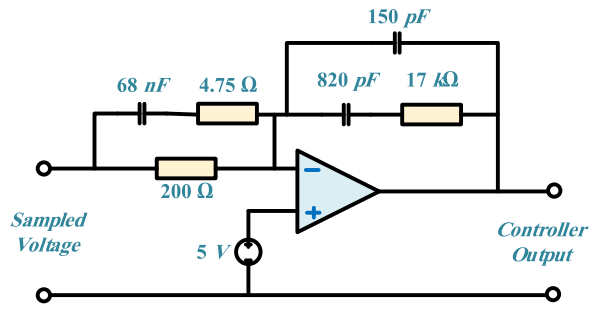

FIGURE 23. The adopted Type-3 controller and the components values.

also applied; the controller maintained the output voltage at 150V during this load change, demonstrating robust regulation and stable closed-loop performance.

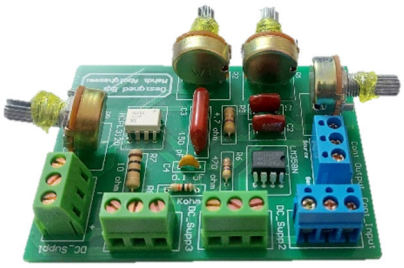

FIGURE 24. The controller prototype.

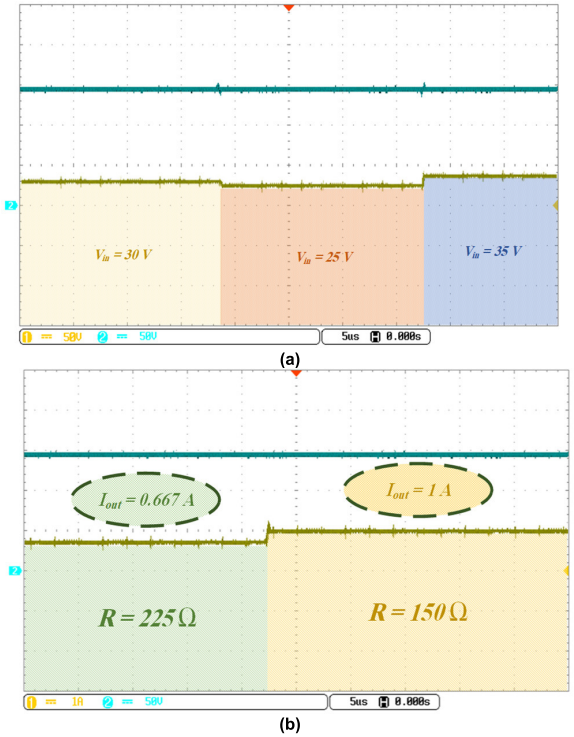

FIGURE 25. Output voltage consistence in accordance with (a) the input voltage variation between 25 to 35 V and (b) the load variation from 225 to 100Ω.

IX. CONCLUSION

A two-switch, high-gain, step-up transformerless DC–DC converter is proposed. The non-isolated topology features a continuous input current, making it well-suited for renewable-energy applications, and achieves a high voltage conversion ratio within a compact component set. A detailed theoretical analysis is presented and the non-ideal voltage gain is derived using the SSA, accounting for inductor series resistances, diode forward voltages and series resistances, and MOSFET on-resistance. Among these non-idealities, MOSFET on-resistance is shown to have the largest influence on voltage gain. The analysis also shows that increasing output power produces a noticeable drop in output voltage, highlighting the need to trade off performance parameters to meet application requirements.

Comparative analysis demonstrates that the proposed converter delivers higher voltage gain than most other topologies

studied, except for two referenced converters over limited duty-cycle ranges. This result indicates that the proposed topology achieves high gain while keeping the component count reasonable. Stress evaluation for diodes and switches indicates relatively low voltage stresses and acceptable current stresses compared with competing designs. Considering voltage gain, component count, and stress levels together, the proposed converter exhibits superior overall performance. Loss and efficiency analyses include conduction losses of switches, diodes, and inductors, as well as switching losses. Under the nominal conditions of $30V$ input, $150V$ output and $100W$ output power, the converter achieves a simulated efficiency of 95.33%, outperforming the compared designs. Notably, switching losses are low, and the converter maintains efficiencies above 93% for duty cycles from 0 to 0.9 under the stated conditions. As expected, efficiency decreases with increasing output power. However, this converter suffers from non-common ground nature and it corresponding consequences. Furthermore, the simultaneous operation of the MOSFETs, lead to higher input current ripple. A $100W$ prototype was built to validate the theoretical and simulation results. Experimental measurements agree closely with theory and simulation, confirming the converter's performance, high efficiency, and practical viability for high-gain, transformerless applications.

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