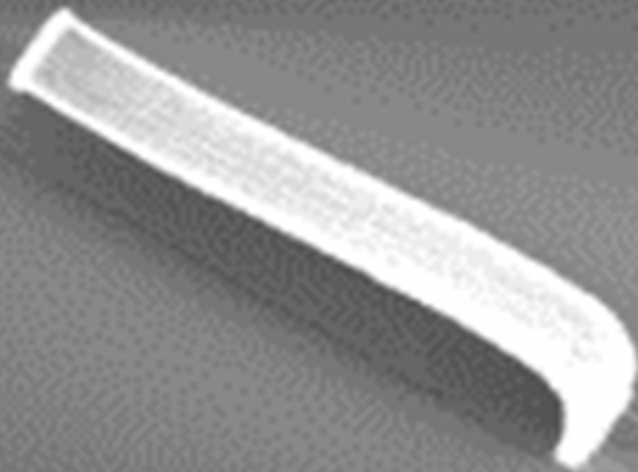


# Design and Fabrication of MEMS Switches by Carbon Nanotubes with Silicon Carbide Coating

by Ziqiao Huang



**MEMS Switches Fabricated by Carbon Nanotubes with Silicon Carbide Coating**

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# **MEMS Switches Fabricated by Carbon Nanotubes with Silicon Carbide Coating**

by

**Ziqiao Huang**

in partial fulfillment of the requirements for the degree of

**Master of Science**

in Electrical Engineering

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*An electronic version of this thesis is available at <http://repository.tudelft.nl/>*



## **Abstract**

The research of advanced material such as Carbon Nanotubes (CNT) has attracted considerable attention in achieving high efficiency and good performance in the electrical and electronic system during the last few decades.

In this research project, the designs and fabrication process for microswitches which are made by carbon nanotubes have been investigated. Much efforts have been done for optimization in growing micrometer length carbon nanotubes, horizontalization of carbon nanotube bundles, and mechanical properties controlled by silicon carbide (SiC) coating. A modeling design is developed to show the feasibility of the electrostatic drive and the electromagnetic drive for the on and off states of the switch. Besides this, the phenomenon that the substrate topology can give a significant influence on carbon nanotube bundles' alignment direction during its growth by temperature no uniform distribution was observed and proved by the simulation and the measurement. In order to compensate and put right the aligned direction, horizontalization methods supplied by disposing photoresists have been explored and successfully showed the practicability to change the bundles' direction after deposition. Also, optical and electrical characteristics have been done to show the good performance of this device.

The future work can relate to optimizing the process parameters to improve the throughput and repeatability. Also, device dimensions can be optimized to get higher electrical performance. An additional test in reliability can also help with checking its robustness under extreme working conditions. More interestingly, substrate topology design can be explored to implement self-controlled carbon nanotube bundles alignment.



## Preface

This thesis work is shown as part of the master graduation project which is required by the Master degree requirements of Master of Science in Electrical Engineering at the Delft University of Technology. This thesis project aims at designing and fabricating a cantilever MEMS switch by carbon nanotubes and tuning the mechanical properties with coating silicon carbide.

The initial aim of this work is to show the potential utilization of carbon nanotubes in making MEMS switch. In order to realize the microscale feature, carbon nanotubes need to be synthesized as bundles. High aspect ratio carbon nanotube bundles as  $20\pm 1$   $\mu\text{m}$  diameter and  $180\pm 4$   $\mu\text{m}$  height have been achieved. Later work we successfully made a single micro pin of 3  $\mu\text{m}$  in width, 15  $\mu\text{m}$  in length, and  $128\pm 5$   $\mu\text{m}$  height bundles so that it gave the microbundles possibility.

The second concern is to design the structure and choose the drive mode. The structure of cantilever is chosen because of its fabrication procedures compatible with clean room process, and previous work has shown that horizontalization of carbon nanotube bundles can be achieved by immersing bundles in solutions. Therefore, we choose electrostatic drive mode to generate the attraction force for the electrode of switches to switch on.

The third part is to optimize the process of horizontalization because we observed the unexpected phenomenon that our asymmetric topology designs can generate the bundles self-aligned to an undesired direction which makes the electrostatic drive impossible. With defining this process, we achieved improving the desired alignment percentage at more than 400% for one structure per die for some deposition recipe.

Moreover, mechanical properties are also important for the structure. Without the coating, the bundles are too soft to behave as a cantilever. Previous work in our group has given modeling and predictions in Young's modulus of carbon nanotubes with silicon carbide coating which shows a potential coating thickness in our work.

Additional work is to etch silicon carbide, then etch silicon oxide by vapor HF to release cantilevers. As silicon carbide is an excellent blocking layer for HF etching, it needs to make sure that all silicon carbide has been etched away.

At last, with longtime deposition of carbon nanotubes growing, a thin film of carbons have been generated on the device surface which leads to conducting everywhere on wafers. This thin film is hard to remove because any methods that can etch the carbons away will also etch and damage the cantilever. Fortunately, the carbon layer's conductivity can be considered as a parallel resistance of carbon nanotube cantilevers and subtracted by mathematical calculations.

The thesis committee consists of my full supervisor, professor Kouchi Zhang, the chair professor of the Electronic Components, Technology and Materials (ECTM) group, my daily supervisor, Dr. Sten Vollebregt, the assistant professor of the ECTM group, and Dr. Murali Ghatkesar, assistant professor in the department of Mechanical, Maritime and Materials Engineering (3mE), who experts in exploring solutions for physics and biology problems by micro/nanoscale devices.

Z.Q. Huang Author

Delft, February 13<sup>th</sup>, 2019

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I have gone through the toughest time in my life in the last year. Problems and setbacks came on every aspect, but I believe all the experience will become the treasure in the future. I thank my family a lot for their encouragement and support. Thank all my friends who enlighten, guide, companion, and keep going with me.

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Delft, February 13<sup>th</sup>, 2019

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# 1. Introduction

This chapter depicts the introduction to this thesis. First, the current state-of-art Micro-Electro-Mechanical System (MEMS) switches technologies and technology challenges will be discussed. This is followed by a discussion of MEMS system technologies, which is the bedrock of implementing MEMS switches. Challenges and limitations in the MEMS Switches technology are identified, and Carbon Nanotubes (CNT) coated with Silicon Carbide (SiC) are presented as a potential material to overcome these obstacles and enhance its performances. The research goals of this work and an overview of previous work from the literature are presented. This chapter concludes with the definition of the research problem and ends with an outline of this thesis.

## 1.1. MEMS switches

Nowadays, the most commonly used switches are transistors and relays. The switch-used transistors are reckoned as contactless switches which depend on electrons transportation between source and drain controlled by its gate voltage. The electron transportation speed has a limitation so that the electrons normally transport at a saturation speed which makes the switching speed correlate with channel's length: the shorter channel length, the faster switching speed. The smaller size also means improving the integration that results in higher performance, lower power consumption per transistor, and lower cost. This is why people are interested in keeping improving the integration level of chip manufacturing all the time. However, the power consumption per unit area increases with higher integration level so that a higher temperature will become a big problem when transistors are working. At the meanwhile, as the source, channel, and drain are not strictly insulated in transistors, current leakage happens between the collector and the emitter. With longtime one direction current flow, electron migration can also generate the defects on circuits.

In this case, people also using electrical signal controlled relays as mechanical switches for better insulation and protection for circuits. But it has a short lifetime, longer switching time (lower frequency) and poor maintainability of contact points. Normally it needs a second stage diode to prevent to be broken down. Also, the dimension of relays is normally centimeter which makes it more difficult to be integrated and utilized in ultra-high integration circuits.

It will be interesting to think about a kind of small scale switches which has good capabilities in low power consumption, good insulation, and high integration. MEMS is an advanced technology of which the size is limited within several micro or even nanometers. Due to the rapid development of the demand in electrical and integration device, MEMS technology has

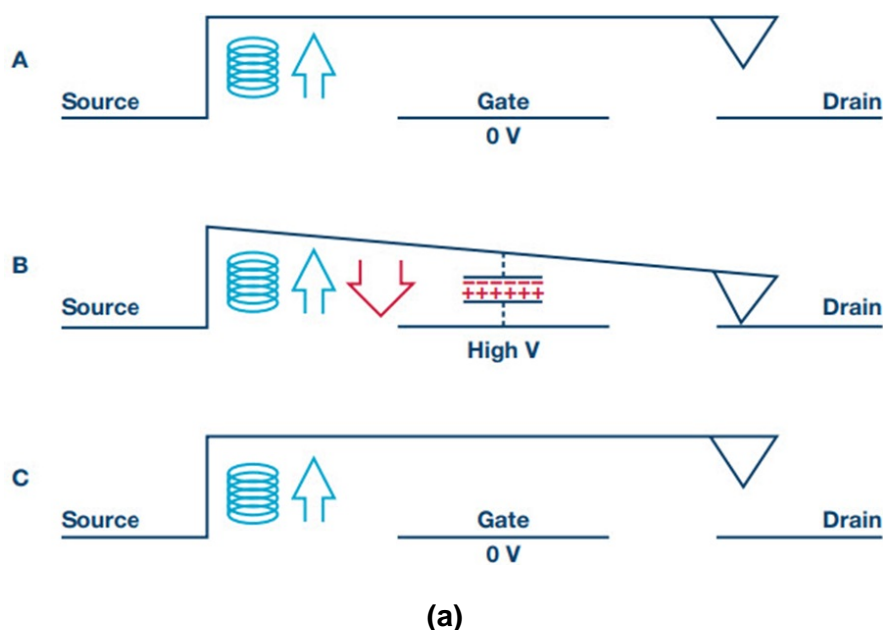
received much attention as an efficient and effective technology making the circuits and device more integral and high performance. Notably, the MEMS switches have raised great consideration as one of the valuable potential applications of MEMS technology.

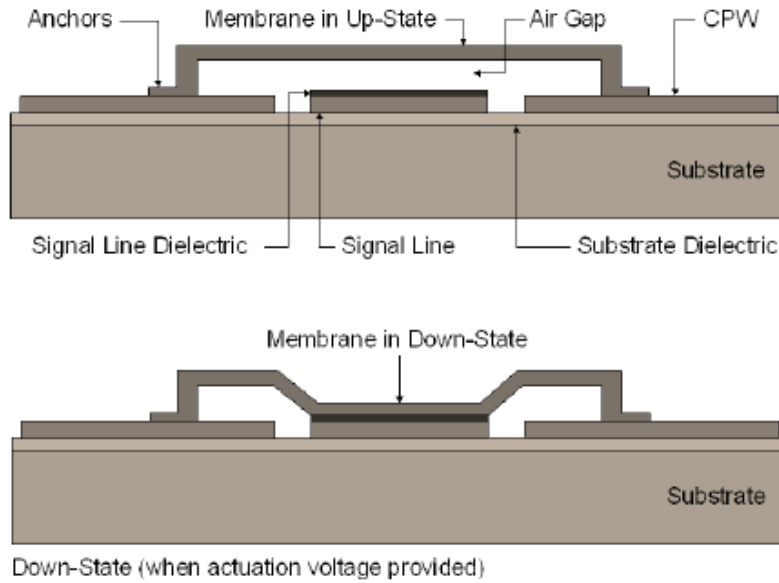
### 1.1.1. A brief history of MEMS switches

Prior to the invention of the MEMS switch, high-frequency switching was accomplished by mechanical or reed relays invented in the 1970s. In the last ten years, MEMS technology has seen rapid growth with the emerge of a large number of supersensitive sensors, nanorelays, micromechanics, microstructures and control elements like accelerometers, pressure sensors, micro-manipulators, etc [1-3].

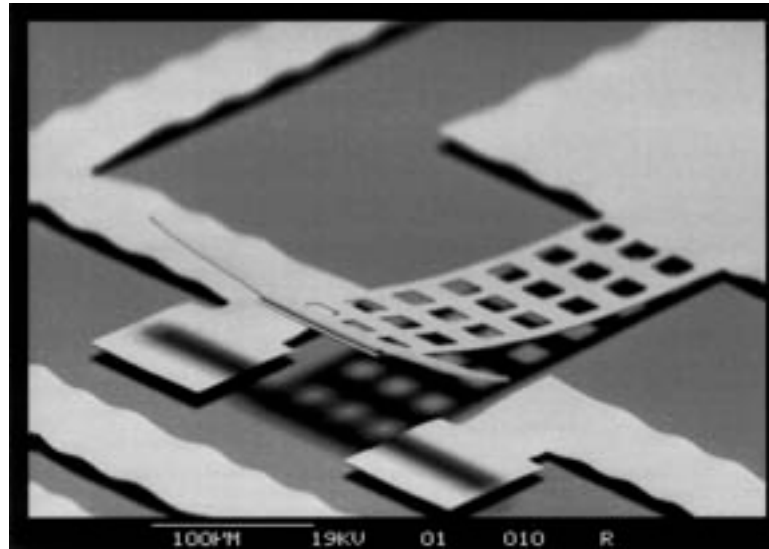
Some of them have been commercialized and others are about to be introduced into the market. The earliest MEMS switch is demonstrated by Petersen in 1979 who developed a 0.35  $\mu\text{m}$  thick, metal-coated electrostatic cantilever switch [4]. However, due to the limitations of the manufacturing process, MEMS switches have not made much progress in the following ten years. From the 90s, MEMS switches have made tremendous development. In 1991, a rotary transmission line switch was produced [5] and in 1995, surface micro-machining was created to make cantilever switches [6]. Some cantilever switches are shown in figure 1.1.

Meanwhile, many membrane switches were developed. In order to reduce the threshold voltage of the switch and improve the on-off stability and energy handling capability of the switch, MEMS switch was designed with the structure of spiral cantilever and large excitation plate later. The switch is a key component of microwave signal conversion.





(b)



(c)

**Figure 1.1:** General MEMS switches shape and function mode. (a) MEMS switch actuation process, A and C show the switch turned off, B shows it turned on [7]. (b) The operational principle of MEMS switch in ON and OFF [8]. (c) Micro-relay with electrostatic actuation [9].

### 1.1.2. Advantages of MEMS switches

In applications with frequencies below 1 GHz, transistors and relays are still preferred. They are cheap, low-loss, easy to integrate and widely used. When the solid-state electronic switch is above gigahertz, the loss begins to increase and it becomes difficult to integrate into the switch. In this case, the advantages of the MEMS switch become obvious. They are superior to solid-state electronic switches in electrical performance. Even at the high-

frequency domain, the insertion loss of the MEMS switch can easily reach a lower level than other switches.

**Table 1.1:** Performances Comparison of Conventional Switches and MEMS Switches

Parameters	MEMS Cantilever	GaAs PIN	FET Transistor	Ref
Steady-state Power consumption (mW)	0	25	0	[10]
Linearity	Yes	No	No	
Capacitance (fF)	11	110	100	[10]
On resistance ( $\Omega$ )	0.22	1	5	[10]
Loss (dB) in Frequency at X-band (10 GHz)	0.3/bit	1.2/bit	-	[11]
Turn-on voltage (V)	20 – 80	3 - 5	3 - 5	[12]
Response Time	1 - 300 $\mu$ s	1 – 100 ns	0 – 20 ns	[12]
Insulation level	Very high	High	Normal	[12]
Lifetime	$430 \times 10^9$ cycles	-	-	[13]

Nowadays, PIN and FET semiconductor switches are widely used in high-frequency communication. It can be easily seen from the comparison that with the increase of frequency, there are not able to be used as switches anymore. On the contrary, the MEMS switches with slits and metal contacts can ensure high insulation in high frequency through the opening and closing of metal contacts. This is one of the most important reasons that it gets highly expected in high-frequency communications. Moreover, the insulation performance can be modified according to the gap's dimension. So the MEMS switches have shown great potential in markets of mobile phones, laptops, gaming, Tablets which enable

structures redistributed inside electronic devices. The technology of MEMS switches also aims at improving performance and lower the limitation of devices' working ambience. Table 1.1 presents the comparisons of conventional switches and MEMS switches in multiple aspects.

From the Table, it is easy to see the advantages of MEMS switches. Take an example of FET switches, it almost lost the switch function when the frequency reaches 40-100 GHz. Similar degradation of PIN diode switches occurs at the high-frequency band. Besides, the MEMS switch has merits in low power consumption, high cut-off frequency, and good isolation.

To conclude, compared to traditional P-Intrinsic-N (PIN) diodes and field-effect transistor (FET) switched, MEMS Switches have advantages showed as following:

- Reduce the contact resistance and diffusion resistance in Ohm contact which results in lowering Ohmic loss
- No power consumption on steady-state
- Low capacitance
- Low resistance after switching on
- Low loss in the high-frequency domain
- Very good insulation properties when switching off

#### **1.1.3. Requirements for MEMS switches**

Combined with mechanical and electronic technologies, the research of MEMS Switches has been focused on manufacturing ultra-small size systems for many years. These following features are the main requirements of MEMS Switches for nowadays design.

- Devices can serve the basic function as a switch, controlling circuit on and off
- The dimension of the device ranges from micrometers to millimeters and smaller
- The process should be compatible with standard Si manufacturing technologies
- Wafer level manufacturing gives merit of low cost
- Switches can be used under a safe consideration without current leakage or other dangerous circumstances

#### **1.1.4. Issues and future work**

Since the 21st century, the development of MEMS technology based on Si has made great progress. With the rapid expansion of the application field of MEMS, the performance of Si materials limits the application performance and utilization range under extreme conditions such as high temperature, high frequency, strong radiation, and chemical corrosion. On the other hand, high-density integration and miniaturization require the MEMS switches to avoid

electric leakage and function in low power consumption, good isolation, and high frequency. Therefore, the search for new advanced materials that own good electrical, thermal, mechanical properties has become a new trend of development and attracted much attention. Among many semiconductor materials, SiC has obvious advantages in electrical conductance, mechanical strength, thermal performance, corrosion resistance, and is compatible with Integrated Circuit (IC) technology.

At the same time, the development of silicon carbide devices nowadays mainly focuses on the fabrication process of chip structure, such as avoiding defect percentage of silicon carbide, trying to have low efficiency of epitaxy, many other special requirements of the doping process, temperature resistible of matching materials, and so forth. Many research has been shown to characterize the physical properties of silicon carbide. It will be interesting to show this material can be utilized in applications which can benefit from its properties.

As advanced materials with special physical and mechanical properties, CNT coated with SiC has many potential advantages in making MEMS switches: smaller size, more efficiency, lower switching loss, high switching frequency, and the ability to work at a high temperature [3]. Miniaturization and high-temperature resistance make these devices more widely used. Therefore, it has the potential to become the preferred alternative material in the application under extreme conditions in MEMS.

## **1.2. Materials in this work**

### **1.2.1. Carbon nanotubes for microswitches**

As mentioned before, MEMS switches have many advantages in some conditions. But also, the disadvantage is obvious that it needs much higher voltage supply (20 – 100 V) compared to conventional PIN or FET (up to 5 V). The high voltage power will decrease the lifetime of switches and influence the devices' reliability. Therefore, we intend to find out a solution to improve the lifetime, enhance the reliability of the device.

In contemporary researching field of microscale electrical systems, much ink has been spilled about new materials or composite materials, especially one dimension and two dimension materials as carbon nanotubes and graphene partly due to their low dimension and small scale to be able to integrate device smaller.

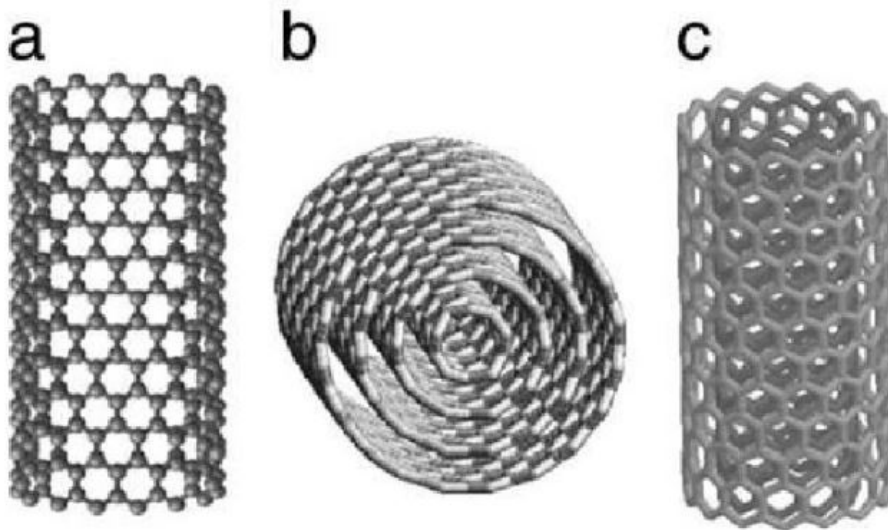
In 1991, Iijima Chenguao first discovered carbon nanotubes from carbon fibers in arc-discharge. In 1992, researchers found that carbon nanotubes (CNT) exhibit special conductivity of semiconductors and good conductivity depending on the structure of the tube wall. Since then, more and more research has been done to show its particular properties and expected applications of CNT.



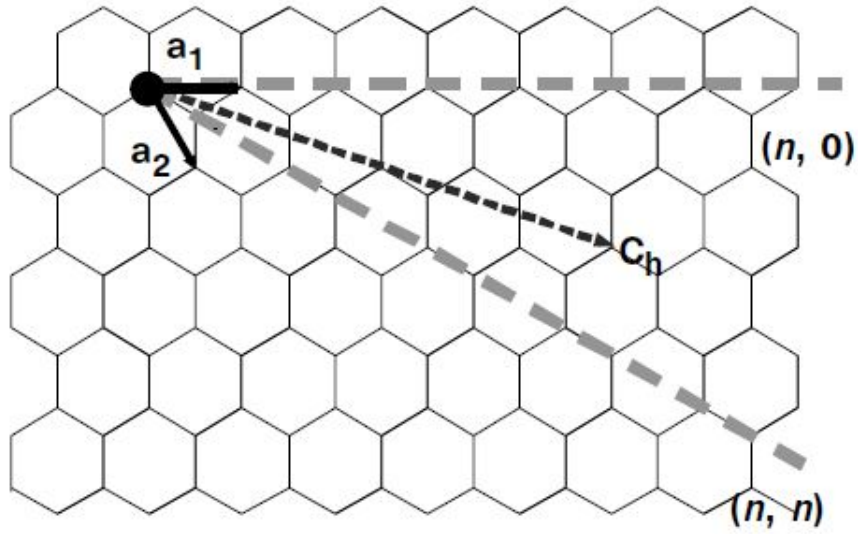
### 1.2.1.1. What is CNT?

Carbon nanotubes are nanotubes with single or multi-layer graphene sheets curled around the central axis at a certain helical angle. The hollow tube forms a cap-like structure at both ends and becomes a closed tube structure at one end or at both ends. The diameter is generally 1 - 30 nm and the length can be micro to millimeters. As a one-dimensional crystal, CNT can be classified into single-walled carbon nanotubes (SWCNT) and multi-walled carbon nanotubes (MWCNT) by layer. SWCNT can be seen as a single layer of a graphene sheet curled while MWCNT can be seen as a number of SWCNTs concentric overlapping. Each layer of nanotubes is a cylindrical surface consisting of a hexagonal plane formed by the complete bonding of carbon atoms through  $sp^2$  hybridization. The chirality of graphene sheets determines the diameter, helicity and lattice constants of CNTs, thus determining the physical properties of CNTs. Figure 1.2 depicts the conception of carbon nanotubes structure as Single-walled Carbon Nanotubes (SWCNT), Multi-walled Carbon Nanotubes (MWCNT), and Double-walled Carbon Nanotubes (DWCNT) respectively.

Based on the chirality, single-wall CNT can be divided into zigzag and armchair. Figure 1.3 shows the illustration of chiral vector  $\mathbf{C}_h$  and integer indexes (n, m) which are the definition of the chirality. A defect-free SWCNT can be presented as the vector  $\mathbf{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2$  where  $\mathbf{a}_1$  and  $\mathbf{a}_2$  are the lattice vector, and (n,m) the chiral indexes. The chirality of carbon nanotubes has implication on its electrical properties and this will be further discussed in chapter 2.



**Figure 1.2:** Schematic illustration of different structured CNT (a) Single-walled Carbon Nanotubes (SWCNT); (b) Multi-walled Carbon Nanotubes (MWCNT); (c) Double-walled Carbon Nanotubes (DWCNT)



**Figure 1.3:** Schematic of a two-dimensional graphene sheet illustrating lattice vectors  $\mathbf{a}_1$  and  $\mathbf{a}_2$ , and the roll-up vector  $\mathbf{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2$ . The limiting cases of (n,0) zigzag and (n,n) armchair tubes are indicated with dashed lines. As represented here, the angle between the zigzag configuration and  $\mathbf{C}_h$  is negative [14].

#### 1.2.1.2. Advantages of CNT

Nowadays, as Si-based materials have almost reached its physical limitation, advanced nanotechnology has switched to the investigation of nanomaterials which have distinct advantages of traditional materials for specific application, like carbon nanotubes. As the typical and original material of one-dimensional and two-dimensional material, CNT has unique properties such as customized shape, nanoscale size, high porosity, large surface area to volume ratio. The hydrogen storage and thermal conductivity that results in huge amount of applications involved in microelectronic devices, field emission devices, scanning tunneling microscopy needle tips, information storage, supercapacitors, thermally conductive materials, special adsorption materials, lithium batteries, proton exchange membranes, catalyst carriers, composite materials, and so on. All of these excellent properties give CNT a good perspective and prerequisite of implementing in small-scale devices.

To be more specific, carbon nanotubes have lots of distinguished properties and capabilities in electricity, mechanism, like high directional stiffness [15], large mechanical strains [16], thermal stability [17], flexibility [18], etc.

However, when an ideal single carbon nanotube with excellent mechanical properties is fabricated into macro size, its performance is often far below the theoretical value. The main reason is that the carbon nanotubes are too short in length, and the elements are attracted by van der Waals force. Under the action of tension, the carbon nanotubes are prone to slip

and cannot make full use of the intrinsic high strength of carbon nanotubes. The porous properties of CNT make it hard to behave as a monolithic solid cantilever. Even after densification in solutions, it is still not possible for CNT bundles to have a linear and elastic strain-stress relationship within any range. This makes it hard to be controlled by electrostatic force as a MEMS switch. Therefore, extra material for coating is considered to be the potential method for adjusting the bundles' mechanical properties. Previous work in our group has shown that thicker silicon carbide coating will enhance the CNT bundles' compressive strength and stiffness. In this case, silicon carbide is considered to be the coating material for changing the mechanical properties of CNT bundles.

### **1.2.2. Silicon Carbide**

Silicon carbide is a typical representative of wide bandgap semiconductor material. It has many excellent characteristics, such as wide band gap, high breakdown field, high thermal conductivity, high saturation rate of electron drift, low dielectric constant, good conductivity, stable chemical performance, and good wear resistance. These properties make it a potential semiconductor material working at high temperature, high frequency, high-density integrated high power electronic devices.

As the desirable mechanical and physical properties of CNT with SiC coating by previous work, the compressive strength and the elastic modulus increase exponentially as a function of the coating thickness [19] which gives it a possibility to control the mechanical properties of CNT bundles.

Only CNT bundles will be too soft to behave as a cantilever and pure silicon carbide will be too stiffness to be actuated in a relatively low voltage. Combining the MEMS technology and advanced materials as CNT coated with SiC, there seem to be more capabilities to manufacture micro scale switches which have the requirements such as extremely small scale, Si-based industrial compatible process, high throughput, high sensitivity, reliability, and robustness. Furthermore, all of them are robustness materials which will enable the devices to be more stable and steady.

With the high demand for miniaturization and thermal conductivity of semiconductor devices in the market, SiC has got much attention in the field of semiconductors [20].

Silicon carbide has a long history since it has been found. But it is not popularly utilized until it has been artificially produced. The SiC is first discovered by Edward G. Acheson in the laboratory during the experiment of electro melting diamond in 1891, which was misrecognized as a mixture of diamonds. In 1907, the first silicon carbide crystal light emitting diode was born. In 1955, Lely produced needle-like 3C-SiC by seedless sublimation, which laid the foundation for the development of SiC. In the early 1990s, Cree Research Inc

improved Lely's method to grow 6H-SiC, made it commercialized, and successfully fabricated 4H-SiC in 1994. This breakthrough immediately triggered a surge in the research of SiC crystals and related technologies. Nowadays, in the global market, there are many companies have involved in the business of SiC such as Cree, Dow Corning, SiCrystal, Dow Corning, II-VI, Norstel, Mitsubishi Electric Machine, Infineon and so on. In 2018, Infineon announced a \$139 million acquisition of Siltecta, a start-up, who acquired an innovative technology called ColdSpilt for cutting silicon carbide wafers, for further expansion in the silicon carbide market. X-Fab and Roma had also announced that they would expand their SiC market. It can be seen that SiC is highly expected in the global market by power semiconductor companies.

### **1.3. Problem statements**

None CNT with SiC coating MEMS switches have been shown up to now. Only some researches have shown the possibility of achieving small scale switches with CNT [21-25]. Due to its low stiffness, most of the switch structures are limited by designing as suspended single nanotubes which the two terminals are connected to metal substrates. The pull-in voltage is normally at several volts. In order to extend the utilization and structure design possibility, a mechanical property tunable mixture of CNT and SiC need to be explored.

### **1.4. Proposed Solution**

With the current state problems proposed previously, we found the solutions as follow. Previously in our group, we investigated the vertical growth and multi-dimensional characterization of CNT [26-30], using metal catalyst on a different substrate [29], conformal coating with SiC by LPCVD [19, 31, 32], and methods to make them horizontal [33-38]. With depositing oxide as a carrier and the sacrificial layer, cantilevers will be able to be suspended after vapor HF etching. Also, electrical and mechanical properties will be characterized by multiple measurements such as Raman spectroscopy measurement, resistance measurement, contact resistance measurement, frequency testing, reliability testing.

This research focuses on designing and fabricating microscale switches based on compound materials CNT conformably coated by SiC. With self-directed folding techniques, it shows the success of establishing horizontal CNT cantilevers. Moreover, one of the novelties is that this work also combines the attraction system design.

### **1.5. Thesis outline**

This research is mainly at investigating and demonstrating that CNT coated with SiC can be used as sTable, robust and high voltage level MEMS switches. The research showed by this thesis will be discussed along with these questions independently. In chapter 2, some

background knowledge will be provided, mainly focusing on the electrical and mechanical properties of CNT and SiC. At the same time, fundamental physical theory of electrostatic and RF micro switches will be demonstrated. In chapter 3, we systematically investigate the mechanical and kinematic behavior of this new designed micro switches made of CNT coated with SiC through finite element analysis (FEA) modeling approach in software COMSOL Multiphysics. Special design in combination of electrostatic and RF actuated microswitch structure will be displayed. Various parameters of switches' dimension will be provided, thereby showing potential and predicting relations between size features and switches' performance. Our models account for the mechanical properties of densification CNT cantilever, which contains multiple influences from SiC coating, contact and the frictional force caused by densification, van der Waals interactions and so forth. In chapter 4, the mask design topology will be presented. Many test structures as Transfer Length Measurement (TLM), Electrical Linewidth Measurement (ELM) structures are combined in mask design. This will be followed by the fabrication details and process flowcharts in chapter 5. Henceforth, chapter 6 focuses on the characterization of the effective electrical conductivity of SiC-coated CNT Micro Switches. The quality of CNT and deposition of SiC will be defined by Raman Spectroscopy characterization experiment. The thermal conductivity will be explored by a heat transfer experiment. Moreover, further discussions will be given after showing measurement results. Chapter 7 will give the conclusion and perspectives of future work.

## 2. Background Theory

### 2.1 Introduction

This chapter serves as background information of carbon nanotubes' electrical properties, mechanical properties, growth mechanism and methods, previous work on CNT switches, silicon carbide's electrical properties, mechanical properties, previous work on CNT bundles coated with SiC.

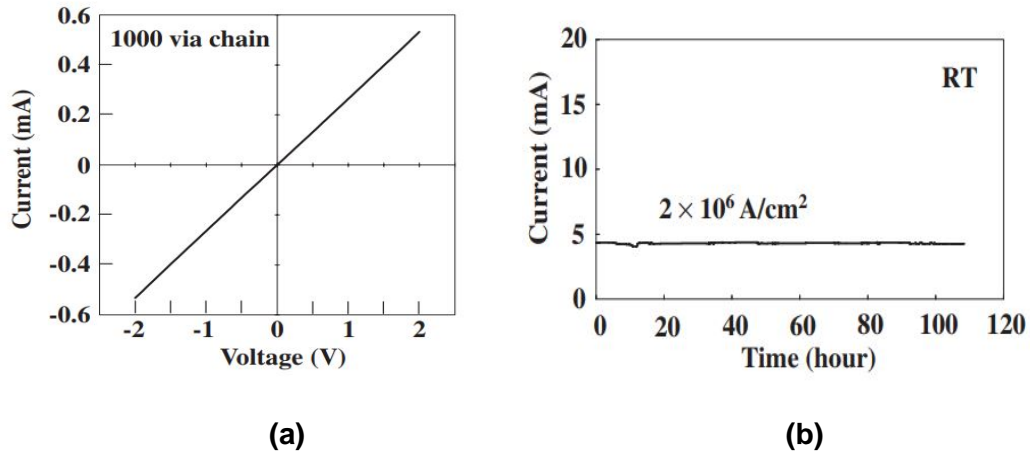
### 2.2 Properties of CNT

#### 2.2.1 Electrical properties of CNT

Under the influence of quantum effect, the conductivity of SWCNT can be shown as metal, semi-metal or semiconductor with different chiral angles and diameters [1, 16]. As mentioned before, the vector indexes  $n$  and  $m$  can be used to describe the chirality. Also, different parts of the same carbon nanotube can also exhibit different conductivity due to structural changes. When  $n - m$  is a multiple of 3, CNT is semi-metallic, which is a conductor. Otherwise, it is a semiconductor [1]. In addition, carbon nanotubes (CNTs) can transform from metal to insulator under the magnetic field, which is affected by CNT diameter, chirality, and direction of the applied magnetic field. In our work, the MWCNT is more similar to copper in electrical conductivity as Table 2.1 shows.

Some research has measured that CNT bundles have a linear IV characteristic showing that resistance was  $5 \Omega/\text{via}$  at a voltage of 100 mV at room temperature and the density of around 1000 tubes per  $2 \mu\text{m}$  diameter via [17]. Besides, figure 2.1 shows no obvious degradation in their experiments at the estimated current density of  $2 \times 10^8 \text{ A}/\text{cm}^2$ . Some research also showed, in theory, metallic nanotubes can carry an electric current density of  $4 \times 10^9 \text{ A}/\text{cm}^2$  [39].

The resistivity of SWCNT is as low as  $10^{-6} \Omega \cdot \text{cm}^{-1}$  at room temperature which is much better than typical conductive metals [40]. The lowest resistivity reported for MWCNT amounted to  $5 \times 10^{-6} \Omega \cdot \text{cm}^{-1}$  which was not good as SWCNT probably due to the fact that MWCNT has higher diameters than typical SWCNT [41].



**Figure 2.1:** Electrical properties of CNT [42]. (a) IV characteristic of Carbon Nanotubes Bundles; (b) Current in the test showed no visible degradation.

**Table 2.1:** Electrical conductivity of CNT and Cu [43]

Material	Electrical Conductivity (S/m)
Carbon Nanotubes	$10^6 - 10^7$
Copper	$6 \times 10^7$

### 2.2.2 Mechanical properties of CNT

The mechanical strength of materials is one of the most important properties of materials, especially for MEMS technology. Carbon nanotubes are considered to be one of the strongest materials found at present. Its Young's modulus is over 1 TPa, its tensile strength is over 100 GPa which is over 10 times than that of T1000 carbon fibres. In addition, structural defects and disordered orientation in carbon nanotubes will all lead to the decrease of fibre strength. More mechanical properties are presented in Table 2.2.

**Table 2.2:** Properties of CNT

Characteristics	Comments	Ref
Young's Modulus	$472 \pm 215$ GPa	[44]
CNT Outer Diameter in Our Process	3 nm	[32]

CNT Inner Diameter in Our Process	9 nm	[32]
Bending Strength of MWCNTs	$14.2 \pm 0.8$ GPa	[45]

## 2.3 Carbon Nanotubes Growth

### 2.3.1 Growth Mechanism

The CNT bundles can be produced by current arc-discharge [46], laser ablation [47], pyrolysis of Hydrocarbons [48], ion beam irradiation [49], polymerase chain reaction [50], and Chemical Vapour Deposition (CVD) [51]. Nowadays, the arc-discharge, laser ablation, and CVD are the three most commonly used methods for CNT producing.

The conventional arc-discharge method is implemented by graphite electrodes. In the ambient of inert gas such as helium or argon, the graphite in anode will be consumed, and then the CNT will be generated at the cathode. This method is comparably simple and easy for applying. Even though the ratio of multiple productions can be adjusted by controlling the catalyzer and percentage of hydrogen, it is still hard to produce pure SWCNT or MWCNT because the by-product of C60 and amorphous carbon will also be generated together and hard to remove completely. Later, some research showed that the electrodes replaced by the graphite composited with a metal oxide such as Fe, Co, Ni, and Mo can increase the production ratio of SWCNT and reduce the by-product effectively. Alternatively, much energy can be saved if the lithium chloride is used as the electrodes [46].

Laser ablation is the method to utilize the laser to create gas phase carbon. A graphite target mixed graphite with metal catalyzer is put in the middle of a long quartz tube which is heated up from 500 - 1000°C inside a furnace. There is one inlet port with inert gas and one exhaust port at both ends of the tube. The graphite target will generate gas phase carbon which will flow from the high-temperature region to low temperature region with catalyzer particles and then generate CNT. This method can produce high-quality SWCNTs that are less defection with complete structure. However, it is a high-cost process with low efficiency [47].

The thermal decomposition of hydrocarbon vapor is to generate CNTs by decomposing hydrocarbon solid under high temperature. This method is comparably stable and does not need catalyzer. But it is not suitable for large scale and continuous production due to the limitation of precursors [48].

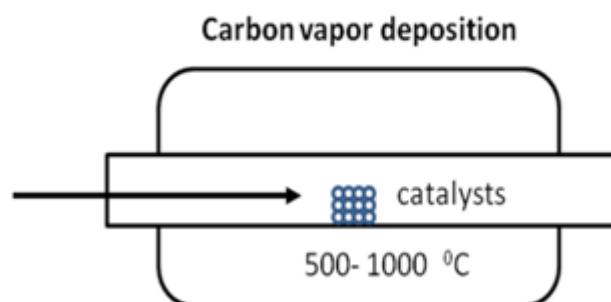
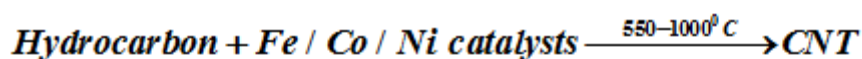


In the Chemical Vapour Deposition process, CNTs were synthesized by pyrolysis of carbon source gases (methane, acetylene, ethylene, propylene, benzene, carbon monoxide and so forth) at relatively low temperatures (500 - 1000°C) using nanoscale transition metals or their oxides as catalysts. The nanometer thin catalyzer layer will cover the substrate surface, which can help with activating and decomposing the hydrocarbon under a relatively low temperature after the catalyst being broken into small particles. During the process, an etching gas like  $H_2$  or  $NH_3$  is used to react with a-C to remove redundant carbon. There are two growing directions of CNTs called tip growth that catalyst particles will be lifted so the CNTs grow under the catalyst and base growth that CNTs grow on the top of the catalyst. Due to the Van der Waals interaction, CNTs can easily be aligned vertically during the growth. Plasma can also be used to help with vertical alignment. Horizontal growth can be implemented by several methods like liquid induced and densification. This method has the advantages that it is simple, reproducible, higher purity with gas phase by-products, large output, and low reaction temperature. In other words, it is a lower energy consumption. However, the CNTs have irregular diameters and shapes, and the catalyst must be used in the preparation process. Some research has been done to control the structure of carbon nanotubes by controlling the arrangement of catalysts on the template [51].

Besides, works of literature also showed more methods of CNTs growth like hydrothermal crystallization method, solar energy method, electrolysis method, sol-gel method [52-55].

### **2.3.2 Growth Process**

In our work, CVD is considered for growing CNTs due to its large scale production ability and low temperature compatible. And the most important part is that with CVD, the CNT can grow at the desired location, which is not possible with most other methods. In this work, the AIXTRON Blackmagic (BM) CVD reactor is used. This tool allows operators to change the temperature, top heater, process time, gas pressure. Both Low-Pressure Chemical Vapour Deposition (LPCVD) mode and Plasma- Enhanced Chemical Vapour Deposition (PECVD) mode can be implemented in this tool. In this work, only LPCVD is used. See figure 2.2 for LPCVD deposition.



**Figure 2.2** Schematics for CVD deposition of CNT [56].

### 2.3.3 Challenges of CNT Growth

The first challenge of this work is how to make the CNT horizontal aligned, thereby making the cantilever switch. Also, making the bundles horizontalization and aligned to the desired direction under asymmetric substrates is quite important. The previous work has shown some methods of making bundles horizontal. However, it does not work well when bundles have been self-aligned during growth. The future work of this process can focus on improving the yielding and repeatability of horizontalization.

How to make a long length of CNT bundles is also essential to make this cantilever switch. However, during long time deposition, a thin film of carbons will also be deposited on the wafer, which will make the surface conductive everywhere. The future work can focus on finding a solution to remove this carbon layer without damaging the CNT bundles.

## 2.4 Properties and growth of SiC

As we said before in chapter 1, the excellent properties of SiC bring it a broad prospect of applications. A SiC molecule is composed of Si atom and C atom. The basic structure of SiC is Si-C tetrahedron, which belongs to closed-packed arrangements. There are more than 250 homogeneous polymorphs that have been found, which are produced by different unidirectional stacking modes.

As a semiconductor, SiC has the resistivity ranging from  $10^{-2}$  to  $10^{12} \Omega \cdot \text{cm}$  depending on the type and quantity of impurities in the crystal. The most important impurities are aluminium, nitrogen, and boron.

In addition to its good electrical conductivity, silicon carbide also has special mechanical properties. The hardness of silicon carbide is very high. Its Mohs hardness is 9.5, ranked second only after the hardest diamond in the world graded 10. It has an excellent thermal conductivity which can resist oxidation at high temperature.

See the typical mechanical properties of SiC as Table 2.3 below.

**Table 2.3:** Properties of SiC of coating thickness from 2 – 30nm

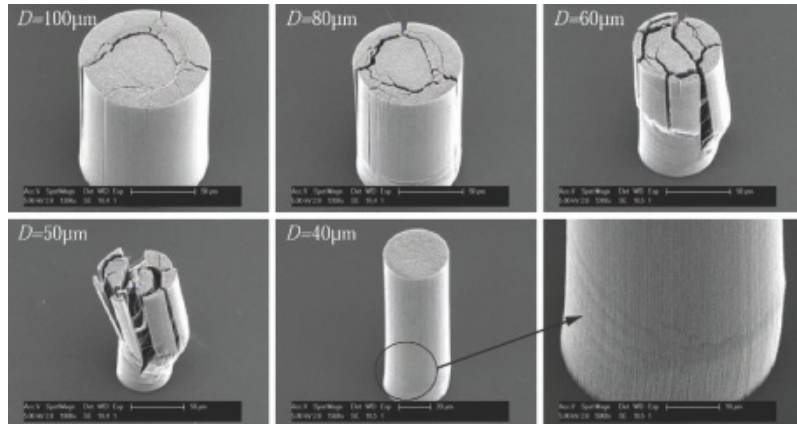
Characteristics	Comments	Ref
Density at 300K	3.1 - 3.2 g·cm <sup>-3</sup>	[57, 58]
Thermal conductivity	4.9 W·cm <sup>-1</sup> ·K <sup>-1</sup>	[59]
Young's modulus	292 - 459 GPa	[60, 61]
Poisson's Ratio	0.17 - 0.24	[62]
Strength	0.49 - 0.81 GPa	[62]

## 2.5 Coating SiC on CNTs

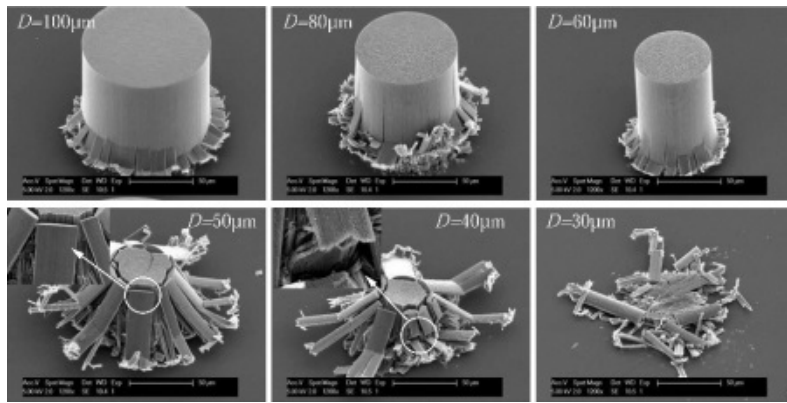
As the CNTs bundles are puffy and porous, conformal coatings can be used to fill the tubes, thereby changing the electrical and mechanical properties of CNTs bundles. In previous work, amorphous silicon carbide has been used as one of the coating material. In previous work, the test of compressive strength and coating thickness of carbon nanotube arrays with SiC has been done [32], see as figure 2.3.

The results show that the CNT mechanical properties varied when a different thickness of amorphous silicon carbide by LPCVD deposition was applied. Increasing the conformal coating thickness results in a strong exponential increase in compressive strength and stiffness. That is to say, the foam-like CNT arrays will lose its porosity and gain stiffness as the conformal coating of SiC get thicker [19, 32]. It has proven that the mechanical properties of CNT arrays can be modified by SiC conformal coating which laid the foundation for this work.

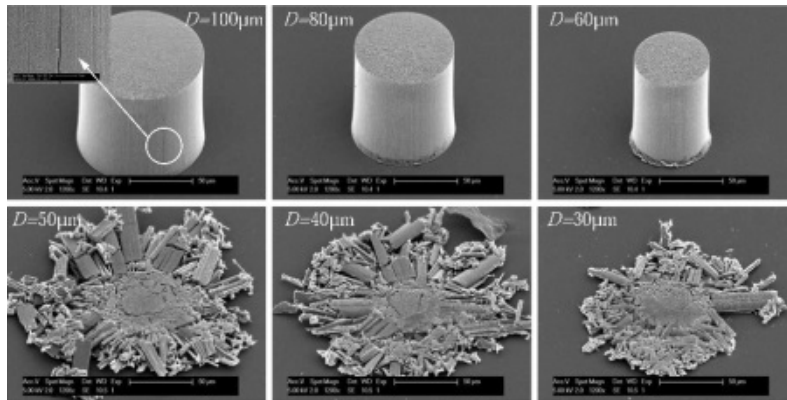
At present, the fabrication methods of SiC thin films mainly include PVD and CVD. In particularly, PVD mainly includes sputtering, ion implantation synthesis and Molecular Beam Epitaxy (MBE). In this work, SiC was deposited using furnace by the method of LPCVD. Compared to normal CVD, LPCVD can avoid impurities diffusion and migration, improve thin film conformity as well as increase deposition speed.



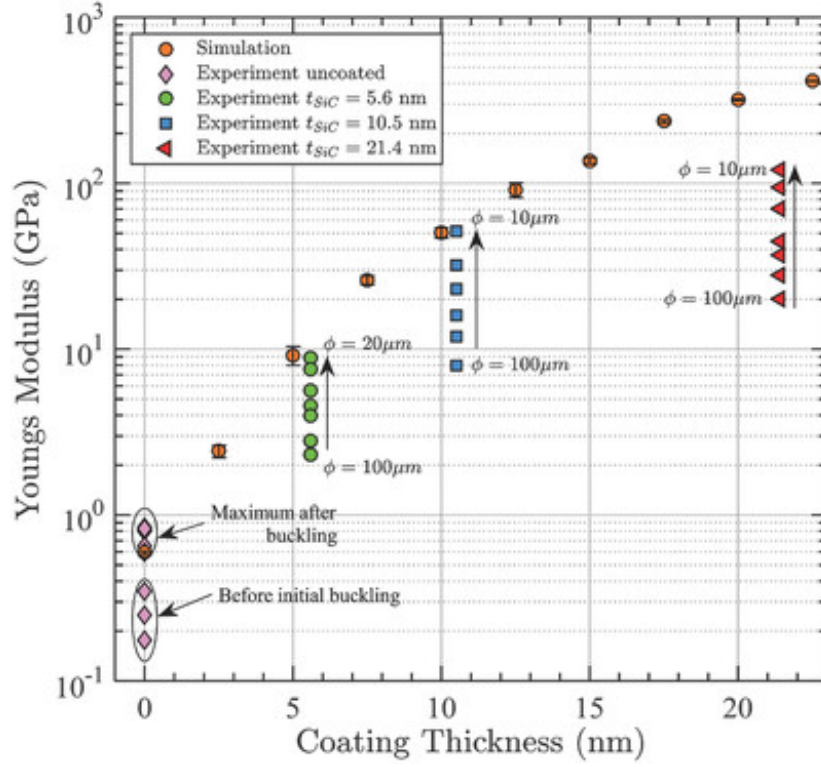
(a)



(b)



(c)



(d)

**Figure 2.3:** Compressive failure of CNT pillars coated with different thickness SiC. (a) Compressive failure of CNT pillars coated with 5.6 nm a-SiC; (b) Compressive failure of CNT pillars coated with 10.5 nm a-SiC; (c) Compressive failure of CNT pillars coated with 21.4 nm a-SiC. (d) Effective Young's modulus of coated and uncoated CNT arrays.

## 2.6 MEMS switches

Higher efficiency and robustness are key points in improving device performances. Therefore, electronic application downscaling has exerted a measure of influence on the semiconductor industry. It enables low cost and higher performance due to the effective utilization of wafer areas. MEMS Switches, in particular, are the devices developed under this conception. MEMS technology has been developed in the last a few decades based on the semiconductor manufacturing process which combines processes of lithograph, etching, surface micromachining, thin film technologies and so forth, focusing on manufacturing devices in micro size or even smaller size. Besides, depending on the advanced fabrication process, material science also throws a significant influence on downscaling technology.

In the following text, the common drive mode, types of MEMS switches and more advantages will be introduced.

### **2.6.1. MEMS switches drive mode**

There are several main drive modes of MEMS devices: electromagnetic, thermodynamic, shape memory alloy, piezoelectric, electrostatic. Electromagnetic drive mode and electrostatic drive will be mainly elaborated.

#### **2.6.1.1. Electromagnetic drive mode**

Electromagnetic drive mode utilizes magnetic force, the interaction between magnetic fields or a magnetic medium, to drive the switch to achieve closure. And it is popular in the devices of a traditional relay. The advantage of the electromagnetic drive is a small drive voltage, a large range of motion, not easy to breakdown, and can achieve larger-scale non-contact drive.

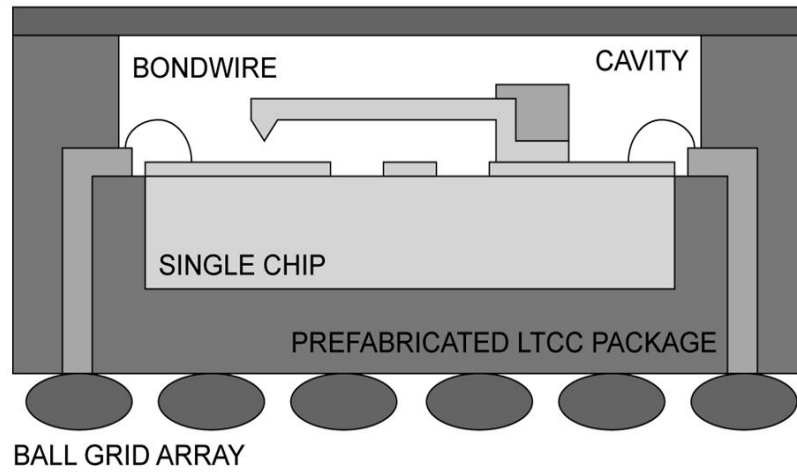
#### **2.6.1.2. Electrostatic force**

The electrostatic drive is a relatively common used drive mode which utilizes the Coulomb attraction between the upper and lower plates to achieve the opening and closing of the switch. It shows lots of merits in low power consumption, simple and elegant structure, fast response and small volume. However, it also shows shortcomings in high drive voltage and requires protection from breakdown. One key point to optimize electrostatic drive mode is to reduce drive voltage by choosing appropriate material, size, and dielectric.

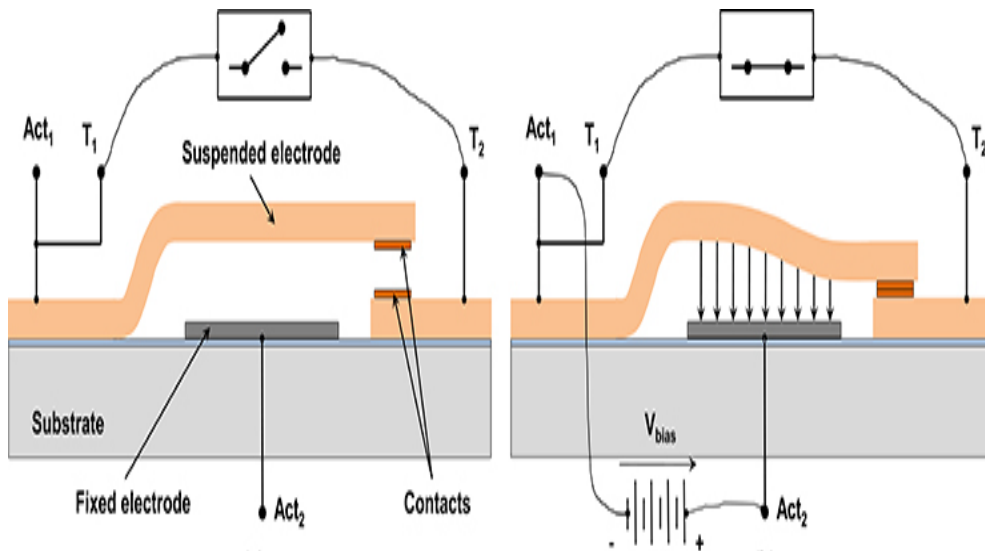
### **2.6.2. MEMS switch structures**

In considering of microstructures, MEMS switches can be classified into a cantilevered switch and fixed beam switch. Both cantilevers and membrane are commonly used in the structure design. In accordance with the switch contact mode, MEMS switches can be divided into the capacitive-coupled switch and an Ohmic contact switch. Series contact switch and parallel resistance switch are comparable common used. Figure 2.5 shows some typical schematics of cantilever MEMS switch structure.

One terminal of the cantilever is fixed to the substrate and isolated from the other electrodes. One extra electrode is supplied under the suspended cantilever to provide the attraction force. Also, there is an electrode under the other terminal of a cantilever. When the switch is off, there is a gap between cantilever and contact pad. The cantilever will contact the bottom pad when the voltage supplied and the switch turned on.



(a)



(b)

**Figure 2.5** MEMS structures. (s) Single chip packaging of an ohmic cantilever MEMS switch; (b) Schematic cross-section of a cantilevered MEMS switch controlled through the electrostatic principle [9, 63].

## 2.7 Conclusions

This chapter mainly discussed the properties as well as gave some brief introduction to CNT growth and SiC conformal coating.

The electrical and mechanical properties of CNT and SiC are discussed respectively. As the dimension of CNT bundles is as large as micro level, the quantum effects can be ignored mostly. Electrical properties as conductivity and mechanical properties as stiffness will be the most important index for investigation. CNT can show different characteristic as

semiconductor, metal, and semi-metal. In our work, the MWCNT behaves as similar to copper. As the SiC has good behavior in electrical conductivity as well, coating CNT with SiC will not give negative influence in the aspect of conductivity. Besides, both CNT and SiC have high Young's Modulus. As the CNT bundles are porous and soft, SiC is potentially to change its mechanical behavior as enhancing its stiffness, thereby making the controllable MEMS switches cantilever feasible and doable. The thicker the coating, the more stiffness the mixture will be.

In addition, the drive mode of MEMS switches is discussed. The most common drive modes are electromagnetic, thermodynamic, shape memory alloy, piezoelectric, and electrostatic. In this work, electrostatics drive mode and electromagnetic drive mode are used to switch on and off independently. The cantilever will be used as the switch structure. Some typical cantilever structures of MEMS switches are shown, and the functioning mechanism is also discussed.



### **3. Horizontalization Technique Characterization**

#### **3.1 Introduction**

In practical, we typically need microscale CNT bundles to build MEMS switches. Particularly, as the bundles are porous, it cannot behave as an integrated solid block. Even though there are van der Waal forces between each tube, due to the weak interaction the behaviour of the bundle is still not predictable when outer stronger forces are introduced such as electrostatic force and the electromagnetic force. In this work, the most important function is to make the bundles horizontally flattened and aligned. Densification in the solution can help with condensed the bundles as well [1].

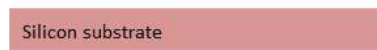
Because of the design requirement of electrostatic drive mode switches, there needs to be an electrically insulating gap between the actuated electrode and the substrate. There are theoretically three movement directions as along x, y, and z-axis in which a switch could move. However, due to the process limitation of the planar silicon technology, the first two directions are not practical. We chose the cantilever structure as the final design because it is easier to implement and compatible with standard MEMS micromachining.

Another problem came out that in order to make this cantilever structure, the CNT electrode needs to be aligned horizontally. In previous work, we introduced the methods to make CNT bundles horizontally aligned. As we use solutions for densification, we also implemented the folding technology with different solutions in this work.

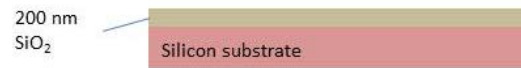
In this chapter, we will present two tests. First, IPA is used on wafer 1 for verifying whether the folding technology works and trying to find if any process procedures can be optimized to get better horizontalization results. Secondly, IPA, Acetone, Ethanol are used for testing the horizontalization capability of these commonly used solutions in the cleanroom.

#### **3.2 Mask design**

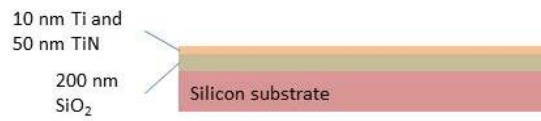
We used masks from previous work in our group designed by Cinzia Silvestri for the densification and horizontalization test. See figure 3.1 for detailed process. The wafer will be sputtered with a uniform 10 nm/50 nm Ti/TiN layer. Then the mask design of figure 3.1 is used for Fe lift-off. CNT bundles will only grow on the location with Fe evaporated. The mask patterns are shown in figure 3.2. Four blocks are designed in this mask, which contain different CNT bundle geometries. The specification for each pattern are shown in Appendix A.



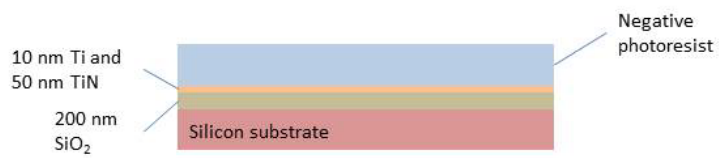
(a)



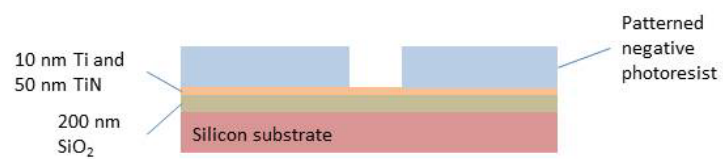
(b)



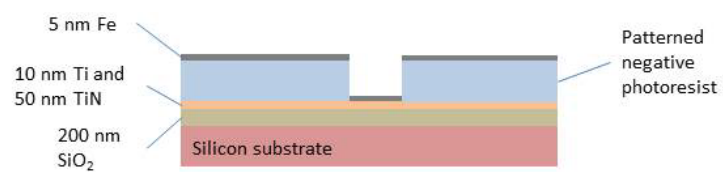
(c)



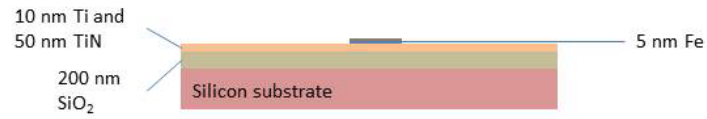
(d)



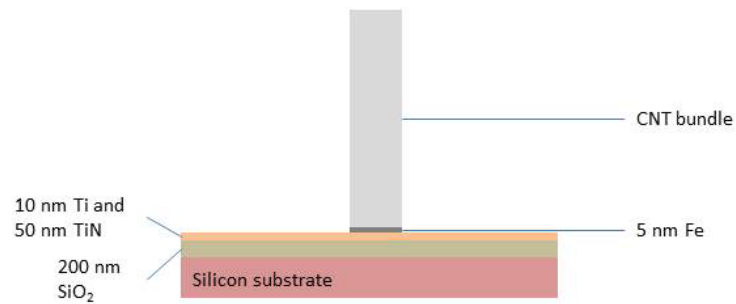
(e)



(f)

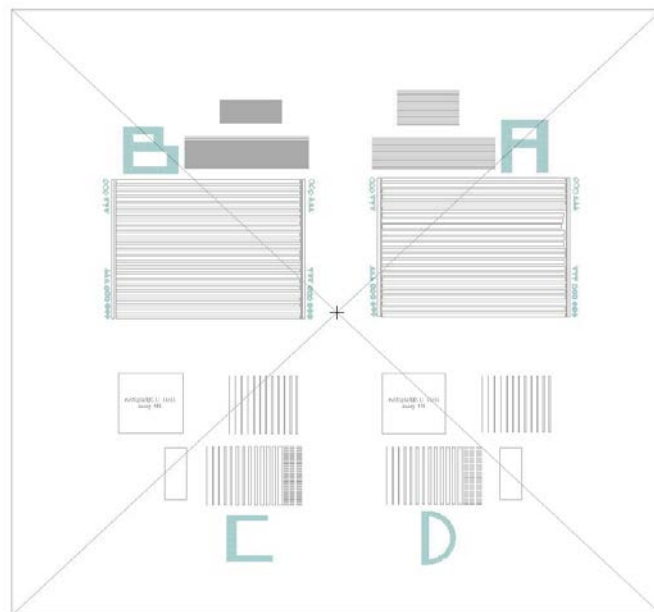


(g)

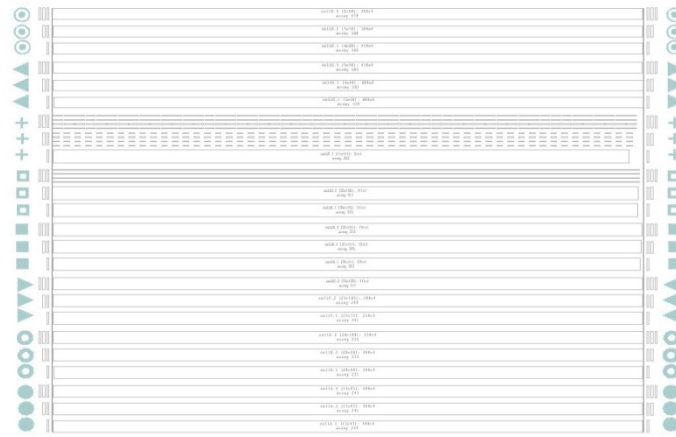


(h)

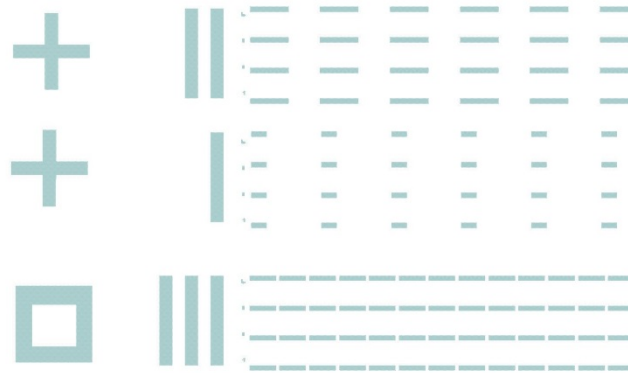
**Figure 3.1** Process of CNT growth on the catalyser layer with the unpatterned Ti/TiN metal layer. (a) P-type silicon substrate. (b) 200 nm oxide layer for isolation. (c) Sputtering with 10nm/50nm Ti/TiN. (d) Negative photoresist for lift-off. (e) Photoresist patterning. (f) 5 nm catalyser Fe evaporated. (g) Fe lift-off. (h) CNT deposition.



(a)



(b)



(c)

**Figure 3.2** Mask design of different patterns of CNT dimension. (a) Complete view of mask design; (b) Zoom in view of quarter A; (c) Zoom in view of several structures in quarter A.

### 3.3 Horizontalization test

#### 3.3.1 Preparation

Two wafers are split into pieces for the horizontal test. Wafer 1 use the recipe 3600 sec of CNT growth at 600 °C, using 700/50 sccm H<sub>2</sub>/C<sub>2</sub>H<sub>2</sub> at 80 mbar, which gives CNT bundle of 120 ± 50 μm long (big bundles with dimension at around 80 μm × 80 μm can give MWCNT growth up to 160 ± 20 μm). Wafer 2 use the same recipe in the 1800s which gives 100 ± 10μm height of CNT. Wafer with block symbol ‘A’ and ‘B’ are cut into three pieces respectively.

#### 3.3.2 Test Process

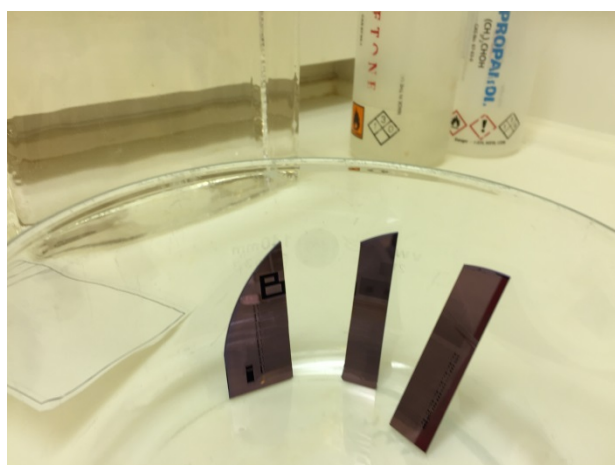
- Wafer 1

Four tiles are separately put into IPA in a vertical direction. Then it will be soaking in IPA for a certain amount of time as figure 3.3 shows. After this, the tile is carefully removed and also

dried vertically as figure 3.4 presents. Different parameters in the process such as the time for taking the samples in/out of the solution, the soaking time in the solutions, and drying time are recorded as shown in Table 3.1.



**Figure 3.3** Tiles are immersed in solutions.



**Figure 3.4** Tiles drying by vertically held of container's sidewall.

**Table 3.1:** Process records

Tile	Time of insertion (s)	Time of removal (s)	Time in solution (s)	Time for drying (min)
1	2	15	15	5
2	148 (solution is slowly added)	240	15	5
3	15	240	5	5

4	5	900	5	5
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- Wafer2

Six tiles will be supplied with the same process but solutions will be varied between IPA, acetone, and ethanol. Check for more details Table 3.2.

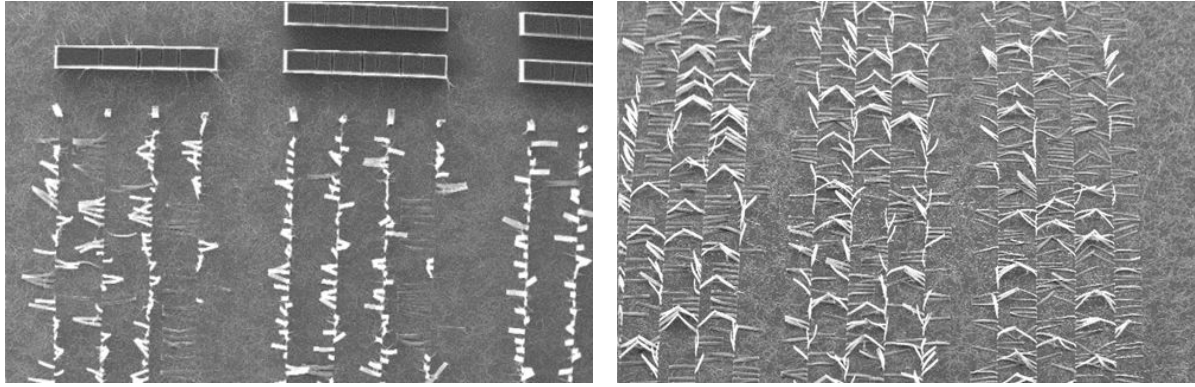
**Table 3.2:** Tile Soaking and Drying Time

Tile	Solution	Time of insertion (s)	Time of removal (s)	Time in solution (s)	Time for drying (min)
1	IPA	5	5	150	5
2	Ethanol	5	5	150	5
3	Acetone	5	5	150	5
4	IPA	5	5	300	10
5	Ethanol	5	5	300	10
6	Acetone	5	5	300	10

### 3.3.3 Result and Discussion

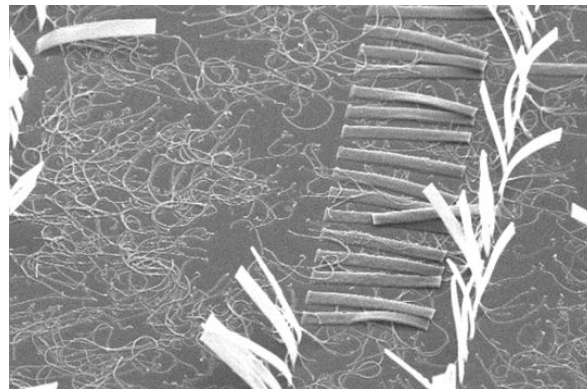
- Wafer 1 (3600 sec)

From Figure 3.5, it is shown that with structure width or length declining, more percentage of CNT fall to the right. When inspecting three columns of bundles for tile 1 - 4, we found that putting the tiles in IPA for a longer time (150 sec) will result into more folding CNT bundles (average 198/203) to the right direction than for short time of 15 secs (average 149/203). This means that a longer time in solution will give positive influence to the result. But immersion time of 240 sec in solution does not give significant influence of CNT bundles folding in the right direction (average 197/203). It is interesting to find that some CNT might fall in the opposite direction which gave a tent shape as figure 3.5 shows..



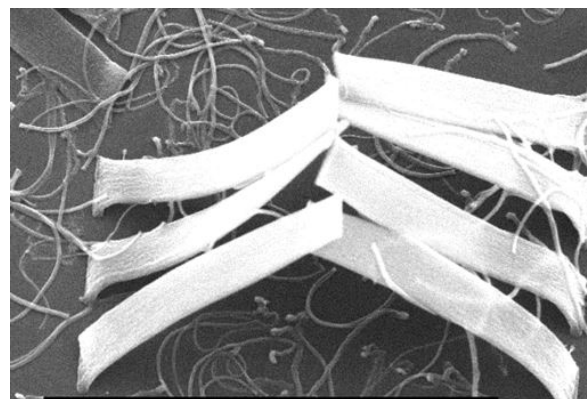
(a)

(b)



(c)

**Figure 3.5** Smaller Width of CNT will increase the number of horizontal bundles. (a) top view of CNT bundles after horizontalization (b) tilted view of CNT bundles after horizontalization (c) tilted and zoom in view of CNT bundles after horizontalization.

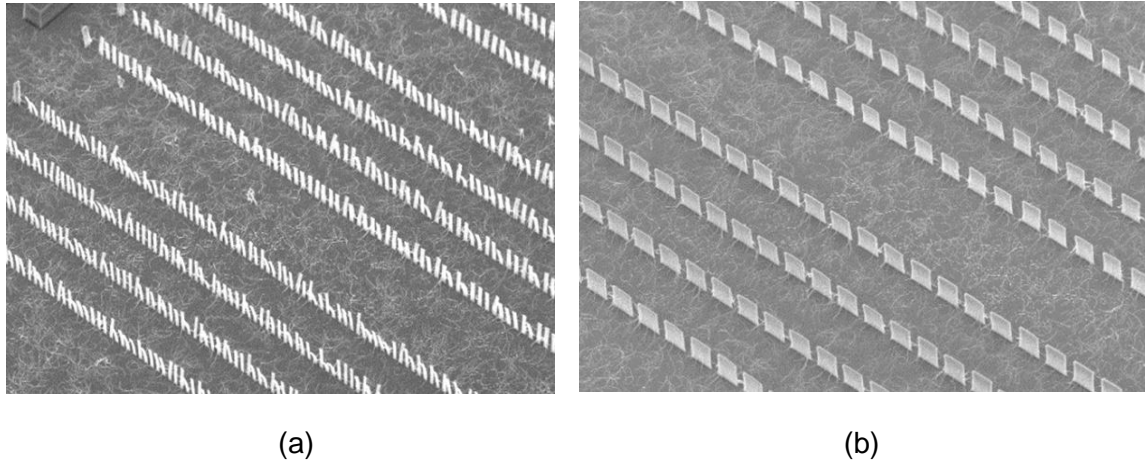


**Figure 3.6** Tent shape because of Wrong Horizontal Direction from Adjacent column

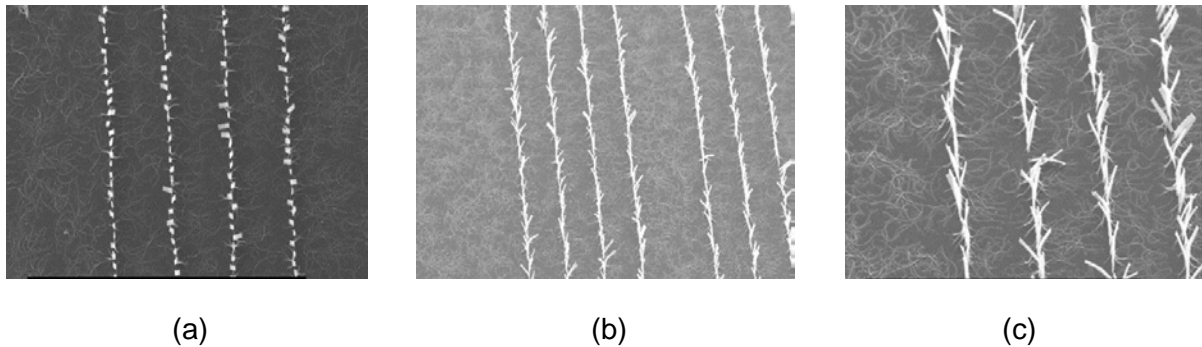
Also, only the last few columns of the mask design show good result in CNT horizontal as more than 80% bundles fell to the desired direction. The size ratio of that part is at  $3\mu\text{m} : 15\mu\text{m} - 3\mu\text{m} : 25\mu\text{m}$  (width : thickness). When the width increases, it is harder for the  $138 \pm 20\mu\text{m}$  long CNT to be folded into the horizontal direction.

- Wafer 2 (1800 sec)

Figure 3.6 shows columns with the smallest thickness ( $3\text{ }\mu\text{m}$ ). The height of CNT in this wafer is at around  $100\text{ }\mu\text{m}$  which results in all tiles that most CNT bundles are still standing only with bending for small angles even for the smallest width. But with the same structure, we can see there are still influence of different solutions from figure 3.7.



**Figure 3.6** Most CNT bundles are still standing only with little shape bending. (a) the second area of a wafer, block B. (b) third quarter of wafer, block C



**Figure 3.7** Same structure  $3\text{ }\mu\text{m} : 15\text{ }\mu\text{m} - 3\text{ }\mu\text{m} : 25\text{ }\mu\text{m}$  and same time 150 s in different solutions. (a) IPA. (b) Ethanol. (c) Acetone.

From the pictures, Ethanol seems to give a little bit more influence of the horizontal than IPA. But the difference is not obvious. There is either no dramatically difference can be seen between Ethanol and Acetone, only thing is that Acetone shows better performance than Ethanol in shape bending.

### 3.4 Conclusions

In order to make CNT cantilever switches, vertical CNT bundles need to be made solid and horizontal to show good mechanical properties and allow integration into planar MEMS technology. With liquid-assisted flattening approach, CNT bundles will show densification, thereby being able to build it both solid and horizontal.



From this test, we can see that the horizontalization of CNT is practical and feasible. At the CNT growth height at the range of 100  $\mu\text{m}$ , the width of CNT bundles should be controlled smaller than 3  $\mu\text{m}$ , and length from 15  $\mu\text{m}$  - 25  $\mu\text{m}$  in order to make the bundles horizontal. Increasing soaking time under 2 mins will have a positive influence in horizontalization, but no more significant influence when keep increasing soaking time. Meanwhile, CNT height under 100  $\mu\text{m}$  is not recommended for this method which means it should better be processed with growing CNT for more than 1 hour.

For horizontalization, both acetone, ethanol, and IPA are workable. In considering of fast drying, Acetone can be seen as the first choice. In considering of safety and less corrosion, IPA can be chosen.

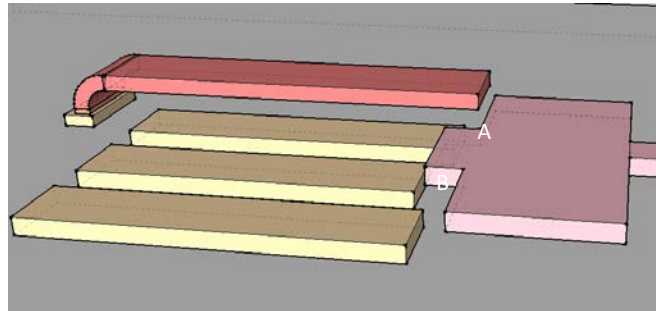
## 4. Structure Design and Simulation

### 4.1 Introduction

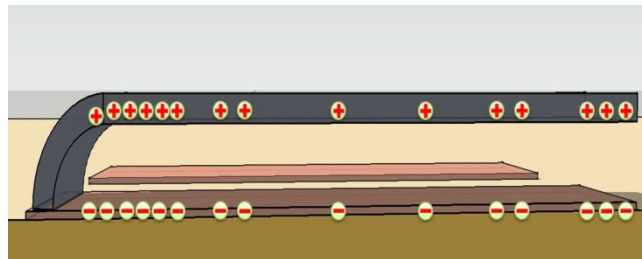
This chapter mainly introduces mask designs, modeling, and simulation results. First, the proposed CNT MEMS switch concept will be given. Then, five switch structure designs and three structures for electrical characterization tests are presented. It is followed by the modeling and simulation using the finite-element analysis (FEA) by simulation software COMSOL Multiphysics 5.2. Finally, the conclusion will be given.

### 4.2 Carbon nanotubes based micro switches structure design

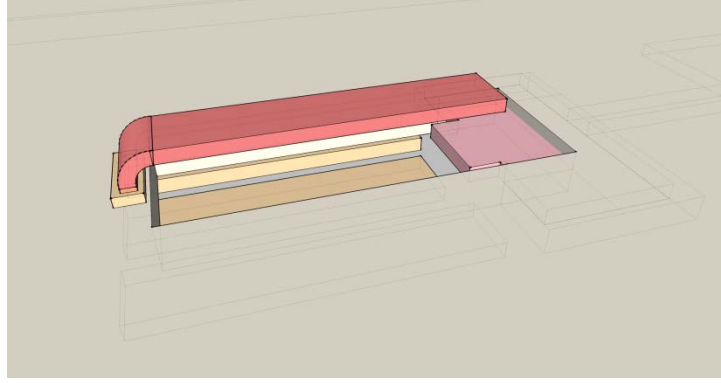
The whole switch design contains two drive modes, the electrostatic drive and an electromagnetic drive. There are four electrodes in total as figure 4.1 shows. The cantilever A are movement electrode which will be supplied with the voltage source. The electrode B is the ground terminal. The opposite polar charges will be concentrated on the upper and lower surfaces of the two plates which will generate a strong electrostatic force that attracts the upper cantilever electrode down as figure 4.2 shows below. Figure 4.3 shows the MEMS switches after  $\text{SiO}_2$  etching by vapour HF.



**Figure 4.1** MEMS switch conceptual illustration



**Figure 4.2** electrostatic force is produced because of opposite charges accumulated on upper and bottom Electrodes



**Figure 4.3** After silicon oxide etching by vapour HF.

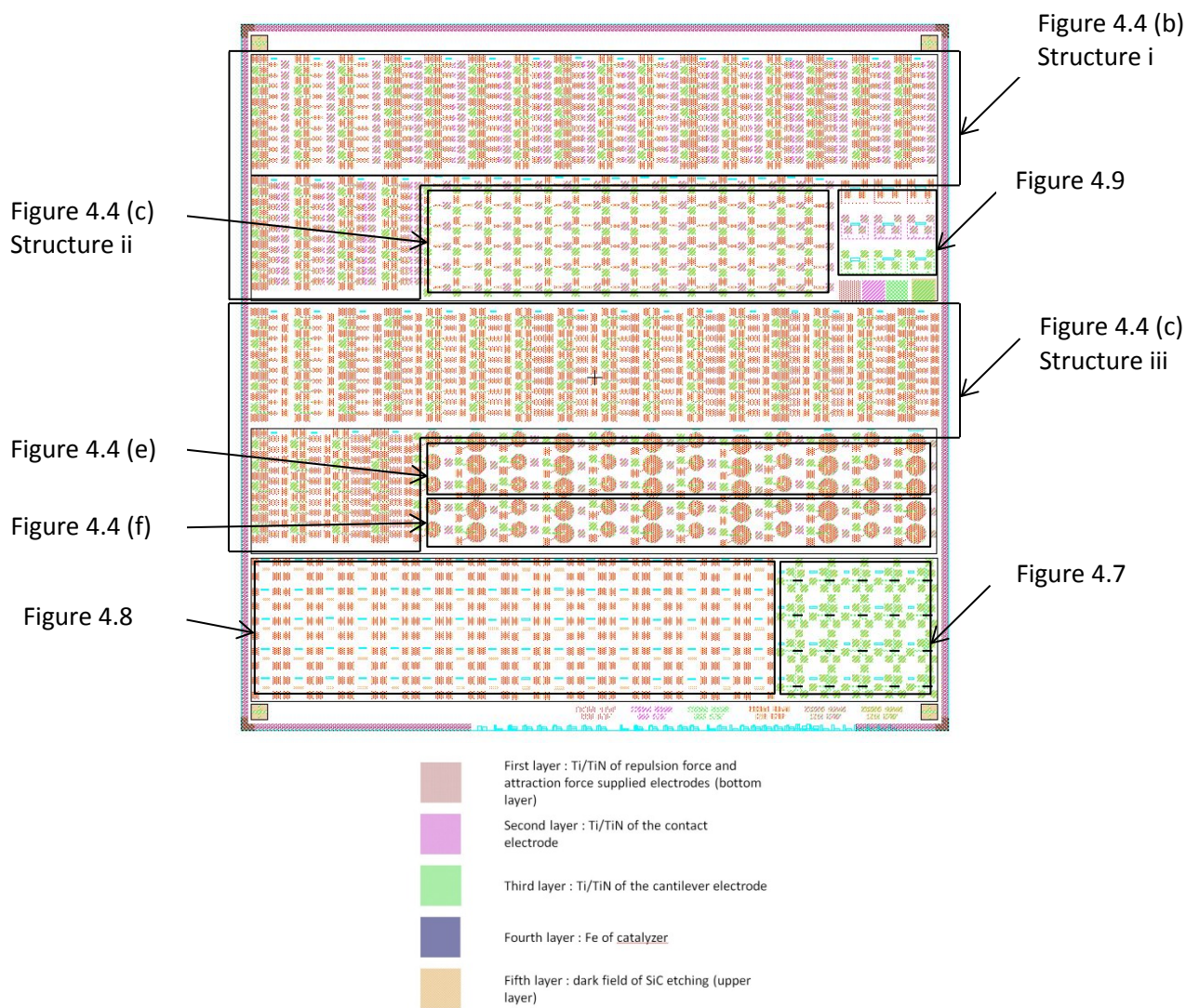
## **4.3 Layout design (L-Edit)**

### **4.3.1. MEMS switch structures**

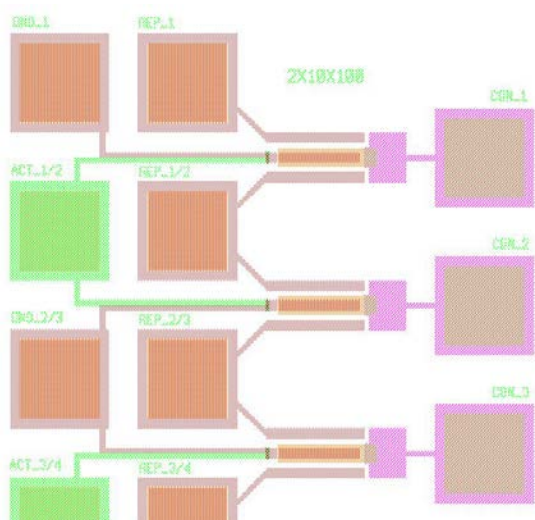
Figure 4.4 shows the five layers of masks as designed in L-Edit. There are five designs of potential switch structures shown as bellow.

First, a design in which the contact electrode is in different Z position with the bottom electrodes, containing both the attraction mechanism structures is shown. In the previous two designs, there need to be oxidation layers between each Ti/TiN metal layer for isolation. If the isolation layer is too thin, electrical breakdown can happen. However, if it is too thick, the tip displacement of the cantilever electrode will be too small to touch the contact electrodes due to the small electrostatic force at a large gap. In this case, we designed the third structure that the contact electrode is in the same plane with the bottom electrodes, containing the attraction structures.

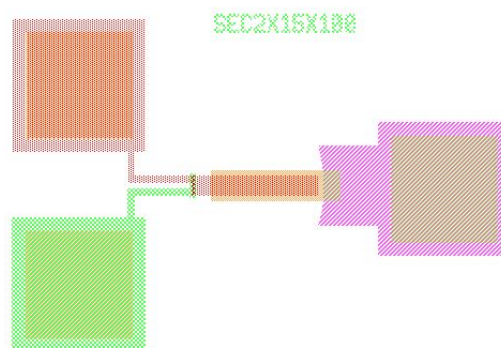
Because the horizontalization process is manual and hard to control, the CNT bundles are not for sure to fall to the exact desired direction, therefore we also designed the circular shape of the first metal layer and annular shaped contact electrode for which it does not matter which direction the CNT bundles will fall in. In order to avoid electric breakdown around the TiN metal lines, a cut in the circular structure is designed to partially exclude the first layer Ti/TiN metal under the third metal line. The catalyst layer will be evaporated on the third metal layer. CNT will only give a growth on the substrate where both metal layer and catalyst are patterned. Besides, after SiC coating, in order to release the cantilever, openings will be patterned around CNT bundles where SiC will be etched so that vapour HF can etch the silicon oxide layer under the cantilever. More specifications of each structure are presented in Appendix 2.



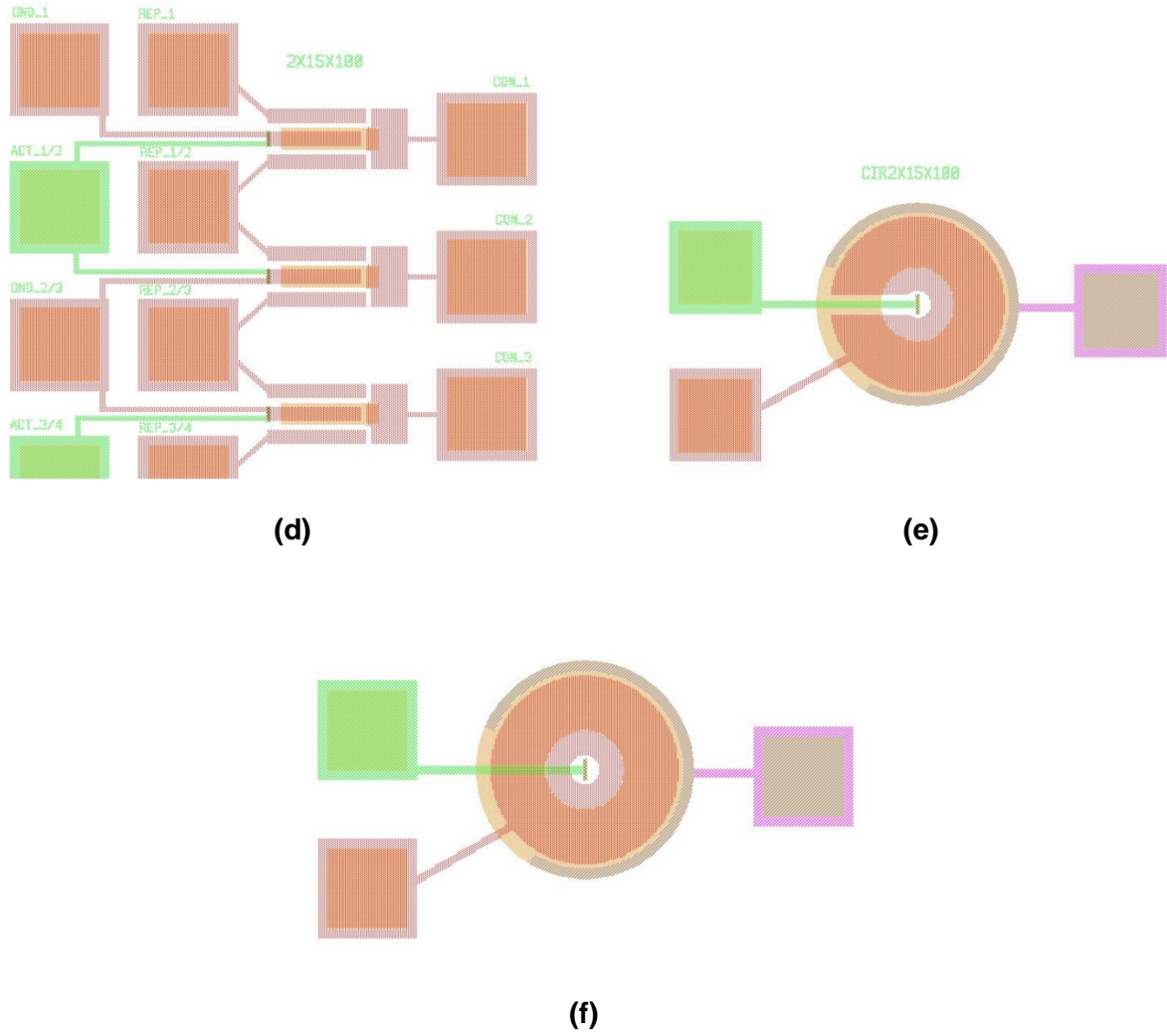
(a)



(b)



(c)



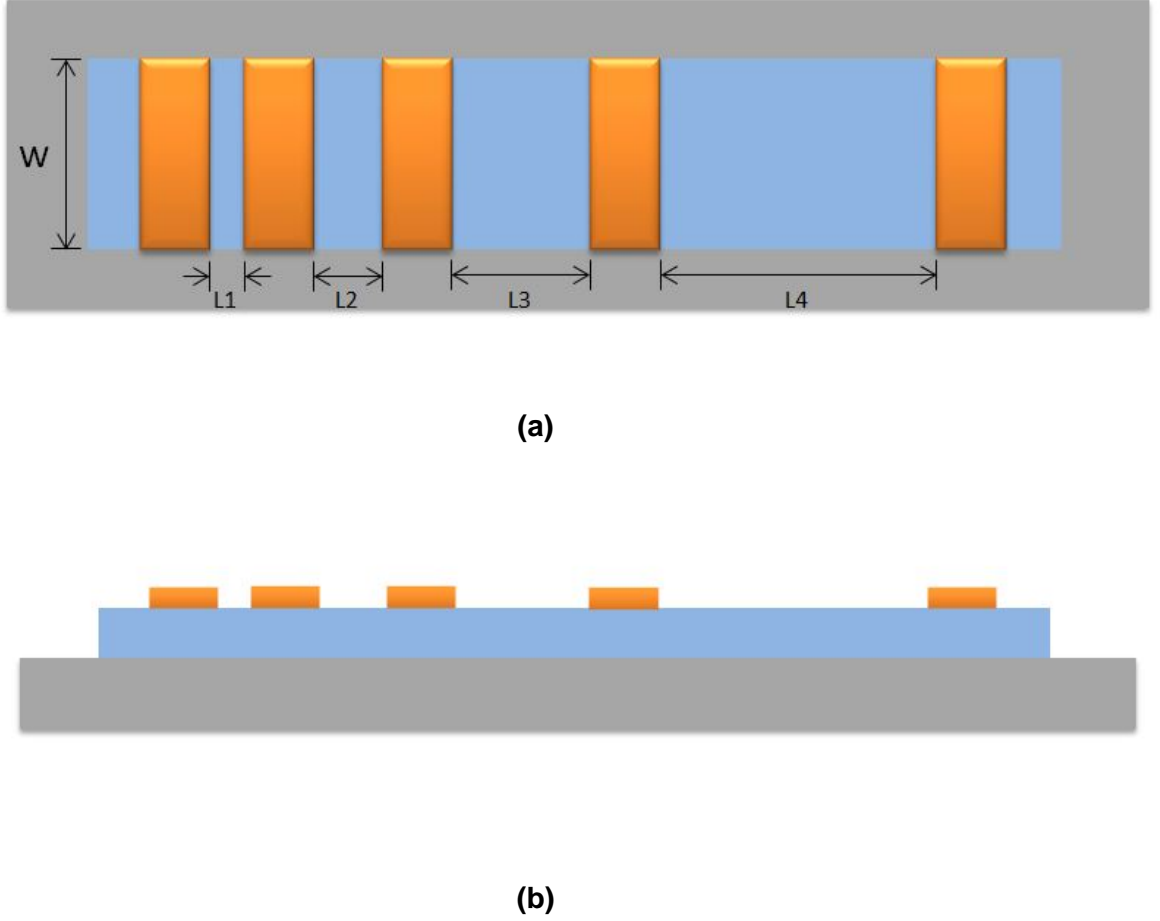
**Figure 4.4** Five-layer mask design. (a) Total view of MEMS switches mask design; (b) MEMS switches mask design of first structure design in which the contact electrode is in different Z position with the bottom electrodes, containing the attraction structures; (c) MEMS switches mask design of second structure design in which the contact electrode is in different Z position with the bottom electrodes, containing only the attraction mechanism structures; (d) MEMS switches mask design of third structure design in which the contact electrode is in the same plane with the bottom electrodes, containing the attraction structures; (e) MEMS switches mask design of fourth structure design in the shape of circular at first Ti/TiN metal layer, excluding partial first layer Ti/TiN metal under the third metal line to avoid breakthrough under high voltage supply; (f) MEMS switches mask design of fourth structure design in the shape of complete circular at first Ti/TiN metal layer.

#### 4.3.2. Transmission Line Model (TLM) for contact resistance measurement

In this work, the contact resistance is also a part of the design. It gives the influence especially when the cantilever electrode touches the bottom contact electrode. In this case, we need to know both the sheet resistance of the Titanium/Titanium Nitride (Ti / TiN) and the contact resistance between MWCNT bundles and metal pad independently. One typical



method for this measurement is called Transmission Line Model (TLM) of contact resistance [64, 65]. Figure 4.5 shows a typical topology of a TLM structure.



**Figure 4.5** TLM structure. (a) Top view of TLM structure; (b) Sectional view of TLM structure.

Normally, when we measure the I-V value, we will get the resistance value. In this model, the total resistance is composed of three factors: carbon nanotube resistance  $R_{CNT}$ , contact resistance  $R_C$ , and metal (Ti/TiN) resistance  $R_M$ .

$$R_T = R_{CNT} + 2R_C + 2R_M \quad (4.1)$$

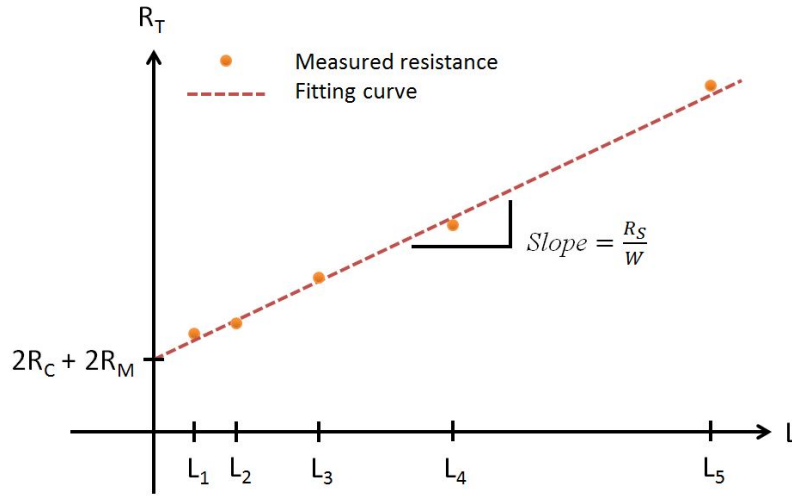
The resistance of carbon nanotube bundles can be modelled as

$$R_{CNT} = R_S \frac{L}{W} \quad (4.2)$$

So, the total resistance can be rewritten as

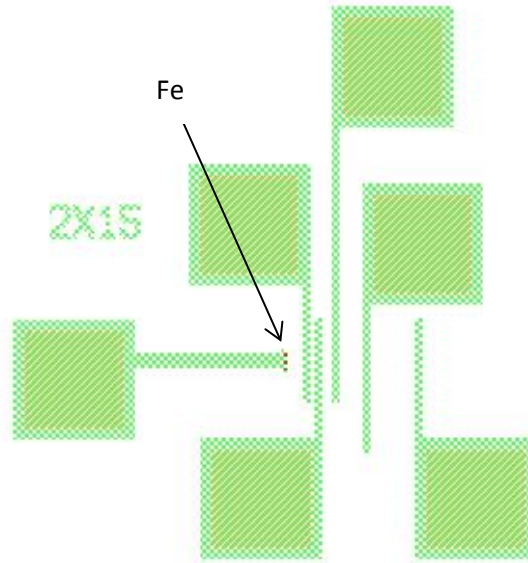
$$R_T = R_S \frac{L}{W} + 2R_C + 2R_M \quad (4.3)$$

When the resistors are measured in different lengths while  $R_C$ ,  $R_S$ ,  $W$  and  $R_M$  are not changed, we can make the line fitting of different length curve like the figure 4.6 shows.



**Figure 4.6** Line fitting of TLM I-V characteristics. The slope of the line shows the resistance per unit length of width and the intercept of y axis is as twice the contact resistance and contact pad metal resistance.

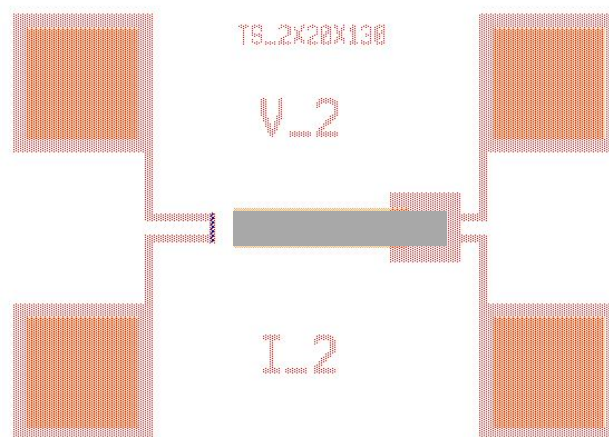
After fitting the curve, we can calculate the line slope which represents the sheet resistance per unit width of carbon nanotubes. At the meanwhile, the intercept of y-axis can be regarded as twice the contact resistance and the resistance of contact metal. The two different contact resistances here, first the TiN-CNT contact resistance at the point where the CNT are grown, and second the CNT-TiN contact resistance where the bundle touches the metal can be determined both by using different combinations of pads. Figure 4.7 shows the mask design of the TLM structure. The green structures are the metal layer (Ti/TiN:10nm/50nm) and the small black structure is iron patterning. Carbon nanotubes bundles will grow on the iron pattern and follow its shape in the x-y plane. After horizontalization, CNT bundles will fall in the right direction.



**Figure 4.7** mask design of the TLM structure.

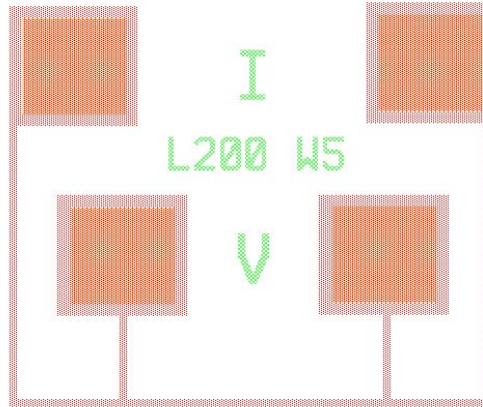
#### 4.3.3. Four-point-probe model I for resistance measurement

Except for TLM measurement structure, we also supply the four-point-probe measurement structure as the figure shows. Probes 1 and 2 are supplied with potential difference, probes 3 and 4 are supplied with current detection. The slope of the I-V line will present the resistance of carbon nanotube bundles and the contact resistance between carbon nanotube bundles and the contact Ti/TiN pad. The measurement results will be presented in chapter 5.



**Figure 4.8** First four-point-probe structure for CNT resistance measurement.





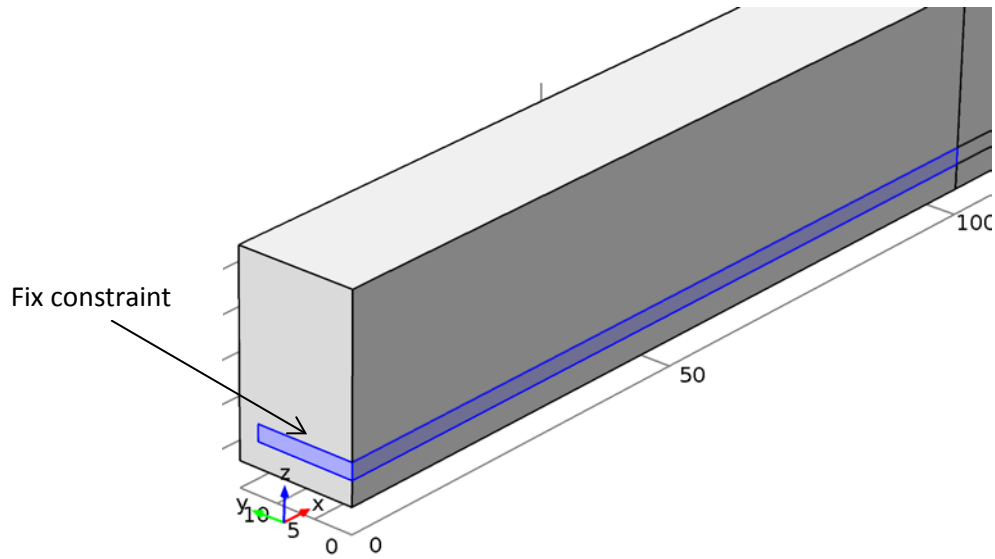
**Figure 4.9** Second four-point-probe structure for metal resistance measurement.

## 4.4 Simulation in COMSOL Multiphysics

We did the simulation of the complete structure as figure 4.4 (b) showed in Finite Element Analysis (FEA) simulation tool COMSOL Multiphysics 5.2. Figure 4.10 shows the scenography geometry of the switch design which contains the attraction mechanism structures. The fixed constraint is shown in the figure as well. We only show the simulation results of one size here as shown in Table 4.1. The voltage sweep is from 10 V – 80 V. As figure 4.11 shows, we set the device ambient in the air which possesses the relative permittivity of 1. The three bottom electrodes are defined as Ti/TiN while the upper electrode is defined as MWCNT bundles. Insufficient materials properties demanded by the software are shown in Table 4.2. Finally, the deformation figure, electrical potential planes, cantilever displacement – supplied voltage, tip displacement – voltage are shown from figure 4.11 to figure 4.14. The relationship between tip displacement and CNT bundles' width, depth, and height are shown in figure 4.15 to figure 4.18. It is detected that the tip displacement is positive to cantilever's width, negative to the height and distance between electrodes, and not obvious influence from the depth.

From the previous test, the CNT bundles will be able to get flatten horizontally only with  $3\ \mu\text{m} \times 15\ \mu\text{m}$ ,  $3\ \mu\text{m} \times 20\ \mu\text{m}$ ,  $3\ \mu\text{m} \times 25\ \mu\text{m}$  with the length from  $100\ \mu\text{m}$  to  $138\ \mu\text{m}$ . When aspect ratio is smaller than 33, it is more and more hard to get flatten aligned. Bundles at the dimension of  $3\ \mu\text{m} \times 15\ \mu\text{m}$ ,  $3\ \mu\text{m} \times 20\ \mu\text{m}$  are too slim to be aligned well. They are easy to get an angle with alignment direction which is not desired. In this case, we designed the device with CNT bundles in the length of  $100\ \mu\text{m}$ . In the COMSOL Multiphysics, bundles' dimension are called width (dimension in X direction), depth (dimension in Y direction), and height (dimension in Z direction). In this chapter, we will follow the same name definition as the software defines.

#### 4.4.1. Geometry



**Figure 4.10** Scenography geometry of MEMS switch with symmetry.

**Table 4.1:** Parameters of geometry.

Name	Value	Description
The distance between the cantilever and the bottom electrode	3	$\mu\text{m}$
Cantilever width	100	$\mu\text{m}$
Cantilever depth	12.5	$\mu\text{m}$
Cantilever height	4	$\mu\text{m}$
Initial V0	2 V	Bias on the cantilever

#### 4.4.2. Material properties

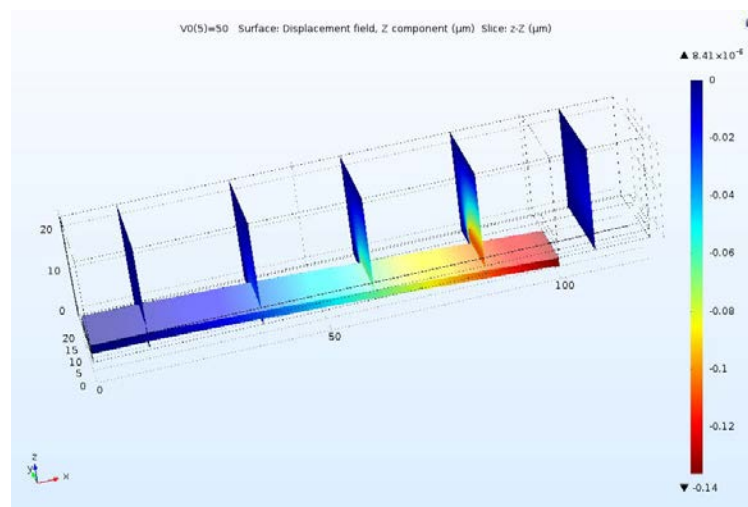
The passion ratio is from 0.35 to 0.37 for SiC and 0.32 to 0.36 of MWCNT. We chose 0.35 here.

**Table 4.2:** Mechanical, electrical, and thermal properties of each domain.

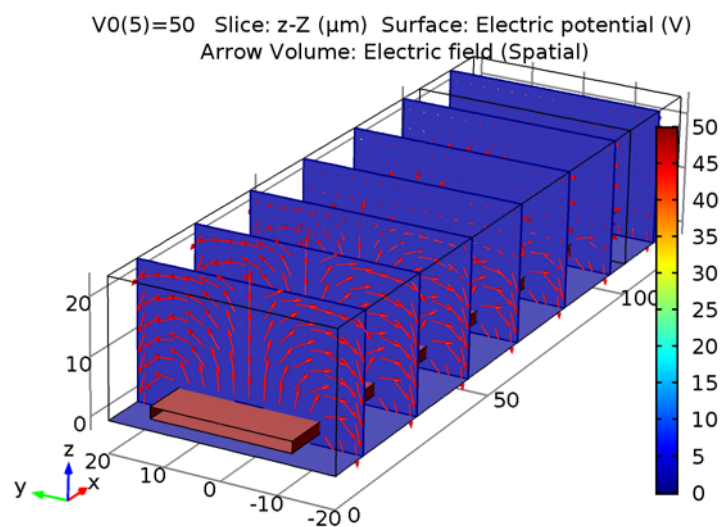
Domain	Name	Value	Unit
--------	------	-------	------

Domain	Name	Value	Unit
Air	Relative permittivity	1	1
Cantilever CNT with SiC coating	Density	3200	kg/m <sup>3</sup>
	Young's modulus	400	GPa
	Poisson's ratio	0.35	1

#### 4.4.3. Simulation results

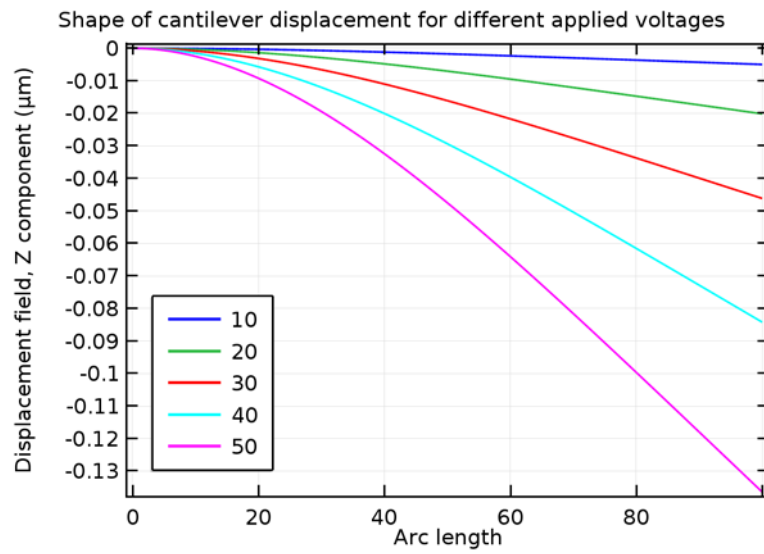


**Figure 4.11** Displacements at multiple y-z plane.

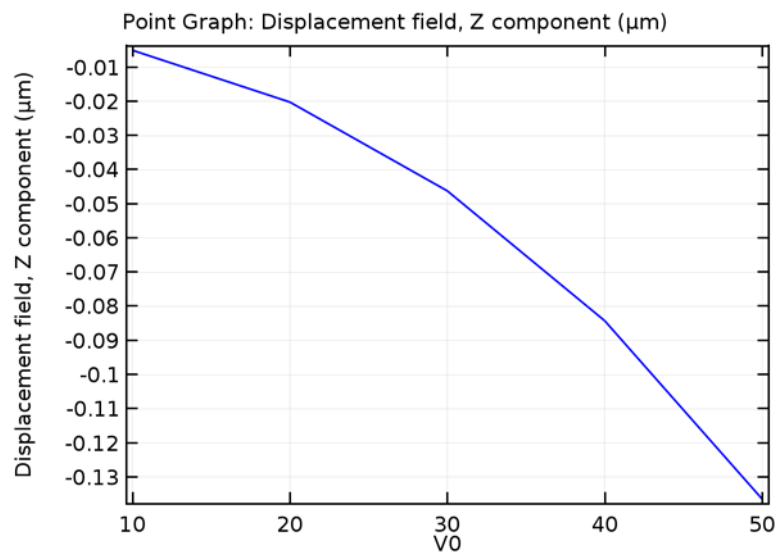


**Figure 4.12** Electric potential (V) of cantilever and electric field in different x-y surface.

#### 4.4.4. Displacement and supplied voltage

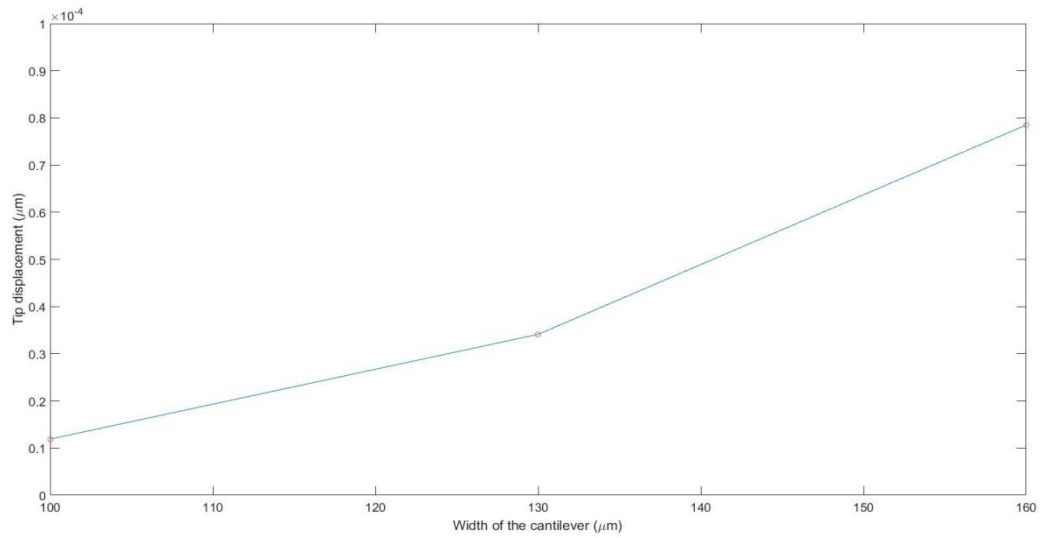


**Figure 4.13** Cantilever displacement and supplied voltage



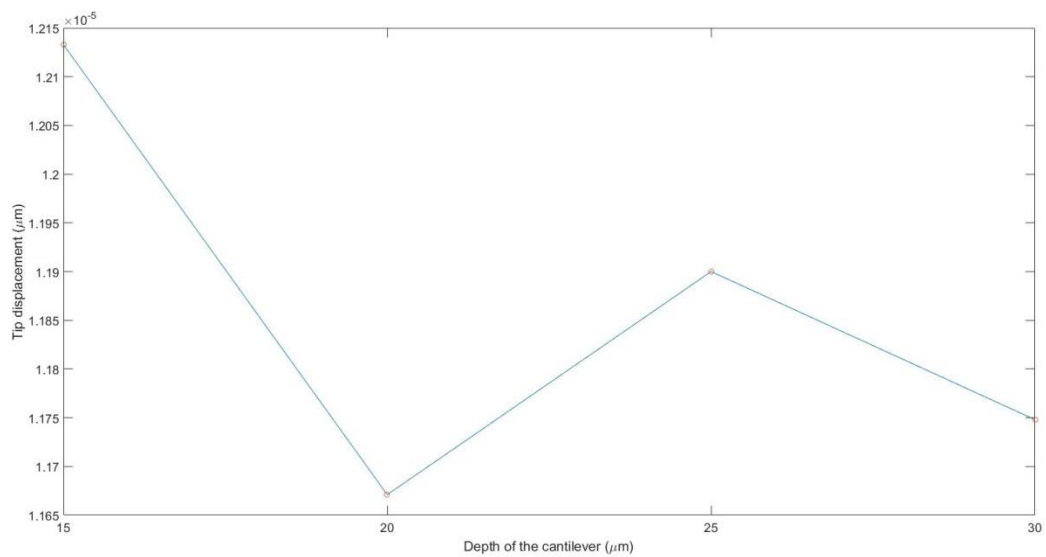
**Figure 4.14** Tip displacement and supplied voltage of 50 V.

#### 4.4.5. Tip displacement and width



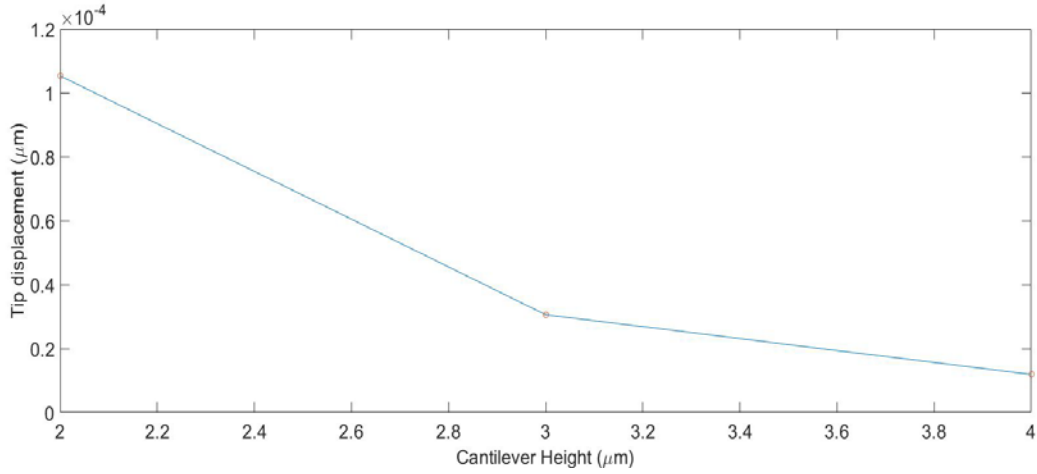
**Figure 4.15** Tip displacement and the width of cantilever

#### 4.4.6. Tip displacement and depth



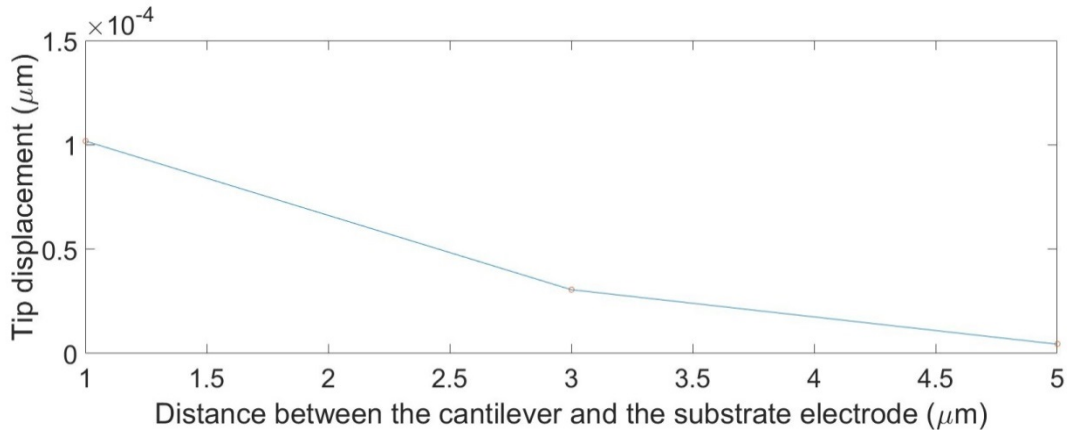
**Figure 4.16** Tip displacement and the depth of cantilever

#### 4.4.7. Tip displacement and height



**Figure 4.17** Tip displacement and the height of cantilever.

#### 4.4.8. Tip displacement and gap



**Figure 4.18** Tip displacement and the distance between the cantilever and the substrate electrode.

### 4.5 Conclusions

This chapter serves as elaboration of designing conception for devices. It is explained from two aspects. First, the mask design is shown with four structure designs out of different considerations. Also, some measurement structures are shown for metal sheet resistance measurement, contact resistance measurements, and CNT bundle resistance. Next, we show the simulation of electrostatic drive.

For a  $width \times depth \times height$  is  $100 \mu m \times 25 \mu m \times 4 \mu m$  CNT bundles, with 2 V pull-in voltage, 3  $\mu m$  gap between the cantilever and the substrate electrode, the tip displacement can reach  $\mu m$  which is approximately can get contact.

From simulations, the displacement is positively related to the supplied voltage and width but negative related to the height of the cantilever and the distance between the cantilever and the substrate electrode. There is no obvious relationship can be seen from the cantilever depth and the displacement which seems not much influence to the displacement.

## **5. Fabrication and results**

### **5.1 Introduction**

This chapter mainly introduces process procedures, fabrication results, and discussions of these results. First, the process illustration will be given. Then, microscopy inspection of each step after carbon nanotubes' growth will be shown. Beside this, Raman inspections and electrical characterizations are presented. This is followed by the discussions and potential explanation of some observed phenomena. Finally, conclusions will be given.

### **5.2 Process**

The whole process begins with a p-type silicon substrate on which a 200 nm thermal oxide layer is added for isolation. After alignment marks are patterned, the first metal layer for the bottom electrodes which is 10nm Titanium (Ti) and 50 nm Titanium Nitride (TiN) is deposited and patterned. Then a thick layer of oxide will be deposited using PECVD. This layer is aimed at isolating the contact metal layer and the bottom electrode layer to make sure the cantilever will contact the contact pad without touching the bottom electrode. Then the second layer (contact pad layer, 10 nm Ti and 50 nm TiN) is deposited and patterned. The third oxide layer is deposited by PECVD after this to make the carbon nanotubes cantilever higher and isolated from the bottom layers. After the third metal layer (Ti/TiN) been deposited and patterned, iron (Fe) will be patterned by evaporation and lift-off. CNT will be deposited by LPCVD in BM after photoresist cleaning by NMP to give a CNT length at around 100  $\mu\text{m}$ . The CNT bundles might be vertically aligned or left-side aligned in our design. The horizontalization is supplied to implement densification and horizontalization of the bundles in the direction of the contact pad. Silicon carbide will be deposited by LPCVD in the furnace at a thickness of several nanometers (1 – 35 nm) to fill the CNT bundles. After this, the dark-field mask and positive photoresist are used to pattern the SiC layer which is followed by SiC dry etching. Acetone and oxygen plasma are used to clean the hardened photoresist remaining after SiC etching. The vapour HF etching of  $\text{SiO}_2$  is supplied after photoresist cleaning in order to release the cantilevers.

### **5.3 Results and discussions**

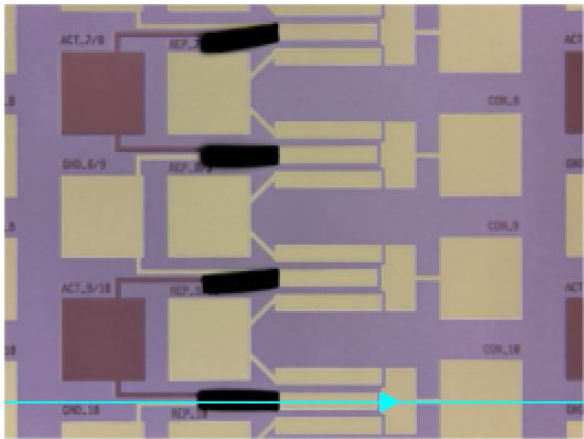
#### **5.3.1. Microscopy inspection by Keyence**

After 2 hours deposition at 605°C in BM, bundles have been shown to be self-aligned as Figure 5.1 (a) shows. Figure 5.1 (b) presents the bundles after horizontalization in acetone for 5 mins. The 3D image as obtained by the laser profilometer in Figure 5.1 (c) show the profile of the bundles, and the measurement of the length and uniformity is shown in figure

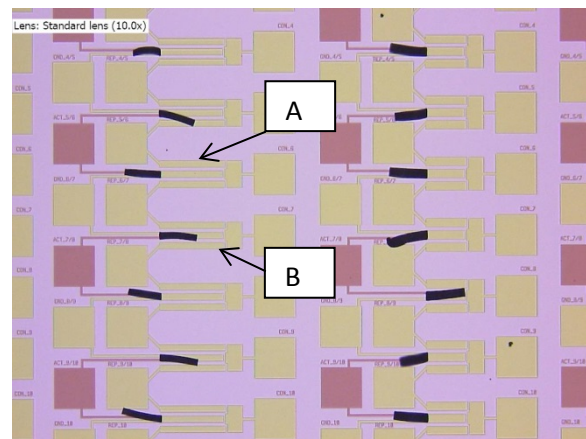


5.1 (d). From the measurement, the distance between the highest point of CNT bundles and the first metal layer in the Z direction is  $27.927 \pm 5.765 \mu\text{m}$ . That is because of the buckled shape at the root part of CNT bundles which is shown in the next section 5.3.2 as figure 5.2. The roughness measurement of figure 5.1 (d) is obtained from the profile shown by the blue arrow in figure 5.1 (a). Due to the buckled root, the bundle length will be 15 to 25  $\mu\text{m}$  shorter than the original length after horizontalization. This will make it more difficult to fabricate 100  $\mu\text{m}$  CNT bundles.

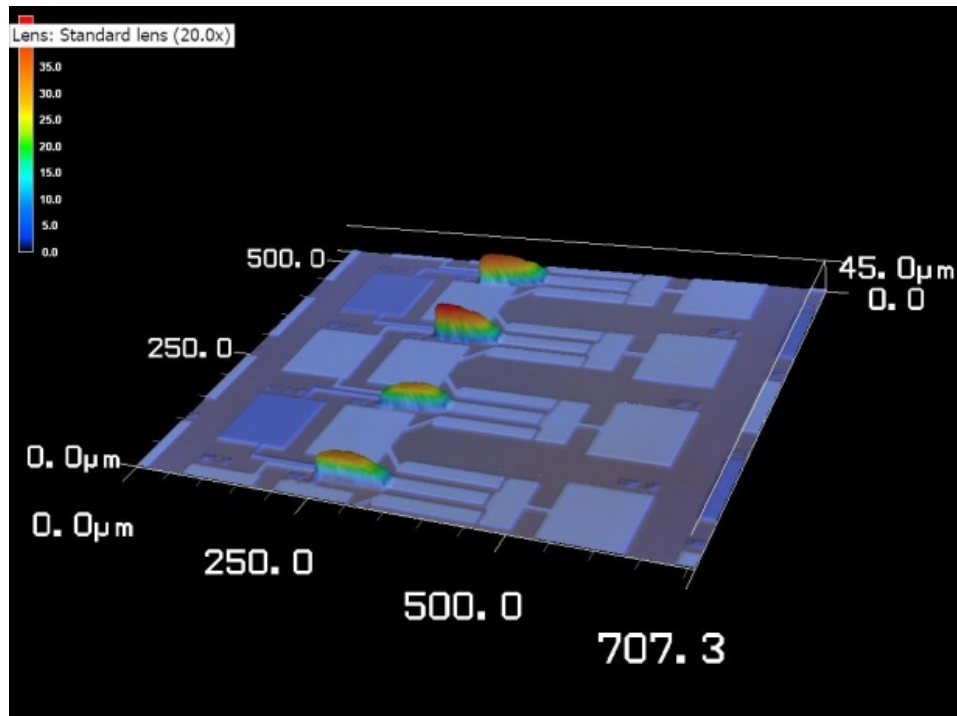
For the remaining discussion, we define the bundles' direction of A in figure 5.1 (b) as left-aligned or misaligned and the bundle direction of B in figure 5.1 (b) as right aligned or correctly aligned. It needs to be mentioned that at this temperature, there are around 6% bundles aligned to the right. In chapter 6 the cause of this behavior, and ways to improve the yield will be discussed.



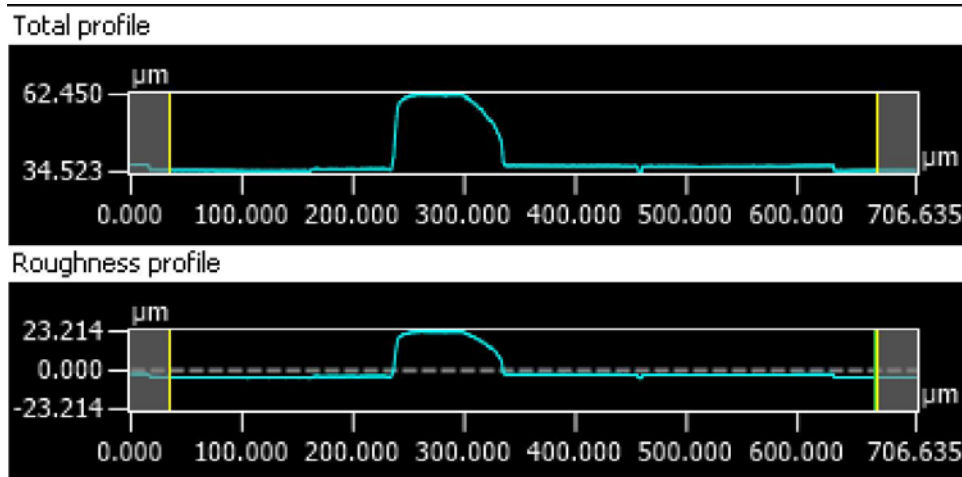
(a)



(b)



(c)

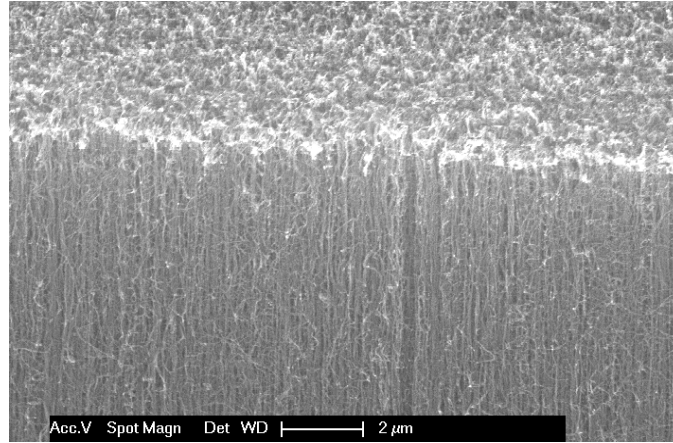


(d)

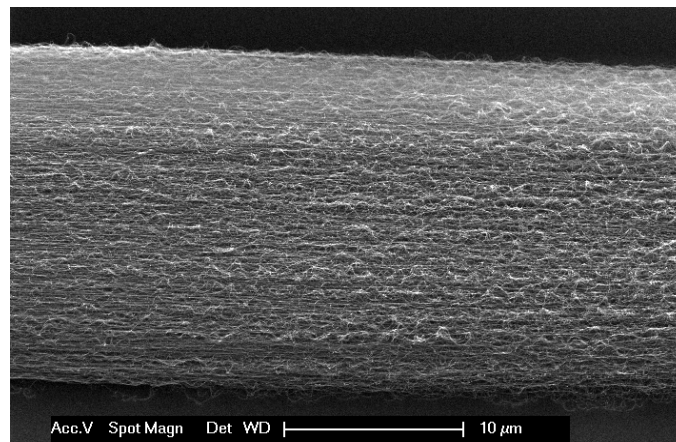
**Figure 5.1** Keyence 3D Microscopy inspection of samples with deposition recipe 605°C for 2 hours. (a) Laser and optical inspection. (b) ) Microscopy inspection after horizontalization in acetone for 5 mins. (c) 3D imaging of CNT bundles. (d) Profiles of CNT bundles in the direction of the blue arrow shown in (a).

### 5.3.2. Microscopy inspection by SEM

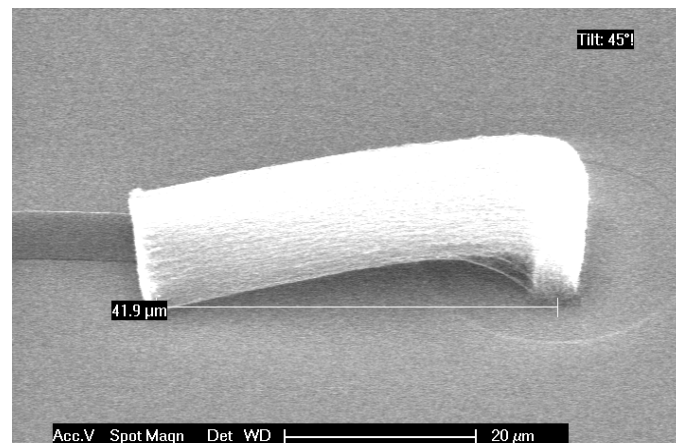
Figure 5.2 shows some Scanning Electron Microscope (SEM) images of the CNT bundles. Figure 5.2 (a) and (b) show that the single nanotubes are mostly vertically aligned. More images can be seen in Appendix 5.



(a)



(b)

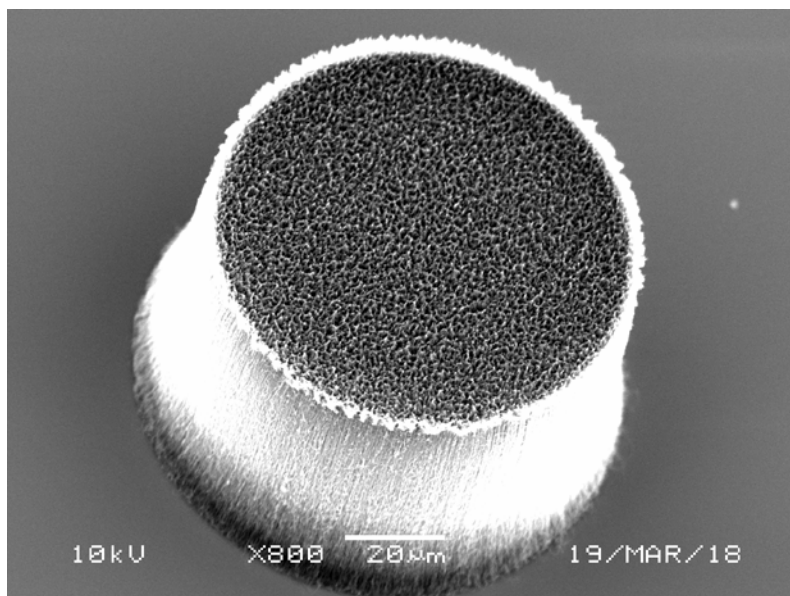


(c)

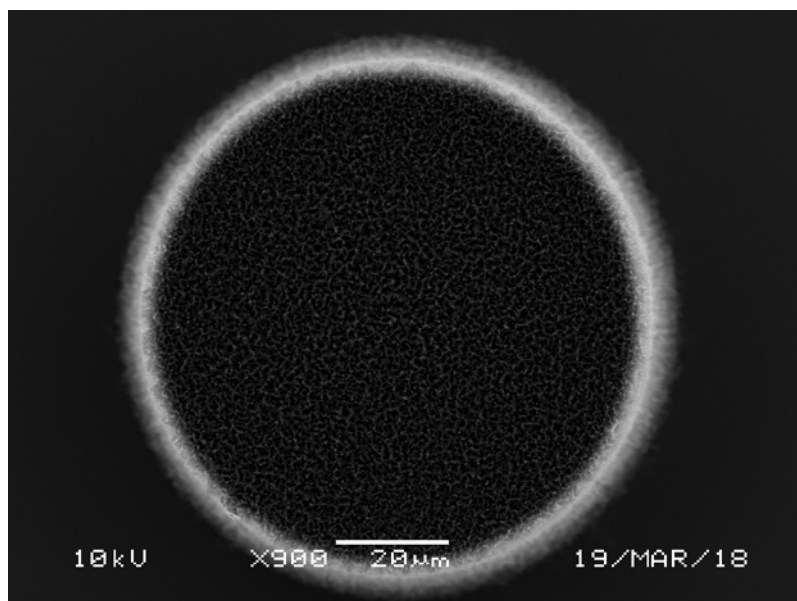
**Figure 5.3** SEM images of cylinder MWCNT bundles. The diameter is 100  $\mu\text{m}$  and height in  $50 \pm 5 \mu\text{m}$ . (a) Vertically aligned Carbon Nanotubes. (b) Horizontally aligned Carbon Nanotubes. (c) Horizontally aligned Carbon Nanotubes bundles with a short length.

Figure 5.3 shows the large cylinder CNT bundles after densification in acetone for 5 mins. From the tilted view, it is clear to see the top part of the bundles appear to shrink because of

the densification. This is not easy to be observed in the High Aspect Ratio (HAR) bundles but there is also assumed that the densification shrinks the dimensions of the HAR bundle slightly.



(a)

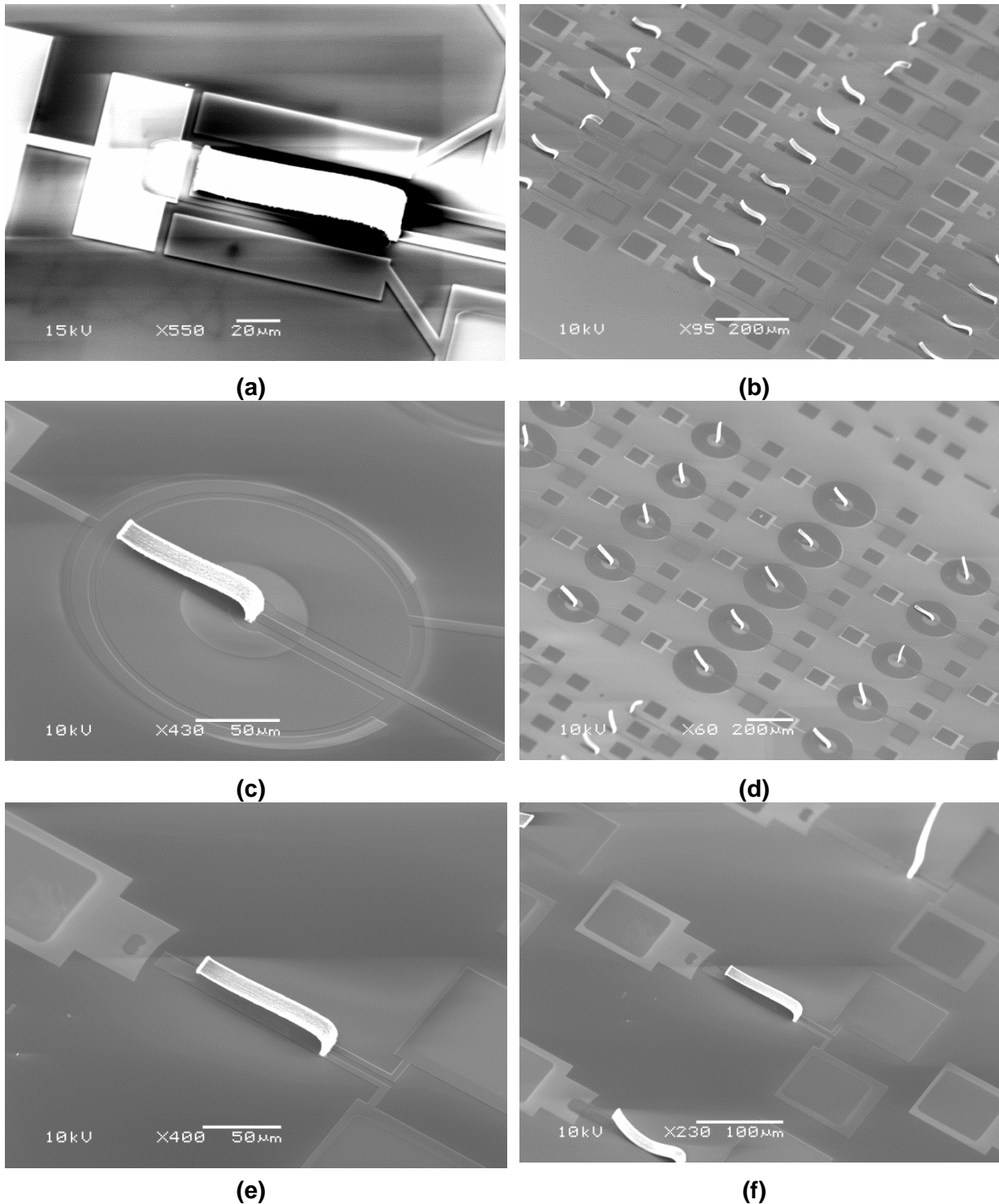


(b)

**Figure 5.3** SEM images of cylinder MWCNT bundles. The diameter is 100  $\mu\text{m}$  and height in  $50 \pm 5 \mu\text{m}$ . (a) Tilted view of densified bundles in acetone for 5 mins. (b) Top view of densified bundles in acetone for 5 mins.

Figure 5.4 shows devices after vapour HF etching for two cycles (each cycle takes 10 mins) with etch rate 1559  $\text{\AA}/\text{min}$ . The bundle geometry appears unaffected by the HF etching. On

top of the contact pads, openings etched in the SiC are visible (fig. 5.4 b). As can be seen in fig. 5.4 a cavity underneath the bundle is formed due to HF etching. Unfortunately, from the images it is not clear if the vapour HF etch has been sufficiently long to fully etch the oxide.



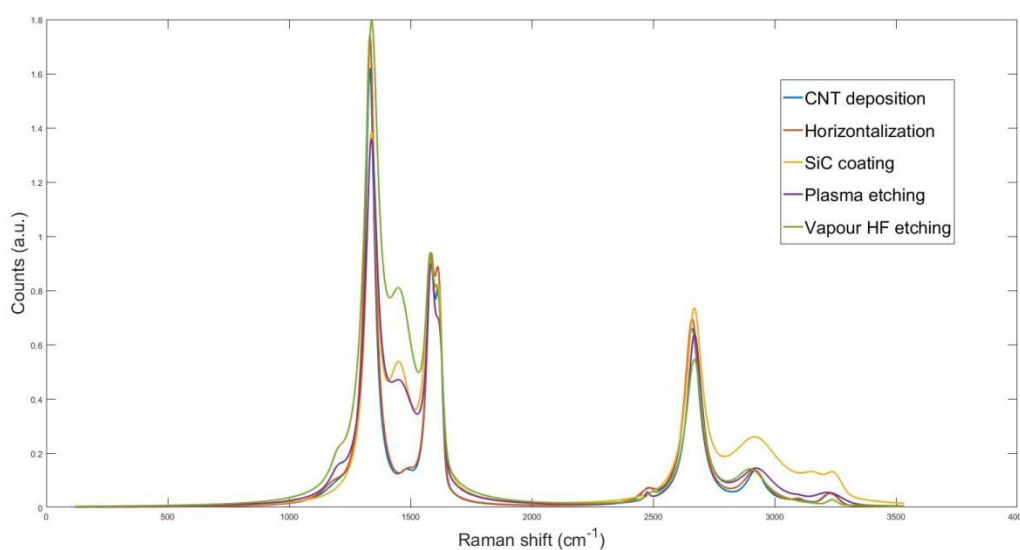
**Figure 5.4** SEM images of CNT bundles after vapour HF etching. (a) A single device in three metal layer design. (b) A group of devices in three metal layer design. (c) A single device in

circular structure design. (d) A group of devices in circular structure design. (e) A single device in section structure design. (f) A group of devices in section structure design.

### 5.3.3. Raman microscopy

Raman microscopy is one of the effective and convenient measurements for characterizing CNT bundles in measuring its quality and radius distribution. The main analysis principle is based on the frequency shift of the light when it passes through the material which can indicate some information of the molecular structure, molecular vibration, molecular rotation and so on. The peak at around  $1580\text{ cm}^{-1}$  is called G-band which shows the CNT's ordering degree. And the peak at around  $1350\text{ cm}^{-1}$  is called D-band which shows its defect degree. The second-order bands D' and G' (2D) occurs at around  $1600\text{ cm}^{-1}$  and  $2600\text{ cm}^{-1}$  respectively as figure shows. The absolute independent intensity of  $I_D$  or  $I_G$  cannot indicate defects of MWCNT, but the intensity ratio of  $I_D/I_G$  can be used: the higher the more disorder there is present. Lorentzian curve and Gaussian curves are used for fitting the measurement results and all data are normalized to G peak value as previous work [66]. The Radial Breathing Mode (RBM) is normally composed of multiple small value peaks under the range of  $300\text{ cm}^{-1}$  and corresponds to its diameter distribution independently but we did not detect it here, which indicate there are no SWCNT.

We measured the Raman microscopy after CNT deposition at  $605^\circ\text{C}$  for 2 hours, horizontalization by acetone disposing for 5 mins, 8.9 nm thickness SiC deposition, oxygen plasma cleaning, and vapour HF etching separately. The spectra are shown in figure 5.5. A comparison of the fitted peak data can be found in Table 5.1.



**Figure 5.5** Raman spectra of MWCNT after different process step.

**Table 5.1:** Raman data obtained from MWCNT after different process steps.

Samples Bottom temperature_top heat_wait time				FWHM ( $cm^{-1}$ )			
	$I_{D/G}$	$I_{D'/G}$	$I_{G'/G}$	D	G	D'	G'
CNT deposition	1.79	0.60	0.73	48	41	29	76
Horizontalization	1.97	0.68	0.78	50	42	33	76
SiC coating	1.57	0.48	0.84	55	58	28	80
O <sub>2</sub> plasma etching	1.62	0.49	0.81	60	43	33	73
Vapour HF etching	2.27	0.62	0.74	69	46	36	83

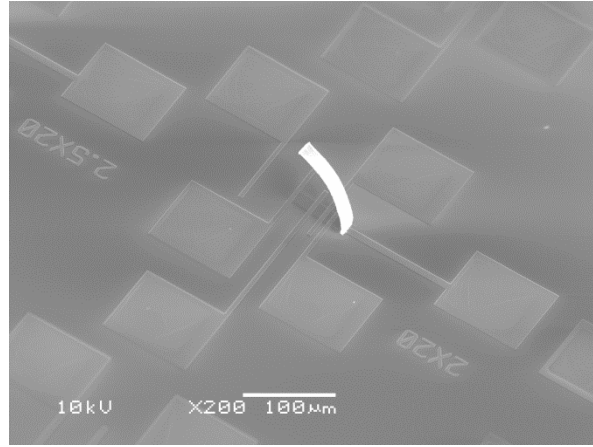
The increase of FWHM of D band,  $I_{D/G}$  and  $I_{D'/G}$  after horizontalization indicate more defects in CNT bundles. After coating, the lower FWHM of D band,  $I_{D/G}$  and  $I_{D'/G}$  indicate the CNT bundles have better quality, possibly due to the high temperature anneal in the LPCVD furnace. However, the obvious larger FWHM of D band, G band G' band indicates a broader defect distribution. This can also be because of the SiC influencing the Raman scattering and frequency shift of CNTs.. Plasma etching in oxygen gave a little bit of negative influence on SiC coated CNTs, which show the coatings are effective in protecting the CNT. Nevertheless, the vapour HF etching indeed has a large influence in CNT crystalline and significantly decreases the quality. The exact cause of this is currently unknown, as HF is not known to be an etchant of CNT.

#### 5.3.4. Electrical measurements

##### 5.3.4.1. TLM measurement

As most bundles are misaligned and the buckled shape at the roof part as figure 5.6 shows, there is no contact with the substrate metal layer for measuring. Therefore, unfortunately we were unable to measure the resistance of the CNT bundles using the TLM structure.





**Figure 5.6** No contacts between the CNT bundle and the substrate measurement contact pads for the TLM structure.

#### 5.3.4.2. The sheet resistance of Ti/TiN

The resistance of 10nm/50nm Ti/TiN metal layer is measured by Electrical Linewidth Measurement (ELM) structure mentioned in chapter 4.

As we observed that there is conduction everywhere on the surface, even between unconnected metal pads, after long-time CNT deposition samples, but good isolation in samples before deposition, we assumed there is thin carbon film also deposited on the surface which will influence the conductivity measurements of the metal layer. Additional measurements of the metal layer resistance with a deposition time of 1h and 2h independently are taken to show the influence of deposition time on the metal layers. See the results in Table 5.2. More details are presented in appendix 6.

For sheet resistance calculation we have the formula:

$$R = \frac{l}{w} \cdot R_{\square} \quad (5.1)$$

$R$  is the resistance of Ti/TiN,  $l$  is the length which is 200  $\mu\text{m}$  for all the samples,  $w$  is the width which is 2  $\mu\text{m}$ , 5  $\mu\text{m}$ , and 10  $\mu\text{m}$  respectively. The calculated sheet resistance is shown in Table 5.3.

**Table 5.2:** Resistance measurement of the Ti/TiN layer

Deposition time (h)	Average resistance of width in 2 $\mu\text{m}$ , length in 200 $\mu\text{m}$ ( $\Omega$ )	Average resistance of width in 5 $\mu\text{m}$ , length in 200 $\mu\text{m}$ ( $\Omega$ )	Average resistance of width in 10 $\mu\text{m}$ , length in 200 $\mu\text{m}$ ( $\Omega$ )



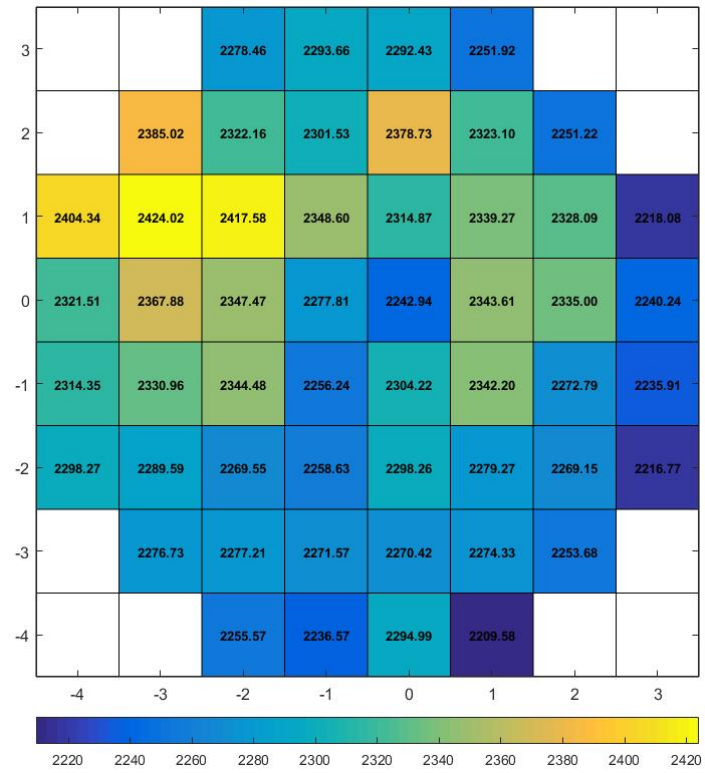
1	$2969 \pm 51.1$	$1316 \pm 70.4$	$749 \pm 93.1$
2	$2299 \pm 50.8$	$965 \pm 29.2$	$495 \pm 21.0$

**Table 5.3:** Sheet resistance of the Ti/TiN layer

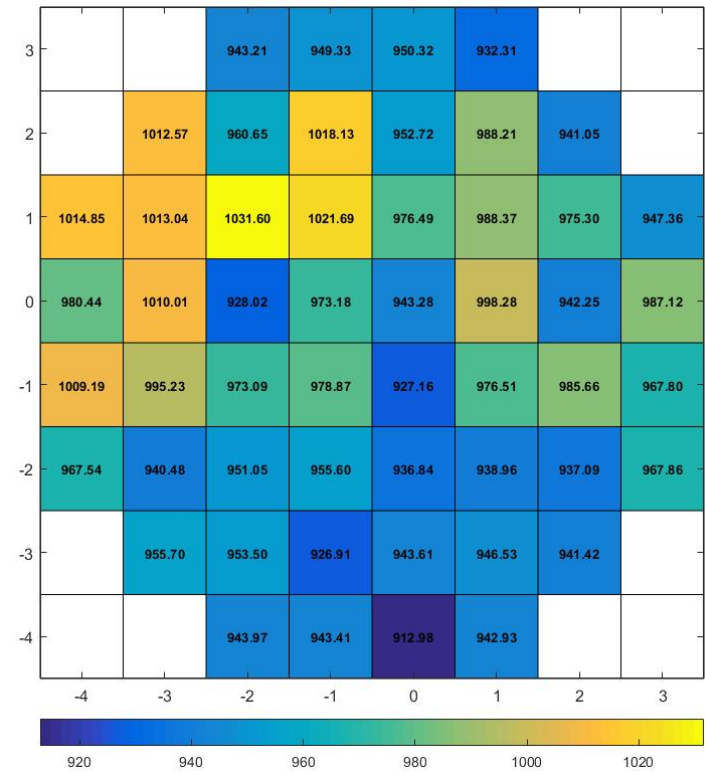
Deposition time (h)	Average sheet resistance of width in $2\mu\text{m}$ , length in $200\mu\text{m}$ ( $\Omega/\square$ )	Average sheet resistance of width in $5\mu\text{m}$ , length in $200\mu\text{m}$ ( $\Omega/\square$ )	Average sheet resistance of width in $10\mu\text{m}$ , length in $200\mu\text{m}$ ( $\Omega/\square$ )	Mean sheet resistance of $10\text{nm}/50\text{nm}$ Ti/TiN ( $\Omega/\square$ )
1	$30 \pm 0.5$	$33 \pm 1.8$	$37 \pm 4.7$	$33 \pm 2.3$
2	$23 \pm 0.5$	$24 \pm 0.7$	$25 \pm 1.1$	$24 \pm 0.8$

The narrow width structure shows to have a little bit larger sheet resistance which can be related to the process accuracy. The resolution of the wafer stepper is  $1\mu\text{m}$ , very close to  $2\mu\text{m}$ , which will give larger influence when the width is smaller. Besides this, the longer deposition time at 2 hours will lower the sheet resistance of Ti/TiN. This can be generated by the conductive thin film carbons produced in the longer deposition which covers the surface. Longer time will get a thicker layer which might result in increasing the conductivity therefore lowering the resistivity.

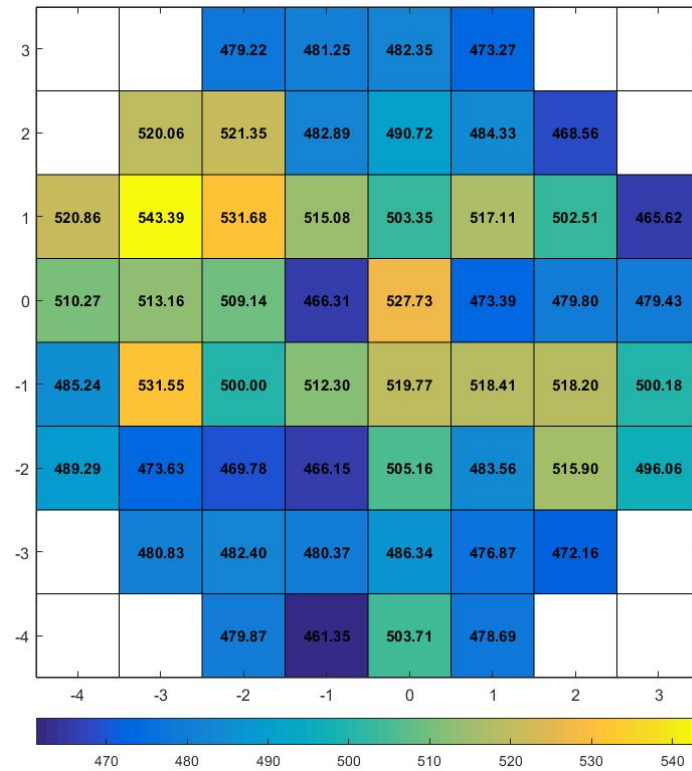
With two hours deposition at  $605^\circ\text{C}$ , the resistance distribution over the wafer is shown in figure 5.7. The left-up corner shows to have a little bit higher resistance. If this is caused by thin film carbon layers, than that means this area has a larger resistance of carbon layers which means a thinner thickness. From the later finding in chapter 6, the left-up corner has a lower temperature distribution. Therefore, the lower temperature will generate thinner carbon layer during deposition. But this can also be caused by the Ti/TiN thickness no uniform which needs to be explored with resistance of Ti/TiN layer without CNT deposition.



(a)



(b)



(c)

**Figure 5.7** ELM structure for resistance measurement of different width 10nm/50nm thickness Ti/TiN layer under CNT growth recipe at 605°C for 2 hours. (a) Resistance measurements of 2  $\mu\text{m}$  width and 200  $\mu\text{m}$  length Ti/TiN line; (b) Resistance measurements of 5  $\mu\text{m}$  width and 200  $\mu\text{m}$  length Ti/TiN line; (c) Resistance measurements of 10  $\mu\text{m}$  width and 200  $\mu\text{m}$  length Ti/TiN line.

#### 5.3.4.3.

The resistance of CNT bundles connection with contact pads at 605°C for 2 hours and horizontalization in acetone for 10 mins is shown as Table 5.4. This measurement is done with the structure shown in figure 4.8 of chapter 4. As the aspect ratio is larger than 10, we assume the depth and height will not generate much influence on the resistance once the length is longer than 100  $\mu\text{m}$ .

**Table 5.4:** Resistance of CNT bundles with a thin film of a carbon layer

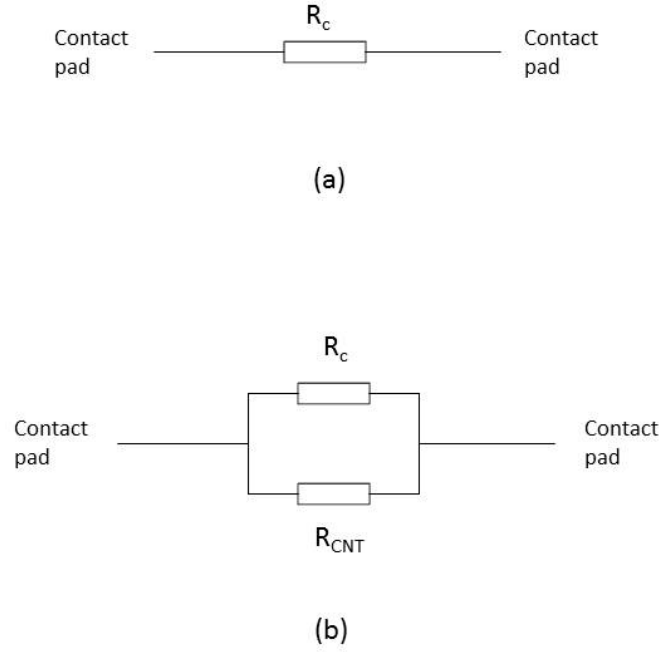
Length of bundles [ $\mu\text{m}$ ]	Resistance of CNT bundle with the thin film of carbon layer [k $\Omega$ ]							
100	1.55	1.60	2.16	1.54	1.92	1.68	1.52	1.25

	1.74	1.37	1.78	1.57	1.30	1.47	1.77	1.64
	1.62	1.39	1.20	2.01	2.01	2.10	1.31	1.38
	1.33	1.94	1.38	1.50	1.51	1.89	1.89	1.92
130	2.06	2.90						

As the thin carbon layer on the entire wafer is also conductive, it will influence the resistance results of CNT bundles. Therefore, the resistance between contact pads without CNT connection needs to be identified. The results are presented in Table 5.5. The thin film of carbons can be modelled as a parallel resistor with CNT bundles as figure 5.8 shows. Therefore, the average resistance of CNT bundles can be calculated, which are shown in Table 5.5.

**Table 5.5:** The average resistance of CNT bundles.

Length of bundles [ $\mu\text{m}$ ]	Average Resistance of CNT bundles with the thin film of carbon layer [ $\text{k}\Omega$ ]	Resistance between pads [ $\text{k}\Omega$ ]	Average resistance of CNT bundles [ $\text{k}\Omega$ ]
100	1.633 $\pm$ 0.0715	72	1.671 $\pm$ 0.0716
130	2.480 $\pm$ 0.3528	87	2.553 $\pm$ 0.354



**Figure 5.8** Schematic circuits of resistance. (a) Equivalent resistance structure without CNT bundles connection to contact pads; (b) Equivalent resistance structure with CNT bundles connection to contact pads.

**Table 5.6:** Comparison of CNT bundles resistance.

	$R_{con}$ $\Omega$	$R_{CNT}$ $\Omega\mu m^{-1}$	$R_{CNT}$ $\Omega\mu m$
Previous work $Al_2O_3$ [67]	$1041 \pm 116$	$2.25 \pm 0.4$	18000
Previous work $ZrN$ [67]	$786 \pm 83$	$2.4 \pm 0.29$	19200
This work	-	29.3	879 - 2930

Compared with previous measurement results of barrier layer as  $Al_2O_3$  and  $ZrN$ , the area (depth x height) of that CNT sheets are  $10 \mu m \times 800 \mu m$  [67] which range from  $2 \mu m \times 15 \mu m$

to 4  $\mu\text{m}$  x 20  $\mu\text{m}$  in our work. It is clear to see that the CNT bundles have a better conductivity with barrier layer of Ti/TiN in this work than the previous work with barrier layer of  $\text{Al}_2\text{O}_3$  and  $\text{ZrN}$ .

## 5.4 Conclusion

This chapter mainly functions as showing the process results and measurement results. First, we show some microscopy inspection images from 3D microscopy Keyence and high-resolution SEM. The top of the bundles will be densified in the acetone. Raman inspections of each step after CNT deposition are provided to show all the later process will give a negative influence on CNT bundles' quality. The vapour HF damages the bundle the most. We also noticed that the coating of SiC protects the bundles from oxygen plasma etching.

TLM measurement is not possible to execute because no bundles completely get touch with all the contact pads with enough length. The average sheet resistance of 10 nm/50 nm Ti/TiN layer is calculated as  $33.34 \pm 2.309 \, \Omega/\square$  and  $23.96 \pm 0.763 \, \Omega/\square$  for 1 hour and 2 hours deposition of CNT respectively. There is a thin film layer of carbons which will influence the conductivity everywhere on the wafer and shows a better conductivity for a longer deposition time. The resistance of CNT bundles is also calculated to get an average value of  $1.671 \pm 0.0716 \, \text{k}\Omega$  and  $2.553 \pm 0.354 \, \text{k}\Omega$  for 100  $\mu\text{m}$  length. The width and thickness are presented as Appendix B.

Up to now, we have not been successful in fabricating the MEMS switches. Firstly, even though we tried the recipe with 650°C which can give a growth up to 138  $\mu\text{m}$  with masks from previous work, however, this recipe does not work for our design. The average length at this recipe in our topology is always shorter than 100  $\mu\text{m}$  which can be attributed to the different topologies will have an influence on the temperature distribution then influence the CNTs' growth. Moreover, we did not expect most of the bundles are already self-aligned to the left side which is an undesired result in our case. The reason will be detailed discussed in the next chapter. Many efforts have been done to correct and improve this which will be shown in the next chapter as well.

## 6. In-depth investigation of CNT bundle growth and optimization of horizontalization process

In previous discussion, the CNT bundles are preferably to be aligned to left during the deposition, and the previous recipe for horizontalization does not work anymore in this situation. So we defined a new recipe for the horizontalization process. This chapter serves as an optimization for horizontalization test and a deeper investigation of CNT bundle growth.

### 6.1. Influences of location in CNT growth

When performing the LPCVD deposition in the BM, the chip tiles are put on a graphite substrate holder shown in the figure 6.1 (a). During the deposition, the heating sources come from the bottom of the substrate (the bottom heater) and the gases come from the top through a showerhead. Because we will process small pieces (5 – 8 dies, each die size 10 mm x10 mm) on the 4 inches substrate holder, the location of these pieces is impossible to be precisely controlled to be on the same location each time. As the location is related to the actual inner conditions such as gas flow and surface temperature distribution which can give an influence to the CNT growth, we, therefore, supplied a whole wafer growth in the chamber to detect the influence of the location of the pieces by measuring the length and quality (by Raman inspection) of the CNT bundles.

#### 6.1.1. Bundle dimension and length

In order to see whether the bundles' dimension will influence the length, several dimensions in one die were chosen randomly for the length measurement as Table 6.1 shows. The CNT bundles were supplied with the bottom temperature at 650°C for 1.5 hours.

**Table 6.1:** Length measurements of carbon nanotubes with different bundle dimension

Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ ) in structure i	2x10	2x10	2x15	2x15	3x15	4x20	Average length ( $\mu\text{m}$ )
Length ( $\mu\text{m}$ )	85	85	85	80	80	85	$83.3 \pm 6.7$
Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ ) in structure ii	2x15	2x15	3x20				
Length ( $\mu\text{m}$ )	85	85	80				$83.3 \pm 8.3$
Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ ) in structure iii	2x15	2x15	2x20				

Length ( $\mu\text{m}$ )	80	80	85				$81.7 \pm 8.3$
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Because there were nearly no bundles which are perfectly vertically aligned, the measurement was taken after horizontalization. That gave the resolution of length measurement at 5  $\mu\text{m}$  because some bundles were not completely flattened and most bundles have a curve shape at the tip which can be seen in Appendix G. In another words, the real bundle length could be 5 -10  $\mu\text{m}$  longer than the measurement results. We did this and the following measurement only to show that different growth conditions can have an influence on the CNT growth with comparing their roughly horizontal length with curved tip shape.

From Table 6.1, we can see the different bundle dimension did not give an obvious influence on CNT bundles' length in one die. That can be the aspect ratio among these bundles not much differences so that the dimension will not be the main factor for length. It needs to be mentioned that in for significant larger dimension (180  $\mu\text{m}$  x 180  $\mu\text{m}$ ) on the same wafer, we observed extra-long bundles ( $155 \pm 5 \mu\text{m}$ ).

### 6.1.2. Length distribution

One 4 inch wafer which contains 52 dies (10 mmx10mm) with CNT growth of bottom temperature at 650°C for 1.5 hours is supplied in this test. The wafer flat mark faced the operator. As we previously got the conclusion that different dimension will not have an obvious influence on CNT bundles' growth, we chose the measured bundles randomly for each die. See the results as shown in Table 6.2. The measurement resolution is 5  $\mu\text{m}$ .

**Table 6.2:** Length of carbon nanotubes at different locations

Die number			<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>		
Length ( $\mu\text{m}$ )			85	85	80	85		
Die number		<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>	<b>9</b>	<b>10</b>	
Length ( $\mu\text{m}$ )		85	75	65	65	65	65	
Die number	<b>11</b>	<b>12</b>	<b>13</b>	<b>14</b>	<b>15</b>	<b>16</b>	<b>17</b>	<b>18</b>
Length ( $\mu\text{m}$ )	80	65	55	55	60	65	55	75

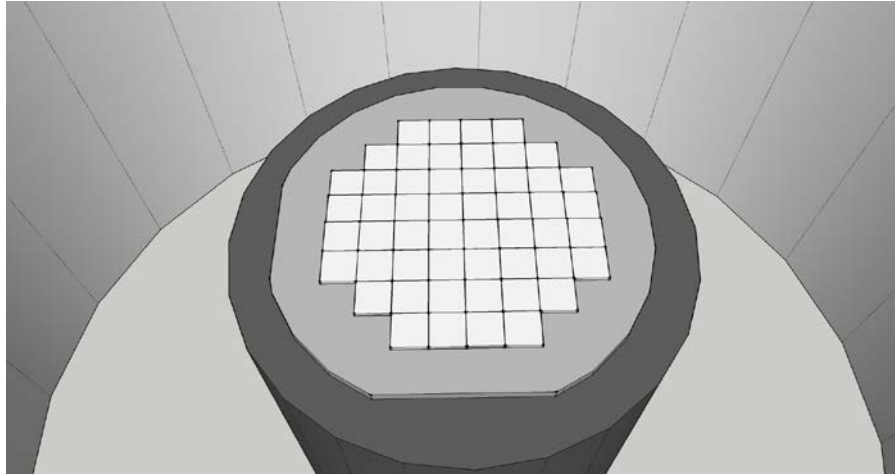


Die number	<b>19</b>	<b>20</b>	<b>21</b>	<b>22</b>	<b>23</b>	<b>24</b>	<b>25</b>	<b>26</b>
Length ( $\mu\text{m}$ )	90	70	55	50	45	50	70	75
Die number	<b>27</b>	<b>28</b>	<b>29</b>	<b>30</b>	<b>31</b>	<b>32</b>	<b>33</b>	<b>34</b>
Length ( $\mu\text{m}$ )	80	65	50	45	45	55	60	75
Die number	<b>35</b>	<b>36</b>	<b>37</b>	<b>38</b>	<b>39</b>	<b>40</b>	<b>41</b>	<b>42</b>
Length ( $\mu\text{m}$ )	80	65	45	40	40	50	50	75
Die number		<b>43</b>	<b>44</b>	<b>45</b>	<b>46</b>	<b>47</b>	<b>48</b>	
Length ( $\mu\text{m}$ )		60	45	40	35	50	55	
Die number			<b>49</b>	<b>50</b>	<b>51</b>	<b>52</b>		
Length ( $\mu\text{m}$ )			60	50	45	55		

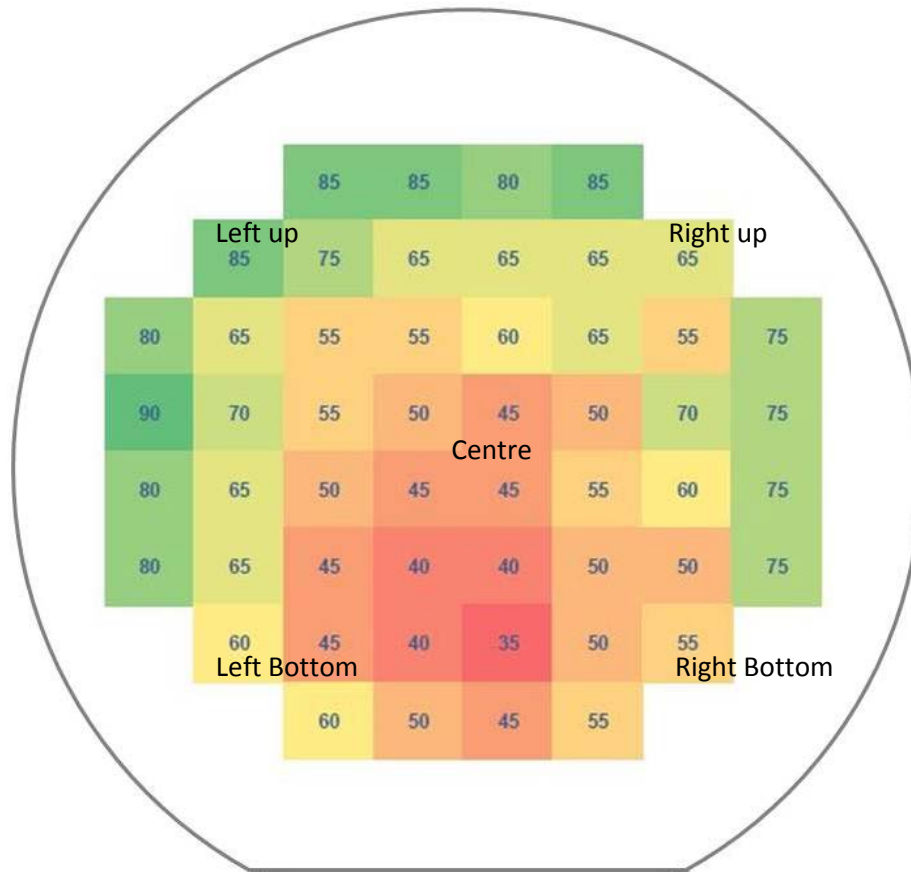
The CNT growth rate follows a parabolic relation with temperature [68]. Below a certain temperature level, the growth rate increases with temperature but turns to be a negative relation with temperature after a point of inflection. As we have observed that lower temperature than 650°C can give longer growth which will be shown in the later experiments, that means at 650°C we have exceeded the inflection temperature. In other words, the longer lengths in Table 6.2 showed likely a lower substrate temperature. Figure 6.1 shows the temperature distribution corresponding to Table 6.2.

It is obviously seen that the different locations relate to different temperature. The center point has a higher temperature than the periphery. The temperature in the right part is a little bit higher than the left. And the temperature at the bottom area is higher than the temperature in the upper area. The cause of this is the single-zone heater design of the BM.

In order to keep the accordance for the rest of the tests, individual samples were put in the center of the chamber.



(a)

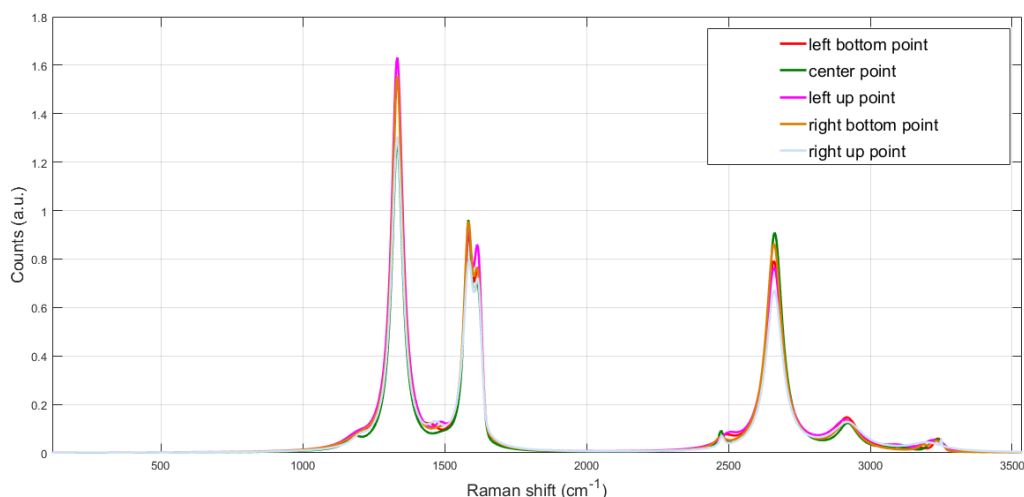


(b)

**Figure 6.1** Whole wafer CNT growth in Blackmagic chamber. (a) Reaction chamber in Blackmagic. (b) Temperature distribution in different location.

### 6.1.3. Raman microscopy

The Raman spectra of CNT at different locations is shown in the figure 6.2 and Table 6.3.



**Figure 6.2** Raman spectra of CNT in different points on the same wafer which is supplied with deposition at 650°C for 1.5 hours

**Table 6.3:** Raman data of different points on the same wafer which is supplied with deposition at 650°C for 1.5 hours.

Location point (see figure 6.1)	Intensity ratio			FWHM [cm <sup>-1</sup> ]			
	I <sub>D/G</sub>	I <sub>D'/G</sub>	I <sub>G'/G</sub>	D	G	D'	G'
Center	1.37	0.53	0.97	47	35	31	64
Left up	1.81	0.66	0.85	48	41	28	72
Left bottom	1.74	0.54	0.89	45	44	26	67
Right up	1.67	0.57	0.86	49	48	26	71
Right bottom	1.66	0.54	0.93	45	40	29	67

From the Table 6.3, the center point shows a largest I<sub>D/G</sub> and I<sub>D'/G</sub> ratio, smallest I<sub>G'/G</sub> ratio, and sharpest FWHM of G band which all indicates that CNT in the center point has better crystallinity and quality. This is consistent with the previous conclusion that higher temperature gives a better crystallinity with Fe catalyzer [66]. On the contrast, the left up point is indicated to be the lowest temperature and less crystallinity.

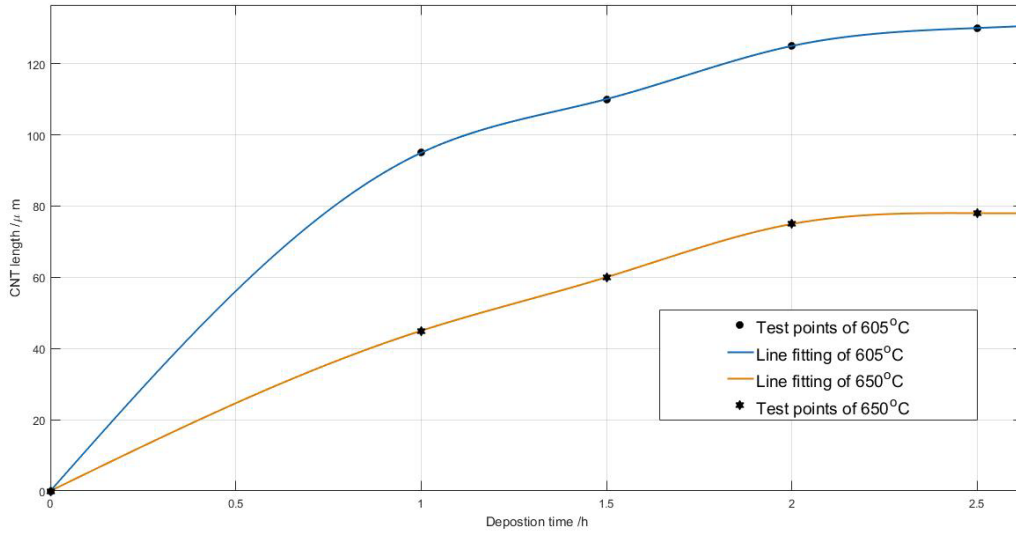
#### 6.1.4. Discussion

From the previous measurements of carbon nanotube bundles' length, it is shown that the dimension of bundles will not give an obvious influence on bundles' length which might due to the aspect ratios of bundles are more or less the same. However, the location in the reaction chamber indeed showed a significant influence on CNT growth. The inner temperature is higher than the outer field and the highest temperature location is at around the bottom side of the chamber. The Raman inspection also verified the conclusion that the inner location has better crystallinity which means the central temperature is higher than the outer periphery. In this case, when we process with small pieces, we should align the pieces at the location as the same as possible. In our later process, all pieces are located at the center of the chamber.

## 6.2. Influences of growing time in CNT growth

### 6.2.1. Length of CNT bundles in different growing time

We measured the average length of CNT bundles after horizontalization in acetone under different deposition time and temperatures as figure 6.3 shows.

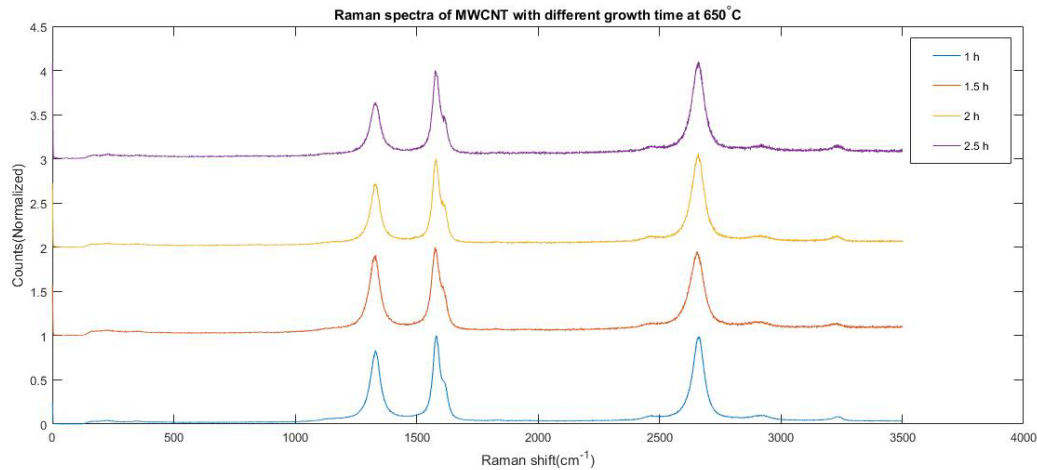


**Figure 6.3:** Length of CNT bundles with deposition time in BM.

Figure 6.3 is the CNT length by smoothing spline fitting with smoothing parameter  $p > 0.9999$  in different growing time under deposition temperature of 605 and 650 independently. With deposition time increasing, the growth rate became slower and slower. This is explored by previous research that the catalyst being supplied with too much carbon over time which poisons the catalyst [69]. The 605°C can give a length and growth rate larger than 650°C, which shows as we mentioned before that the peak inflection point of largest growth rate is lower than 650°C. For most of the samples grown between 600°C to 700°C, a no more obvious increase of CNT length were observed after a growing time longer than 2 hours for our dimensions. Therefore, the following samples are mostly supplied with growing time of 2 hours.

### 6.2.2. Raman microscopy inspection

The Raman inspection of 650°C growth with different growing time is measured. It is obvious to see the ID is lower but the IG keeps constant as the growing time increases which mean the longer growing time gives better quality and more crystallinity of CNT. All the samples are located in the centre of reaction chamber in BM.



**Figure 6.4:** Raman spectra of CNT with different growing time at the temperature of 650°C.

### 6.2.3. Discussion

The growth rate increases with time in the beginning but decreases after a certain inflection point. This gives the length of carbon nanotubes a trend that it is positive to reaction time in the beginning, but after 2 hours, it will not give a longer growth anymore. Besides, the Raman inspection shows that with longer growing time, CNT bundles will have better quality.

In our later process, all pieces are supplied with a growing time of 2 hours for the long length and good CNT quality.

## 6.3. Influences of bottom temperature in CNT growth

### 6.3.1. Length of CNT bundles

We measured the length of the CNT bundles of different bottom temperature from 600°C to 650°C for 2 hours separately. See the results as shown in Table 6.4. It is clear to see that the longest length of CNT shows a parabolic relation to the temperature. The peak inflection temperature appears at around 605°C which can give a length up to 110  $\mu\text{m}$ . With a temperature higher than 700°C, hardly any CNT growth is observed.

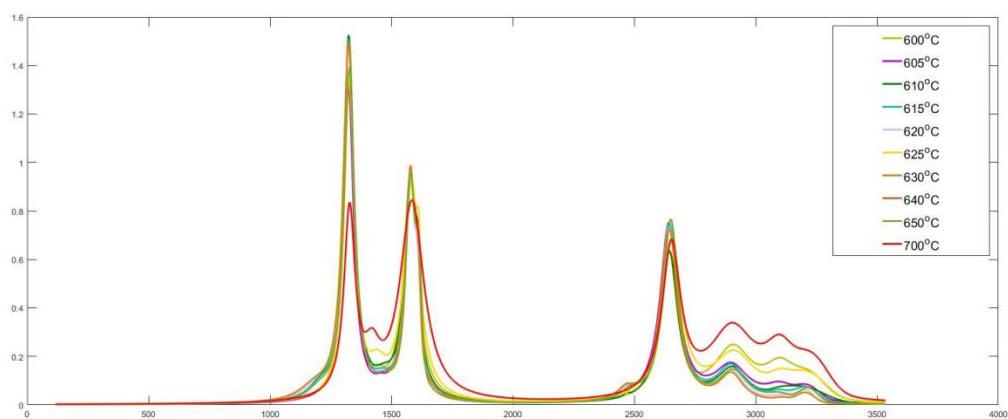
**Table 6.4:** Length of CNT bundles at different bottom temperature

Length ( $\mu\text{m}$ )	1	2	3	4	5	Average ( $\mu\text{m}$ )
700°C	20	25	20	30	30	25 $\pm$ 25
650°C	60	55	55	60	55	57 $\pm$ 7.5

640°C	65	60	60	60	65	62±7.5
630°C	75	80	80	75	70	76±17.5
620°C	75	75	80	75	85	78±20
615°C	80	80	80	80	85	81±5
610°C	85	85	90	95	90	89±17.5
605°C	100	100	105	100	110	103±20
600°C	100	95	95	95	100	97±7.5

### 6.3.2. Raman inspection

Figure 6.5 shows a trend that higher temperature gives a smaller width of G band and a smaller  $I_{D/G}$  which all indicate more crystallinity. Table 6.5 also shows this trend as the  $I_{D'/G}$  and  $I_{G'/G}$  increase with higher temperature. A decrease in  $I_{D/G}$  and an increase in  $I_{G'/G}$  mean an increase in quality. However, the increase in  $I_{D'/G}$  shows a conflict.



**Figure 6.5** Raman spectra of CNT deposited at different temperature for 2 hours.

**Table 6.5:** Raman data of samples deposited at different temperature for 2 hours.

Temperature	Intensity ratio	FWHM [ $\text{cm}^{-1}$ ]
-------------	-----------------	---------------------------

	$I_{D/G}$	$I_{D'/G}$	$I_{G'/G}$	D	G	D'	G'
600°C	1.40	0.19	0.64	48	68	20	79
605°C	1.36	0.21	0.77	52	58	19	89
610°C	1.61	0.29	0.67	54	58	23	85
615°C	1.59	0.14	0.79	52	55	21	85
620°C	1.53	0.27	0.77	52	53	19	82
625°C	1.45	0.23	0.72	51	77	15	95
630°C	1.53	0.32	0.74	55	51	22	84
640°C	1.48	0.42	0.81	53	46	28	78
650°C	1.38	0.39	0.83	53	48	25	78
700°C	0.93	-	0.76	56	119	-	92

### 6.3.3. Discussion

The length of CNT will increase with the temperature increasing, after the inflection point at around 605°C, the length will be shorter.

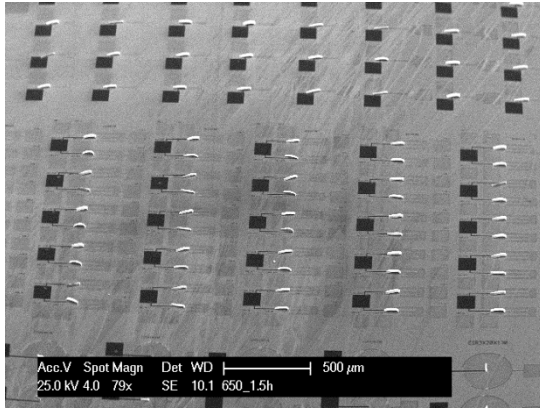
However, no matter how long the CNT bundles can grow, the higher temperature gives bundles better quality and more crystallinity.

Moreover, combined the Table 6.4 and figure 6.1, it is surprising to find that the temperature difference can go beyond 50°C in the same deposition recipe only due to the location difference.

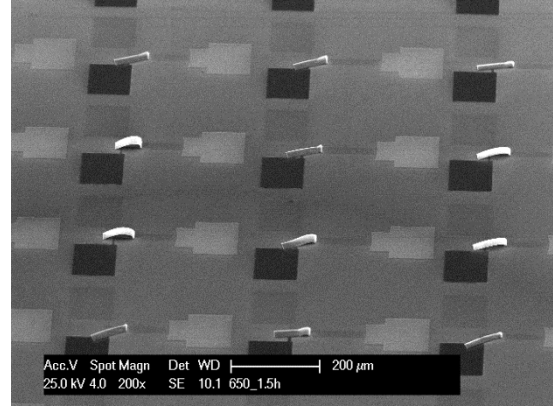
## 6.4. Influences of substrate topology in CNT growth

In our design, we aimed at making the bundles folded to the right side, thereby the CNT cantilevers being able to contact with the contact pad. However, after growing carbon nanotubes by LPCVD, we observed that the bundles show an obvious appealing to fall to the left, especially when the length of CNT bundles reaches more than 50  $\mu\text{m}$ . Figure 6.6 shows the CNT bundles grew to the left after LPCVD for 1.5 h at 650°C.

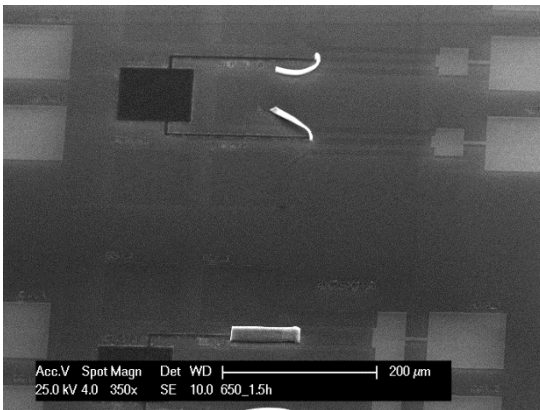




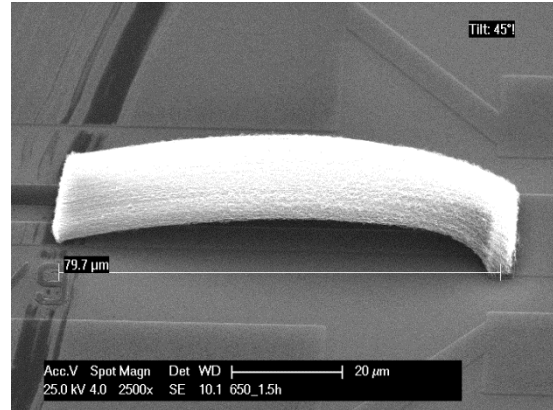
(a)



(b)



(c)

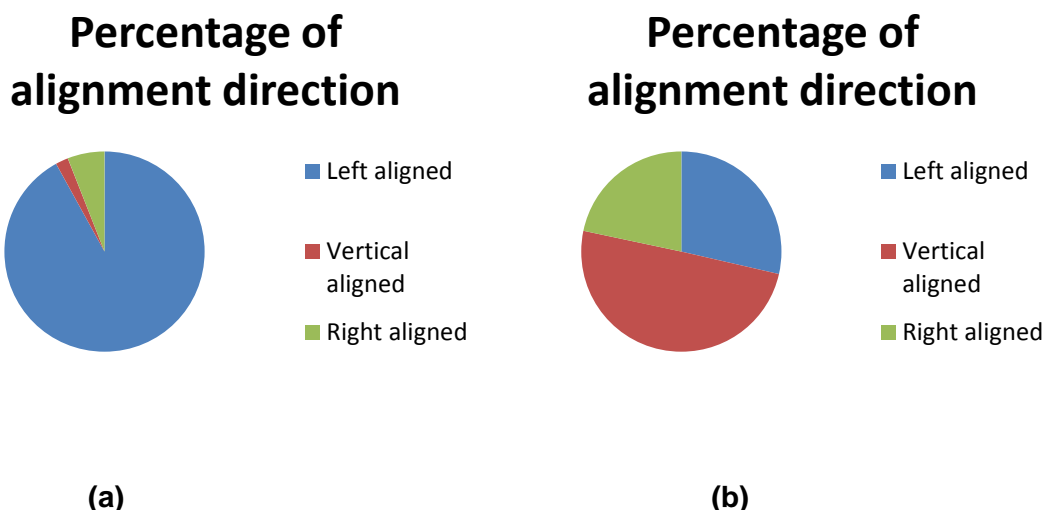


(d)

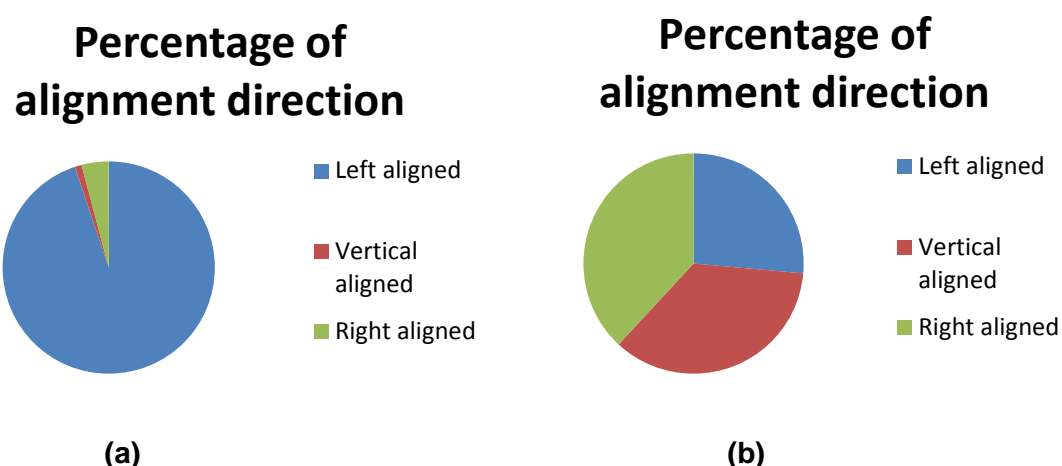
**Figure 6.6** SEM inspection of CNT bundles grew to the left. (a) CNT bundles grew to the left with patterning II and III at the percentage of nearly 100%. (b) High magnification of CNT bundles growing to the left with patterning II. (c) Close-up of CNT bundles growing to the left of patterning I and II. (d) One CNT bundle growing to the left at the length of 79.7 μm..

In order to verify the assumption that most bundles showed a preference to the left side during the LPCVD deposition is because of the substrate topology but not due to other factors, we grew CNT bundles of two wafers without metal patterning. One of them is performed at bottom temperature of at 620 °C without top heat for 2 hours, and the other one at bottom temperature of 600°C with top heat of 600°C independently. One die was selected from each wafer, recording the number of bundles that fall to the left, right, and vertical standing among three structure designs.

#### 6.4.1. Influence from substrate topology



**Figure 6.7** Percentage of CNT bundles alignment after growth at the recipe of the bottom temperature of 620°C for 2 hours. (a) Patterned substrate layers; (b) Un-patterned substrate layers.



**Figure 6.8** Percentage of CNT bundles alignment after growth at the recipe of the bottom temperature of 600°C and top heat of 600°C for 2 hours. (a) Patterned substrate layers; (b) Un-patterned substrate layers.

From the Table H.1, Table H.2 (see Appendix H), figure 6.7, and figure 6.8, it is clear to show that no matter with or without top heat, the CNT bundles grew on un-patterned substrate topology have at least 30% possibility to be vertically aligned which is rare to see in the patterned substrate samples. And the ratio of left aligned and right aligned in unpatterned topology (1.32 at 620°C bottom temperature for 2 hours, 0.69 at 600°C bottom temperature and 600°C top heat) is far less than patterned topology (15.4 at 620°C bottom temperature for 2 hours, 22.95 at 600°C bottom temperature and 600°C top heat). It is no doubt to draw

the conclusion that the patterning of the substrate will give a significant influence on CNT bundles alignment during the growth.

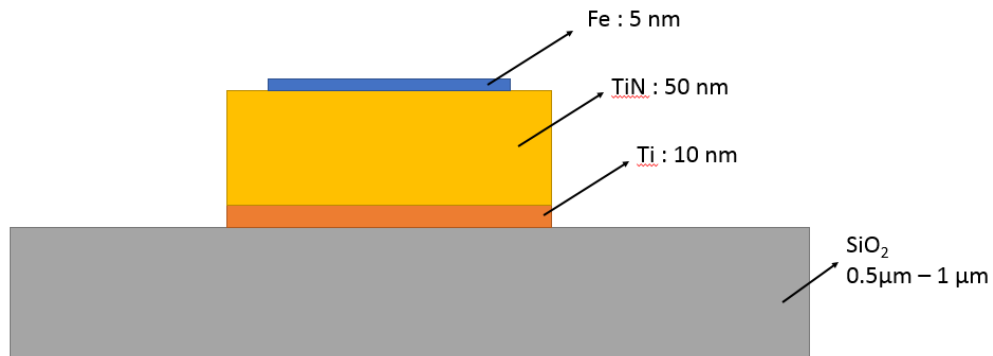
In order to understand what was happening during the deposition, we provided some potential explanations and conjectures for this phenomenon as gas flow and real temperature distribution. Therefore, simulation is provided to show the temperature influences.

#### 6.4.2. Simulation and analysis

The model's profile is shown in Figure 6.9. The bottom layer is silicon oxide at a thickness of 0.5  $\mu\text{m}$  or 1  $\mu\text{m}$ . The second bottom layer is Titanium at a thickness of 10 nm which is exactly covered by the layer of TiN at a thickness of 50 nm. The top layer is Fe at a thickness of 5 nm. The dimensions match that of the actual geometry. The ambient is first pumped down to vacuum, then reaction gases flow in with room temperature. As the heat source is located under the sample, we assume that temperature nearby the metal layers are lower than bottom contact  $\text{SiO}_2$  layer. So, the initial temperatures are set as follow:

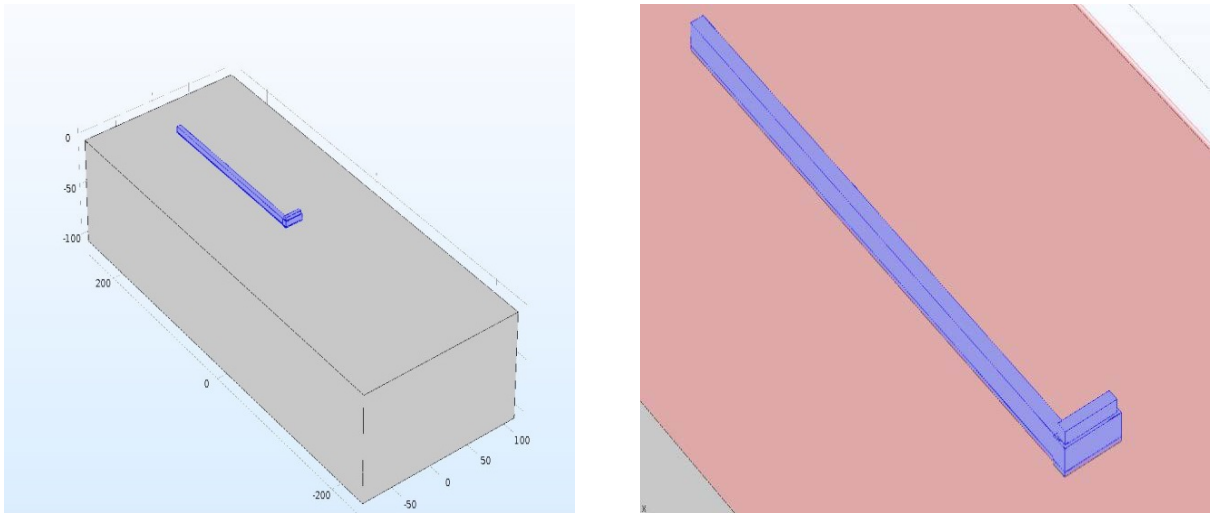
$$T_{\text{Ambient}} < T_{\text{Metal layers}} < T_{\text{SiO}_2}$$

Also, as the thermal conductivity of solid is larger than that of air, the heat transfer between metal layers and  $\text{SiO}_2$  is from  $\text{SiO}_2$  to metal layers,  $\text{SiO}_2$  to ambient and metal layers to ambient.

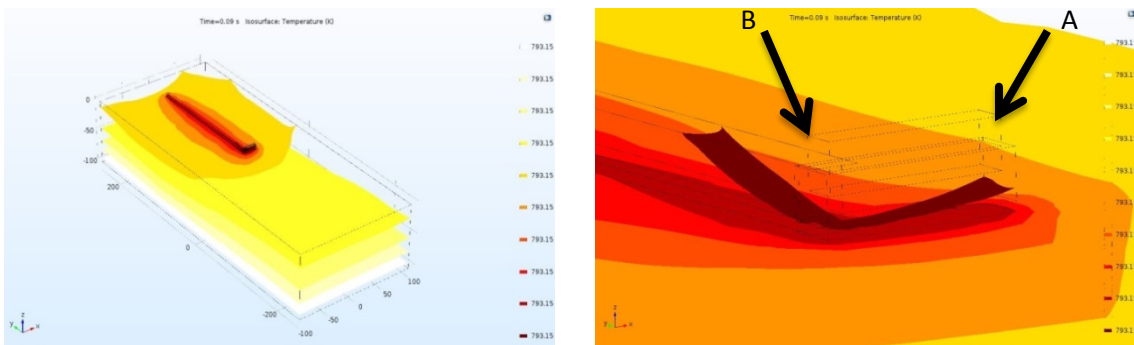


**Figure 6.9:** Structure profile of metal layers and  $\text{SiO}_2$  temperature heat source

On COMSOL Multiphysics, we build the one model as follow.



**Figure 6.10** Model structures in COMSOL Multiphysics



**Figure 6.11** model structures in COMSOL Multiphysics

The outside air boundary is set as a cylinder chamber approximately the same as a real condition at a diameter of 0.3 meters. The bottom surface of SiO<sub>2</sub> was set to a temperature of 650°C. Heat flux coefficient was set as  $h=0.1 \text{ W/(m}^2\cdot\text{K)}$ ). The initial temperature was set to room temperature 25°C (283.5 [K]).

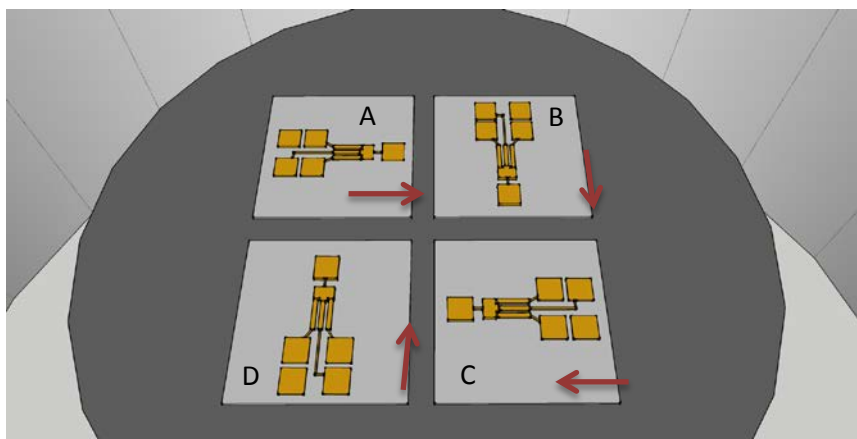
Figure 6.11 shows the temperature contour lines in metal layers at time point  $t=0.1 \text{ s}$ . It can be postulated that at the same XY level surface planer, point A and point B have different temperature. Because the heat transfer in metals is completed instantaneously, it is hard for the software to show the temperature value at the certain time point but only to show the trend.

From our previous discussion, after temperature exceeds than 605°C, the growth rate shows a negative relationship with the temperature. As the recipe we used is at 650°C, the higher temperature side will have a lower growth rate. From the simulation, it shows clearly that asymmetric substrate topology will give influence on temperature distribution over the area of

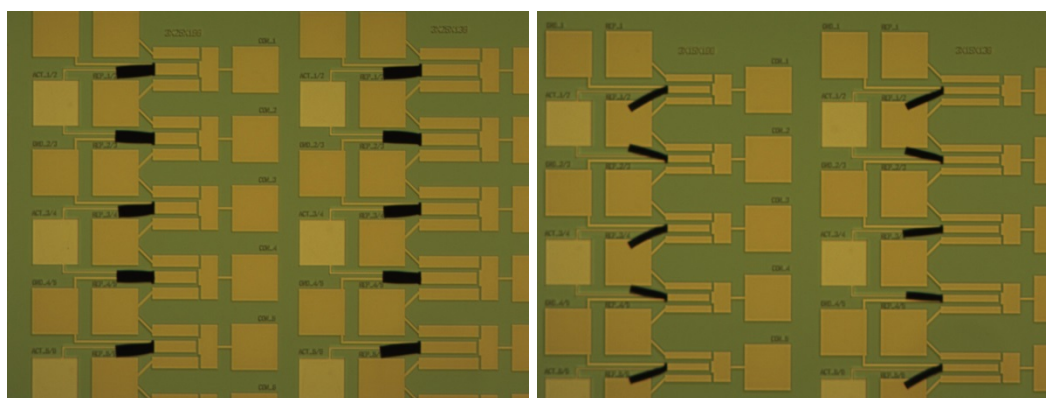
the bundle. The location with lower temperature distribution will give a positive influence on CNT growth rate, thereby causing bending towards point B which is at higher temperature and lower growth rate.

### 6.4.3. Gas flow

In order to figure out whether the gas flow can also be the influence factor of CNT bundles' alignment, we supplied some samples with the same recipe but changed the located orientation inside the reaction chamber. Four pieces are deposited with 90 °C rotation clockwise in turn like figure 6.12 shows, which are divided from one wafer fabricated with the same process parameters.

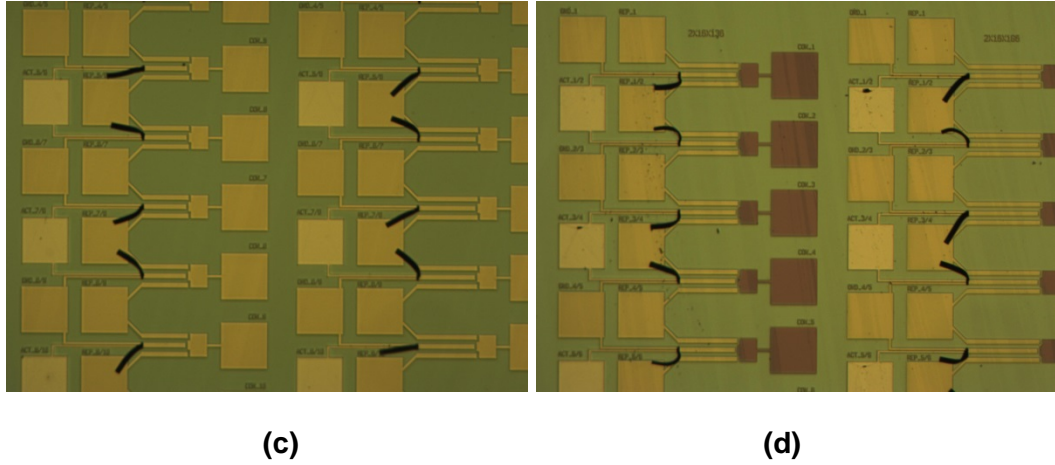


**Figure 6.12** Conceptual illustration of pieces direction in BM.



**(a)**

**(b)**



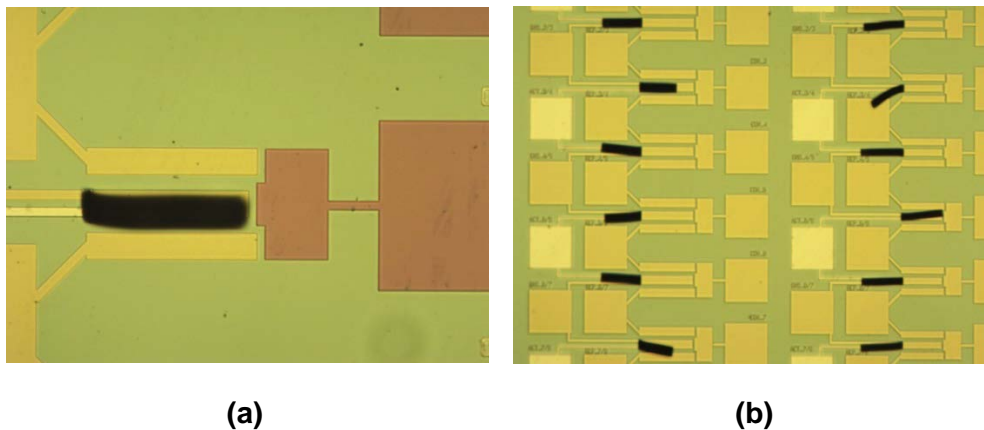
**Figure 6.13** Microscopy inspection of four orientation samples, each rotated with 90°. (a) Inspection of piece A. (b) Inspection of piece B. (c) Inspection of piece C. (d) Inspection of piece D.

From figure 6.13, it can be seen that the orientation of 0°, 90°, 180°, and 270° did not give significant correction bundles' alignment. Only some spiral occurred among small dimension bundles (2  $\mu\text{m}$  x 10 $\mu\text{m}$  and 2  $\mu\text{m}$  x 15 $\mu\text{m}$ ). Therefore, the sample orientation is not the key element for the self-alignment and does not work in correcting the alignment direction.

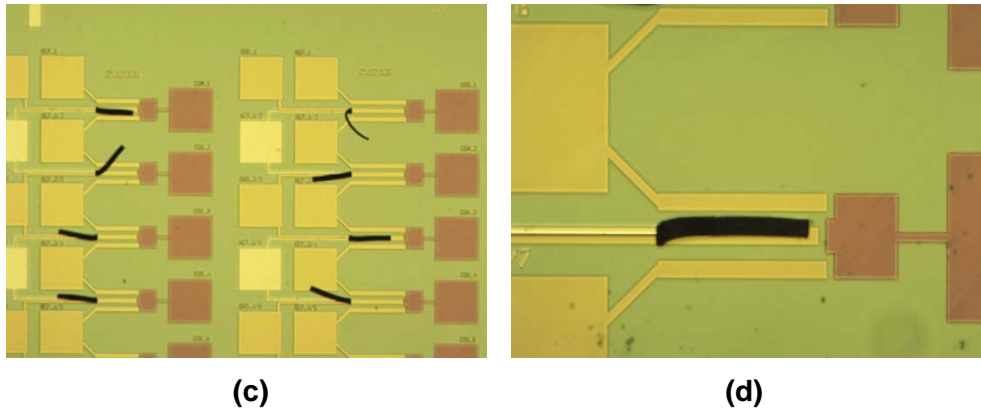
#### 6.4.4. Bottom temperature

As the temperature is the key element as we simulated, it is comprehensible that if we lower the temperature to some point, the lower temperature side will turn to give a negative influence on growth rate. That means, if we lower the temperature to some point where the temperature difference between two sides is large enough, there should be some right-aligned CNT bundles after deposition.

It is verified that with the bottom temperature at 600 °C, 605°C, 610 °C, 620 °C, and 625 °C, we observed a few bundles bending to the right side aligned at different extent as figure 6.14 shows. But with temperature over 630 °C, it can be hardly any bundles that are aligned to the right are observed.



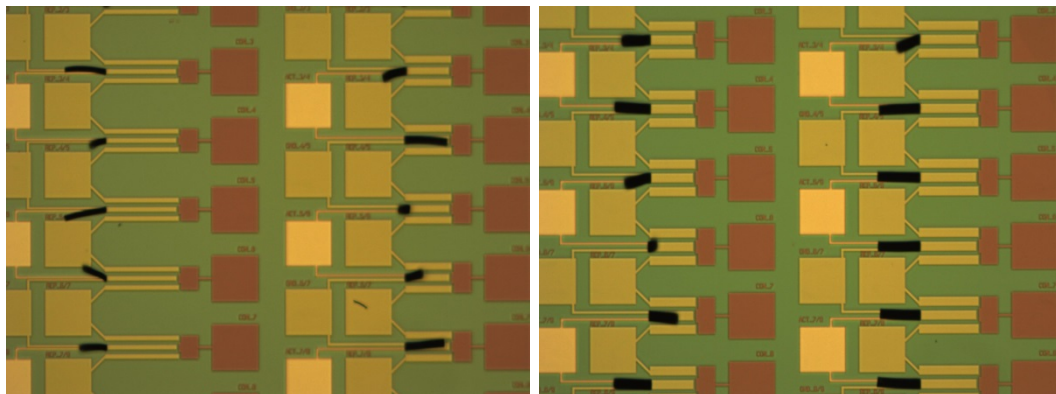




**Figure 6.14:** A few bundles self-aligned to the right side at the temperature from 600 °C to 620°C. (a) Temperature at 600°C. (b) Temperature at 605°C. (c) Temperature at 610°C. (d) Zoom in view of temperature at 610°C.

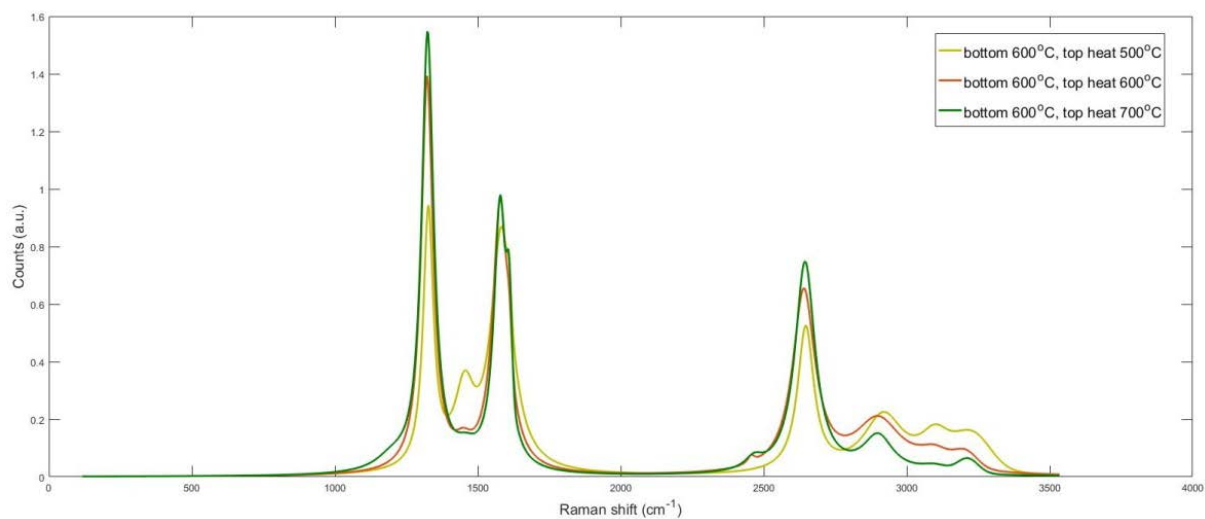
#### 6.4.5. Top heat

As the temperature is the essential cause of this alignment, we tried to supply energy with a different heating source to see if it can give a correction. Except for bottom heating, the BM can also give a top heat below the showerhead as the heating source. Several recipes as Table 6.8 shows have been tried.

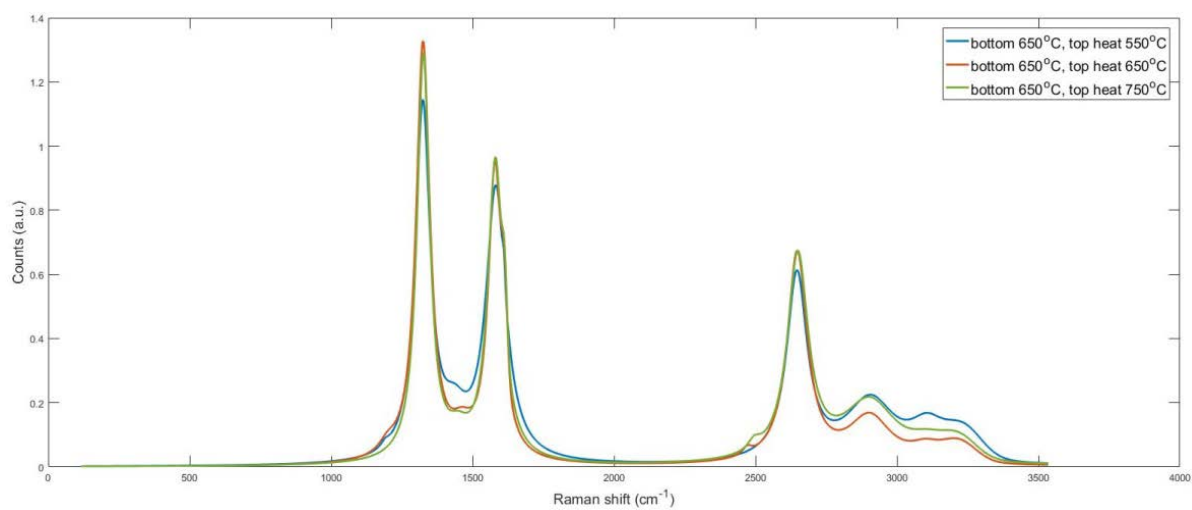


**Figure 6.15** CNT bundles at a growth temperature of 600°C with top heat 600°C.

The results show that with a bottom temperature at 600°C, all three samples with top heat at 500°C, 600°C, and 700°C have been observed with right-aligned bundles. At bottom heater temperatures above 650°C, no more right-aligned bundles were observed.

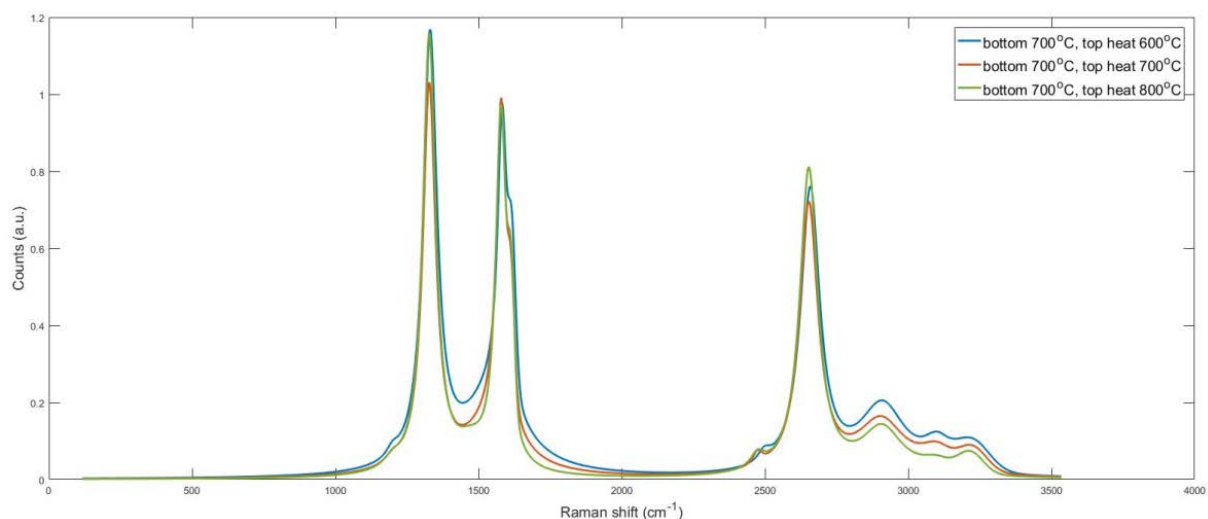


(a)



(b)





(C)

**Figure 6.16** Raman spectra of CNT grown on different temperature recipes. (a) Raman spectra of CNT grown on a bottom temperature at 600°C and top heat at 500°C, 600°C, and 700°C respectively. (b) Raman spectra of CNT grown on a bottom temperature at 650°C and top heat at 550°C, 650°C, and 750°C respectively. (c) Raman spectra of CNT grown on a bottom temperature at 700°C and top heat at 600°C, 700°C, and 800°C respectively.

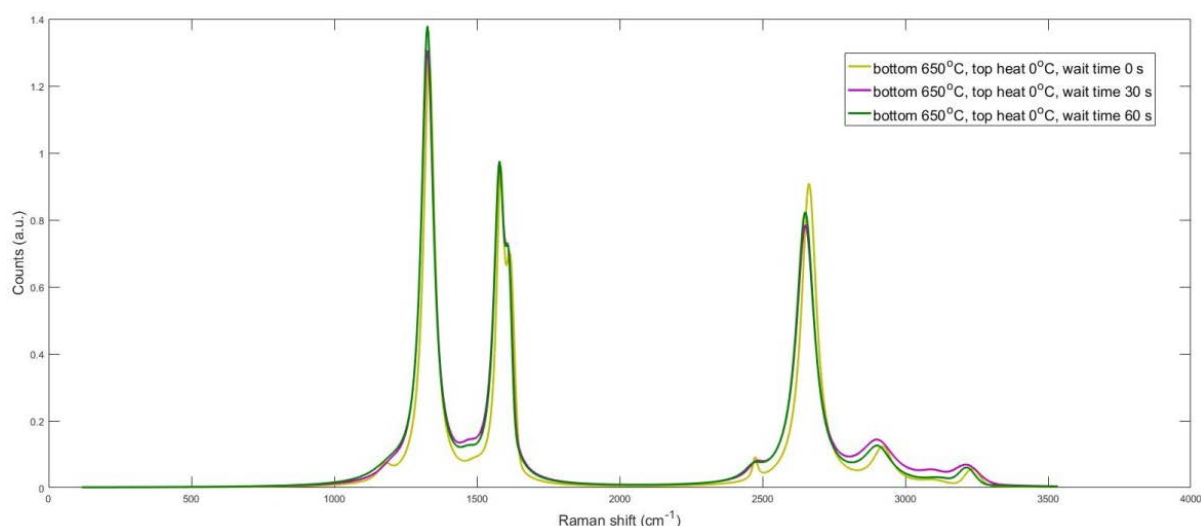
**Table 6.6:** Raman data obtained from different temperature recipes

Samples  Bottom temperature_top heat				FWHM ( $cm^{-1}$ )			
	$I_{D/G}$	$I_{D'/G}$	$I_{G'/G}$	D	G	D'	G'
600°C _500°C	1.06	0.12	0.60	43	89	15	69
600°C _600°C	1.45	0.14	0.66	50	65	19	95
600°C _700°C	1.59	0.36	0.77	50	53	20	85
650°C _550°C	1.30	0.08	0.69	63	84	10	87
650°C _650°C	1.42	0.28	0.71	58	57	24	85
650°C _750°C	1.34	0.22	0.68	54	64	20	89
700°C _600°C	1.46	0.45	0.96	58	38	30	80
700°C _700°C	1.16	0.31	0.81	54	41	27	78
700°C _800°C	1.21	0.33	0.84	54	46	26	75

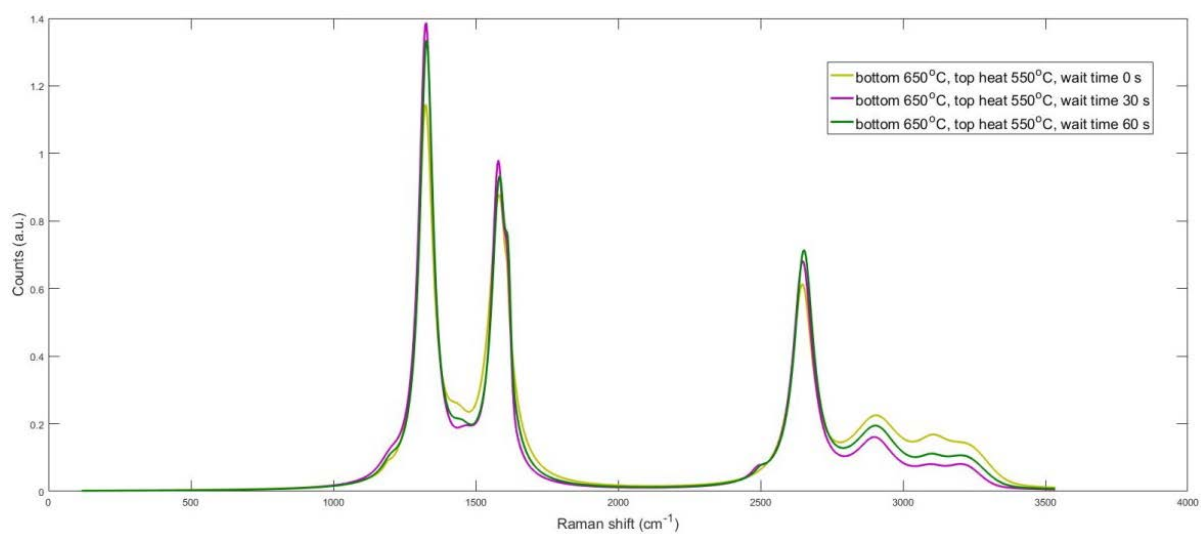
From figure 6.16 and Table 6.6, the result of bottom temperature at 600°C shows that the higher top heat, the higher  $I_{D/G}$  ratio, which indicates that there is worse quality for higher top heat temperature. As for bottom temperature at 650°C, the increasing of  $I_{D/G}$  indicates worse quality with temperature increasing, and it is hard to draw conclusions from other data. But for the bottom temperature at 700°C, this gives a conflict. It seems higher temperature gives a better quality which follows the previous conclusion.

#### 6.4.6. Wait time

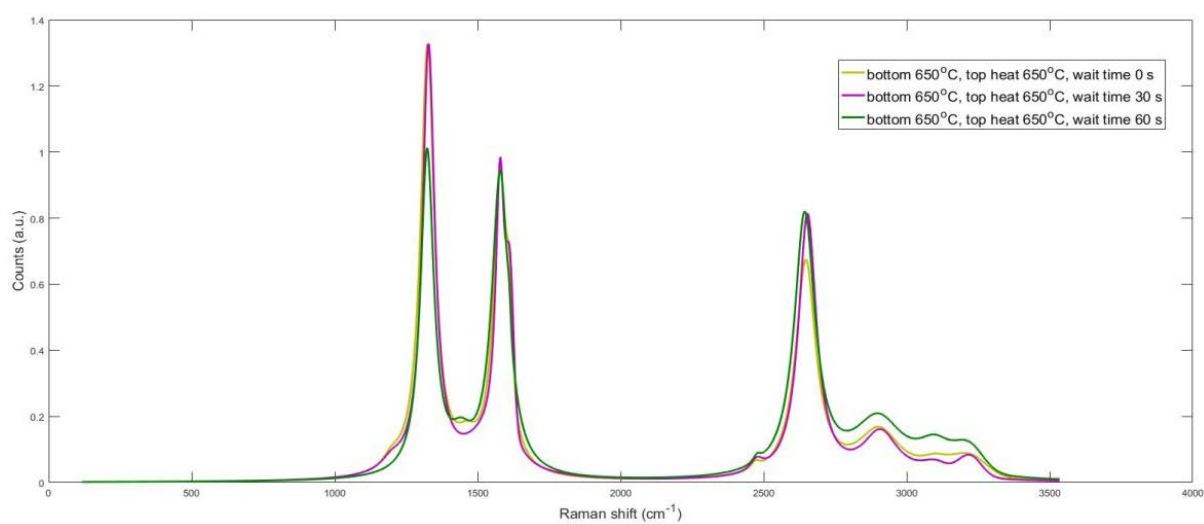
At the initial recipe we enable the  $CH_4$  when the temperature has not reached the desired target (normally 5°C lower). In this experiment, we postponed the gas insertion time to begin the growth when the temperature has been exactly what has been set plus an additional delay. The postponed time duration is so called the wait time. Several recipes are supplied as Table 6.7 shows.



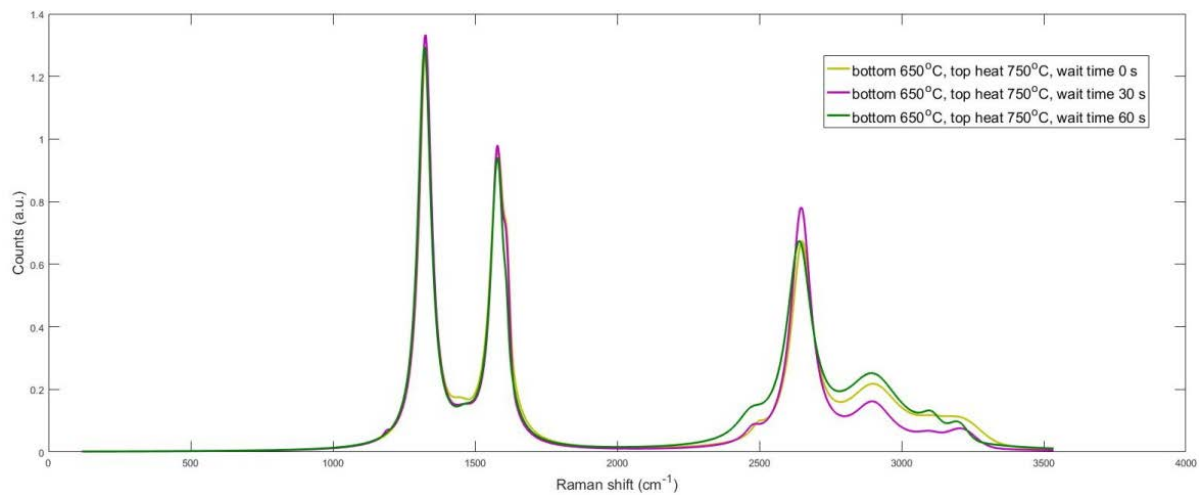
(a)



(b)



(c)



(d)

**Figure 6.17** Raman spectra of CNT grown on different heat temperature and wait time recipes. (a) Raman spectra of CNT grown on the bottom temperature at 650°C and no top heat with wait time 0, 30s, and 60s respectively. (b) Raman spectra of CNT grown on the bottom temperature at 650°C and top heat at 550°C with wait time 0, 30s, 60s respectively. (c) Fitted Raman spectra of CNT grown on the bottom temperature at 650°C and top heat at 650°C with wait time 0, 30s, 60s respectively. (d) Raman spectra of CNT grown on the bottom temperature at 650°C and top heat at 750°C with wait time 0, 30s, 60s respectively.

**Table 6.7:** Raman data obtained from different temperature recipes

Samples Bottom temperature_top heat_wait time				FWHM ( $cm^{-1}$ )			
	$I_{D/G}$	$I_{D'/G}$	$I_{G'/G}$	D	G	D'	G'
650°C_0_0 s	1.37	0.53	0.97	47	35	31	64
650°C_0_30 s	1.38	0.39	0.83	53	48	25	78
650°C_0_60 s	1.42	0.39	0.86	50	46	24	76
650°C_550°C_0 s	1.30	0.08	0.69	63	84	10	87
650°C_550°C_30 s	1.44	0.29	0.70	58	57	24	82
650°C_550°C_60 s	1.44	0.24	0.76	57	66	18	81
650°C_650°C_0 s	1.42	0.28	0.71	58	57	24	85

650°C_650°C _30 s	1.48	0.47	0.91	51	39	30	76
650°C_650°C _60 s	1.10	0.07	0.86	56	72	13	88
650°C_750°C _0 s	1.34	0.22	0.68	54	64	20	89
650°C_750°C _30 s	1.38	0.28	0.80	53	54	23	84
650°C_750°C _60 s	1.39	0.10	0.68	55	59	15	104

From Figure 6.17 and Table 6.7, no significant conclusion can be drawn. Also, from microscopy inspection, no changes or influences of length and alignment directions are observed. It can be because the wait time is very short compared to the deposition time (60 versus 7200 seconds) so that this factor will not give an obvious influence on the results. It can also be because the temperature can reach the desired point and a steady-state condition very quickly due to the relative low mass of the sample with respect to the reactor chamber.

## 6.5. Optimization for CNT horizontalization and densification

Any pieces which have shown a left-alignment during deposition supplied with horizontalization by acetone or IPA with the previous recipe discussed in chapter 3 did not make an influence for correcting the bundles direction from the left to the right. The IPA or acetone solution mainly functions to make the densification of the bundle and makes bundles better contact with the substrate. It did not change the direction of left-aligned bundles at all: they densify and fall on the substrate in the same direction as grown.

As we thought when we pull out the sample in the direction that desired alignment direction of bundles is the same as solutions dropping out direction, the bundles might be pulled by the force which the liquid supplied during dropping, however, Figure 6.18 shows pieces deposited at 650°C for 2 hours and horizontalized in acetone for 5 mins and drying for 5 mins with nothing changes happening. Therefore we tried to find a new method which can give a better rectification of bundles horizontalization into the desired direction.

### 6.5.1 Different solutions and increasing immersing time

The horizontalization is related to solutions' evaporate rate and surface tension, see the density, surface tension, and evaporate rate of these solutions as Table 6.8. The four solutions compounds all have an –OH group which relates to the Molecular Weight (MW). The evaporation rate is corresponding to the molecular weight. Also, a higher vapour pressure will evaporate easier.

**Table 6.8:** solutions evaporate rate and surface tension

Solutions	Molecular weight	Vapour pressure at 20°C [KPa]
Acetone	58	24.6
Ethanol	46	5.8
IPA	60	4.2

However, we made simple tests as Table 6.9 shows, to evaluate the evaporate rate of four commonly used solutions in the clean room, like acetone, ethanol, IPA, and water. The results show that acetone evaporates first, and then Ethanol, IPA, and water.

**Table 6.9:** Evaporate rate test

Solutions	Initial volume (ml)	Evaporate time (h)	Rest volume	Approximately evaporated volume (ml)
Acetone	200	3.5	120	80
Ethanol	200	3.5	170	30
IPA	200	3.5	175	25
Water	200	3.5	190	10
Evaporate rate	Acetone >> Ethanol > IPA >> Water			

The evaporate rate of ethanol is a little bit faster than IPA but not obvious. Water has the slowest evaporate rate among these solutions. Because this test is supplied in the SALAB wet bench of a clean room which has a venting system and lower humidity than natural ambient so that the evaporating rate of this test is much faster than natural evaporates rate sources from the literature.

First, we tried the same recipe as we defined before to see if the solution used for densification can change the direction of left-aligned bundles in Table 6.10. However, there was no change of bundles' direction observed as we did the same horizontalization recipe for CNT bundles with the asymmetric substrate for all the four solutions.

Secondly, we modified the recipe in Table 6.11 and Table 6.12 to see if the immersing angle and a longer immersing time will have an influence of the bundles' alignment. All the samples are supplied with 650°C\_2h recipes which gave the CNT bundles a mean length at  $70 \pm 20$   $\mu\text{m}$ .

**Table 6.10:** Samples supplied with previous horizontalization recipes by different solutions.

Solutions	Immersing angle	Immersing time	Drying time
Acetone	90	5	5
Ethanol	90	5	5
IPA	90	5	5
Water	90	5	10

**Table 6.11:** Samples supplied with different horizontalization recipes in immersing angles.

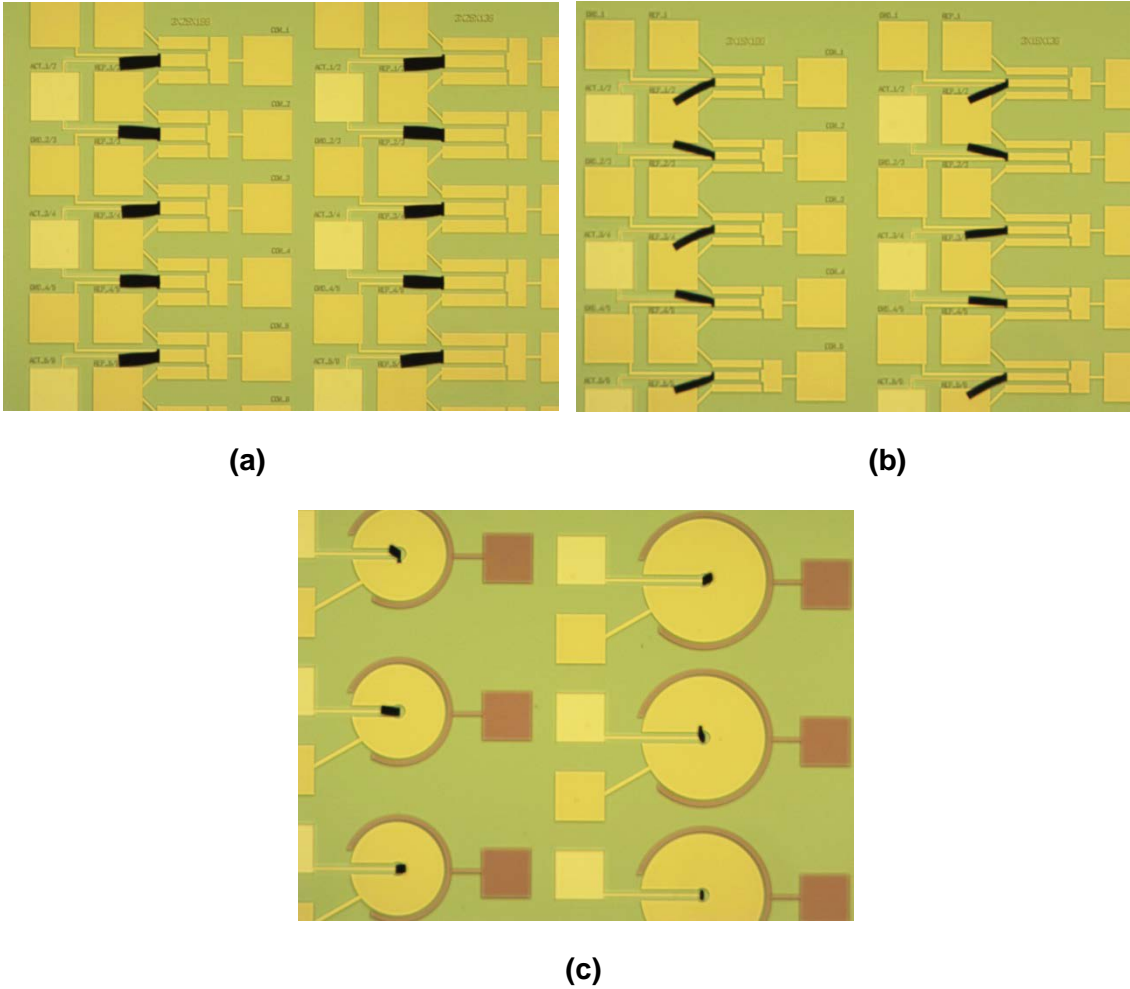
Solutions	Immersing angle	Immersing time	Drying time
Acetone	45	5	5
Ethanol	45	5	5
IPA	45	5	5
Water	45	5	10

**Table 6.12:** Samples supplied with different horizontalization recipes in immersing time.

Solutions	Immersing angle	Immersing time	Drying time
Acetone	90	10	5
Ethanol	90	10	5
IPA	90	10	5

Water	90	10	10
-------	----	----	----

However, the immersing angle, immersing time, and the drying time seem not to work in tuning the bundles' direction. See also figure 6.18.



**Figure 6.18** Samples supplied with different horizontalization recipes did not make any changes.

### 6.5.2 Immersing direction

As the buoyant force may be potential to change the bundles, we tried to modify the other parameters during immersing.

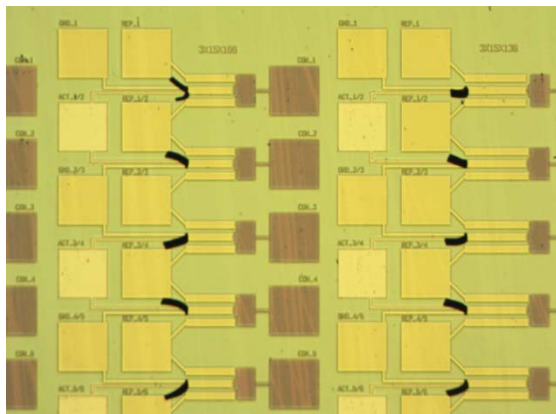
First we tried three samples which were deposited with 650°C recipes at 1 h, 1.5 h, 2 h separately. All these samples are immersed in acetone for 10 mins in the direction that the contact pads (the right side) are on the upside but dragged out from the solution with contact pads downside by rotating pieces with 180° before dragging them out of the solution. See the Table 6.13 below.

**Table 6.13:** Samples supplied with different horizontalization recipes in immersing directions.

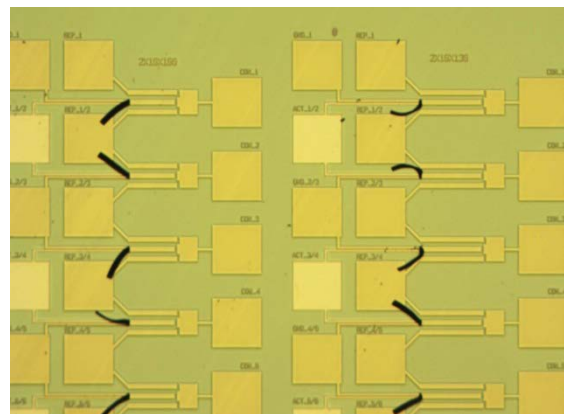


Piece number	CNT growth recipe	Immersing direction	Immersing solution	Immersing time (min)	Drying time
A	Bottom 600 °C & top heat 500 °C & 1 h	90 but contact pad downside	acetone	10	5
B	Bottom 600 °C & top heat 500 °C & 1.5 h	90 but contact pad downside	acetone	10	5
C	Bottom 600 °C & top heat 500 °C & 2 h	90 but contact pad downside	acetone	10	5

In this test, no changes in bundle direction were observed. Nevertheless, for some small width structures, bundles are not fully aligned to left. Bending on the root of the bundles are seen as figure 6.19 shows. Increasing the time in the solution and changing the immersing angles seem to give some influence on bundles shape reversing.



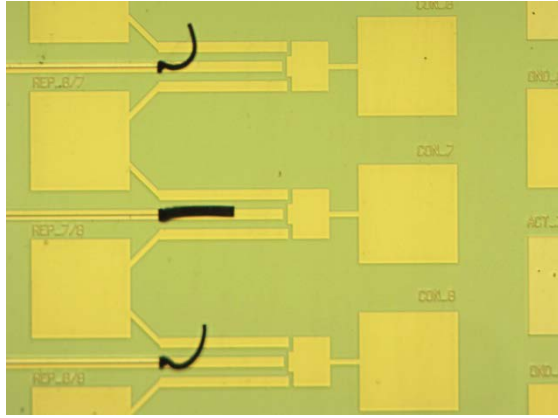
(a)



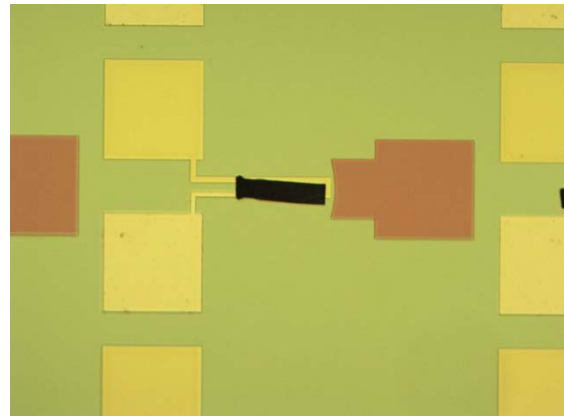
(b)



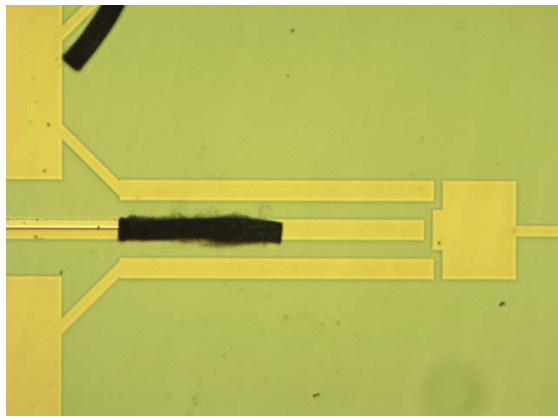




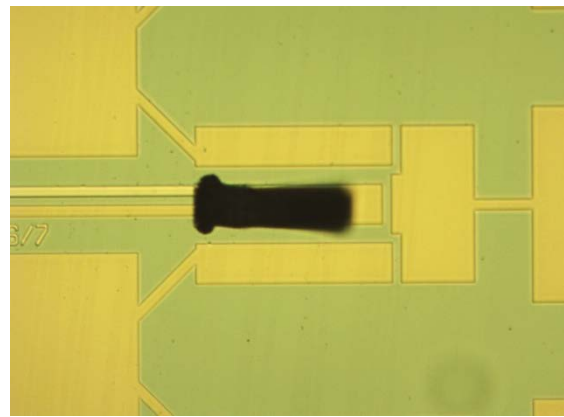
(e)



(f)



(g)



(h)

**Figure 6.20** Samples supplied with different horizontalization recipes in photoresists showed a big change on alignment. (a) Structure iii of sample D. (b) Structure i of sample D. (c) Structure iii of sample A. (d) Structure ii of sample D. (e) Structure iii of sample B. (f) Structure ii of sample B. (g) Structure iii of sample C. (h) Structure iii of sample C.

Figure 6.20 shows that some bundles unzipped at the middle and root due to the photoresist horizontalization. When the bundles are forced to align to the right, the shorter length of the left side will have an opposing force to the surface tension force making bundles to the right which is supplied by the solution. The asymmetry in the difference of length in the bundle causes additional forces within the bundle which are stronger than the Van der Waals forces and therefore start unzipping the bundle.

See the results for the number of right-aligned bundles as Table I.1 (see Appendix I). We defined the bundles that have changed more than  $90^\circ$  respect to left horizontally aligned can be thought as significantly influenced and direction changed by the horizontalization procedure.

From Table I.1, Table I.2, Table I.3 (see Appendix I), all the three structures have shown a big change in alignment correction. It needs to be mentioned that the blue marked rows are

the first die which was disposed by solutions and dragged out from the solutions first. These dies all show a larger percentage of alignment changes. So keeping the bundles exposed to the solution dispose and let the desired bundle direction keep the same as the solution dropping direction can help with alignment correction.

#### 6.5.4 Dispensing of the solutions

As the buoyance in the solutions might have a negative influence on alignment, we tried to replace immersing procedure with suspending the samples and keeping dispensing the solutions from the top to the bottom as the Table 6.15 and figure 6.21 shows.

All these four tiles were grown with the recipe bottom temperature at 650°C and top heat at 550°C for 2 hours which gave a normal length at  $70 \pm 10 \mu\text{m}$ .



**Figure 6.21** Dispensing solutions from the up to the bottom

**Table 6.15:** Right-aligned results of structure iii

	Photoresist	Process procedure	Dispensing of time (min)	Cleaning time by acetone (min)	Drying time (min)
A	SPR3012	Samples vertically	5	5	5
B	Acetone		5	5	5

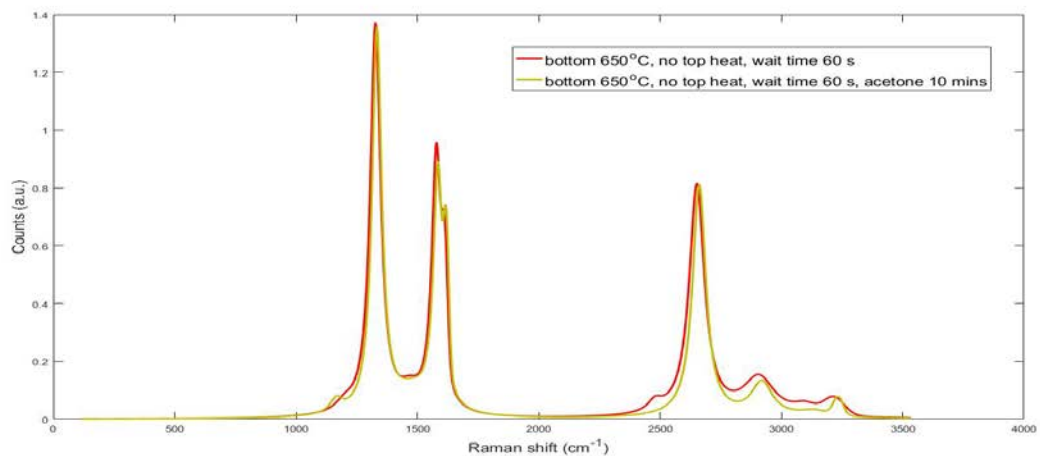
C	SPR3012	suspended and dispense of solutions from the top to the bottom	5	5	5
D	AZ2027		5	5	5

See the results of the number of right-aligned bundles in Appendix J. One die of each sample is chosen from the second row which shows an improvement compared to the dies on the second row in Appendix H and Appendix I. From Table 6.16 and figure 6.22, after horizontalized by acetone, IPA, SPR3012, and AZ3027, there are all showing higher  $I_{D/G}$  and  $I_{D'/G}$  which means more impurities and worse quality. After acetone, there are smaller FWHMs of D, D', and G' which normally indicate more crystallinity. After horizontalization in IPA, the FWHM are much larger which means less crystalline. It is hard to investigate the trend of FWHM with photoresists. The small sample space can generate an inaccuracy in this conclusion. More tests need to be done before a conclusion can be drawn.

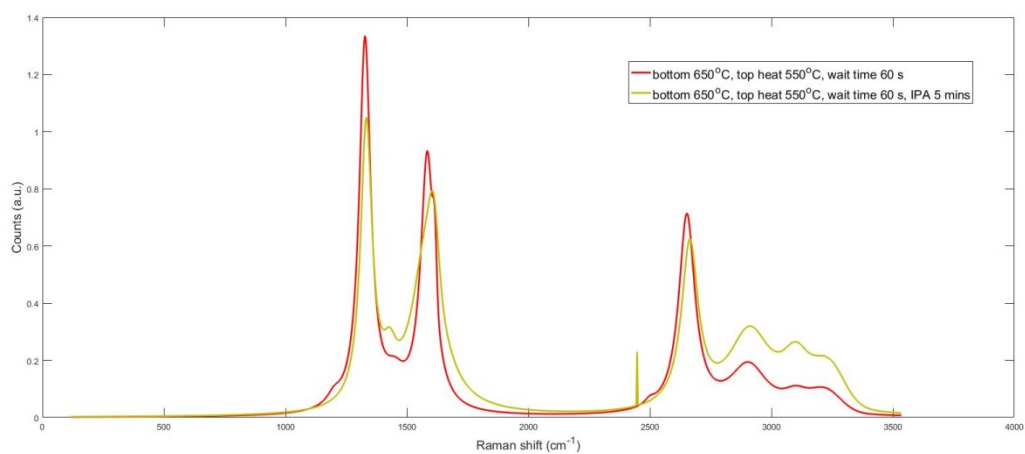
### 6.5.5 Raman comparison of different solutions

**Table 6.16:** Raman data obtained from CNT bundles in different horizontalization solutions

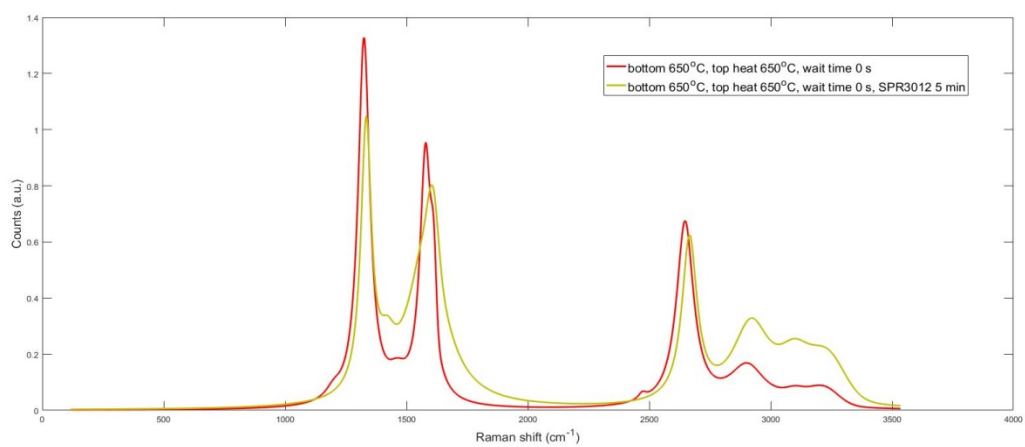
Samples Bottom temperature_top heat_wait time_solution_time				FWHM ( $cm^{-1}$ )			
	$I_{D/G}$	$I_{D'/G}$	$I_{G'/G}$	D	G	D'	G'
650°C_0°C_60s	1.47	0.42	0.87	51	46	27	76
650°C_0°C_60s_acetone_10mins	1.56	0.52	0.94	48	46	25	66
650°C_550°C_60s	1.44	0.24	0.76	57	66	18	81
650°C_550°C_60s_IPA_5mins	1.55	0.31	0.90	57	142	42	82
650°C_650°C_0s	1.42	0.28	0.71	58	57	24	85
650°C_650°C_0s_SPR3012_5mins	1.57	0.35	0.95	52	177	48	75
650°C_650°C_30s	1.48	0.47	0.91	51	39	30	76
650°C_650°C_30s_AZ3027_5mins	1.98	0.72	1.00	57	29	38	81



(a)

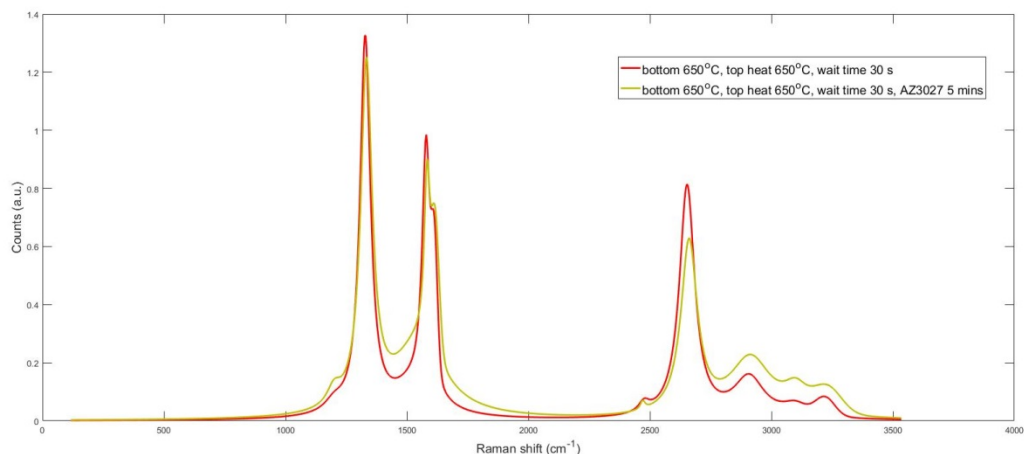


(b)



(c)





(d)

**Figure 6.22** Raman data obtained from CNT bundles in different horizontalization solutions.

## 6.6. Conclusion

In this chapter, we first found that the small difference of bundle dimensions did not influence the CNT growth length. Then we found out that the different location of one wafer can have different real reaction temperature which will influence the length significantly. The center point has a higher temperature than the outer periphery and bottom side has a higher temperature than upside. The Raman inspection also verified this conclusion.

The CNT growing time also shows a relationship with the CNT length. Longer growing time gives longer length, but it does not give more growth after 2 hours for most temperatures. The Raman inspection shows that longer growing time gives CNT better quality with more crystallinity. The temperature is the key element of CNT final length that they are in a parabolic relation between growth-rate and temperature, which means the longest CNT bundles appears at the temperature around 605°C, before the inflection, the temperature shows a positive influence on length and after the inflection, the length will decrease. The Raman still shows the higher temperature gives better quality.

Then we noticed that most of the bundles have already been self-aligned to the left side during the deposition. In this case, it is not useful anymore for rectifying the bundles to right by the same densification and horizontalization recipe that immerses the CNT bundles in acetone and natural drying: the bundle will be aligned in the wrong direction (left). Other methods need to be explored to correct the alignment direction. With un-patterned samples, we verified that the topology is a key element causing this phenomenon. The simulation show that the temperature is asymmetrically distributed, which is likely the cause of different growth rate of CNT on different sides of the bundle. Therefore the side with higher growth



rate will push the bundle towards the side of lower growth rate to generate the self-alignment bundles (in our case predominately to the left). In order to correct the alignment direction, we supplied four samples with 90° rotation clockwise in turn within the CVD chamber, but not many changes have been observed demonstrating that sample orientation within the reactor has no influence. Lower the bottom temperature can make some bundles aligned to the right and so does using the top heater in the reactor. Delaying the insertion time of the CH<sub>4</sub> gas source does not help with alignment correction at all.

For horizontalization optimization, different recipes with angles modification, immersing time, different solutions, immersing or dispensing process are defined. The most useful method is to dispense photoresist to the suspending samples which make the desired aligned direction the same as the dispensing direction of the solution. But of course, this method will give have a negative influence on CNT quality. From the microscopy, it can be seen the bundles unzip in the middle and root. From the Raman inspection, it can also be seen the quality decreases from the increasing of  $I_{D/G}$  and  $I_{D'/G}$ .

## 7. Conclusion and future work

This chapter gives a conclusion of all accomplished results and observations of the previous work. As it is quite new research regarding the materials utilized in MEMS switches and the corresponding processes, there are still many places for optimization and improvements. Future works and recommendations are given at the end of this chapter.

### 7.1. Conclusions for MEMS switches

The commonly used switches as relays and transistors show a limitation in linearity, contact resistance, much loss in the high-frequency domain and so on. So we think of fabricating a MEMS switches which have good performance in high isolation, low contact resistance, and low power consumption on steady-state. As the MEMS switches are normally fragile and easy to be broken at the root, we thought about designing a robust MEMS switches with materials that are robust. The one dimension material CNT is a good choice for this design because the MWCNT have many advantages such as good conductivity, customized shape, nanoscale size, high porosity, robust, and the large surface area to volume ratio is a good prerequisite for coating other materials for more properties optimizing.

During the process, the first challenge is that the old recipe which used to work does not work well in the new design anymore. 650°C can at most give an 80  $\mu\text{m}$  length of CNT bundles after horizontalization. That can because of the buckled shape at the root part which make the bundles 10  $\mu\text{m}$  to 20  $\mu\text{m}$  shorter after horizontalization. The second possible reason is that the multilayer substrate has different heat transfer efficiency as the old samples. And we know the temperature is really the key element of CNT growth rate and final length. After many tests, we found out that 605°C for bottom temperature gives the longest growth length of CNT bundles.

The second challenge is that it is quite unexpected that almost all CNT bundles are left-aligned which is very undesired. We tried to find out what is the reason for this phenomenon. Several tests are made and excluded the causes of gas flow in the reaction chamber. The samples with an unpatterned metal layer show a similar number of left aligned or right aligned CNTs. Also, vertical aligned CNTs are there which is very different from the patterned metal layer that most of the bundles are left-aligned. This can give a clear conclusion that the substrate topology is the main reason for this phenomenon. Besides, the simulation shows that it can be the temperature no uniform distribution on the catalyzer surface which results in the growth rate different. The side with larger growth rate will generate a force to the other side CNTs which finally make the bundles horizontalized during the deposition. As there is an inflection temperature point of CNT length, the assumption that the temperature is the inner cause of CNT self-aligned is also verified that the temperature

higher than 650°C mainly give the left-aligned bundles but the temperature decreases to 615°C or even lower, right-aligned bundles can be observed.

In order to correct this misalignment, many tests are done. Except for the location and the rotation during deposition, the recipes in the aspects of time, top heat, wait time of gas injection are done but none of them showed a good result. Then we consider about the alignment correction in horizontalization. Solutions, immersing time, samples' angles, and disposing of ways have been done. We found out that disposing of the solutions to the samples which is suspended as 45 angles function very well. And the more viscous photoresist seems to work better than less viscous photoresist and IPA or acetone. This can give some dies even 100% alignment correction.

After this, we noticed that after a long time deposition in BM, a thin film Carbons are deposited everywhere on the wafer as well which make the whole surface conductivity. We cannot etch this layer because the etching method will also damage the CNT bundle. Besides, the photoresist which is used for SiC patterning gets harden and not easy to be removed after SiC etching. But we are lucky to find that the coating of SiC can protect the CNT from oxygen plasma etching. Then the thin film carbons will be etched away without damaging the CNT bundles.

The Ti/TiN layer shows a sheet resistance of  $23.96 \pm 0.763 \Omega$ . And the CNT bundles show an average resistance of  $1.671 \pm 0.0716 \text{ K}\Omega$  and  $2.553 \pm 0.354 \text{ K}\Omega$  for 100  $\mu\text{m}$  and 130  $\mu\text{m}$  CNT bundle respectively.

The Raman inspection shows that higher temperature growth recipe will have better quality CNTs. And it also shows that every step after CNT deposition will give a negative influence on the quality and crystalline. And the vapor HF shows the heaviest weight.

However, as time is limited, we still not get the workable devices yet. But once we have figured out these process challenges, the SiC-CNT MEMS switches is still quite promising to be fabricated.

## **7.2. Future work and recommendations**

As we are quite close to making the device fabricating, the next step is very recommended for making it. There are still some process need to be checked out. The first thing is SiC etching. Manual coating after CNT growth showed to give a big influence on bundles' order. Many bundles showed to be zipped during the manual lithography process. SiC etching rate is lower than the PECVD SiC etching. So longer time etching is very recommended. Also, HF etching is another question. Proper etch time still needs to be figured out. Shorter etching time will not etch the silicon oxide layer away which means the cantilever cannot be released and the contact pads cannot be contacted as well. But too much etching time will probably

etch the oxide layer between the third metal layer and a first metal layer. If these two layers are connected, it will be impossible to generate an electrostatic force between the two electrodes.

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## Appendix A

Structure dimensions of CNT bundles in the solution test

### **A** (first quarter (Q1) of the wafer)

ArrayA

Symbol	Cell	Cell size	Array	Dx	Dy
Full Circle	a.1	15x45	300x4	100	215
Full Circle	a.2	15x65	300x4	100	215
Full Circle	a.3	15x85	300x4	100	215

ArrayB

Symbol	Cell	Cell size	Array	Dx	Dy
Empty circle	b.1	20x60	300x4	100	220
Empty circle	b.2	20x80	300x4	100	220
Empty circle	b.3	20x100	250x4	120	220

ArrayC

Symbol	Cell	Cell size	Array	Dx	Dy
Triangle	c.1	25x75	250x4	120	225
Triangle	c.2	25x105	200x4	150	225
Triangle	c.3	25x135	200x4	150	225

ArrayD

Symbol	Cell	Cell size	Array	Dx	Dy
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Square	d.1	30x90	230x4	130	230
Square	d.2	30x120	150x4	200	230
Square	d.3	30x150	150x4	200	230

#### ArrayE

Symbol	Cell	Cell size	Array	Dx	Dy
Empty square	e.1	35x105	127x4	235	235
Empty square	e.2	35x155	127x4	235	235
Empty square	e.3	35x205	127x4	235	235

#### ArrayF

Symbol	Cell	Cell size	Array	Dx	Dy
Cross	f.1	40x120	54x4	550	240
Cross	f.2	40x300	54x4	550	240
Cross	f.3	40x500	54x4	550	240

W/L = 10

#### ArrayG

Symbol	Cell	Cell size	Array	Dx	Dy
Triangle	g.1	3x30	600x4	50	203
Triangle	g.2	4x40	600x4	50	203

Triangle	g.3	5x50	428x4	70	203
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#### ArrayH

Symbol	Cell	Cell size	Array	Dx	Dy
Triangle	H.1	6x60	428x4	70	206
Triangle	H.2	7x70	300x4	100	207
Triangle	H.3	8x80	300x4	100	208

IslandA.1: 20 rows of size 10um X 2cm distance 200um

IslandA.2: 20 rows of size 10um X 1cm distance 200um

## **B (second quarter wafer)**

#### Array1 (partendo dal basso)

Symbol	Cell	Cell size	Array	Dx	Dy
full circle	1.1	3x15	1000x4	30	203
full circle	1.2	3x20	860x4	35	203
Full circle	1.3	3x25	750x4	40	203

#### Array2

Symbol	Cell	Cell size	Array	Dx	Dy
Empty circle	2.1	4x15	1000x4	30	204
Empty circle	2.2	4x20	860x4	35	204

Empty circle	2.3	4x25	750x4	40	204
--------------	-----	------	-------	----	-----

#### Array3

Symbol	Cell	Cell size	Array	Dx	Dy
triangle	3.1	5x15	1000x4	30	205
triangle	3.2	5x20	860x4	35	205
triangle	3.3	5x25	750x4	40	205

#### Array4

Symbol	Cell	Cell size	Array	Dx	Dy
square	4.1	6x20	860x4	35	206
square	4.2	6x25	750x4	40	206
square	4.3	6x30	666x4	45	206

#### Array5

Symbol	Cell	Cell size	Array	Dx	Dy
Empty square	5.1	7x20	860x4	35	207
Empty square	5.2	7x25	750x4	40	207
Empty square	5.3	7x30	666x4	45	207

#### Array6

Symbol	Cell	Cell size	Array	Dx	Dy
cross	6.1	8x20	860x4	35	208

cross	6.2	8x25	750x4	40	208
cross	6.3	8x30	666x4	45	208

#### Array7

Symbol	Cell	Cell size	Array	Dx	Dy
triangle	7.1	9x30	666x4	45	209
triangle	7.2	9x35	600x4	50	209
triangle	7.3	9x40	545x4	55	209

#### Array8

Symbol	Cell	Cell size	Array	Dx	Dy
triangle	8.1	10x30	666x4	45	210
triangle	8.2	10x35	600x4	50	210
triangle	8.3	10x40	545x4	55	210

IslandB.1: 20 rows of size 30um X 2cm distance 300um

IslandB.2: 20 rows of size 30um X 1cm distance 300um

### **C (Q3 wafer)**

SquareC.1: 11x11 array. Each array made of 4 blocks of size 7x30

SquareC.2: 12 columns. Each column is constituted by 50 blocks of size 7x(30+20\*cost)  
distance 200um

Column	size
A	7x30

B	7x50
C	7x70
D	7x90
E	7x110
F	7x130
G	7x150
H	7x170
I	7x190
L	7x210
M	7x230
N	7x250

SquareC.3: 15 columns. Each column made by 50 blocks of size 10x(50+50\*cost)  
distance 200um

Column	size
A	10x50
B	10x100
C	10x150
D	10x200
E	10x250
F	10x300
G	10x350

H	10x400
I	10x450
L	10x500
M	10x550
N	10x600
O	10x650
P	10x700
Q	10x750
R	10x800

SquareC.4: 10x8 blocks of size 7x30

## **D (quarto quadrante del wafer)**

SquareD.1: 11x11 array. Each array made by 3 blocks of size 7x30

SquareD.2: 12 columns. Each column made by 33 blocks of size 7x(30+20\*cost) distance 300um

Column	size
A	7x30
B	7x50
C	7x70
D	7x90
E	7x110

F	7x130
G	7x150
H	7x170
I	7x190
L	7x210
M	7x230
N	7x250

SquareD.3: 15 columns. Each column is made by 50 blocks of size 10x(50+50\*cost)  
distance 300um

Column	size
A	10x50
B	10x100
C	10x150
D	10x200
E	10x250
F	10x300
G	10x350
H	10x400
I	10x450
L	10x500
M	10x550



N	10x600
O	10x650
P	10x700
Q	10x750
R	10x800

SquareD.4: 10x8 blocks of size 10x500

## Appendix B

Structure dimensions of CNT bundles in the MEMS switches mask design

A First Structure of Figure 4.4 (b)

Dimension specifications (from left to right)	CNT bundles dimension ( $\mu\text{m}$ )	Bottom electrode dimension ( $\mu\text{m}$ )	Contact probe dimension ( $\mu\text{m}$ )
1	2x10x100	2x10	100x100
2	2x10x130	2x10	100x100
3	2x10x160	2x10	100x100
4	2x15x100	2x15	100x100
5	2x15x130	2x15	100x100
6	2x15x160	2x15	100x100
7	2x20x100	2x20	100x100
8	2x20x130	2x20	100x100
9	3x15x100	3x15	100x100
10	3x15x130	3x15	100x100
11	3x20x100	3x20	100x100
12	3x20x130	3x20	100x100
13	3x25x100	3x25	100x100
14	3x25x130	3x25	100x100
15	4x15x100	4x15	100x100
16	4x15x130	4x15	100x100
17	4x20x100	4x20	100x100
18	4x20x130	4x20	100x100
19	4x25x100	4x25	100x100
20	4x25x130	4x25	100x100

B First Structure of Figure 4.4 (c)

Dimension specifications (from left to right)	CNT bundles dimension ( $\mu\text{m}$ )	Bottom electrode dimension ( $\mu\text{m}$ )	Contact probe dimension ( $\mu\text{m}$ )
1	2x15x100	2x15	100x100
2	2x15x130	2x15	100x100
3	2x20x100	2x20	100x100
4	2x20x130	2x20	100x100
5	3x15x100	3x15	100x100
6	3x15x130	3x15	100x100
7	3x20x100	3x20	100x100
8	3x20x130	3x20	100x100
9	4x15x100	4x15	100x100
10	4x15x130	4x15	100x100
11	4x20x100	4x20	100x100
12	4x20x130	4x20	100x100
13	4x25x100	4x25	100x100
14	4x25x130	4x25	100x100

C First Structure of Figure 4.4 (d)

Dimension specifications (from left to right)	CNT bundles dimension ( $\mu\text{m}$ )	Bottom electrode dimension ( $\mu\text{m}$ )	Contact probe dimension ( $\mu\text{m}$ )
1	2x10x100	2x10	100x100
2	2x10x130	2x10	100x100

3	2x10x160	2x10	100x100
4	2x15x100	2x15	100x100
5	2x15x130	2x15	100x100
6	2x15x160	2x15	100x100
7	2x20x100	2x20	100x100
8	2x20x130	2x20	100x100
9	3x15x100	3x15	100x100
10	3x15x130	3x15	100x100
11	3x20x100	3x20	100x100
12	3x20x130	3x20	100x100
13	3x25x100	3x25	100x100
14	3x25x130	3x25	100x100
15	4x15x100	4x15	100x100
16	4x15x130	4x15	100x100
17	4x20x100	4x20	100x100
18	4x20x130	4x20	100x100
19	4x25x100	4x25	100x100
20	4x25x130	4x25	100x100

D First Structure of Figure 4.4 (e)

Dimension specifications (from left to right)	CNT bundles dimension ( $\mu\text{m}$ )	Bottom electrode dimension ( $\mu\text{m}$ )	Contact probe dimension ( $\mu\text{m}$ )
---	---	--	---

1	2x15x100	2x15	100x100
2	2x15x130	2x15	100x100
3	2x20x100	2x20	100x100
4	2x20x130	2x20	100x100
5	3x15x100	3x15	100x100
6	3x15x130	3x15	100x100
7	3x20x100	3x20	100x100
8	3x20x130	3x20	100x100
9	4x15x100	4x15	100x100
10	4x15x130	4x15	100x100
11	4x20x100	4x20	100x100
12	4x20x130	4x20	100x100

E First Structure of Figure 4.4 (f)

Dimension specifications (from left to right)	CNT bundles dimension ( $\mu\text{m}$ )	Bottom electrode dimension ( $\mu\text{m}$ )	Contact probe dimension ( $\mu\text{m}$ )
1	2x15x100	2x15	100x100
2	2x15x130	2x15	100x100
3	2x20x100	2x20	100x100
4	2x20x130	2x20	100x100
5	3x15x100	3x15	100x100
6	3x15x130	3x15	100x100

7	3x20x100	3x20	100x100
8	3x20x130	3x20	100x100
9	4x15x100	4x15	100x100
10	4x15x130	4x15	100x100
11	4x20x100	4x20	100x100
12	4x20x130	4x20	100x100

F Test Structure of Figure 7

Dimension specifications (from left to right)	CNT bundles dimension (μm)	Contact probe dimension (μm)
1	2x10	100x100
2	2.5x10	100x100
3	3x10	100x100
4	3.5x10	100x100
5	4x10	100x100
6	2x15	100x100
7	2.5x15	100x100
8	3x15	100x100
9	3.5x15	100x100
10	4x20	100x100
11	2x20	100x100
12	2.5x20	100x100
13	3x20	100x100

14	3.5x20	100x100
15	4x20	100x100
16	2x20	100x100
17	2.5x20	100x100
18	3x20	100x100
19	3.5x20	100x100
20	4x20	100x100

G Test Structure of Figure 8

Dimension specifications (from left to right)	CNT bundles dimension ( $\mu\text{m}$ )	Contact probe dimension ( $\mu\text{m}$ )
1	2x15x100	100x100
2	2x15x130	100x100
3	2x20x100	100x100
4	2x20x130	100x100
5	3x15x100	100x100
6	3x15x130	100x100
7	3x20x100	100x100
8	3x20x130	100x100
9	3x25x100	100x100
10	3x25x130	100x100
11	4x15x100	100x100

12	4x15x130	100x100
13	4x20x100	100x100
14	4x20x130	100x100
15	4x25x100	100x100
16	4x25x130	100x100

H Test Structure of Figure 4.9

Dimension specifications (from left to right)	Mask layer	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Contact probe dimension ( $\mu\text{m}$ )
1	First	200	5	100x100
2		200	10	100x100
3		200	2	100x100
4	Second	200	5	100x100
5		200	10	100x100
6		200	2	100x100
7	Third	200	5	100x100
8		200	10	100x100
9		200	2	100x100

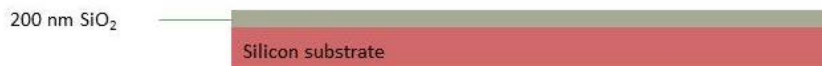


## Appendix C

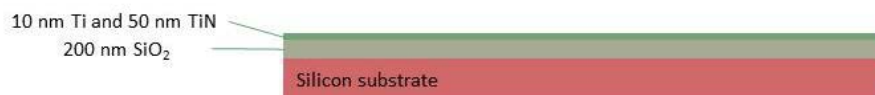
### Process illustrations



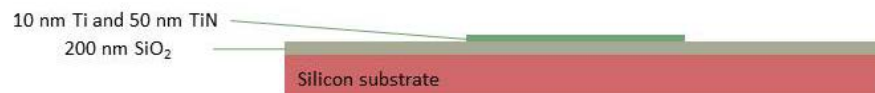
(a) Begins with p-type silicon substrate.



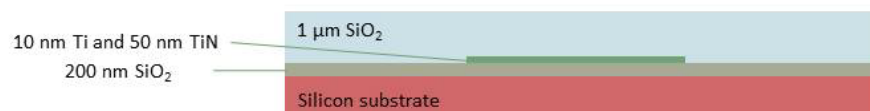
(b) Thermal oxidation in furnace



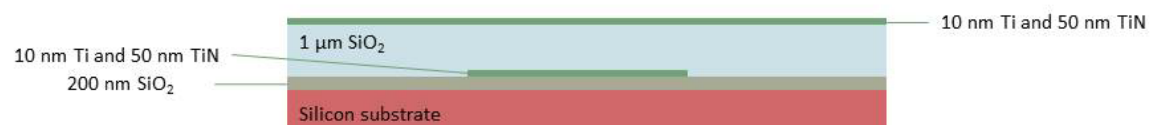
(c) First metal layer of 10nm/50nm Ti/TiN



(d) Patterned first metal layer



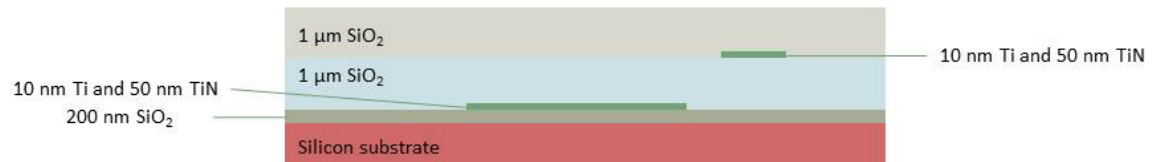
(e) Oxide layer to make contact layer higher than bottom electrode layer



(f) Second metal layer of 10nm/50nm Ti/TiN



(g) Patterned second layer



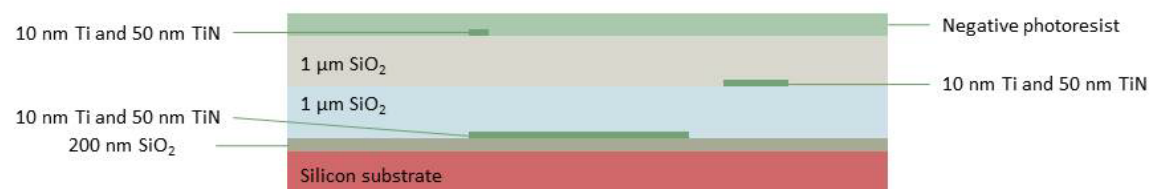
(h) Oxide layer to make cantilever layer higher than contact layer



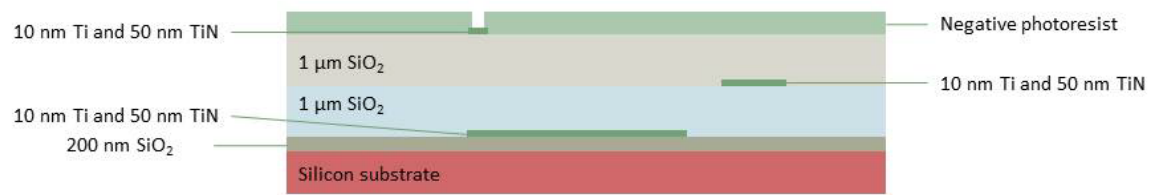
(i) Third metal layer of 10nm/50nm Ti/TiN



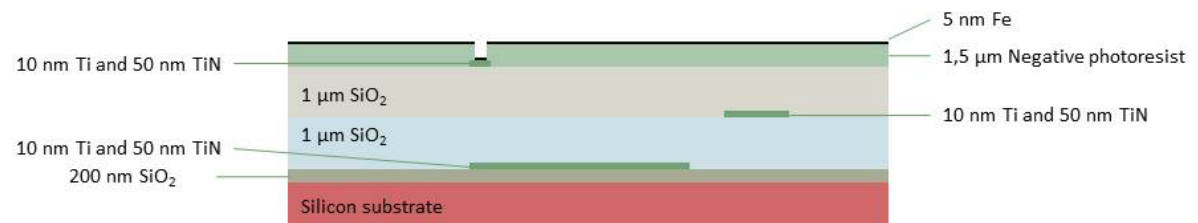
(j) Patterned third layer



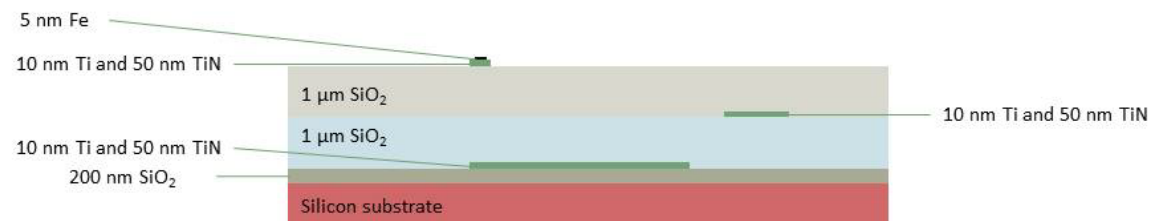
(k) Negative photoresist for Fe lift-off



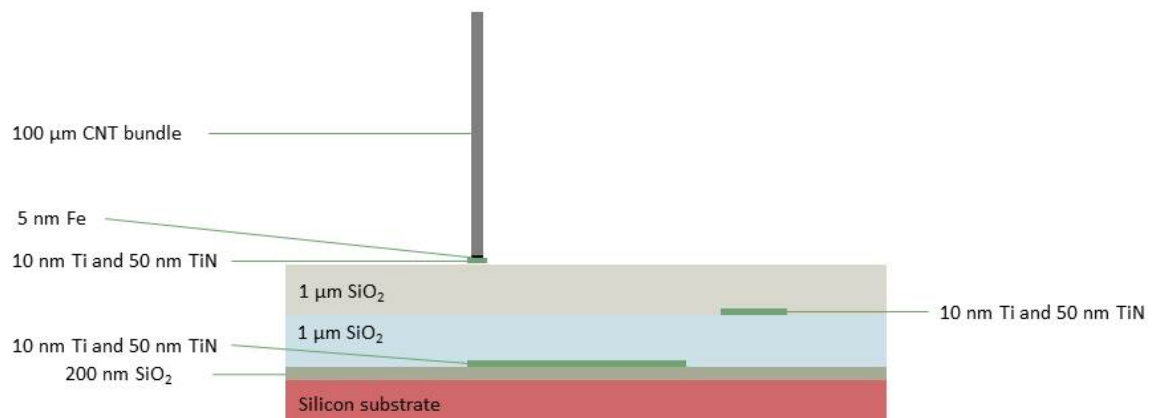
(l) Negative photoresist patterning for Fe lift-off



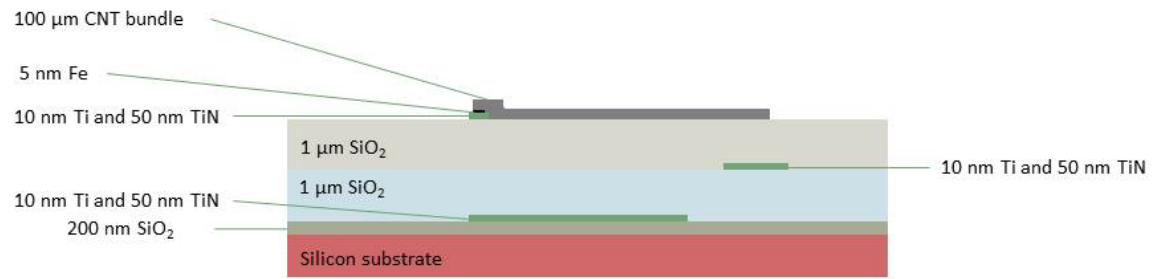
(m) Fe evaporation



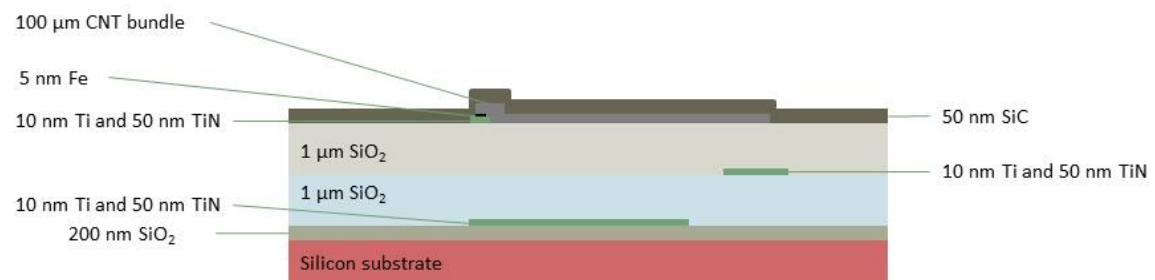
(n) NMP cleaning



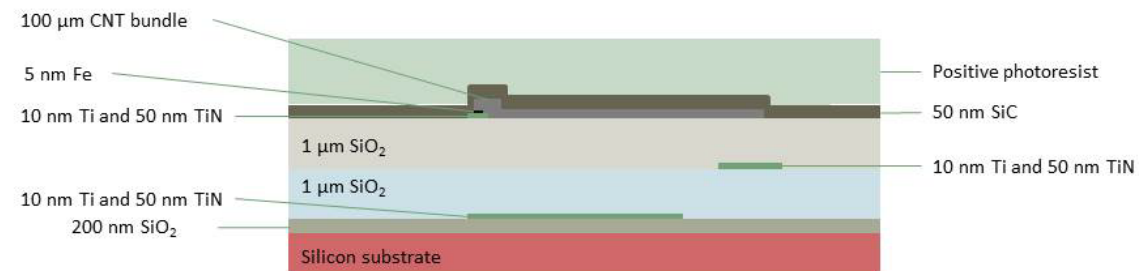
(o) CNT growth



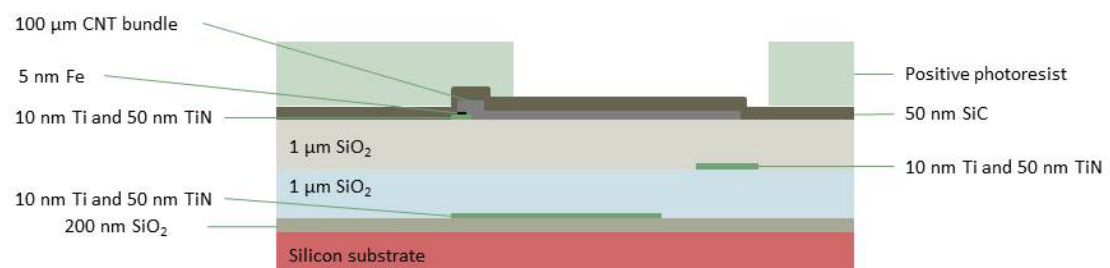
(p) CNT bundle horizontalization



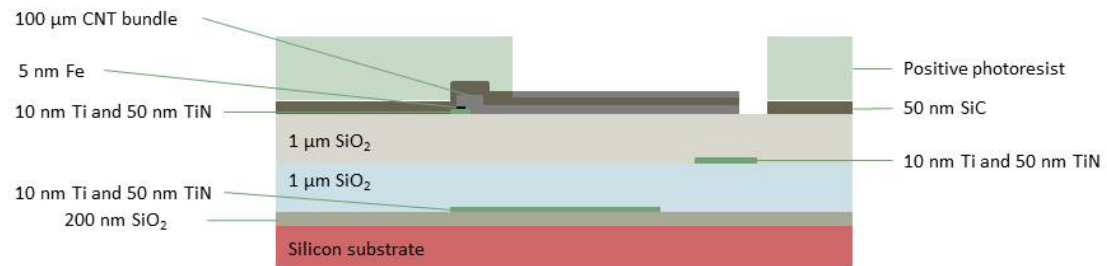
(q) SiC deposition



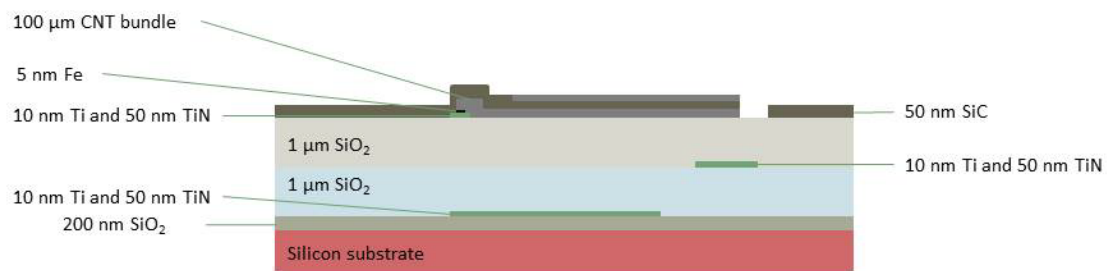
(r) Positive photoresist for SiC patterning



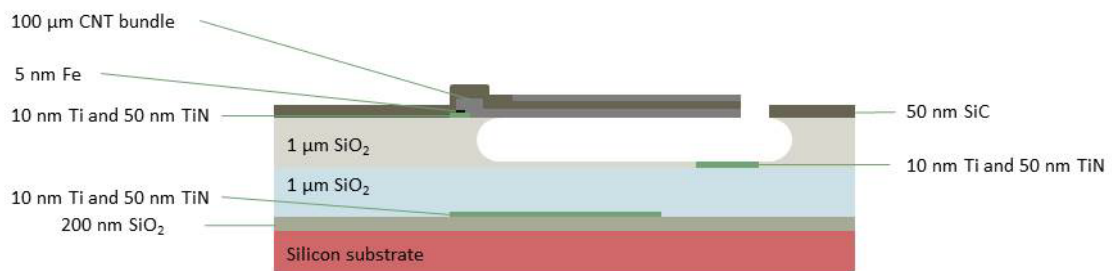
(s) Patterned positive photoresist for SiC patterning



(t) SiC etching



(u) Cleaning before vapour HF etching



(v) Vapour HF etching for releasing cantilevers

Figure: Process flowcharts of SiC-CNT MEMS switch.

## Appendix D

Process Flowchart



# CNT-SiC electrostatic micro-switches

## Flow chart

Version

30 August 2018

Ziqiao Huang

EC: EC2299

Process engineer: Ziqiao Huang

Start: 04/09/2018

Contamination: Yes

Labs: CR100, CR10000, SAL, MEMS

**EKL(Else Kooi Laboratory)**

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### Detailed information about possible contamination:

**Place/Clean Rooms used in process:**

**Write the sequence of used labs from start to finish.**

**Which (Non-standard) materials or process steps**

**What kind of process or machine was used?**

**The other materials that wafers contain that are also processed on this machine**

Lab/Clean room	(Non-standard) material/ process steps	Process/Machine/	Other materials used in machine
CR100	non	non	non
CR10000	Yes, CNT	BlackMagic	Fe, Co, Ni, Pt
CR10000	Yes, Fe	CHA	Pt, Ta, Mo, Ni, Co, Fe, Pd
CR10000	Yes, SiC in F3	F3	Pt

**If other labs are used:**

**Write the steps number: Possible contamination issues/materials.**

None

**If there are non-standard processing steps in a standard process: Write down the steps number, the material and machine that is used.**

Step number	Material	Machine/Tool
37	Fe	CHA
41	CNT	Black Magic
44	SiC	F3
54	Etch	HF vapour etch

**After the graphene growth in Black magic, the subsequent litho steps will be manually performed using contaminated chucks.**

Use 9 **single side polished** test wafers, with the following specifications:

Type: p-type, boron

Orientation: 1-0-0, 0 deg off orientation

Resistivity: 2-5  $\Omega\text{cm}$

Thickness:  $525 \pm 15 \mu\text{m}$

Diameter:  $100.0 \pm 0.2 \text{ mm}$

## **Si Substrate with Alignment Markers**

### **1. COATING AND BAKING**

**Equipment:** EVG 120 Coater/developer

**Recipe:** Use coating 1-Co-3012-zero layer (resist thickness:  $1.400 \mu\text{m}$ ).

**Note:**

Follow the instructions specified for this equipment;

The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas;

Spin coating with Shipley SPR3012 positive photoresist, and a soft bake at  $95^\circ\text{C}$  for 90 seconds.

Always check the temperature of the hotplate and the relative humidity ( $48 \pm 2 \%$ ) in the room first.

### **2. ALIGNMENT AND EXPOSURE**

**Equipment:** ASML PAS 5500/80 automatic waferstepper

**Recipe:** Use COMURK (common align markers) mask, the correct litho job : Litho/ZEFWAM and the correct exposure energy ( $120 \text{ mJ/cm}^2$ ).

**Note:** 14 markers for stepper and two blocks for contact aligner (FWAMs)

### **3. DEVELOPMENT**

**Equipment:** EVG 120



**Recipe:**1- Dev-SP(Dev - Single Puddle)

**Note:**

EVG 120 wafer track to develop the wafers, and follow the instructions specified for this equipment;

The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 90 seconds;

#### **4. WAFER NUMBERING**

Use the glass scribe in the litho room to write the run number and wafer number manually in the resist close to the primary flat.

#### **5. INSPECTION: LINEWIDTH**

**Equipment:** microscope

Visually inspect the wafers through a microscope, and check the linewidth.

**Note:** No resist residues are allowed.

#### **6. PLASMA ETCHING OF ALIGNMENT MARKS**

**Equipment:** Trikon Omega 201 plasma etcher.

**Recipe:** Use sequence URK\_NPD and set the platen temperature to 20 °C to etch 120nm deep ASML URK's into the silicon.

**Note:** The process conditions of the etch program may not be changed!

If not possible to do the next step after cleaning(for example: sputtering) at the same day, always stop before cleaning step to save time.

#### **7. CLEANING PROCEDURE: TEPLA + HNO3 100% and 65%**

Plasma strip Use the **Tepla plasma system** to remove the photoresist in an oxygen plasma;

Use **program 1**.

Cleaning 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature.

Use wet bench "HNO3 (100%)" and the carrier with the **White** dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 M ☐.

Cleaning 10 minutes in concentrated nitric acid (Merck: HNO<sub>3</sub> 65% selectipur) at 110 °C.

Use wet bench "HNO<sub>3</sub> (65%)" and the carrier with the **White** dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 M ☐.

Drying Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a **red dot**.

**Note:** If put too many wafers one time, the plasma might not be able to get ignited. Put one wafer after a vacancy. Leave the first three vacancy and last three vacancy empty.

Oxidation: SiO<sub>2</sub>

## 8. 200NM OXIDATION FOR ALL 6 WAFERS

**Equipment:** Furnace C1, D1, B4

**Recipe:** Using recipe WET1000, time **24 min (the time need to be edited in the recipe)**

**Function:** Thermal wet oxidation

**Note:** This recipe does not boat out, which is nice for overnight deposition. Common furnace, gas come from right side (side of furnace), so the wafer's front side should face to right.

## Bottom Electrodes\_ Electrostatic Attraction Supplier

Sputtering: Ti/TiN Stack (10/50 nm)

## 9. TI/TIN DEPOSITION

**Equipment:** TRIKON SIGMA sputter coater

**Recipe:**

The first wafer need to use the recipe **\_Trgtch\_Ti\_350C**. Use recipe **Ti10\_TiN50\_350C (DEP\_B)**, Use **Ti\_in\_Between\_350C** module for target clean after each TiN reactive sputtering.

**Note:**

350 °C to sputter a 0.01 µm thick layer of Ti, followed by reactively sputtering a 0.050 µm thick layer of TiN (to prevent oxidation of Ti). Add dummy wafers between the process wafers as required. Temperature = 350 °C.

The target must exist of 100% Ti.

**Note:**        **Front side (last wafer)** [ ←←←← ] **Back side (first wafer)**

TiN Patterning

## 10. COATING AND BAKING

**Equipment:** EVG 120 Coater/developer

**Recipe:** Use Coating Program “1-Co-3012-1.4um”

**Note:**

The process consists of a treatment with HMDS (hexamethyldisilazane; hydrophilic) vapour with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95°C for 90 seconds (manual for 1 min);

Always check the temperature of the hotplate and the relative humidity ( $48 \pm 2 \%$ ) in the room first;

## 11. ALIGNMENT AND EXPOSURE

**Equipment:** ASML PAS 5500/80 automatic waferstepper

Follow the operating instructions from the manual when using this machine.

**Mask:** mask1, ID: 2x2

**Job:** diesize\_10mm/DIE10x10\_4IMG, layer ID: image 1

**Exposure energy:** 140 mJ/cm<sup>2</sup>

## 12. DEVELOPMENT

**Equipment:** EVG 120 developer

**Recipe:** Dev - SP.

**Note:**

The process consists of a post-exposure bake at 115 °C for 90 seconds (manual for 1 min), followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 90 seconds.

Always check the temperature of the hotplates first.

## 13. INSPECTION

Inspection of wafers after development. Make sure all lines are open.

#### 14. PATTERNING OF Ti/TiN(10/50nm)

**Equipment:** Omega

**Recipe:** tintisvo@25°C, each time of step 1 should be set to approximately 25 sec(this might be changed)

**If software problems happen, might try Ctrl + P to resume. If still does not work, contact Mario.**

#### 15. CLEANING LINE FOR METALS: TEPLA + HNO3 100%

Plasma strip Use the **Tepla plasma system** to remove the photoresist in an oxygen plasma;

Use **program 1**.

Cleaning 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature.

Use wet bench "HNO3 (100%) Metals" and the carrier with the **Black/Yellow** dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 M ☐.

Drying Use the Semitool "rinser/dryer for metals" with the standard program, and the white carrier with a **black dot**.

### *Deposition 1um SiO2(PECVD)*

#### 16. DEPOSITION 1UM(variable) SiO2

**Equipment:** Novellus Concept 1

**Recipe:** xxxnmTEOS

**Thickness:** 1um

**Note:** This time is only for roughly check. Please refer to the latest record.

Approximately Time /s	Thickness /nm
16.7/17.6	483/510

<b>36.5</b>	<b>1000</b>
<b>54.6</b>	<b>1500</b>
<b>74</b>	<b>2030</b>

## Bottom Electrodes\_ Contact Pad

Sputtering: Ti/TiN Stack (10/50 nm)

### 17. TI/TIN DEPOSITION

**Equipment:** TRIKON SIGMA sputter coater

**Recipe:** Use recipe **Ti10nm\_TiN50nm\_350C (DEP\_B)**, Use **Ti\_inbetween** module for target clean after each TiN reactive sputtering.

#### **Note:**

350 °C to sputter a 0.01 µm thick layer of Ti, followed by reactively sputtering a 0.050 µm thick layer of TiN (to prevent oxidation of Ti). Add dummy wafers between the process wafers as required. Temperature = 350 °C.

The target must exist of 100% Ti.

## *TiN Patterning*

### 18. COATING AND BAKING

**Equipment:** EVG 120 Coater/developer

**Recipe:** Use Coating Program “3012-1.4µm”

#### **Note:**

The process consists of a treatment with HMDS (hexamethyldisilazane, hydrophilic) vapour with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95 °C for 90 seconds;

Always check the temperature of the hotplate and the relative humidity ( $48 \pm 2$  %) in the room first;

## 19. ALIGNMENT AND EXPOSURE

**Equipment:** ASML PAS 5500/80 automatic waferstepper

**Mask:** mask2, ID: 2x2

**Job:** 10mm\_diesize/DIE10x10\_4IMGS, layer ID: image 2

**Exposure energy:** 140mj/cm<sup>2</sup>

## 20. DEVELOPMENT

**Equipment:** EVG 120 developer

**Recipe:** Dev - SP

### **Note:**

The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 90 seconds.

Always check the temperature of the hotplates first.

## 21. INSPECTION

Inspection of wafers after development. Make sure all lines are open.

## 22. PATTERNING OF Ti/TiN(10/50nm)

**Equipment:** Omega

**Recipe:** tintisvo@25°C, each time of step 1 should be set to approximately 25 secs (this might be changed)

**Note:** If cannot find the recipe, should go to the 'Process' level. Keyword: PROcESS(except for 'c', all capital letters)

## 23. CLEANING LINE FOR METALS: TEPLA + HNO3 100%

Plasma strip Use the **Tepla plasma system** to remove the photoresist in an oxygen plasma;

Use **program 1**.

Cleaning 10 minutes in fuming nitric acid (Merck: HNO<sub>3</sub> 100% selectipur) at ambient temperature.

Use wet bench "HNO<sub>3</sub> (100%) for Metals" and the carrier with the **red/yellow** dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 M ☐.

Drying Use the Semitool "rinser/dryer for metals" with the standard program, and the white carrier with a **black dot**.

## *Deposition 0.5um SiO<sub>2</sub>(PECVD)*

24. DEPOSITION 0.5UM SiO<sub>2</sub>

**Equipment:** Novellus Concept 1

**Recipe:** xxxnmstdteos

**Thickness:** 0.5um

## Cantilever Electrodes

Sputtering: Ti/TiN Stack (10/50 nm)

### 25. TI/TIN DEPOSITION

**Equipment:** TRIKON SIGMA sputter coater

**Recipe:**

Use recipe **Ti\_10nm\_TiN\_50nm\_350C (DEP\_B)**, Use **Ti\_inbetween** module for target clean after each TiN reactive sputtering.

**Note:**

350 °C to sputter a 0.01 µm thick layer of Ti, followed by reactively sputtering a 0.050 µm thick layer of TiN (to prevent oxidation of Ti). Add dummy wafers between the process wafers as required. Temperature = 350 °C.

The target must exist of 100% Ti.

TiN Patterning (cantilever electrode)

### 26. COATING AND BAKING

**Equipment:** EVG 120 Coater/developer

**Recipe:** Use Coating Program “3012-1.4um”

**Note:**

The process consists of a treatment with HMDS (hexamethyldisilazane; hydrophilic) vapour with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95 °C for 90 seconds;

Always check the temperature of the hotplate and the relative humidity ( $48 \pm 2$  %) in the room first;

## 27. ALIGNMENT AND EXPOSURE

**Equipment:** ASML PAS 5500/80 automatic waferstepper

**Mask:** mask3, ID: 2x2

**Job:** 10mm\_diesize/DIE10x10\_4IMGS, layer ID: image 3

**Exposure energy:** 140mj/cm<sup>2</sup>

## 28. DEVELOPMENT

**Equipment:** EVG 120 developer

**Recipe:** Dev - SP.

**Note:**

The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 90 seconds.

Always check the temperature of the hotplates first.

## 29. INSPECTION

Inspection of wafers after development. Make sure all lines are open.

## 30. PATTERNING OF Ti/TiN(10/50nm)

**Equipment:** Omega

**Recipe:** tintisvo@25°C, each time of step 1 should be set to approximately **25 sec (the time need to be edited)**.



### 31. CLEANING LINE FOR METALS

Remove the resist after etching in fresh NMP @70°C for about 10 mins, use non-contaminated glass ware.

**Note: A tepla strip cannot be used as it will oxidize the TiN and negatively affect the CNT growth.**

Use wet bench “HNO<sub>3</sub>(100%) for Green Metals” and the carrier with the **red/yellow** dot.

QDR rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 M?

Drying use the Semitool “rinser/dryer” with the standard program, and the white carrier with a black dot (green metal).

## *Patterning Resist for Fe Lift-off*

### 32. COATING AND BAKING

**Equipment:** EVG 120 Coater/developer

**Recipe:** Co-Nlof-1.5um, no EBR

**1.5um** thick resist layer for lift-off

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment;

The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with AZ\_Nlof2020 negative photoresist (check the mask bright field or dark field, if bright field, use positive resist. Otherwise, use negative resist). And a soft bake at 95 °C for 90 seconds (manual for 1 min);

Always check the temperature of the hotplate and the relative humidity ( $48 \pm 2$  %) in the room first;

### 33. ALIGNMENT AND EXPOSURE

**Equipment:** ASML PAS 5500/80 automatic waferstepper

**Mask:** mask 4, ID: 2x2

**Job:** 10mm\_diesize/DIE10x10\_4IMGS, layer ID: image 4

**Exposure energy:** 55 mJ/cm<sup>2</sup>

#### 34. ALIGNMENT AND EXPOSURE FOR OUTER FRAME

**Equipment:** ASML PAS 5500/80 automatic waferstepper

**Box:** 262, open 10x10

**Mask:** name mask 'A1',

**Job:** 10mm\_diesize/gloa\_edge(full), layer ID: image 2

**Exposure energy:** 55 mJ/cm<sup>2</sup>

#### 35. DEVELOPMENT

**Equipment:** EVG 120 developer

**Recipe:**

First perform a cross-link bake: Only X-link-bake

Use development program: 1-Dev-DP2- **no** PEB(2\*39s)

**Note:** The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 90 seconds.

Always check the temperature of the hotplates first.

We don't use Dev-SP-no PEB(1\*57s)

#### 36. INSPECTION

Inspection of wafers after development. Make sure all lines are open.

*Evaporation: 5 nm Fe (red metal, bad bad) Catalyst*

#### 37. CATALYST DEPOSITION

Use the CHA Solution e-beam evaporator to deposit 5 nm Fe directly on the TiN surface.

Use dedicated contaminated shields!

### *Lift-off: NMP(N-Methyl-2-pyrrolidone) for Fe*

put wafers in **white blister** with Fe written on it after evaporation.

#### 38. LIFT-OFF @ SAL

Perform lift-off procedure with NMP(*N*-Methyl-2-pyrrolidone) at **70°C** for **8mins**;

If necessary, use a Q-tip to remove residues; Be patient not to scratch;

Change the liquid after a few (5-6) wafers if required.

**Note:** use only the contaminated glassware.

#### 39. RINSE & DRY @ SAL

Rinse the wafers in DI and dry using manual dryer with **special Cu chuck**.

#### 40. INSPECTION @ SALAB

Visually inspect the wafers through a microscope, check if catalyst layer remained on surface.

Put paper under wafer and throw away paper after use.

## CNT Growth

#### 41. CNT GROWTH

Use the AIXTRON BlackMagic Pro to grow CNTs using LPCVD at 600°C.

Use recipe: lpcvd\_v3\_600\_vartime, with time set to 1800 sec which should give 100um.

Change time to 5400s/7200s.

Recipe includes an activation step (3 min) in H<sub>2</sub> environment at 600 °C, followed by CNT growth using 700/50 sccm H<sub>2</sub>/C<sub>2</sub>H<sub>2</sub> at 80 mbar and 600°C for 60 minutes. Check growth rate with 1 test wafer/piece of wafer

**Note:** Use contaminated reactor interior!

1800s	100 $\mu\text{m}$
3600s	128 $\pm$ 5 $\mu\text{m}$
5400s	128 $\pm$ 5 $\mu\text{m}$
7200s	128 $\pm$ 5 $\mu\text{m}$

#### 42. SEM OF CNT HEIGHT

**Equipment:** SEM

Make some SEM photos of the top view, side view and cross-section view of the CNTs.

**Note:** Use a **clean** carrier wafer **with carbon tape**, or the contaminated samples holder.

## CNT Horizontal

#### 43. CNT HORIZONTAL TEST

**Location:** SALAB

**Equipment:** tissue, contaminated container, timer, safety glasses

**Recipe:** dice wafer into pieces, put it into IPA, Acetone, Methanol, Ethanol in 90 degrees for 1'30"; take out and dry in 90 degrees for 5mins. Record and mark tiles.

## SiC Coating

#### 44. LPCVD SiC COATING

**Location:** class 10000

**Equipment:** Furnace F3

**Recipe:** to be determined

Thickness: 10-15nm (27-37min, variable)

**Note:** use clean Si wafer as carrier for pieces. The precursor gasses were acetylene ( $\text{C}_2\text{H}_2$ ) and dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) diluted in 5% hydrogen ( $\text{H}_2$ ) and the deposition temperature and pressure were fixed at 760 °C and 0.8 mbar, respectively. The average deposition rate is 5 Å min<sup>-1</sup>, with an incubation time of around 7 mins.

## *SiC Etching (Need to be re-checked from here)*

### 45. COATING AND BAKING

**Location:** CR100, polymer lab

**Equipment:** spinner

**Coating:** SPR3012

**Remove edge bead:** Acetone

### 46. SOFT BAKE

**Recipe:** soft bake at 110 °C for 60 seconds (Henk did 30 sec)

### 47. ALIGNMENT AND EXPOSURE

**Equipment:** EVG Contact Aligner (power density: 5 mWatt/cm<sup>2</sup> ± 0.5 mWatt/cm<sup>2</sup>), 15 sec

**Mask:** FWAM mask

### 48. POST-EXPOSURE BAKE

**Recipe:** 110 °C for 60 seconds, contact mode

### 49. DEVELOPMENT

**Equipment:** Manual develop

**Recipe:** Shipley MF322 developer 120 (Henk did 60 sec), single pundle

### 50. Rinse

**Recipe:** IPA and water for 5 mins

### 51. INSPECTION

Inspection of pieces after development. Make sure all lines are open.

### 52. SiC ETCHING

**Location:** Kavli Lab

**Equipment:** Actal

**Recipe:** etch rate PECVD SiC 55 nm/min

### 53. CLEANING

**Location:** CR100

**Recipe:** Acetone or oxygen plasma can be used if the photoresist became harden.

## *SiO<sub>2</sub> HF Etching*

### 54. HF ETCHING

**Location:** CR100

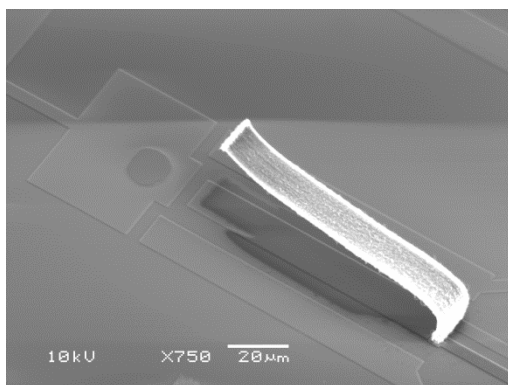
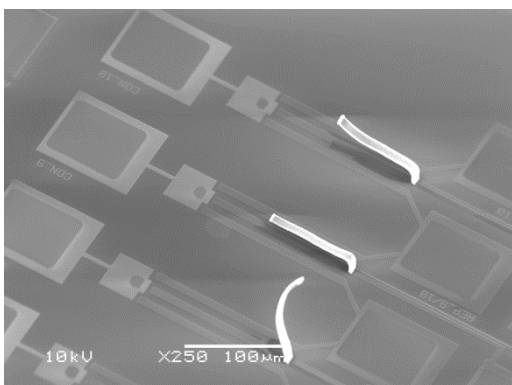
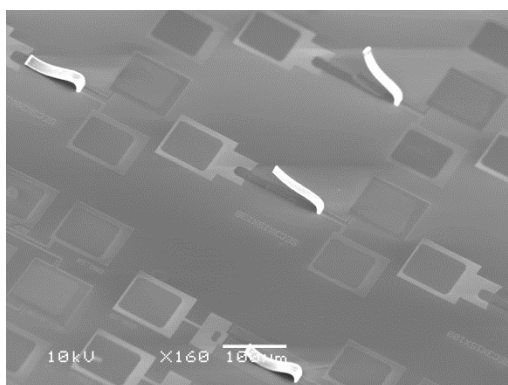
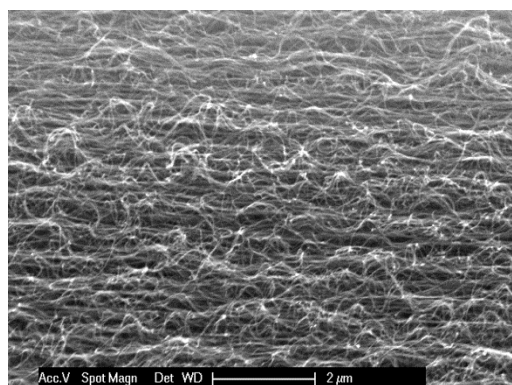
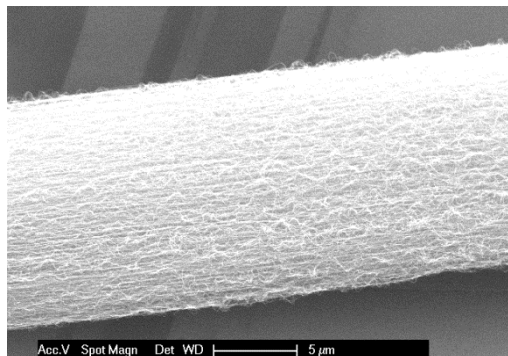
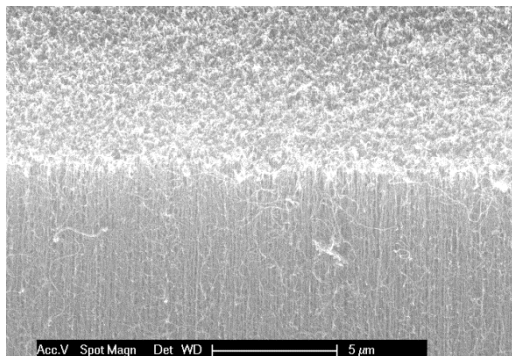
**Equipment:** SPTS uEtch

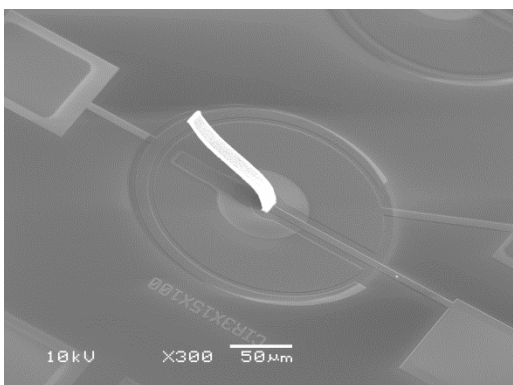
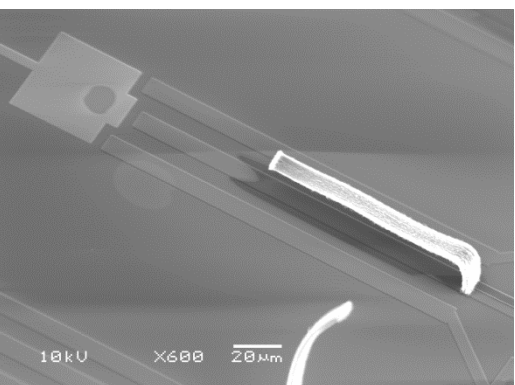
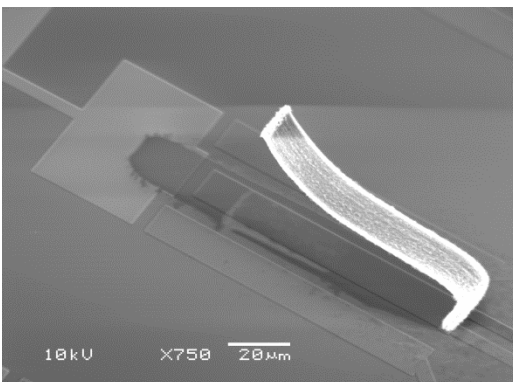
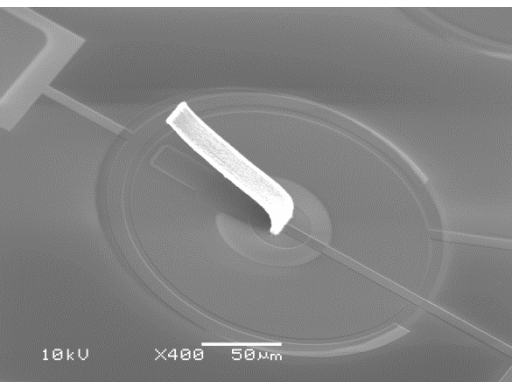
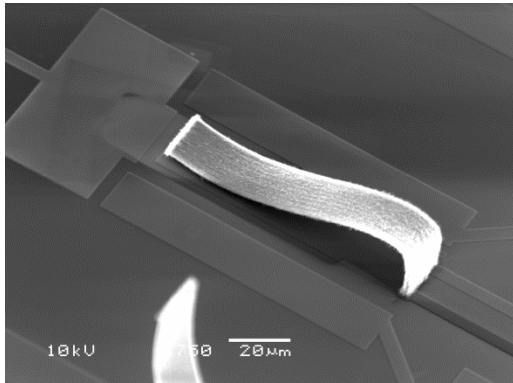
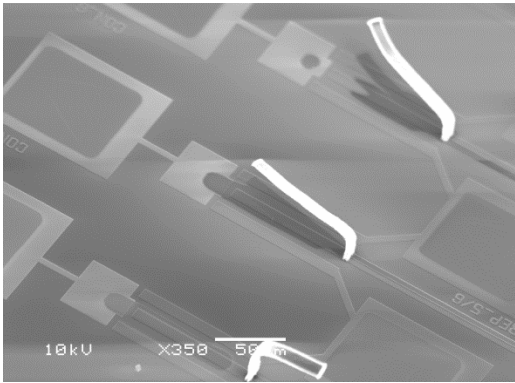
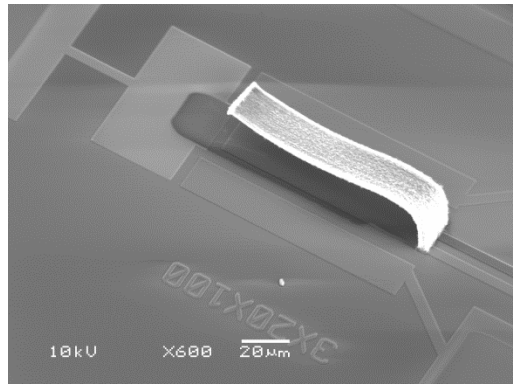
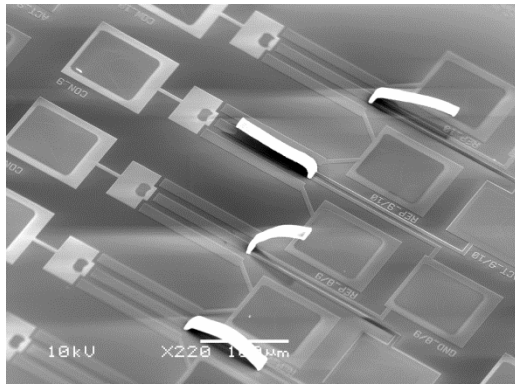
**Note:** recipe 4, cycle 3 (1 cycle = 600 s)

Etch rate of thermal oxide: ~1 μm/cycle

## Appendix E

### Additional Images of CNTs and Devices



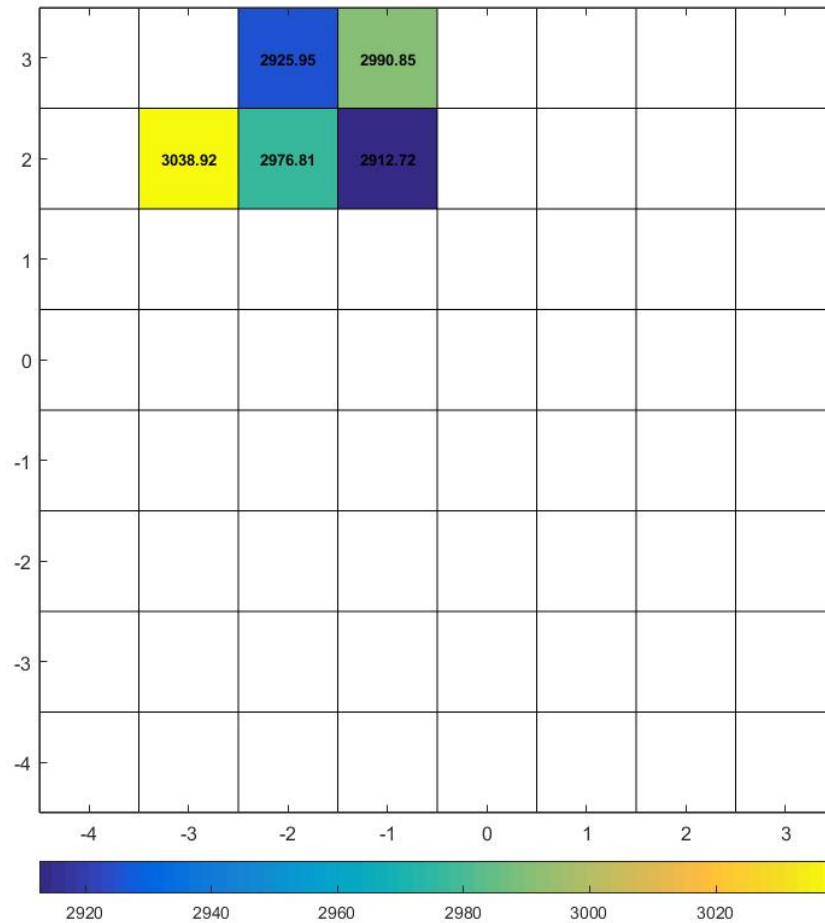


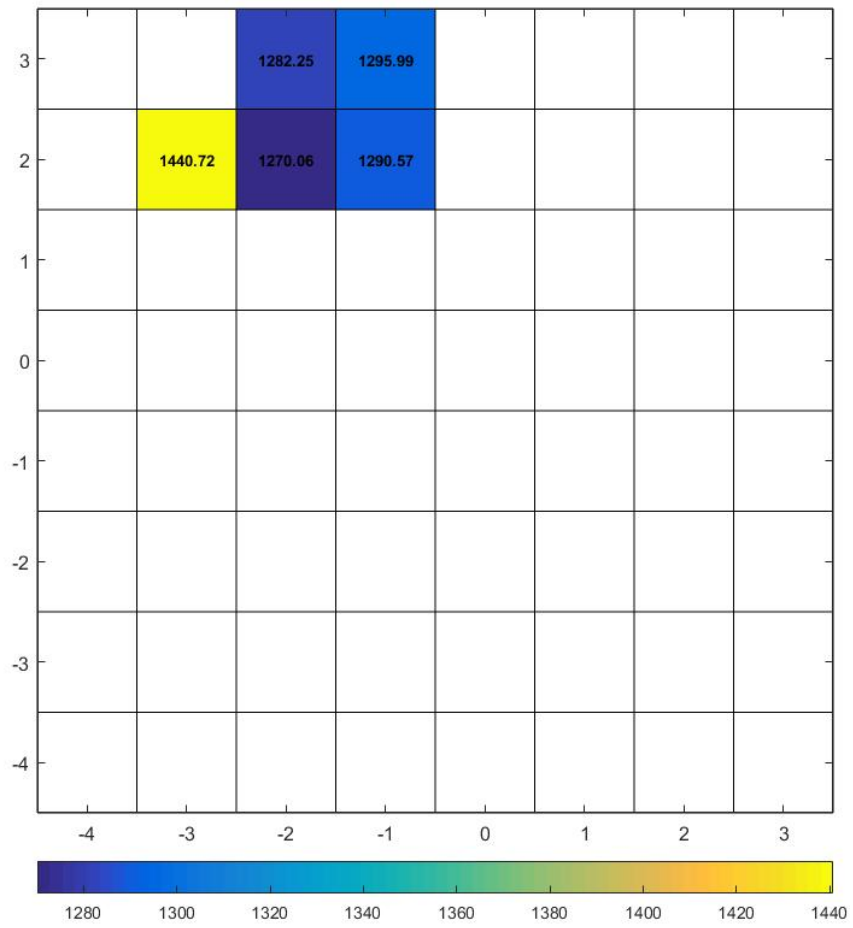


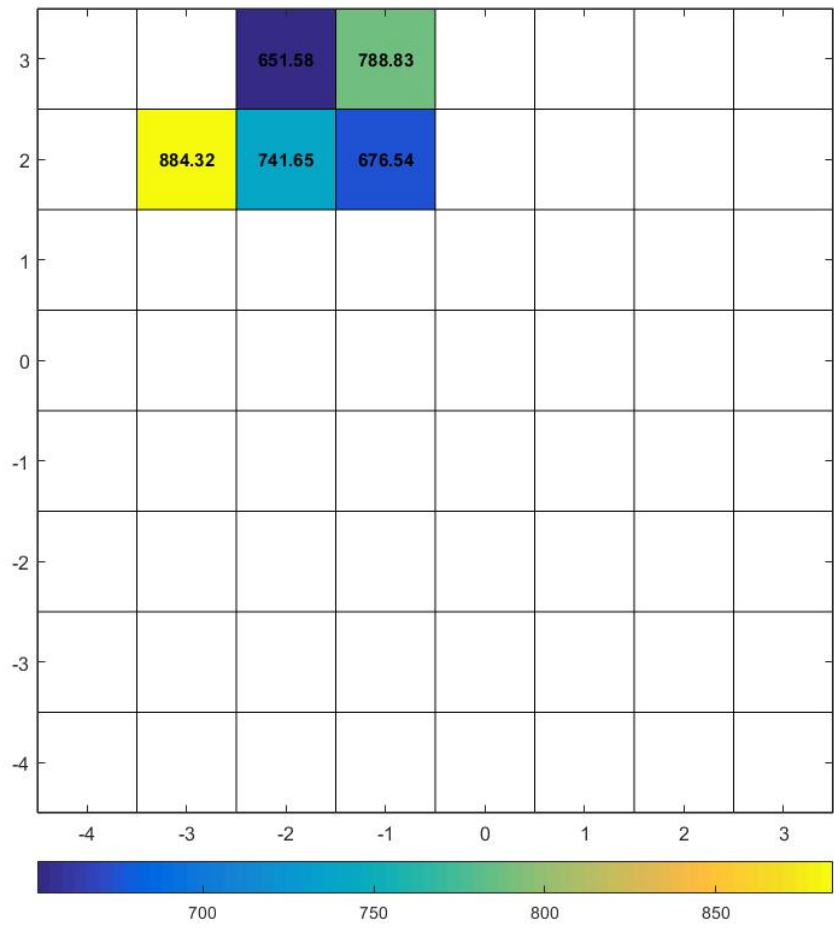
## Appendix F

Wafer distribution of Ti/TiN layer sheet resistance measurement

Ti/TiN sheet resistance measurement with 1 hour deposition





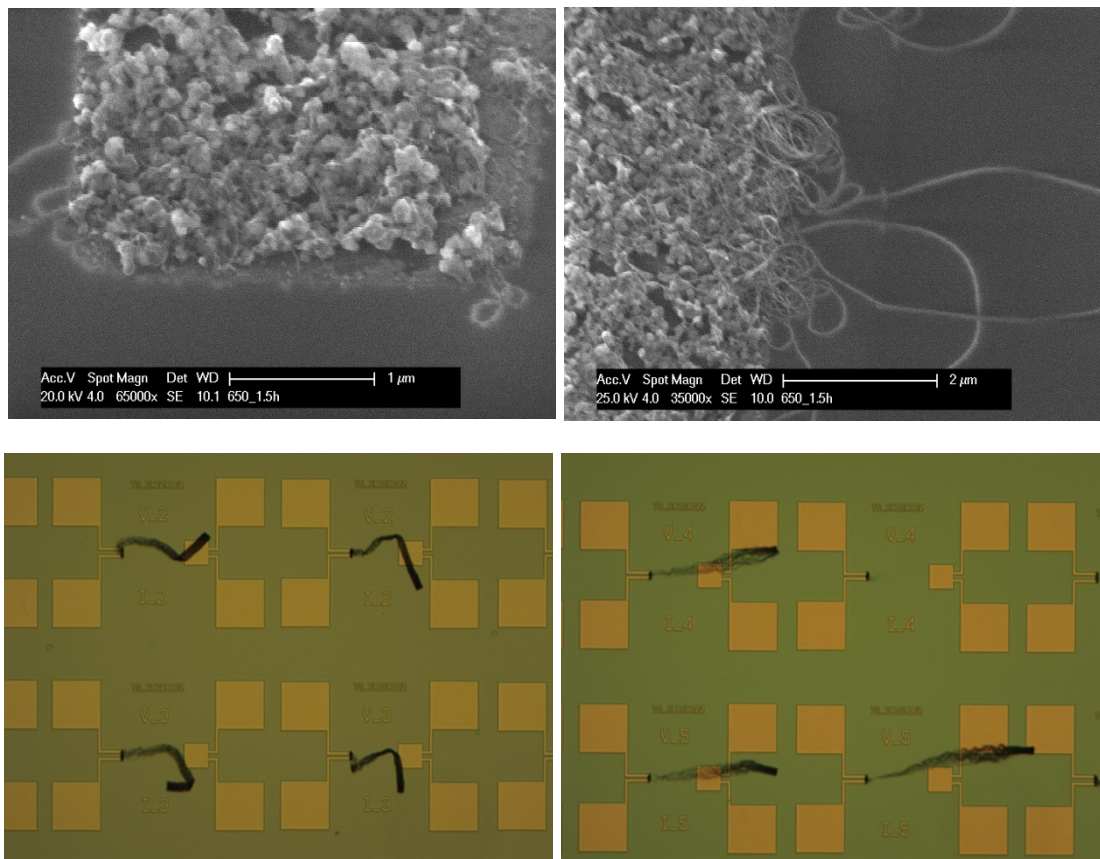


## Appendix G

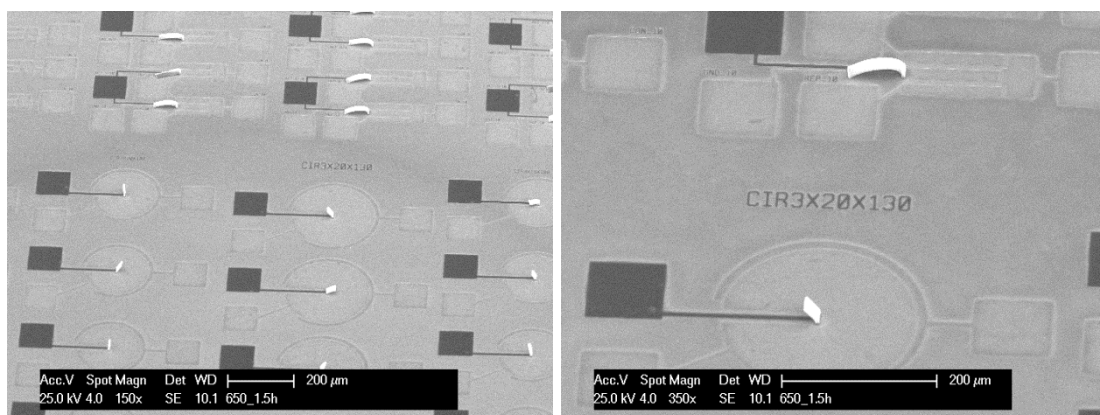
### Interesting observations

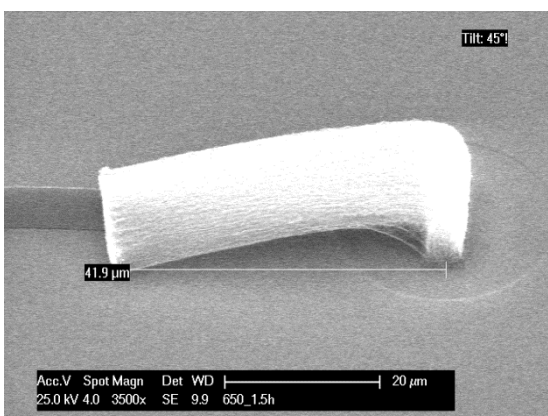
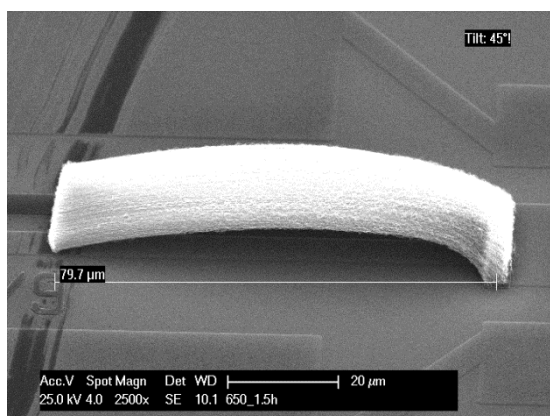
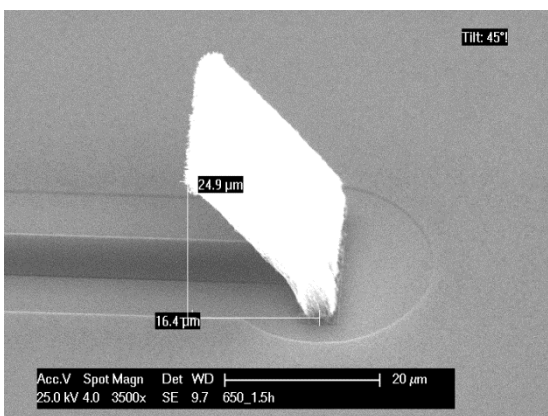
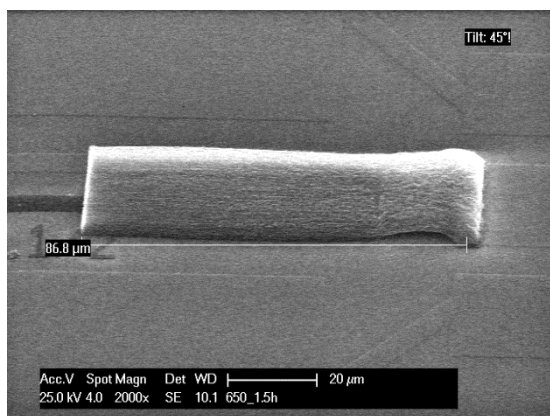
Below are some interesting observations which are not directly related to the studies explained in the remainder of the thesis.

#### G.1 Messy aligned CNT on the oxide layer

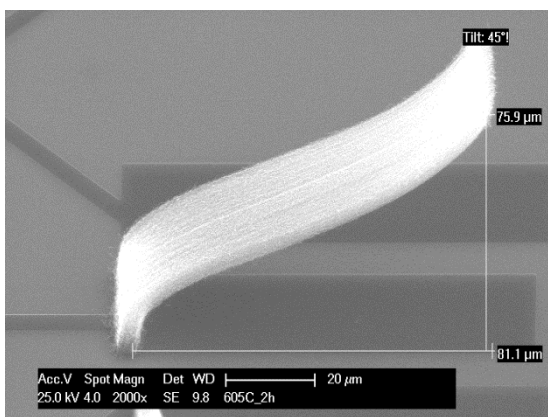
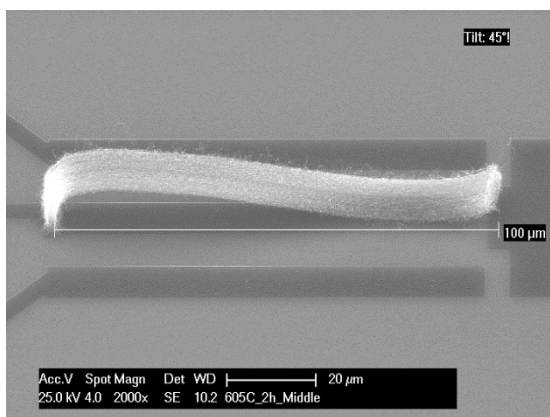


#### G.2 Length difference in one die for different patterns





### G.3 Upturned shape at the CNT bundle tip



## Appendix H

**Table H.1:** Bundles aligned direction after deposition at 620°C for 2 hours with unpatterned substrate topology. L: left aligned; V: vertically aligned; R: right aligned.

	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x10			2x10			2x10			2x15			2x15		
i	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	5	3	2	4	1	5	4	2	4	3	2	5	4	4	2
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x15			2x20			2x20			3x15			3x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	4	4	2	1	6	3	2	4	4	2	7	1	2	5	3
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	3x20			3x20			3x25			3x25			4x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	1	9	0	2	7	1	3	5	2	2	6	2	1	7	2
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	4x15			4x20			4x20			4x25			4x25		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	2	8	0	4	1	5	3	4	3	4	5	1	2	6	2
ii	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x15			2x15			2x20			2x20			3x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	3	5	2	4	3	3	2	6	2	3	7	0	4	4	2
	Bundle dimension	3x15			3x20			3x20			4x15			4x15		

	( $\mu\text{m} \times \mu\text{m}$ )															
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	3	6	1	2	7	1	0	7	3	4	5	1	1	8	1
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	4x20			4x20			4x25			4x25					
	Direction	L	V	R	L	V	R	L	V	R	L	V	R			
	total number	2	6	2	3	4	3	Damage								
iii	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x10			2x10			2x10			2x15			2x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	Damage														
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x15			2x20			2x20			3x15			3x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	Damage														
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	3x20			3x20			3x25			3x25			4x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	Damage														
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	4x15			4x20			4x20			4x25			4x25		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	Damage			7	2	1	3	4	3	4	5	1	3	4	3

**Table H.2:** Bundles aligned direction after deposition at bottom temperature of 600°C and top heat of 600°C for 2 hours with unpatterned substrate topology. L: left aligned; V: vertical aligned; R: right aligned.

Pattern of Structure	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x10			2x10			2x10			2x15			2x15		
i	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	5	1	4	5	0	5	4	2	4	3	1	6	4	3	3
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x15			2x20			2x20			3x15			3x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	1	4	5	3	4	3	4	3	3	2	4	4	4	2	4
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	3x20			3x20			3x25			3x25			4x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	2	2	6	2	3	5	2	4	4	0	5	5	3	4	3
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	4x15			4x20			4x20			4x25			4x25		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	2	4	4	3	2	5	3	4	3	1	6	3	2	7	3
ii	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x15			2x15			2x20			2x20			3x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	2	0	4	4	2	0	2	2	2	2	2	2	2	1	3
	Bundle	3x15			3x20			3x20			4x15			4x15		



	dimension ( $\mu\text{m} \times \mu\text{m}$ )															
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	1	2	3	1	3	2	1	3	2	0	2	4	0	2	4
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	4x20			4x20			4x25			4x25					
	Direction	L	V	R	L	V	R	L	V	R	L	V	R			
	total number	0	5	1	0	5	1	1	4	1	0	5	1			
iii	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x10			2x10			2x10			2x15			2x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	3	5	2	2	2	6	2	5	3	3	5	2	2	2	6
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	2x15			2x20			2x20			3x15			3x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	3	2	5	3	3	4	5	2	3	0	4	6	4	2	4
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	3x20			3x20			3x25			3x25			4x15		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	3	3	4	5	2	3	0	4	6	4	2	4	3	3	4
	Bundle dimension ( $\mu\text{m} \times \mu\text{m}$ )	4x15			4x20			4x20			4x25			4x25		
	Direction	L	V	R	L	V	R	L	V	R	L	V	R	L	V	R
	total number	0	6	4	4	3	3	3	6	1	2	5	3	5	4	1

## Appendix I

**Table I.1:** Right-aligned results of structure i

		Group number (specific dimensions see the appendix 2)																			
	No . die	1	2	3	4	5	6	7	8	9	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8	1 9	2 0
1	i	6	3	5	3	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	ii	1	1	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iii	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iv	1	1	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	v	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	i	5	3	2	1	1	4	2	1	0	0	0	0	0	0	0	0	0	0	0	0
	ii	5	6	3	1	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iii	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iv	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	v	7	4	3	3	5	4	3	3	1	1	2	1	0	0	0	0	0	0	0	0
	vi	4	3	3	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	vii	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	viii	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	i	2	1	3	3	Damaged												0	0	0	0
	ii	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iii	2	1	1	8	6	6	3	2	0	2	1	0	0	0	1	1	0	0	0	0
	iv	3	5	5	2	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	v	2	1	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
4	i	4	8	3	2	6	7	8	4	5	1	4	2	0	0	1	0	0	8	2	1
	ii	5	3	2	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

iii	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
iv	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
v	1 0	1 0	1 0	9	1 0	1 0	6	8	8	4	2	8	8	3	5	0	1 0	9	7	5
vi	1 0	9	8	7	2	2	1	0	0	0	0	0	0	0	0	0	1	0	0	0
vii	5	4	2	0	1	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
viii	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**Table I.2:** Right-aligned results of structure ii

		Group number (specific dimensions see the appendix 2)													
	No. die	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	i	4	1	1	0	1	0	0	2	0	0	0	0	0	0
	ii	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	iii	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iv	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	v	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	i	1	0	0	2	0	1	0	1	1	0	1	0	0	1
	ii	2	1	0	0	0	0	0	0	0	0	0	0	0	0
	iii	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iv	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	v	3	3	0	3	1	0	0	0	0	0	0	0	0	0
	vi	1	0	2	0	0	0	0	0	0	0	0	0	0	0
	vii	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	viii	0	0	0	0	0	0	1	0	0	0	0	0	0	0
3	i	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	ii	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iii	6	1	2	4	0	1	0	0	1	0	1	0	0	0
	iv	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	v	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4	i	1	2	2	3	3	1	3	4	3	2	1	1	0	0
	ii	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	iii	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	iv	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	v	0	1	0	3	3	2	1	1	0	1	3	1	3	3
	vi	2	1	4	4	1	2	0	0	0	0	0	0	0	0
	vii	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	viii	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**Table I.3:** Right-aligned results of structure iii

		Group number (specific dimensions see the appendix 2)																			
	No . die	1	2	3	4	5	6	7	8	9	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8	1 9	2 0
1	i	3	4	6	1	2	1	1	1	0	0	0	1	1	0	1	0	0	0	0	0
	ii	2	3	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	iii	0	1	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iv	2	4	3	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	v	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	i	7	6	3	2	4	1	1	2	0	0	0	0	0	0	0	0	0	0	0	0
	ii	4	4	3	1	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	iii	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iv	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	v	3	5	4	2	2	2	2	2	0	0	0	0	0	0	0	0	0	0	0	0
	vi	4	2	1	2	2	2	1	0	0	0	0	0	0	0	1	0	1	0	0	0
	vii	3	0	2	2	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	viii	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
3	i	2	1	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	ii	2	3	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	iii	3	1 0	1 0	5	7	7	5	4	4	4	1	1	0	0	2	0	0	0	0	0
	iv	4	6	4	1	2	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

	v	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
4	i	6	1 0	1 0	1 0	2	2	7	6	2	0	4	3	3	1	0	0	1 0	1 0	1 0	1 0
	ii	6	4	5	3	1	2	1	0	0	0	0	0	0	0	0	0	2	1	1	0
	iii	2	1	1	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	
	iv	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	v	5	3	3	3	3	0	0	1	0	3	1	0	1	0	2	0	0	1	0	0
	vi	1	1	4	5	2	3	3	0	0	0	0	0	0	0	0	0	0	0	0	
	vii	2	0	2	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
	viii	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

## Appendix J

**Table J:** Right-aligned results of structure iii

Soluti ons/p hotor esists	Dispensi ng of time+cle aning time+dryi ng time	Group number (specific dimensions see the appendix 2)																					
		Numbe r of row in each die	1	2	3	4	5	6	7	8	9	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8	1 9	2 0	
SPR3 012	3+2+5	1	4	3	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		2	0	1	0	0	0	0	0	0	0	0	0	0	0	0							
		3	0	3	2	0	1	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	
AZ30 27	3+2+5	1	-	4	3	4	4	1	2	1	2	1	1	1	0	0	1	0	-	0	0	0	
		2	2	1	3	2	0	0	1	0	0	0	0	0	0	0							
		3	-	1	4	3	3	3	2	3	1	2	0	1	0	0	0	0	0	0	0	0	
IPA	5+5	1	4	6	4	4	3	1	1	1	1	0	0	0	0	0	2	1	1	2	0	0	
		2	0	0	3	0	0	0	0	1	0	1	0	0	0	0							
		3	3	6	2	5	1	1	4	1	1	0	0	0	0	1	0	0	1	1	0	0	
Aceto ne	5+5	1	1	1	4	3	5	4	4	0	1	1	1	1	0	1	0	1	0	0	0	0	
		2	0	0	0	2	1	0	0	0	1	0	0	0	0	0							
		3	2	2	0	1	3	1	3	0	1	1	0	0	0	0	0	0	0	0	0	0	



## Acronyms

MEMS	Micro-Electro-Mechanical Systems
CNT	Carbon Nanotube
MWCNT	Multi-Walled Carbon Nanotube
SWCNT	Single-Walled Carbon Nanotube
SiC	Silicon Carbide
LPCVD	Low Pressure Chemical Vapor Deposition
BM	Blackmagic
SEM	Scanning Electron Microscope
SiN	Silicon Nitride