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Output Voltage Ripple Analysis and Capacitor Sizing in a Four-Switch Buck+Boost Converter Under ZVS Modulation Strategies

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ABSTRACT This article investigates the peak-to-peak output voltage ripple for the four-switch buck+boost (FSBB) converter under four-segment inductor current mode zero-voltage switching (ZVS) modulation strategies in a comprehensive way. Based on the operating mode of the FSBB converter and the relative magnitudes of the output current and inductor current at the switching instants, four distinct cases were analyzed, with corresponding voltage ripple expressions derived for each. The analysis presented in this article provides theoretical guidance for the selection of output capacitor size of the FSBB converter under ZVS modulation strategies. In addition, the introduced analytical method was also used to evaluate and compare the output voltage ripple under three state-of-the-art ZVS modulation schemes. To validate the theoretical analysis, two sets of simulations were conducted. Finally, a laboratory FSBB converter prototype was also built and tested for the validation purpose with an input voltage of 150 V, output voltage of 200 V, and operating power of 1.2 kW.

INDEX TERMS Four-switch buck+boost (FSBB) converter, modulation, output voltage ripple, zero-voltage switching (ZVS), capacitor sizing.

I. INTRODUCTION

The four-switch buck+boost (FSBB) converter has recently attracted significant attention with its circuit topology shown in Fig. 1. Due to its bidirectional power flow capability and voltage step-up (boost) and step-down (buck) functions, this converter has proven to be well suited for many applications requiring wide voltage range, such as electric vehicle (EV) charging [1], two-stage inductive power transfer systems [2], battery energy storage systems [3], envelope tracking application in linear power amplifiers [4], photovoltaic dc-dc power applications [5], common mode noise mitigation applications [6].

Due to the multiple degrees of freedom inherent in the FSBB converter, different modulation strategies can be implemented, which is well summarized in [7]. Meanwhile, the continuous pursuit of higher power density has led to an increase in the switching frequency of power electronic converters over the past several decades [8]. To reduce switching losses in high-frequency operation, soft-switching modulation strategies including zero-voltage switching (ZVS) and zero-current switching (ZCS) are necessary [9]. According to [9], ZVS turn-on and ZCS turn-off can almost completely eliminate switching losses. Meanwhile, turn-on losses of MOSFET switches are typically larger than its turn-off losses due to the existence of the parasitic capacitance C_{oss} [10], and therefore, ZVS turn-on is preferred, which is also the soft-switching modulation studied in this article.

The basic principle of the ZVS modulation method in an FSBB converter is to utilize the inductor current at switching instants to charge and discharge the parasitic capacitance C_{oss} of the MOSFETs such that when the drain-source voltage reduces to zero, the MOSFET can be turned on with zero voltage. To achieve this goal, the inductor current is required to be negative during the turn-on instant for S_1 and S_4, and to be positive during the turn-on instant for S_2 and S_3. Fig. 2 shows the four-segment inductor current mode ZVS

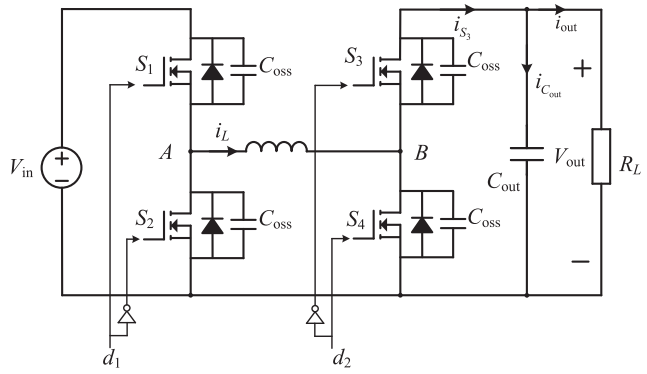


FIGURE 1. Circuit topology of the FSBB converter.

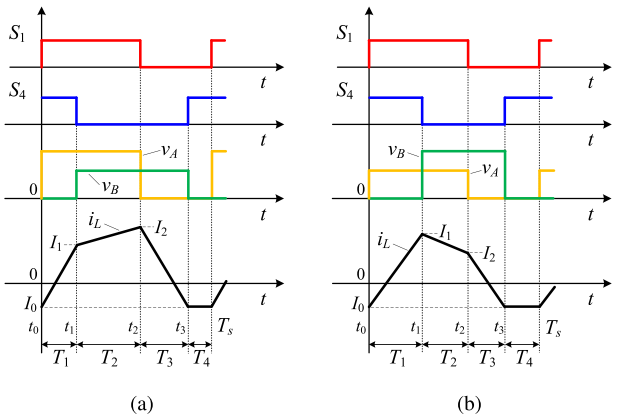


FIGURE 2. Key waveforms of four-segment inductor current mode ZVS modulation, I_0, I_1 and I_2 are inductor current values at switching instants. (a) $V_{in} > V_{out}$. (b) $V_{in} < V_{out}$.

modulation method proposed and presented in [10] and [11]. I_0, I_1 and I_2 are the inductor current values at switching instants. As stated previously, to ensure ZVS turn-on of S_1 and S_4, I_0 should be negative. Meanwhile, I_1 and I_2 should be positive to achieve ZVS turn-on of S_3 and S_2, respectively. Through this modulation method, the ZVS turn-on of all switches can be achieved.

In recent years, significant efforts have been made to optimize the modulation efficiency for the FSBB converter including constant-frequency [10], [12], [13], [14] and variable-frequency ZVS modulation schemes [7], [15], [16], [17], [18]. For example, Zhou et al. optimized the four control time intervals of the modulation method shown in Fig. 2 to minimize the root-mean-square (rms) value of the inductor current and its associated conduction losses [12].

Although modulation strategies of the FSBB converter have received considerable attention recently, the research on its output voltage ripple and the selection of its capacitor capacitance under ZVS modulation strategies remains insufficient. On the other hand, the selection of capacitors will affect the performance indicators of power electronic converters, such as voltage ripple and power density. Previous studies have conducted detailed analysis of output voltage ripple for conventional buck, boost, and buck-boost converters in [19], [20] and [21], respectively. In [22], analysis of the input and output voltage ripple was performed for the synchronous buck, boost, and buck-boost converters under triangular current mode (TCM) ZVS modulation strategy. However, such research on FSBB converters is still lacking. Therefore, to fill this research gap, a comprehensive and detailed analysis of the output voltage ripple in an FSBB converter under ZVS modulation strategies is necessary and meaningful.

Herein, the main contributions of this article are summarized as follows: A comprehensive and detailed analysis of the output voltage ripple of the FSBB converter, along with the expressions for the capacitance selection under the four-segment inductor current mode ZVS modulation strategy, is presented. Additionally, cases under three-segment inductor current mode ZVS modulation strategy in the condition of $T_4 = 0$ are also discussed, and the previously derived voltage ripple formulas remain applicable to these cases. Besides, the relation between TCM-ZVS modulation and three-segment inductor current mode ZVS modulation strategies in terms of voltage ripple is also presented.

The rest of this article is organized as follows: The basic operating principle of the FSBB converter is briefly described in Section II. Section III presents a comprehensive and detailed analysis of the output voltage ripple in the FSBB converter under ZVS modulation strategies. A comparison of voltage ripple under three different ZVS modulation strategies is provided in Section IV, and it is also validated by simulation. In Section V, the presented analysis is experimentally validated using a laboratory prototype. Finally, Section VI concludes this article.

II. OPERATING PRINCIPLE OF FSBB CONVERTER

In this section, the operating principle of the FSBB converter will be briefly described. Some assumptions are made for the following analysis:

1) The inductance is a constant.
2) The gating signals for each half bridge are complementary and their dead time is small enough to be ignored.
3) The input and output voltages are assumed to be constant when the voltage ripple is sufficiently small.

The FSBB converter consists of two half bridges as shown in Fig. 1. S_1 and S_2 form the buck bridge while S_3 and S_4 form the boost bridge. Defining d_1 and d_2 as the duty cycles of S_1 and S_4, respectively, the average voltages of points A and B relative to the bottom bus rail are

$$\bar{v}_A = d_1 V_{\text{in}} \tag{1}$$

$$\bar{v}_B = (1 - d_2) V_{\text{out}}, \tag{2}$$

where V_{in} and V_{out} are the input and output voltages. Based on the volt-second balance law of the inductor under steady state operation, the voltage gain can be derived as (3)

$$G_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{d_1}{1 - d_2}. \tag{3}$$

Equation (3) always holds regardless of the modulation strategies and power values.

Given the modulation strategy shown in Fig. 2, the inductor current expression for both step-up and step-down cases can be expressed as follows with $t_0 = 0$:

$$i_L(t) = \begin{cases} I_0 + \frac{V_{\text{in}}}{L}t, & \text{for } 0 < t \le t_1 \\ i_L(t_1) + \frac{V_{\text{in}} - V_{\text{out}}}{L}(t - t_1), & \text{for } t_1 < t \le t_2 \\ i_L(t_2) - \frac{V_{\text{out}}}{L}(t - t_2), & \text{for } t_2 < t \le t_3 \\ I_0, & \text{for } t_3 < t \le T_s. \end{cases} \tag{4}$$

In (4), L is the inductance, T_s is the switching period with its value being $T_s = T_1 + T_2 + T_3 + T_4$. T_1 to T_4 are the control time intervals.

According to (4), the inductor current values I_1 and I_2 at the switching instants t_1 and t_2 can be expressed as follows:

$$I_1 = I_0 + \frac{V_{\text{in}}}{L}T_1, \quad I_2 = I_1 + \frac{V_{\text{in}} - V_{\text{out}}}{L}T_2. \tag{5}$$

Besides, d_1 and d_2 can also be expressed as follows:

$$d_1 = \frac{T_1 + T_2}{T_s}, \quad d_2 = \frac{T_1 + T_4}{T_s}. \tag{6}$$

According to [12], the ZVS conditions are expressed as follows:

$$\begin{cases} I_1 \ge \frac{2C_{\text{oss}}V_{\text{out}}}{t_{\text{dead}}}, & \text{for ZVS of } S_3 \\ I_2 \ge \frac{2C_{\text{oss}}V_{\text{in}}}{t_{\text{dead}}}, & \text{for ZVS of } S_2 \\ |I_0| \ge \frac{2C_{\text{oss}}\max(V_{\text{in}}, V_{\text{out}})}{t_{\text{dead}}}, & \text{for ZVS of } S_1 \text{ and } S_4. \end{cases} \tag{7}$$

In (7), C_{oss} is the MOSFET parasitic capacitance, t_{dead} is the dead time. For simplicity, the ZVS conditions can be expressed in (8), as presented in [12].

$$|I_0| \ge I_{\text{zvs}}, \quad I_1 \ge I_{\text{zvs}}, \quad I_2 \ge I_{\text{zvs}}. \tag{8}$$

In (8), $I_{\text{zvs}} = \dfrac{2C_{\text{oss}}\max(V_{\text{in}}, V_{\text{out}})}{t_{\text{dead}}}$.

III. OUTPUT VOLTAGE RIPPLE ANALYSIS

In this section, the output voltage ripple analysis will be carried out based on the four-segment inductor current mode modulation strategy. To calculate the output voltage ripple, herein, it is assumed that the output current is constant and that the capacitor equivalent series resistance (ESR) is neglected [23], [24].

A. VOLTAGE RIPPLE ANALYSIS UNDER FOUR-SEGMENT INDUCTOR CURRENT MODE MODULATION

Based on the operation of the FSBB converter in either step-up or step-down mode, as well as the magnitudes of the output current and inductor current at switching instants, four cases need to be considered when analyzing the voltage ripple of the output capacitor, and they are shown in Fig. 3 for the case when $V_{\text{in}} < V_{\text{out}}$ and Fig. 4 for the case when $V_{\text{in}} > V_{\text{out}}$, respectively.

During steady state operation, within a single switching period, there is no net change in the charge accumulated on the capacitor. Therefore, the voltage ripple can be calculated based on either the charge accumulated or released by the capacitor, yielding the same result in both cases. Meanwhile, one can also find that for all the cases shown in both Figs. 3 and 4, within a single switching period, the capacitor voltage will only continuously rise from its minimum to its maximum value, and then continuously fall from its maximum to its

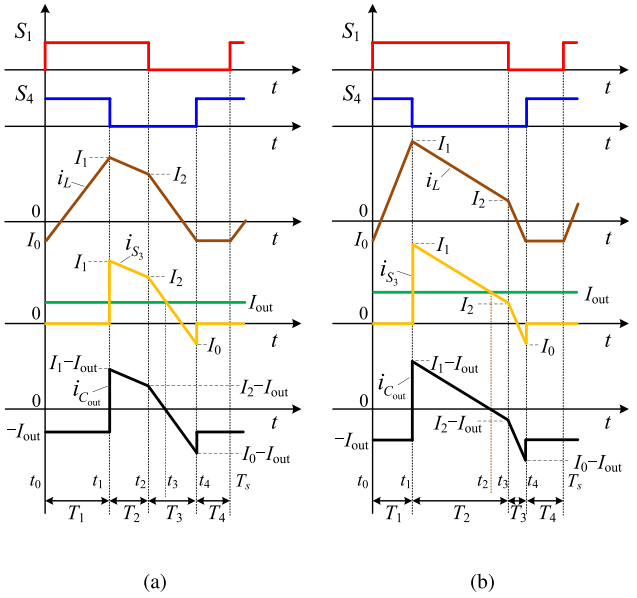


FIGURE 3. Waveforms of gating signals, inductor current, current flowing through S_3, and capacitor current in step-up mode operation when $V_{\text{in}} < V_{\text{out}}$. The reference directions of voltage and current are shown in Fig. 1. (a) Case when $I_2 > I_{\text{out}}$. (b) Case when $I_2 < I_{\text{out}}$.

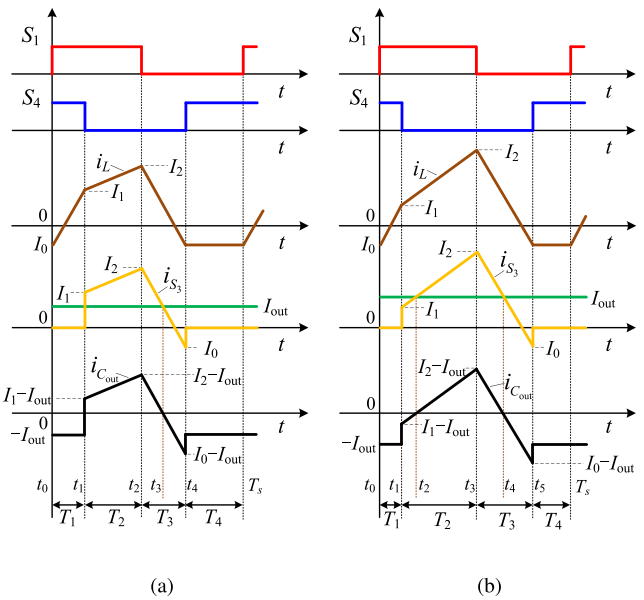


FIGURE 4. Waveforms of gating signals, inductor current, current flowing through S_3, and capacitor current in step-down mode operation when $V_{\text{in}} > V_{\text{out}}$. (a) Case when $I_1 > I_{\text{out}}$. (b) Case when $I_1 < I_{\text{out}}$.

minimum value, without exhibiting intermediate behaviors such as rising, falling, and rising again. This characteristic facilitates the calculation of the peak-to-peak voltage ripple of the capacitor.

For the rest of the article, the peak-to-peak voltage ripple will be calculated based on the accumulated charge during the period when the capacitor current is positive within a switching cycle. During this phase, the capacitor voltage will increase from its minimum value to its maximum value.

1) CASES IN STEP-UP MODE

For Fig. 3(a) when $I_{out} < I_2$, the peak-to-peak voltage ripple based on the charge accumulated during time interval from t_1 to t_3 is

$$\Delta V_{pp\_boost\_1} = \frac{1}{C_{out}} \cdot \left[\frac{(I_1 + I_2 - 2I_{out})(t_2 - t_1)}{2} + \frac{(I_2 - I_{out})(t_3 - t_2)}{2} \right]. \quad (9)$$

In (9), I_{out} is the output current, $t_2 - t_1 = T_2$ and $t_3 - t_2 = \frac{I_2 - I_{out}}{I_2 - I_0} T_3$. Substituting these two expressions into (9) then yields (10)

$$\Delta V_{pp\_boost\_1} = \frac{(I_1 + I_2 - 2I_{out})T_2}{2C_{out}} + \frac{(I_2 - I_{out})^2 T_3}{2(I_2 - I_0)C_{out}}. \quad (10)$$

For Fig. 3(b) when $I_{out} > I_2$, the peak-to-peak voltage ripple based on the charge accumulated during time interval from t_1 to t_2 is

$$\Delta V_{pp\_boost\_2} = \frac{(I_1 - I_{out})(t_2 - t_1)}{2C_{out}}. \quad (11)$$

In (11), $t_2 - t_1 = \frac{I_1 - I_{out}}{I_1 - I_2} T_2$. Substituting this expression into (11) then yields (12)

$$\Delta V_{pp\_boost\_2} = \frac{(I_1 - I_{out})^2 T_2}{2(I_1 - I_2)C_{out}}. \quad (12)$$

2) CASES IN STEP-DOWN MODE

For Fig. 4(a) when $I_{out} < I_1$, the peak-to-peak voltage ripple based on the charge accumulated during time interval from t_1 to t_3 is

$$\Delta V_{pp\_buck\_1} = \frac{1}{C_{out}} \cdot \left[\frac{(I_1 + I_2 - 2I_{out})(t_2 - t_1)}{2} + \frac{(I_2 - I_{out})(t_3 - t_2)}{2} \right]. \quad (13)$$

In (13), $t_2 - t_1 = T_2$, $t_3 - t_2 = \frac{I_2 - I_{out}}{I_2 - I_0} T_3$. Substituting these two expressions into (13) then yields (14)

$$\Delta V_{pp\_buck\_1} = \frac{(I_1 + I_2 - 2I_{out})T_2}{2C_{out}} + \frac{(I_2 - I_{out})^2 T_3}{2(I_2 - I_0)C_{out}}. \quad (14)$$

For Fig. 4(b) when $I_{out} > I_1$, the peak-to-peak voltage ripple based on the charge accumulated during time interval from t_2 to t_4 is

$$\Delta V_{pp\_buck\_2} = \frac{(I_2 - I_{out})(t_4 - t_2)}{2C_{out}}. \quad (15)$$

In (15), $t_4 - t_2 = \frac{I_2 - I_{out}}{I_2 - I_1} T_2 + \frac{I_2 - I_{out}}{I_2 - I_0} T_3$. Substituting this expression into (15) then yields (16)

$$\Delta V_{pp\_buck\_2} = \frac{(I_2 - I_{out})^2 T_2}{2(I_2 - I_1)C_{out}} + \frac{(I_2 - I_{out})^2 T_3}{2(I_2 - I_0)C_{out}}. \quad (16)$$

TABLE 1. Summary of Peak-to-Peak Voltage Ripple Expressions

Cases	Voltage Ripple Expression
Case in Fig. 3(a) when $V_{in} \le V_{out}$ and $I_2 \ge I_{out}$	$\frac{(I_1+I_2-2I_{out})T_2}{2C_{out}} + \frac{(I_2-I_{out})^2 T_3}{2(I_2-I_0)C_{out}}$
Case in Fig. 3(b) when $V_{in} < V_{out}$ and $I_2 \le I_{out}$	$\frac{(I_1-I_{out})^2 T_2}{2(I_1-I_2)C_{out}}$
Case in Fig. 4(a) when $V_{in} \ge V_{out}$ and $I_1 \ge I_{out}$	$\frac{(I_1+I_2-2I_{out})T_2}{2C_{out}} + \frac{(I_2-I_{out})^2 T_3}{2(I_2-I_0)C_{out}}$
Case in Fig. 4(b) when $V_{in} > V_{out}$ and $I_1 \le I_{out}$	$\frac{(I_2-I_{out})^2 T_2}{2(I_2-I_1)C_{out}} + \frac{(I_2-I_{out})^2 T_3}{2(I_2-I_0)C_{out}}$

3) BOUNDARY CONDITION ANALYSIS

First, when $V_{in} = V_{out}$, in this case, $I_1 = I_2$, so the output current I_{out} will only be smaller than I_1 or I_2. Therefore, in this case, the voltage ripple can be calculated using the corresponding expression presented in either (10) for Fig. 3(a) or (14) for Fig. 4(a). By further setting $I_2 = I_1$, the voltage ripple expression when $V_{in} = V_{out}$ can be derived from both (10) and (14) as

$$\Delta V_{pp} = \frac{(I_1 - I_{out})T_2}{C_{out}} + \frac{(I_1 - I_{out})^2 T_3}{2(I_1 - I_0)C_{out}}. \quad (17)$$

Second, the cases when the output current I_{out} equals the inductor current of I_1 or I_2 at switching instant need to be analyzed. For both Fig. 3(a) and (b), when $I_2 = I_{out}$, the time interval from t_2 to t_3 is zero, and by setting $I_2 = I_{out}$, both equations of (10) and (12) for Fig. 3 yield the same result, which is

$$\Delta V_{pp} = \frac{(I_1 - I_{out})T_2}{2C_{out}}. \quad (18)$$

Similarly, for Fig. 4(b) when $I_1 = I_{out}$, the time interval from t_1 to t_2 becomes zero, by setting $I_1 = I_{out}$, both equations of (14) and (16) for Fig. 4 yield the same result, which is

$$\Delta V_{pp} = \frac{(I_2 - I_{out})T_2}{2C_{out}} + \frac{(I_2 - I_{out})^2 T_3}{2(I_2 - I_0)C_{out}}. \quad (19)$$

4) SUMMARY OF EQUATIONS

A summary of the previously derived equations of the peak-to-peak voltage ripple is given in Table 1. As can be seen from Table 1, the voltage ripple expressions of the cases in Figs. 3(a) and 4(a) are the same.

According to the previous theoretical analysis, it can be concluded that once the control time intervals are determined,

TABLE 2. Summary of Expressions for Capacitor Sizing

Cases	Minimum Capacitance Needed For Voltage Ripple $\Delta V_{\rm pp}$
Case in Fig. 3(a) when $V_{\rm in} \le V_{\rm out}$ and $I_2 \ge I_{\rm out}$	$\frac{(I_1+I_2-2I_{\rm out})T_2}{2\Delta V_{\rm pp}} + \frac{(I_2-I_{\rm out})^2 T_3}{2(I_2-I_0)\Delta V_{\rm pp}}$
Case in Fig. 3(b) when $V_{\rm in} < V_{\rm out}$ and $I_2 \le I_{\rm out}$	$\frac{(I_1-I_{\rm out})^2 T_2}{2(I_1-I_2)\Delta V_{\rm pp}}$
Case in Fig. 4(a) when $V_{\rm in} \ge V_{\rm out}$ and $I_1 \ge I_{\rm out}$	$\frac{(I_1+I_2-2I_{\rm out})T_2}{2\Delta V_{\rm pp}} + \frac{(I_2-I_{\rm out})^2 T_3}{2(I_2-I_0)\Delta V_{\rm pp}}$
Case in Fig. 4(b) when $V_{\rm in} > V_{\rm out}$ and $I_1 \le I_{\rm out}$	$\frac{(I_2-I_{\rm out})^2 T_2}{2(I_2-I_1)\Delta V_{\rm pp}} + \frac{(I_2-I_{\rm out})^2 T_3}{2(I_2-I_0)\Delta V_{\rm pp}}$

the inductor current at each switching instant can be obtained accordingly, and thus the output voltage ripple can also be calculated.

B. CAPACITOR SIZING

Based on the derived formulas summarized in Table 1, the capacitor size can also be determined according to the specified peak-to-peak voltage ripple or ripple factor requirement. For example, if the maximum allowed voltage ripple is $\Delta V_{\rm pp\_max}$, then the minimum required output capacitance should be determined based on (20) for the case in Fig. 3(a):

$$C_{\rm out} \ge \frac{(I_1 + I_2 - 2I_{\rm out})T_2}{2\Delta V_{\rm pp\_max}} + \frac{(I_2 - I_{\rm out})^2 T_3}{2(I_2 - I_0)\Delta V_{\rm pp\_max}}. \quad (20)$$

Similarly, the corresponding formulas for the remaining three cases can also be derived, and they are summarized in Table 2.

C. CASE UNDER THREE-SEGMENT INDUCTOR CURRENT MODE MODULATION WHEN T_4 IS ZERO

When the time interval T_4 is zero, the modulation strategy shown in Fig. 2 transitions into a three-segment inductor current mode modulation presented in Figs. 5 and 6, which occurs in many cases [7], [11], [13], [18], [25]. The previously derived equations of (9), (11), (13), (15) or (10), (12), (14), (16) remain applicable to the cases presented in Figs. 5 and 6. Specifically, in this case, the control time intervals can be expressed as follows:

$$T_1 = d_2 T_s, \quad T_2 = (d_1 - d_2)T_s, \quad T_3 = (1 - d_1)T_s. \quad (21)$$

D. RELATION WITH TCM-ZVS MODULATION STRATEGY

TCM-ZVS modulation strategies can also be applied to the FSBB converter [7], [15]. In [22], the output voltage ripple was analyzed under TCM-ZVS operations, and its voltage ripple expressions were also derived. In fact, these expressions can also be derived from the three-segment inductor current mode modulation strategy, and they are discussed as follows.

1) TCM-ZVS BOOST MODE MODULATION

When switch S_1 is always on, namely, its duty cycle becomes one, then the modulation strategy in Fig. 5(b) turns into TCM-ZVS boost mode modulation. In this case, the time interval T_3 in Fig. 5(b) becomes zero, and I_2 coincides with I_0.

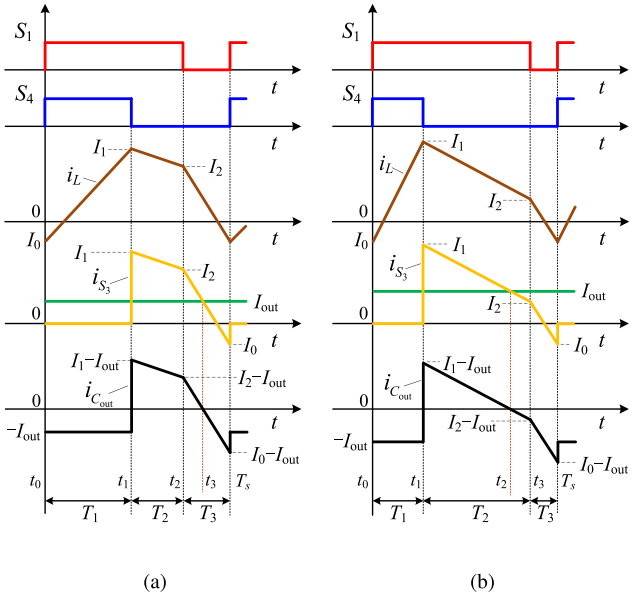


FIGURE 5. Waveforms of gating signals, inductor current, current flowing through S_3, and capacitor current in step-up mode operation when $V_{\rm in} < V_{\rm out}$ and $T_4 = 0$. (a) Case when $I_2 > I_{\rm out}$. (b) Case when $I_2 < I_{\rm out}$.

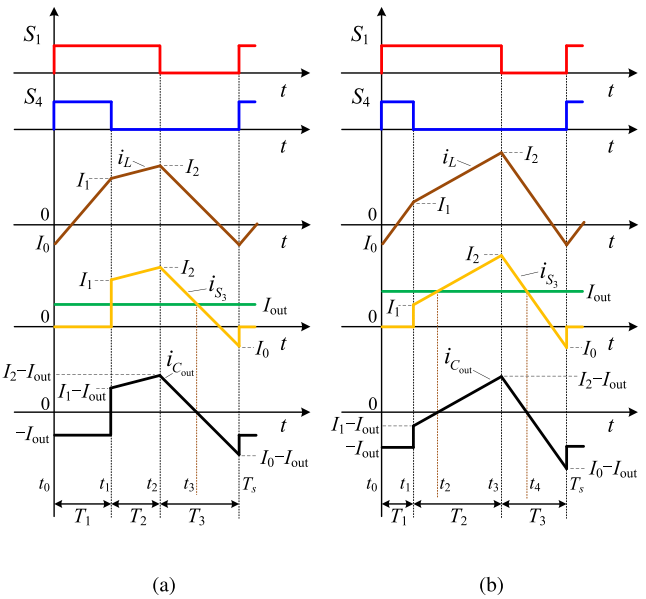


FIGURE 6. Waveforms of gating signals, inductor current, current flowing through S_3, and capacitor current in step-down mode operation when $V_{\rm in} > V_{\rm out}$ and $T_4 = 0$. (a) Case when $I_1 > I_{\rm out}$. (b) Case when $I_1 < I_{\rm out}$.

Fig. 7(a) redraws the corresponding waveforms under TCM-ZVS boost mode modulation. In this case, (11) still holds with $t_2 - t_1 = \frac{I_1 - I_{\rm out}}{I_1 - I_0} T_2$.

2) TCM-ZVS BUCK MODE MODULATION

When switch S_3 is always on, then the modulation strategy in Fig. 6(b) turns into TCM-ZVS buck mode modulation.

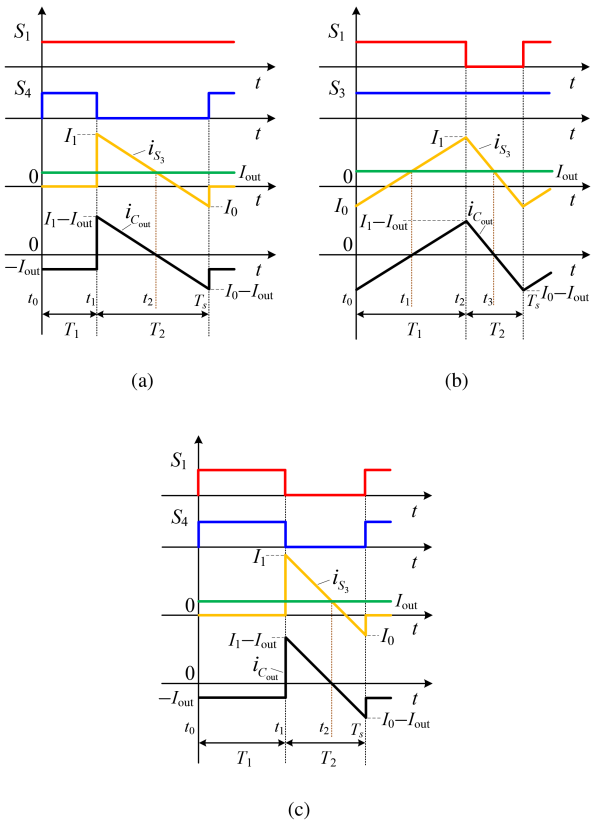


FIGURE 7. Waveforms of gating signals, current flowing through S_3, and capacitor current in TCM-ZVS modulation. (a) Boost mode. (b) Buck mode. (c) Buck-boost mode.

In this case, the time interval T_1 in Fig. 6(b) becomes zero, and I_1 coincides with I_0. Fig. 7(b) redraws the corresponding waveforms under TCM-ZVS buck mode modulation. By using the same approach as in Fig. 4(b) [also in Fig. 6(b)], the expression for the voltage ripple can be derived as follows:

$$\Delta V_{\text{pp\_TCM\_buck}} = \frac{(I_1 - I_{\text{out}})(t_3 - t_1)}{2C_{\text{out}}}. \tag{22}$$

In (22), $t_3 - t_1 = \dfrac{I_1 - I_{\text{out}}}{I_1 - I_0}(T_1 + T_2) = \dfrac{I_1 - I_{\text{out}}}{I_1 - I_0}T_s$.

3) TCM-ZVS BUCK-BOOST MODE MODULATION

When switches S_1 and S_4 turn on/off simultaneously, then the modulation strategies in Figs. 5(a) and 6(a) turn into TCM-ZVS buck-boost mode modulation. In this case, the time interval T_2 in both figures becomes zero, and I_1 coincides with I_2. Fig. 7(c) redraws the corresponding waveforms under TCM-ZVS buck-boost mode modulation. In this case, the voltage ripple is described by the same expression as in the TCM-ZVS boost mode modulation.

From the above analysis, it can be seen that the voltage ripple under TCM-ZVS modulation can be derived from the three-segment inductor current mode modulation. Further simplifications of the expressions can be found in [22].

IV. VOLTAGE RIPPLE COMPARISON UNDER DIFFERENT ZVS MODULATION STRATEGIES AND SIMULATION VALIDATION

In this section, the previously derived formulas will be applied to compare the output voltage ripple under three different state-of-the-art ZVS modulation strategies, which were introduced in [12], [13] and [18]. The simulation results will also be presented, which shows a close match with the theoretical calculations.

A. COMPARISON OF VOLTAGE RIPPLE AND CAPACITOR SIZING

A case study with parameters close to experiments was carried out for comparison, herein, the input voltage V_{in} ranges from 150 V to 250 V, output voltage V_{out} is 200 V, power is 1.2 kW, inductance L is 100 μH, and $I_0 = -I_{\text{zvs}} = -3$ A. The switching frequency is selected to be 25 kHz for the methods based on [12] and [13] since they are constant-frequency modulation strategies, whereas in [18], it is varied.

In [12], the modulation strategy, shown in Fig. 2, with minimum inductor rms current was proposed. According to [12], the relationship between T_1 and T_2 can be expressed as

$$T_1 = \frac{-LI_0 - V_{\text{in}}T_2 + \sqrt{A}}{V_{\text{in}}}. \tag{23}$$

In (23), $A = L^2I_0^2 + 2LT_sV_{\text{out}}I_{\text{out}} + V_{\text{in}}V_{\text{out}}T_2^2$.

For T_2, an enumeration approach can be adopted, since once T_2 is known, T_1 can be determined. Based on (3) and (6), T_3 can also be calculated, which is

$$T_3 = \frac{V_{\text{in}}}{V_{\text{out}}}(T_1 + T_2) - T_2. \tag{24}$$

Since all the control time intervals are known with $T_4 = T_s - (T_1 + T_2 + T_3)$, the corresponding currents, including the rms value of the inductor current, can be calculated accordingly. It should be pointed out that the selection of T_2 must ensure that the ZVS operating condition of the FSBB converter meets the requirement of (8), and all calculated control time intervals are greater or equal to zero. The searching time step of T_2 is 100 ns in this article.

In [13], a constant frequency ZVS modulation strategy featuring two operating modes, namely, pseudocritical continuous current mode (PCRM) and pseudodiscontinuous current mode (PDCM), was proposed. Under PCRM, T_4 is zero, the duty cycle d_2 can be expressed as (25) based on [13].

$$d_2 = \frac{(\frac{V_{\text{out}}}{V_{\text{in}}})^2 + \frac{LI_{\text{zvs}}}{V_{\text{in}}T_s} - \sqrt{B}}{(\frac{V_{\text{out}}}{V_{\text{in}}})^2 + \frac{V_{\text{out}}}{V_{\text{in}}} + 1}. \tag{25}$$

In (25), B is expressed as

$$B = \left(\frac{V_{\text{in}} + V_{\text{out}}}{V_{\text{in}}} - \frac{LI_{\text{zvs}}}{V_{\text{in}}T_s}\right)^2 - \left[\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right)^2 + \frac{V_{\text{out}}}{V_{\text{in}}} + 1\right]\left(\frac{2LI_{\text{out}}}{V_{\text{in}}T_s} + 1\right). \tag{26}$$

Once d_2 is known, d_1 can be calculated based on (3). Combing (5), (21), and formulas in Table 1, the voltage ripple can be subsequently calculated. It should be noted that when the input voltage is 230 V, 240 V or 250 V, in order to meet the ZVS condition given by (8), the four control time intervals are calculated using (27), which follows the same approach proposed in [26], where $I_1 = I_{zvs}$ in step-down mode.

$$\begin{cases} T_1 = \frac{2LI_{zvs}}{V_{in}}, \\ T_2 = \frac{-b+\sqrt{b^2-4ac}}{2a}, \\ T_3 = \frac{V_{in}}{V_{out}}(T_1+T_2) - T_2, \\ T_4 = T_s - (T_1+T_2+T_3). \end{cases} \tag{27}$$

In (27), $a=(V_{in}-V_{out})V_{in}$, $b=2LV_{in}I_{zvs}$, $c=-2LT_sV_{out}I_{out}$.

In [18], a variable-frequency three-segment inductor current mode ZVS modulation strategy was proposed, and its operating waveforms are shown in Figs. 5 and 6. For this modulation, when the FSBB converter is in step-up mode, the duty cycle d_1 is fixed at a constant value, denoted as d_{max}. When the converter is in step-down mode, the duty cycle d_2 is fixed at a constant value, denoted as d_{min}. Besides, $d_{max}+d_{min}=1$ for the purpose of achieving a seamless step-up and step-down mode transition. The switching frequency of this modulation for both step-up and step-down operating modes can be expressed as follows according to [18]:

$$f_s = \frac{V_{in}[d_1(1-d_1)+d_2(d_1-d_2)]}{2L[I_{out}-I_0(1-d_2)]}. \tag{28}$$

Combing (3), (5), (21), (28), and formulas in Table 1, the voltage ripple can be subsequently calculated.

Fig. 8(a) shows the optimal values of T_2 and duty cycles based on the method in [12] while Fig. 8(b) shows the values of T_4 and duty cycles based on the method in [13]. Fig. 9 shows the switching frequency value based on the method in [18].

Fig. 10 shows the peak-to-peak output voltage ripple under the previously mentioned ZVS modulation strategies based on the derived formulas in Table 1. Since the modulation strategies presented in [12] and [13] yield same control time intervals, the output voltage ripple values are also the same. Based on the expressions for capacitor sizing summarized in Table 2, Fig. 11 shows the minimum output capacitance required to achieve a maximum peak-to-peak voltage ripple factor of 1% ($\Delta V_{pp\_max}=2$ V) under the previously mentioned ZVS modulation strategies. So, based on this example, if the maximum allowed output voltage ripple is 2 V, then a capacitor with value larger than 50 μF is required.

B. SIMULATION VALIDATION

To validate the previous theoretical calculations, two sets of simulations were conducted based on method from [13] and [18], respectively. The circuit simulation parameters are consistent with those described in Section IV-A. The circuit was simulated using MATLAB Simulink with variable-step ODE45 solver. The maximum step size was 2e-7 s, and the relative tolerance was 1e-6. The simulation results are shown in Fig. 12.

As can be seen from Fig. 12, the simulated ΔV_{pp} closely matches the calculated ΔV_{pp}, which effectively validates the correctness of the previous theoretical derivations.

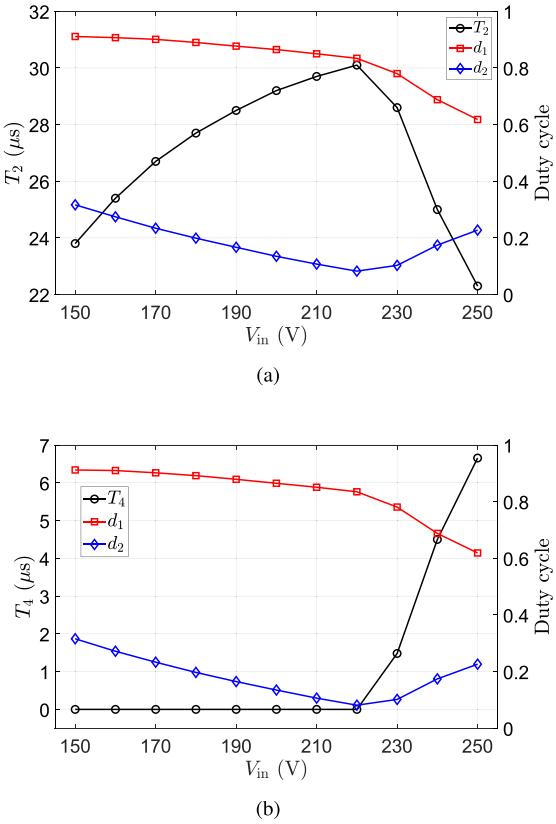


FIGURE 8. Time interval values of T_2, T_4, and duty cycles based on the methods in [12] and [13]. (a) Values of T_2, d_1 and d_2 based on the method in [12]. (b) Values of T_4, d_1 and d_2 based on the method in [13].

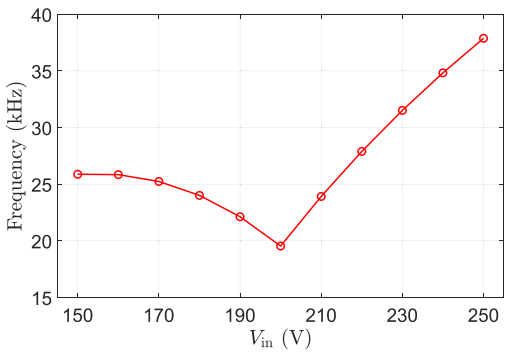


FIGURE 9. Switching frequency based on the method in [18], $d_{max}=0.9$.

V. EXPERIMENTAL VALIDATION

In addition to simulation validation, a laboratory prototype of FSBB converter was also built for the experiment, which consists of two half-bridge boards. The converter prototype

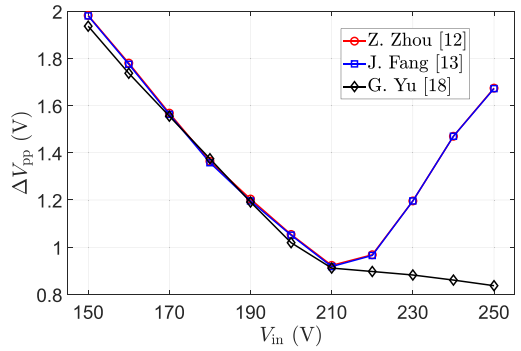


FIGURE 10. Peak-to-peak output voltage ripple under ZVS modulation strategies, C_{out} is selected to be 50 μF as an example.

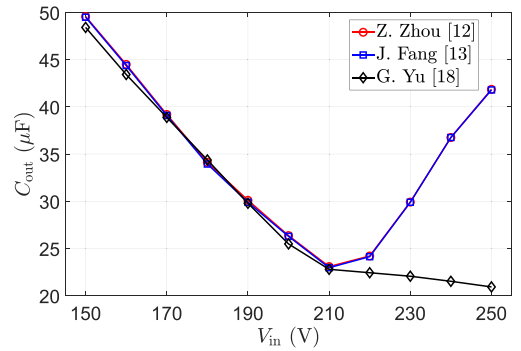


FIGURE 11. Minimum output capacitance required to achieve a maximum peak-to-peak voltage ripple factor of 1%, namely $\Delta V_{pp\_max} = 2$ V.

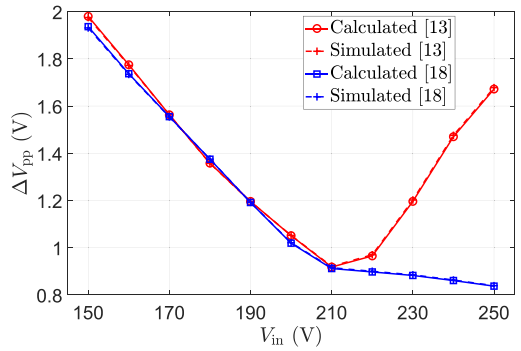
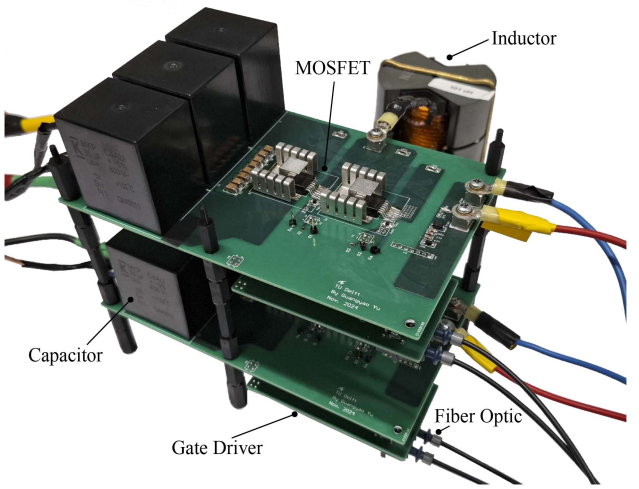
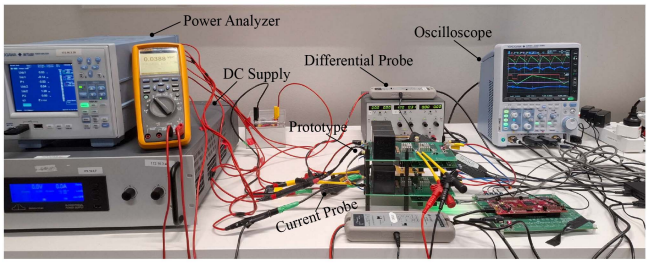


FIGURE 12. Simulated and calculated peak-to-peak output voltage ripple based on the ZVS modulation strategies from [13] and [18]. The circuit operating parameters are described in Section IV-A.



(a)



(b)

FIGURE 13. FSBB converter prototype and experimental setup. (a) Converter prototype. (b) Laboratory experimental setup.

TABLE 3. Key Parameters of the FSBB Prototype

MOSFET Switch	C3M0032120J1
Input Capacitor C_{in}	KEMET, C4AU Film, 35 μF × 3 Knowles, MLCC, 100 nF × 8
Output Capacitor C_{out}	KEMET, C4AU Film, 35 μF × 3 Knowles, MLCC, 100 nF × 8
Inductor	PM 74/59, N87, 100 μH
Gate Driver IC	Broadcom, ACPL-W349

TABLE 4. Measured Inductance

f_s (kHz)	0.1	1	10	100
L (μH)	101	100.9	100.58	100.63

and its laboratory test setup is shown in Fig. 13. The key parameters of the FSBB converter prototype is given in Table 3.

Table 4 shows the measured inductance with B&K Precision 880 LCR meter. For experiment, the three-segment inductor current mode modulation method based on [18] was chosen. Keysight N2782B current probe with 50 MHz bandwidth was used to measure both the inductor and output current while Keysight N2791A differential voltage probe with 25 MHz bandwidth was used to measure both the gating signal and drain-source voltages. The oscilloscope used was a Yokogawa DLM3034. The negative ZVS current I_0 was chosen to be -3 A, and the dead time was 320 ns. The converter was tested with $V_{in} = 150$ V, $V_{out} = 200$ V and $P_o = 1200$ W. For both ZVS operation and voltage ripple measurement, two sets of operating cases were adopted: the first with $d_1 = 0.8$, $d_2 = 0.4$, and $f_s = 30769$ Hz; and the second with $d_1 = 0.9$, $d_2 = 0.325$, and $f_s = 25876$ Hz. For the first case, I_2 is larger than I_{out} while for the second case, I_2 is smaller than I_{out}.

TABLE 5. FSBB Converter Operating Parameters, $V_{in} = 150$ V, $V_{out} = 200$ V, $P_o = 1200$ W, $L = 100\,\mu$H, $C_{out} = 105\,\mu$F, and $I_0 = -3$ A

Operating Cases	$d_1 = 0.8$, $d_2 = 0.4$, $f_s = 30769$ Hz	$d_1 = 0.9$, $d_2 = 0.325$, $f_s = 25876$ Hz
Input Current I_{in} (A)	8	8
Output Current I_{out} (A)	6	6
Inductor Current I_1 (A)	16.5	15.8
Inductor Current I_2 (A)	10.0	4.7
Calculated ΔV_{pp} (V)	0.94	0.92

Table 5 summarizes the operating parameters of the FSBB converter under these two operating cases.

A. ZVS OPERATING WAVEFORM

Fig. 14 shows the ZVS operating waveforms of the FSBB converter, indicating that ZVS turn-on was achieved for switches S_1, S_2, and S_4. Since the current value I_1 is larger than $|I_0|$, it can be inferred that ZVS turn-on of S_3 was also achieved. Yokogawa WT500 power analyzer was used to measure the efficiency.

B. VOLTAGE RIPPLE

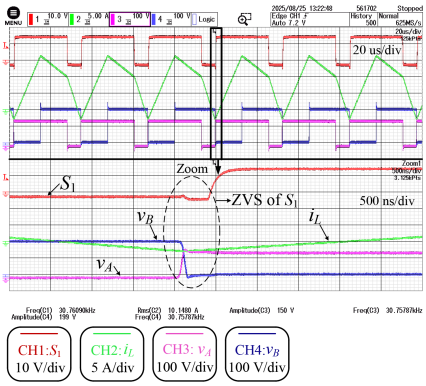
The voltage ripple across the output capacitors was measured and analyzed to validate the proposed analysis. To measure the voltage ripple, the oscilloscope was AC-coupled. Additionally, a 2 MHz low-pass filter was employed to suppress high-frequency noise caused by switching transients. Fig. 15 shows the operating waveforms of the voltage ripple across the output capacitor. As can be seen from Fig. 15, the output current was nearly DC. The output voltage ripple was measured to be approximately 1 V under both operating cases. Based on the theoretical calculations shown in Table 5, the expected output voltage ripple are 0.94 V and 0.92 V for the operating cases shown in Fig. 15(a) and (b), respectively.

1) FURTHER DISCUSSION ON VOLTAGE RIPPLE

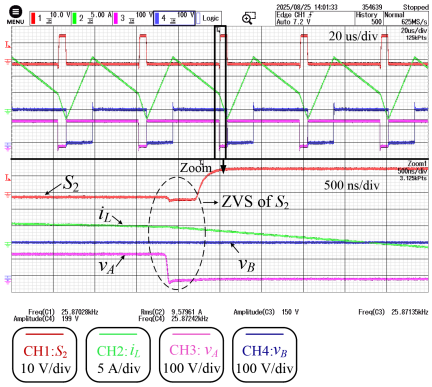
By further checking the output voltage ripple waveform shown in Fig. 15, it can be observed that the positive peak voltage is not equal to the absolute value of the negative peak voltage. For example, Fig. 16 shows the simulation result under steady state from MATLAB Simulink based on the operating parameters in Fig. 15(b). As one can observe, the simulation results of the voltage ripple clearly confirm the previous statement. Furthermore, the simulated peak-to-peak voltage ripple was 0.92 V, which precisely matches the calculated result. In summary, both the experimental and simulation results proved the validity of the proposed analysis.

C. DISCUSSION ON ASSUMPTIONS

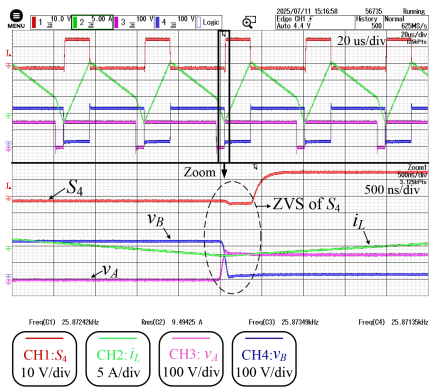
First, during analysis, the dead time was ignored. This is because, on the one hand, the dead time is typically very small relative to the switching period, for example, the ratios of the dead time to one switching cycle are only 0.83% and 0.98% in the experiments presented in this article. On the other hand, the analysis of voltage ripple is based on the variation of capacitor charge, which is the integral of current with respect to time. Therefore, it is reasonable to ignore the impact of circuit resonance during the dead time on the voltage ripple.



(a)

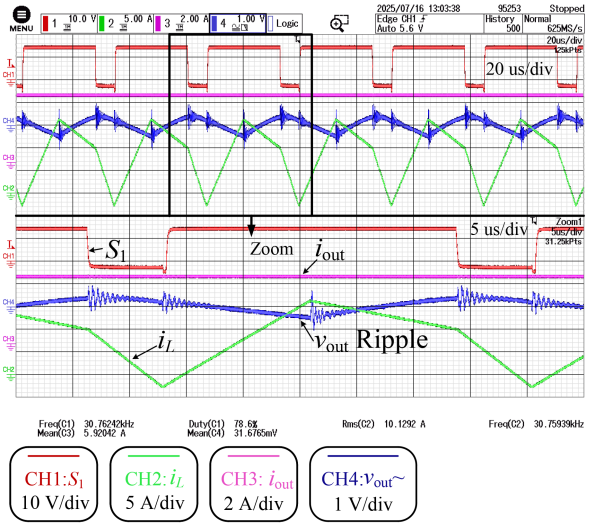


(b)

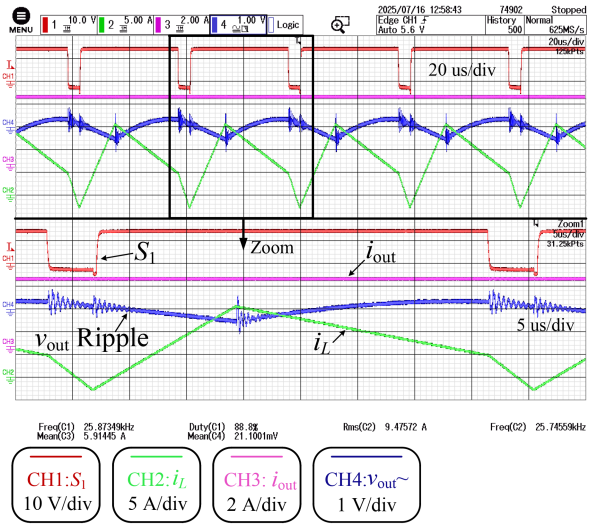


(c)

FIGURE 14. ZVS operating waveforms, $V_{in} = 150$ V, $V_{out} = 200$ V, $I_0 = -3$ A and $P_o = 1.2$ kW. S_1, S_2 and S_4 are the gate-source voltage signals for switch S_1, S_2 and S_4, respectively. i_L is the inductor current, v_A and v_B are the voltages of points *A* and *B* relative to the bottom bus rail shown in Fig. 1. (a) ZVS turn-on of S_1, $d_1 = 0.8$ and $f_s = 30769$ Hz. The efficiency was 98.7%. (b) ZVS turn-on of S_2, $d_1 = 0.9$ and $f_s = 25876$ Hz. The efficiency was 99.0%. (c) ZVS turn-on of S_4, $d_1 = 0.9$ and $f_s = 25876$ Hz.



(a)



(b)

FIGURE 15. Output voltage ripple operating waveforms, $V_{in} = 150$ V, $V_{out} = 200$ V, $I_0 = -3$ A and $P_o = 1.2$ kW. (a) Case when $d_1 = 0.8$, $d_2 = 0.4$, and $f_s = 30769$ Hz. (b) Case when $d_1 = 0.9$, $d_2 = 0.325$, and $f_s = 25876$ Hz.

Second, the inductance was assumed to be a constant. As observed from the experimental inductor current waveforms, within one switching period, each segment of the inductor current was approximately linear, which indicates that this assumption is reasonable. For the built inductor, a PM 74/59 ferrite core made of N87 material was employed. The peak magnetic flux density during converter operation can also be calculated according to $\hat{B} = \dfrac{L\hat{I}}{NA_e}$, substituting corresponding parameters with $L = 100\,\mu$H, $\hat{I} = 16.5$ A, $N = 18$, and $A_e = 790\,\text{mm}^2$ [27], the peak flux density is calculated to be 0.116 T, which is less than the saturation flux density of N87 material [28].

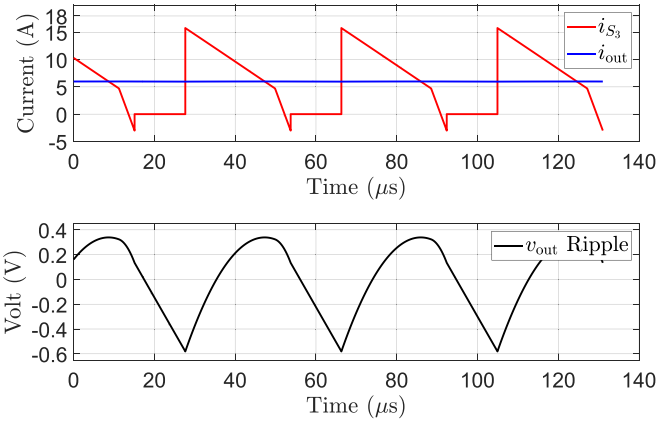


FIGURE 16. Voltage ripple simulation result under steady state based on the operating parameters in Fig. 15(b), namely, $V_{in} = 150$ V, $R_L \approx 33.33\,\Omega$, $d_1 = 0.9$, $d_2 = 0.325$, $f_s = 25876$ Hz, and $C_{out} = 105\,\mu$F.

Third, for the purpose of simplifying the voltage ripple analysis, the ESR of the capacitor is neglected in this article. Incorporating the effects of ESR could be a future research direction.

VI. CONCLUSION

In this article, the peak-to-peak output voltage ripple was comprehensively analyzed in a four-switch buck+boost converter under ZVS modulation strategies. The operating mode of the FSBB converter, along with the relative magnitudes of the output current and inductor current at switching instants, was considered. Four distinct cases were analyzed, and corresponding voltage ripple expressions were derived for each, along with a summary of the capacitor sizing. The analysis was validated by both simulations and experiments. Incorporating the effects of ESR can be a future study to further improve the accuracy of the voltage ripple modeling.

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