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6.2 An Ultrasound-Powering TX with a Global Charge-Redistribution Adiabatic Drive Achieving 69% Power Reduction and 53° Maximum Beam Steering Angle for Implantable Applications

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State-of-the-art intracortical neural recording and stimulation systems rely on subdural implants tethered to a cranial implant which itself has a wireless power and data link to the outside world [1] (Fig. 6.2.1). However, this tethered configuration poses challenges such as scarring and potential damage to the surrounding tissue due to strain and micromotions, making this approach unsuitable for chronical implants [2]. Consequently, there is growing interest in wireless connections between cranial and subdural implants. This paper focuses on wireless powering between implants, traversing the dura and cerebrospinal fluid (CSF) tissue layers over distances of 0.5 to 1cm (transdural powering). With modern burr-hole craniotomy, the hole drilled in the skull is ~6mm in diameter, limiting the available size for the TX. Moreover, the power dissipation of the TX must be low to keep tissue heating below 1°C [3]. RF and optical modalities suffer from higher attenuation in tissue compared to ultrasound (0.6dB/cm/MHz) [4]. Furthermore, for transdural powering, power losses from reflections at medium interfaces (e.g., skull) are avoided, making ultrasound (US) a prime candidate for efficient in-body wireless power transfer. US is also preferable to inductive powering since US beam steering up to large angles (>45°) is needed to maximize power delivery and compensate for brain micromotions of up to ±4mm [5] and misalignment during surgery. However, prior art US driving systems either use single-phase transducer driving [6,7], incapable of beam steering, or use class D drivers with low power transfer efficiency (PTE) [8,9]. A phased array with increased driving efficiency was presented in [10], but it cannot perform beam steering without grating lobes that can be eliminated with miniature transducers with a pitch close to λ/2. To facilitate direct integration between CMOS and the transducer array, the CMOS driving units should also be pitch matched [8,9].

Figure 6.2.1 shows the chip architecture. A beam steering controller with 1.2V supply uses an external 250MHz clock to generate the time delays for the 16 driving units of a 16-element transducer array, implementing beam steering based on the equation in Fig. 6.2.1. The delay between 2 adjacent elements (ΔT) sets the angle. For continuous powering, the delays of all elements can be contained within one US period (wrapped delays). While typical US powering uses <1MHz [10], this work uses ~8MHz such that the natural focus point of the mm-sized transducer array is close to the maximum powering distance. Furthermore, due to small attenuation for sub-cm distance and higher voltage-to-pressure sensitivity (kPa/V) of transducers at higher frequencies, PTE can be improved. However, the smaller pitch further complicates the design of power-efficient pitch-matched driving circuits. To achieve high driving efficiency, adiabatic driving with "global charge redistribution" (GCR) is proposed. Unlike existing adiabatic driving, this method does not require external capacitors for the charge recycling, but leverages the parasitic capacitors of the full transducer array itself. Also, a GCR controller implements beam steering to large angles ensuring GCR. Figure 6.2.2 shows the details of the GCR 16-unit 5-level adiabatic driving circuits implemented with switches S1-S5 that turn on and off sequentially and drive the transducers from V_{DD} US (4.8V) supply. The GCR controller determines the operation of the switches and the delays of all units. The dominant source of power loss in US transducer driving is the energy stored in the equivalent parasitic capacitor C_p of each element. With adiabatic driving, a capacitive load can be charged via intermediate levels (V2-V4). When the load is discharged, the charge Q_i can partially flow back into these levels to be reused in a later cycle, implementing charge recycling [6,10]. Theoretically 75% of the energy can be recycled with 5-level adiabatic driving. While adiabatic driving is well-known, it typically requires large capacitors (C_{ext} in Fig. 6.2.2) on each intermediate voltage level, increasing the implant size beyond volume constraints. However, in theory in a phased array, if 1 element is charging to a specific level (V2, V3 or V4), and at the same time exactly 1 other element is discharging to the same voltage level, charge recycling directly between transducer elements can be achieved [6]. If this happens for all intermediate voltage levels and all elements (GCR condition), then no net charge flows into the intermediate nodes, eliminating the need for C_{ext} and resulting in an area-efficient implementation. However, this has not yet been achieved, such that prior art still requires ~50nF external capacitors [6]. This work proposes a special GCR beam steering scheme, achieving GCR for all non-zero angles and eliminating C_{ext} (Fig. 6.2.2).

A fundamental condition for GCR to apply is that each voltage level (V2-V4) is only connected to exactly one pair of a charging and a discharging element at each time. No two elements in the array should have the same delay, otherwise they would be charging simultaneously to the same level. Setting the delay resolution to $T_{US}/16$ ensures that for ΔT_{min} of 8ns, no delay repetition occurs. Furthermore, if a unit (e.g., V_US16) recycles its C_p at two consecutive intermediate voltage levels with 2 other units (V_US1 for level 2 and V_US2 for level 3), then the duration of these levels should be half of the delay τ between V_US1 and V_US2, i.e., τ/2 (Fig. 6.2.2, right middle). By setting τ equal to ΔT_{min} (8ns), GCR is achieved for the minimum angle. However, by applying a conventional linear beam steering pattern for larger angles, some delays are repeated and not all the elements share their C_p charge with exactly one other element at each intermediate voltage level (Fig. 6.2.2, bottom), making charge redistribution partial and C_{ext} necessary. This is solved with a "delay skipping" scheme, applicable for all ΔT, in which whenever the wrapped delay of a unit is about to be repeated in the 16-unit row, a "-τ" offset is introduced in the delay of this specific unit. It is shown for the example of $\Delta T = 4\tau$ (Fig. 6.2.2) and the necessary delay skips for all ΔT are mentioned in the table in Fig. 6.2.2. It has also been validated that such delay skips do not affect the beam profile (Fig. 6.2.5).

For an 8MHz pitch-matched transducer array the parasitic gate capacitance C_g of the high voltage driving switches is not negligible compared to the transducer C_p (few pF) and becomes a major source of circuit loss. As in [8], the switch driving circuits and the transducers have comparable power consumption. This is a bigger issue in adiabatic driving because more power switches are needed. To overcome this issue, the architecture not only minimizes C_g but also implements charge recycling between the parasitic gate capacitances of the switches. The implementation of the adiabatic driver unit is depicted in Fig. 6.2.3. Switches S1-S3 are implemented with NMOS transistors and S4, S5 with PMOS to minimize the number of switch drivers and allow smaller switch V_{gs}. The control bits (D1-D5) from the GCR controller are level-shifted and buffered to control the switches, drawing current from V_{DDH} (4.8V). Both the power loss for charging and discharging C_g as well as the level shifter power loss are greatly reduced when limiting V_{gs} of the switches S1-S2 and S4-S5 to $V_{DDH}/2$ (Fig. 6.2.3). Thanks to the GCR, charge recycling between C_g happens automatically via $V_{DDH}/2$. If 1 unit has S2 closed, there will be exactly 1 other unit with switch S4 closed (units 3 & 1 at times t_1 & t_3). Similarly, charge recycling between switch S5 of every unit and an S1 of another unit will happen (t_2). Thus, zero net current is drawn from $V_{DDH}/2$ for the switch drivers. These circuit innovations result in a fully integrated 116×116μm² driving unit that is the smallest US adiabatic driving unit and has the lowest power consumption among the state of the art (Fig. 6.2.6).

The chip was fabricated in 65nm CMOS, and the chip micrograph is shown in Fig. 6.2.7. 4 rows of 16 units are implemented, with the 4 units of each column having connected outputs, thus forming 16 TX channels for 1D beam steering. The TX is connected to a PMUT-array chip with a resonance frequency of ~7.8MHz, with each TX channel driving a row of 32 PMUT elements (60μm width and 105μm pitch each). Single channel measurements with PMUT array load (10pF load per channel in water) verify the adiabatic driving (Fig. 6.2.4), while multichannel measurements verify the good delay linearity between channels. The measured power consumption demonstrates that the GCR adiabatic driver technique saves 69% of power from V_{DD} US compared to class-D driving and 46% of power in total, including the power consumed by the adiabatic switch driver (V_{DDH}) and the GCR controller (V_{DDL}). The TX is also compatible with pitch-matched integration with a PZT transducer array for further miniaturization and increased pressure and PTE [9]. Acoustic measurements with the PMUT array in water (Fig. 6.2.5) verify that beam steering at angles of up to 53° is achieved without grating lobes. Figure 6.2.6 compares performance with state-of-the-art US drivers and beam steering arrays.

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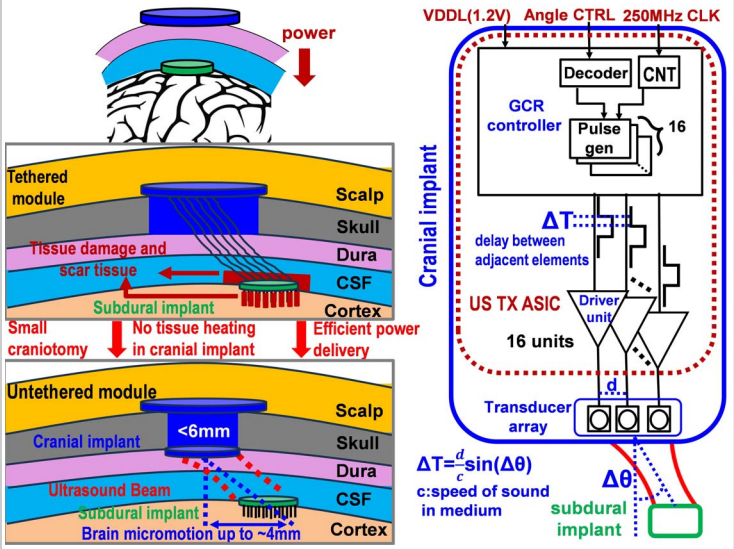


Figure 6.2.1: Simplified block diagram and concept illustration of the proposed transdural powering system.

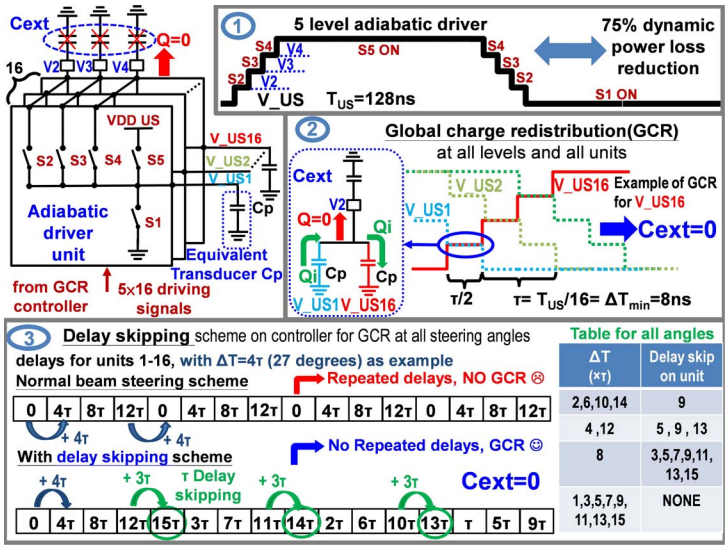


Figure 6.2.2: Simplified schematic and concept illustration of the global charge redistribution adiabatic driver.

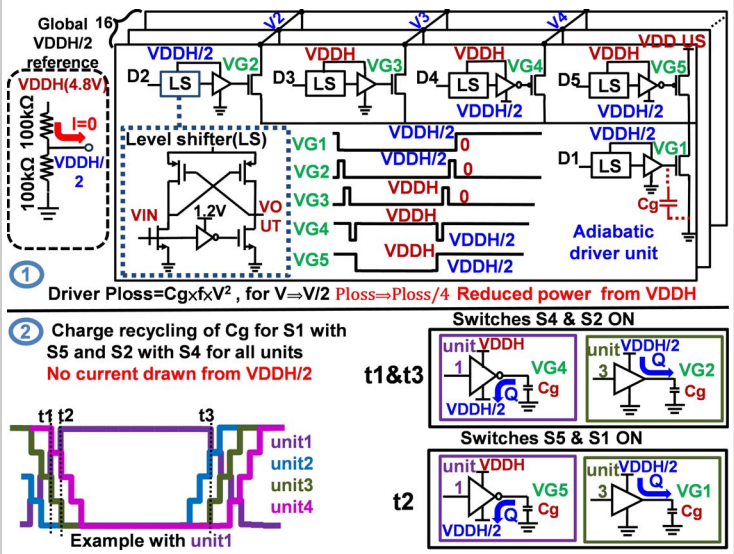


Figure 6.2.3: Simplified schematic of adiabatic driving unit with power-efficient and charge-recycling switch drivers.

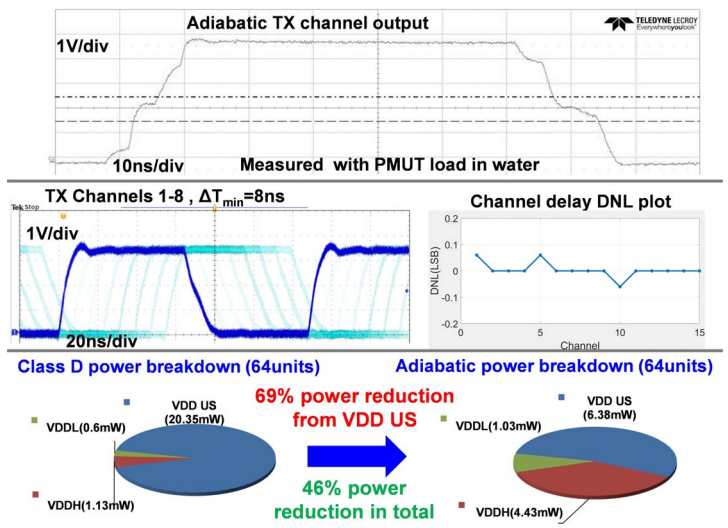


Figure 6.2.4: Measured single-channel adiabatic output, multichannel outputs and power consumption of TX array.

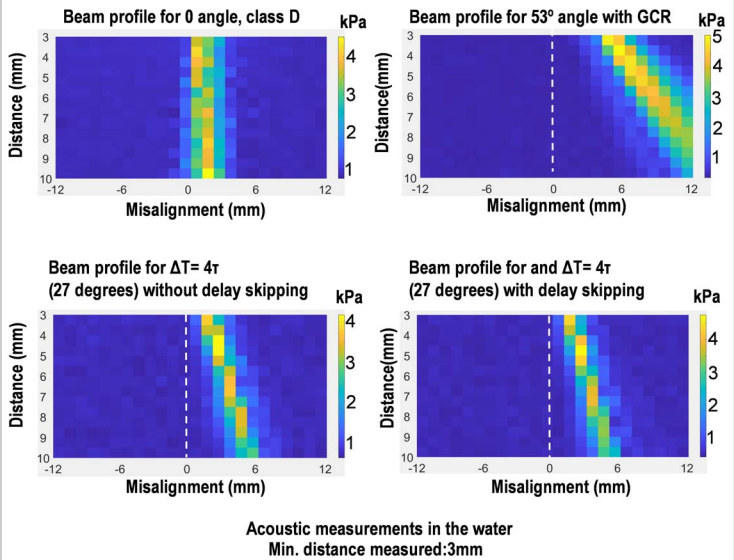


Figure 6.2.5: Acoustic measurements with PMUT array for beam profiles at 0° and 53°, beam profiles with and without GCR.

	This work	[10] So, JSSCC'22	Lee, JSSC'21	[9] Costa, TBioCAS'21	Wu, JSSC' 22	[6] Pelgrims, ESSCIRC'21	[7] Choi, ISSCC'21
	With beam steering				Without beam steering		
Process	65nm	180nm BCD	180nm	180nm	180nm	180nm BCD	180nm BCD
Application	Powering	Powering	Imaging	Powering/ Stimulation	Imaging	Imaging	Imaging
Transducer	PMUT[B]	PZT	PMUT	PZT	PZT	PMUT	PZT
Frequency	7.8MHz	850kHz	5MHz	8.4MHz	40kHz	250kHz	1MHz
Transducer load Cp per unit	2.5pF	125pF	15.4pF	N/A	1.9nF	235pF	820pF
Driving voltage (V)	4.8V	4.5V	13.2V	5V	10V	32V	30V
Scheme	5-level adiabatic	6-level adiabatic	charge redistribution	class D	energy recycling	7-level adiabatic	energy replenishing
#Units	64	6	36	676	64	4	1
Area per unit	**0.013mm²**	0.0536mm²	0.02mm²	0.018mm²	0.035mm²	0.16mm²	5.43mm²
Power consumption per unit	**185μW**	N/A	9.26mW	1.5mW	6.54mW	12.5mW	1mW [E]
Cap. required for driver	**0**	250pF	0[C]	0	>141μF	50nF	0[D]
Dynamic power saving	**69% (46% total)**	N/A	42.6%[A]	0%	44% [A]	80%	73.1%
Max angle without grating lobes	**53 degrees**	0 degree	13 degrees	15 degrees	No beam steering		

[A] PMU power consumption not included [B] also compatible with pitch-matched integration with PZT array
[C] capacitance of PMU not included [D] 1 off-chip inductor is used [E] power consumption for duty cycled operation

Figure 6.2.6: Summary and comparison table of state-of-the-art ultrasound drivers and beam steering arrays.

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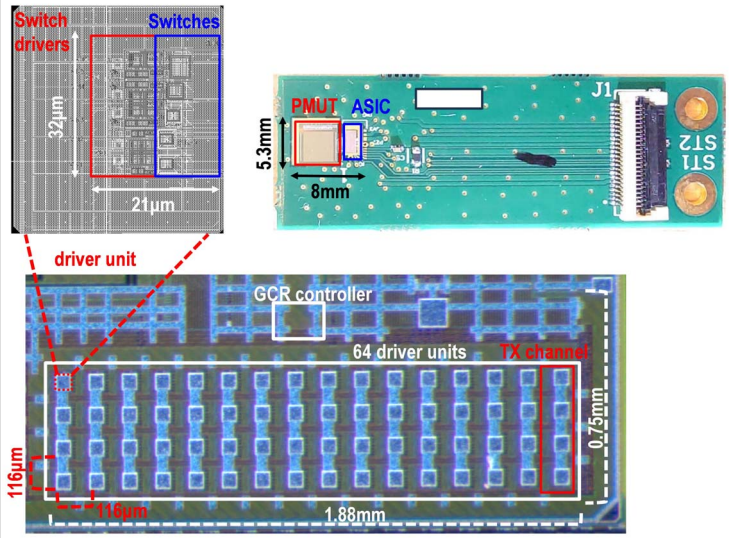


Figure 6.2.7: Chip micrograph, unit layout and ASIC to PMUT connection.

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