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A 121.7-dB DR and −109.0-dB THD+N Filterless Digital-Input Class-D Amplifier With an HV IDAC Using Tri-Level Unit Cells

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***Abstract*— The dynamic range (DR) of digital-input closed-loop class-D amplifiers (CDAs) is typically limited by the noise introduced by their resistive DAC (RDAC) or current-steering DAC (IDAC). It could be improved by using tri-level cells in the IDAC, but this has not yet been realized in high-voltage (HV) CDAs due to the large difference in the common-mode levels between the DAC and the CDA. This article describes an HV CDA directly driven by an HV IDAC. By using the same output common mode for the digital-to-analog converter (DAC) and CDA, the noise penalty associated with shifting the common mode is avoided. To address the distortion due to mismatch and intersymbol interference (ISI) in the IDAC, a transition-rate-balanced bidirectional real-time dynamic element matching (RTDEM) technique is also introduced. Fabricated in a 180-nm BCD process, the CDA prototype achieves a DR of 121.7 dB and a peak THD+N of −104.0 and −109.0 dB for 1- and 6-kHz inputs, respectively. It can deliver a maximum of 14 W into an 8-Ω load with a power efficiency of 90%.**

***Index Terms*— Class-D amplifier (CDA), digital-to-analog converter (DAC), dynamic element matching (DEM), intersymbol interference (ISI), pulsewidth modulation (PWM).**

I. Introduction

DIGITAL-INPUT class-D amplifiers (CDAs) have gained widespread use in contemporary audio systems due to their ability to achieve high power efficiency through a switching output power stage, coupled with the high level of integration and robustness to external interference offered by digital-input interfaces [1], [2], [3], [4], [5], [6], [7], [8], [9], [10].

Despite its simplicity, the open-loop architecture suffers from high clock jitter and supply sensitivity [3], [6]. To address this, typically, the output stage of these amplifiers is incorporated into a feedback loop to mitigate distortion and supply sensitivity. In this architecture, the current-steering DAC (IDAC) or resistive DAC (RDAC) driving the analog loop plays a critical role in the CDA's noise and distortion. Moreover, to interface the DAC with the high-voltage (HV) CDA, pull-down resistors have been used in the feedback network, which adds noise and boosts the noise gain of the opamp in the first integrator of the loop filter [1], [11], as shown in Fig. 1(a).

In [12], a digital-feedback HV CDA is presented, where the CDA output is directly sensed by a low-voltage (LV) $\Delta\Sigma$ ADC without resistive attenuation, as shown in Fig. 1(b). This is achieved by drawing a large amount of current through the feedback resistor using the differential-mode (DM) IDAC inside the $\Delta\Sigma$ ADC. To ensure high linearity, the IDAC output voltage should be fixed, which is realized by a common-mode (CM) control loop based on a CM IDAC. Thanks to the high output impedance of the IDACs, the loop filter's noise is no longer boosted, but the use of a CM control loop still introduces additional noise.

Another way to bridge the CM difference between the DAC and CDA output stage is to operate the DAC and the loop filter in an LV voltage domain floating around half of the HV output stage supply [13], as shown in Fig. 1(c). However, generating the floating supply rails using linear regulators will lead to high power loss due to the large dropout voltage, while using charge pumps or inductor-based dc–dc converters requires extra external components.

Efforts have been made to address the challenges associated with the resistive-feedback CDA architecture by using capacitive feedback instead [10], as shown in Fig. 1(d). While capacitive feedback offers benefits in noise reduction by eliminating the contribution from the feedback network, it requires an *LC* filter for operation. Otherwise, the CDA's rail-to-rail output pulses would directly saturate the loop filter's capacitively couple front-end stage [14]. Therefore, capacitive feedback cannot be used in filterless applications where cost and size reduction are prioritized.

Another approach to improving a closed-loop CDA's dynamic range (DR) is to drive the analog loop directly with an IDAC based on tri-level unit cells [8]. This is because, at low

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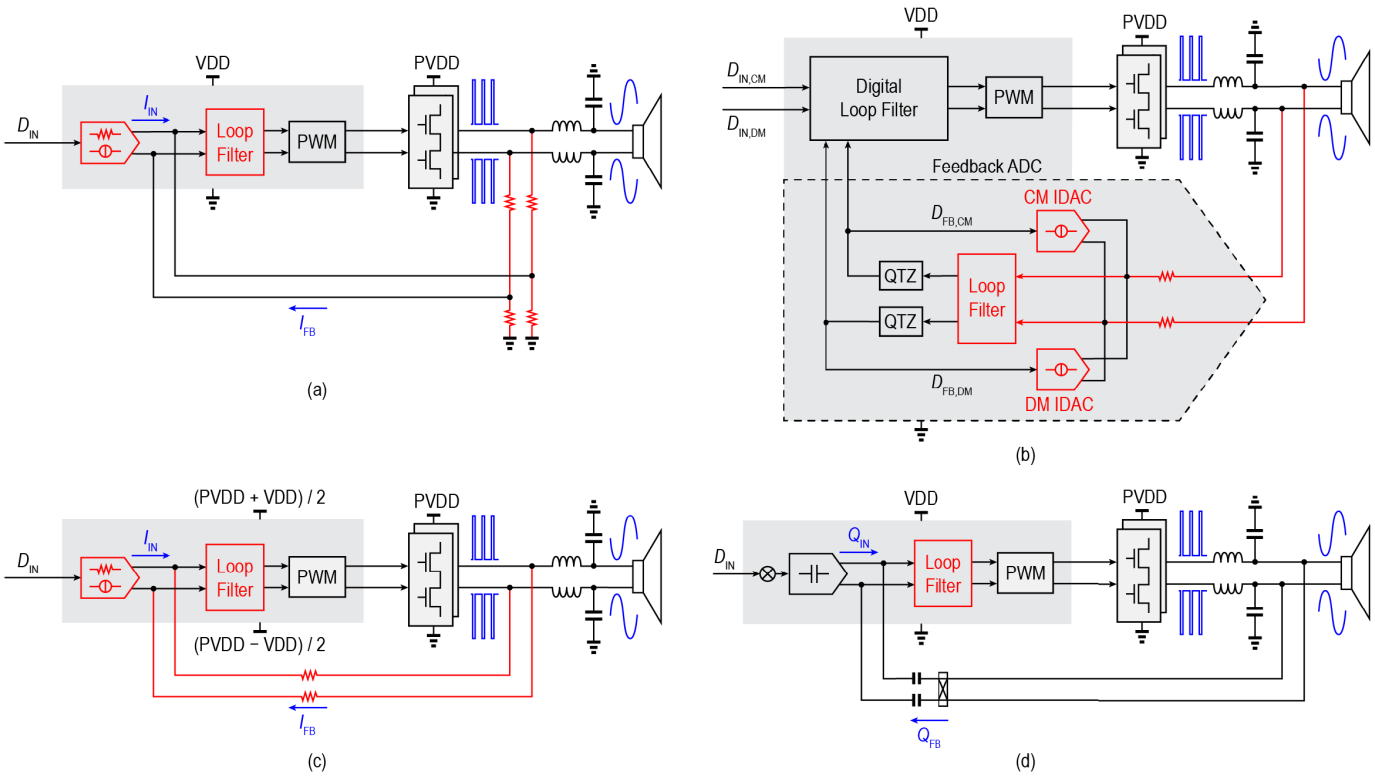

Fig. 1. Prior HV closed-loop digital-input CDA architectures using (a) pull-down resistors, (b) CM IDAC, (c) floating LV voltage domain, and (d) capacitive feedback to reduce the loop filter input CM voltage. Major noise sources are highlighted in red.

signal levels, a large portion of the IDAC current, hence its noise, does not enter the loop filter [15]. Furthermore, with unity-gain feedback around the CDA loop, the noise gain of the opamp in the first integrator to the CDA output is unity. However, the inherent inter-symbol interference (ISI) and mismatch issues associated with tri-level current-steering cells pose challenges in achieving high linearity [15], [16], [17]. Moreover, Matamura et al. [8] target a headphone application with both the DAC and the CDA output stage operating from the same 1.8-V supply, limiting the maximum output power below 100 mW. Driving an HV CDA with LV tri-level IDAC cells would require CM regulation at the DAC output since the latter has no control over its output CM in the zero state. However, the noise introduced by the CM regulation circuitry would then negate the noise benefit of tri-level IDAC cells.

This work aims to extend the use of tri-level IDAC cells to higher power filterless CDAs and achieve a DR beyond 120 dB with state-of-the-art linearity. A 14.4-V supply is employed to deliver up to about 10 W into an 8-Ω load, necessitating the DAC to drive into an output CM of about 7.2 V. In addition, a transition-rate-balanced real-time dynamic element matching (RTDEM) scheme is introduced to mitigate distortion due to mismatch and ISI of the tri-level IDAC cells.

This article is an extension of [18] and is organized as follows. Section II provides an overview of the CDA architecture. Section III discusses the transition-rate-balanced RTDEM technique. Circuit implementation of the HV IDAC is presented in Section IV, while that of the rest of the CDA is presented in Section V. Section VI presents the measurement results, and Section VII concludes this article.

II. HV IDAC-Based Filterless CDA

Fig. 2 shows an overview of the HV IDAC-based filterless CDA of this work. The audio input is upsampled by 16× to $f_S = 768$ kHz and is then truncated to 5 bits using a sixth-order delta-sigma modulator (DSM) with an out-of-band gain (OBG) of 2.8 in the digital domain. This process yields a peak signal-to-quantization noise ratio (SQNR) of 130.9 dB and a maximum stable amplitude of −0.4 dBFS. The 5-bit quantization enables a signal-to-noise ratio (SNR) of 129 dB in the presence of 10 ps of jitter on the sampling clock.

Subsequently, the output of the digital DSM drives the digital-to-analog converter (DAC) through the dynamic element matching (DEM) logic. It ensures the DAC's linearity in the presence of mismatch and ISI, which will be elaborated in Section III.

The DAC output is directly connected to the virtual ground node of the first integrator of the closed-loop CDA. Since the CDA output stage nominally employs a 14.4-V supply, the CM voltage at the virtual ground is about 7.2 V. Since no CM current flows through the pair of feedback resistors R_{FB}, the CDA's PSRR is no longer limited by their mismatch [19], [20] and is determined by the CMRR of the OTA in the first integrator.

The analog feedback loop comprises three integrators, offering a total loop gain of 70 dB within the audio band. This configuration effectively suppresses distortion from the output stage, which has a simulated open-loop total harmonic distortion (THD) of about −40 dB, to below −110 dB. An inner feedback path to the third integrator is introduced to stabilize

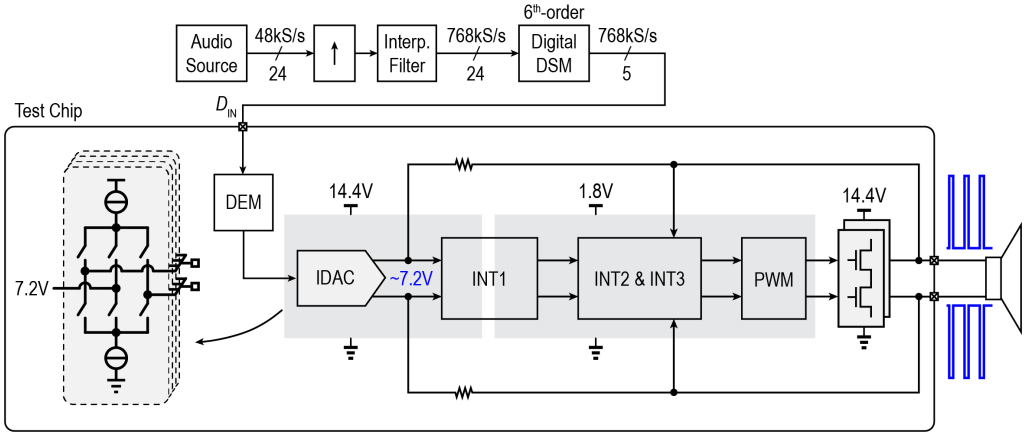

Fig. 2. Architecture of the proposed HV IDAC-based CDA.

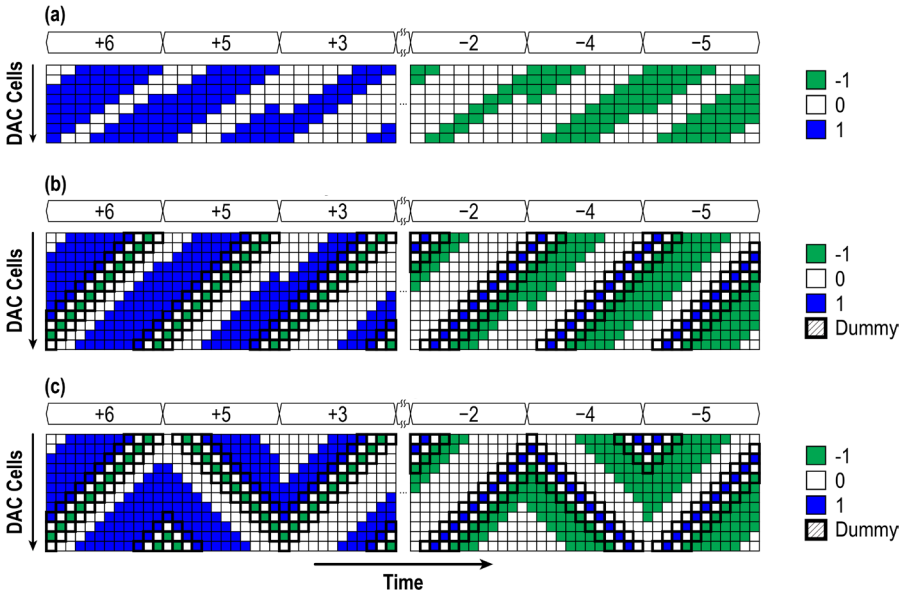

Fig. 3. Usage pattern of DAC unit element (a) if the conventional RTDEM was directly applied to a tri-level-cell-based DAC, (b) with dummy patterns added to conventional RTDEM, and (c) with the proposed bidirectional RTDEM and dummy patterns. A 3-bit example is illustrated for simplicity.

the loop. The input CM of the third integrator is set below 1.8 V by a resistive network. More details will be presented in Section V.

The output stage employs fixed frequency pulsewidth modulation (PWM) with fully differential switching (also known as AD modulation [21]) to maintain a constant CM output for the CDA. This ensures that the IDAC connects to a fixed output CM voltage. It operates at a PWM frequency $f_{\text{PWM}} = 3f_S = 2.304$ MHz. This choice avoids quantization noise foldback due to the PWM operation [1] and situates the PWM tone above the AM radio band, mitigating electromagnetic interference (EMI) [22], [23].

III. Transition-Rate-Balanced RTDEM

DEM is essential for achieving state-of-the-art linearity in this work. Various DEM techniques have been proposed for IDACs based on tri-level cells [15], [16], [17]. However, it is challenging to achieve a THD below −100 dB due to the ISI issue associated with tri-level cells [8], [17]. In [15] and [17], extra switches are introduced to disconnect the DAC from the subsequent amplifier during DAC transitions, but they would be complicated to implement given the 7.2-V DAC output CM of this work, and the switching action could alias PWM sidebands to the audio band.

The DEM logic of this work is based on the RTDEM technique [24]. It operates by dividing each sampling period into several sub-intervals, corresponding to the total number of DAC cells. During the first sub-interval of each sampling period, a thermometer code is loaded into the DAC. Subsequently, in each subsequent sub-interval, this thermometer code is shifted by one position. This approach ensures that after completing a full sampling period, a complete rotation occurs, with each DAC cell contributing equally to the output. Notably, RTDEM mitigates the idle tone issue often encountered in other DEM techniques (e.g., data-weighted averaging, DWA) [25].

While RTDEM aligns well with a low oversampling ratio (OSR), applying it directly to tri-level cells, illustrated in Fig. 3(a), presents challenges with nonlinear ISI error and residual mismatch, which will be discussed next.

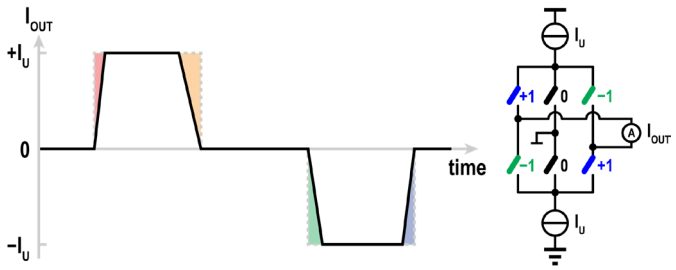

Fig. 4. Asymmetric ISI errors for different input polarities due to DAC switch mismatch.

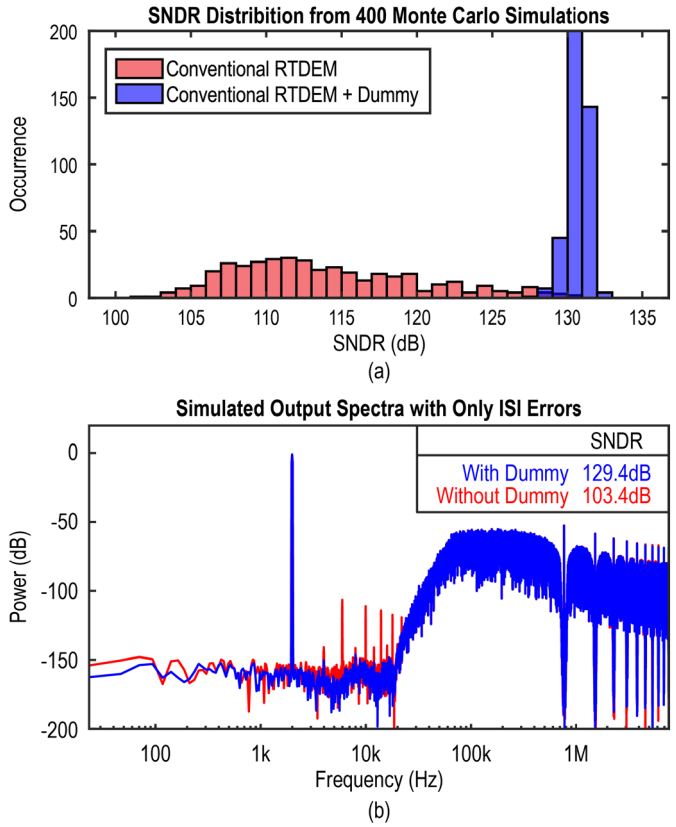

Fig. 5. (a) SNDR distribution of 400 Monte Carlo simulations with ISI mismatch only. (b) Simulated DAC output spectra from two of the cases with relatively low SNDR.

A. Input-Polarity-Dependent ISI

In an IDAC based on tri-level cells, when the input data are positive, each cell only switches between the +1 state and the zero state and similarly between the zero state and the −1 state for negative input data. Since these are controlled by different switches, the switching transients, i.e., ISI, are subject to the mismatch of the switches depending on the input polarity, as illustrated in Fig. 4. Monte Carlo simulations are carried out to evaluate the effect of switch mismatch. The DAC switches employ a minimum size for high speed and minimal loading on the level shifters driving them, which will be discussed in Section VI-B. The THD variation and an FFT from one of the runs are shown in Fig. 5 in red. The worst case THD due to ISI mismatch is approximately −102 dB.

To address this distortion, this work introduces dummy patterns to the thermometer code. As illustrated in Fig. 3(b), for input data ≥0, a dummy pattern of (+1, 0, −1, 0) is appended at the end of each thermometer code, while for negative input data, (0, +1, 0, −1) is added at the beginning, which requires four extra DAC cells. The RTDEM process translates the vertical dummy pattern into the time domain. As a result, transitions to and from −1 are added to each input sample ≥0 and vice versa for each input sample <0. Fig. 5 also shows the simulated residual ISI distortion in the presence of switch mismatch after introducing the dummy patterns in blue, which is about −130 dB. The extra DAC cells outputting "+1" and "−1" will introduce some extra noise, but this is 5.5× less than the thermal noise introduced by the rest of the CDA.

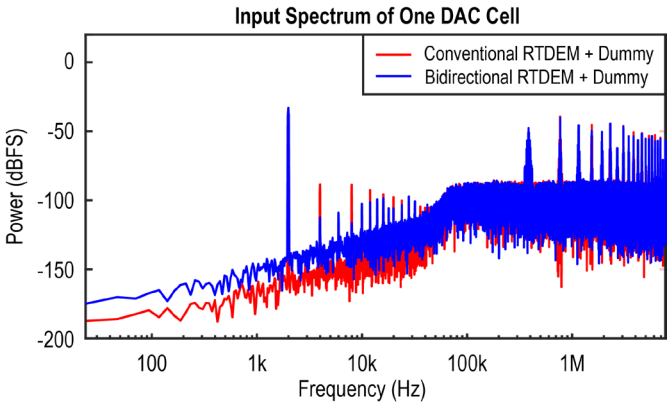

Fig. 6. FFT spectra of the input of one DAC cell controlled by conventional and bidirectional RTDEM.

B. Unit-Current-Source Mismatch

Even though, in the RTDEM technique, each DAC cell contributes to the output equally over a sampling period, their timing is signal-dependent. It turns out that this leads to some residual distortion [24]. This is because the pulse driving each DAC cell is essentially single-sided PWM pulses with frequency components at harmonics of the input frequency, due to the intermodulation between PWM and high-frequency DAC images. Furthermore, the DAC cell input contains out-of-band quantization noise, which can be demodulated to the signal band by the aforementioned intermodulation and degrade the noise floor, as shown in Fig. 6(a) in red. If the DAC cells were matched perfectly, the harmonics and demodulated noise of all DAC cells add out-of-phase and cancel each other perfectly at the DAC output. In reality, mismatch makes the cancellation imperfect, leading to some residual harmonic distortion.

It has been shown that double-sided PWM exhibits lower harmonic distortion compared to single-sided PWM [26]. Inspired by this, a bidirectional RTDEM algorithm is introduced in this work, by flipping the direction of rotation for every input sample. The resulting DAC element usage pattern is shown in Fig. 3(c). Fig. 6 compares the input spectra of one DAC cell when it is controlled by the RTDEM schemes of Fig. 3(b) and (c). Note that, in Fig. 6, no circuit non-ideality is included since it shows the spectrum of a DAC cell's input, which is a digital signal. The harmonics and elevated noise floor are introduced by the RTDEM algorithms, not by any

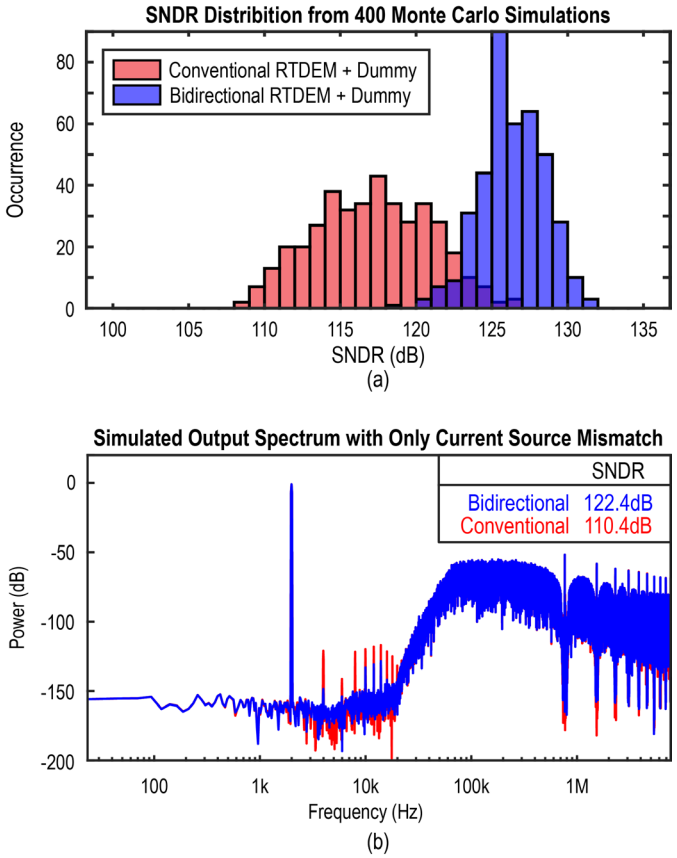

Fig. 7. (a) SNDR distribution of 400 Monte Carlo simulations with current source mismatch only. (b) Simulated DAC output spectra from two of the cases with relatively low SNDR.

circuit imperfections, which will contribute to the output due to the abovementioned imperfect cancellation. As expected, the DAC cell input exhibits lower input harmonics when controlled by the bidirectional RTDEM. However, having opposite directions of rotation for the input samples in odd and even clock cycles demodulates some more quantization noise from around $f_S/2$. Monte Carlo simulations with mismatched current sources indicate a significant improvement in the SNDR by approximately 12 dB, as shown in Fig. 7. The higher HD5-7 follows the same trend in Fig. 6 due to the abovementioned imperfect cancellation. Furthermore, according to simulations, the quantization noise leakage due to mismatch for the proposed bidirectional RTDEM only degrades the SQNR by about 2 dB, which is acceptable.

IV. HV IDAC Implementation

This section details the circuit design of IDAC, which is required to interface an output CM voltage of 7.2 V. The design of unit current sources, bias noise filter, and the level shifters driving the DAC switches will be described.

A. Unit Current Source

The current source in the DAC must support a high headroom due to the 7.2-V CM output. To mitigate potential overstress issues, HV LDMOS transistors could be employed, which would consume a large area due to their large isolation rings. Instead, source degeneration with 270-kΩ resistors is implemented in this work, which also effectively lowers the flicker noise and thermal noise of the DAC, as shown in Fig. 8. The current sources further include 1.8-V core transistors cascoded by 5-V I/O devices. Two HV isolation tubs can then be shared by all the nMOS and pMOS current sources, avoiding the need for repeated isolation structures for individual DAC cells. For optimal linearity, the IDAC's PVDD supply is bonded out separately from that of the CDA's output stage to avoid the supply bouncing caused by the latter's high di/dt switching activities.

B. Bias Noise Filter

In IDAC designs, the biasing circuitry often introduces considerable noise, through V_{BN} and V_{BP} in Fig. 8. To address this, in [27] and [28], bias noise filters with very low cutoff frequencies are created using a sample-and-hold technique and off-transistors, respectively. Implementing the sample-and-hold technique of [27] in this HV DAC would require additional level shifters to drive the switches, and implementing the technique of [28] would require HV opamps. For simplicity, this work employs a passive noise filter, as shown in Fig. 8. Polysilicon resistors are used instead of off-transistors for less PVT sensitivity.

The noise filter is optimized using MATLAB. Its output-referred noise and area consumption are first obtained based on the simplified circuit model in Fig. 9(a) and PDK data, respectively. In Fig. 9(a), R_S and $V_{N,S}$ represent a Thevenin model for the circuitry to the left-hand side of V_{BN} in Fig. 8. $V_{N,R1}$ and $V_{N,R2}$ are the noise introduced by the resistors in the noise filter. Then, A-weighting is numerically applied to the bias filter's output noise in MATLAB. The A-weighted noise and filter area are then fed into the MATLAB function *fmincon*. It iteratively finds the R and C values for minimal A-weighted noise at the output of the bias noise filter. An area constraint of 0.05 mm^2 is applied. Fig. 9(b) shows the A-weighted noise output noise and area of the noise filter from 100 iterations. The design point highlighted in red ($R_1 = 29$ MΩ, $R_2 = 99$ MΩ, $C_1 = 1.1$ pF, and $C_2 = 62$ pF) is chosen for the final design. In the actual layout, the noise filter is placed in an HV isolation tub, leading to a total area of 0.065 mm^2 each, thus a total area of 0.13 mm^2, occupying 1.7% of the total die size. The worst case 3-dB cutoff frequency across PVT variations is 31 Hz.

C. Level Shifters

Given the 7.2-V output voltage of the current DAC, level shifters are required to interface the DEM logic and DAC switches. Employing the same level shifters as in the CDA's HV output stage such as [23] and [29] would occupy a large area due to the large LDMOS transistors and the large number of DAC cells. For the DAC in this work, as shown in Fig. 8, two floating voltage domains are created above and below the 7.2-V output CM voltage to control the pMOS and nMOS DAC switches, respectively. These voltage domains are buffered by 5-pF on-chip metal–insulator–metal (MIM)

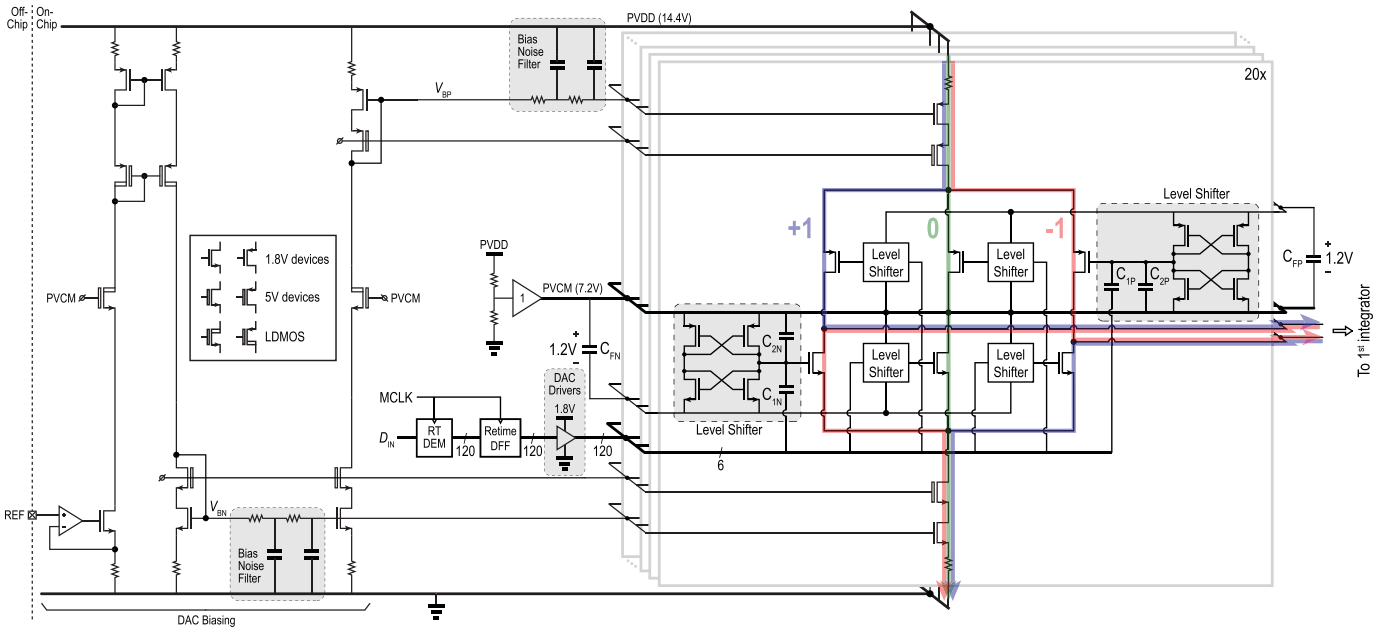

Fig. 8. Schematic of the IDAC of this work with HV tri-level unit cells, including biasing circuitry.

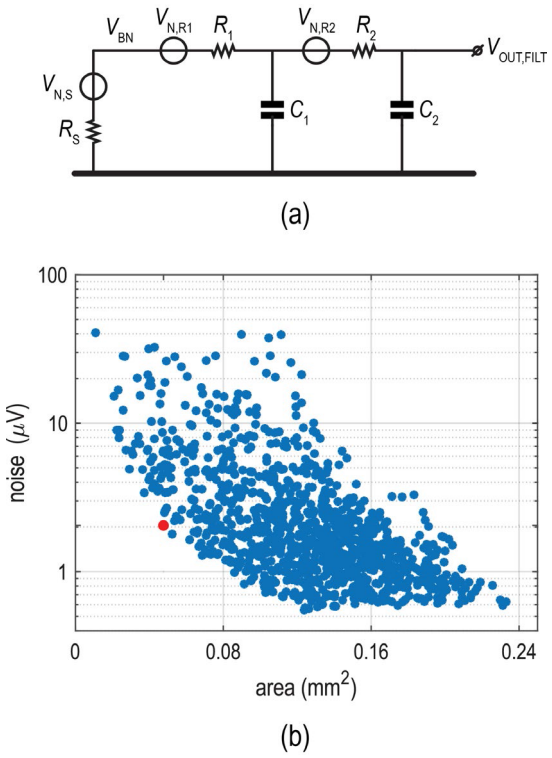

Fig. 9. (a) Circuit model for the bias filter's noise analysis. (b) A-weighted output noise and area of the bias noise filter from 100 iterative solutions in MATLAB.

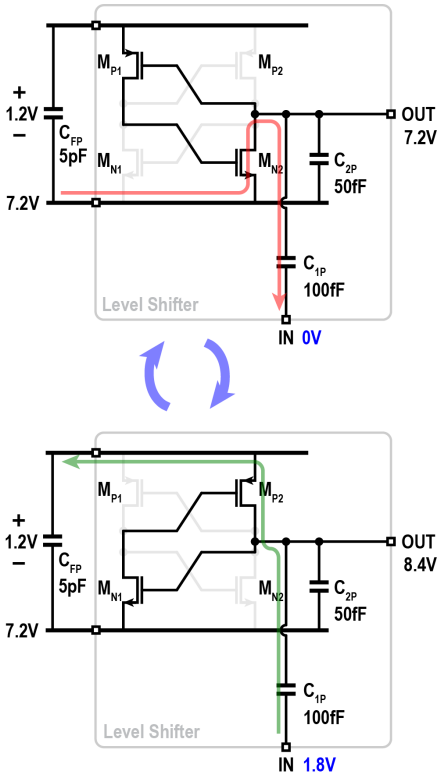

Fig. 10. Automatic refreshing of C_{FP} by the level shifters.

capacitors C_{FP} and C_{FN}, stacked on top of active circuitry to minimize the area overhead.

Each level shifter incorporates a latch to receive and hold the DAC control voltage through a dc level-shifting capacitor $C_{1N/P}$ (= 100 fF). Compared to the cross-coupled differential level shifter in [30], the number of dc level-shifting capacitors is reduced by half. Furthermore, to reduce the kickback onto the output node of the current sources, which is also the source nodes of the switches, the latch outputs are loaded by $C_{2N/P} = C_{1N/P}/2 = 50$ fF, reducing the gate swing of the DAC switches from 1.8 to about 1.2 V.

The DAC drivers, level-shifting capacitors, and latches also function as charge pumps to generate and maintain the voltages across the two floating voltage domains. For example,

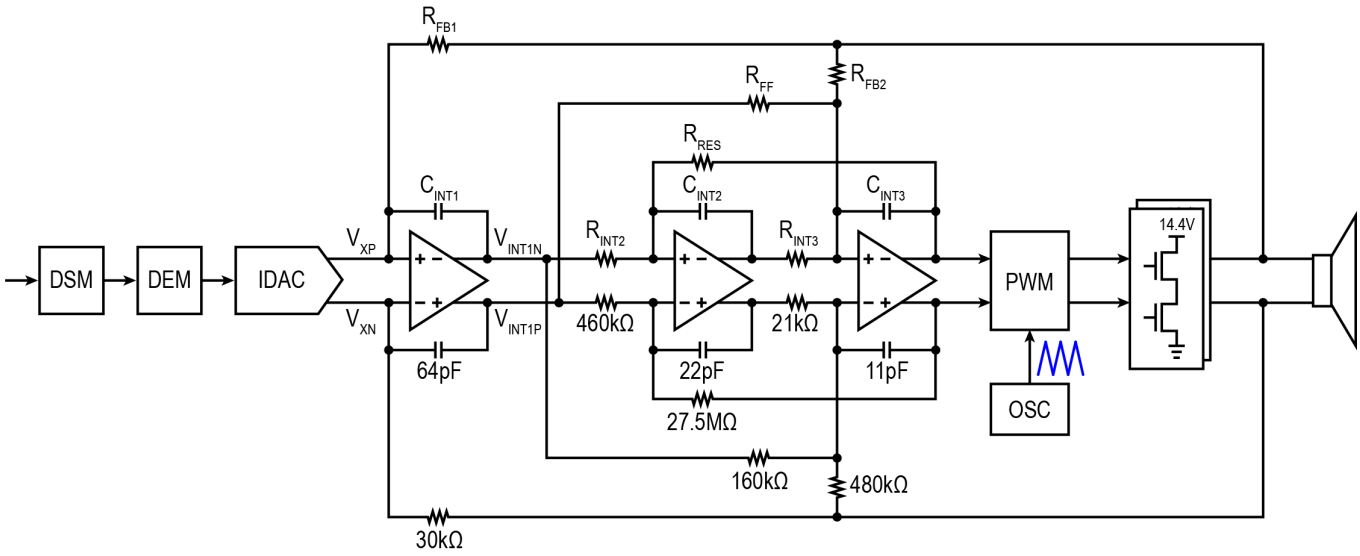

Fig. 11. Top-level schematic of the HV IDAC-based CDA.

as illustrated in Fig. 10, for the level shifter driving the pMOS DAC switches, when the DAC driver outputs low, M_{N2} is turned on by M_{P1}, and C_{1P} is connected across PVCM (= 7.2 V) and ground. When the DAC driver output goes high, M_{P2} is turned on by M_{N1}, and the charge in C_{1P} is pumped into C_{FP} through M_{P2}. Thanks to the transition-rate-balanced RTDEM, the total number of latches toggled during every input sample period, and thus, the refresh rates of C_{FP} and C_{FN} are insensitive to the input signal. No extra circuitry is required to set the voltages across C_{FP} and C_{FN}.

V. Class-D Amplifier Implementation

Fig. 11 shows the top-level implementation of the closed-loop CDA. The third-order loop filter employs a cascade of integrators with feedforward and feedback (CIFF-B) structure [31] since it suppresses the audio-band output swing of the first integrator, relaxing its linearity requirement. Furthermore, it offers second-order low-pass filtering of out-of-band quantization noise, which could otherwise increase the signal swing in the CDA. The loop is stabilized by a feedforward path through R_{FF} and an additional feedback path through R_{FB2}. The input CM of the OTA in the third integrator is set by the resistive network consisting of R_{FB2}, R_{FF}, and R_{INT3} to about 1.1 V, so no extra CM shifting circuitry is required here. The noise contribution of R_{FB2}, R_{FF}, and R_{INT3} is insignificant since it is suppressed by the gain of the first two integrators.

The feedback resistor to the first integrator is chosen to be 30 kΩ, so its integrated noise is below −126 dBFS. Fig. 12 shows the simulated noise breakdown of this CDA. Thanks to the tri-level DAC cells, the total A-weighted noise with zero input is about 6 dB lower than that with a −1-dBFS input. As mentioned in Section III-A, the DAC units still introduce some noise at zero input due to the dummy patterns.

Fig. 13 shows the first integrator's OTA (A_1), which is tasked with handling a 7.2-V input CM voltage. This is achieved by cascoding the input differential pair, which operates from the 14.4-V supply, with HV pMOS transistors.

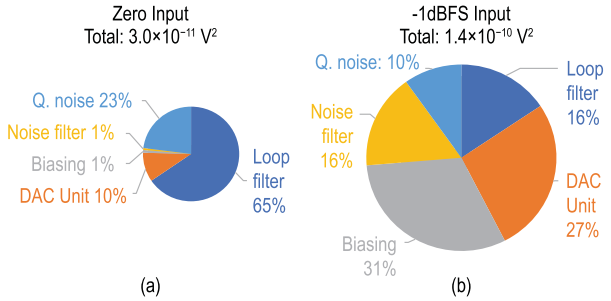

Fig. 12. Simulated noise breakdown of this CDA with (a) zero input and (b) −1-dBFS input.

As mentioned in Section II, in this architecture, the first integrator's CMRR is crucial for the CDA's PSRR. The first stage's tail current source is cascoded to provide a CMRR of about 100 dB. A_1 adopts the two-stage feedforward compensation from [23], [29], and [32], with the second stage g_{m2} and feedforward stage g_{m3} reusing the output stage bias current and operating in the 1.8-V domain. The OTAs in the rest of the loop filter reuse the same design from [23] and [29].

The pulsewidth modulator with on-chip triangle wave generation from [29] is used, and the CDA output stage is based on [20]. To ensure that $f_{\mathrm{PWM}} = 3f_{\mathrm{S}}$, as mentioned in Section II, the triangle wave oscillator is placed in a phase-locked loop as in [10].

VI. Measurement Results

A prototype of the designed circuit was fabricated in a 180-nm BCD process, occupying an area of 7.9 mm^2. Fig. 14 shows a microphotograph of the die. The output stage operates from a 14.4-V supply, while the majority of the loop filter and other digital blocks operate from a 1.8-V supply. For flexibility in testing, the digital interpolation filter and DSM were implemented on an FPGA.

As shown in Fig. 15, when the CDA drives 1 W into an 8-Ω load with a 1-kHz sinewave input, the measured THD+N

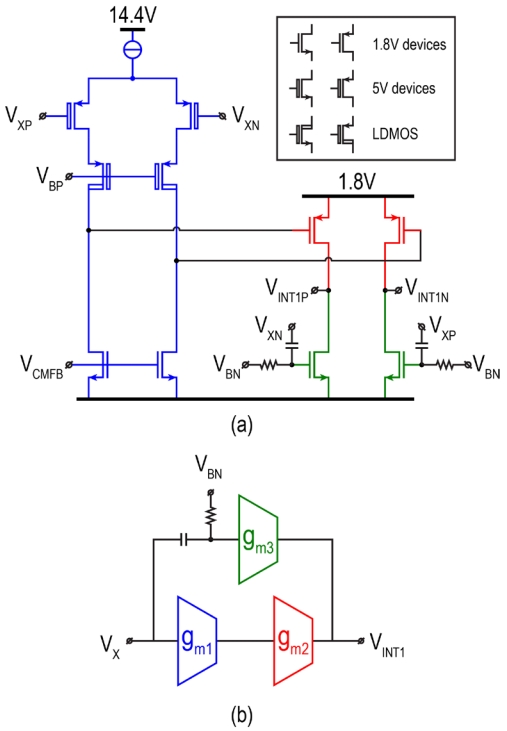

Fig. 13. Amplifier A_1 in the first integrator using an HV input stage. (a) Schematic. (b) Macromodel.

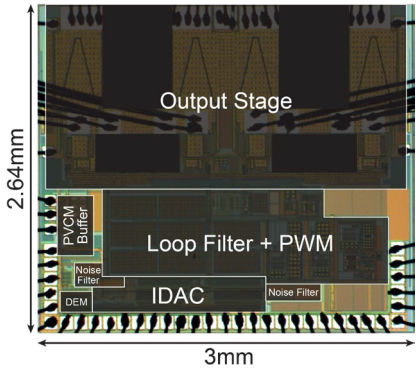

Fig. 14. Die micrograph.

is −102.3 dB, with an SNR of 111.1 dB. Lowering the input to −60-dBFS yields an SNR of 61.7 dB, indicating a DR of 121.7 dB.

To analyze the cause of the high HD2 in Fig. 15(a), an empty-load test is performed. An FFT is shown in Fig. 16. The HD2 is much lower compared to Fig. 15(a), and the THD is −121.7 dB. Therefore, the high HD2 is likely due to the interference to the DAC reference in the PCB setup under high output current.

Fig. 17 shows the THD+N recorded while sweeping the input amplitude. For a 1-kHz input, a peak THD+N of −104.0 dB is achieved, while for 6 kHz, the peak THD+N reaches −109.0 dB.

Fig. 18 shows the measured power efficiency across output power. A peak power efficiency of 90% is achieved at 14 W, where the CDA outputs a (clipped) sinewave with 10% THD.

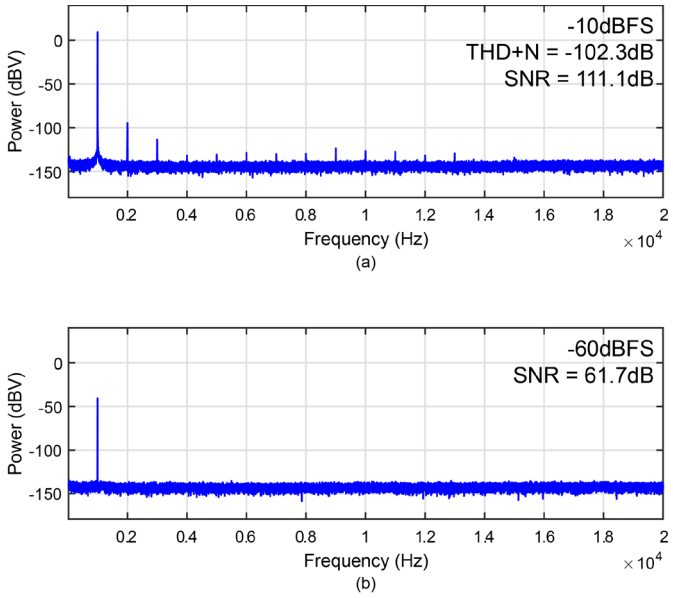

Fig. 15. 128k point 4×-averaged FFT spectra of the CDA output with (a) −10-dBFS and (b) −60-dBFS input sinewaves at 1 kHz.

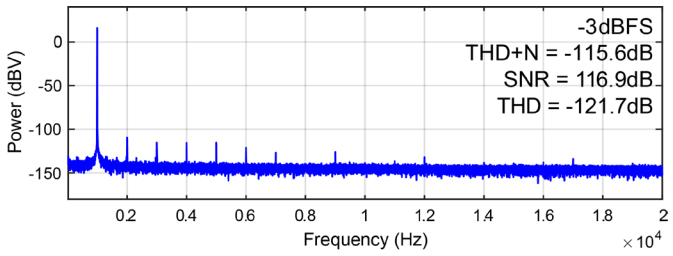

Fig. 16. 128k point 4×-averaged FFT spectrum obtained from an empty-load test with a −3-dBFS input.

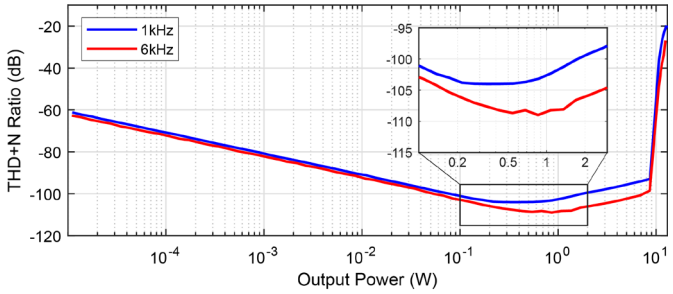

Fig. 17. Measured THD+N at the CDA output across output power.

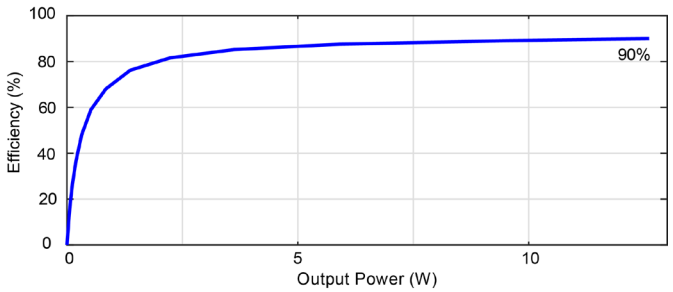

Fig. 18. Measured power efficiency versus output power.

The PSRR is measured by superimposing a 2-V peak-to-peak sinewave onto the supply. The measured PSRR of the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART DIGITAL-INPUT HV CDAS

	This Work	[10] Zhang JSSC 2023	[8] Matamura ISSCC 2021	[11] Cope ISSCC 2018	[12] Schinkel JSSC 2017	[1] Ido ISSCC 2006	[33] ADI SSM3582A	[34] Cirrus Logic CS35L45
Process	**180 nm BCD**	180 nm BCD	40 nm CMOS	180 nm BCD	140 nm BCD	-	-	-
Area (mm^2)	**7.9**	7.5	1.33	4.3	-	23(1)	-	6.5
DAC Cell Type	**Tri-level IDAC**	CDAC	Tri-level IDAC	RDAC	2-level IDAC	2-level IDAC	-	-
Supply (V)	**14.4**	14.4	1.8	8~20	25	35	4.5~16.5	2.5~15
R_{LOAD} (Ω)	**8**	8/4	16	8	4	4/6/8	8/4	8
$P_{OUT,MAX}$ (W)	**12.7**	13/23	0.086	20	80	130/99/74(1)	18/32	6.8
Efficiency	**90%**	90%/86%	93%	90%	>90%	81%(1)	94%/91%	88%
$I_{Q,PVDD}$ (mA)	**22**	13.9	0.68	20.5	-	-	12.3	-
A-wt. Output Noise (μV_{RMS})	**8**	9.3	-	20	34	-	36	5
DR (dB)	**121.7**	120.9	113	115.5	115	113	109	-
Peak THD+N (dB) @ 1kHz	**-104.0**	-111.2/ -106.6	-93	-97.2(2)	-88.6	-94.9	-94(2)	-79
Peak THD+N (dB) @ 6kHz	**-109.0**	-	-90	-97.7				
PSRR (dB) (Freq./Hz)	**93~71 (20~20k)**	97~78 (20~20k)	94 (1k)	80~50 (20~20k)	88~60 (100~20k)	-	88 (1k)	-
Support filterless operation?	**Yes**	No	Yes	Yes	Yes	Yes	Yes	Yes

(1) Output stage is off chip
(2) Extracted from figure

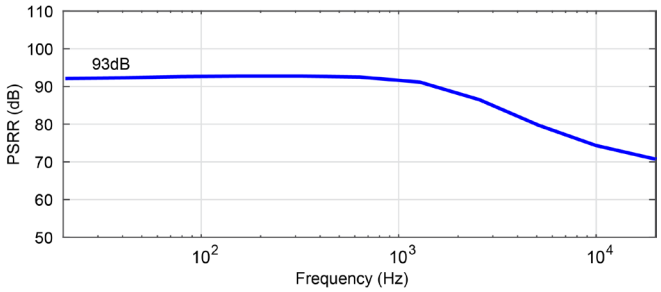

Fig. 19. Measured PSRR across this audio band.

prototype CDA is shown in Fig. 19, indicating a value of 93 dB at low frequencies, which remains above 70 dB at 20 kHz. This is attributed to the absence of CM voltage drop across feedback resistors in the CDA architecture.

Table I summarizes the performance of this HV IDAC-based CDA and compares it with the state-of-the-art works [1], [8], [10], [11], [12], [33], [34]. By incorporating an IDAC with tri-level cells on an HV CDA, this work achieves a DR improvement of approximately 6 dB and a THD+N improvement of about 7 dB compared to the state of the art. Meanwhile, competitive performance metrics in power efficiency, idle power, and PSRR are demonstrated. The quiescent current is relatively high due to the placement of f_{PWM} above 2 MHz, which could be further improved. Multilevel output stages with a constant output CM [6], [29], [35], [36] could be explored to reduce the EMI.

VII. CONCLUSION

This article presents an HV CDA design utilizing tri-level IDAC cells and implementing a transition-rate-balanced bidirectional RTDEM technique to address mismatch and ISI challenges. Achieving a DR of 121.7 dB and a peak THD+N of −104.0 and −109.0 dB for 1- and 6-kHz inputs, respectively, the Class-D amplifier also demonstrates competitive power efficiency, idle power consumption, and PSRR.

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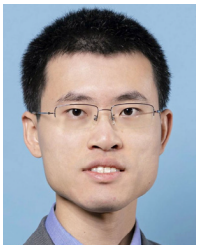

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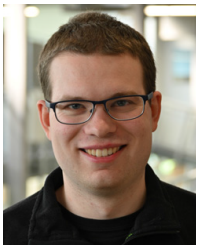

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