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Wafer-level direct bonding of optimized superconducting NbN for 3D chip integration

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ABSTRACT

3D integration has well-developed for traditional CMOS technology operating at room temperature, but few studies have been performed for cryogenic applications such as quantum computers. In this paper, a wafer-to-wafer bonding of superconductive joints based on niobium nitride (NbN) is performed to demonstrate the possibility of 3D integration of superconducting chips. The NbN thin films are deposited by magnetron sputtering. Its high critical temperature (15.2 K) is achieved by optimizing the sputtering recipe in terms of N_2 flow rate and discharge voltage. Wafer-level bumping is bonded by the thermo-compression method. The sheet resistance of the thin film and the contact resistance of the joints are measured by the Greek-cross (4-point Kelvin method) and daisy chain structures at cryogenic temperature, respectively. Direct-bonding wafers with NbN superconductive joints avoid using adhesive layers and the bonding interface could still present superconducting electrical connections in a cryogenic environment above 4 K, which will allow us to use a smaller and high-cooling power cryostat. The contribution of this work could lead to the fabrication of multi-layered superconducting chip that operates beneficially in cryogenic temperature, which is essential in building scalable quantum processors.

1. Introduction

Superconducting integrated circuits (SIC) surpass complementary metal–oxide–semiconductor (CMOS) in the computing domain with many advantages including faster switching speed, low power dissipation, and information transfer at limited software complexity [1]. SIC fabrication process has been developed to encompass a wide range of applications such as radiation detectors [2], digital electronics [3], quantum metrologies [4], magnetic field sensors and ultra-low-noise amplifiers [5]. However, the necessity of cooling to and operating at cryogenic temperatures makes SIC difficult to apply in practice. One of the challenges in this technology is the lack of integration schemes that meet the stringent requirements of cryogenic applications. 3D integration has been widely used in semiconducting devices due to smaller package size, higher interconnection density, and better performance [6]. Introducing the superconducting 3D integration technology opens up a new window into the future commercial product like quantum computers.

As the field of superconducting quantum computing advances from the few-qubit stage to large-scale devices, scalability requirements will necessitate the use of standard 3D packaging and integration processes. 3D integration of qubits has advantages of signal delivery perpendicular to the plane of 2D circuit, locally confining electromagnetic, suppressing substrate modes and layer coupling. Besides, 3D integration approach shrinks superconducting computing hardware to small enough area to fit in a cryogenic chamber and decrease electrical resistance in the signal path, which increases the processing speed [7]. In addition, large-scale qubit arrays would require integration of high density I/O connections to external control circuits. The challenges include the development of flexible routing of control wiring and readout circuitry from the qubit arrays [8]. In traditional integrated circuits, flip-chip bonding with ball grid arrays (BGA) is used for routing of a large number of I/O connections from the chip to external circuits. It has advantages in comparison to wire bonding including better thermal and electrical performance, higher density I/O capability and wafer-scale bump process development. Other advantages include minimising switching noise in sensitive

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signal paths and shielding the I/O bumps from noises by other components [9]. However, such industrial technique is yet to be developed with superconducting materials for integration of qubit arrays.

Standard CMOS flip-chip bonding involves the formation of solder bumps on wafer scale using solder alloys of Sn/Ag/Cu. These conventionally used solders are not superconducting and cannot be used for integration with qubit arrays. In addition, at cryogenic temperatures, these solders will undergo a ductile to brittle transition due to a phase change, resulting in powder-like material and thus catastrophic failure of electronic components. Even worse, the coefficient of thermal expansion (CTE) mismatch between Si and metal bumps may prohibit cryogenic use. For compatibility with qubit fabrication, bump bonds and under-bump metal with superconducting material needs to be developed for providing lossless electrical connection between chips and low thermal losses.

Up to now, there are a few demonstrations of 3D chip structures that are potentially used for integration of multiple superconducting qubits. Google scientists demonstrated a daisy chain pattern to show the superconducting connection between the bottom surface of the top chip and surface of the base substrate [10]. They used indium as a conducting adhesive to stick two chips together. Other groups used indium bumps to bond two separate chips [7,11,12]. Indium is a good superconducting material for wafer bonding at cryogenic temperature, due to its good wettability, low melting point, and softness at low temperature. However, the critical temperature (T_c) of indium being 3.4 K which means it is suitable for superconducting qubits, but not high enough for other cryogenic systems that operate above 4 K. The high critical temperature will allow use of much smaller cryostat system with a significantly higher cooling power. Besides, extra layer of adhesives used to join two neighbouring planes create potential issues. First, one general challenge in wafer bonding is making accurate alignment. Adding an extra layer increases the degree of misalignment. Hence it is not suitable for applications, e.g. silicon quantum dots, that fine pitch and small size are desired. Second, the way adhesive works is that it needs to be melted first, the molten adhesive forms a certain alloy with its neighbouring material and then it cools down and re-crystallizes. This whole process is, to a certain extent, uncontrollable in size [13].

In this work, NbN is chosen to be the skeleton for 3D structure due to its high T_c, simple composition and relatively easy fabrication. We will first describe the procedure of producing high T_c superconductive NbN films by sputtering. After patterning the film with test structures, we will bond two wafers with NbN films as joints without the extra adhesive layer by the thermo-compression direct-bonding method. Then we will discuss the methods and results to optimize the critical temperature of the film. Finally, we will provide results of the sheet resistivity of the film and the contact resistance of the joints. This work shows the potential of direct-wafer bonding in 3D chip integration working at cryogenic environment.

2. Experimental procedure

2.1. NbN thin-film deposition by PVD

The NbN films are deposited on 400-μm *p*-type (100) Si wafers in a cryo-pumped magnetron sputtering system (Trikon Sigma 204). The target is 99.95% pure Nb and the reactive gas is N_2. The volume of the whole chamber is about 24 liters. Distance between a circular shape Nb target and the Si substrate is about 5.2 cm. Before each deposition, the Nb target is cleaned using a specialized recipe to remove target surface contamination including a nitride layer that accumulated in the earlier process. The cleaning procedure could remove the notorious hysteresis during deposition. Then the platen temperature is set at 350 °C and the Ar flow rate is 100 sccm. The stabilization time is set long enough (174 s) for the plasma to reach equilibrium before the discharge voltage and chamber pressure are noted down. The N_2 flow rate changes for each deposition ranges from 0 sccm to 100 sccm in order to achieve a high critical temperature of the film.

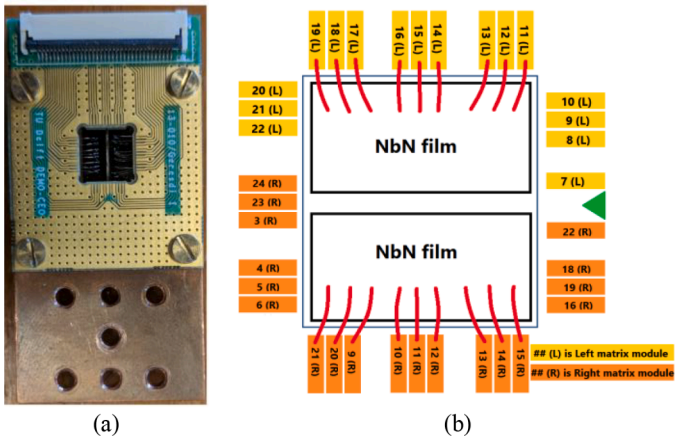

Fig. 1. (a) Sample of the NbN film glued to the PCB and (b) the wire-bonding scheme.

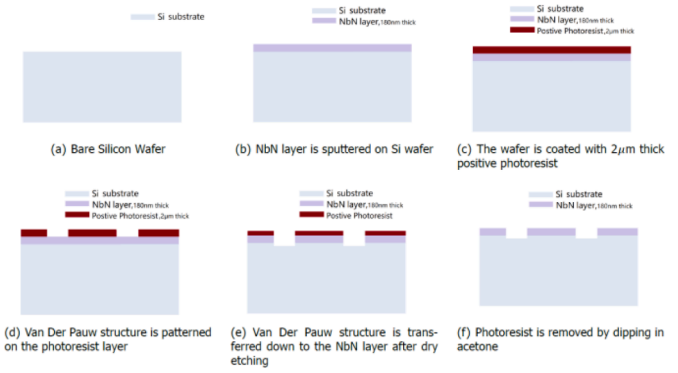

Fig. 2. Schematic of Van der Pauw structure fabrication process for measuring sheet resistance of NbN.

2.2. Dicing and wire bonding

The deposited NbN films are diced and mounted on a small printed circuit board (PCB) to measure its critical temperature in the cryogenic environment (Fig. 1(a)). Silver paste is used to improve the thermal conductivity between the substrate of the sample and the PCB. The sample surface is connected to the pads on PCB using aluminium wires. In principle, 4 wires are needed to conduct Kelvin resistance measurement; as shown in Fig. 1 (b), more wires are bonded in practice to backup failed bonds due to incomplete wielding. The PCB is then hooked to the end of a dipstick which will be later immersed in liquid *He*.

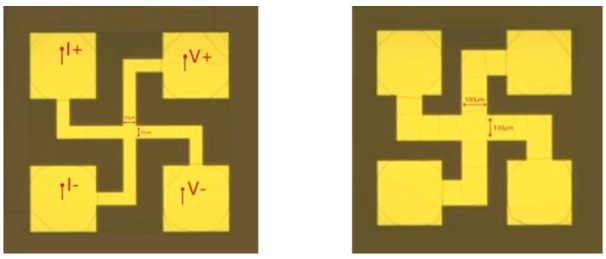

Fig. 3. Van Der Pauw structure of 180 nm-thick NbN film with central square size of (a) 50 μm × 50 μm, (b) 100 μm × 100 μm.

Fig. 4. (a). Illustration of the wafer bonder (b) Top and bottom wafers loaded on the platens.

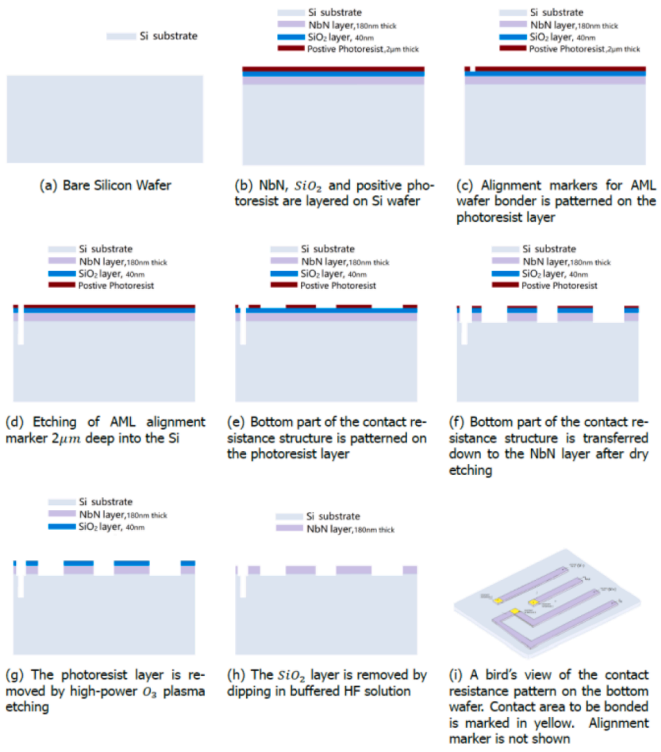

Fig. 5. Fabrication of contact resistance pattern on the bottom wafer.

2.3. Sheet resistance

The Van der Pauw structure is fabricated for characterization of sheet resistance of NbN films. The fabrication process is illustrated in Fig.2 in sequence from (a) to (f). The NbN film is coated with 2 μm-thick positive photoresist. The photoresist is then patterned to give the Van Der Pauw structure. The patterning is a two-step process that includes exposure in AMSL PAS 5500/80 stepper and development. After patterning, the wafer is dry-etched in Trikon Omega 201 to transfer the pattern from the photoresist layer down to the NbN layer. Once the etching is done, the photoresist is removed by dipping the wafer in acetone for 10 minutes.

Fig. 3 shows the Van Der Pauw Pattern of two different central square sizes. Trails of the underdeveloped photoresist are still attached to the pattern surface, but it does not influence the measurement.

2.4. Wafer bonding of NbN by thermo-compression

Thermo-compression bonding is a technique to achieve wafer bonding by inter-diffusion of metal atoms with the aid of elevated temperature and pressure. Fig. 4(a) illustrates working principle of the wafer bonder that a heater acts on the bottom platen. Once both wafers get into contact during bonding, the temperature of the upper platen will also rise. A motor controls the bottom platen with horizontal adjustment for alignment and vertical adjustment for force application. In order to

Fig. 6. Fabrication of contact resistance pattern on the top wafer.

align the patterns on the wafers, two holes are drilled for microscope inspection. Infrared light is employed to enable a penetrating view of the patterns on double-side polished wafers. For wafer loading, the top wafer is fixated by a mechanical clamp and the bottom wafer is just

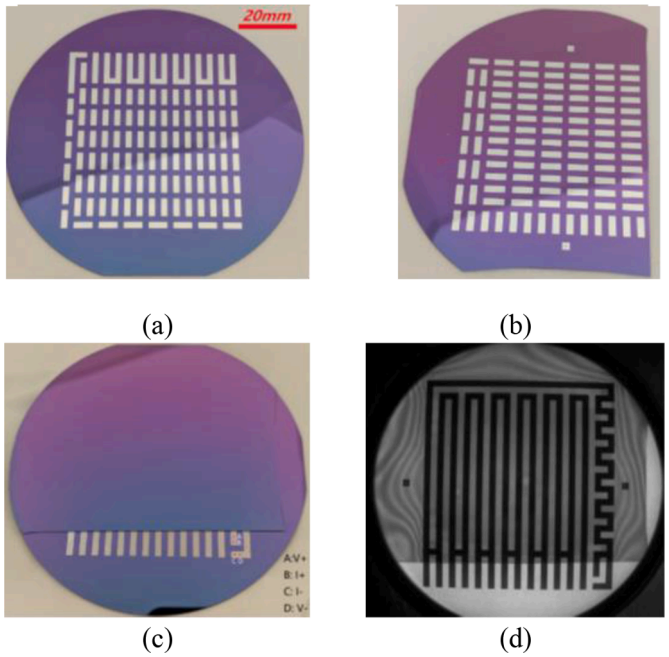

Fig. 7. Wafer-scale daisy chain pattern on the (a) bottom wafer, (b) trimmed top wafer and (c) bonded wafers. (d) Infrared light inspection of bonded wafers.

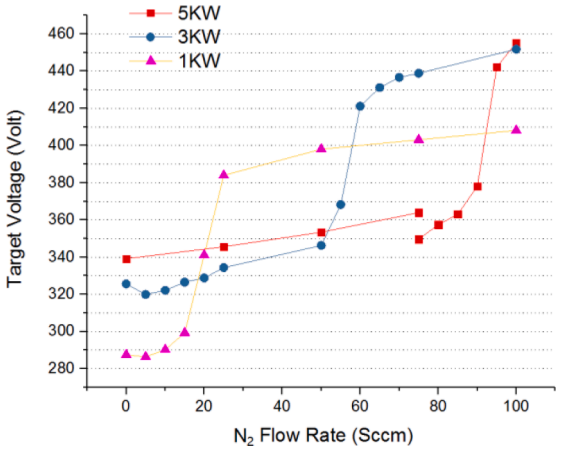

Fig. 8. Discharge voltage as a function of N_2 flow rate at target powers of 1 kW, 3 kW and 5 kW. The platen temperature is 350 °C and the Ar flow rate is 100 sccm.

placed as normal (Fig. 4(b)). Once the vacuum of 10^{-4} mBar is achieved in the chamber, the bottom platen can be pushed up to contact the top platen. The bonder of our experiment can provide temperature and pressure up to 550 °C and 15 kN.

2.5. Contact resistance

Daisy chain resistance was adopted to test the contact resistance of the bonding interface. In Figs. 5 and 6, the fabrication process of the contact resistance pattern on the bottom and top wafer are presented. In a daisy chain structure, test current flows through many stripes and contact spots. The total resistance of the daisy chain depends on the length of the circuitry, the bulk resistivity of constructing materials, and the contact resistivity at the bonding interface. The purpose of implementing a wafer-scale daisy chain pattern is to easily and quickly extract macroscopic contact resistance.

Fig. 7(a) and (b) shows the bottom and top wafers with respective

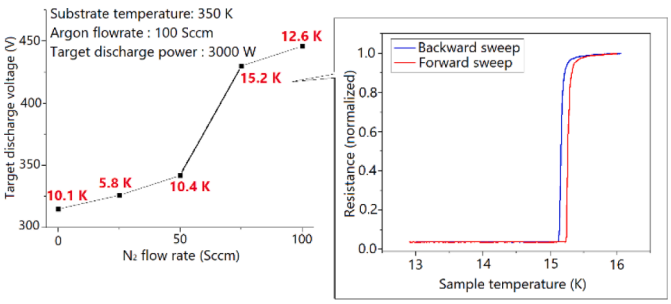

Fig. 9. Target discharge voltage as a function of N_2 flow rate with measured T_c attached. Subplot gives the normalized resistance versus computer-controlled sweeping temperature.

daisy chain patterns and Fig. 7(c) shows the bonded wafers by thermo-compression. Both wafers are double side polished for the infrared light inspection. As shown in Fig. 7(d), the rectangular patterns from the top wafer aligns perfectly with those on the bottom wafers.

3. Results and discussion

3.1. Superconducting temperature of NbN films

In order to produce high T_c NbN film by reactive sputtering, the partial pressure of N_2 inside the chamber plays an important role as it controls the target surface to be either in metallic state or nitrided (poisoned) state. Depositing high-T_c NbN film requires the target to be kept in a fixed 'transition' state between the purely metallic and poisoned state consistently.

Fig. 8 gives the data to find the transition point between the two states. The figure shows the target voltage in the deposition chamber as a function of the N_2 flow rate for different discharge powers. As can be clearly seen, given a certain discharge power, a steep slope shows up in the curve as N_2 flow rate reaches a certain amount. For 1 kW, the abrupt slope change happens when N_2 flow rate is around 25 sccm; for 3 kW around 60 sccm and for 5 kW around 90 sccm. The mechanism behind this phenomenon is that as N_2 becomes abundant in the chamber, NbN film is not only formed on the substrate as desired, but also on the sputter target. Since NbN is less conductive than pure Nb, the target poisoning causes the discharge current to decrease while the discharge power is held constant and lead to a sharp increase in target voltage. As the discharge power increases, the ion flux hitting the target becomes stronger, making it more difficult for NbN to accumulate on the target surface. Therefore, to reach the poisoned state of the target, more N_2 needs to be injected into the chamber, which explains why the sharp slope appears at a larger dose of N_2 for higher discharge power.

Fig. 9 picks 5 points from the 3 kW curve in Fig. 8 and additionally attaches the result of T_c measurement of NbN films. The film superconductivity is measured at temperature ranges between 4.2 K and 20 K, reached by fixing the sample on one end of the dipstick and immersing it in a dewar of He^4. As can be seen, films that are deposited under the elevating N_2 flow rate first show an increase and then decrease in T_c, and the film that exhibits the highest T_c (15.2 K) are located right at the steep slope of the curve of discharge voltage versus N_2 flow rate. This conforms to the theory that at the transition state of the target, deposited NbN film exhibits the highest critical temperature [14,15].

The subplot in Fig. 9 shows the resistance measurement of the sample with maximum T_c deposited at 75 sccm N_2 flow rate. The temperature is swept from 13 K to 16 K. The resistance is normalized to the resistance at 16 K where superconductivity surely vanishes. Since the temperature sensor measures the temperature of the PCB rather than the sample, there is always the curve hysteresis during measurement. The real T_c of the sample should be in between the uprising points of two curves which is 15.2 K. Notice that at 0 sccm of N_2 flow rate, the deposited film is not

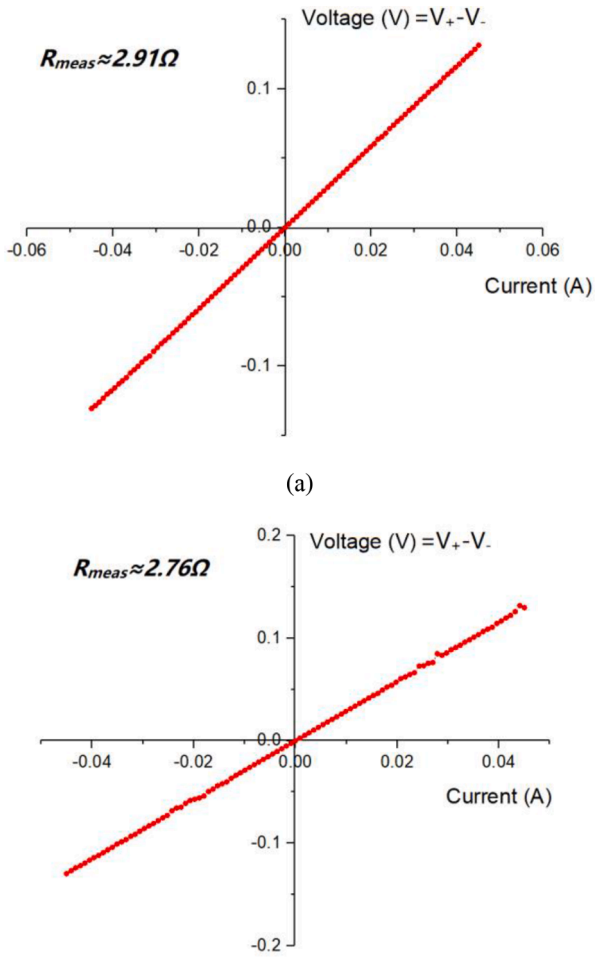

Fig. 10. I-V curves of Van Der Pauw structure made of NbN with center size of (a) 50 μm × 50 μm, (b) 100 μm × 100 μm.

NbN but pure Nb. Nb is also a superconductor and its T_c is reported to be around 10 K. So, it should come with no surprise that the T_c of pure Nb is higher than that of a poorly stoichiometric NbN deposited at N_2 flow rate of 25 sccm.

3.2. Wafer bonding of NbN by thermo-compression

Direct bonding of NbN film to NbN film by the thermo-compression method was demonstrated in Section 2.4. Two Si substrates sputtered with 180 nm thickness NbN films are first placed inside AML wafer bonder for thermo-compression bonding, with 500 °C heating on both plattens and applied force of 2 kN for 40 h. Next, the bonded wafer pair is placed into a furnace for annealing. The annealing temperature is 1100 °C and the duration is 3 h. Annealing at high temperature could greatly enhance the bonding strength, since the annealing temperature reaches almost half of the melting point of NbN. The breaking and forming of Niobium-Nitrogen chemical bonds happen in high frequency, and the diffusion of Nb and N atoms across the interface dominates wafer-bonding process.

3.3. Sheet resistance of thin film NbN

Fig. 10 depicts the room-temperature NbN resistance measured from Van der Pauw structures. In principle, the sheet resistance is independent of the square size; but the measured resistance have shown slightly decrease with the increasing of the center square size [16]. It can also be

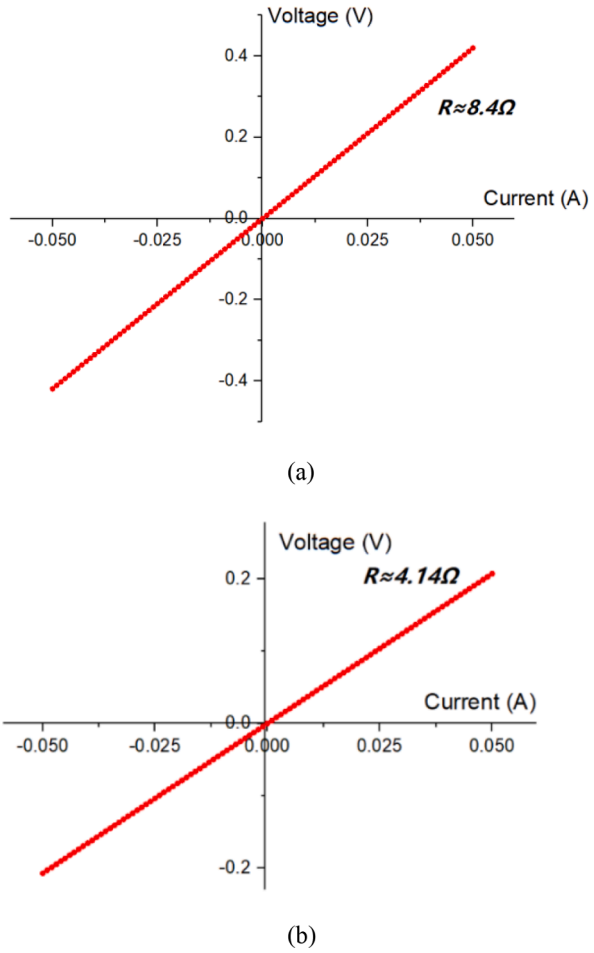

Fig. 11. Measured I-V curves of wafer-scale daisy chain pattern over (a) 202 contact spots of Al-Al, (b) 80 contact spots of NbN-NbN.

seen in our results that the 100 μm × 100 μm pattern on the wafer is a bit less resistive than the 50 μm × 50 μm patterns. The measured resistance R_{meas} is taken to be the average of the two, which gives 2.83 Ω. The sheet resistivity ρ_{sheet} is calculated according to Eqs. (1) and (2), where the sheet resistance is denoted as R_{sheet} and the film thickness t is 180 nm. Calculation renders 12.83 Ω of the sheet resistance and 230.9 μΩ•cm of the sheet resistivity.

$$R_{sheet} = \frac{\pi}{ln(2)} \times R_{means} = 12.83\ \Omega \tag{1}$$

$$p_{sheet} = R_{sheet} \times t = 230.9\mu\Omega{\cdot}cm \tag{2}$$

3.4. Contact resistance of bonded NbN

The resistance of wafer-scale daisy chain is measured in 4-point Kelvin fashion at room temperature. More pins that stick out on the bottom wafer are designed to locate the area on the bonded wafer with bad bonding quality in terms of electrical connection. The I-V results shown in Fig. 11(a) and (b) are both straight lines that go through the origin. For the Al-Al daisy chain, 202 contact spots on the bonded wafers give a total resistance of 8.4 Ω, indicating that the contact resistivity of a single contact spot is on average not greater than 1.66×10^{-3} Ω·cm^2. Likewise, for NbN-NbN daisy chain resistor, 80 contact spots on a branch of the entire chain give a total resistance of 4.14 Ω, indicating that the contact resistivity of a single contact spot is on average not greater than 2.36×10^{-3} Ω·cm^2.

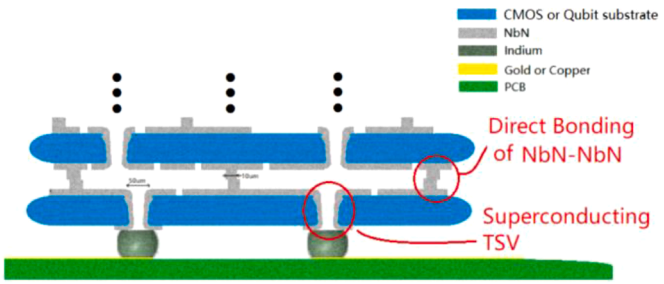

Fig. 12. Conceptual Schematic of a two(multi)-layer superconducting structure for 3-D qubit integration.

4. Conclusion

The direct bonding of superconducting material is important for integration of 3D superconducting chips and particularly quantum processors. The research into this topic is not abundant so far. In this paper, fabrication, measurement and direct bonding of superconducting NbN film have been demonstrated. Major achievements are summarized as:

- Optimization of T_c for NbN film is achieved by correlating with the curves of discharge voltage and the chamber pressure v.s. N_2 flow rate during magnetron sputtering deposition in Trikon Sigma 204. The highest T_c for Ar flow rate of 100 sccm and substrate temperature of 350 °C was 15.2 K at 75 sccm N_2 flow rate.
- Van der Pauw structure is fabricated for sheet resistance measurement of a NbN film which was 12.83Ω.
- Wafer scale daisy chain pattern is designed and fabricated to fast derive room temperature contact resistance from thermo-compression bonding. The contact resistivity of the NbN to NbN daisy chain was 2.36 $\times 10^{-3}\Omega{\cdot}cm^2$.
- NbN to NbN thermo-compression bonding is achieved and shows good bonding strength as it could survive the force from handling and transportation and wafer dicing, as well as from the shear force a human hand could generate.

To achieve 3D integration of superconducting chips, directing bonding is not enough. TSV and BGA are also required for superconducting connection between chip and PCB, integrated in one structure as shown in Fig. 12. A step forward would be integrating these substructures with qubits.

CRediT authorship contribution statement

Ye Li: Data curation, Visualization, Validation, Writing - review & editing. **Amir Mirza Gheytaghi:** Writing - original draft, Formal analysis. **Miki Trifunovic:** Investigation, Software. **Yuanxing Xu:** Methodology, Resources. **Guo Qi Zhang:** Conceptualization, Project administration, Supervision. **Ryoichi Ishihara:** Conceptualization, Project administration, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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