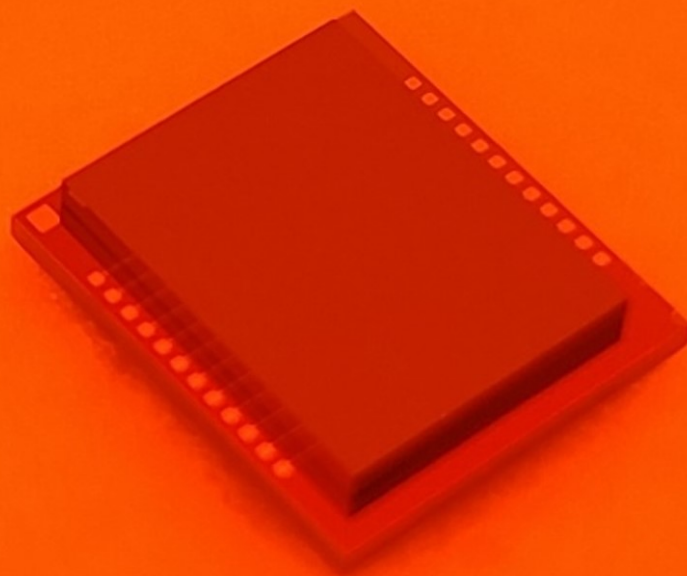


Cryogenic Interposer System for 3D Integration of Quantum Computers

Enhancing Scalability of Next-Generation Computing Solutions

Aryan Dubey



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Enhancing Scalability of Next-Generation
Computing Solutions

by

Aryan Dubey

to obtain the degree of Master of Science
at the Delft University of Technology,
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*This thesis is confidential and cannot be made public until August 29, 2028.
Op dit verslag is geheimhouding van toepassing tot en met 29 August 2028.*

An electronic version of this thesis is available at <http://repository.tudelft.nl/>.

Preface

This thesis is written as a partial satisfaction for the requirements of the Master of Science Degree in Microelectronics at the Faculty of Electrical Engineering, Mathematics and Computer Science, at the Delft University of Technology.

This project aims to design an Active Interposer and Flip-Chip Bonding Scheme to enable 3D integration of CryoCMOS and Photonic Circuits, leading to highly scalable and reproducible Quantum Computers. It involves the design, fabrication, and cryogenic testing of samples in-house at TU Delft, Else Kooi Lab, and Kavli Nanolab.

I want to express my gratitude to my project supervisors, peers, and friends, as this thesis would not have been possible without their unwavering support.

First, as part of the QIT group and EEMCS, I want to thank Dr. Ryoichi Ishihara, who gave me the opportunity to work in his research group and provided me with all the facilities and tools needed for successfully undertaking this project. I would like to thank Dr. Salahuddin Nur for his guidance during the formative stages of this project. Also, a special thanks to Maurice van der Maas for his guidance in Kavli Nanolab, and to Sadik Ilik and Deb Dutta for their assistance in device measurements using the cryogenic probe station.

Second, as part of TNW and QuTech, I would like to thank Dr. Matvey Finkel, Martijn Veen, and Rebecca Gharibaan, for their vital roles during the flip-chip and cryogenic measurements phase of the project.

Third, as part of Kavli Nanolab and Else Kooi Lab, I would like to thank Eugene Straver, Charles de Boer, Bas van Asten, Marinus Fischer, Roald van der Kolk, and Dr. J. van Wingerden for their support in solving fabrication-related challenges during my project.

Last, but definitely not least, I want to thank my parents, Sanjeev Kumar Dubey and Vijayshree Dubey, and my brother Kartikeya Dubey for their support and encouragement for the entire two years of my Master's Studies.

*Aryan Dubey
Delft, August 2023*

Abstract

Demand for high density, high bandwidth, and low power Integrated Circuits (ICs) is rapidly increasing even as Moore's Law is starting to plateau. Among the new wave of technologies that are meant to continue the prevalent trend of semiconductor device scaling, 3D System Integration promises many advantages over traditional single-planar designs. This technology enables designers to stack multiple dies and unlock new functionality by reducing the footprint of the final device package. Using 3D Integration, multiple different types of chiplets (Digital IC, Analog IC, MEMS) can be integrated into a single package, potentially bypassing an expensive move to a newer process node and unlocking even more functionality from the same package.

These downscaling issues are not limited to traditional CMOS technologies but extend to Quantum Computers. Due to the highly heterogeneous nature of Quantum ICs, and especially their requirement of low qubit decoherence noise, we require high-density connections from the Qubit layer to the Microelectronics Control layer while maintaining appropriate spacial separation between the two. In this project, the qubit layer is comprised of Diamond Colour Centers in a Photonic IC with other optical components such as SNSPDs, and MEMS switches. On the other hand, the microelectronics control layer is a Cryogenic CMOS chip.

The main goal of this project is to design an Interposer and related technologies like Through Silicon Vias (TSVs) and Microbumps to successfully integrate these two chiplets in a single 3D assembly. We conduct thermal analysis of multiple 3D assembly designs using Finite Element Modelling to derive optimum fabrication specifications. Subsequently, fabrication recipes are developed and optimised for TSV etching, coating, and patterning with superconductive sidewall liners. Recipes are also developed to fabricate Indium Microbumps using techniques like evaporation, liftoff, and atmospheric reflow. Utilizing these microbumps, we conduct cold-compression flip-chip experiments. Finally, we establish cryogenic measurement setups to electrically characterize these fabricated devices.

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1

Past, Present, and Future of Computing

We are nearing the end of Moore's Law, a techno-economic model, and the driving force behind semiconductor device scaling for the last 50 years. As devices shrink and consumers demand more functionality out of them, designers are pushed towards higher power density, higher bandwidth, and smaller footprint IC designs. Over these past 50 years, we have come to expect a steady increase in fast, predictable, and reliable performance from consumer and industry-grade computing devices.

The rise of "big-data" companies has resulted in the vast majority of us having access to the world's knowledge at our fingertips [1]. Furthermore, there is a growing demand to integrate different types of circuits into a single package including digital logic, memory, analog, RF, and possibly even MEMS sensors. Since all of these circuits are designed using different process technologies and fabrication flows, some more advanced than others, large-scale fabrication of such systems is proving to be a major issue [2].

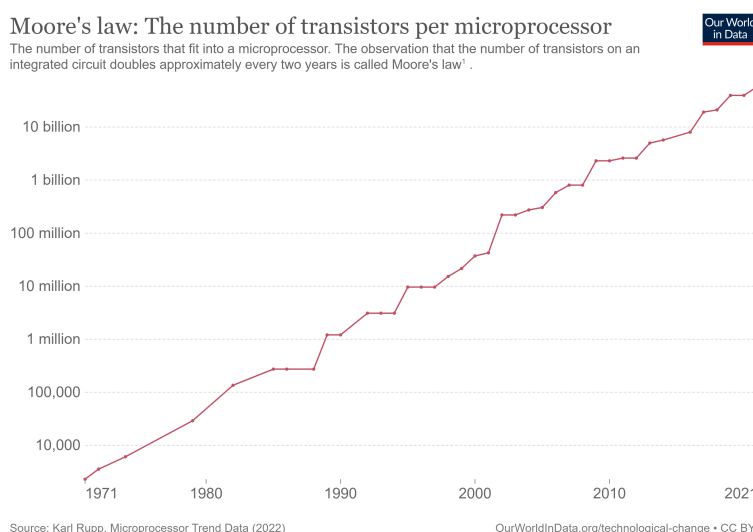


Figure 1.1: Trends in Moore's Law over the past 50 years [3].

The primary driving forces behind Moore's Law are now failing. On-chip interconnect density has reached a plateau; transistors are limited by the Critical Dimension (CD) of their gates leading to highly sensitive transistor performance, sometimes dependent on a few atoms; and, current leakage through thin and narrow dielectrics is now more apparent [4].

Several roadmaps have been proposed to address this issue, both for the near (~ 10 years) and long term (10-20 years); with 3D Integration playing a key role in both scenarios. Using new device stacking methodology we can go beyond single-die planar structures in our design and integrate a variety of homogeneous and heterogeneous systems in a single package [5]. This thesis will elaborate on such 3D Integration methodologies, explain their relevance, and showcase a new design for their application in next-generation Quantum Integrated Circuits (QICs).

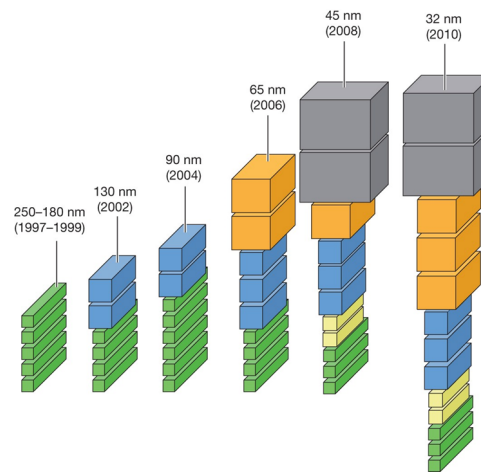


Figure 1.2: Representation of interconnect density evolution from 1977 to 2010 [1].

1.1. Quantum Information Processing

Among the several novel computing breakthroughs in recent years, quantum computing is one of the most promising routes. Ever since their proposal by Richard Feynman and Yuri Manin in the 1980s, scientists and engineers have made huge strides in trying to explain the world of Quantum Mechanics, which has proven to be the ultimate barrier in semiconductor device scaling [6].

If successful, Quantum Computers will have far-reaching applications in two major fields, Quantum Computing and Quantum Communication. The latter focuses on network security and cryptography, while the former harnesses the power of the Qubit to perform complex computation problems that would take classical computers exponentially more time to perform.

Quantum ICs are built upon the Qubit, the fundamental object of information in Quantum Computing. Contrary to a binary bit, that can represent a value of 0 or 1, a Qubit can denote a value of 0 or 1 or a superposition of both. They are usually represented by a Bloch Sphere as shown in Figure 1.3. In the sphere, the Qubits are represented in two common forms, the column vector notation, and the "bra-ket" notation. The Qubit can form *linear combinations of states*, i.e. superpositions, as

denoted in Equations 1.1 or 1.2, where α and β are complex numbers satisfying the condition $|\alpha|^2 + |\beta|^2 = 1$ [7].

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle \quad (1.1)$$

$$|\psi\rangle = \alpha_{00}|00\rangle + \alpha_{01}|01\rangle + \alpha_{10}|10\rangle + \alpha_{11}|11\rangle \quad (1.2)$$

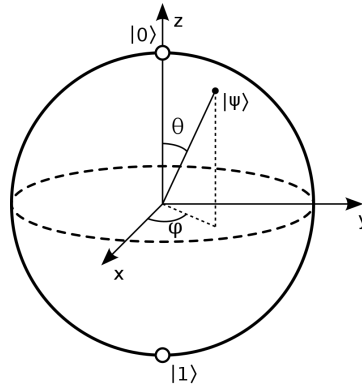


Figure 1.3: Representation of a Qubit as a Bloch Sphere [7]

Due to this property, theoretically, it is possible to build an n -level quantum system with the basis states of the form $|x_1 x_2 \dots x_n\rangle$, consequently, such a system will have its quantum state specified by 2^n distinct amplitudes. Due to the power of exponents, assigning $n=500$ will mean this number becomes larger than the total atoms in the entire universe. Such a system is obviously not realisable using a classical computer and binary bits, and this is why we must explore different types of Qubits that can harness the power of quantum mechanics to perform intense computation tasks.

1.1.1. Quantum Computing using Diamond-based Spin Qubits

The establishment of entanglement over two or more qubits is the main goal of both Quantum Computation and Quantum Communication systems under development [8]. However, this entanglement is very sensitive, and even a small interference from the environment can break this entanglement causing *decoherence*. Due to this, Quantum Computation is usually performed at cryogenic temperatures and in noise-free environments that are custom-built for this application.

In this project, we will be considering Diamond based Spin Qubits, as they have been long-standing candidates for applications in not just Quantum Computation but also Quantum Sensing. *Nitrogen-Vacancy (NV) Centers* are some of the best characterised defect-centers in diamond [9]. They consist of a Nitrogen impurity paired with a vacant site in the carbon lattice of diamond as shown in Figure 1.4. NV-centers have demonstrated long coherence times, and allow readout of electron spin states at a wide range of relatively high temperatures (1K - 4K).

Another advantage of using colour centers in diamonds as qubits is their optical interface. This enables entanglement between physically separated colour centers, even on different chips. This, in turn, unlocks vast potential in the scalability of our system to beyond 1000's qubits subdivided into reproducible unit cells. These unit cells can be connected using optical waveguides in the same chip, or using optical fibers to connect between other chips in different cryostats [11].

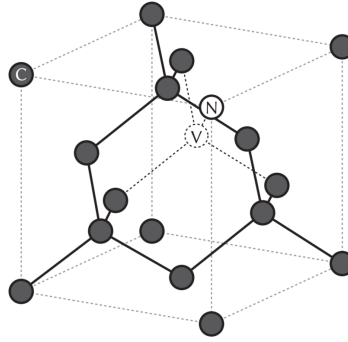


Figure 1.4: Nitrogen-Vacancy Defect in carbon lattice of diamond [10]

However, in trying to combine the Photonic Circuitry and CMOS Control Circuitry, we come to a realisation that integrating these technologies on a single substrate is currently not feasible. The approximate footprint of a diamond-based spin qubit is $50\mu m \times 50\mu m$, while the CMOS process node considered in this project is the TSMC 40nm design. This gap between both technologies imposes stringent demands when it comes to fabricating these devices, and thus it is necessary to explore techniques that can integrate these qubits and their control electronics in the same package. This is where the concept of Heterogeneous 3D Integration comes into play. 3D Integration employs multiple vertically stacked chiplets without the use of wirebonds for very high interconnect density and the possibility of integrating technologies across process nodes and fabrication flows [12].

1.2. Heterogeneous Integration of Quantum Computers

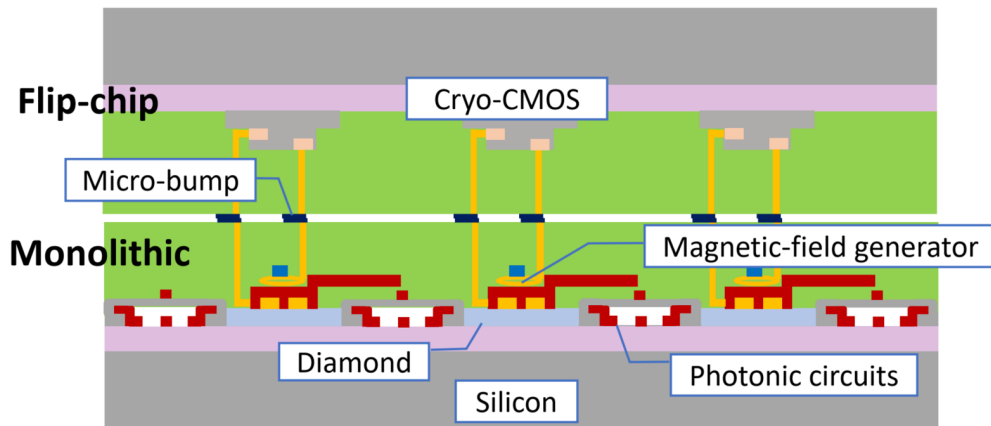


Figure 1.5: Vision for the scalable quantum computer built upon diamond-based spin qubits. Interconnects will connect the Qubit layer (bottom layer) to the classical error-correction electronics (top layers) [12]

As shown in Figure 1.5, our vision for the future scalable quantum computer necessitates the development of 3D integration schemes that can integrate the different technologies (Qubits, CryoCMOS, MFG Coils, Photonic circuits etc.) and provide sufficient thermal resistance in the Z-direction to maintain the gradient between the 1K and 4K operational zones.

As we want to increase the number of qubits beyond 1000s, major integration problems emerge. Specifically, in the case of diamond defects, decoherence noise plays a major role in limiting the total number of qubits on one layer. We can try to reduce this noise by physically distancing the different quantum systems (chipelets) and increasing the coherence times of the qubits. These separated chipelets can then be bonded together using flip-chip or similar 3D integration techniques. A study by Ishihara et al. [12] has proposed an integration scheme for integrating a modular quantum computer with diamond spin qubits using flip-chip techniques.

1.2.1. Overview of 3D Integration Mechanisms

3D Integration can be achieved by a variety of technologies depending on the type of application, Figure 1.6 showcases three major techniques that we have considered for our design, *Direct Oxide Bonding*, *Metal-to-Metal Bonding*, and *Adhesive Bonding* [13].

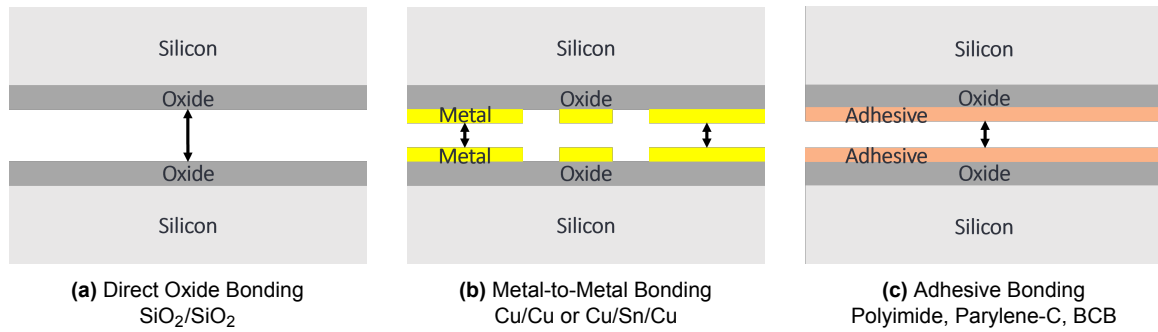


Figure 1.6: Chip/Wafer bonding technologies based on the type of bonding mechanism, adapted from a study by Lu et al. [13]

Direct Oxide Bonding

It consists of bonding extremely smooth surfaces (RMS roughness <1nm) by means of Van der Waals forces and/or surface OH bonds. Most commonly performed for oxides [14], this can be done at room temperatures, with additional annealing at higher temperatures to form stronger covalent bonds. However, the requirement of high smoothness and high flatness (<25μm over a 6-inch wafer) means that additional process steps (like chemical metal polishing) are required. The surfaces also need to be very clean and small contaminants can cause cracks in the wafer due to the high bonding forces (~1kN) [15].

Direct Metal Bonding

It consists of direct bonding of metals that form both mechanical support and electrical interconnects between the bonded chips. The metal bonds are more thermally conductive and allow for high heat-flux between the chips, however, this property is not desirable for our application since we need to maintain a high thermal resistance between the CryoCMOS and Photonic chipelets. Metal bonds also require extremely clean and oxide-free surfaces which can be achieved using HCl or HF cleaning before bonding [15]. Another disadvantage of this technique is the long and high annealing times and temperatures required to achieve optimum bonding strength. A study done by Ye Li et al. has showed that for direct bonding of NbN, annealing at 1100°C for 3

hours was required to achieve the required bonding strength, which is not suitable for the CryoCMOS chips with aluminium interconnects [16].

Adhesive Bonding

If, for some reason, highly smooth contact surfaces are not attainable, adhesive bonding is an option. Polymers like Benzocyclobutene (BCB), Polyimide (PI), or Parylene-C can be spin coated, patterned, bonded and cured to mate the chips/wafers together. Curing takes place at relatively low temperatures (e.g. 250°C in N_2 atmosphere for BCB) and is CMOS compatible. However, this process is prone to void formation if spin-coating or spray-coating is not done properly or bonding is not done from the inside of the sample towards its edges [15]. Out-gassing is also an issue especially if we are to put these samples in a vacuum cryostat chamber.

The specifications for this project require a superconducting electrical connection between the CryoCMOS and Photonic chips, thereby eliminating the oxide fusion and adhesive bonding approaches for now. Thus, only Direct Metal Bonding for cryogenic superconducting applications was considered for further evaluation during this project.

1.2.2. Key Technologies Enabling 3D Interconnections

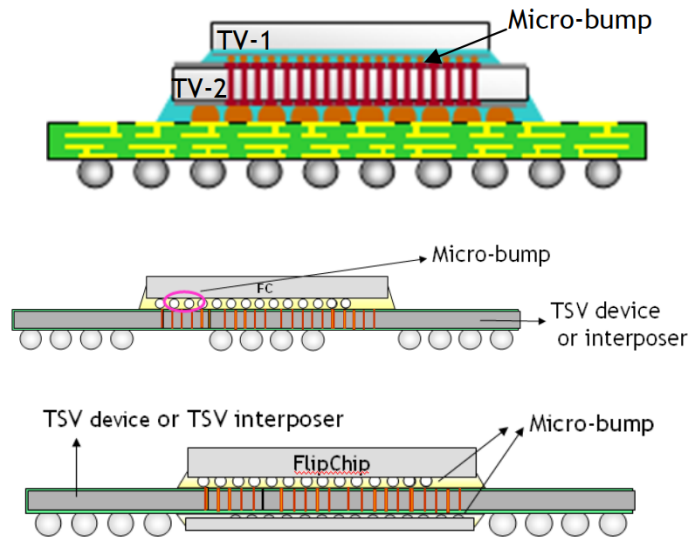


Figure 1.7: Packaging of multiple chiplets using microbumps and interposers with TSVs [17]

Superconducting Through Silicon Vias

Through Silicon Vias (TSVs) are vertical interconnects used to connect electrical circuits on either side of the silicon wafer. They are often used in MEMS ICs to integrate the control and readout electronics with the MEMS sensors which are usually fabricated on the backside of the wafer as shown in Figure 1.8 [18].

TSVs are an important component of our interposer design and need to be fabricated using superconductive materials. Copper, Tungsten, and Aluminium are the most commonly used materials used for TSV filling [19], however, none of them are

superconductive in the operational temperature range of our Quantum Computer (1K-4K). They also have high thermal conductance as showcased in Chapter 3, which increases the heat flux between the CryoCMOS and Photonic chips. Thus, new fabrication techniques and materials are explored in this project to satisfy the requirement of superconductivity and low thermal conductivity at the same time.

Foxen et al. [20] have previously studied the application of TSVs in Quantum Computers and have come forward with the following recommendations: yield must be high on routing control signal lines (>99.9%), performance must be reproducible on cooling down from 300K to 1K, and superconductivity is essential to provide a lossless connection between both chips and avoid local hotspots.

Further discussions regarding Through Silicon Vias and their application in Quantum Computers will take place in Chapter 3.

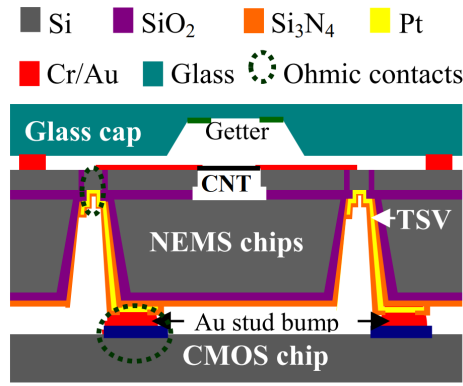


Figure 1.8: System in Package concept for CNT resonator with electrical connection to the control IC using TSVs [21]

Plasma Enhanced Direct Metal Bonding

Direct Metal Bonding is the ideal flip-chip technique for our application since it allows using materials like Nb ($T_c = 9.3K$), NbN ($T_c = 15.7K$), NbTiN ($T_c = 15.2K$), and TiN ($T_c = 5.6K$) for the bonding interface [16, 22]. However, as discussed previously, this technique requires a relatively high bonding temperature ($\sim 500^\circ C$) and even higher annealing temperature ($\sim 1100^\circ C$) for optimum bonding strength [16]. This can cause changes in the optical properties of the previously fabricated Photonic Waveguides and the defect implantation properties of the diamond colour centers. Several techniques have been proposed to overcome this issue.

Fujino et al. [23] have demonstrated room temperature surface activated direct bonding of 200nm thick Niobium (Nb) using Argon (Ar) fast atom bombardment. Huang et al. [24] have demonstrated Ar plasma enhanced direct bonding of GaAs on Si substrates with minimal voids and high shear strength. A similar approach is proposed for the direct bonding of NbTiN to form superconducting interconnects between the CryoCMOS and Photonic chips. Moreover, NbTiN and related Niobium alloys have low thermal conductivity, and direct bonding of these materials will allow for reduction of heat flux between the two chips, as discussed further in Chapter 2 [25, 26].

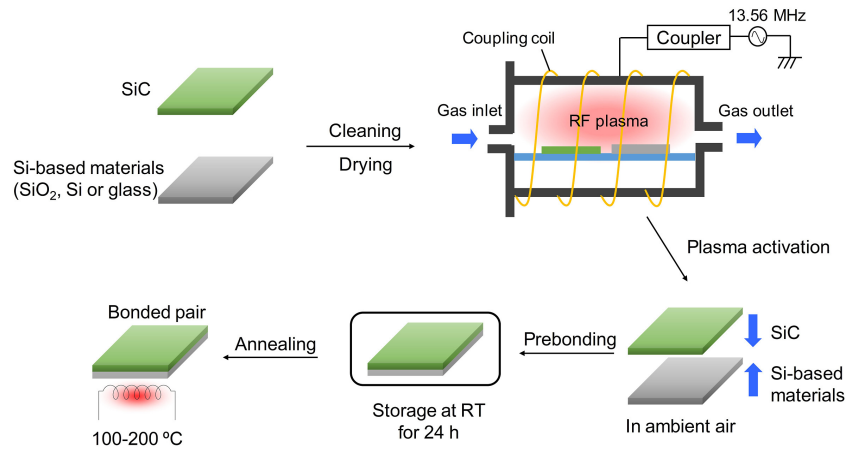


Figure 1.9: Plasma Enhanced bonding of SiC and Si-based materials. A similar approach can be applied to Niobium alloys for flip-chip bonding [27]

High-Pitch Indium Microbumps

Microbumps are an important component of flip-chip integration schemes as they provide better electrical, thermal, and mechanical performance when compared to wire-bonds [28]. Current industry standards exist for Sn/Ag/Cu microbumps at room temperature applications as shown in Figure 1.10. However, SnAg is shown to be unsuitable for cryogenic applications due to its brittle nature and low critical temperature resulting in poor life cycles for the integrated assemblies.

Indium has been demonstrated as a good replacement candidate for Sn/Ag/Cu microbumps mainly due to its ductility at cryogenic temperatures and critical temperature (T_c) of 3.4K [29]. And while this T_c is higher than the operating temperature of the CryoCMOS stage (4K) it is within the operational range of the Photonic stage (1K). Moreover, Indium microbumps can be bonded using room temperature compression in atmospheric conditions, eliminating the extremely high-temperature annealing steps that are required for direct metal bonding.

Due to these reasons, Indium Microbumps were deemed necessary for study in this project and their specific application and fabrication process will be explored further in Chapter 4.

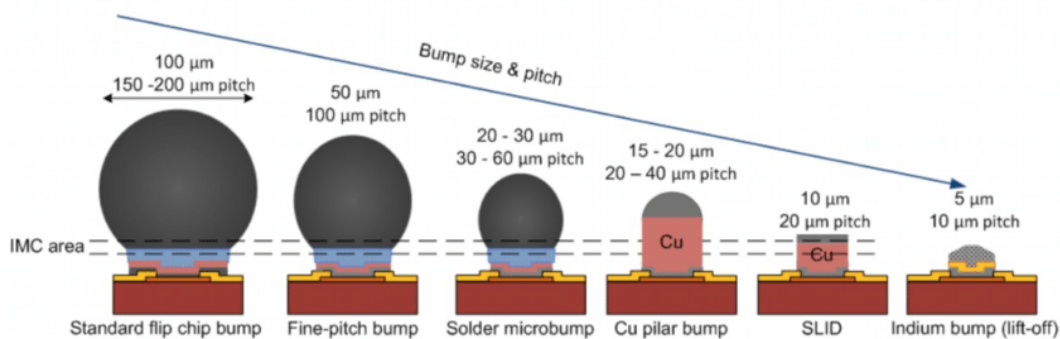


Figure 1.10: Evolution of microbump diameter and pitch [30]

Active Interposer

An important component of any 3D integration scheme is the *Interposer* as it allows us to combine different technologies (RF, MEMS, Optical) into a single package for placement inside the cryostat. Two options exist for implementing this interposer, namely the *Passive Interposer*, as shown in Figure 1.11, and the *Active Interposer*, as shown in Figure 1.12. The Active Interposer was considered the more attractive choice for this project since it can reduce the final package footprint even more than the passive option, and aid in heat flow regulation from the CryoCMOS chip to the Photonic chip.

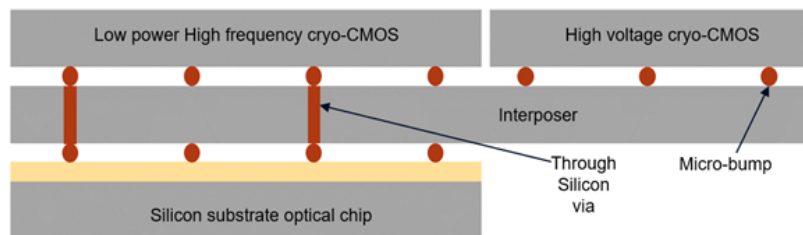


Figure 1.11: Passive Interposer proposal for connecting CryoCMOS chips to the Photonic chip.

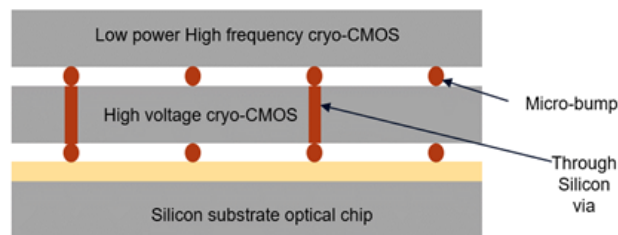


Figure 1.12: Active Interposer proposal that utilises the HV CMOS chip as the interposer between the RF CMOS chip and the Photonic chip.

1.3. Goal of this Study

This project is part of a larger collaboration between QuTech and Fujitsu, which aims to design and fabricate a *Scalable Quantum Computer using Diamond-based Spin-Qubits*. The preliminary specifications for 3D integration of the Photonic Chip and the CryoCMOS Chip are therefore set as follows:

- Temperature range: Photonic Circuits @ 1K, CryoCMOS Circuits @ 4.2K.
- 15 mW heat load at 1K (10 mW direct and 5 mW from CryoCMOS).
- 1 W heat load at 4K, 5% (50 mW) for interconnects to the 50K stage, 95% (950 mW) for unit cells at 9.5 mW/unit-cell.
- Low thermal conductance between the TSV and the silicon substrate (e.g. BCB liner, SiO₂ (>3 μ m)).
- 10mm x 10mm active area with 1mm peripheral on two sides for bond pads and optical connections.
- Bond-pad size 30 μ m x 30 μ m, bond-pad pitch $\leq$ 40 μ m.

- TSV diameter $\leq 30\mu\text{m}$, TSV pitch $\leq 40\mu\text{m}$.
- Microbump diameters $\leq 20\mu\text{m}$.

To meet the above-described specifications, this project will make three important contributions; (i) thermal design of the interposer stack based on finite element modelling, (ii) design, fabrication, and patterning of superconductive through silicon vias, and (iii) design, fabrication, atmospheric reflow, and flip-chip bonding of Indium microbumps. Fabrication process recipes will be optimised for the following:

- Through Silicon Via (TSV) SiO_2 hard mask etching;
- Through Silicon Via (TSV) Silicon etching, sidewall roughness and sidewall shape optimisation;
- Through Silicon Via (TSV) dielectric lining with SiO_2 and Al_2O_3 ;
- Through Silicon Via (TSV) superconductor lining with TiN and NbTiN;
- Interposer patterning for the via-last TSV process.
- Indium e-beam evaporation and patterning (lift-off);
- Indium microbumps annealing and reflow;
- Flip-chip bonding using Indium microbumps.

1.4. Outline of this Thesis

Building upon the project requirements discussed in this chapter, this thesis will be organised as follows:

Chapter 2 will showcase the results of thermal simulations performed in Ansys Icepack to analyse the heat flux between the CryoCMOS and Photonic chiplets in three distinct Interposer design proposals.

Chapter 3 will discuss the design requirements and fabrication processes for Through Silicon Vias, and elaborate upon their integration in the cryogenic interposer.

Chapter 4 will explain the fabrication methodologies of Indium Microbumps and showcase the results of flip-chip bonding utilizing said microbumps.

Chapter 5 will showcase the preliminary electrical characterisation results for the devices fabricated in Chapters 3 and 4, and give recommendations about future cryogenic measurements that can be performed to further understand device performance metrics.

Finally, Chapter 6 will present the conclusions drawn from this project and provide recommendations for future research into the 3D Integration of Scalable Quantum Computers.

2

Thermal Modelling of Cryogenic Interposers

2.1. Introduction

Among the many issues present in 3D System-in-Package (SIP) Integration, thermal management is of high importance to us due to operations at cryogenic temperatures. Heat flux generated by the stacked chips is high, resulting in high power density, and improper cooling of such assemblies can seriously affect the performance of such chips [31]. 3D assemblies also increase the total power generated per unit cell, which may lead to overheating and thermal hotspot issues if not cooled adequately [32]. The Qubit layer of our Quantum Stack operates at 1K and the CryoCMOS layer at 4K, and hence, maintaining good electrical conductivity and bad thermal conductivity is paramount to the performance of our Quantum IC.

Through Silicon Vias, especially when grouped in arrays, exhibit thermal coupling through the Silicon substrate, resulting in local heating of the 3D assembly and increasing the heat flux between the TOP and BOTTOM surfaces of the interposer [33]. TSVs can also be used as a heat sink in an effort to reduce substrate temperatures, by using high thermal conductivity materials like Copper, Aluminium, and Indium to fill the structures as demonstrated by Lay et al. [31]. Thermal conductivity of a filled TSV Interposer is anisotropic, i.e. $k_{eq,x} = k_{eq,y} \neq k_{eq,z}$. The equivalent thermal conductivity can be obtained using the Equations 2.1, 2.2, and 2.3.

$$q = -k_{eq,z} \frac{dT}{dz} = k_{eq,z} \frac{|\Delta T|}{\Delta z} \Rightarrow k_{eq,z} = q \frac{\Delta z}{|\Delta T|} \quad (2.1)$$

$$q = -k_{eq,x} \frac{dT}{dx} = k_{eq,x} \frac{|\Delta T|}{\Delta x} \Rightarrow k_{eq,x} = q \frac{\Delta x}{|\Delta T|} \quad (2.2)$$

$$k_{eq,y} = k_{eq,x} \quad (2.3)$$

A major difference between our study and the one conducted by Lau et al. is the requirement for superconductivity in the TSV and direct bonding interconnections. This, in turn, affects the material choices of our project. Figure 2.3 showcases the thermal conductivity of various materials under review. It can clearly be seen that materials

such as Indium, Niobium, and Copper possess a relatively higher thermal conductivity compared to other Niobium alloys such as NbTi, NbTiN, or even TiN, thereby necessitating a preliminary thermal analysis to refine the fabrication specifications of TSV diameter, metallization coating thickness, oxide coating thickness, direct bonding pillar height, and microbump thickness.

2.2. Heat Transfer Analysis using Finite Element Modelling

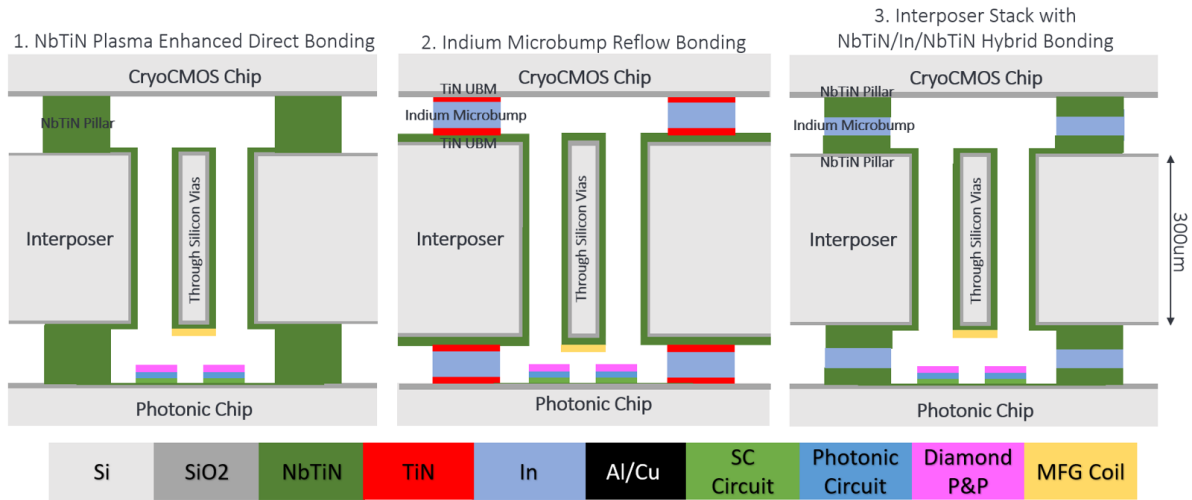


Figure 2.1: 3D Integration Schemes discussed in this report.

Based on the thermal conductivity and critical temperature of the materials under review, three design recommendations are made as showcased in Figure 2.1:

- **NbTiN Plasma Enhanced Direct Bonding.** In an effort to reduce the bonding and annealing temperature, plasma-enhanced bonding can be used for surface activation of the NbTiN thin films. This changes the bonding mechanism from bulk-diffusion dominant to surface-diffusion dominant but retains the same bonding strength [16]. A major disadvantage is the requirement of ultra-smooth surfaces to enable optimum inter-metallic bond formation.
- **Indium Microbump Reflow Bonding.** This is a commonly used 3D integration technique for cryogenic applications since Indium does not undergo a brittle transition at milliKelvin temperatures. It is also a good superconductor with a critical temperature of 3.4K and is malleable enough to facilitate room-temperature compressive bonding. This eliminates the requirement for ultra-smooth surfaces, unlike during direct bonding of Niobium alloys, and the reflowability of Indium ensures a void-free bonding interface. However, Indium is highly thermally conductive even at cryogenic temperatures, leading to high heat flux between the two bonded chips. A TiN under-bump material has been used during the fabrication of Indium Microbumps since it acts as a barrier layer between Indium and the wiring material (Aluminium, Niobium etc.) and prevents the formation of lossy intermetallic compounds [20].

- **Interposer Stack with NbTiN/In/NbTiN Hybrid Bonding.** To solve the issue of high heat flux in Indium Microbump bonding, NbTi or NbTiN pillars can be utilised to provide enough thermal resistance across the bonded interconnects. NbTi or NbTiN have relatively low thermal conductivity compared to Indium and similar schemes already exist for Cu/Sn/Cu hybrid bonding [34].

Ansys Icepack was chosen for the FEM thermal analysis of these design proposals. The general model used in the steady-state simulations is described in Figure 2.2 and consists of a single TSV and two direct bonds in a single unit cell. The effects of Thermal Boundary Resistance (a.k.a. Kapitza Resistance) will not be modelled in these simulations. A positive heat flow value indicates a direction of net heat conduction from the CryoCMOS chip to the Photonic chip.

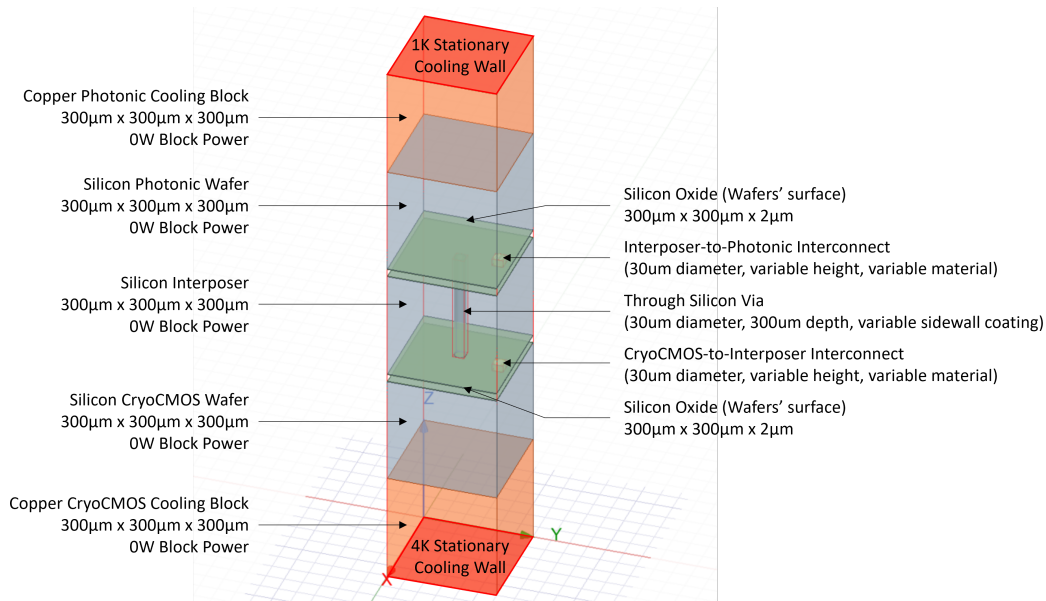


Figure 2.2: Ansys Icepack model used in the steady-state thermal simulations. Only a single TSV and two direct bonds were simulated to save simulation time, and the results can be extrapolated to n -number of TSVs or unit cells.

Ansyp Setup 2.1: Ansys Icepack Solver Settings

1. Final Residual System Energy: $1e-12$
2. Initial System Temperature: 3K
3. Initial System Heat Flow (X/Y/Z-directions): 0W
4. Thermal Boundary Resistance: 0 K/W
5. Bounding Box Conditions: Vacuum
 - (a) Thermal Conductivity: $1e-9$ W/m-K
 - (b) Mass Density: 0 kg/m³
 - (c) Specific Heat: 0 J/kg-K
 - (d) Thermal Expansion Coefficient: 0 µm/K

2.2.1. Direct Bonding Thermal Simulations

For optimisation of the direct bonding material and its thickness, the TSV coatings are kept constant at a thickness of $1\mu\text{m}$ for SiO_2 and $1\mu\text{m}$ for NbTiN. The TSV diameter is

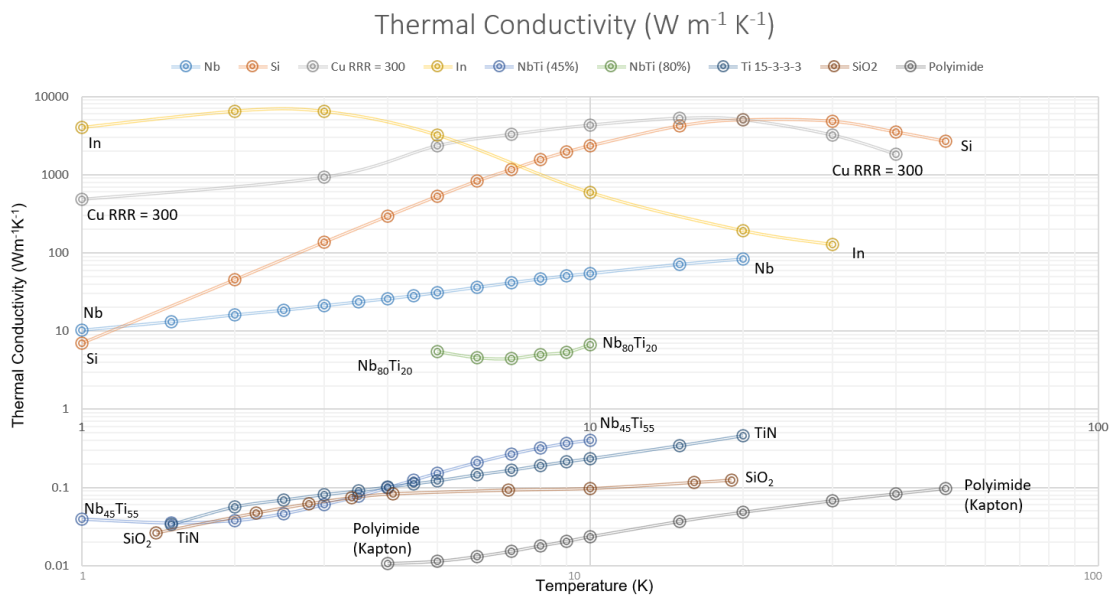


Figure 2.3: Thermal Conductivity of various materials under review, re-plotted from [25, 26, 35, 36].

also constant at $30\mu\text{m}$, and the interposer thickness is constant at $300\mu\text{m}$. The TSV is not filled with any material, not even polymer, and is exposed to a vacuum of very high thermal resistance as shown in Ansys Setup 2.1.

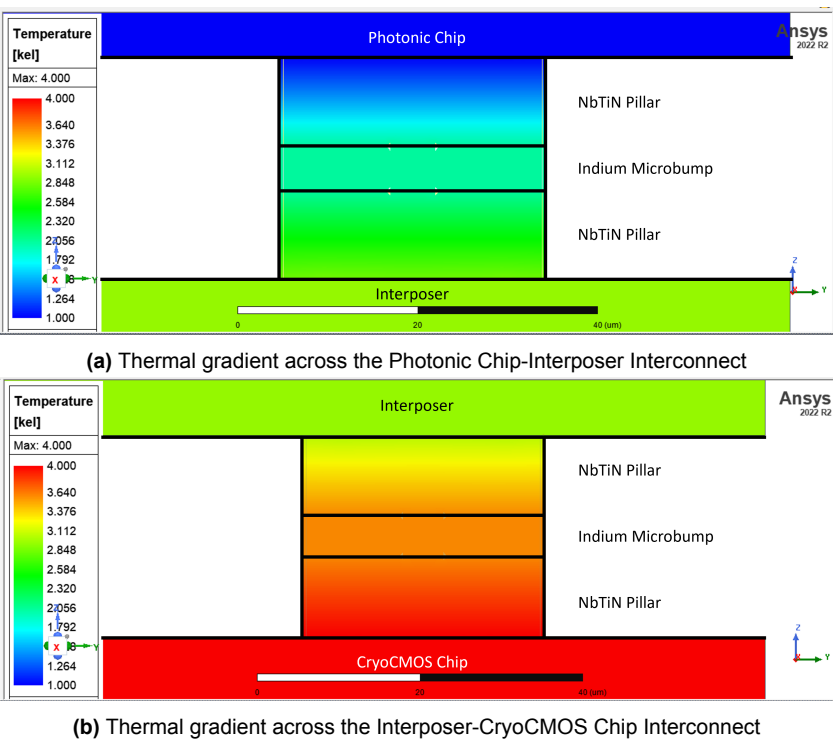


Figure 2.4: Temperature gradients across the direct bonding interconnects.

The direct bonding simulation results are shown in Table 2.1 and the temperature gradients across the direct bonds are shown in Figure 2.4. The results can be summarised as follows:

Table 2.1: Ansys Icepack thermal simulation results of various direct bonding schemes.

Direct Bond Type	Heat Flow Rate per Interconnect Pair (W)	Total Interconnect Pairs for Total Heat Flow Rate <5mW
TiN/In/TiN (1um/3um/1um)	2.76e-5	181
TiN/In/TiN (1um/5um/1um)	1.547e-5	323
TiN/In/TiN (1um/10um/1um)	1.541e-5	324
NbTiN (5um)	8.58e-6	582
NbTiN (10um)	4.89e-6	1022
NbTiN (20um)	2.65e-6	1886
NbTiN (20um) (without TSV)	2.859e-6	1750
NbTiN/In/NbTiN (10um/5um/10um)	2.36e-6	1900
NbTiN/In/NbTiN (20um/5um/20um)	1.38e-6	3630

- Indium Microbump direct bonding is insufficient to keep the total heat flow below 5mW unless the total interconnect pairs are reduced by a large amount.
- Due to the high thermal conductivity of Indium, increasing the diameter of the microbump does not reduce the heat flow by a significant amount. The thickness of the TiN UBM is minuscule (100nm - 1um) compared to the diameter of the microbump, and as such, it has no effect on the thermal resistance of the interconnect either.
- NbTiN direct bonding simulations yield positive results in reducing the total heat flux between the CryoCMOS and Photonic chips, however, the thickness of NbTiN pillars dictates that CMP steps will need to be added to the fabrication flow to reduce the RMS surface roughness below ~ 1 nm. Refer to Figure 4.1 for more details.
- The hybrid NbTiN/In/NbTiN bonding scheme is shown to be feasible provided NbTiN pillars of more than $20\mu\text{m}$ height can be fabricated. Such fabrication flows already exist for Cu pillars and electrodeposition of NbTi has been demonstrated for use in cryogenic superconducting applications [37].

2.2.2. TSV Sidewall Coating Thermal Simulations

As discussed in Chapter 1, our application demands a superconductor-lined Through Silicon Via with a dielectric liner separating it from the Interposer bulk. Multiple deposition processes exist to coat the TSV sidewall with these materials such as ALD,

PVD, and PECVD. Regardless of the process used, we first need to gauge the relation between the coating thickness and heat flux through the interposer.

Table 2.2: Ansys Icepack thermal simulation results for varying SiO₂ coating thickness.

Direct Bond Type	TSV Sidewall Coating Thickness (um)	Heat Flow Rate per Interconnect Pair (W)
NbTiN/In/NbTiN (1um/3um/1um)	SiO ₂ - 0.250 NbTiN - 0.500	2.75858e-5
	SiO ₂ - 0.500 NbTiN - 0.500	2.75918e-5
	SiO ₂ - 0.750 NbTiN - 0.500	2.75856e-5
	SiO ₂ - 1.000 NbTiN - 0.500	2.75844e-5
	SiO ₂ - 1.250 NbTiN - 0.500	2.75820e-5

Table 2.3: Ansys Icepack thermal simulation results for varying NbTiN coating thickness.

Direct Bond Type	TSV Sidewall Coating Thickness (um)	Heat Flow Rate per Interconnect Pair (W)
NbTiN/In/NbTiN (1um/3um/1um)	SiO ₂ - 1.250 NbTiN - 0.200	2.75822e-5
	SiO ₂ - 1.250 NbTiN - 0.300	2.75820e-5
	SiO ₂ - 1.250 NbTiN - 0.400	2.74823e-5
	SiO ₂ - 1.250 NbTiN - 0.750	2.76003e-5
	SiO ₂ - 1.250 NbTiN - 1.000	2.76005e-5

The simulation model is the same as shown in Figure 2.2, with the direct bonds on the TOP and BOTTOM being a constant layer stack of NbTiN/In/NbTiN (1um/3um/1um) of 30μm diameter. The TSV sidewall coating simulation results are shown in Table 2.2 and Table 2.3 and can be summarised as follows:

The heat flux between the CryoCMOS and Photonic chips does not depend on the coating thickness of the TSV sidewall, neither on the dielectric liner nor on the metallization layer. This goes against the findings of Lau et al. [31], however, this discrepancy can easily be explained by our material choices. In their study, Lau et al. used Copper filled TSVs which have a thermal conductivity much higher than Silicon at room temperature (~400 W/m-K v/s ~130 W/cm-K). This reduces the effective thermal conductivity in the Z-direction according to Equation 2.1, thereby increasing the heat flux with an increase in TSV diameter. This is not the same in our model, as NbTiN has a thermal conductivity of 100 times less compared to Silicon at cryogenic

temperatures. Hence, heat flow through the Silicon bulk dominates the total heat flux between the CryoCMOS and Photonic chips.

Comparing the results shown in Table 2.1, 2.2, and 2.3, we can also deduce that due to the high thermal resistance of the TSV liner materials compared to Silicon, the presence or absence of TSVs plays an almost insignificant role in the total heat flux through the interposer. Based on the above simulation results, *Design 3* (from Figure 2.1 is recommended for further evaluation as it promises 3D integration at low processing temperatures and the direct bonding scheme promises low heat flux between the CryoCMOS and Photonic chips.

2.3. Conclusion

In this chapter, three distinct 3D cryogenic interposer designs were presented and their pros and cons were discussed in detail. Thermal simulations were performed in Ansys Icepack to gauge their applicability in our potential 3D architecture, with a particular effort to optimise the direct bonding material and dimensions and TSV sidewall liner material and thickness. It was shown that Indium Microbump direct bonding or NbTiN thin-film direct bonding will be insufficient to regulate heat flux between the CryoCMOS and Photonic chips, resulting in massively reduced interconnections between the two chips (181 - 582 total pairs). Hence, a hybrid bonding scheme with tall NbTiN/NbTi pillars and Indium microbumps is recommended for further exploration. It was also shown that different TSV sidewall liners have negligible effects on the interposer surface temperatures or the heat flux through the interposer due to their low thermal conductivity compared to Silicon.

In the next chapter, we will study Through Silicon Vias in detail and optimise deep reactive ion etching recipes for the fabrication of high aspect ratio vias in $300\mu m$ silicon substrates. We will also explore various TSV sidewall coating techniques and pattern electrical test structures for further analysis.

3

Through Silicon Vias: Etching, Metallization, and Patterning

3.1. Introduction

Moore's Law was defined primarily for single-planar 2D ICs and the integrating of these ICs into a single chip using the System-on-Chip (SoC) approach. To move beyond this, we must develop system and device-level technologies such as System-in-Package (SiP), 2.5D Integration, and 3D Integration. Through Silicon Vias (TSVs) play an important role in all these integration schemes as they enable the reduction of interconnect pitches, and scaling down the RC delay that accompanies them.

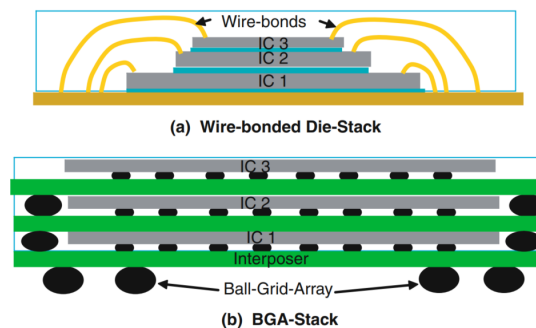


Figure 3.1: 3D packaging technologies [13]

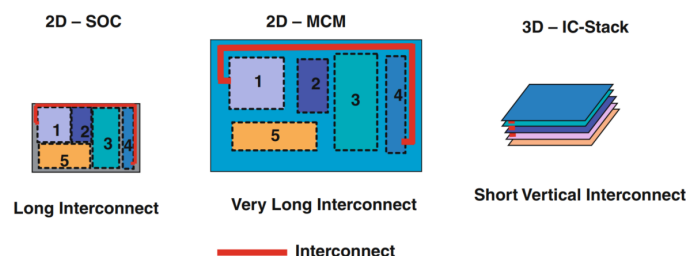


Figure 3.2: Reduction of interconnect length in different packaging options [13]

TSVs can be fabricated in a *via-first*, *via-middle*, or *via-last* approach depending on the specific implementation as shown in Figure 3.3. Via-first TSVs are fabricated before the front end of line (FEOL) fabrication of the active devices, doped polysilicon or Tungsten is often used to fill these TSVs since they can withstand high temperatures of further process steps. Via-middle TSVs are made after FEOL processing but before metallization in the back end of line (BEOL) process. Via-last TSVs are made after the BEOL process. This choice varies between different applications of the target chip/chiplet [38].

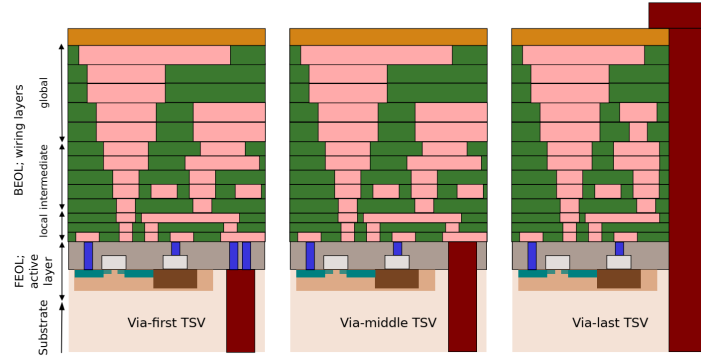


Figure 3.3: TSV fabrication techniques [39]

There are multiple reasons why TSV Interposers are an attractive choice for Quantum Computing applications, some of which are [40]:

- **Signal Delivery.** Integrating a large number of Qubits on a 2D lattice is not efficient when considering the traditional bond-pad approach at the boundary of the chip. Flip-chip processes using Indium bumps have been demonstrated to have high Qubit coherence ($\geq 20\mu\text{sec}$), however for delivering signals through the thick Silicon substrate, TSVs are a necessity.
- **Signal Isolation.** To achieve maximum coherence and minimum crosstalk, the Qubit layer and the Cryogenic-CMOS layer must ideally be completely isolated from each other (except for signal couplings). Careful layout and floorplanning of TSV landing pads to surround resonant elements can locally confine the EM modes, and a conductive plane on the top layer of the interposer can theoretically create a full 3D enclosure.
- **Suppressing Substrate Modes.** Bulk Silicon has its own electromagnetic mode, and for sufficiently large chips this mode falls into the operational range of Qubit devices (3-10GHz), which in turn creates another lossy channel we need to model. However, adding a large number of TSVs enforces additional boundary conditions on these substrate modes, thereby limiting the $\max(\lambda)$ to the designed TSV spacing. The study by Vahidpour et al. has cited that this can push the lowest mode frequency to well above 10GHz allowing for more flexibility in chip size [40].

In this chapter, we will study the theory of Deep Reactive Ion Etching and Atomic Layer Deposition as they are critical procedures in our fabrication flow. Next, the etching, coating, and patterning fabrication flows of TSVs will be developed and multiple failure modes and their solutions will be identified in the process.

3.2. Theory of Deep Reactive Ion Etching

Deep Reactive Ion Etching (DRIE) is a widely used technology in MEMS and 3D Integration since it can be used to etch a wide variety of materials, primarily Silicon, at very high etch rates up to $5\mu\text{m}/\text{min}$ [22]. It utilises high-energy ions in a plasma reactant to form volatile products and physically remove atoms on the reaction surface. It allows for the fabrication of ultra-high aspect ratio TSVs, provided suitable masks have been used (e.g. thick photoresist, silicon oxide, or silicon nitride). There are two main DRIE techniques available, the *Cryogenic DRIE Process* and the *Bosch DRIE Process*. Both use a Fluorine-based plasma like SF_6 or CF_4 during the etching step and demonstrate highly directional and anisotropic etching of the silicon substrate.

3.2.1. Cryogenic DRIE Process

Cryogenic DRIE was demonstrated in 1988 by Tachi et al. [41]. In it, the wafer is cooled to temperatures of -100°C and the passivation layer on the sidewall is formed by adding Oxygen to the plasma (SiO_xF_y) which creates a layer of SiO_2 as shown in Figure 3.4. The concentration of O_2 dictates the shape of the sidewall and hence this is a single-step process (which also leads to no scalloping). However, this process is highly susceptible to the crystal orientation of silicon, oxygen concentration, and temperature [22, 41]. Undercutting the hard mask is also a common occurrence in Cryogenic DRIE, which limits the minimum pitch of the TSVs in our interposer.

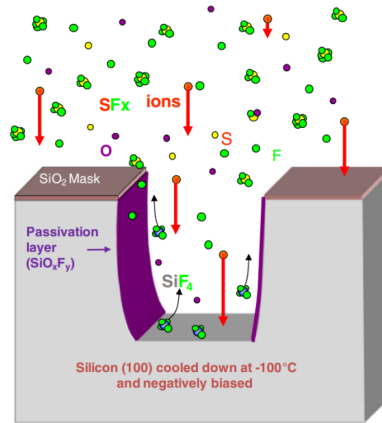


Figure 3.4: Etching mechanism of Cryogenic DRIE Process [42]

3.2.2. Bosch DRIE Process

Bosch Process consists of the three cycling steps. First, SF_6 is introduced to the plasma and etches the exposed Silicon isotropically in all directions. Second, an ultra-thin layer of C_4F_8 is deposited on the newly exposed surface to provide passivation from the upcoming cycles. Third, a DC bias voltage is applied to the wafer and it is bombarded with ions from the plasma in a breakthrough step. This removes the C_4F_8 polymer from the bottom-most surface but leaves the sidewall polymer intact due to the ion directionality. These steps are repeated till we achieve the required depth and shape of the TSV [38, 22]. This physical and chemical etching mechanism of this process is showcased in Figure 3.5.

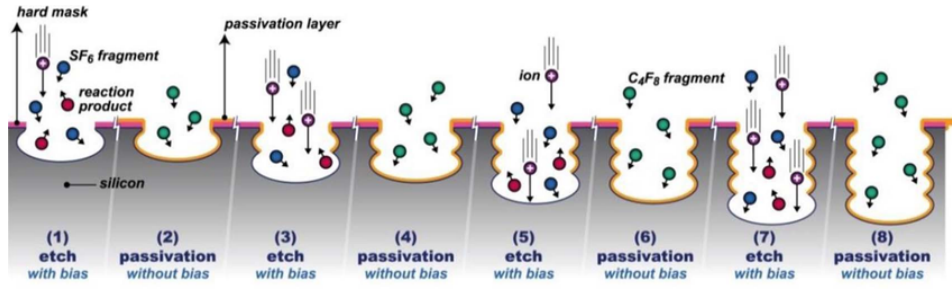


Figure 3.5: Etching mechanism of Bosch DRIE Process [43]

Despite these advantages, Bosch DRIE is not without its shortcomings. Longer etching steps give us faster etch rates, but also result in large scallops which can cause problems in the conformal coating of the sidewalls with dielectric or metallic layers. Improper substrate temperature control over long periods can negatively impact the etch rates and result in hard-mask undercutting. Different feature sizes are etched at different rates due to a phenomenon called *Aspect Ratio Dependent Etching*, as demonstrated in Figure 3.6. This is caused by limited *Knudsen Transport* of reactive content to the bottom of the via, and if the size of the trench/cavity is small the effect is more visible and leads to slow etching of smaller structures and large variation of etch depths across the wafer. In our application we generally work with TSVs of the same aspect ratios, however, their placement density can vary between designs and this can lead to a loading effect in some parts of the wafer [22].

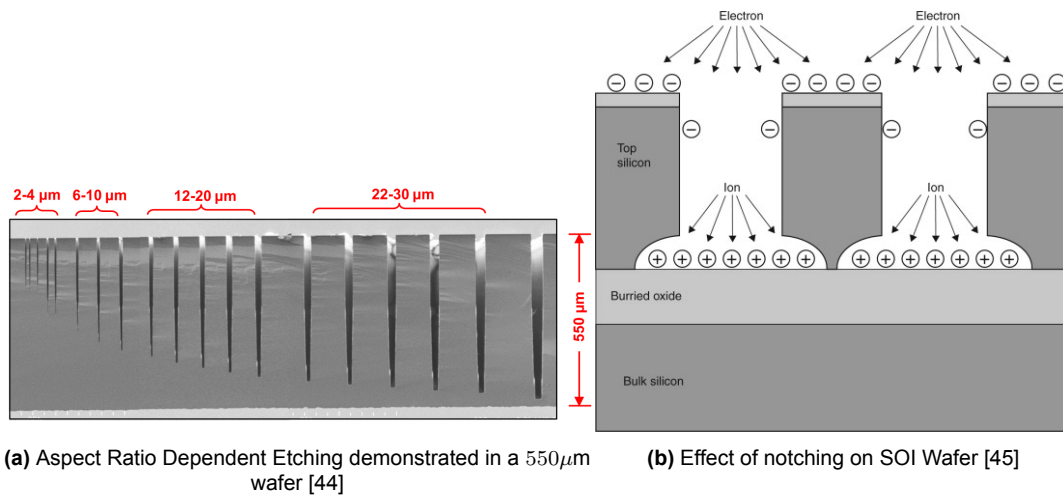


Figure 3.6: Representation of ARDE and Notching effects seen during Bosch DRIE.

Since there can be slight variations in the TSV etch rate across the wafer, an etch stop layer (usually SiO_2 or Al) is often used to protect the wafer holder from damage due to over-etching. This can cause an effect known as notching as shown in Figure 3.6, and is caused by a charge accumulation once the etching ions contact the dielectric etch-stop layer at the backside of the wafer. This may be avoided by using a conductive material as the etch stop layer, like Aluminium or a bare-Silicon carrier wafer.

3.3. Theory of Atomic Layer Deposition

Among the many TSV sidewall coating techniques available, *Atomic Layer Deposition (ALD)* promises the highest conformality and ability to coat ultra-high aspect ratio vias. ALD can be used to deposit a variety of metals, alloys, and dielectrics from their vapour phase precursors, and has emerged as a promising driver in the quest for device downscaling. As the project requirements demand smaller and more spacially demanding structures, alternative deposition methods like chemical vapour deposition (CVD) and physical vapour deposition (PVD) are unable to meet the demands of accurate thickness control, accurate composition control, and conformal deposition [46].

The basic ALD process is shown in Figure 3.7 and consists of sequential pulsing of chemical precursors that react with the exposed surface to form the desired material. This process can theoretically be repeated n -number of times till we achieve the desired thickness. However, in practice, film thicknesses of only up to 100nm are fabricated using this technique since cycling the precursors takes a long time and even 100nm thin films can take up to 12 hours to fabricate.

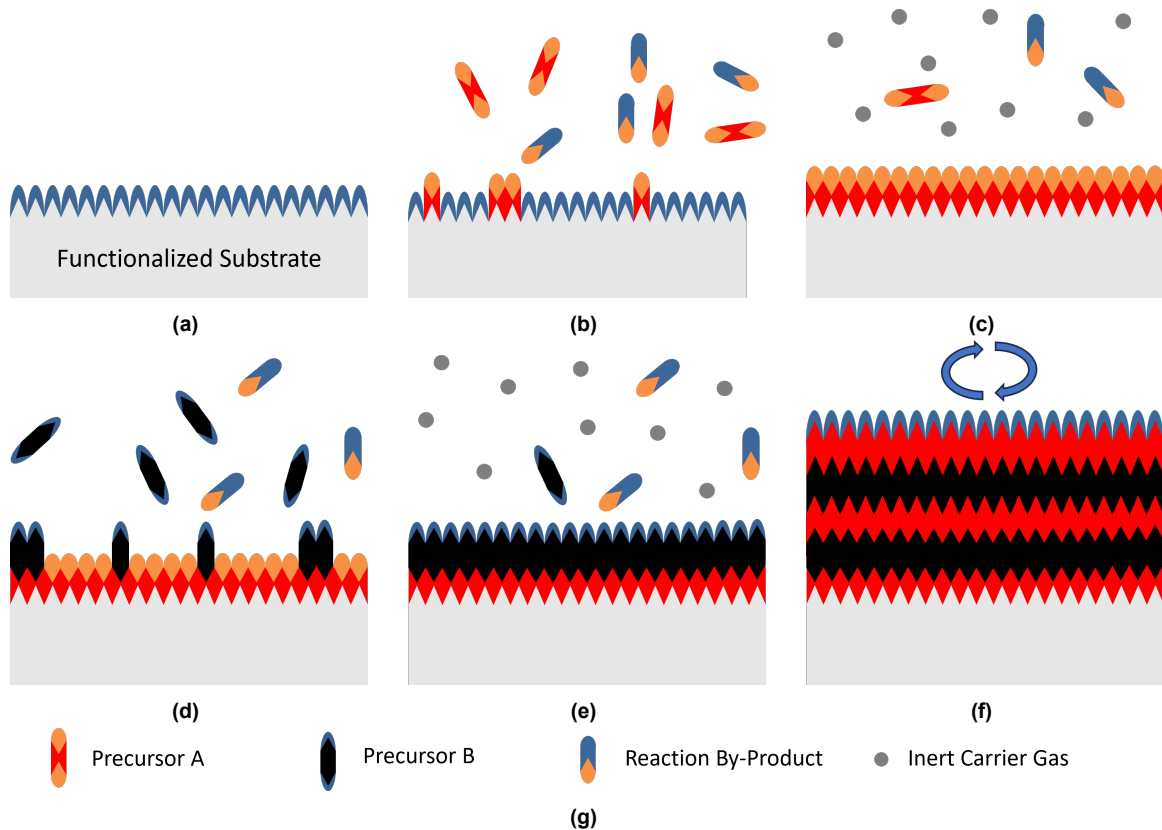


Figure 3.7: Atomic Layer Deposition schematic. (a) Substrate with a functionalized surface. (b) Precursor A pulse. (c) Precursor A and reaction by-products purge with inert gas (usually Argon). (d) Precursor B pulsed. (e) Precursor B and reaction by-products purged (with optional post-purge plasma reaction step). (f) Repeat steps b-e until desired thickness is achieved; adapted from [46]

As mentioned in Figure 3.7, Plasma Enhanced ALD can be utilised to lower the processing temperature, reduce purge times by eliminating the need for H_2O as a precursor, reduce nucleation times, and enable deposition of complex Nitrides and

other alloys that would've been challenging using Thermal ALD steps [47].

3.4. DRIE of High Aspect Ratio TSVs

3.4.1. DRIE Test Structure Patterning

Two types of test structures were designed, first, to determine the effects of Aspect Ratio Dependent Etching (ARDE), and second, to etch vias for cryogenic and room temperature electrical characterisation. ARDE tests were performed on vias of different diameters on the same sample to gauge if it is feasible to have varying aspect ratios across the sample. It is important to perform this test since we need a lower bound for the density of vias that we can etch in our sample without compromising the mechanical integrity of our wafer.

The ARDE test design is shown in Figure 3.8 and consists of vias with diameters in the range $10\mu\text{m}$ - $100\mu\text{m}$ and pitches in the range $17.5\mu\text{m}$ - $140\mu\text{m}$. The pattern was repeated multiple times across the $2\text{cm} \times 2\text{cm} \times 300\mu\text{m}$ sample to gauge the uniformity of etch rate across a small area. The vias were oriented in such a way that cleaving along any line in the XY-axis will yield an appropriate cross-section of the etched vias that can be observed in the SEM.

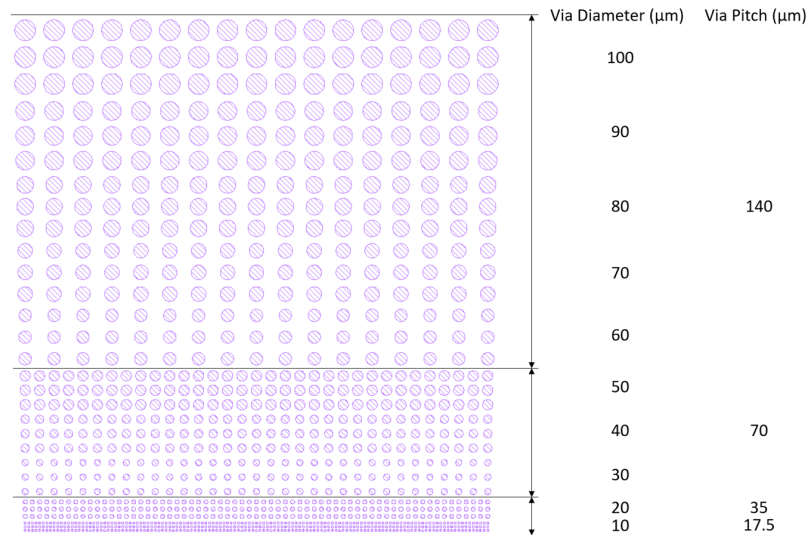


Figure 3.8: Aspect Ratio Dependent Etching Test pattern with vias of different diameters and pitched on a single substrate. No metal layers were patterned for the ARDE Test.

Based on the results from ARDE testing, further five mask designs were made for the cryogenic electrical characterisation of the $30\mu\text{m}$, $40\mu\text{m}$, $50\mu\text{m}$, $70\mu\text{m}$, and $100\mu\text{m}$ diameter TSVs. These samples were used for testing the efficacy of various sidewall coating methods (PVD, PECVD, ALD, ICPECVD), and for the final test structure patterning experiments. The TSV layout shown in Figure 3.9 has a varied patterning density across the sample to verify the uniformity of Silicon etch rates and test different metal patterning recipes with different photoresists.

3.4.2. SiO_2 Hard Mask Patterning

Photoresist masks are usually not suitable for TSV Bosch Etching since their etch selectivity is usually in the range of 50-100 [48]. It is possible to protect the mask

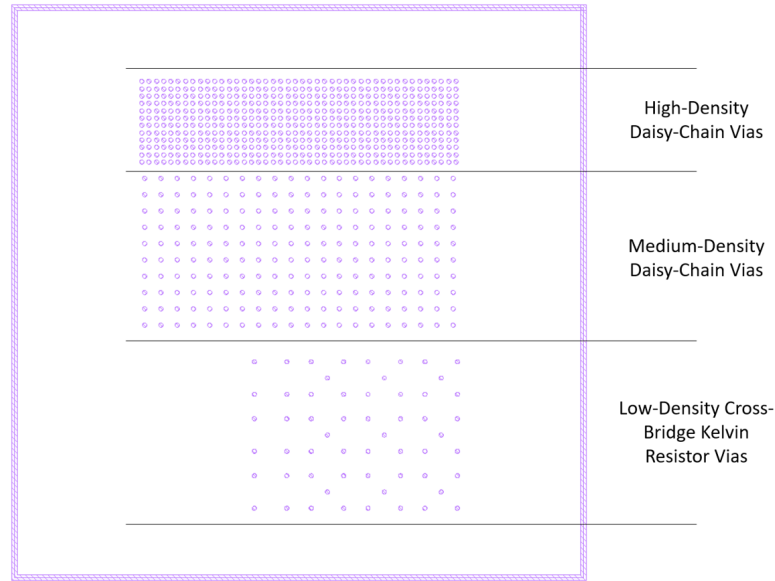


Figure 3.9: Example of holes patterned for 50 μ m vias, the other hole diameters follow a similar convention.

to some degree by carefully tuning the bias voltage, but this process is not easily reproducible or scalable with different designs of varying TSV densities. Therefore, a SiO₂ hard mask was deemed suitable for our application as it can provide etch selectivity to Silicon of above 150. The 300 μ m thick double-side polished Silicon wafer was deposited with 5 μ m of PECVD Silicon Oxide on the TOP side (for use as the hard mask), and 1 μ m of PECVD Silicon Oxide on the BOTTOM side for use as the etch stop layer. The patterning steps for the hard mask fabrication are listed in Recipes A.1 and A.2.

The cooling steps have been added to the Recipe A.2 to avoid burning the S1813 photoresist mask due to the high plasma power. The sample holder is brought down to 200mm from the plasma source since this part of the chamber has a lower ambient temperature compared to the top part near the plasma source. The results after Recipes A.1 and A.2 are shown in Figure 3.10.

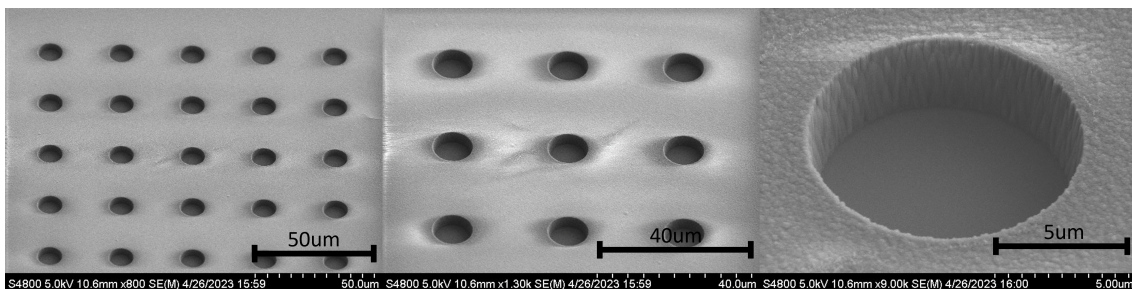


Figure 3.10: SEM images of Silicon Oxide hard mask, with landing on the Silicon substrate, showing uniformity over the surface and shape of the hard-mask sidewall.

3.4.3. Straight TSV Etching

After successful patterning of the SiO_2 hard mask, ARDE tests were performed to fine-tune the Bosch process etching and passivation pulsing times, substrate temperature, cooling times, and etch rates. TSVs were formed by DRIE of Silicon for a duration of 15 min (without cooling steps) according to the Recipe A.3. The first iterations were done on the ratio of pulsing times of SF_6 and C_4F_8 with the starting value of $7_{\text{sec}} : 2_{\text{sec}} = 3.5$.

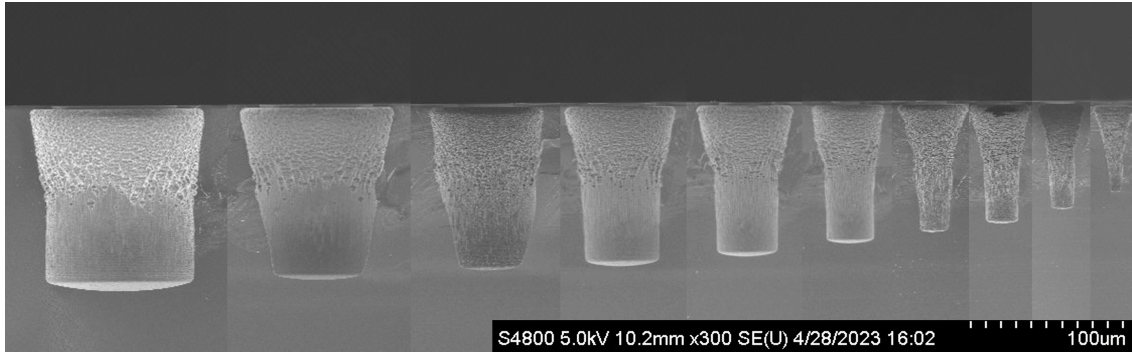
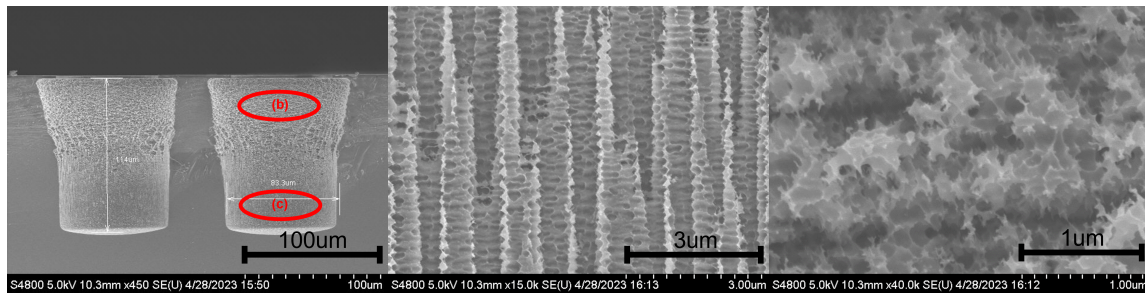


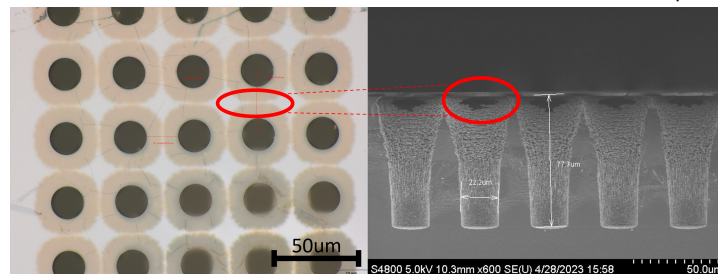
Figure 3.11: ARDE test results for Recipe A.3.



(a) 80μm Diameter Via.

(b) Sidewall roughness in the top part of the TSV.

(c) Sidewall roughness in the middle part of the TSV.



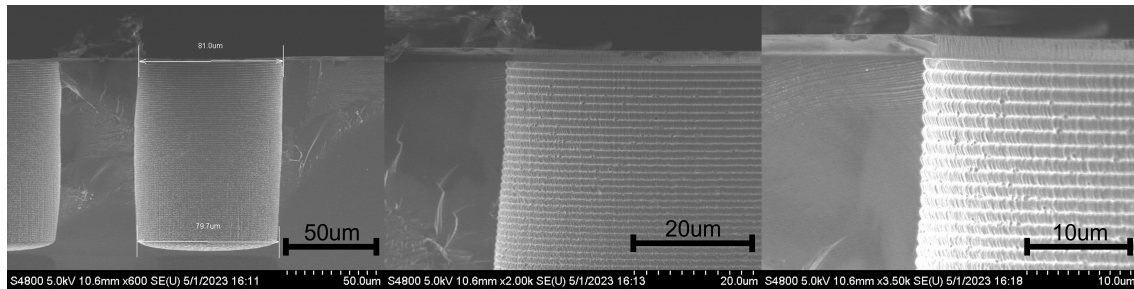
(d) Pronounced etching under the SiO_2 hard-mask of 10μm due to low C_4F_8 flow rate (150 sccm) which resulted in improper sidewall passivation on the top part of the TSV. The funnelled shape can be utilised for future TSV filling steps.

Figure 3.12: ARDE test results for Recipe A.3.

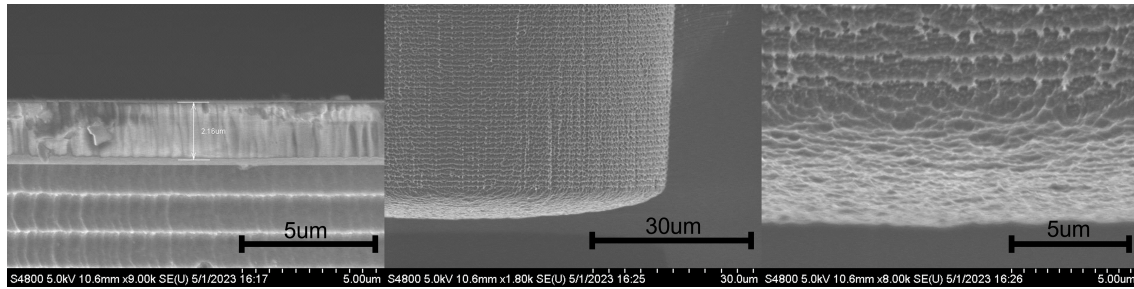
Recipe A.3 resulted in the vias as shown in Figure 3.11 and 3.12, with the top opening of the via having a conical opening shape with large ($10\mu\text{m}$) undercuts along the hard mask. It was theorised that this is due to insufficient pulsing time during the passivation step. Therefore, the next iteration of the recipe increased the ratio of pulsing times of SF_6 and C_4F_8 to $7.4_{\text{sec}} : 2.3_{\text{sec}} = 3.2$, increased the C_4F_8 flow to 245

sccm, and kept the other parameters constant as shown in Recipe A.4. The power was increased to 2200W to compensate for this increase in passivation pulse time, and the substrate temperature was reduced to 0°C for better substrate cooling.

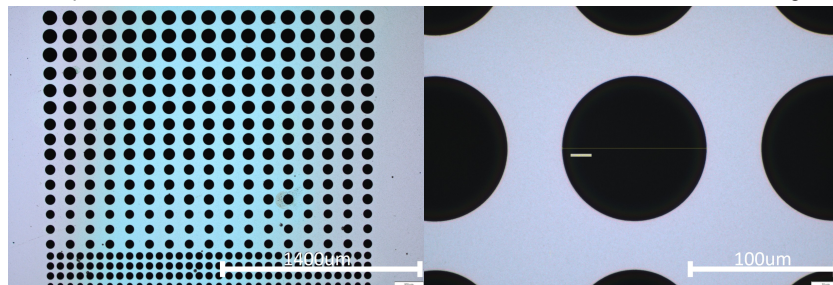
The resulting vias had a slightly slowed etch rate as demonstrated in Table 3.1, but features perfectly straight openings with negligible undercuts (<300nm) which were almost the same dimensions as the scallops. Figure 3.13 showcases the results after 15 min of etching with Recipe A.4. The scallop pattern is uniform and the sidewall roughness is within expectations for the top and middle part of the etched TSV.



(a) Closeup of top part of the TSV showcases minimal undercuts and uniform scallop pattern.



(b) Closeup of the hard mask and bottom of the TSV showcases minimal micro-masking effects.



(c) ARDE test pattern showcasing no undercutting for all TSV test diameters.

(d) Closeup of 100µm TSV opening showcasing no undercutting and no hard-mask chipping effects due to overheating.

Figure 3.13: Closeup of via-sidewall for Recipe A.4.

Recipe A.4 was extended to 1 hr of etch time and the results are showcased in Figure 3.15. The undercut seen here has a different sidewall profile compared to the one seen in Figure 3.11. It was theorised that this shape is not due to insufficient passivation, but rather due to burning and removal of said passivation due to improper cooling and high surface temperatures attained during the high power (2200W) etching of Silicon. This problem with cooling of the substrate may be occurring due to the usage of a Quartz carrier wafer for holding the small 2cm x 2cm test samples inside the reaction chamber as shown in Figure 3.15. This prevents the Helium coolant from

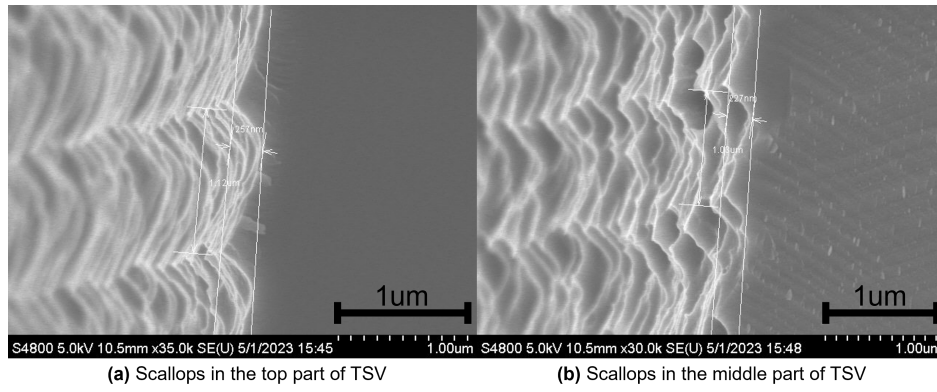


Figure 3.14: Closeup of scallops in the top and middle of the TSV for Recipe A.4. The sidewall roughness is within reasonable limits and does not necessitate a reduction of etching and passivation step times for even smaller scallop widths.

Table 3.1: Silicon DRIE Etch Rates showcasing Aspect Ratio Dependent Etching

Feature Diameter (μm)	Etch Rate Recipe A.3 ($\mu\text{m}/\text{min}$)	Etch Rate Recipe A.4 ($\mu\text{m}/\text{min}$)
100	7.73	6.5
90	7.53	6.43
80	7.2	6.42
70	6.66	6.36
60	6.58	6.14
50	5.95	6.04
40	5.55	5.84
30	5.18	5.47
20	4.56	5.19
10	3.8	4.55

being in direct contact with the sample and reduces the heat flux between the sample and the chuck.

To alleviate this failure mode, a 30 sec cooling step was added for every 3 min of etching while keeping the other parameters the same, as shown in Recipe A.5. The etching process was split into two parts of varying SF_6 and C_4F_8 pulsing times, with the second step having a ratio of $8.4\text{sec} : 2.5\text{sec} = 3.36$. This was done to compensate for the effects of *Knudsen Transport* that can lead to tapering in the TSV sidewalls and slow the etch rate as well [49]. The parameters m and n in Recipe A.5 can be adjusted to increase or decrease the etching time depending on the aspect ratio of the desired TSV.

The results of Recipe A.5 can be seen in Figure 3.16 and prove that the previous passivation burn theory was correct. This recipe was tested for etching time of beyond 3 hours for 20 μm diameter vias, and still did not lead to any noticeable hard-mask undercuts and can be scaled to suit a variety of aspect ratios simply by tuning the loop counts for each of the two cycling steps. Hence, Recipe A.5 should be considered to be the primary DRIE procedure for all experiments from this point on in the thesis.

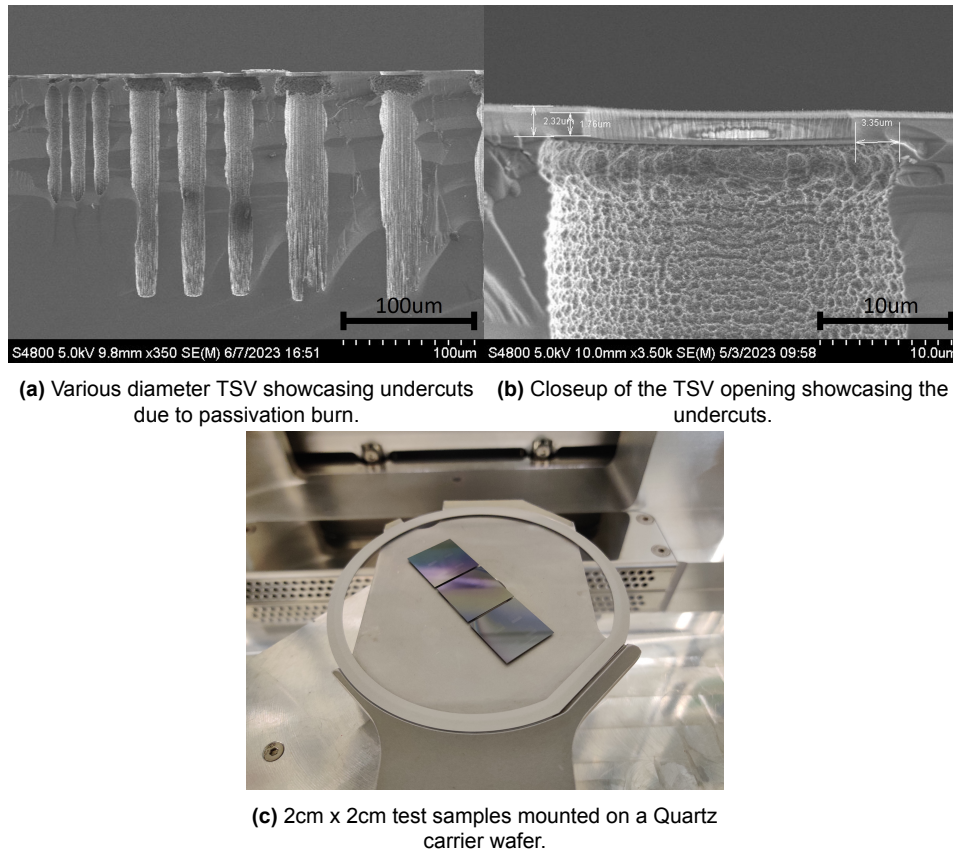


Figure 3.15: Undercuts due to passivation layer burn during 1 hr long etching cycles of Recipe A.4.

3.4.4. Post-DRIE Sample Cleaning

The etched TSV samples are cleaned using Acetone and IPA at room temperature immediately after dismounting from the carrier wafer. The samples are then cleaned with Oxygen plasma as shown in Step 6 of Recipe A.1. This is followed by immersion in fuming Nitric Acid at 40°C for 10 min (under ultrasonic agitation) for removal of organic compounds, and subsequent immersion in 7:1 BOE solution at 40°C for 30 min (under ultrasonic agitation) for removal of the leftover SiO₂ hard-mask. The resulting samples feature a bare silicon surface and must be handled with care.

The TSV samples are now ready for sidewall coating. They are particularly fragile at this stage due to the thin substrate size (300 μm) and the absence of metallic layers on the surface. Even minute damage or contamination to the surface of the sample will result in delamination of the subsequently deposited oxide and metallic thin films.

3.5. TSV Sidewall Dielectric Coating

At cryogenic temperatures, Silicon behaves like an insulator. However, the project requirements dictate that the High-Voltage chip should act as the active interposer between the RF and optical chips. This means that the TSV parasitic capacitance will also have a prominent impact on its circuit operation [50]. The following materials were evaluated for fulfilling this role:

- *Benzocyclobutene (BCB)* has attractive properties for liner applications due to

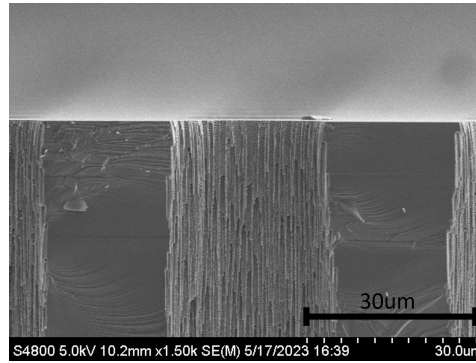


Figure 3.16: SEM image showcasing lack of undercuts resulting from cooling steps added in Recipe A.5.

its low dielectric constant (reduces TSV capacitance), and thermal stability after hard-curing ($>350^{\circ}\text{C}$). Lee et al. have demonstrated the use of BCB as a TSV liner [51], and well-defined industrial processes already exist for its application.

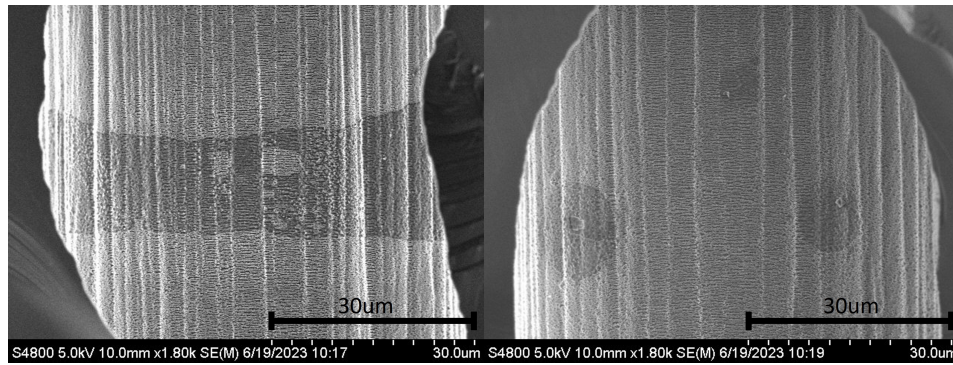
- *Parylene-C* can be considered as an alternative to BCB since its properties are better characterised at cryogenic temperatures. It also has a straightforward vacuum deposition process that does not alter the thin membranes, it is robust to further processing steps and has a CTE similar to Silicon [40].
- SiO_2 liner can be easily grown using thermal oxidation of Silicon, however, thermal oxidation will not be compatible with our via-last approach of TSV fabrication. Therefore, PECVD or ICPECVD deposition of SiO_2 is the best option as it is CMOS compatible and easily tunable to meet our specific requirements.
- Al_2O_3 is another option to consider as it has been proven to reduce TSV capacitance when compared to a SiO_2 liner in a study by Zhang et al. [52]. Moreover, low- κ dielectrics with low modulus of elasticity (like Al_2O_3) have been shown to improve reliability in TSVs by reducing thermo-mechanical stress between the metal coating in the substrate [53]. Al_2O_3 can also be easily coated in high aspect ratio TSVs by ALD techniques, thereby giving us a highly conformal and stress-free deposition along the sidewalls.

Out of the above-mentioned options, PECVD SiO_2 and ALD Al_2O_3 were chosen to be tested for this project due to availability of equipment and compatibility with successive processing steps. Polymer processing can also interfere with the operation of the SiN waveguides and the MEMS switches in our Photonic chip due to complications in its removal and subsequent descum steps involved.

3.5.1. SiO_2 PECVD Deposition

TSV coating experiments were performed on $300\mu\text{m}$ deep TSVs with diameters of $30\mu\text{m}$, $40\mu\text{m}$, $50\mu\text{m}$, $70\mu\text{m}$, and $100\mu\text{m}$. The samples were coated with a 850nm layer of PECVD SiO_2 on both sides at a substrate temperature of 300°C .

As seen in Figure 3.17, this technique cannot adequately coat the sidewalls of TSVs with diameter $\leq 50\mu\text{m}$. The SiO_2 coating thickness in the middle of the $70\mu\text{m}$ and $100\mu\text{m}$ TSVs was in the range of 180nm to 300nm , which was sufficient to ensure a repeatable oxide coating for successive TSV metallization experiments. ICPECVD



(a) SEM Image of the middle section of 50 μ m TSV showcasing incomplete coverage of PECVD SiO₂. (b) SEM Image of the middle section of 50 μ m TSV showcasing quality of deposition around debris.

Figure 3.17: PECVD SiO₂ coating of 50 μ m diameter, 300 μ m deep vias. The curved sidewall shape is due to cleaving angle and does not reflect actual sidewall angle.

deposition of SiO₂ yielded similar results to PECVD deposition with a slightly better thin film quality in the coated regions of the via. Next, ALD coating of Al₂O₃ was investigated for TSVs under 70 μ m in diameter.

3.5.2. Al₂O₃ ALD Deposition

Atomic Layer Deposition has been studied for both SiO₂ [54], and Al₂O₃ [55] with promising results for coating ultra-high aspect ratio TSVs (aspect ratio $\geq 30 : 1$). Al₂O₃ was chosen for this experiment due to the fast deposition rates (up to 50nm per 1hr 30min) compared to SiO₂ (≥ 2 hr for 50nm), and relatively simple precursors (TriMethylAluminum (Al(CH₃)₃) compared to SiO₂ (Di(Isopropylamino)Dimethylsilane, H₂Si[N(C₂H₅)₂]₂). Al₂O₃ has also been demonstrated as a reliable low- κ material with a low CTE mismatch to Silicon, and with a proven reduction in capacitance of about $\sim 26\%$ when compared to plasma-enhanced tetrahydrothosilicate (PETEOS) oxide lined Cu-filled TSVs.

30 μ m, 40 μ m, and 50 μ m diameter TSV samples were coated with 50nm of ALD Al₂O₃ on both sides at a substrate temperature of 300°C. The results in Figure 3.18 showcase that the deposition was highly conformal even for 30 μ m diameter TSVs, and the coating thickness in the middle of the TSV was ~ 100 nm owing to the double side deposition technique used. Special care must be taken to clean the bare Silicon sample before this ALD process to ensure that the initial surface functionalization step is successful. Failure to do so will result in delamination of the thin film as shown in Figure 3.19.

3.6. TSV Sidewall Metallization

3.6.1. NbTiN Physical Vapour Deposition

Based on the equipment availability and results of the thermal simulation, two candidates were chosen for metallization of the TSV sidewall, NbTiN and TiN. NbTiN was deposited using Physical Vapour Deposition (a.k.a. Sputtering), which is the physical ejection of particles from a target material by means of energetic ion bombardment. A negative bias is applied to the cathode (i.e. the target disk) and a positive bias is

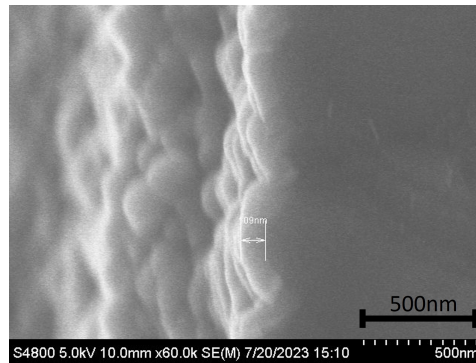


Figure 3.18: TSV sidewall showcasing coating thickness of ALD Al₂O₃.

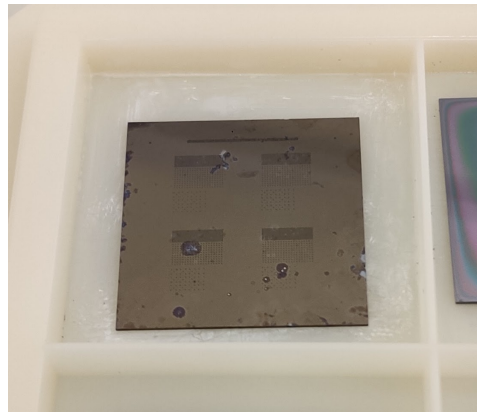


Figure 3.19: Unsuccessful Al₂O₃ ALD due to poor surface functionalization.

applied to the anode (i.e. the substrate/wafer/sample).

A key feature of PVD is the ability to perform *Reactive Sputtering*, which enables deposition of compounds on the substrate. The reaction primarily takes place at the target surface since there is a relatively larger release of energy when incident ions bombard the target [16]. This is a useful property since we want to deposit thin films of NbTiN, which can be easily generated by bombarding a NbTi target disk with high energy Argon plasma in the presence of a constant Nitrogen gas flow. Another key characteristic of Sputtering is the randomness of the particles that are released from the target disk; as a result of this, deposition conformality is usually not as high as other processes like ALD or CVD.

NbTiN was sputtered on 30 μ m, 40 μ m, 50 μ m, 70 μ m, and 100 μ m diameter vias at a chamber pressure of 2.3 mTorr, 250W power, N₂ flow rate of 4 sccm, Ar flow rate of 50 sccm, with a resulting bias voltage and current readings of 343V and 728mA. Sputtering was performed for a total of 8 min to achieve a film thickness of 200nm (on the surface of the sample). Figure 3.20 showcases the coating results of this experiment on different aspect ratio vias, with vias of diameter $\geq 70\mu$ m being successfully coated with the NbTiN thin film without delamination, shadows, or cracks in the layer. The 30 μ m, 40 μ m, and 50 μ m vias were not coated with the thin film beyond 10-40 μ m beyond the opening of the via.

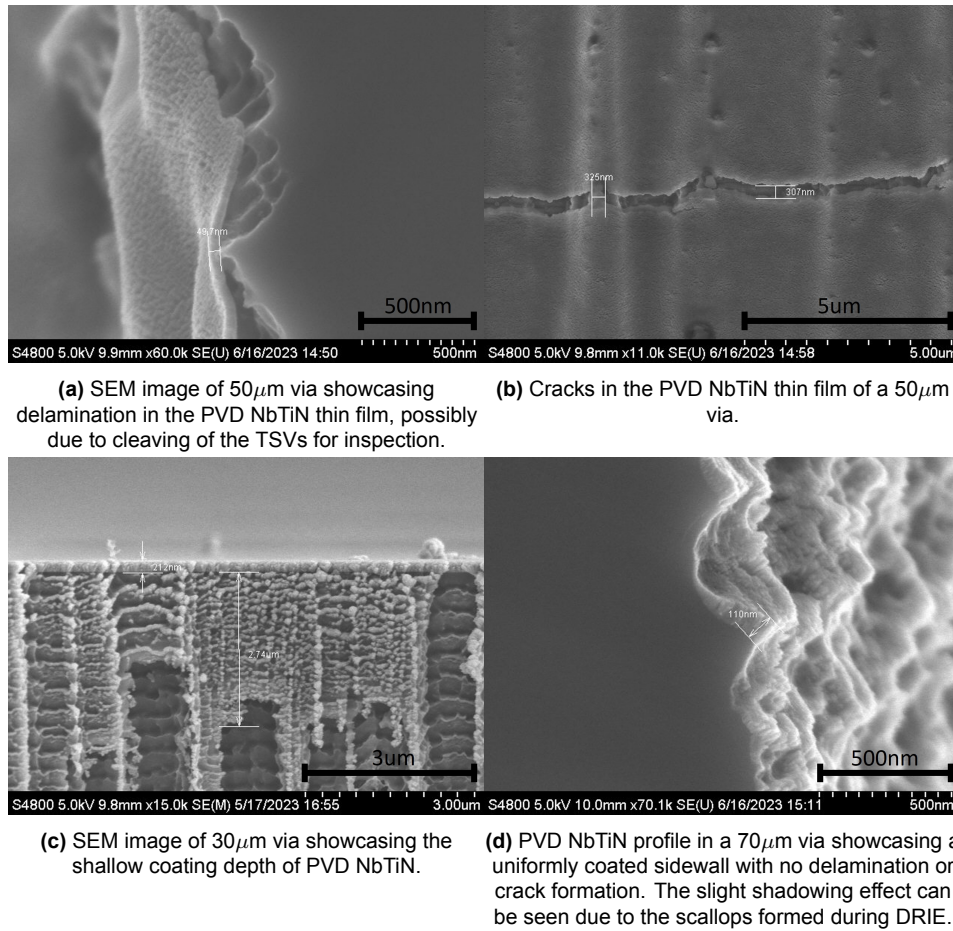


Figure 3.20: Results of NbTiN CVD metallization of 30 μ m, 50 μ m, and 70 μ m TSV sidewalls.

3.6.2. TiN ALD Deposition

Due to PVD coating failures of 30 μ m, 40 μ m, and 50 μ m TSVs, ALD deposition of TiN was experimented upon next. Plasma Enhanced ALD was utilised in a Nitrogen reactive atmosphere at a substrate temperature of 270°C and using TDMAT, $(\text{Ti}(\text{N}(\text{CH}_3)_2)_4)$ as the precursor. The process is similar to the one described by Musschoot et al. [56] with a slightly longer plasma step of 10sec. The deposition was done for 1500 cycles to achieve a film thickness of 100nm on only one side of the sample to accurately gauge the coating efficacy in the middle of the TSVs.

The results are shown in Figure 3.21 and indicate that repeatable ALD coating of $\sim 30\mu\text{m}$ TSVs may not be feasible. The samples with via diameters $\geq 40\mu\text{m}$ all showed excellent coverage of ALD TiN on the TSV sidewall. Nevertheless, all three aforementioned via diameters were coated for the next patterning and measurement experiments to gain conclusive results regarding the usage of 30 μm vias in the final interposer design.

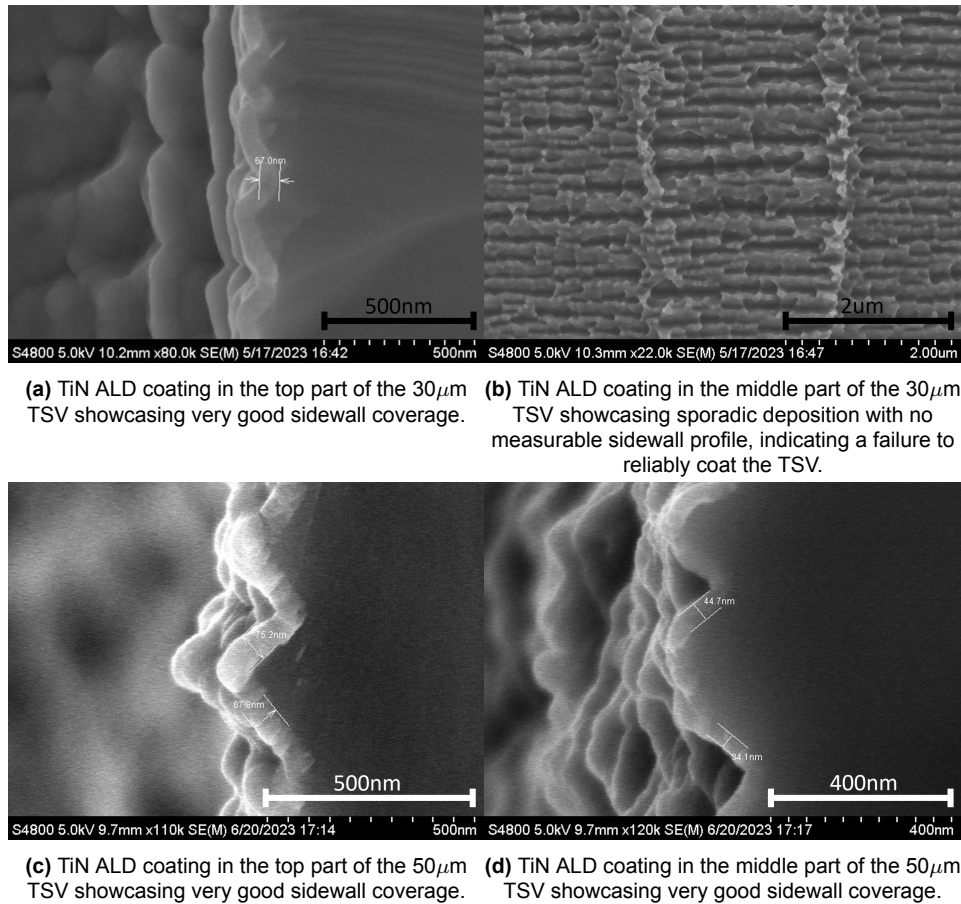
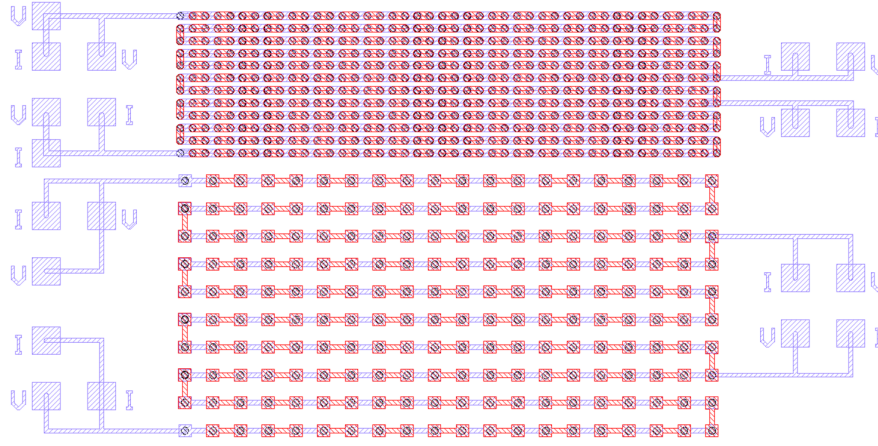


Figure 3.21: Results of TiN ALD metallization of 30 μ m and 50 μ m TSV sidewalls.

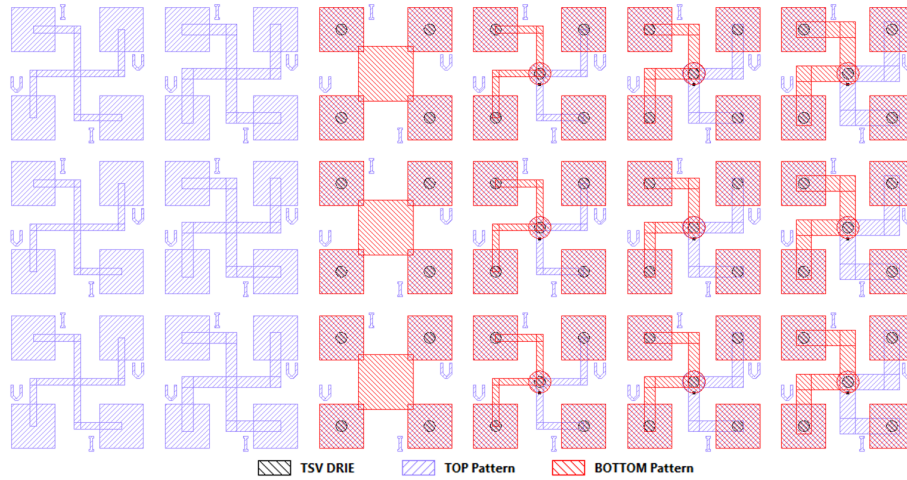
3.7. Electrical Characterisation Test Structures

After coating the 30 μ m, 40 μ m, and 50 μ m TSVs with 50nm ALD Al_2O_3 and 100nm ALD TiN (dual side), and the 70 μ m, and 100 μ m TSVs with 1 μ m PECVD SiO_2 and 200nm PVD NbTiN (dual side) the samples showed no delamination around the TSV openings or along the surface of the sample. The next step was patterning the electrical test structures which consisted of two daisy chains (high and low via density) and multiple Cross-Bridge Kelvin Resistor (CBKR) structures for 4-wire resistance measurement.

For superconductivity measurements, it is important to compare the resistance of planar structures with the structures interrupted by TSVs as shown in Figure 3.22. The bonding pads were designed large enough (200 μ m x 200 μ m) to be easily probed or wire bonded for placement in different types of cryostats. The daisy chain densities were varied across a single sample to gauge the patterning capability of different types of photoresists in samples containing TSVs.



(a) Design for 50 μ m TSV daisy chain resistance measurements, containing high density (top, 530 total vias, 90 μ m pitch) and low density (bottom, 200 total vias, 200 μ m pitch) daisy chains on a single substrate.



(b) Design of Van der Pauw structures for 50 μ m TSV 4-wire resistance measurements.

Figure 3.22: Patterns for electrical characterisation of 50 μ m TSVs. The other TSV aspect ratios follow a similar design convention.

3.7.1. Interposer Patterning

Since the test samples at this stage consist of etched TSVs with just sidewall metallization without complete filling, placing the samples on a vacuum chuck for photoresist spinning is not feasible. In such scenarios, multiple techniques can be used to attach the sample to the vacuum chuck [57]:

- *Pocket Wafer Bonding.* Pockets are etched using DRIE or KOH etching in a 4-inch Silicon wafer to make cutouts that can exactly fit the test samples. The deeper the pocket (and thicker the wafer) the more stable the sample will be during spinning. A major disadvantage of this method is its inflexibility to accommodate different sample sizes on the same pocket wafer, requiring the fabrication of multiple carrier wafers for different sample sizes.

- **Kapton Tape.** Double-sided Kapton Tape is easy to use and remove, and ideal for substrate with patterns on both sides (like our interposer). However, baking the photoresists at high temperatures can degrade the adhesion quality of such tapes and may even leave behind some residue on the surface of the sample.
- **Photoresist Bonding.** It is the most easily available, easily applicable, and cleanest method to mount double-side-polished samples on a carrier wafer. It can support a variety of samples on the same carrier wafer and is easy to remove with a basic Acetone and IPA cleaning cycle. This method is utilised in this project for mounting the etched and metallized samples on the vacuum chuck for photoresist spinning, and the procedure for this mounting is described in Recipe A.6.

A major failure mode when it comes to the patterning of high aspect ratio structures like TSVs is over-etching along the edge of the structure. For low-viscosity liquid photoresists, the resist film forms a curved shape along the edge of the TSV as shown in Figure 3.23. Recipe A.7 was first used to coat the samples with relatively low-viscosity MAN1410 negative resist, and the samples were then patterned using RIE with SF_6 flow of 13.5 sccm, O_2 flow of 5 sccm, 55W of RF power, and 10 μbar chamber pressure. The result of these steps can be seen in Figure 3.23 and clearly showcases the over-etching effect discussed previously.

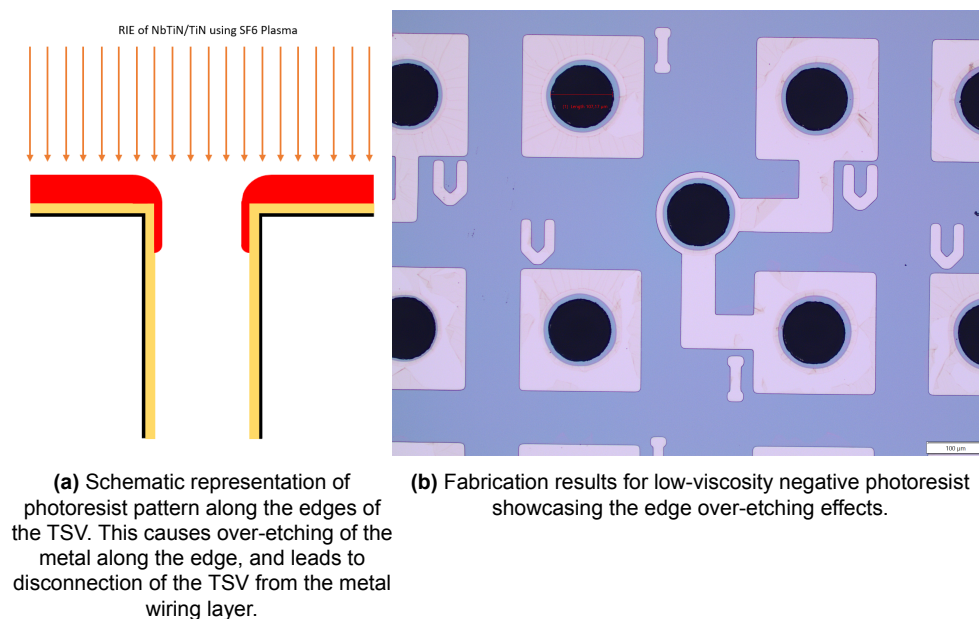


Figure 3.23: Overetching effects seen during TSV patterning due to the shape of the photoresist along the TSV opening.

We can reduce the effects of this over-etching in two ways; (i) Using a dry-film photoresist which is applied by a die bonder or a rolling assembly bonder. This dry photoresist will not enter the holes of the TSV and prevent over-etching of its edges and sidewalls, or (ii) Using a high viscosity photoresist that does not flow over the edges of the TSV, but rather hangs off it after baking. For this experiment, the second option was used as a proof of concept since the fabrication complexities are not too

extreme, unlike the dry-film method. AZ10XT positive photoresist was chosen for this purpose as it has very high film thicknesses when coated at lower spinning RPMs, as shown in Recipe A.8. The samples were then patterned using RIE with SF_6 flow of 13.5 sccm, O_2 flow of 5 sccm, 55W of RF power, and $10\mu\text{bar}$ chamber pressure. The leftover resist was cleaned using AR600-71 solution @ 50°C under ultrasonic agitation for 10 min, followed by an IPA clean for 2 min.

The results of the new patterning recipe can be seen in Figure 3.24 and showcase that patterning low-density structures using this method yields good results with no over-etching. However, high-density daisy chain structures cannot be patterned properly since the photoresist faces problems with surface adhesion. The samples developed bubbles and cracks in these high-density parts after the baking step and as a result, these test structures were rendered unusable. Another approach that can be feasible is filling the TSVs with a polymer like Parylene-C after metallization to prevent etching of the exposed TSV sidewall by the SF_6 plasma. However, filling ultra-high aspect ratio vias with Parylene-C has its own challenges like void formation and CTE mismatch with metallized sidewalls at cryogenic temperature.

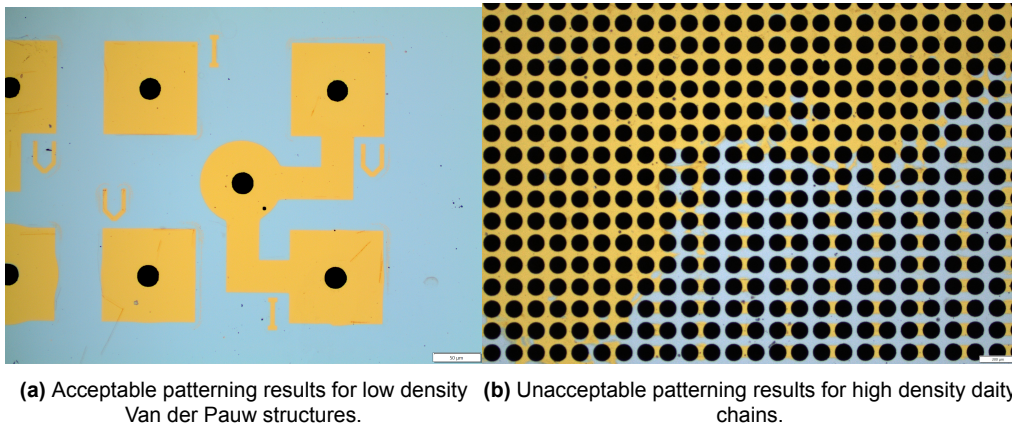


Figure 3.24: Patterning results for AZ10XT thick photoresist coating.

3.8. Conclusion

In this chapter, process recipes were developed and optimised for etching, metallization, and patterning of ultra-high aspect ratio Through Silicon Vias based on the simulation results from Chapter 2. Various daisy-chain and Van der Pauw structures were designed and patterned in preparation for cryogenic testing of the samples. Vias from $10\mu\text{m}$ diameter and $17.5\mu\text{m}$ pitch up to $100\mu\text{m}$ diameter and $140\mu\text{m}$ pitch can be fabricated with the developed recipes. Vias with opening diameter $\leq 50\mu\text{m}$ were lined with ALD Al_2O_3 and ALD TiN, and those with opening diameter $\geq 70\mu\text{m}$ were lined with PECVD SiO_2 and PVD NbTiN. Fabrication hurdles still remain in the patterning of fine-pitch TSVs due to photoresist adhesion issues, however, suggestions were made to alleviate some of these problems in future experiments.

In the next chapter, we will study Indium Microbumps and their integration potential in our 3D assembly. We will discuss the deposition, lift-off, and reflow of Indium Microbumps and showcase the flip-chip bonding of two substrates with the help of said microbumps.

4

Flip Chip Bonding using Indium Microbumps

4.1. Introduction

Flip-chip bonding technique can play a significant role in realizing large-scale quantum computers with 1000s of integrated qubits. It enables the separation of functional units of Quantum ICs such as low-temperature control electronics and photonic circuitry along with high-density interconnects between them. While Through Silicon Vias allow for electrical interconnections between the TOP and BOTTOM of a single substrate, Flip-Chip Bonding allow interconnects spanning multiple chiplets. As explained in Chapter 1, multiple techniques like adhesive bonding, metal-metal direct bonding, and direct oxide bonding can be employed for achieving such flip-chip bonded assemblies. In the specific application domain of Quantum Computers, we have additional requirements when choosing a 3D integration scheme for our assembly that must be compatible with our qubit architecture [20]:

- Microbumps must be compatible with Qubit fabrication process flow, which deviates considerably from traditional CMOS process flow.
- Fabrication yield must be high, especially along the control signal lines (>99.9%) compared to ground plane connections.
- Materials must be chosen keeping in mind the Coefficient of Thermal Expansion (CTE) mismatch and mechanical stability during cryogenic cooling cycles.
- Bonding must be performed at relatively low temperatures to avoid changing the implantation characteristics of the diamond-based colour centres.
- Interconnects must ideally be superconductive at the operational temperatures to avoid local heating and enable near-lossless connection between CryoCMOS and Photonic circuitry.

As discussed in Chapter 3, thermal simulations have shown that due to high thermal conductivity of Indium, maintaining a low heat-flux dictates reducing the total number of microbumps considerably, thereby affecting the functionality of the interposer assembly. It was recommended to achieve direct bonding using NbTiN pillars

of thickness $\geq 10\mu m$. However, a problem arises when aiming to bond such thick films of sputtered materials, the surface roughness goes beyond the requirements for plasma-enhanced direct bonding. As demonstrated by Fujino et al. [23], the surface roughness of $\sim 1nm$ RMS is required to reliably bond metal surfaces, and this necessitates polishing steps in thicker metallic films. Figure 4.1 shows that even $1.3\mu m$ thin films of PVD NbTiN fall way beyond the specification of 1nm RMS surface roughness, and are therefore unsuitable for use in a direct metal bonding scheme.

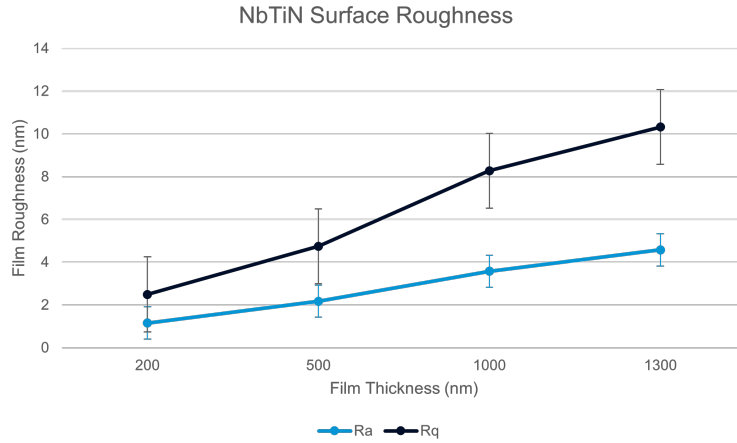


Figure 4.1: AFM microscopy of PVD NbTiN surface roughness for higher deposition thicknesses, demonstrating the need for extra polishing steps to prime the surface for direct bonding.

A compromise between these two bonding schemes (Indium Reflow Bonding and NbTiN Direct Bonding) is the use of Indium Microbumps as the adhesive layer between relatively tall NbTiN pillars. The Indium bumps do not require ultra-high surface smoothness for undergoing proper reflow and can be fabricated on high aspect ratio pillars as has been demonstrated for Cu/Sn/Cu bonding schemes [58]. The schematic for this type of bonding scheme is given in Figure 4.2

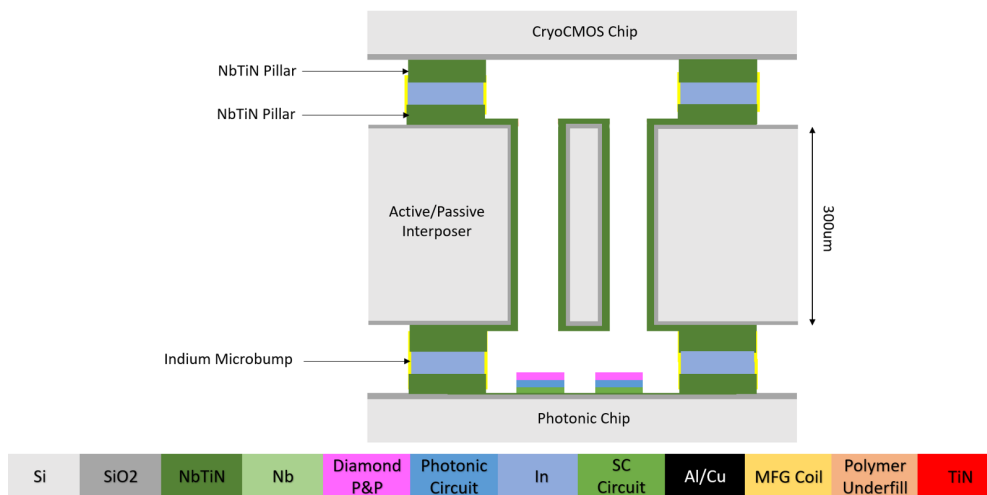


Figure 4.2: Design proposal for a hybrid bonding scheme consisting of Indium Microbumps acting as an adhesive/superconductive contact between NbTi/NbTiN pillars.

This chapter will focus on the fabrication of such Indium Microbumps and elaborate upon the processes involved in the deposition, lift-off, and reflow of Indium Microbumps in an effort to integrate them into a cryogenic interposer system.

4.2. Theory of e-Beam Evaporation

There are multiple ways to deposit Indium, with the most commonly studied ones being *Electron-Beam Evaporation* and *Electroplating*. Electroplating is mainly used to deposit large quantities of Indium in a short deposition period (1.5 mils/hour at a current density of 20 amperes/ft [59]). However, due to these fast deposition rates, electroplated Indium is prone to void formation and porous deposition as shown in Figure 4.3. The deposited Indium is also damaged during the seed layer removal step due to Argon ion bombardment [60].

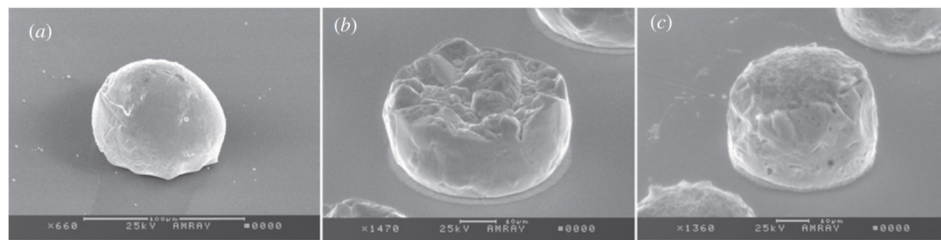


Figure 4.3: Negative effects of Indium Electroplating showcasing porosity of deposited Indium and negative damaging effects of the seed layer removal steps [60].

E-beam Evaporation is the alternative to electroplating and does not require a seed layer to start the deposition process. It has lower deposition rates ($2\text{\AA}^{\circ}$ - $15\text{\AA}^{\circ}/\text{sec}$) compared to electrodeposition, but as a result, promises a less-porous deposition quality and can enable deposition of a Gold oxide-prevention layer in the same equipment [28]. This Gold-capping-layer inhibits the formation of Indium Oxide (In_2O_3), which is the main deterrent to successful reflow and flip-chip bonding of Indium microbumps. Indium Oxide has a melting point of 1910°C (compared to 156.6°C for pure Indium) and hinders proper spherification of the deposited Indium by increasing its surface tension [61].

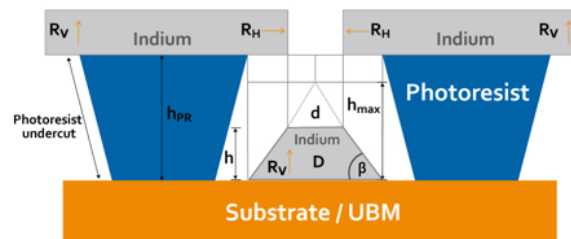


Figure 4.4: Schematic of Indium deposition for purposes of lift-off patterning.

In e-Beam Evaporation, as shown in Figure 4.5, the target material is bombarded with electrons generated by a charged Tungsten filament under a high vacuum. This

causes the particles of the respective material to gain enough energy to transform into its gaseous phase and precipitate into a solid form upon coming into contact with the substrate (which is usually cooled using Helium). It is a line-of-sight deposition technique since the evaporated metal particles travel in a straight line till they reach the target. This is a major advantage over processes like PVD since it makes lift-off and patterning much easier. The general rule of thumb is to limit the deposition thickness to $2/3$ the height of the photoresist used for lift-off as shown in Figure 4.4.

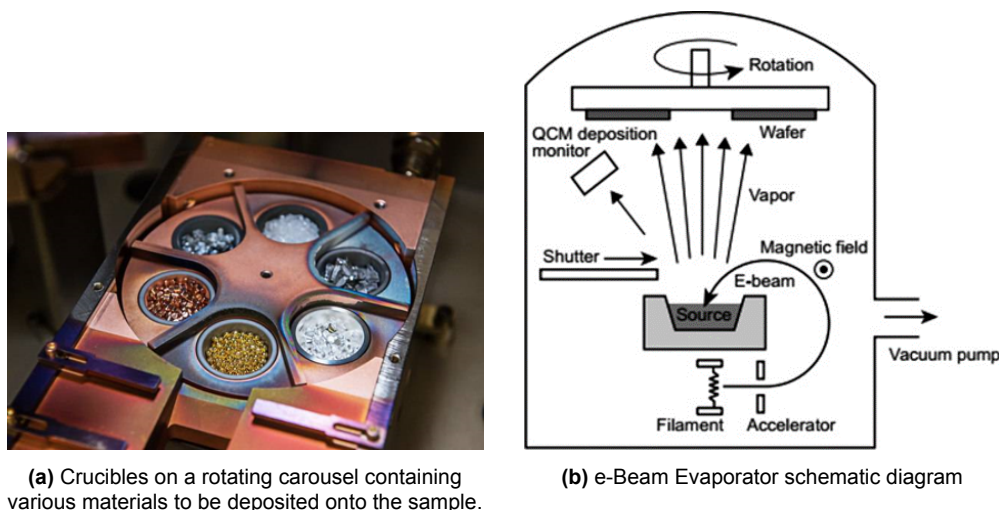


Figure 4.5: Electron-Beam Evaporator schematic showcasing ability to deposit multiple materials without removal of the sample from the vacuum.

4.3. Indium Deposition and Liftoff

As discussed in the previous section, e-beam evaporation was chosen as the Indium deposition method due to its flexibility, ability to deposit without a seed layer, and void-free deposition characteristics. Figure 4.6 shows the test pattern used for electrical characterisation of the flip-chip assembly and consists of 600 Indium Microbumps connected in a daisy-chain of $200\mu\text{m}$ pitch.

The wiring layer consists of 200nm thick PVD NbTiN, patterned into landing pads of $30\mu\text{m} \times 30\mu\text{m}$ size containing Indium Microbumps of $20\mu\text{m}$ diameter (pre-reflow) in the centre. The landing pads for wire bonding or probe-tip landing are of $200\mu\text{m} \times 200\mu\text{m}$ dimension and consist of bare 200nm thick PVD NbTiN. The patterning of the wiring layer was done using the MAN1410 negative photoresist according to Recipe A.7, and the patterns were transferred using RIE with SF_6 flow of 13.5 sccm, O_2 flow of 5 sccm, 55W of RF power, and $10\mu\text{bar}$ chamber pressure. The leftover resist was cleaned using AR600-71 solution @ 50°C under ultrasonic agitation for 10 min, followed by an IPA clean for 2 min.

The TOP and BOTTOM chips were patterned on the same substrate and were designed to be diced after reflow to save processing time and accommodate more samples inside the evaporation chamber. After patterning of the wiring layer, the sample was cleaned in Oxygen plasma to remove traces of photoresist still on the landing pads according to Step 6 of Recipe A.1.

The samples were then coated and patterned with a $6.8\mu\text{m}$ thick film of AZ10XT

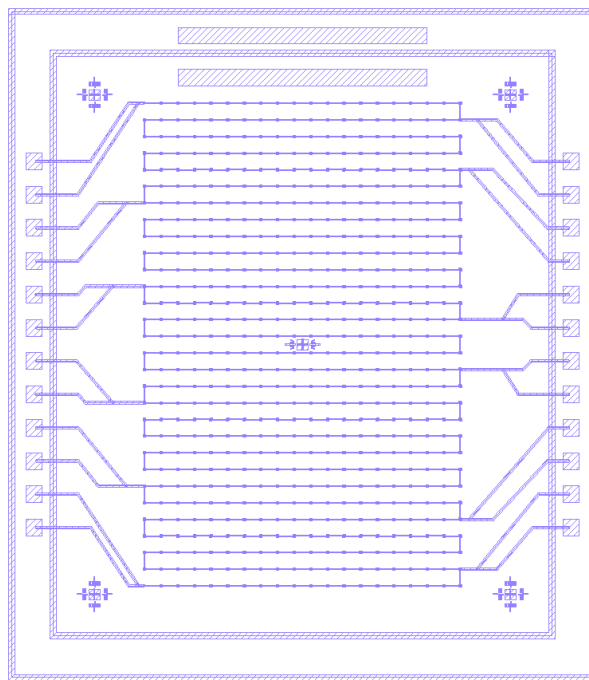


Figure 4.6: Daisy-chain pattern for electrical characterisation of the flip-chip assembly containing Indium Microbumps. 600 microbumps are connected in series with alignment markers in all four corners and the center (for angular alignment).

positive photoresist for the lift-off step according to Recipe A.9. Initially, a hard-baked ARN4450-10 negative photoresist was used for its characteristic property of side-wall overhangs, however, problems were faced during lift-off in AR600-71 solution as shown in Figure 4.7. The AZ10XT resist was chosen as a replacement due to its ease of removal and residue-less etching process.

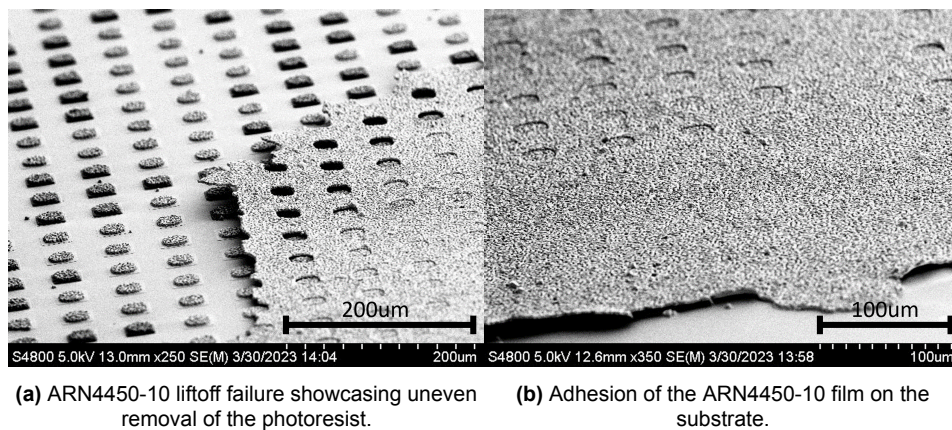


Figure 4.7: Poor liftoff results using ARN4450-10 Negative Photoresist.

A $1.5\mu\text{m}$ thick film of Indium was deposited using e-Beam Evaporation, the deposition rate was initially set to $2\text{Å}/\text{sec}$ for the first 100nm to ensure a uniform initial layer on the under-bump material (UBM). The deposition rate was subsequently ramped up to $12\text{Å}/\text{sec}$ to reduce the total deposition time. The evaporation equipment didn't feature active substrate cooling, however, this did not cause any noticeable problems

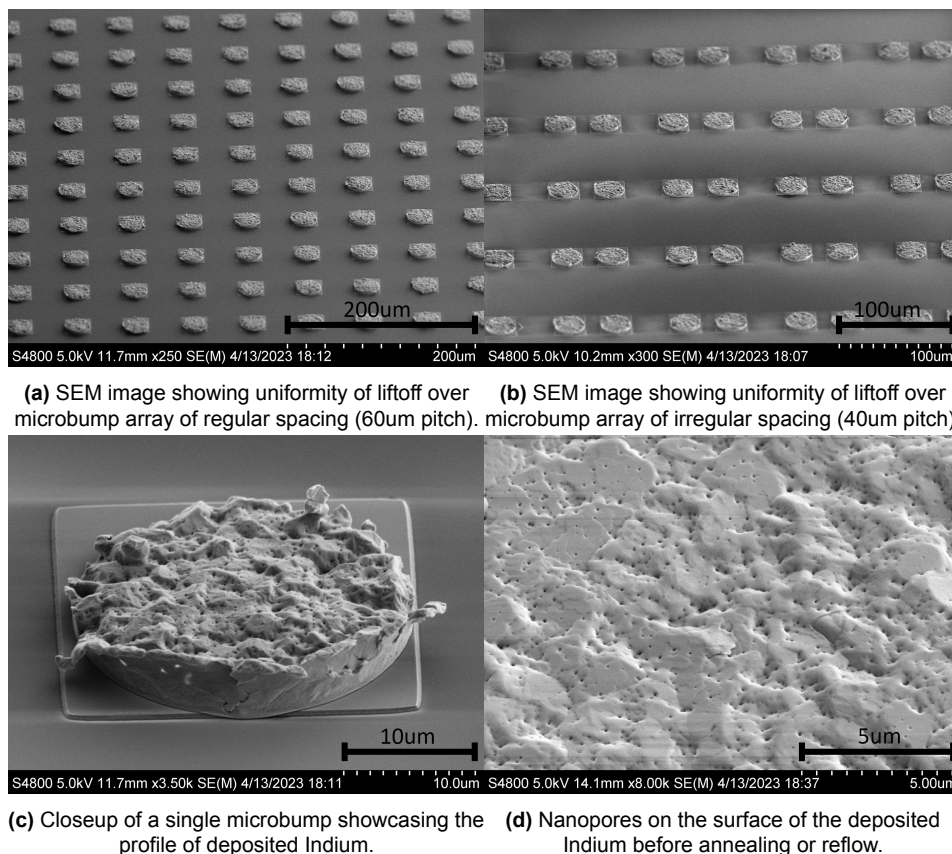


Figure 4.8: Successful lift-off results using AZ10XT Positive Photoresist. Height of the Indium disks is $> 1.5 \mu m$ due to high porosity and roughness of the deposited material.

with our deposition. Lift-off was performed immediately after evaporation in Acetone @ $50^{\circ}C$ under mild ultrasonic agitation. The sample was left undisturbed for 1 hr and then transferred to IPA cleaning solution for 5 min. The results of these successful deposition and lift-off steps can be seen in Figure 4.8.

4.4. Indium Bumping using Atmospheric Wet Reflow

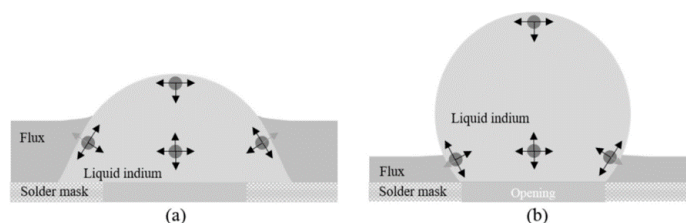


Figure 4.9: Theoretical reflow mechanism of Indium when using (a) solid and (b) soft liquid fluxes [61]

The quality of the evaporated and patterned Indium bumps as shown in Figure 4.8 is not satisfactory enough to proceed to flip-chip bonding. Therefore, further annealing and reflow steps were undertaken to reduce the native Indium Oxide layer and change the profile of the bump to be more suitable for bonding.

After the lift-off process, all samples were annealed @ $120^{\circ}C$ in Forming Gas

(10% H_2/N_2) for 10 min. Reflow experiments were then performed using a series of wet fluxes with varying levels of viscosity to study the effect of flux surface tension on the reflow results. The evaluated fluxes were all supplied by Indium Corp. and were designed for optimum reflow in an inert N_2 environment. However, for this project, reflow experiments were performed using a hotplate and in an atmospheric reflow oven to study the effects of an oxidising environment on the quality of reflow.

The evaluated fluxes were SC-5R, Indalloy-84004, and Indalloy-84002. All of these fluxes are water/acetone soluble and can be applied by spraying or spin-coating techniques. The technical details about these fluxes can be found here [62]. All three fluxes were spin-coated and reflowed according to Recipe A.10.

Reflow experiments were performed using a test sample containing microbump pitches of different lengths, ranging from $120\mu\text{m}$ to $40\mu\text{m}$, with a constant $20\mu\text{m}$ diameter Indium disk on a $30\mu\text{m} \times 30\mu\text{m} \times 200\text{nm}$ NbTiN UBM. The slow ramp-up time allowed for effective reduction of Indium Oxide and the 30sec hold step after reaching 175°C ensured uniform reflow across the sample. The results of SC-5R reflow experiment can be seen in Figure 4.10 and 4.11 and indicate a sufficiently reflowed microbump for flip-chip bonding. Microbumps across all the test pitches were uniformly reflowed across the substrate, with a hemispherical peak of $4\mu\text{m}$.

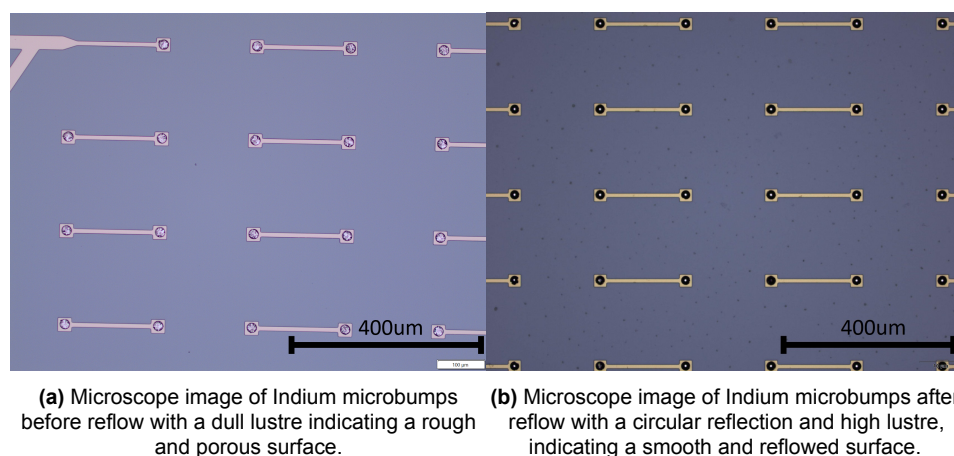


Figure 4.10: Results of successful SC-5R Flux Reflow after completion of Recipe A.10.

On the other hand, the less viscous Indalloy-84004, and Indalloy-84002 fluxes yielded negative results as seen in Figure 4.12. This unsatisfactory reflow is theorised to be due to the low quantity of Indium being reflowed. Usually, experiments of soft-flux reflow of Indium dictate longer Indium evaporation times, or usage of electroplating for deposition of 10's of microns of Indium [60, 61]. The limitations set forth by the evaporation equipment meant that Indium pillars of more than $4\mu\text{m}$ could not be reliably fabricated. This, coupled with the low viscosity of the respective fluxes meant that the liquid Indium coagulated in discrete groups throughout the sample, instead of adhering to the UBMs on which they were deposited.

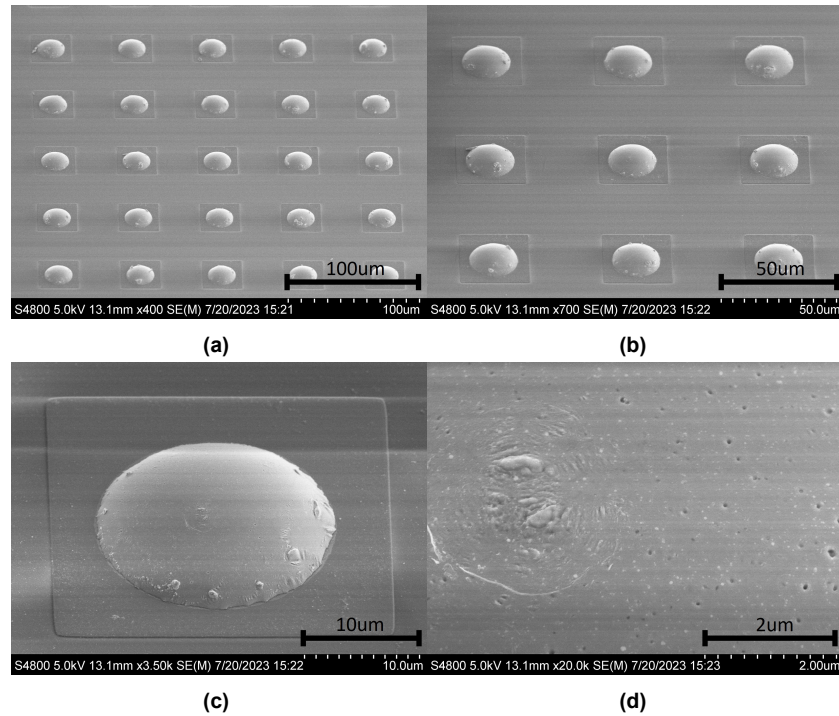


Figure 4.11: SEM Images of the successful SC-5R Flux Reflow showcasing the smooth and pore-free surface of Indium Microbumps, with a hemispherical peak of $4\mu m$, ideal for flip-chip bonding.

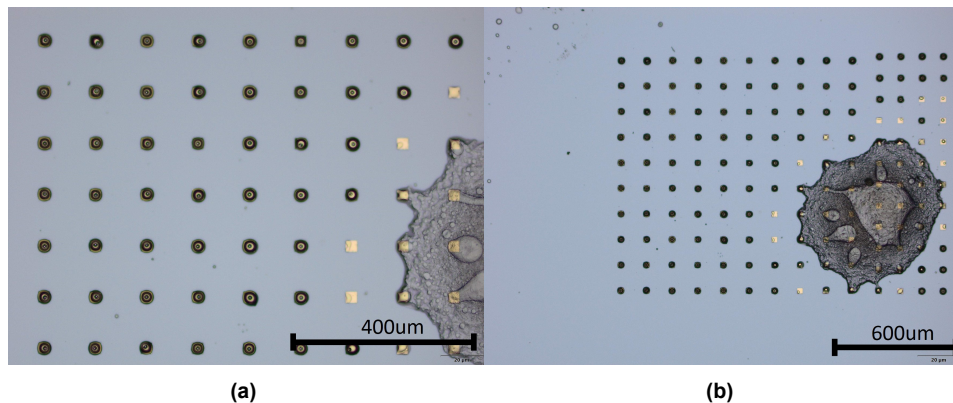


Figure 4.12: Microscope images of failed reflow experiments using the Indalloy-84004, and Indalloy-84002 low-viscosity fluxes.

4.5. Flip-Chip Bonding of Indium Microbumps

4.5.1. Experimental Setup

Following the satisfactory reflow results using the SC-5R Liquid Flux, the pattern shown in Figure 4.6 was fabricated on a single substrate, and Indium microbumping reflow was carried out using Recipe A.10. Then the sample was diced by covering the microbumps with a 10μm thick AZ10XT photoresist protective layer according to Recipe A.9.

The *Tresky T-3000-Pro Die Bonder* was used in the flip-chip experiment as it is a versatile tool capable of die-to-die or die-to-wafer bonding for a variety of applications

like die-attach, ultrasonic assembly, adhesive bonding, and flip-chip bonding. The bond force can range from 20g to 50kg using the external hydraulic press, and when calibrated properly, it features an XY placement accuracy of $\pm 1\mu\text{m}$. The alignment is done using a beam splitter as shown in Figure 4.13.

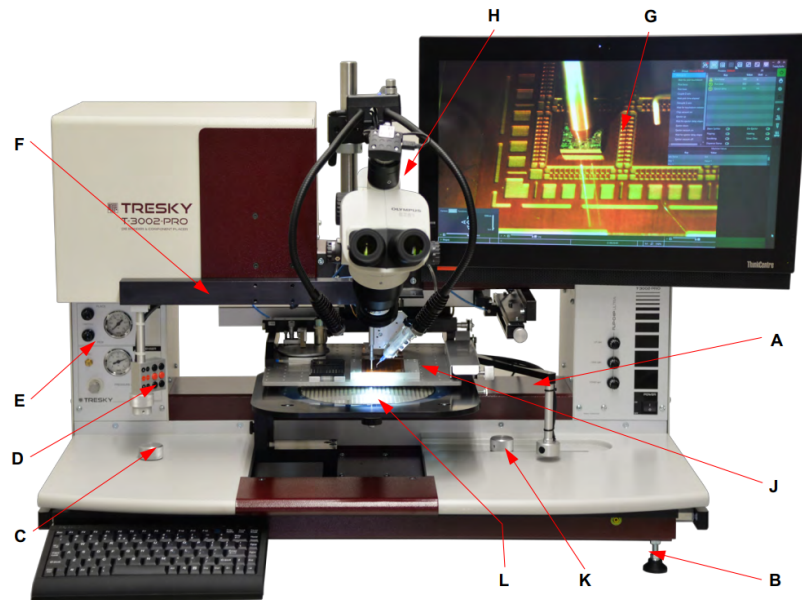


Figure 4.13: Labeled diagram of the T-3000-Pro Die Bonder. (a) Frame, (b) Leveling Screws, (c) BOTTOM Substrate adjustment knob (X-direction), (d) Control panel, (e) Pneumatic controller(chuck vacuum), (f) Pick and place arm, (g) Control PC, (h) Microscope for P&P arm alignment, (j) XY worktable, (k) BOTTOM Substrate adjustment knob (Y-direction), (l) BOTTOM Substrate.

4.5.2. Cold Compression Bonding

As discussed previously, keeping a low heat load on the sample during processing is paramount to gaining a high device yield. Since the microbumping and flip-chip bonding processes occur at the end of the BEOL process flow, reducing the bonding temperature plays a significant role in keeping this thermal budget low. Hence, cold compression bonding was chosen for experimentation as Indium is a highly malleable material and has been demonstrated to provide a good bonding strength using this method numerous times in peer-reviewed literature [63, 64, 20, 65]. Three different types of samples were prepared for this experiment:

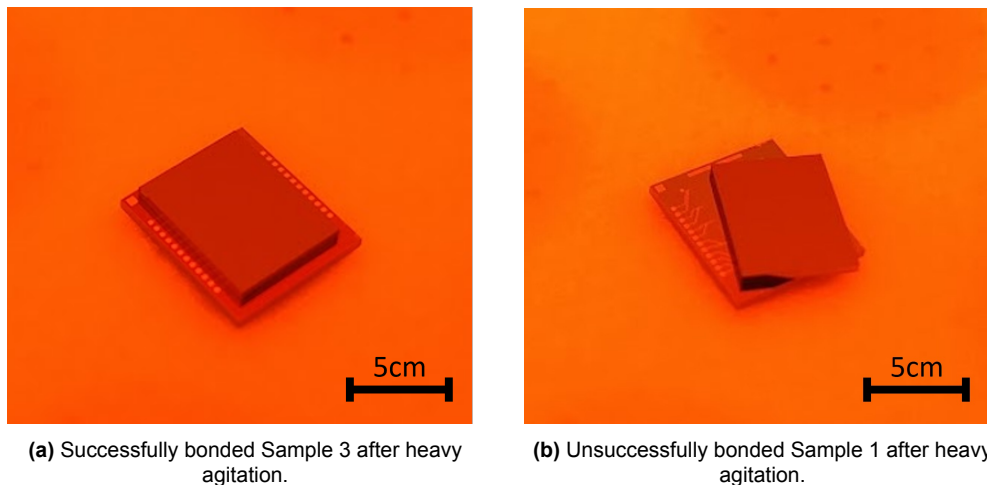
- *Sample 1.* Un-reflowed Indium microbumps, annealed in Forming Gas for 10 min, no pre-etching of Indium Oxide in 10% HCl.
- *Sample 2.* Reflowed Indium microbumps, annealed in Forming Gas for 10 min, no pre-etching of Indium Oxide in 10% HCl.
- *Sample 3.* Reflowed Indium microbumps, annealed in Forming Gas for 10 min, 2 min pre-etching of Indium Oxide in 10% HCl.

Table 4.1: Optimization of Flip-Chip Fabrication Flow.

Sample No.	Fabrication Flow	Status immediately after cold compression	Status after slight agitation	Status after heavy agitation
1	No uBump reflow, no pre-etching in HCl	Bonded	De-bonded	De-bonded
2	uBump reflow, no pre-etching in HCl	Bonded	Bonded	De-bonded
3	uBump reflow, pre-etching in HCl	Bonded	Bonded	Bonded

The bonding force was incrementally increased from 0.5g/bump (300g total weight per 600 bumps) to 3.5g/bump (2.1kg total weight per 600 bumps), at which point adhesion between the TOP and BOTTOM samples was apparent. The bonding results are summarized in Table 4.1, and show that the best bonding technique consists of reflowed Indium microbumps which are then annealed in Forming Gas (10% H_2/N_2) and pre-etched in 10%HCl solution for 2 min for reduction of the Indium Oxide layer. This pre-etching step must be performed immediately before flip-chip bonding since Indium Oxide will form an 80-100Å thin layer approximately 1 hr after this HCl etching step [66]. The successful and unsuccessfully bonded assemblies are shown in Figure 4.14.

A common issue faced with flip-chip bonding is angular misalignment along the XY-plane, which results in the overcompression of some microbumps and the under-compression of others. This effect can be clearly seen in Figure 4.15, and leads to a massive reduction in the yield of our devices. To eliminate substrate warpage as the cause of this effect, White-Light Interferometry analysis was performed on a 2cm x 2cm x 300 μm pure Silicon sample with and without any TSVs etched. The total warpage over all of the test samples was $\leq 1\mu m$, thereby eliminating it as the probable cause. The solution to this problem is thus theorised to be an active alignment of XY-plane during compression, a feature which is not available in the die bonder used in this experiment.

**Figure 4.14:** Examples of flip-chip cold compression bonding results.

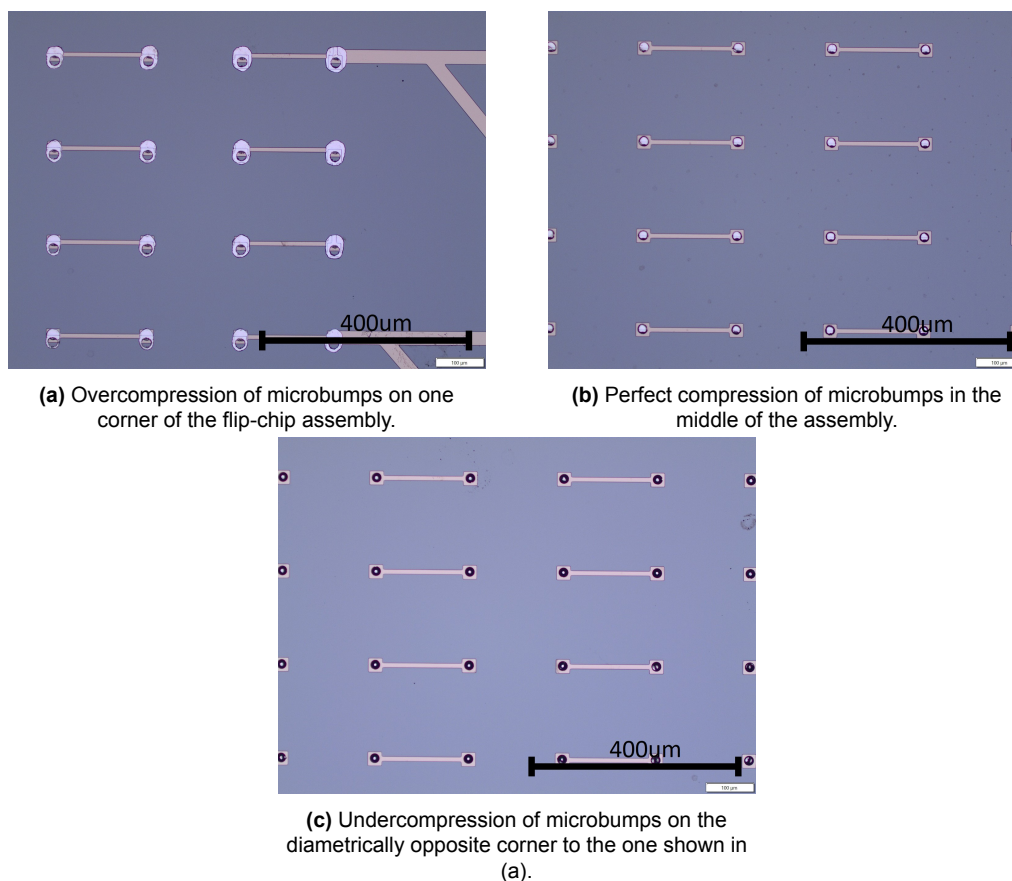


Figure 4.15: Microscope images of status of compression of microbumps in different parts of the flip-chip assembly. This is due to angular misalignment in the XY-plane of both substrates.

4.6. Conclusion

In this chapter, process flows were developed and optimised for the fabrication of Indium Microbumps and Flip-Chip Bonding utilising said microbumps. Recipes were optimised for evaporation, lift-off, patterning, and reflow of Indium Microbumps, down to $40\mu m$ pitch and $20\mu m$ bump diameter. Moreover, sample preparation recipes for flip-chip bonding were optimised and 3D integration was demonstrated for samples with 600 microbumps connected in a daisy chain with $200\mu m$ pitch and $20\mu m$ bump diameter.

In the next chapter, we will characterise the fabricated samples to evaluate the electrical performance of the Indium interconnects at cryogenic temperatures.

5

Electrical Characterisation

5.1. Introduction

In Chapters 3 and 4, test samples were fabricated for electrical characterisation of through silicon vias and Indium microbump flip-chip assemblies. TSVs were coated with superconducting materials (TiN and NbTiN) and were successfully patterned to form Van der Pauw structures for resistance measurements. Daisy-chain structures were fabricated using Indium microbumps by successful room-temperature bonding of two substrates.

In this chapter, we will attempt to characterise these test samples, with the objective to measure the superconducting critical temperature (T_c) of the fabricated test structures. The resistances will be measured using the four-point probe method by utilising 3D Cross-Bridge Kelvin Resistor structures. The resistances will be measured at room temperature, and if within specification, cryogenic measurements will be performed by cooling down the samples to 4.5K.

5.2. Measurement Setup

Lakeshore CPX Cryogenic Probe Station was used for the electrical characterisation of the test samples. It features four retractable probes for DC measurements and two more retractable probes for RF characterisation. Figure 5.1 showcases the probe station assembly, which consists of a central "4K-stage" which can hold up to a 4-inch wafer for cryogenic testing. It should be noted that this probe station has a lower cooling limit of 4.5K, which is not sufficient for T_c measurements of Indium microbumps. However, electrical connectivity can still be measured by monitoring the superconducting transition of the NbTiN/TiN wiring layer, which should occur at or near 15.2K/4.8K.

This probe station was chosen for its flexibility and ability to accommodate a wide variety of sample sizes on the same chuck. It enabled quick turnaround during the measurements phase of the project due to the fast 300K to 4.5K cool-down time of approximately 1 hr 30 min. The double-side patterned samples need to be covered by a Kapton tape on the backside before placement on the Copper cooling chuck since they have conductive wiring layers on the backside. The samples can then be mounted on the chuck with "GE-varnish" which is thermally conductive and adhesive at cryogenic temperatures.

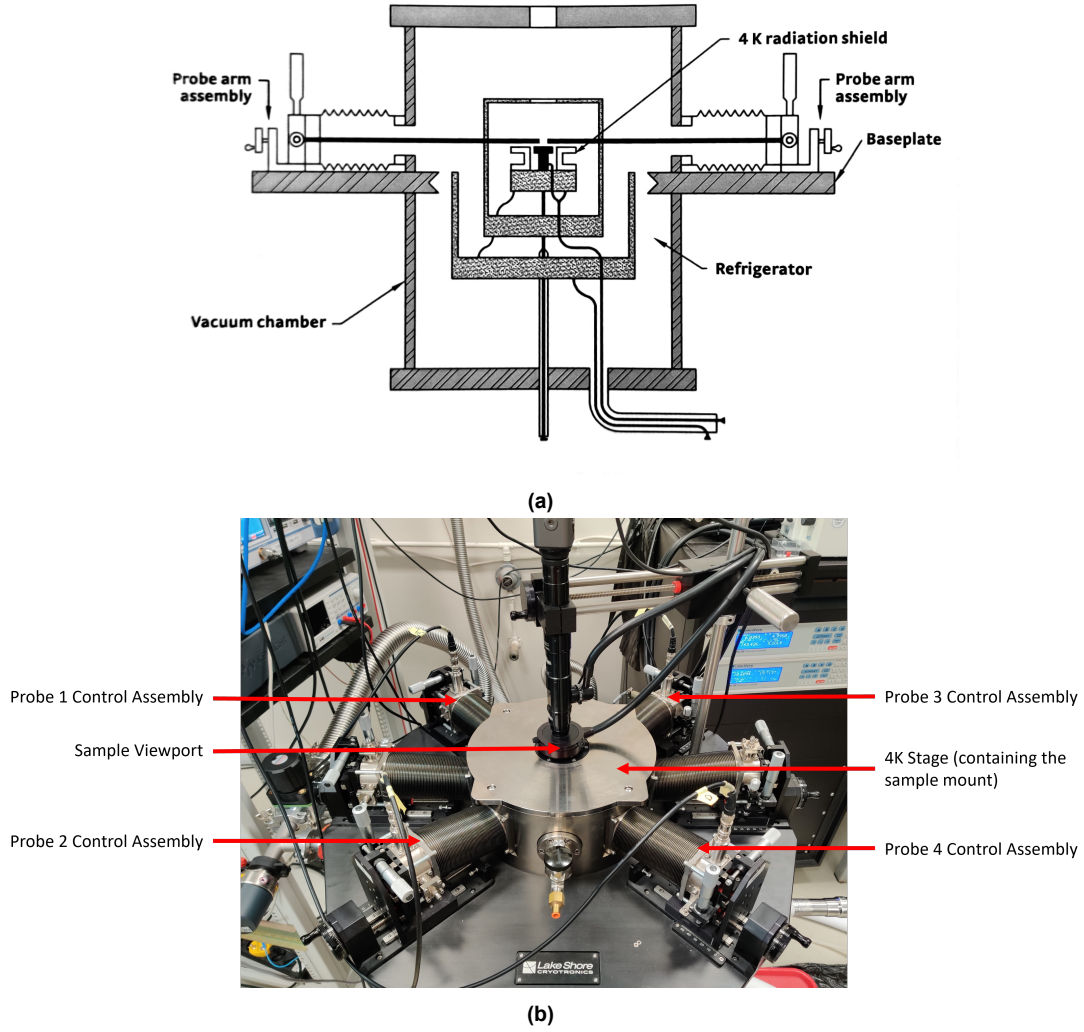


Figure 5.1: Lakeshore CPX Cryogenic Probe Station used for electrical testing of the test samples.

5.3. Measurement Results

TSV resistance was measured using a 4-probe method with a Cross-Kelvin Bridge Resistor as shown in Figure 5.2. V-I characteristics were measured and the resistance was calculated using Equation 5.1 which has been adapted from a study by Stavitski et al. [67]. Resistance of the Indium Microbump flip-chip daisy chain was measured in a similar manner by probing diametrically opposite landing pads on the test sample as shown in Figure 4.6.

$$R = \frac{\pi}{\ln(2)} \frac{\Delta V}{I} \quad (5.1)$$

Due to restrictions in the usage time of the cryostat, only the $30\mu m$ and $40\mu m$ TSVs, and the Indium microbump daisy chain test structures were tested during the electrical resistance measurements. During room-temperature measurements, high resistance in the order of multiple hundreds of $M\Omega$ was measured using the 4-point probe method on the $30\mu m$ TSV Van der Pauw structures. This validated the theory proposed in Chapter 3 that the ALD TiN coating thickness in the middle of the TSV is

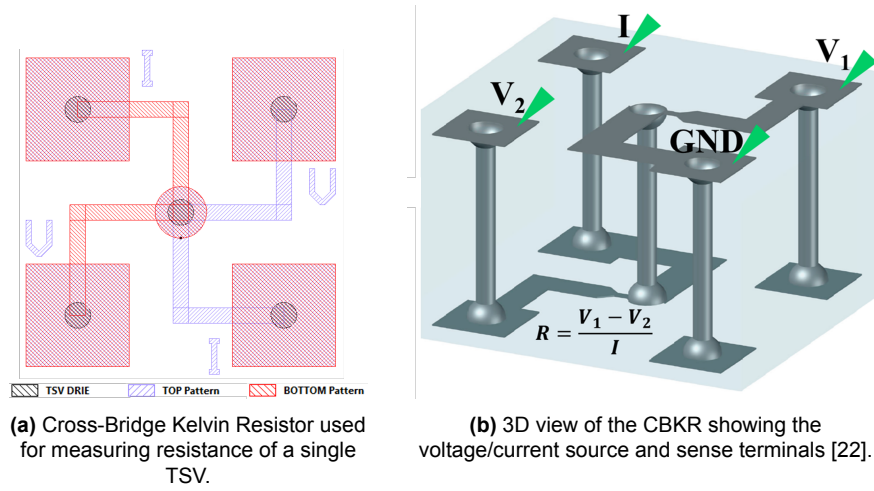


Figure 5.2: CBKR structure used during electrical characterisation, adapted from [67].

not sufficient or uniform enough to facilitate an electrical connection.

The room-temperature resistance measurement results of $40\mu m$ diameter and $300\mu m$ deep ALD TiN coated TSV structures are reported in Figure 5.3. Due to patterning difficulties described in Chapter 3, more measurement readings could not be taken with confidence that they represent an optimally formed TSV. Nevertheless, the reported results indicate that ALD TiN can indeed be used for reliable and repeatable coating of the sidewalls of through silicon vias $\geq 40\mu m$ diameter and $300\mu m$ depth.

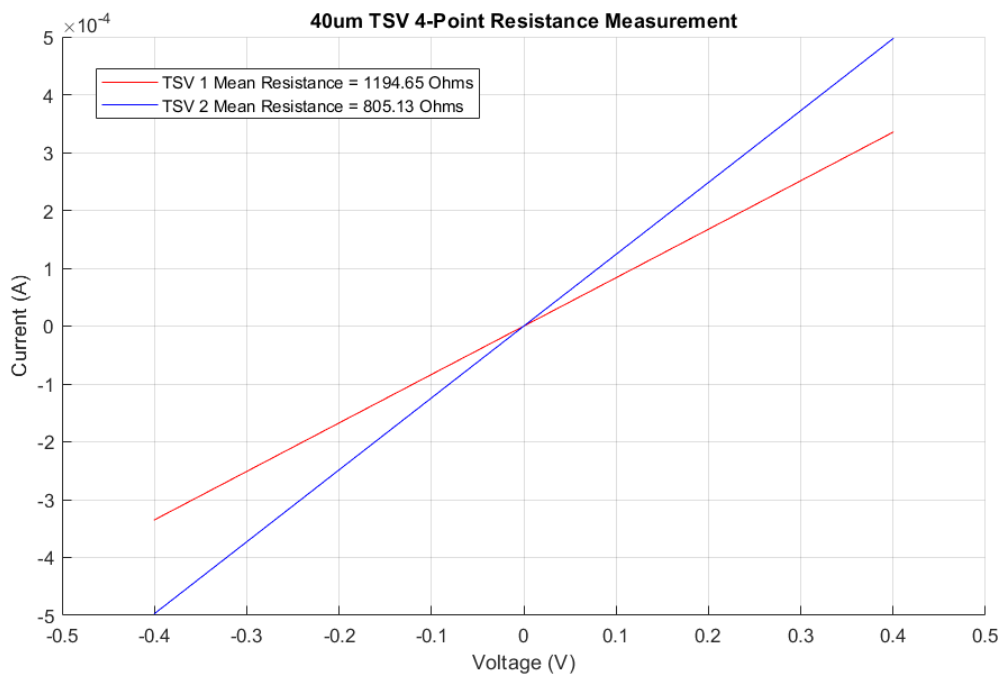


Figure 5.3: Results of room-temperature 4-point resistance measurements for two identically fabricated $40\mu m$ diameter TSVs.

Cryogenic measurements of the $40\mu m$ diameter TSVs and Indium daisy chains

could not be performed due to an equipment malfunction which resulted in readings in the order of multiple hundreds of $M\Omega$. It was discovered that the probe needle broke during the probing of the extremely hard NbTiN landing pads of the test samples. For future measurements, it is advised to coat these landing pads with a thin layer of gold to facilitate better electrical connectivity, reduce oxidation of TiN/NbTiN, and reduce stresses on the probe tips.

It should be noted, however, that the Indium microbump flip-chip assembly was intact after two 300K to 4.5K cooling and heating cycles, validating its choice as the material of choice for 3D flip-chip bonding.

5.4. Discussions

From the results of the electrical resistance measurements, it is proven that $30\mu\text{m}$ TSVs are not feasible for application in our 3D integration scheme due to poor sidewall coating of ALD TiN. However, further tests need to be performed to find the lower bound of this effect.

Room-temperature measurements of $40\mu\text{m}$ TSVs yielded positive results with multiple vias showcasing conductivity with similarly measured resistance values. Further cryogenic testing of these samples is recommended to form a more complete understanding of the structures in the operational temperature range.

The cryostat setup is being worked upon and more measurement sessions are planned to further characterise the Superconducting Through Silicon Vias and the Indium Microbumps. Unfortunately, it was not possible to characterise all the test devices within the bounds of this project.

6

Conclusion

6.1. Project Summary

The aim of this project was to create architectures for 3D Integrated Assemblies that could be implemented in the design of the Scalable Quantum Computer using Diamond-based Spin-Qubits. Additionally, the project aimed to formulate reproducible and scalable fabrication methodologies for these assemblies. As part of this, a 3D Interposer structure was proposed to facilitate the integration of CryoCMOS and Photonic Circuits in a single package. The application of such an interposer can reduce the interconnect wiring lengths between the control and readout electronics and the optical circuitry that controls the spin-qubits and theoretically lead to an increase in qubit coherence times, reduction in decoherence noise, and the ability to integrate 1000s of qubits in a single package. Meeting these requirements is imperative to satisfy *DiVincenzo's Criteria*, which provide a roadmap for achieving the realization of a Quantum Computer [68].

A major challenge faced during the design of this 3D assembly was the fact that our operational temperature range was cryogenic, i.e. 1K - 4K, and the fact that the interconnects needed to be superconducting in this temperature range to facilitate a near-lossless transmission of electrical signals. The heat flux between the CryoCMOS chip and the Photonic chip was also a critical design factor, with the upper limit of 5mW dictating the material choices for our direct bonding and flip-chip design schemes.

To review, satisfy and refine these requirements, this project was split into five phases. First, thermal simulations were performed in Ansys Icepack to derive the best option for the 3D assembly out of the numerous design recommendations. Second, Through Silicon Vias were etched, coated, and patterned based on the above simulation results, and multiple via aspect ratios were studied for their potential application in our interposer. Third, Indium Microbumps were designed and fabricated to test their properties of liquid-flux reflow and room-temperature compressing bonding. Fourth, flip-chip bonding recipes were optimised using said microbumps to integrate two distinct substrates into a single package. Finally, electrical resistance measurement experiments were set up to characterize the performance metrics of the above-fabricated devices at ambient and cryogenic temperatures.

Thermal simulations were performed using finite element modelling in Ansys Icepack to refine the device fabrication specifications. It was shown that the Indium Microbump bonding and NbTiN direct bonding schemes will not be sufficient to reduce heat flux

between the CryoCMOS and Photonic Chips below the requirements' set threshold of 5mW, without severely reducing the total number of interconnects between these chips and the interposer. As such, it was advised to adopt a Hybrid Bonding Scheme utilising $\geq 20\mu\text{m}$ tall NbTi/NbTiN pillars with an Indium microbump interface for adhesion of the two pillars. It was also shown that the presence or absence of NbTiN-coated TSVs does not affect the total heat flux through the interposer by a large margin due to the low thermal conductivity of NbTiN compared to the Silicon-substrate at cryogenic temperatures.

It is showcased that TSVs of opening diameter $\sim 30\mu\text{m}$ cannot be reliably coated with a superconducting liner even with the use of processes like ALD. Moreover, patterning of ultra-fine pitch $\leq 40\mu\text{m}$ TSVs using liquid photoresist yielded negative results, and it is recommended that experiments be performed using dry-film photoresist to accurately pattern such structures. Consequently, it is recommended to change the project baseline specifications of the minimum TSV diameter and pitch based on the above findings. TSVs of diameter $\geq 40\mu\text{m}$ were reproducibly coated with a dielectric (SiO_2 and Al_2O_3) and a superconductor liner (TiN and NbTiN). Preliminary room-temperature electrical measurements on $40\mu\text{m}$ TSVs demonstrated the viability of such structures. Due to logistical issues, more intensive electrical tests were not performed on these test devices, however, new testing methodologies and devices were made for future experiments.

Indium Microbumps of $20\mu\text{m}$ diameter and $1.5\mu\text{m}$ pre-reflow height were fabricated and reflowed into a hemispherical shape of $4\mu\text{m}$ height to facilitate an optimum flip-chip bonding profile. It was showcased that liquid-flux atmospheric reflow can indeed be performed on a simple hotplate without the need for expensive reflow equipment with reducing gases like Formic Acid or Forming Gas. These hemispherical microbumps were also successfully bonded in a flip-chip assembly after surface functionalization by annealing in Forming Gas and pre-etching in 10% HCl.

Overall, various proof-of-concept designs were realised, fabricated, and tested to gain insight into the challenges we will face when integrating our 3D assembly of CryoCMOS and Photonic Integrated Circuits. The results of this thesis can be built upon and the fabrication processes can be optimised even further to ensure reliable and scalable production of *Diamond-based Spin-Qubit Quantum Computers*.

6.2. Recommendations for Future Research

The following recommendations are made for continued research into the design of a *Cryogenic Interposer System for 3D Integration of Quantum Computers*:

- Electroplating of NbTi can be considered as an option for the fabrication of tall pillars as recommended previously in this thesis. The porosity and roughness of the deposited material will need to be optimised to facilitate proper reflow of the Indium microbumps deposited on top of said pillars.
- Plasma-Enhanced Direct Bonding of superconducting NbTiN/NbTi thin films and tall pillars can be experimented upon, but will require alteration of the fabrication flows to accommodate the chemical metal polishing steps that may be required to prepare the bonding surface.

- Dry-film photoresist patterning is recommended for etching the redistribution layer on the frontside and backside of the interposer. This can greatly increase the yield of the TSVs by reducing over-etching along the via opening and on the sidewalls.
- Polymer filling of TSVs can be experimented upon, in an effort to increase the reliability of the sidewall liners. This can help reduce patterning errors when using a liquid photoresist by closing the via opening and preventing exposure of TSV sidewalls during further processing steps. Depending on the stability of this filling, a carrier wafer may also become unnecessary when trying to mount the post-TSV-etched samples on a vacuum chuck.
- Use of an Aluminium etch-stop layer is recommended for reducing notching effects during DRIE of TSVs. Alternatively, a polished silicon carrier wafer can also be experimented with as it promises a cleaner fabrication flow with a faster turnover rate.
- Electroplating of Indium is recommended for the formation of taller Indium pillars if the project necessitates a complete spherical reflow of the Indium microbumps.
- Surface functionalization experiments of the Indium Microbumps' under-bump material (UBM) are recommended to increase the yield of the bumps and reduce the boundary resistance between these interconnects.
- Post-bonding Indium reflow can be experimented upon, provided the thermal budget allows for it, for self-alignment of the 3D assembly by utilising surface tension of the molten Indium bumps.

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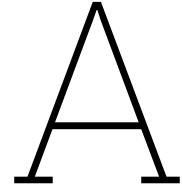
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Appendix: Device Fabrication Recipes

Recipe A.1: S1813 Positive Photoresist Coating, Baking, and Patterning

1. HMDS vapour treatment @ 150°C with 10 min dehydration step.
2. Spin coating S1813 @ 2000 rpm (verified 2.1µm thickness).
3. Bake @ 115°C for 1 min.
4. Pattern using uMLA Laserwriter (Dose = 250 mJ/cm², Defoc = 6)
5. Development in MF321 for 1 min, rinse in H₂O for 30 sec.
6. RIE Descumm step with Oxygen-plasma...
 - (a) O₂ = 20 sccm
 - (b) RF Power = 50 W
 - (c) Chamber Pressure = 10ubar
 - (d) Etching time = 1 min

Recipe A.2: Silicon Oxide 4µm Hard Mask Etching using AMS Bosch (Ramp Etch Mode)

1. Chamber Pressure = 1e-5 mbar
2. Sample Holder Temperature = 0°C
3. Loop 20 times (Total 20 min etch time)...
 - (a) Sample Holder Position from Plasma Source = 120mm
 - (b) CH₄ = 10 sccm, C₄F₈ = 50 sccm, He = 100 sccm
 - (c) Ar = 0 sccm
 - (d) RF Power = 2500 W
 - (e) Etching time = 1 min
 - (f) RF Power = 0 W
 - (g) CH₄ = 0 sccm, C₄F₈ = 0 sccm, He = 0 sccm
 - (h) Sample Holder Position from Plasma Source = 200mm
 - (i) Ar = 100 sccm
 - (j) Waiting time = 2 min

Recipe A.3: Silicon DRIE Iteration 1

1. Chamber Pressure = $1\text{e-}5$ mbar (Valve Position 25%)
2. Sample Holder Temperature = 10°C
3. Sample Holder Position from Plasma Source = 200mm
4. Cyclic Pulsing (15 min)...
 - (a) RF Power = 1800W
 - (b) SF_6 = 300sccm = 7 sec pulse
 - (c) C_4F_8 = 150sccm = 2 sec pulse

Recipe A.4: Silicon DRIE Iteration 2

1. Chamber Pressure = $1\text{e-}5$ mbar (Valve Position 25%)
2. Sample Holder Temperature = 0°C
3. Sample Holder Position from Plasma Source = 200mm
4. Cyclic Pulsing (15 min)...
 - (a) RF Power = 2200W
 - (b) Bias Power = 60W
 - (c) SF_6 = 300 sccm = 7.4 sec pulse
 - (d) C_4F_8 = 245 sccm = 2.3 sec pulse

Recipe A.5: Silicon DRIE Iteration 3

1. Chamber Pressure = $1\text{e-}5$ mbar (Valve Position 25%)
2. Sample Holder Temperature = 0°C
3. Sample Holder Position from Plasma Source = 200mm
4. Cyclic Pulsing Step 1 (m-loops)...
 - (a) RF Power = 2200W, Bias Power = 60W
 - (b) SF_6 = 300 sccm = 7.4 sec pulse
 - (c) C_4F_8 = 245 sccm = 2.3 sec pulse
 - (d) Etching time = 3 min
 - (e) RF Power = 0W
 - (f) SF_6 = 0 sccm, C_4F_8 = 0 sccm
 - (g) Cooling time = 30 sec
5. Cyclic Pulsing Step 2 (n-loops)...
 - (a) RF Power = 2000W, Bias Power = 80W
 - (b) SF_6 = 300 sccm = 8.4 sec pulse
 - (c) C_4F_8 = 245 sccm = 2.5 sec pulse
 - (d) Etching time = 3 min
 - (e) RF Power = 0W
 - (f) SF_6 = 0 sccm, C_4F_8 = 0 sccm
 - (g) Cooling time = 30 sec

Recipe A.6: Attaching Small Samples on a Carrier Wafer for Photoresist Spinning

1. Clean the carrier wafer with Acetone and IPA @ 50°C for 10min.
2. Spin coating S1813 @ 2000 rpm (verified 2.1um thickness).
3. Place the test sample on the carrier wafer, taking care not to touch the photoresist below.
4. Bake @ 100°C for 15 min on the hotplate.

Recipe A.7: MAN1410 Negative Photoresist Coating, Baking, and Patterning

1. HMDS vapour treatment @ 150°C with 10 min dehydration step.
2. Spin coating MAN1410 @ 3000 rpm (verified 1.1um thickness).
3. Bake @ 100°C for 90 sec.
4. Pattern using uMLA Laserwriter (Dose = 180 mJ/cm², Defoc = 6)
5. Development in MAD533 for 100 sec, rinse in H₂O for 30 sec.

Recipe A.8: AZ10XT Positive Photoresist Coating, Baking, and Patterning for TSV Electrical Structures

1. HMDS vapour treatment @ 150°C with 10 min dehydration step.
2. Spin coating AZ10XT @ 2000 rpm (verified 10um thickness).
3. Bake @ 110°C for 3 min 30 sec.
4. Rest the sample for 30 min for rehydration of photoresist film.
5. Pattern using uMLA Laserwriter (Dose = 650 mJ/cm², Defoc = 2)
6. Development in 1:4 solution of AZ400K:H₂O for 5 min with agitation every 1 min, rinse in H₂O for 30 sec.

Recipe A.9: AZ10XT Positive Photoresist Coating, Baking, and Patterning for Indium Lift-Off

1. HMDS vapour treatment @ 150°C with 10 min dehydration step.
2. Spin coating AZ10XT @ 4000 rpm (verified 6.8um thickness).
3. Bake @ 110°C for 3 min.
4. Rest the sample for 30 min for rehydration of the photoresist film.
5. Pattern using uMLA Laserwriter (Dose = 800 mJ/cm², Defoc = 4)
6. Development in 1:4 solution of AZ400K:H₂O for 4 min with agitation every 1 min, rinse in H₂O for 30 sec.

Recipe A.10: Indium Atmospheric Wet-Reflow for SC-5R Microbump Flux

1. Turn ON the hotplate and ensure the carrier wafer is clean.
2. Set the initial hotplate temperature to 95°C.
3. Spin coat sample with SC-5R Microbump Flux @ 300 rpm for 30 sec.
4. Place the sample on the hotplate and change the setpoint temperature to 175°C. Vary the power of the hotplate to ensure the heating time from 95°C to 175°C is exactly 5 min.
5. Once the hotplate reaches 175°C, leave the sample on the hotplate for an additional 30 sec before removal.