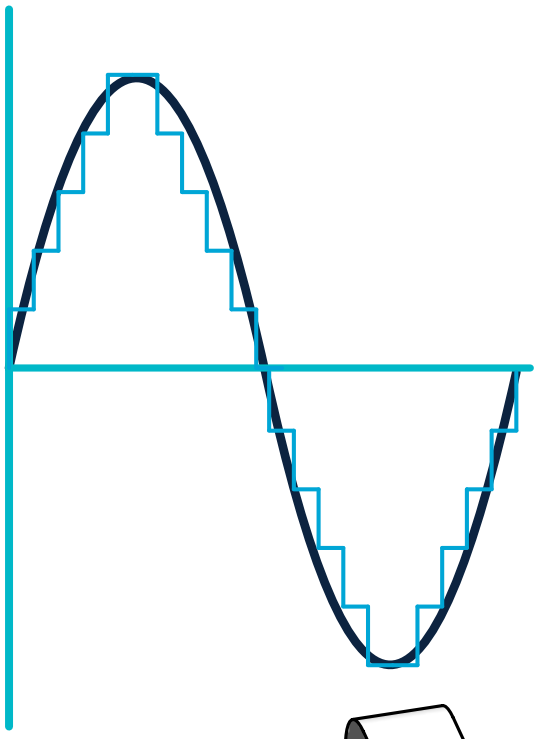
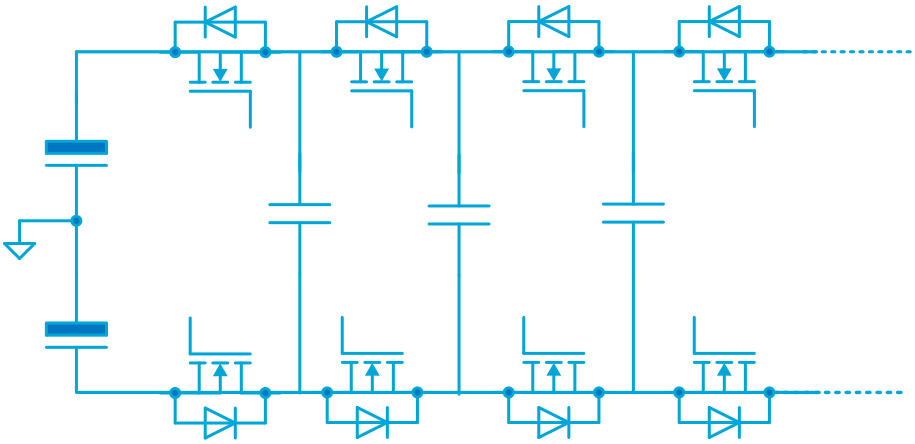
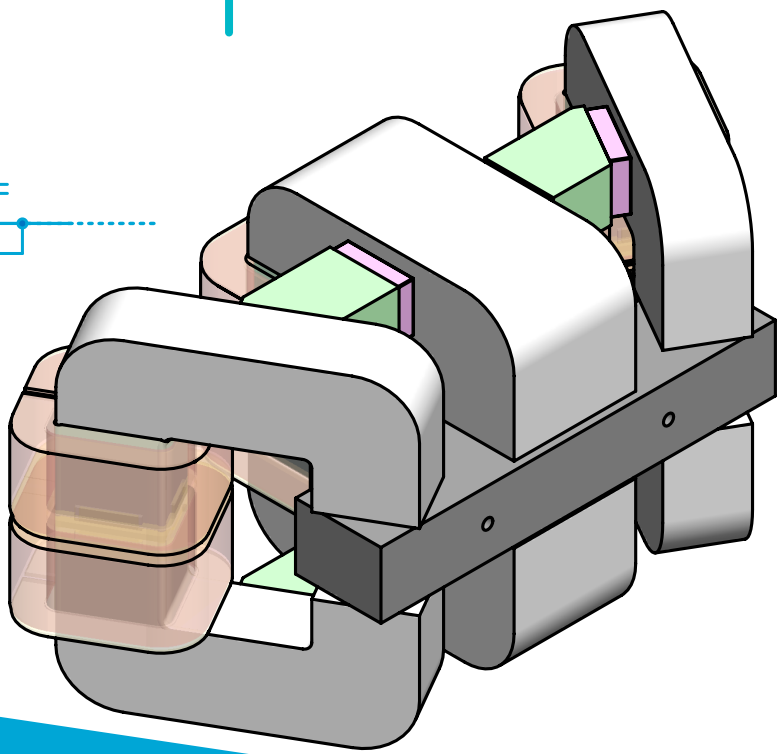
# Flying Capacitor Multilevel Inverter for High-bandwidth Switched-Mode Power Amplifier







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# Flying Capacitor Multilevel Inverter for High-bandwidth Switched-Mode Power Amplifier

By

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to obtain the degree of Master of Science at Delft University of Technology, to be defended publicly on Tuesday, August 26, 2025 at 14:00.


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*Giel Berden*
*Delft, August 2025*

# Abstract

This thesis presents a high-bandwidth multilevel power amplifier based on a flying capacitor topology. This amplifier is designed, in part, to drive a novel tunable magnetic actuator and other electromechanical actuators. These tunable actuators are based on a low-coercive-force AlNiCo magnet, which can be remagnetized in situ to generate a static force output. This is done to minimise heat dissipation. These actuators and others of their type require either high output power, high bandwidth or superior output quality, as is made clear in the literature. To meet these combined requirements, a multilevel power amplifier is proposed. Multilevel converters possess inherent properties, such as high effective output frequencies, lower transistor stresses, and high power density, which overlap with the needs of the power amplifier. The flying capacitor converter is identified as a suitable candidate for use as an amplifier. This converter operates on the principle of series-connected switches, with floating capacitors between the series nodes to generate multiple voltage levels. A simulation is made to further investigate the operating principle of this topology and its suitability for power amplifiers. As there is always a gap between simulation and reality, a hardware prototype is designed and built. The prototype is tested on multiple types of loads, including a hardware prototype of the tunable magnet actuator. The power amplifier prototype functions as expected and is subjected to further tests. During these tests, performance in line with the literature is measured. The overall system efficiency at the nominal operating point is established at 97%, with a worst-case efficiency of 96.2% and a best-case of 98.5%.

Furthermore, a THD of -38 dB, or 0.016%, at the nominal operating point is measured, rivalling theoretical and practical results from the literature. Finally, open-loop bandwidths of 10 kHz are measured, and closed-loop bandwidths of 4 kHz are achieved. While these results are positive, certain limitations of the system are also identified, mainly related to noise and control. Design flaws in the sensing and software are considered the primary culprits. These are not inherent to the core topology used, but are related to the practical challenges when implementing such a high-bandwidth and high-power amplifier.

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# 1 Introduction

## Background

Modern high-precision production processes, such as microchip lithography, require incredible precision and accuracy on the nanometer scale. At this scale, many factors can cause disturbances and interference with these processes. One of these disturbances is thermal expansion due to electrical losses in the electromechanical actuators [1]. The Beat The Heat project seeks to remedy this issue by attempting to minimise Joule heating in the actuators by using tunable low coercive force permanent magnets[2], [3]. These actuators are a form of hybrid reluctance actuators. Instead of the classic NdFeB high coercive force magnets, the innovation in this project lies in the use of AlNiCo magnets, which have a low coercive force and can be re-magnetised in situ to a setpoint remnant state by a magnetising coil. At this remnant state, a static force is generated without any Joule heating, outside of the short magnetisation pulses. This static force is used to position a mover to the required setpoint. The position loop is then further stabilised by two classical reluctance actuators. The main challenge is controlling the tunable magnetic actuator, as the hysteresis behaviour of AlNiCo magnets is highly nonlinear and complex to model [4].

## Problem definition

Novel electromechanical actuators, like the ones from the Beat The Heat project, require an amplifier to drive them. In the literature about these actuators, not much thought is generally given to these amplifiers and their minimum requirements. Linear amplifiers are often used due to their high output quality and ease of use. However, the peak output efficiency of a class B amplifier is governed by: [5]

$$\eta_{B,max} = \pi/4 = 78.5\%. \tag{1.1}$$

This is only achievable at its maximum output voltage and decreases as the output voltage drops. This means, at higher output power, the cooling system needs to be able to dissipate a significant amount of heat. This impacts the size of the heatsink, leading to a large amplifier package [6]. Considering the goal of the Beat The Heat project, having the amplifier generate all the heat instead of the actuator makes little sense, especially if a linear amplifier is not necessarily required. This project, therefore, aims to analyse the requirements of the actuators and translate them into requirements for a switched-mode power amplifier.

### Translating actuator requirements to amplifier requirements

Electromechanical actuators used in precision industries, such as semiconductor fabrication, require high precision, low noise, repeatability and increased force output to meet ever-increasing requirements. Different types of novel actuators are highlighted, and their requirements are discussed. These, in combination with the Beat The Heat project, will be used as the basis for the requirements of the power amplifier.

- Low friction and levitating actuators: The actuator forces required for high acceleration can be problematic for magnetic bearings, levitating planar actuators, gravity compensators and other similar systems that are characterised by low friction and low damping[7]. Due to these characteristics, the forces are easily converted into unwanted movements and vibration, which are not well compensated by the mechanical

transfer function from force to acceleration. The critical frequencies for this range from DC to roughly 10 kHz, as there is little to no mechanical damping in this range [8]. This means that the actuators must compensate for any vibrations and disturbances within this bandwidth, and thus, the power amplifier must also compensate.

- Fast Tool Servos: Outside of noise rejection, some other actuators used within the semiconductor industry or related industries, such as optics manufacturing, require large mechanical bandwidths. A prominent example of these actuators are Fast Tool Servos (FTS) [9]. These actuators are used to produce nanometer precision surfaces, for example, used in microlens arrays or diamond turning machines. These actuators can have mechanical operating frequencies of up to 10kHz. They need accurate positioning in the nanometer range at these frequencies and can experience accelerations of over 1300G [10]. Accelerations at this scale require small moving masses and very high output forces. This then translates into high peak currents. These systems are often driven by high-bandwidth linear power amplifiers with output powers into the kilo-Watt range [11]. As indicated before, the losses are also in the range of hundreds of watts due to the limited efficiency. This requires significant cooling.

The requirements for these actuators can be combined with the trends from industry, which has seen an increasing demand for output power (to increase force and acceleration), low noise, and high bandwidth [7], [12], [13].
Another concern is the noise being injected into the motion system by the amplifier. For linear amplifiers, this is very low, but switch-mode amplifiers generate more noise through their discrete switching nature [14]. The industry demands a very high Signal-to-Noise Ratio (SNR) and very low total harmonic distortion (THD). According to [12], the required SNR needs to increase by $\approx$ 20dB every five years to keep up with demand, and according to [8], this figure is now at 110dB of SNR and -50dB of THD. Furthermore, EMI is also a concern in these systems, as some of the sensors used for control are very sensitive to coupling EMI. Although EMI can also be mitigated by adding shielding. While SNR and EMI are difficult to measure without building a separate testing setup specific to the project, which is therefore outside of the scope, the THD is not difficult to measure using available equipment. Thus, the THD can be set as a requirement, and the SNR and EMI can be used as motivating reasons.

Given the above considerations, a trade-off must be found between low noise, high output power, and high bandwidth. It has become clear from the published literature on this topic that the requirements of the actuators and processes will continue to become more stringent [8]. The impact these changing requirements have on other systems in the process is visualised in Fig. 1.1.

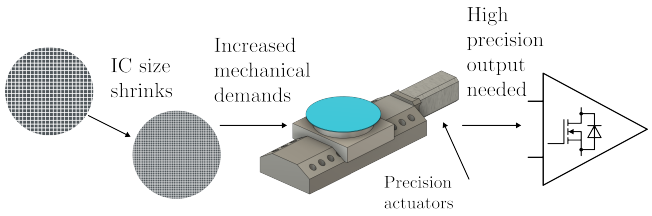



Figure 1.1: Changing requirements have a knock-on effect on all components in the systems.

## Effects of electrical noise and distortion on precision systems

As discussed in the previous section, the requirements on noise and distortion are of vital importance in high-precision systems. An important and easily measurable performance indicator is the THD. The THD can be defined as:

$$\text{THD} = 10\log_{10}\frac{\sqrt{i_2^2+i_3^2+i_4^2+...+i_k^2}}{i_1}. \tag{1.2}$$

Here, $i_k$ is the k-th harmonic of the signal of interest, in this case, the current. Therefore, the THD represents the ratio between the magnitude of the fundamental versus its harmonics. The importance of the THD can be shown with a simple example using the relation between force and current of an actuator. This equation is derived from a simplified model of the C-core reluctance actuator seen in Fig. 2.1:

$$F(t) \approx (\frac{NI(t)}{l_g})^2\frac{\mu_0 A_g}{4}, \tag{1.3}$$

where $N$ is the number of turns, $I$ is the actuator current, $l_g$ and $A_g$ are the airgap length and area, respectively, and $\mu_0$ is the permeability in free space. If the current into this actuator has a very low THD, the current can be adequately described by its fundamental:

$$I(t) = I_{peak} \sin(\omega t). \tag{1.4}$$

Therefore, the output force will also only contain this fundamental frequency. If any harmonic distortion is introduced to the input current, the output force of the actuator will suffer in output quality as well, due to the linkage between force and current. These harmonics are multiples of the fundamental frequency. Then, the current could be described as:

$$I(t) = I_{peak} \sin(\omega t) + \frac{I_{peak}}{n} \sin(3\omega t) + \frac{I_{peak}}{n} \sin(5\omega t) + ... \tag{1.5}$$

Any of these harmonics could then also be present in the actuator if the actuator has a high enough bandwidth, as is the case with the fast tool servos described previously. These harmonics are then coupled into the mechanical system and could excite resonances in the system, causing unacceptable errors in the output.

While the importance of a low THD has been discussed, the sources of harmonic distortion in switched-mode power amplifiers have not been made clear. There are a large number of variables that contribute to the THD [8]. Some of the factors important to this project are highlighted in Fig. 1.2. The power switches themselves can generate distortion and harmonics in multiple ways, mostly generated by the practical non-linear switching transitions and the non-linear transfer from voltage to current, especially when inductive loads are considered [15]. Dead-time is used as a safety mechanism in power electronic circuits using some form of switches working in complement. The term refers to the time in between the turn-off of one switch and the turn-on of the other. Dead-time between the switches has been known as a significant source of harmonic distortion due to the error it generates in the output by the mismatch between input duty cycle and realised duty cycle with dead-time included [12], [16]. Finally, a significant source of distortion is the process of PWM in and of itself. The PWM process can be modelled as a DAC with 1-bit quantisation when converting the input of the modulator into a PWM waveform at the switches, as the switches can only be turned on or off. The resolution of the duty cycle itself is higher, but the change in output level is either fully on or fully off if the switching transitions are taken as ideal.

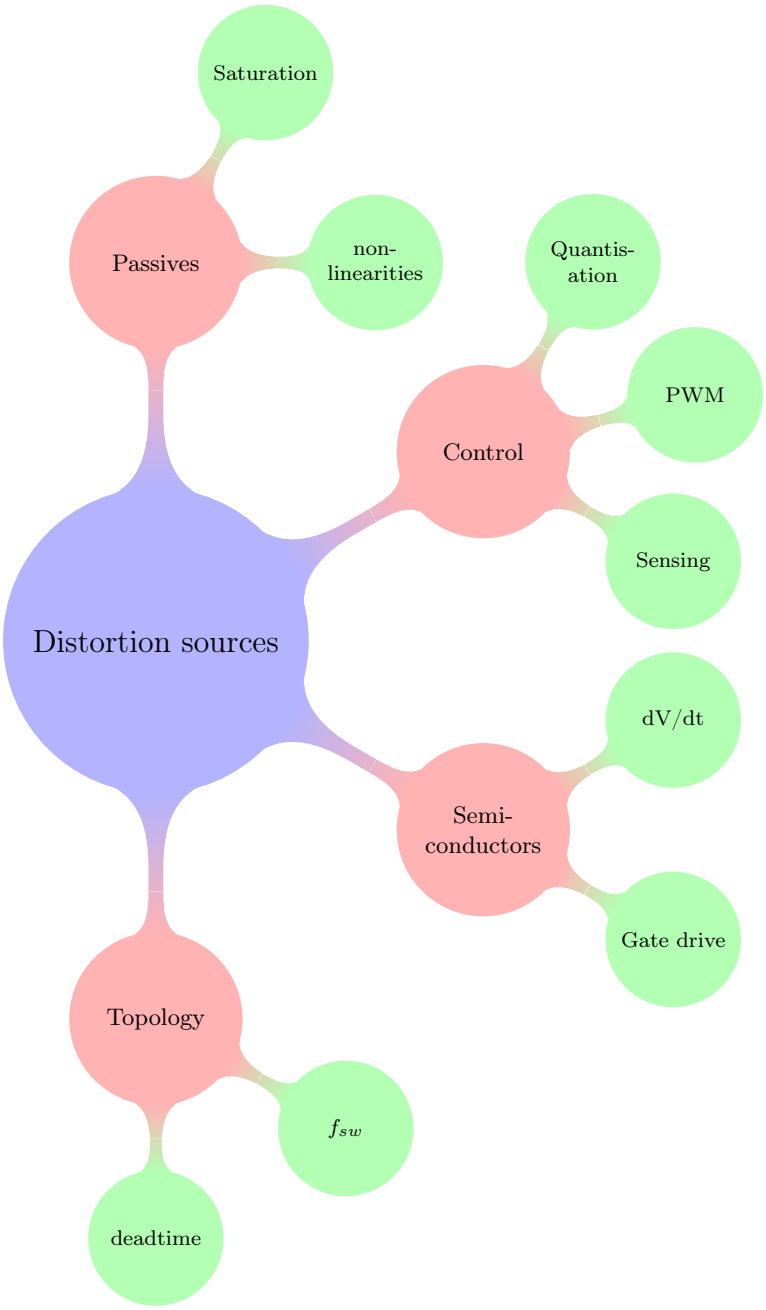



Figure 1.2: Distortion sources

## Research questions

- How can electromechanical actuator specifications be translated into requirements for power amplifiers?
- What factors impact the design of multilevel converters?
- What are the practical considerations when designing multilevel power amplifiers?
- How to design and control a flying capacitor high-bandwidth power amplifier?

## Objective

The challenge for the DCE&S group is to develop a high-bandwidth, small-footprint power amplifier suitable for these types of high-precision motion systems. Specifically, a power amplifier suitable for the Beat The Heat project. As previously identified, power amplifiers used in some novel actuators can be a limiting factor for

performance, with the required power, bandwidth, and precision needing to increase. In contrast, the generated noise and EMI need to decrease [8]. The development of such an amplifier will be the main objective of this thesis. This process will be split up into multiple tasks. The combination of these tasks will lead to the production and testing of the designed power amplifier.

- Task 1: Describe and model the effects the TMA coil has on electrical performance and use this to extract requirements for the converter
- Task 2: Model and design a power amplifier capable of meeting the requirements
- Task 3: Design and build the hardware prototype
- Task 4: Test the amplifier with the Beat The Heat hardware prototype

# 2 Tunable Magnetic Actuators

This chapter provides technical background on the tunable magnetic actuator and modelling of its dynamic behaviour. With this information, requirements can be set up for the design of the power amplifier.

## 2.1 Basics of tunable magnetic actuators

Tunable magnetic actuators are a relatively new and novel subset of hybrid reluctance actuators(HRA)[2]. For nano-positioning systems, classical Lorentz actuators, like voice-coils, have the distinct downside that they have a relatively low motor constant, which dictates the force-to-current ratio[17]. This means that a significant portion of the current is lost in the form of heat. This extra heat can be transferred to the mechanical system, causing it to expand due to thermal expansion. This, in turn, causes errors in the positioning of an actuator, presenting a challenge in the control and operation. These actuators have the advantage that they are more flexible, as they permit bidirectional actuation forces. Previous work has shown that the force density of (hybrid) reluctance actuators can be up to 10 times higher than Lorentz actuators [18]. However, classic reluctance actuators can only exert a unidirectional force and are therefore generally unsuited for position systems of the kind often required in the semiconductor industry.
Hybrid reluctance actuators can generate a bidirectional force by adding magnetic flux from either a biasing coil or a permanent magnet [19]. While a coil is helpful as the bias flux can be varied, it also produces extra losses in the form of heat. Therefore, a permanent magnet is most often used as a biasing source. This means that the biasing flux is fixed and can only be set by the choice of permanent magnet. This can be a disadvantage, as it affects the force output and is thus an uncontrollable variable in the system. This can be shown if the force equation for a hybrid reluctance actuator is derived according to [17]:

$$F = \frac{(\phi_{coil} + \phi_{pm})^2 - (\phi_{coil} - \phi_{pm})^2}{2\mu_0 A_g} = \frac{2\phi_{coil}\phi_{pm}}{\mu_0 A_g}, \tag{2.1}$$

where $\phi_{pm}$ is the permanent magnet airgap flu,x and $\phi_{coil}$ is the flux generated by the coil. From this, it is clear that the flux provided by the permanent magnet has an impact on the output force, but when there is zero current through the coil and therefore zero flux, there is no output force present. If the coil is replaced by a permanent magnet wrapped in a coil, the flux of the permanent magnet remains present even when there is zero current:

$$F = \frac{2(\phi_{coil} + \phi_{coil,pm})\phi_{pm}}{\mu_0 A_g}. \tag{2.2}$$

In this case, the permanent magnet used is a low coercive force magnet, like AlNiCo, which is more easily magnetised in situ. Thereby, a static force can be generated, even when there is no current present[2]. This is what the Beat The Heat project aims to do.

## 2.2 Tunable Magnetic Actuator design

With the basic concept behind (tunable) hybrid reluctance actuators covered, the design of the Beat The Heat actuator can be reviewed. For the tunable part of the actuator, the biasing flux is generated by a magnet made of AlNiCo5 material. This material has a low coercive force when compared to other permanent magnetic materials. The most recent design of the tunable magnetic actuator can be seen in Fig. 2.1

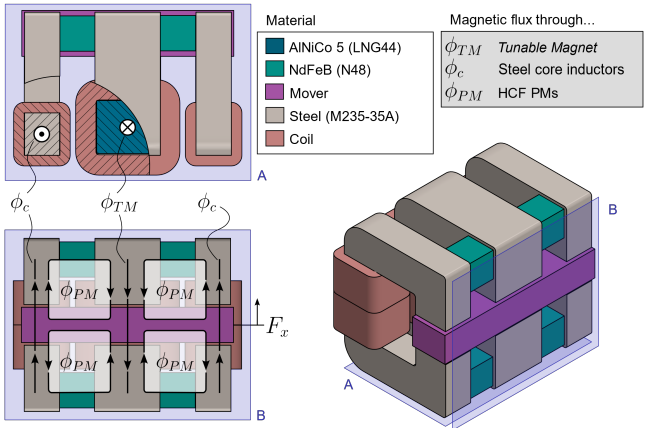



Figure 2.1: TMA design with flux paths

In this design, three coils are present and coupled to each other by permanent magnets. The outer two coils are also referred to as the Reluctance Actuator (RA) coils and are used for dynamic control of the mover, in contrast to the TM actuator, which provides a tunable static offset over a longer time frame. Permanent magnets couple the separate actuators to stop the flux of one coil from influencing another coil. Using the flux paths described in Fig. 2.1, the force equation for when the mover is in the middle of the coils can be determined as:

$$F_x = \frac{1}{2\mu_0}[2A_{RA}((B_{RA}+B_{pm})^2-(B_{RA}+B_{pm})^2)+A_{TM}((B_{RA}+B_{pm})^2-(B_{RA}+B_{pm})^2)]. \tag{2.3}$$

Here, the subscript $x_{RA}$ denotes the auxiliary coils, $x_{PM}$ the coupling permanent magnets and $x_{TM}$ the tunable magnet coil. If the assumption is made that the cross-sectional area of these coils is equal to the cross-sectional area of the magnet, then the equation simplifies to:

$$F_x = \frac{AB_{pm}}{\mu_0}(B_{RA}+B_{TM}). \tag{2.4}$$

Here, it can be seen that both the RA coil magnetic field and the tunable magnet field combine to form the controllable output force, while the permanent magnet field provides a fixed bias force. From this equation, it makes sense to control the magnetic field, or more accurately, the flux across the airgap, as the magnetic field is in $[Wb/m^2]$ and the flux is in $[Wb]$, and the area of the airgap does not change. Although even in this design, there is a static force output, the purpose of the permanent magnet is to separate the fluxes, and therefore it contributes little force and is easily overpowered by the large field produced by the tunable magnet, which thereby provides a bidirectional force.

## 2.3 Modelling of the tunable magnet

To model the system designed by the Beat The Heat project, it must first be determined what these models will be used for, so that the models do not become needlessly complicated. As the goal of this project is not to validate or redesign any part of the actuator, but to design a converter, the model should represent the effects its behaviour has on the electrical circuit, rather than on the magnetics or the output force and position. Therefore, a magnetic equivalent circuit model that shows the hysteresis behaviour of the tunable magnet will be used for the TMA, and a simple R-L circuit should suffice for the RA coils, as these do not exhibit hysteresis and should be kept under the magnetic saturation limit during operation.

### 2.3.1 RA coil model

The reluctance actuator, as seen on the outside in Fig. 2.1, is a simple C-core actuator with a large coil around the closed side. The steel used is selected to prevent saturation during operation. Therefore, this actuator can be seen as a linear system. The mover is rigidly fixed in its place and has minimal deflection in the current setup. Consequently, it can be assumed as fixed from the perspective of the electrical circuit. This means the actuator can be modelled simply by the use of Faraday's Law:

$$u_{RA} = Ri + \frac{d\phi}{dt} = Ri + L(x)\frac{di}{dt}. \tag{2.5}$$

As the position of this actuator does not vary significantly, the inductance can be considered constant for this model. To find the flux generated by this actuator, and thus proportionally the force, the equation can be rewritten in the following way:

$$\phi_{RA}(t) = \int_0^{\tau} u_{RA}(\tau) - Ri(\tau)\ d\tau. \tag{2.6}$$

As the area of the airgap does not change and the force relation can be gathered from rewriting Eq. 2.4, the force from this actuator can be expressed when the mover is in the middle:

$$F_x = \frac{AB_{pm,ra}B_{RA}}{\mu_0}, \tag{2.7}$$

the magnetic field can then be related to the flux through:

$$B = \frac{\lambda}{A}. \tag{2.8}$$

The parameters for the model can be derived from the dummy coil that will later be used for testing, or a first estimate can be made using the design variables of the actuator.

### 2.3.2 Tunable Magnetic Actuator

The TMA will also be modelled as a separate actuator, rather than being coupled together with the other coils, which is better suited to reflect the test conditions for the power amplifier. The approach taken for the RA coil cannot be used so easily on the TMA, as the equation for the TMA becomes:

$$u_{TM} = Ri + \frac{d\phi(x,H)}{dt} = Ri + L(x,H)\frac{di}{dt}. \tag{2.9}$$

Here, the flux and inductance are not only dependent on the position of the mover, but also on the history of the magnetic field intensity. This makes it challenging to model, as the hysteresis behaviour is essential to the dynamics of this electrical system and can therefore not be simplified. To incorporate this behaviour, the Magnetic Equivalent Circuit (MEC) approach will be employed. This method uses the lumped-circuit principle for electrical circuits and applies it to magnetic systems [20]. This allows for the modelling of the TMA based on its physical dimensions and material choices, while adhering to the circuit rules of electrical circuits. This model is made using the simulation software PLECS, which includes a magnetics domain modelling library based on MEC principles. For this model, all parts will be assumed to be linear, except for the tunable AlNiCo5 magnet. This will be modelled using the Preisach method for modelling hysteresis behaviour as described by [21], which is also incorporated into PLECS. The Preisach model utilises hysterons, which are discrete hysteresis operators distributed across a hysteresis plane, known as the $\alpha, \beta$-plane. These operators can have a value of either 1 or -1:

$$\gamma_{\alpha\beta}(u(t)) = \begin{cases} -1, & u(t) \leq \beta; \\ \gamma_{\alpha\beta}[u(t)], & \beta \leq u(t) \leq \alpha; \\ 1, & u(t) \geq \alpha. \end{cases} \tag{2.10}$$

Here, $u(t)$ is the input of the model. In a numerical approach, a grid of equally spaced hysterons is generated in the hysteresis plane. A so-called Preisach function can then be specified for the hysteresis plane:

$$f(t) = \iint_{\alpha>\beta} \mu(\alpha,\beta)\gamma(\alpha,\beta)u(t)d\alpha d\beta. \tag{2.11}$$

In this function, $\mu(t)$ is the weighting function and determines the impact of the hysterons in a certain region of the plane. This function is based on the material properties of the magnet and can either be determined using measured data from the magnet or can be approximated parametrically [22]. The latter approach is employed in PLECS, utilising a Lorentzian distribution function derived from theoretical material properties and mechanical dimensions. With the hysteresis modelling included, the model of the TMA can be made in PLECS as seen in Fig. 2.2

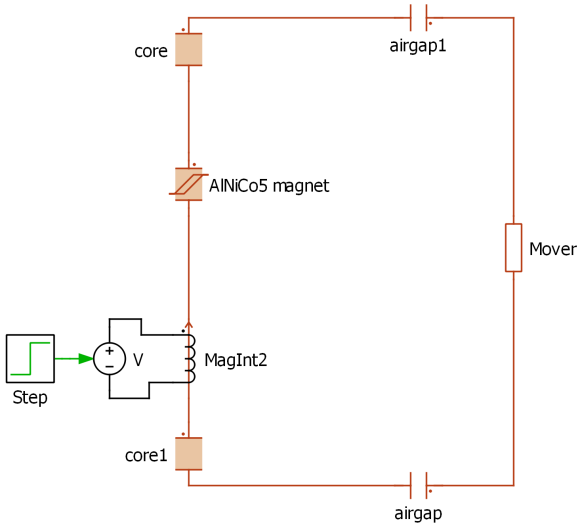



Figure 2.2: PLECS model of the TMA

To show the hysteresis behaviour in this stage of the project, the coil can be excited using a ramping sinusoidal wave. This results in the BH-plot seen in Fig. 2.3

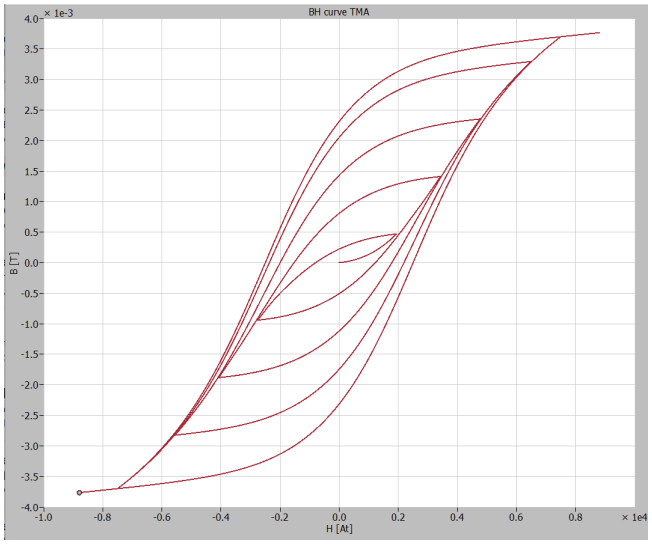



Figure 2.3: BH curve generated by Preisach model in PLECS

This figure shows that both the minor and major loops of the BH curve can be simulated using the Preisach model. At the same time, it is challenging to verify the accuracy of this model at this point, as no measurement data is available. However, the behaviour of the simulation matches expectations and can, at a minimum, be used to verify the working of the power electronics simulation later on.

### 2.3.3 Beat The Heat requirements

With the modelling techniques described, other requirements related to the project are defined:

- Required output voltage: $\pm 300\ V_{dc}$
- Required output current TMA: $10\ A$ at $t_{pulse} \approx 10\ ms$
- Required output current RA:5 $A_{peak}$ at $f_{sw} \gg 20\ kHz$

In addition to these, some other requirements are also needed. To determine these, the control loop for the TMA can be analysed. As mentioned in a previous section, the system will be controlled through a closed-loop

flux controller that regulates the flux in the air gaps of the mover. To visualise this, a diagram of the control scheme has been developed in Fig. 2.4

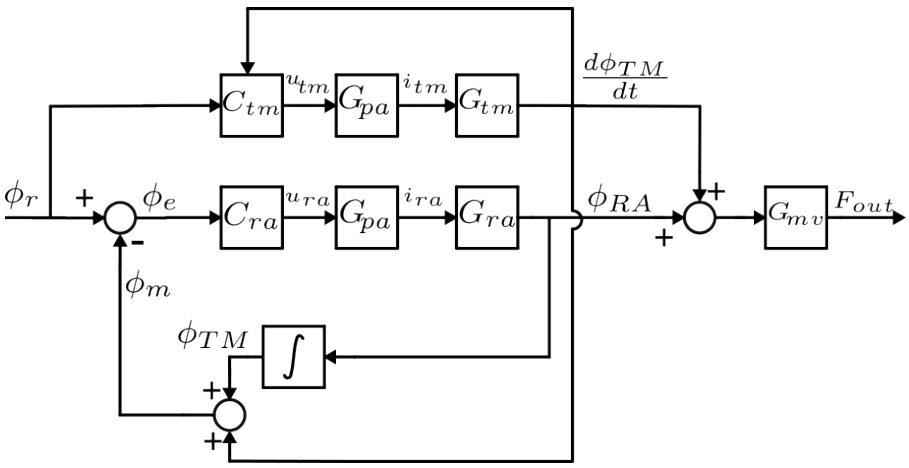



Figure 2.4: Flux control loop

In this figure, $G_{pa}$ indicates the power amplifier for the system. As can be seen, the input to the power amplifier is a voltage, not a current. Therefore, a voltage control loop within the power amplifier will be necessary to maintain the correct voltage at the converter's output. As the amplifier will likely be a voltage source inverter, the output will still exhibit a current characteristic. Therefore, a second outer loop will be necessary to control the voltage.

## 2.4 The case for multilevel inverters

The actuators described require an amplifier, which is the core of this project. Therefore, a power electronics topology for the amplifier should be chosen. While interesting topologies based on modifications of more conventional 2-level converters have been the subject of research for use with electromechanical actuators [8], [12], there seems to be a lack of research on less conventional topologies specifically for use in electromechanical actuators and power amplifiers. Keeping in mind the discussion on bandwidth and distortion, multilevel converters come to mind. These topologies, as the name indicates, are able to generate multiple output levels with a single input. A comparison of multilevel topologies and the two-level topology is given in Tab. 2.1. One important point which has not been mentioned yet is the impact of surge voltages on the windings of actuators. This is partially determined by the dV/dt at the output of the converter or filter. These surges can degrade the insulation layer on the windings and eventually lead to short-circuits and failure of the windings [23].

Table 2.1: Topology comparison

| **Parameter** | **Two level** | **Multilevel** |
|---|---|---|
| Output frequency | $f_{sw}$ | $N_{level} f_{sw}$[24] |
| Current stress | $i_{sw} = i_o$ | $i_{sw} = i_o$ |
| Voltage stress | $V_{sw} = V_{DC}$ | $V_{sw} = \frac{V_{DC}}{N_{level}}$ [24] |
| Output quantisation | 1-bit | N-bit |
| Complexity | low | increases with number of levels |
| Number of switches | two | $2N_{level}$ |
| dV/dt at actuator windings [23] | $\frac{dV_{coil}}{dt} \approx \frac{V_{dc}}{2t_{sw}}$ | $\frac{dV_{coil}}{dt} \approx \frac{V_{dc}}{2N_{level}t_{sw}}$ |

These multilevel topologies could address some of the concerns raised with conventional switched-mode power amplifiers as discussed in [14]. Combining these topologies with modern wide-band-gap semiconductors could even further limit the output distortion due to their lower parasitics and fast switching. However, there seems to be a lack of research into these topologies specifically for use within power amplifiers, focused on electromechanical or mechatronic systems. Therefore, one of the goals of using multilevel topologies is to investigate what is needed to use these as power amplifiers.

# 3

# Multilevel converters

This chapter covers the fundamentals of multilevel inverters and selects one topology based on the previous chapter.

## 3.1 Multilevel converters as power amplifiers

In its basic form, most multilevel converters are a natural extension of common two-level half-bridge converters as seen in Fig. 3.1.

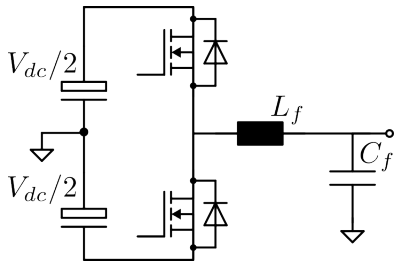



Figure 3.1: Basic half-bridge switching cell

This half-bridge can only generate two voltage levels and must be able to withstand the full switching voltage and currents. This has historically limited the use of power electronics (outside of thyristors) in specific industrial settings where high power demand is required and modest switching frequencies are necessary. This was due to the available semiconductors being unable to handle the voltage and currents in traditional two-level topologies. This led to the development of higher-power semiconductor technology, as well as the development of multilevel converters [24], which in turn led to the use of multilevel converters in medium- to high-voltage, high-power industrial applications, such as reactive power compensators, electrical machine drives, and high-voltage transmission stations, in the Mega-Watt power rage [25], [26].

More recently, these types of converters have become of interest for grid-connected inverters used in solar panels and similar applications [27]–[30] due to their high bandwidth and improved voltage quality. This reduces the required output filtering for grid connection, thus reducing the required volume and increasing power density.

The above examples illustrate the rise and application of the multilevel converter in various academic and industrial settings. The use of these converters in electrical machines is primarily focused on the high-voltage, high-power market. In the case of low-voltage single-phase converters, they are primarily used for grid-interfacing and systems that require high-quality output voltage, but lower output frequencies. The use case for these topologies in low-voltage power amplifiers is less explored, but the benefits for ultra-high-bandwidth power amplifiers are discussed in [14]. Here, the power amplifier is used as a Power-hardware-in-the-loop simulator. While this does not directly align with the use of these amplifiers in precision mechatronic systems, it does show their possibilities with regard to high-frequency output. Especially when considering the requirements for power amplifiers in precision motion systems, as discussed in [13] and the previous chapter. Therefore, these topologies will be the main focus for the basis of the power amplifier in this project.

## 3.2 Basic multilevel switching cells

The basic half-bridge switching cell serves as the building block for many multilevel topologies. This cell can generate two voltage levels with its two switches, $\pm\frac{V_{in}}{2}$. This results in a square wave output. This switching cell typically requires significant filtering to meet output quality requirements. An approach to solving this would be to make the output resemble the required output waveform more closely before any filtering is done. This could be done by adding more switching cells in a specific configuration. This is often done in 2 major ways: parallel or series interleaving

### 3.2.1 Parallel interleaving

If a higher current is required, there are two options. Increase the current rating of the switch, or interleave multiple switches in parallel. These parallel cells can then be coupled to a common node through inductors, as seen in Fig. 3.2, to generate multiple voltage levels.

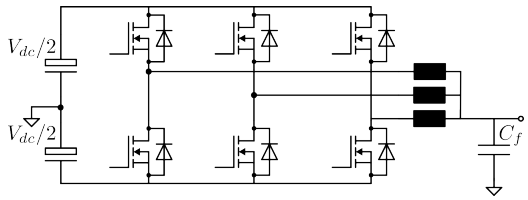



Figure 3.2: 3-level parallel interleaved converter

This configuration can output $N_{cell} + 1$ voltage levels. It achieves this by utilising the output as a sort of voltage divider, where the ratio of the individual cell voltages adds or subtracts from the total voltage to generate specific voltage levels. The current per switch can be expressed as:

$$I_{sw} = \frac{I_o}{N_{cell}}. \tag{3.1}$$

In this equation, $N_{cell}$ is the number of parallel connected switching cells. The switches in this configuration still need to block $V_{dc}$, but the effective switching frequency is increased. This can be expressed as:

$$f_{sw,eff} = N_{cell} f_{sw}. \tag{3.2}$$

This is another advantage over just increasing the current rating of the switch. While parallel interleaving reduces the current rating of devices, the voltage rating generally dominates the switching losses and on-resistance [31]. This method does not reduce the required blocking voltage of a switch, only its current load.

### 3.2.2 Series interleaving

Series interleaving uses the same principle of adding half-bridge cells to the topology, but it connects these cells in series with one another as seen in Fig. 3.3

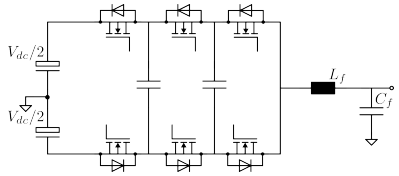



Figure 3.3: Series interleaving flying capacitor converter

The number of output levels is the same as for the parallel interleaved converted, so $N_{cell} + 1$. In this setup, the switch blocking voltage is reduced to:

$$V_{sw} = V_{dc}/N_{cell}, \tag{3.3}$$

where $N_{cell}$ is the number of series-connected switching cells. In this case, the switch current equals the output current for each switch. This imposes stricter requirements on the current rating of the switch. However, as noted before in [31], the voltage rating of the switch is the dominant factor in determining the switching and conduction losses. Therefore, increasing the number of series legs allows for the use of a lower blocking voltage switch, further enhancing the converter's performance.

Both of these techniques can also be used together as a series-parallel-interleaving approach. This combines the advantages of both, but at a higher semiconductor cost.

### 3.2.3 LC-filters in multilevel converters

With the two most basic forms of multilevel converters covered, the significant filtering benefits of the increased semiconductor effort can be analysed. This will be done using a generalised series-parallel-interleaved multilevel converter. As defined by Eq. 3.2, the switching frequency is increased with the number of levels. In general, an LC-filter is used as the output filter in these types of converters[32] as can be seen in Fig. 3.4. To analyse the effort required by the filter, the output current ripple can be used.

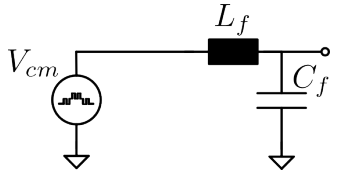



Figure 3.4: LC filter with multilevel waveform as input

The inductor current ripple in a generalised series-parallel-interleaved multilevel converter can be derived from the standard equations for 2-level converters and is described by [33]:

$$\Delta I_f^{pkpk} = \frac{\frac{Vsw}{n_p n_s}}{4L_f(n_p n_s f_{sw})}. \tag{3.4}$$

The same can be done for the capacitor voltage ripple:

$$\Delta V_f^{pkpk} = \frac{\frac{\Delta I_o^{pkpk}}{4}(\frac{1}{2n_p n_s f_{sw}})}{C_f}. \tag{3.5}$$

In both of these equations, $n_p$ indicates the number of parallel cells and $n_s$ the number of series cells. Using these equations, the effects of the number of switching cells on the inductor and capacitor values can be determined.

$$L_f = (\frac{n_p}{n_s^2})V_{dc}/(4\Delta I_{pkpk} I_o f_{sw}), \tag{3.6}$$

$$C_f = \frac{(\frac{I_o \Delta I_{pkpk}}{V_{dc}\Delta V_{pkpk}})}{(8 f_{sw} n_s n_p^3)}. \tag{3.7}$$

With these equations, it becomes clear that the number of parallel and series cells lowers the required capacitance and inductance at different rates. It should be noted that the inductance and capacitance decrease, but the filter's performance remains unchanged. The normalised values for the capacitor and inductor can be plotted for both the parallel and series interleaving as seen in Fig. 3.5 and Fig. 3.6. Note that for both of these figures, the voltages and current ripples are identical.

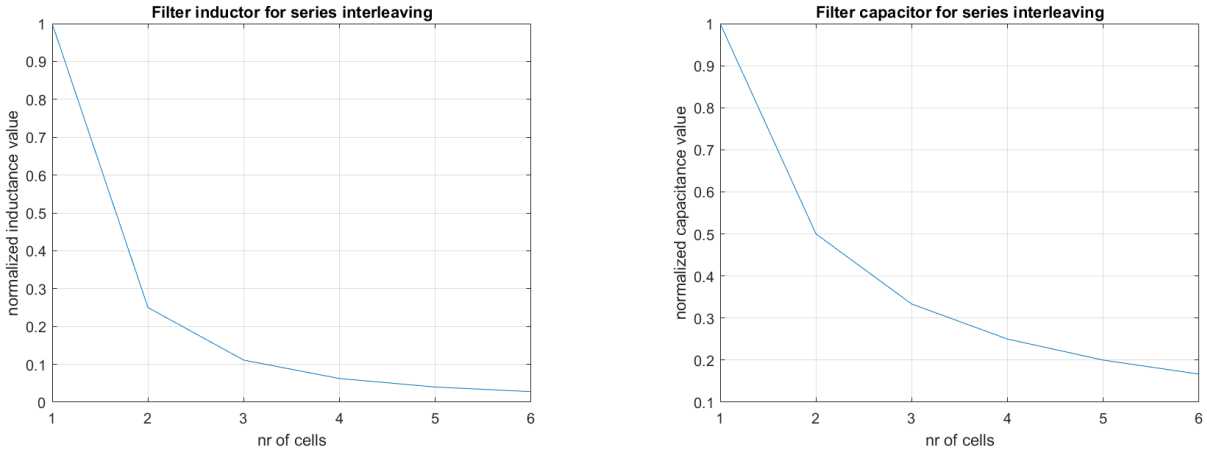



Figure 3.5: LC filter values for series interleaving

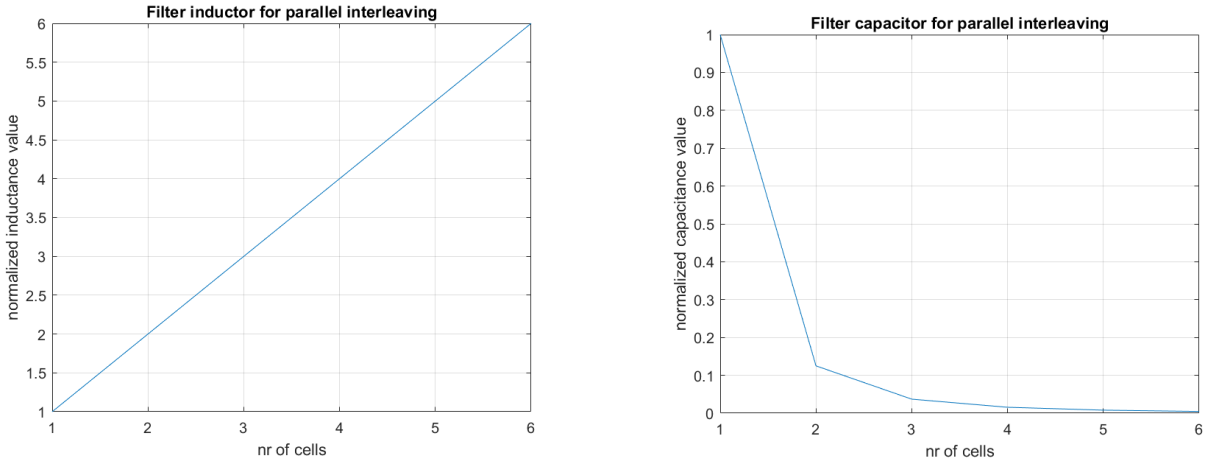



Figure 3.6: LC filter values for parallel interleaving

As can be seen for the capacitor values of both series and parallel interleaving, the number of cells decreases the required capacitance. For the inductor, however, the inductor value for parallel interleaving increases with the number of cells. This makes sense, as each parallel branch requires a separate inductor, thereby increasing the total inductance. In reality, the current ripple per inductor and rms current are much smaller in a parallel setup, as the current is divided by the switches, determined by Eq. 3.1. This leads to a significant decrease in total inductor volume as indicated by [32]. Here, a parallel cell inductor has a 0.1 volume FOM at three cells, where a FOM of 1 is a single-level cell. This is even better than the series configuration, which has a FOM of 0.2 at three levels. This same effect is seen in the capacitor volume. Therefore, if the volume of the LC filter is a significant concern, a parallel or series-parallel interleaved converter would be ideal.

## 3.3 Multilevel converter topologies

With the structure of the basic multilevel switching cells defined, an overview of different topologies can be made. These topologies utilise basic switching cells and expand upon them to enhance performance in various ways. An overview of some topologies can be seen in Fig. 3.7

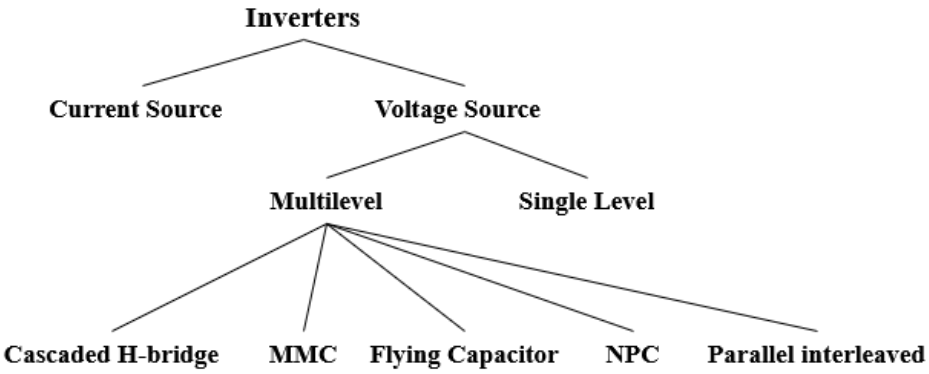



Figure 3.7: Multilevel converter topologies

While current source inverters are not expanded upon, they possess rather interesting properties combined with new wide-bandgap semiconductors and have renewed research interest, as discussed in [34], but are outside the scope of this project due to the added complexity. The voltage source inverters are split between standard single-level converters and multilevel converters.

### 3.3.1 Cascaded H-bridge

This converter utilises separately sourced isolated H-bridges in a series-connected fashion to generate a multilevel output at an increased effective switching frequency, as discussed before. The separate sources are isolated from each other. This means that each cell requires its own isolated power supply. The basic layout of this topology can be seen in Fig. 3.8

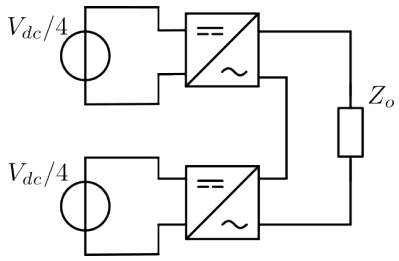



Figure 3.8: 5-level, two cell, Cascaded H-bridge topology

Note that the H-bridges can output the full isolated supply voltage, rather than $V_{dc}/2$, as is the case for the half-bridge switching cells. The switches only need to block $V_{dc}/2n_{cell}$, which further reduces the switching stress. The AC output of these converters is connected between cells, allowing for a multilevel voltage output. These types of converters are fully modular and can be bypassed and enabled whenever required.

These converters were first proposed in the 1970s, primarily for use in high-power, high-voltage applications such as switching substations [14]. They were only suggested for use in power amplifiers after 2000 [35]. This topology is ideal for systems that require a high output voltage, and isolation is a priority. Furthermore, this topology features numerous built-in redundancies, as the H-bridge switching cells have overlapping output voltage states. Therefore, multiple switching states can generate the same output voltage. This redundancy can also be eliminated and leveraged by using asymmetrical DC-link voltages to the cells. This allows the same number of cells to generate a higher amount of different switching levels than if symmetrical DC-link voltages are used[36].

While the aforementioned benefits align with the project's requirements, the required isolated voltage supplies complicate the design in a way that is not necessary for this project. The essential benefits of multilevel output, higher effective frequency and reduced switch blocking voltage can also be achieved using different topologies, which may require less design effort.

### 3.3.2 Modular multilevel converter

The Modular Multilevel Converter, or MMC, is a type of converter that is popular in the high-voltage, high-power region and is used in HV DC-substations. These converters are similar to the cascaded H-bridge converters mentioned in the previous section, but do not require an isolated supply per cell. They do need a local capacitor per cell, which maintains the voltage. While these are interesting converters, they are generally not suitable for DC or very low frequencies without complicated control due to the floating capacitor that requires balancing. The capacitor voltage ripple increases as the output frequency decreases, which could be problematic for use on the TMA coil due to its pulsed current requirements. [37]. Therefore, the MMC is not as suitable. Combined with its higher design complexity due to the design of the switching cells, this topology does not suit this project well.

### 3.3.3 Neutral-point-clamped converters

Neutral-point-clamped, or NPC, inverters are one of the most widely used multilevel inverters in industrial medium-voltage applications [38]. They utilise the basic structure of the series-switching cell and connect these at the shared neutral point using a diode, hence the name "neutral-point (diode)- clamped." The structure of a 3-level NPC circuit can be seen in Fig. 3.9.

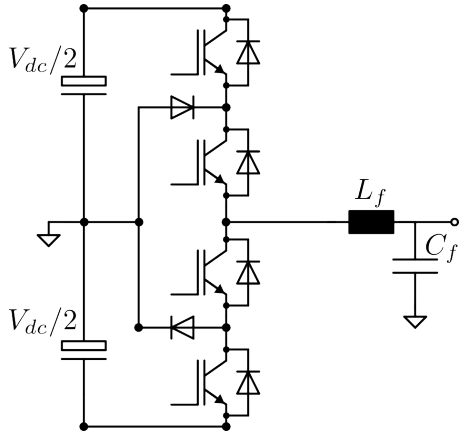



Figure 3.9: 3-level NPC inverter

Although only two switching cells are visible, the third switching level is generated by the clamping diodes connected to the neutral point. From this, it is also clear that the switches have a reduced blocking voltage. To increase the number of levels in an NPC inverter, new clamping points need to be created. This means increasing the number of DC-link capacitors and the number of diodes required to connect to these new neutral points. This leads to complications in DC-link charge balancing and control. Furthermore, this also adds significant costs and design complexity [24].

### 3.3.4 Flying Capacitor converter

The Flying Capacitor Multilevel (FCML) converter is very similar to the NPC inverter, except that the clamping diodes are replaced by capacitors. This adaptation from the NPC can be seen in Fig. 3.10.

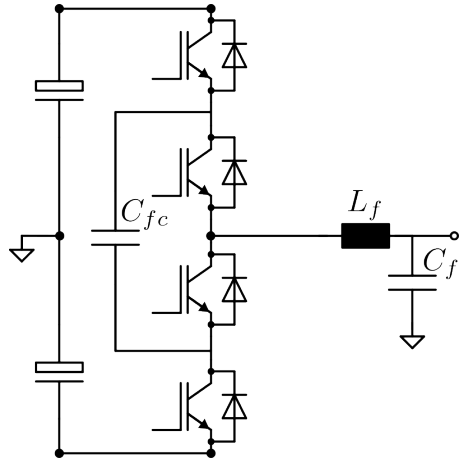



Figure 3.10: 3-level FCML inverter

The FCML can generate its multiple voltage levels by connecting the flying capacitors to the load in different configurations. These capacitors are charged to a varying DC voltage as governed by the following equation:

$$V_{C,k..(N-1)} = \frac{kV_{dc}}{N-1}. \tag{3.8}$$

Here, $k$ is the given capacitor, starting from $k = 1$ at the load side and counting up towards the source, and $N$ is the number of voltage levels. From this, it can be gathered that the capacitors are all charged to different voltages, and this fact can be used to synthesise the required output voltage level. In contrast to the NPC inverter, the FCML cannot generate a zero voltage by connecting the load to the neutral point; instead, it must generate a zero voltage by connecting the flying capacitor in the opposite polarity of the DC-link capacitor. From this, it is clear that multiple combinations can generate this voltage level, either by using the upper or lower half of the DC-link capacitor. If the converter is expanded to a higher number of switching cells, even more redundant combinations are possible [24]. This enables active control of the voltage balances in the cells,

without requiring any additional hardware. The structure of these switching cells enables the FCML topology to be easily expanded to higher levels. The FCML offers nearly all the benefits of the cascaded H-bridge topology, but without the complexity of separate isolated voltage sources at the cost of a lower number of redundant states. The capacitor voltage balance can be a problem, but this will be discussed in detail later.

FCML inverters have gathered more research interest in recent years [39]–[43] as wide band-gap semiconductors, such as GaN, became more available and more powerful. This topology retains many of the attractive features of multilevel inverters, such as a high effective switching frequency, lower switch blocking voltage, and high power density. It does this without the increasing circuit complexity as much as compared to other multilevel topologies. The challenges at higher levels are caused by the need for multiple PWM modulators and increasing sampling requirements as the output frequency increases.

### 3.3.5 Interleaved dual buck converter

The final topology to be discussed is the interleaved dual buck converter. This converter is essentially a pure parallel switching cell, as shown in Fig. 3.2, where the lower switch can be replaced by a diode, as illustrated in Fig. 3.11. The primary benefit of this topology is the absence of dead time between switching states. This reduces distortion due to the lack of a zero-crossing in the transition between switching states, as discussed in [13]. As this topology is fully parallel, the switch blocking voltage is the full DC voltage, but the current is shared among all the switches and diodes. The synchronous version of this topology was able to achieve a THD of -57dB [8]. This version is a parallel switching cell, as discussed in the previous section.

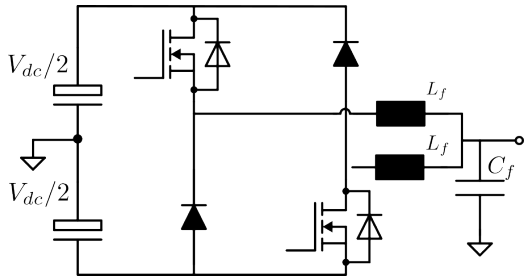



Figure 3.11: interleaved dual buck converter

The main disadvantage of the interleaved dual buck converter is that the blocking voltage remains constant for any number of levels, and the number of required filters increases accordingly. As the switching voltage is the full DC voltage, the $\mathrm{d}V/\mathrm{d}t$ of the switching cells remains quite large, especially if the switching frequency is increased, as will likely be required to achieve the high output bandwidth.

### 3.3.6 Choosing a topology

With the overview of the topologies and the requirements from the previous chapter, a choice of topology needs to be made. As the time and scope of this project are limited, only one topology can be analysed in detail and developed as a prototype. The most challenging requirement is the closed-loop bandwidth of 10 kHz, and therefore, it is used as an essential selection criterion.

Firstly, the CHB converter meets the requirements well, but it has the increased complexity of isolating all the supplies, thereby complicating the design and control. The MMC converter does not perform as well at DC or low frequencies and has increased design complexity.

This leaves the Flying Capacitor and the interleaved dual buck converter. Both of these topologies have the advantage of increasing the effective switching frequency and decreasing the LC-filter size. The main difference between the two is the switch current and the blocking voltage. The Flying Capacitor topology reduces the blocking voltage but does not decrease the switch current. In contrast, the interleaved dual buck converter reduces the switch current while maintaining the blocking voltage. A final option would be to interleave a flying capacitor circuit, thereby decreasing both the current and voltage ratings. This comes at the cost of higher circuit complexity and increased semiconductor effort. Reducing the required blocking voltage could enable the use of lower-voltage semiconductors. These have better performance characteristics, such as lower input/output capacitance and lower on-state resistance [31].

As the switching frequency must be high to meet the output requirements, EMI can be problematic for the converter's proper operation. Therefore, lowering the $\mathrm{d}V/\mathrm{d}t$ by reducing the voltage per switch will reduce EMI problems, lower switching noise, and increase the SNR. It should be noted that likely all of the topologies could

function as a power amplifier, but considering the design complexity and the scope of this project, only one topology is selected for further study. The flying capacitor converter is therefore selected.

## 3.4 Flying Capacitor Multilevel converter

In this section, the theory of operation of the flying capacitor converter will be discussed. In a subsequent chapter, a model will be made for design purposes.

### 3.4.1 Operating principles of flying capacitor converters

As noted earlier, the flying capacitor converter generates multiple voltage levels by connecting and disconnecting flying capacitors charged to different voltage levels. To help understand the workings of the flying capacitor, an annotated 5-level version is shown in Fig. 3.12.

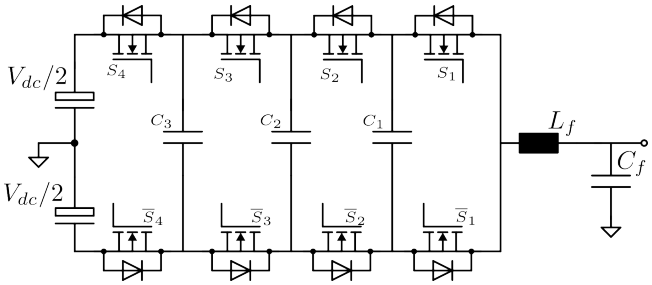



Figure 3.12: 5-level flying capacitor inverter

Here, a 5-level converter consisting of 4 commutation cells can be seen. A commutation cell consists of 1 flying capacitor and two switches. First, some rules for switching and design can be set [44]:

- The number of switching cells for a $n$-level converter is $n-1$, with a voltage rating of $V_{dc}/(n-1)$
- The number of flying capacitors for a $n$-level converter is $n-2$, which are charged to a voltage of $V_{c,k..n-2} = k\frac{V_{dc}}{n-1}$
- Switches $S_k$ and $\overline{S_k}$ switch complementarily and must therefore never conduct at the same time or be open-circuited at the same time
- A dead-time between switches $S_k$ and $\overline{S_k}$ is required

With these rules, the switching states can be analysed. First, this 5-level converter cannot generate a zero voltage directly by connecting the converter to ground, as there is no direct path. To generate 0 Volts, capacitors must be connected in such a way that the resultant voltage is 0. This can be done in multiple ways. Therefore, there are multiple redundant states. This applies to all voltage levels. The working principle of the converter is seen in Fig. 3.13.

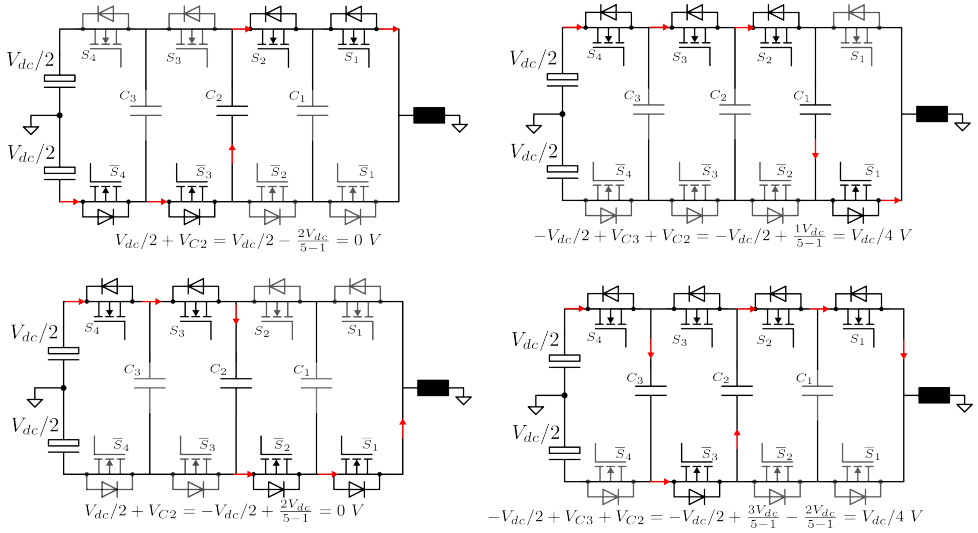



Figure 3.13: Switching states of FCML converter

From this, it becomes clear that there are multiple redundant switching states which generate the same output voltage. The number of combinations increases with $2^{n-1}$. This is a positive aspect, as it helps maintain capacitor balance. From the figure, it can also be seen how the cell voltage across the switches remains constant, even though the capacitors are charged to different voltages, as the switch voltage is imposed by the adjacent capacitors, instead of the input source:

$$V_{S,k} = V_{C,k} - V_{C,k-1} = \frac{kV_{dc}}{n-1} - \frac{(k-1)V_{dc}}{n-1} = \frac{V_{dc}}{n-1}. \tag{3.9}$$

This is beneficial in multiple ways, as the voltage stresses are significantly reduced at higher levels.

The current through the turned-on switches remains equal to that of the total load current. In combination with the switch duty cycle, this can be expressed as:

$$I_{S,k} = \delta_k I_{out},\ I_{\overline{S},k} = (1-\delta_k) I_{out}. \tag{3.10}$$

Consequently, the capacitor current can also be derived:

$$I_{C,k} = I_{S,k+1} - I_{S,k} = I_{out}(\delta_{k+1} - \delta_k). \tag{3.11}$$

From this, it becomes clear that if the duty cycles of all the switches are equal, the effective average capacitor current is zero, and thus the voltage should be stable:

$$V_{C,k} = V_{initial} + 1/C_k \int_0^T I_{C,k}\ dt = V_{initial} + 1/C_k \int_0^T I_{out}(\delta_{k+1} - \delta_k)\ dt = V_{initial}. \tag{3.12}$$

While this is true in theory, there are non-idealities, like the ESR of the capacitors or parasitic inductance, which are not taken into account and can destabilise the capacitor balance. These non-idealities will be dealt with later.

For the output voltage, a convenient notation is the common mode duty-cycle, which is the effective duty-cycle which describes the effective output voltage of the converter, without having to determine all the switch nodes:

$$V_{cm} = \delta_{CM} V_{dc}/2, \tag{3.13}$$

where $\delta_{CM}$ is defined as the sum of all duty-cycles:

$$\delta_{CM} = \sum_{k}^{n-1} \frac{\delta_k}{n-1}. \tag{3.14}$$

From this, the benefits of a multilevel converter in reducing the output current ripple can be demonstrated by comparison with a standard buck converter. The inductor ripple in a buck converter can be described by:

$$\Delta i_L = \frac{V_{in}(D(1-D))}{L f_{sw}}. \tag{3.15}$$

This is the same for the multilevel converter, except the duty cycle, $D$, needs to be replaced by the effective duty cycle, $D_{eff}$:

$$D_{eff} = D(n-1) - \text{floor}(D(n-1)). \tag{3.16}$$

This is necessary because there are multiple locations on the duty-cycle spectrum where a static voltage output level is achieved, similar to $D = 1$ or $D = 0$ for a standard buck converter. This leads to:

$$\Delta i_L = \frac{V_{in}(D_{eff}(1 - D_{eff}))}{L f_{sw}}. \tag{3.17}$$

From this, the duty cycle can be plotted against the current ripple as seen in Fig. 3.14. From this figure, a significant decrease in current ripple can be observed.

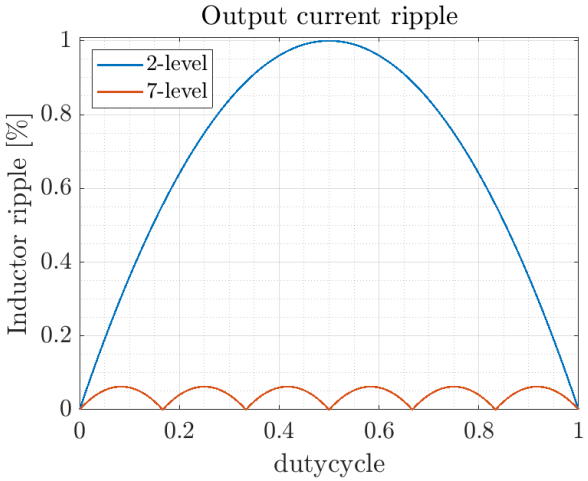



Figure 3.14: duty-cycle compared with inductor ripple in 2-level and 5-level buck converter

It can be seen that the ripple goes to zero for multiples of 1/4, as this means an output voltage that can be directly made by one of the flying capacitors is required. In the case of the inverter and AC signals, this analysis becomes more difficult, but the same ripple benefits are still kept.

### 3.4.2 Capacitor voltage balancing

Previously, it was shown that in an ideal scenario, the capacitor voltages are inherently balanced. Unfortunately, this is not always the case in real life due to non-idealities, parasitic and the effects of certain modulation indices [45]. The voltage balance is crucial to ensure the proper performance and safety of the converter. Excessive capacitor voltage imbalance could cause damage to switches, which can be seen by way of an error factor in the capacitor voltage:

$$V_{S,k} = \beta_k V_{C,k} - \beta_{k-1} V_{C,k-1}. \tag{3.18}$$

If both error factors are opposite of each other, the switch voltage could increase to a high enough level to move the switch outside of its safe operating area, eventually leading to failure.

Therefore, active balancing of the capacitors could be required. This can be implemented in several ways, for instance, through closed-loop control and measurement of the specific voltages[45], [46], or an extension of valley current control[47]. Note that in these papers, the number of output levels for experimental converters does not exceed five levels, and the output frequency does not exceed 100kHz. This is most likely due to the challenges of implementing these active strategies for high output levels and high frequencies on digital control platforms, such as microcontrollers or FPGAs. As both a higher number of levels and switching frequency are required, these active methods could become difficult.

However, previous work has shown that flying capacitor converters, when driven with a phase-shifted carrier-based PWM, exhibit natural voltage balancing [44], [48]–[50]. The cause of this is the harmonics in the converter. Parasitics, unequal gate-drive voltages or many other sources could cause the drift in capacitors. When the voltages drift, harmonics occur in the switches. These harmonics can be modelled by incorporating the frequency spectrum of standard carrier-based PWM [48]. These can be incorporated into the equations described in the previous sections. To represent these, a Double Fourier series can be used:

$$S_k = \frac{C_{00}}{2} + \sum_{n=1}^{\infty}[C_{0n}\cos(n[\omega_0 t + \phi_0])] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[C_{mn}\cos(m[\omega_c t + \phi_{c,k} + n[\omega_0 t + \phi_0]])], \tag{3.19}$$

where $\omega_0$, $\omega_c$ ,$\phi_0$ and $\phi_{c,k}$ are the reference and carrier frequencies and phase-shifts. $C_{mn}$ are the harmonic magnitudes of the main, carrier and sideband frequencies. This is defined by:

$$C_{mn} = \frac{2}{m\pi} \sin([m+n]\frac{\pi}{2}) J_n(m\frac{\pi}{2}M). \tag{3.20}$$

The harmonics modelled by these functions increase the dissipation in the load, which in turn stabilises the capacitor voltages. In theory, for this to work, real power loss is required, and this strategy does not work for purely reactive loads[49]. However, parasitic elements in the converter are, in practice, a large enough source of real power draw to minimise this issue [40]. This could still be problematic for the Beat The Heat project, as the TMA coil has a significant reactive power component, although it also includes a resistive loss element. To ensure that the real power draw still causes sufficient natural balancing, a PLECS simulation model will be developed in a further chapter. This model can be coupled to the previously developed load models.

# 4 Digital control of Power Electronics

This chapter describes the basics of digital control theory applied to power electronics, starting from basic continuous control and expanding it to multilevel control strategies.

## 4.1 Basics of digital control

First, to efficiently describe the requirements of (digital) control of power electronics, the goals that need to be achieved should be clarified. The controller for this project needs to do two things. It needs to control the inner-loop current and the outer-loop voltage. As described in Chapter 1, the flux controller for the TMA and RA coils will output a voltage that is required at the input of the coils. Therefore, the overall goal of the controller is to generate this output voltage while maintaining the controller's stability and safety. To achieve this, closed-loop controllers are required. The basic continuous-time control loop applied to a power converter will serve as a starting point for developing a digital, discrete-time control loop model that can be adapted for multilevel inverters.

### 4.1.1 Continuous time control of power converters

To start, a continuous-time model means that all signals are continuous and there are no discrete time steps. This is the most basic form for control models, as everything can be represented in continuous-time equations. A simple two-level half-bridge inverter will be used initially, which can be expanded into a flying capacitor multilevel inverter at a later stage. This control loop is shown in Fig. 4.1.

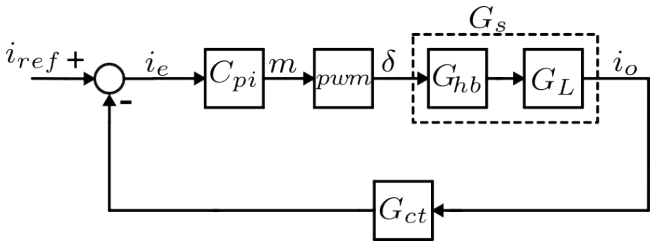



Figure 4.1: Continuous-time control loop of a half-bridge inverter

In this figure, the current controller $C_{pi}$ generates a modulation setpoint based on the error between the current reference and the measured current. The control law for a simple PI control is:

$$C_{pi} = \frac{m}{i_e} = K_p + \frac{K_i}{s}. \tag{4.1}$$

where $1/s$ is the Laplace equivalent of an integral, $K_i$ is the integral gain and $K_p$ is the proportional gain. The output of the PI controller is a modulation index. This index can then be used to generate a PWM waveform that can drive the switches. If naturally sampled carrier-based PWM, thus continuous-time, is assumed, the transfer function simply becomes [51]:

$$\frac{\delta}{m} = \frac{1}{c_{pk}}. \tag{4.2}$$

Where $c_{pk}$ is the peak voltage of the carrier waveform and $\delta$ is the duty cycle for the inverter. If a digital modulator is assumed, this can still be modelled in continuous-time by way of a delay approximation, such as the Padé approximation. Then, the duty-cycle functions as an input for the inverter and load plant, $G_s$. The transfer function of this part depends heavily on the type of inverter modelling and the type of load connected. The inverter could be modelled as simply as a static gain multiplied by the duty cycle, or could be as complex as a complete simulation of the switches and other behaviour. For control modelling, the former is usually taken, as a full simulation of a switched-mode converter requires significant computation, and if the converter switching frequency is far away from the controller frequency, its impact should be minimised. If specific electrical dynamics may disturb the control loop, they can also be modelled and added as a disturbance later on.

Finally, the output load current needs to be measured and used to generate an error reference for the controller, which is typically achieved with a transconductance amplifier, often in the form of a current sensor. It is possible to realise a continuous-time system with the help of dedicated PWM ICs and op-amps to act as PI controllers, but this makes tuning and adapting to changes labour-intensive and more time-consuming. It also does not allow more complicated control laws, like state-space control, to be easily incorporated.

To develop a digital controller, two strategies are possible. One approach is to design a controller in continuous time and then discretise it into the digital domain, revalidating the design. The second option is to start from a digital perspective by creating a discrete-time model, such as a state-space model. The second

method enables certain types of regulators that are not synthesizable in the analogue domain, such as predictive control or LQR-regulators [51]. It should also be noted that even a fully digital controller still has to interface with the continuous-time world. This means that data acquisition must convert continuous data from the plant into discrete data for the controller and vice versa. For this project, the focus is not on research into control design for multilevel converters, but the purpose of the controller is limited to basic functionality. If time permits, various control strategies can be explored to enhance stability or performance. Therefore, the focus will be on the first and most straightforward method of discretising a continuous-time system.

### 4.1.2 Conversion to the digital domain

As mentioned, a digital controller interfaces with the non-digital world. Therefore, it makes sense to digitise only what is strictly necessary to start with and work up from there. One of the key factors in this process is converting the output control variable into the digital domain. To do this, a sensor's continuous output signal is sampled and converted to a discrete signal by an ADC. This can be modelled by an ideal sampler, like a first-order hold, and a quantiser. The quantiser converts the sampled value into a discrete value in a range of $2^n$-bits, which can be expressed as:

$$(N - 1/2)\text{LSB} < x < (N + 1/2)\text{LSB}, \tag{4.3}$$

where LSB is the least significant bit, or the smallest quantisation step the ADC can reach, $x$ is the input, and $N$ is the number of bits. The LSB can be expressed as:

$$\text{LSB} = \frac{\text{FSR}}{2^n}. \tag{4.4}$$

Where $FSR$ is the full-scale input range of an ADC, or the total swing the ADC can achieve, and $n$ is the number of bits in the ADC. As one can imagine, this process introduces an error. This error source can be described by quantisation noise. This is a limiting factor in the performance of ADCs and can be expressed as a probability density with a statistical power of:

$$\sigma^2 = \frac{\text{LSB}^2}{12}. \tag{4.5}$$

This limits the SNR of an ADC to:

$$\text{SNR} = 10log_{10}(\frac{12}{8}2^{2n}) = 6.02n + 1.76 \text{ [dB]}. \tag{4.6}$$

A similar process happens when the digital output voltage is converted into the continuous domain, which will be described later when PWM generation is discussed. With the input digitisation taken care of, the controller needs to be digitised so that it can run on a digital processor, such as a microcontroller or an FPGA.

### 4.1.3 Discretization of PI(D)-controllers

As seen in the previous sections, the PI(D)-controller is based on continuous-time differential equations represented in the Laplace domain. To represent these in the digital domain, a discretisation process must be applied to solve the differential equations for each time step. This can be accomplished using the Z-transform. This transforms the Laplace-domain equations into equivalent versions in the Z-domain, which is the discrete domain equivalent of the Laplace domain. This can be done in several ways, the most popular being the Forward/Backwards Euler and Trapezoidal (Tustin) methods. It should be noted that these are approximates and do introduce a distortion factor[52], but for this use-case this factor can be assumed very limited as long as the $\frac{f_s}{f_c} > 10$ in the case of the Tustin-method, which means that the switching frequency should be at least 10 times higher than the controller bandwidth, which is generally assumed to be the case. This is true especially for flying capacitor inverters where $f_s = f_s(n-1)$. The most used types of discretisation methods are given in Tab. 4.1

Table 4.1: Z-transforms and 3% Distortion Limits [51]

| **Method** | **Z-form** | **3% limit** |
|---|---|---|
| Backward Euler | $s = \frac{z-1}{T_s z}$ | $\frac{f_s}{f} > 20$ |
| Forward Euler | $s = \frac{z-1}{T_s}$ | $\frac{f_s}{f} > 20$ |
| Trapezoidal (Tustin) | $s = \frac{2}{T_s}\frac{z-1}{z+1}$ | $\frac{f_s}{f} > 10$ |

From this table, an example can be made to showcase the use of these transforms. Taking the standard continuous-time PI-controller discussed in the previous section and using the Tustin approach, one can:

$$C_{pi}(s) = K_p + \frac{K_i}{s} \Rightarrow C_{pi}(z) = K_p + \frac{K_i T_s}{2}\frac{(z+1)}{(z-1)} = K_p + \frac{K_i T_s}{2}(\frac{2}{z-1} + 1). \tag{4.7}$$

A parallel implementation of a digital PI-controller can be represented in a block diagram, as seen in Fig. 4.2.

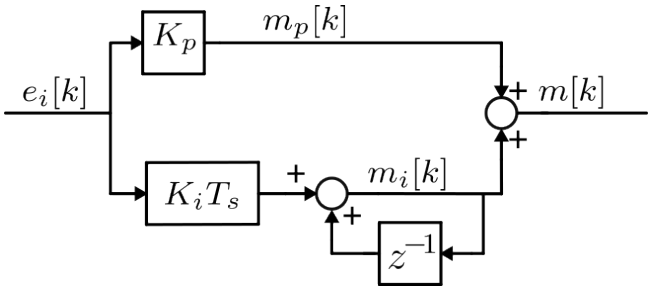



Figure 4.2: Z-domain PI controller

As this equation and block diagram are in the z-domain, the discrete equations can be extracted to form the control laws that could be directly implemented in a microcontroller or DSP:

$$\begin{cases} m_i(k) & = K_i \cdot T_s \cdot \frac{e_i[k]+e_i[k-1]}{2} + m_i[k-1], \\ m(k) & = m_p[k] + m_i[k] = K_p \cdot e_i[k] + m_i[k], \end{cases} \tag{4.8}$$

where $m[k]$ is the required modulation index at time-step $[k]$. This modulation index is then sent to the PWM module. It should be noted that the given equation in this example is assumed to be executed instantly. However, these calculations require multiple processor cycles to finish. Therefore, a computational delay should be added to the output of the block diagram. In general, the simplest model is a $z^{-1}$ delay, equivalent to one time step at the frequency of the control process. This is considered a worst-case situation, meaning that the controller's output is always slightly behind the plant's requirement.

Note that the approach taken here only defines the basics of a digital PI(D)-controller. For instance, integrator wind-up, where the actuating variable saturates but the integrating factor still tries to increase the output, possibly leading to instability [53] , or pre-warping the controller function to account for the distortion caused by the transform, is not yet considered in this case, but could cause problems later on.

## 4.2 Digital PWM generation

One important aspect of the control of power amplifiers is the specifics of the PWM process, which can also be viewed as a conversion from the digital to the analogue domain.

### 4.2.1 Naturally sampled PWM

First, naturally sampled, continuous-time carrier-based PWM can be used as a starting point. This process is illustrated in Fig. 4.3. The modulation signal from the controller is compared to a triangular carrier waveform with a frequency of $f_s$. When the carrier waveform exceeds the modulation signal, the switch is turned off.

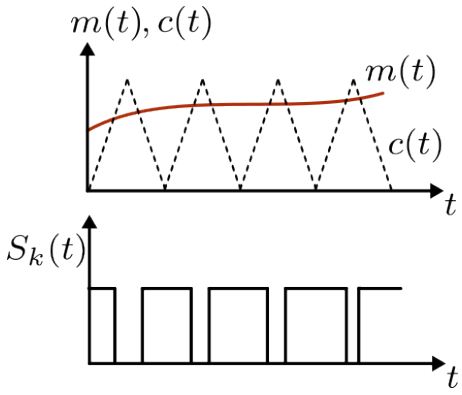



Figure 4.3: Naturally sampled PWM

Here, all signals are in the continuous time analogue domain. Meaning that all changes happen directly, and there is almost no delay between the modulation signal crossing the triangular threshold and the switch changing state. While this is a benefit due to its low distortion, it requires dedicated external hardware, and there is an issue of syncing the clocks of multiple modules together and implementing deadtime. Seeing as the flying capacitor topology requires a significant amount of switches and requires them to be synchronised, this would be difficult to implement.

### 4.2.2 Digital PWM

This same process can be used in the digital domain. Instead of an analogue carrier signal, digital counters, comparators and registers are used to execute the process as seen in Fig. 4.4.

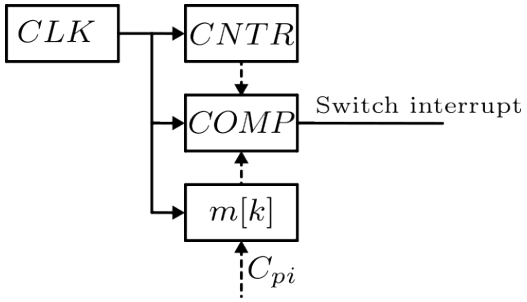



Figure 4.4: Digital PWM blocks

This leads to a similar process as before, but now in a digital system as seen in Fig. 4.5. The distinct difference that can be seen is the static nature of the modulation signal. It can only be updated once for single update mode or twice in the case of double update mode. The update happens at the counter reset for single update mode. For double update mode, an update occurs at a counter reset and when the counter reaches its peak count. This inherently adds a delay that impacts the performance of this digital-to-analogue conversion. Furthermore, the resolution is also limited by the available number of bits.

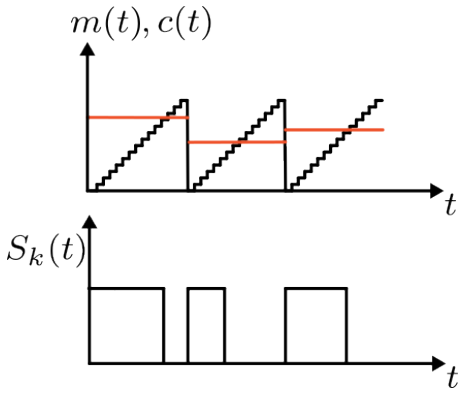



Figure 4.5: trialling-edge, sawtooth-based digital PWM

This limited resolution not only depends on the total number of bits but also on the relation between the clock frequency and the modulation frequency, as can be seen by the following equation[51] dictating the effective number of bits:

$$N_e = \text{floor}[\frac{log_{10}(\frac{f_{clk}}{f_s})}{log_{10}(2)}]. \tag{4.9}$$

Here, floor gives the integer part of the inner argument, $f_{clk}$ is the clock frequency of the timing logic, and $f_s$ is the desired switching frequency. From this, it becomes clear that when the desired switching cycle is very short, the effective number of bits becomes lower. This effect can be lessened by increasing the clock frequency further.

### 4.2.3 Modelling D-PWM modulator delay

The most important takeaway from this description is the delay introduced by the digital PWM process, known as modulation delay. Given that the required effective switching frequency and control frequency will be high, this is an important parameter to consider, as it can significantly limit the controller's performance [54]. It is therefore essential to be able to model these delays to study and mitigate their effect on the control loop.

If it is assumed that the counter and registers used in the digital system have a very high resolution, their effects can be neglected. This is often the case in modern 32-bit controllers. The modulation delay has a more significant impact on the control process, so it will therefore be modelled. With the above assumptions and Fig. 4.5, it is clear that it functions the same as naturally sampled PWM, except for the delay. A Sample and Hold function can thus model this delay, and a Zero-Order Hold can be used to model the digital-to-analogue conversion. This model can be seen in Fig. 4.6

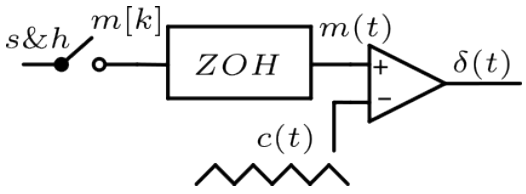



Figure 4.6: modulation delay model

Using this model, a continuous-time transfer function can be derived to feed the continuous-time model of the inverter and load plant described in the previous sections. If the transfer function is derived for Fig. 4.5, the transfer function becomes[51]:

$$PWM(s) = \frac{e^{-s\delta T_s}}{c_{pk}}, \tag{4.10}$$

where $c_{pk}$ is the peak value of the carrier and $\delta$ is the specific duty-cycle. This transfer function can be derived for all other types of carrier-based PWM modulators, like leading-edge and triangular-based. This indicates the orientation and shape of the carrier waveform. This delay has a significant impact on the controllability of an inverter and should therefore be taken into account in the specific design. One way to minimise this problem is by multisampling, or oversampling, [54]. This is especially important for multilevel inverters due to the high

frequency. Later, in the control design, this transfer function can be derived again or modelled for the specific modulator type selected to test the effects of modulator delay.

With the basics of digital control established, these techniques can be applied to multilevel power amplifiers.

## 4.3 Phase shifted PWM

As previously mentioned, to drive a multilevel converter, multiple switches must be driven in a manner that generates distinct output levels. There are various methods for achieving this, including phase-shift PWM, amplitude-shift PWM, and space-vector PWM. The most common method in multilevel converters, such as the flying capacitor converter, is phase-shift PWM due to its relative simplicity and inherent balancing properties. As the name implies, phase-shift PWM is accomplished by generating separate phase-shifted carrier signals. These signals are phase-shifted according to:

$$\phi_k = k\frac{n_{cell}}{2\pi}\ ,\ k = 1, 2..n_{cell}, \tag{4.11}$$

where $k$ is the number of the switching cell and $n_{cell}$ is the total number of switching cells in the multilevel topology. All of these carriers have the same shape and are fed by the same modulator comparison signal to set the output duty cycle. If a steady input modulation signal is given, all the switching cells will have the same duty cycle, but this duty cycle will be realised with a relative phase shift between all the switching cells. This thereby realises all the different switching levels. This method of generating driving signals for the multilevel converter is also relatively simple to implement, as the only aspect that differs from a two-level converter is the phase shift between the modulators.

## 4.4 Multilevel Converter control

While the same basic control building blocks can be used in multilevel power amplifiers, certain distinct specifications and details must be considered. Firstly, various control strategies have been researched in the literature, including state-feedback [55], predictive control [56], and sliding-mode feedback [57]. While these control tactics show great promise and performance, they often have a higher computational cost. This makes it challenging to implement for very high closed-loop frequencies and switching frequencies. Due to the limited scope of this project, these more complicated methods will not be considered further.

The Beat The Heat requirements dictate that the input to the power amplifier is an output voltage, rather than an output current, due to the proposed flux control strategy. Often, a single current control loop can be used, where the input signal is a current reference. In this case, the output voltage must be controlled. As this power amplifier is not only designed to be used with the Beat The Heat project, but also possibly with other actuators, flexibility is needed. Therefore, a cascaded control strategy is required. This means that multiple control loops are employed to stabilise the power electronics and control the outputs.

An analysis of control strategies for both voltage and current output control is presented in [58] and [59], utilising both feedforward and different levels of feedback loops. The most successful strategy achieved a large signal bandwidth of 100 kHz and a small signal bandwidth of 427 kHz at full load. The current control strategy achieved a large signal bandwidth of 17 kHz and a small signal bandwidth of 89 kHz.

Outside of a proper cascaded multi-loop control structure, a way to increase bandwidth could be required. This can be done by a form of linear predictive control, where the control model is defined by the calculated system delays and a very simple transfer function, which constitutes a difference equation, is derived [60]:

$$G_{pred}(z) = \frac{i_{pred}}{i_{avg}} = x - yz^{-1}. \tag{4.12}$$

The constants $x$ and $y$ arise from the calculated time delays and are used to predict the required current setpoint. A method to derive these constants is also given in [60]. This value then gets used in a feedforward. This step is computationally nearly negligible compared to the total time delay if no compensation is used. The results of this increase the stability and minimise overshoot.

Another way to minimise the effects of modulation delay is to change the PWM strategy. When phase-shift PWM (PS-PWM) is used, the nature of the carrier signals, phase-shifted by $\frac{\pi}{n_{cell}}$, means that a switch can only update once per carrier event. Therefore, the multilevel modulator cannot update directly to a change in the required duty cycle, but has a minimum delay of $T_{sw}$, and each cell has a delay of $\frac{T_{sw}}{n_{cell}}$. This limits the control bandwidth. A way to minimise the effects of this, [61] proposes a multirate modulator. This modulator allows the duty cycle of every cell to be updated on each carrier event, instead of its own. This shortens the

delay and allows for higher maximum bandwidth. It also protects the system from overswitching through a protection algorithm. Overswitching occurs when the state of the switch is changed multiple times per carrier cycle, which can significantly increase switching losses and can lead to device failure. This solution also has a very low computational cost, as it utilises a simple algorithm with a minimal number of steps.

# 5 Designing an FCML Power Amplifier

This chapter discusses the design of the converter and the LC filter, utilising simulations and other design tools.

## 5.1 Switching level selection

Before any design efforts can be made, it must first be determined how many switching levels are required for the converter. As described previously, increasing the number of switching levels results in an output that more closely resembles the fundamental of the reference input to the converter, thereby reducing the effective voltage seen by each switch. This comes at the cost of more switches, capacitors and auxiliary circuits, thus increasing design complexity. There is no inherent design limit for this project, which would set a limit to the number of levels. However, one of the common microcontrollers used for these projects within the DCE&S group is the TI C2000. These generally have around 12 PWM modulators, 8 of which are easily accessible. This would put the maximum at 9 levels. As a high bandwidth is required and high efficiency is desirable for the amplifier, GaN switches would be beneficial due to their lower losses and higher achievable switching frequencies in a smaller footprint. They can achieve this due to their incredibly low on-state resistance and gate charges. These switches are offered starting from 20V up to 650V. In general, a higher voltage rating means a worse Figure-of-Merit(FOM) and therefore performance [31]. Taking this into account, a trade-off must be made between switch voltage and complexity. First, a general FOM for GaN switches is defined according to [62]:

$$FOM = (Q_{gd} + Q_{oss})R_{ds,on}, \tag{5.1}$$

where $Q_{gd}$ and $Q_{oss}$ are the gate-drain and total output charges, and $R_{ds,on}$ is the typical on-state resistance of the device. This calculation has been performed for various numbers of GaN switches, ranging from 650V down to 100V, from different manufacturers, as shown in Tab. 5.1.

Table 5.1: GaN FOM comparison, lower FOM is better

| **Device** | $Q_{GD}$ | $Q_{\mathbf{oss}}$ | $R_{\mathbf{DS(on)}}$ | **FOM** |
|---|---|---|---|---|
| TI LMG3522 650V 44Arms GaN | 2.9 nC | 100 nC | 43 mΩ | 4.38 |
| TI LMG3100R017 100V 126Arms GaN | 2 nC | 77 nC | 1.7 mΩ | 0.1343 |
| Infineon IGC033S10S1 CoolGaN 100V 76Arms GaN | 2.8 nC | 43 nC | 2.4 mΩ | 0.109 |
| Nexperia GANE3R9-150QBA 150V GaN | 3.5 nC | 130 nC | 3.7 mΩ | 0.49 |
| EPC2307 200V GaN | 2.5 nC | 58 nC | 7.2 mΩ | 0.43 |
| EPC2304 200V GaN | 2 nC | 120 nC | 3.5 mΩ | 0.43 |
| EPC2308 150V GaN | 1 nC | 50 nC | 4.5 mΩ | 0.29 |

From this table, it can be gathered that the increase in voltage rating leads to a worse FOM. The biggest jump can be observed going from 650V to 200V. Therefore, these high-voltage components will no longer be considered, as their voltage rating is also unnecessarily high. It should also be noted that the switches are rated for a certain current at a certain switch voltage. Normally, the maximum voltage rating of the device does not allow the peak current to be conducted, depending on the switching frequency.

With this information, the required number of levels for different blocking voltages can be determined. The output voltage is required to be $V_o = \pm 300$V, and a half-bridge inverter topology will be used. This means the switch blocking voltage for an $N$-number of levels is calculated as:

$$V_{sw} = \frac{2V_o}{N-1}. \tag{5.2}$$

The number of levels required for a certain blocking voltage is then:

$$N = \text{ceil}(\frac{2V_o}{V_{sw}} + 1). \tag{5.3}$$

The results from this for $100V, 150V$ and $200V$ are given as:

- 100V : $N = 7$
- 150V : $N = 5$
- 200V : $N = 4$

These would be the required number of levels if the device ratings are taken at face value, but looking in the datasheet for the Safe Operating Area (SOA) of the TI LMG3100R017 reveals that the switch can take a maximum of 5A at that voltage. Which is still enough for this project, but it does not allow for any headroom or error in output regulation. Furthermore, due to flying capacitor voltage swings, the required blocking voltage can increase above the theoretical value calculated before. This means that a safety factor needs to be included. This can either be an extra level or an increase in switch rating.

Increasing the number of levels would mean increasing to 9 levels, as an 8-level topology will result in an asymmetric output waveform. A 9-level topology further increases the hardware design complexity and also the total component cost. Increasing the switch rating is therefore the most natural choice, although this decreases the switch's FOM, but it will stay within the same order of magnitude. The price difference between the switches is also negligible for this application.

Given the slight difference in FOM in the 100V-200V range, the decision is made to design a 7-level flying capacitor converter with either 150V or 200V GaN switches. While a 5-level converter would theoretically suffice for the switch rating, including safety margins, the higher number of levels allows for a higher bandwidth at lower per-cell switching frequencies and could decrease the THD at the output. This means the required LC filter can also be smaller and more compact.

## 5.2 Simulation of FCML Amplifier

With more details of the power amplifier known, further design efforts benefit from simulation to evaluate the impact of design choices and develop control strategies. Due to the nature of the electrical dynamics of the flying capacitors, the system is modelled in the simulation software PLECS.

### 5.2.1 Capacitor balance simulation

To verify the sizing of the flying capacitors, a PLECS-based simulation is made. This simulation can also be used to test the multilevel-modulation scheme for the flying capacitor converter and examine the effects of the LC filter on the voltage dynamics.

While the theoretical capacitor value of a flying capacitor converter can be calculated simply by the difference in charge and voltage per flying capacitor cell, this only takes the steady state into account and no parasitics. The equation is as follows:

$$C_{fc} = \frac{\Delta Q}{\Delta V} = \frac{i_o t_{sw} n_{cell}}{2\delta_c \frac{V_{dc}}{n_{cell}}} = \frac{i_o}{2\delta_c V_{dc} f_{sw}}, \tag{5.4}$$

where $i_o$ is the total output current, $n_{cell}$ is the number of switching cells, and $\delta_c$ is the maximum voltage ripple coefficient. This equation can be used to estimate the minimum amount of required capacitance per cell. This can then be used in the simulation and evaluated.

#### Capacitor simulation design

The simulation model was developed before a decision on the number of levels was made. Therefore, the simulation is set up in a modular way, where the switching cells are made as separate components. The PLECS simulation can be seen in Fig. 5.1.

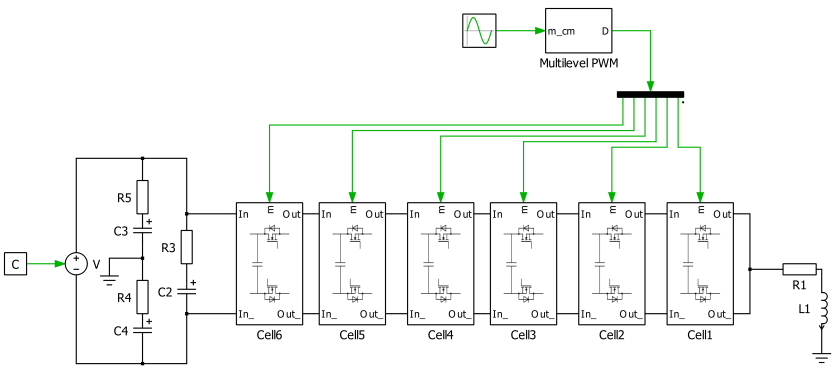



Figure 5.1: FCML PLECS simulation

The inverter is powered by a DC voltage source connected to the DC link capacitor bank. This capacitor bank is divided into two parts. One is an overall DC-link bank, and the other is the split capacitors connected on both sides of the neutral point. These capacitors provide a voltage of $V_{dc}/2$. The load in this case is simplified to a resistance with an inductance in series. The values of these can be adjusted to model different situations. Each of the cells in this simulation has the same internal setup as seen in Fig. 5.2.

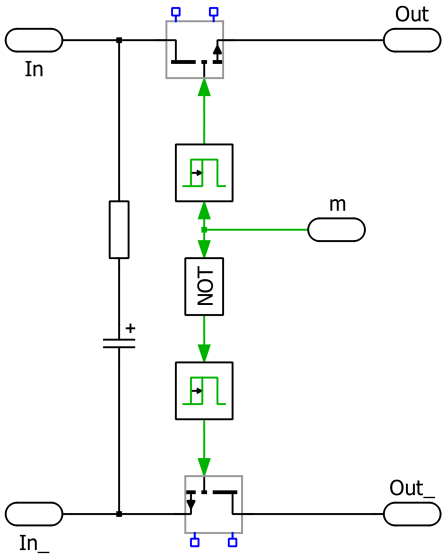



Figure 5.2: Switching cell PLECS simulation

Here, a few important parasitics and variables are modelled. First off, the switches are modelled based on the EPC 2307 GaN [63]. The dead time required for modulation is also included in the gate signalling, as this has an impact on the output quality and the balance of the flying capacitors. Finally, the ESR of the capacitors is also modelled to reflect its effects on the balancing.

Each of these cells has its own parameter set, configured to reflect its position in the topology, such as the capacitor bank voltage and cell numbering.

To drive the switches, phase-shift pulse width modulation is used as discussed previously. For a 7-level converter, six switching cells need to be driven. Therefore, the phase shift required per cell is:

$$\phi_{cell}(k) = k\frac{2\pi}{n_{cell}}, k = 1, 2.. \; n_{cell}. \tag{5.5}$$

Here, $k$ is the cell number. For this 7-level design, the phase shift is 60 degrees between cells. The modulators are double-update triangle wave-based modulators. The structure of this block can be seen in Fig. 5.3.

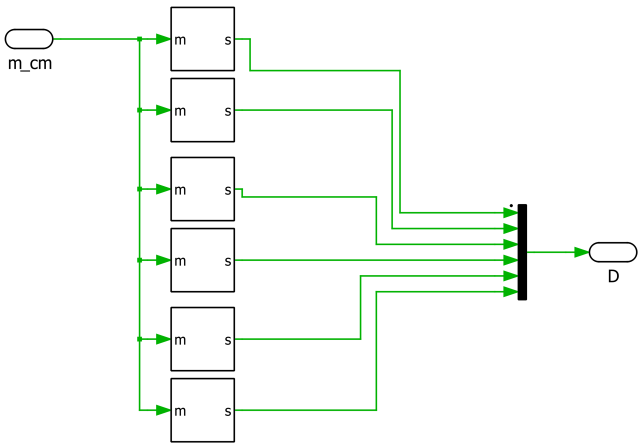



Figure 5.3: Multilevel phase shift modulator

The input of this modulator is the common-mode duty cycle required at the output of the converter. The combined output of the modulator illustrates the stepping between switching levels and how the separate switches can combine to form the multilevel output, as shown in Fig. 5.4.

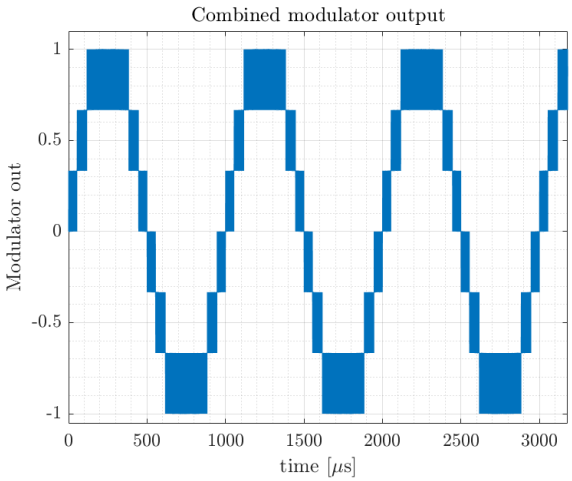



Figure 5.4: Combined modulator output for a sinusoidal input reference of ±300V at a frequency of 1kHz.

The output voltage of the converter should have the same shape as the modulator before being filtered.

### Simulation setup

With the simulation setup complete, it can be used to evaluate the design. To validate the flying capacitor sizing, 5.4 is used with the parameters detailed in Tab. 5.2

Table 5.2: Flying Capacitor design parameters

| Parameter | Value |
|---|---|
| Number of flying capacitor banks, $n_{fc}$ | 5 |
| Output current, $i_o$ | 5 A |
| Cell switching frequency, $f_{sw}$ | 120 kHz |
| Capacitor voltage ripple, $\delta_{Vc}$ | 1.667 % |
| DC-bus voltage, $V_{DC}$ | 600 V |
| Dead time, $t_d$ | 100ns |

The allowable voltage ripple of 1.667% will lead to a ripple of 10V at maximum output voltage and current. This calculation can be seen as a worst-case. This leads to a capacitance large enough to handle this worst-case situation. This voltage ripple will lead to a maximum switch stress of:

$$V_{sw,max} = \frac{V_{dc}}{n_{cell}} + \Delta V_c. \tag{5.6}$$

This design would allow a maximum switch voltage of 110V, thus providing 80V of headroom to the maximum 200V switch blocking voltage. Using these parameters, a worst-case capacitance of 2.08$\mu$F is calculated. For the simulation, this value is rounded off to 2.2 $\mu$F, as it conforms to the standard E-12 series in which components are often produced. The dead time is chosen conservatively at 100ns, so that the effects it has on the circuit are more pronounced. Note that this is relatively high for GaN, and could in theory be as low as 10ns, which could in theory increase efficiency [16]. The input command will be a sine wave with a variable frequency and maximum output voltage. The load will be a resistive load with a resistance of 60 Ω and a varying inductance.

### Capacitor balance simulation Results

With the simulation setup defined, the simulation results can be discussed. In Fig. 5.5, an example of the output can be seen. In this figure, it becomes clear that, even at full load, the capacitor voltage balance with a resistive load only has a peak ripple of $\Delta V_c \approx 3$V.

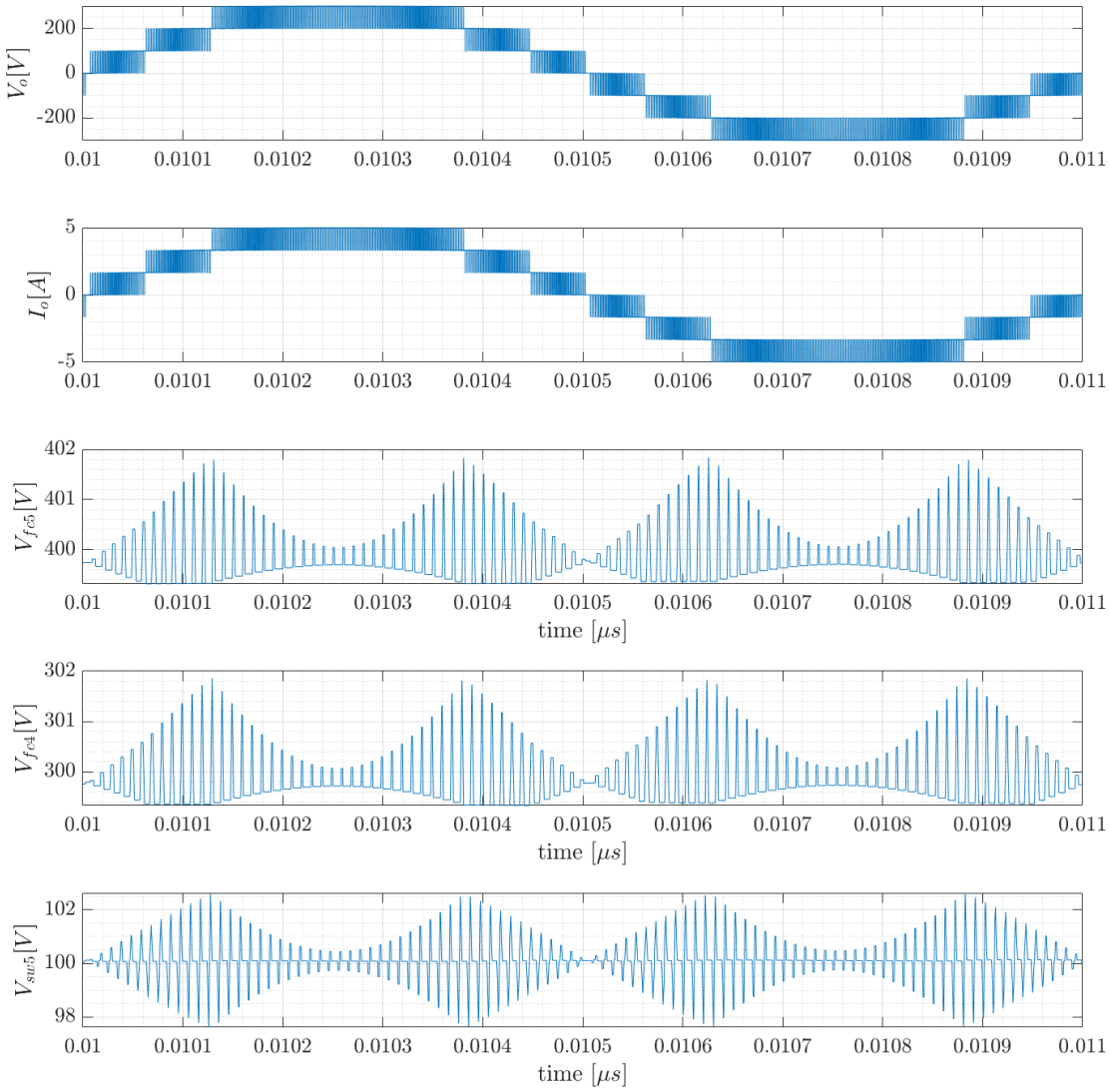



Figure 5.5: PLECS simulation output showing the output voltage and current at full load, the voltage balance of the 5th and 4th capacitor and the voltage across the switch between the capacitor cells at an input frequency of 1kHz and a purely resistive load.

From the figure, one can see the voltage output steps as expected from the modulator's output. The maximum peak to peak ripple of the capacitors translates into an increase in switch voltage as well, where $\Delta V_{sw} \approx 2\Delta V_c$, however the peak stress is not double the capacitor voltage ripple as the switch voltage is the subtraction of the adjacent capacitor voltages and the capacitor ripples are not in phase with each other due to the phase-shift PWM. Therefore, the resulting switch stress has a peak of 102V for the given ripple. All of these results are well within the design limit of $\Delta V_c = 10$V. While one could argue that the capacitors could therefore be smaller, which would result in a larger ripple, but still within the design limit, it should be noted that not all losses and parasitics are taken into account. It may also be required that the converter be able to output higher currents for short periods to magnetise the tunable actuator. Furthermore, the effects of the LC filter have not been taken into account either. Therefore, this capacitance value will be used as a basis for further simulations and can be reevaluated once all other components are designed.

### 5.2.2 Closed-loop control model

While the capacitor voltage model could, in theory, be used for closed-loop control simulations, there is a trade-off to be considered between simulation accuracy and performance. Simulating 1 millisecond using the previous model takes approximately 10-20 seconds, depending on the specific settings. For evaluating control models, it can be beneficial to simulate longer time frames to assess long-term stability or to identify oscillations. Therefore, a more performance optimised model is developed to speed up the design process. To do this, the capacitors and switch models are removed and replaced with a simple gain. The multilevel modulator is used to simulate the effects of the switching behaviour on the LC filter. This leads to the PLECS model seen in Fig. 5.6.

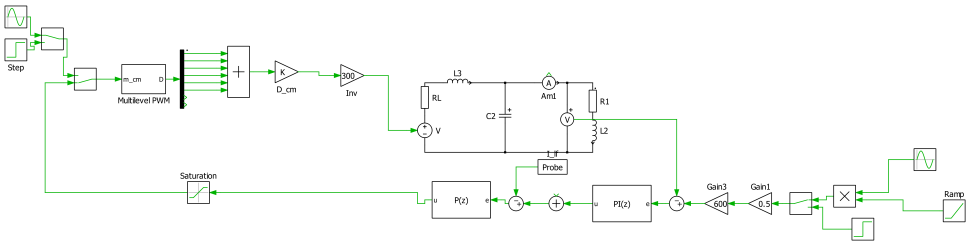



Figure 5.6: PLECS control model

In this control model, a multi-loop control scheme as described in [58], [64] is implemented. The controllers are implemented as discrete-time controllers using the PLECS library blocks. Since the control on the hardware prototype will be executed on a microcontroller, the controls should be verified by simulation in the discrete domain.

## 5.3 Output LC-filter design

An essential part of any power amplifier is its output quality. To ensure this quality consistently meets the requirements, a filter is often used. High effective switching frequencies will be used. Therefore, a single-stage LC filter should suffice, as it is a second-order filter that generates $-40$dB per decade of damping. The transfer function of this filter can also be defined as:

$$H_{LC}(s) = \frac{V_o}{V_{in}} = \frac{\frac{1}{LC}}{s^2 + s\frac{R}{L} + \frac{1}{LC}}. \tag{5.7}$$

From this equation, it becomes clear that there is a resonance point in the filter, which is damped by the resistance $R$. This resonance limits the output frequency. The corner frequency of a single-stage LC filter is defined as:

$$f_c = \frac{1}{2\pi\sqrt{LC}}. \tag{5.8}$$

While the cutoff frequency is one variable in designing an LC filter, the filter's performance is influenced by several additional variables.

Therefore, a design space will be generated according to the boundary values of the performance variables, as discussed in [39] and [65]. Using this design space, viable parameters for the filter components can be chosen and tested in simulation.

### 5.3.1 Generating a LC-filter design space

To define a design space, the following parameters will be considered:

- Corner frequency and maximum output frequency
- Output voltage ripple
- Inductor current ripple
- Voltage drop due to transient currents

First, the corner frequency requirement can be discussed.

Due to the resonance in an LC-filter, as seen in the transfer-function, it is helpful to define a ratio between the maximum output frequency and the corner/resonance frequency of the filter to prevent the required output frequency from resonating with the filter. Therefore, the filter corner frequency equation is adapted to include an additional scaling factor to shift the resonance point away from the maximum output frequency the filter needs to handle. The LC product can then be defined as [65]:

$$LC \leq \frac{1}{(2\pi k_f f_{o,max})^2}, \; k_f = \frac{f_c}{f_{o,max}}. \tag{5.9}$$

Where $f_{o,max}$ is the highest output frequency and $f_c$ is the corner frequency. This inequality will produce a parabola which limits the maximum values of L and C.

The next parameter is the voltage ripple at the output. This parameter ensures a minimum quality of output voltage. This can be modelled by assuming the changing capacitor voltage does not affect the current through the inductor. Then the capacitor voltage ripple becomes:

$$\Delta V_c / V_{dc} = \frac{1}{32LC(n_s f_{sw})^2}. \tag{5.10}$$

Translating this into an inequality leads to:

$$LC \geq \frac{1}{32\Delta V_c(n_s f_{sw})^2}. \tag{5.11}$$

This also leads to a parabola, which defines a minimum value for the L and C components.

Next, the voltage drop due to a current transient can be defined.

$$L_{min}(C) \leq C(\frac{\Delta V_{drop}}{I_{trans}})^2. \tag{5.12}$$

This equation determines the minimum value of the filter inductor as a function of the filter capacitor, based on the output impedance. This is due to the discrete nature of the controller, which always lags due to the finite calculation delays in digital control. Therefore, the voltage drop due to a transient can, in a first approximation, be a function of the LC elements [65]. Thus, the transient voltage drop can be limited by choosing the LC elements based on the given equation.

Finally, the inductor current ripple can be defined:

$$L \geq \frac{V_o}{4n_s^2 f_{sw} \Delta I_L}. \tag{5.13}$$

This equation gives a minimum value for the inductance based on an allowable current ripple in the filter inductor. This equation can be derived from the standard 2-level inductor current ripple. Here, the multilevel output is taken into account by dividing the output voltage by the number of cells and by using the effective switching frequency, $f_{sw,eff} = n_{cell} f_{sw}$ [33].

The design variables used for the filter can be found in Tab. 5.3.

Table 5.3: LC-filter design variables

| Design variable | Value |
|---|---|
| $n$ | 7 |
| $f_{sw}$ | 100 kHz |
| $f_{o,max}$ | 10 kHz |
| $\Delta V$ | 0.5 % |
| $k_f$ | 8 |
| $\Delta V_{drop}$ | 10 % |
| $I_{trans}$ | 5 A |
| $\Delta I_L$ | 20 % |

All the equations, in combination with the design variables, can be used to generate a design space with several viable combinations highlighted. This result can be found in Fig. 5.7.

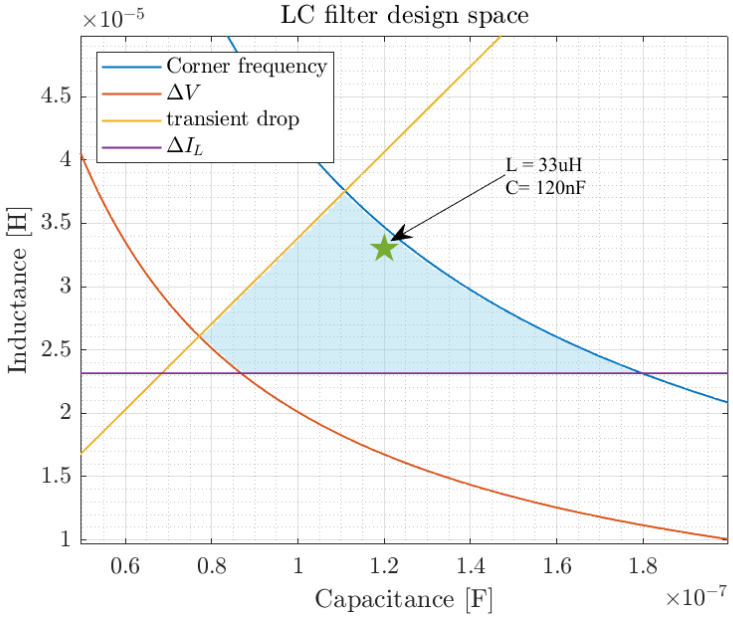



Figure 5.7: LC-filter design space

From this graph, it can be gathered that there is a relatively large area with valid combinations of L and C. A next step could be the implementation of some kind of optimisation algorithm, akin to [65]. However, due to scope and time constraints, the filter combination is determined by hand using the PLECS simulation and by fitting the values to commonly available options from suppliers. This resulted in an LC filter with $C = 120$nF and $L = 33\mu$ H. During the selection of the LC filter values, the capacitor balance was also verified again, this time with the LC filter in place. From these simulations, the capacitor balance once again stayed within the previous design limits of $\pm 10$V and remained roughly at $\Delta V_c \approx 3$V.

## 5.4 Designing a power amplifier controller

The goal for the converter is to utilise it as a power amplifier, capable of tracking a reference using closed-loop control. More specifically, for the Beat The Heat project, voltage control at the output of the filter is required due to the flux control strategy used in that project. These requirements, in combination with the high output bandwidth, mean it would be beneficial to use a multi-loop control strategy as outlined in [64] and [66]. Here, two controllers are used in a cascaded manner. One high-bandwidth inner current control loop, often based on a P-controller and the inductor current, is used to generate a modulator signal for the PWM modulator. The reference used by the current controller is generated based on the output of the outer voltage controller, typically using a PI controller. To increase the bandwidth and reference tracking performance, multiple types of feedforward can be added. The control loop block diagram can be found in Fig. 5.8.

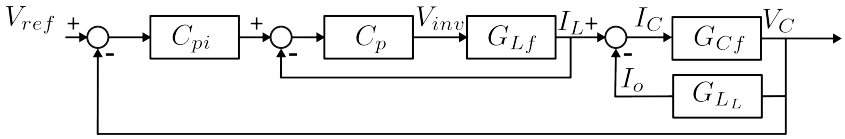



Figure 5.8: Voltage control loop

It should be noted that the modulator has not been taken into account in this control loop to simplify the analytical design; however, it has been implemented in the control simulation in PLECS to verify stability in this manner.

### 5.4.1 Tuning the controller

To get a first basis for the controller parameters, the transfer function of the control loops can be used. First, the inner controller loop must be tuned to have a fast reaction without overshooting or self-oscillation. One tool for this is a Bode plot of the closed-loop transfer function, which can be seen in Fig. 5.9. The inner closed-loop transfer function can be derived as:

$$G_{inner}(s) = \frac{K_p G_{Lf}}{1 + K_p G_{Lf}}. \tag{5.14}$$

Where $G_{Lf}$ is the transfer function from input voltage to inductor current:

$$G_{Lf} = \frac{I_L}{V_{in}} = \frac{1}{L_f s + R_f}. \tag{5.15}$$

Here, $L_f$ is the filter inductance and $R_f$ is the resistance of the inductor.

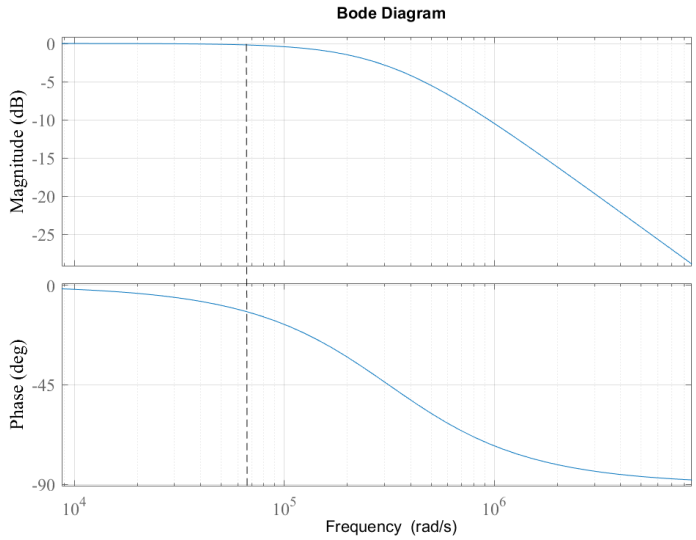



Figure 5.9: Bode plot of inner closed-loop current controller. The current controller gain is set at 0.55. Line indicates 10kHz

From this Bode plot, it can be gathered that the closed-loop bandwidth is beyond the minimum required 10kHz, but also below the effective switching ripple at 600kHz with a bandwidth of 50kHz at -3dB. It should be noted that the plant in this case is a first-order system and is therefore inherently stable. This can also be seen from the closed-loop transfer function, where all the poles are in the left-hand plane and are thus stable as seen in Fig. 5.10.

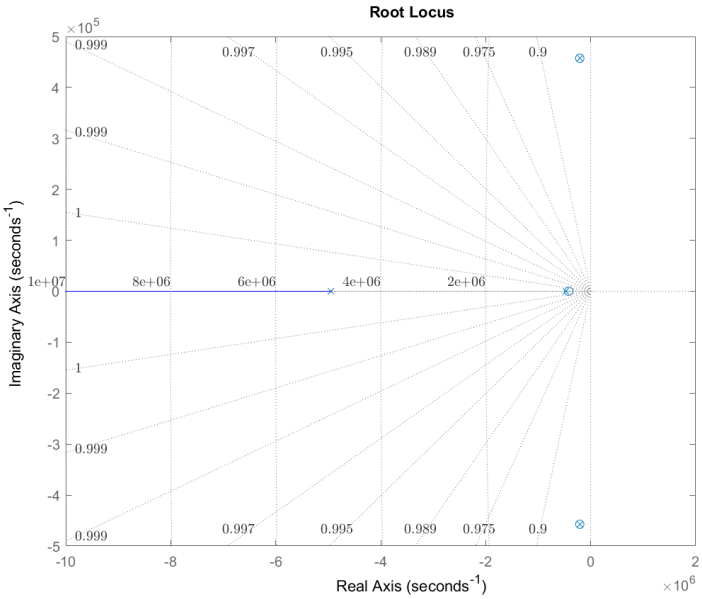



Figure 5.10: Root locus of the inner current controller

With the inner controller tuned, the outer loop can also be tuned. This can be done in the same manner as before, ensuring all the poles lie in the left-hand plane as seen in Fig. 5.11. The final gains can be tuned using the simulation to optimise for performance. The multi-loop transfer function can be derived:

$$G_{o,m} = C_p G_{inner} G_{Vc}, \tag{5.16}$$

where $G_{Vc}$:

$$G_{Vc} = \frac{G_{Cf}}{1 + G_{Cf} G_{LL}}. \tag{5.17}$$

The closed-loop transfer function can then be derived as:

$$G_{cl,m} = \frac{C_{pi} G_{inner} G_{Vc}}{1 + C_{pi} G_{inner} G_{Vc}}. \tag{5.18}$$

These equations can then be used to analyse the control loop.

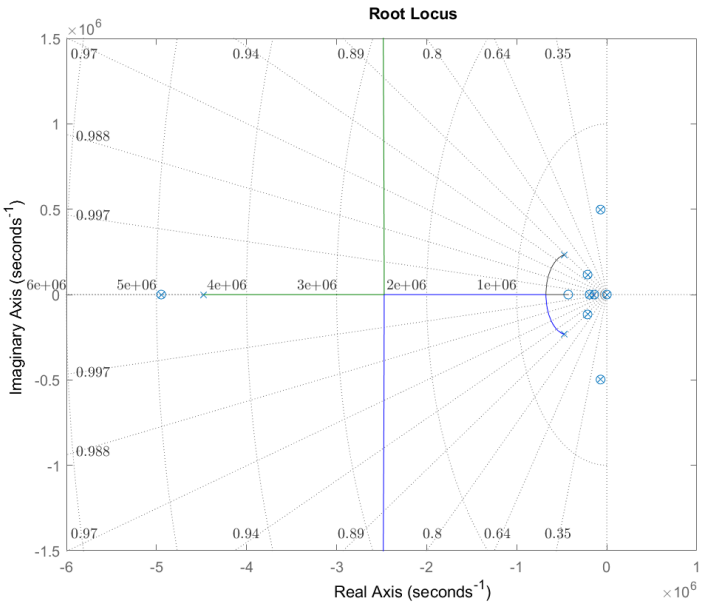


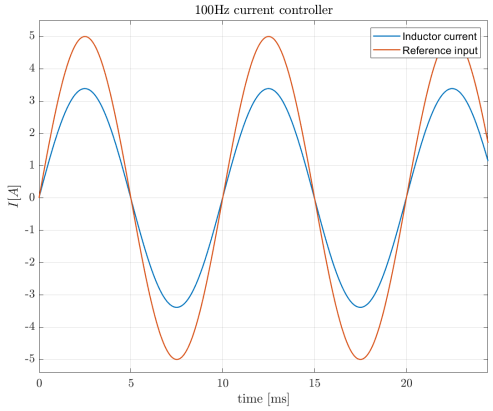

Figure 5.11: Root locus of the multi-loop controller

### 5.4.2 Verifying the controller in simulation

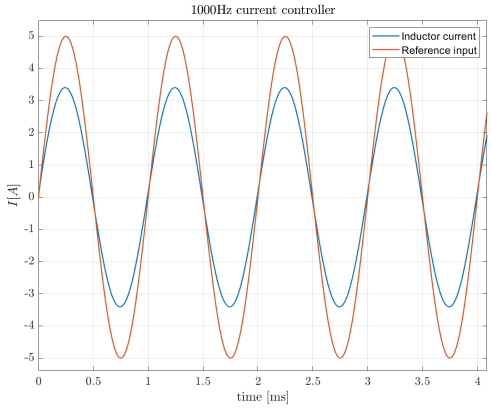
With the first estimate for the controller gains obtained in the previous section, the closed-loop controller can be simulated using PLECS. First, only the inner control loop will be simulated using a current reference as input, and then the whole loop will be simulated. Both configurations will be simulated with and without the multilevel modulator.

#### Inner current controller

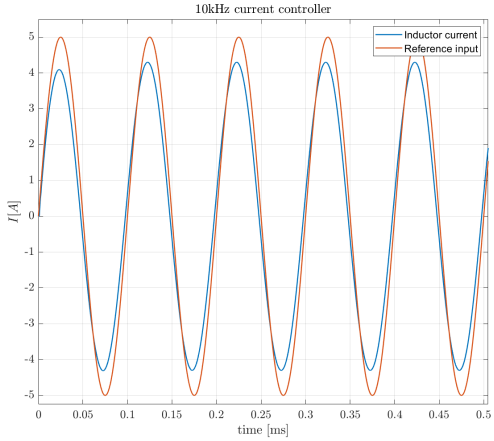
To evaluate the performance of the closed-loop controllers using simulation, the input reference can be compared to the output value for different input types. As the closed-loop full signal bandwidth of the current controller should be 10 kHz, this should be the highest input frequency. The same input is provided for 100Hz, 1kHz, and 10kHz to demonstrate any differences in tracking performance. The results without using a modulator can be seen in Fig. 5.12




(a)



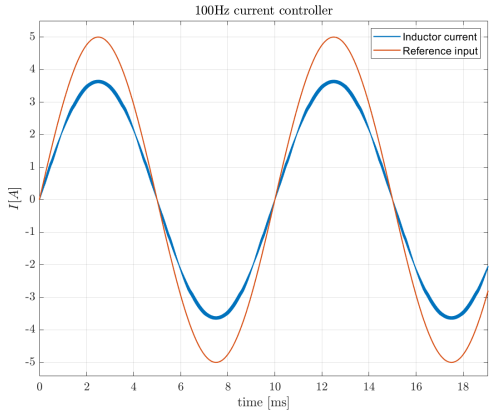

(b)



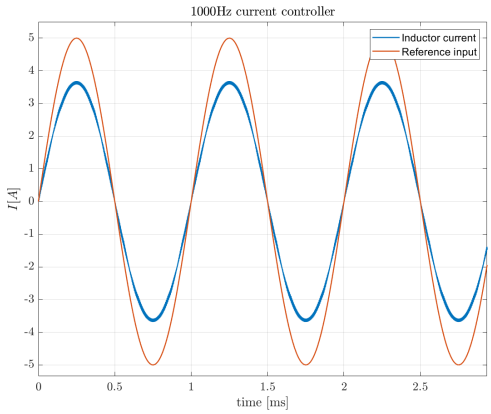

(c)

Figure 5.12: Current controller performance for different input references without multilevel modulator

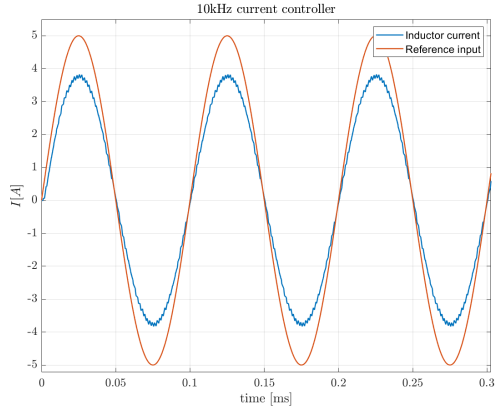
From this figure, it becomes clear that the current controller can track the reference signals but does not achieve the correct amplitude. This is to be expected from a P-controller. It cannot integrate the steady-state error to completely match the input. What should also be noted is the lack of ripple in the inductor current. This is due to the lack of switching emulation. If the modulator is added, a ripple in the inductor current is expected, as shown in Fig. 5.13.




(a)




(b)



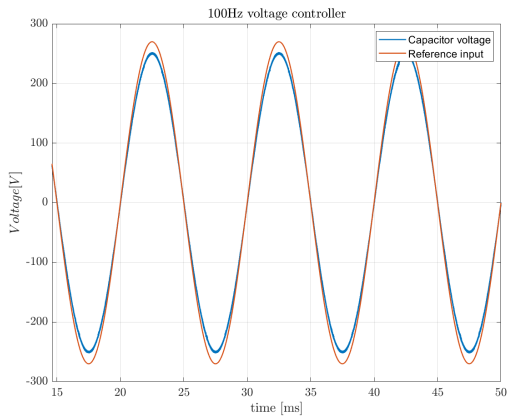

(c)

Figure 5.13: Current controller performance for different input references with multilevel modulator

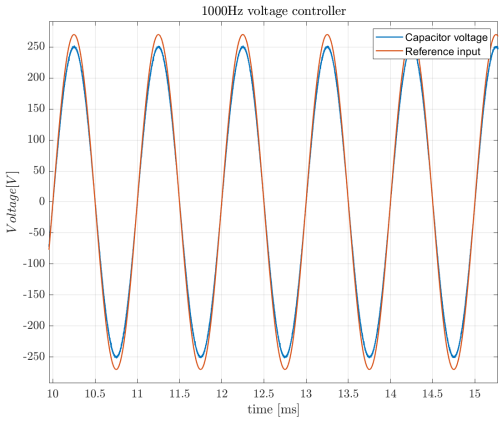
From this figure, it becomes clear that the current control is stable both with and without the modulator, but does have an offset. This offset can be compensated using feedforward. The current controller shows good tracking performance across all frequencies when the load is purely resistive. When an inductive load is simulated, the maximum frequency is limited by the load inductance, as it is an RL circuit, but the tracking performance remains the same.

### Outer voltage controller

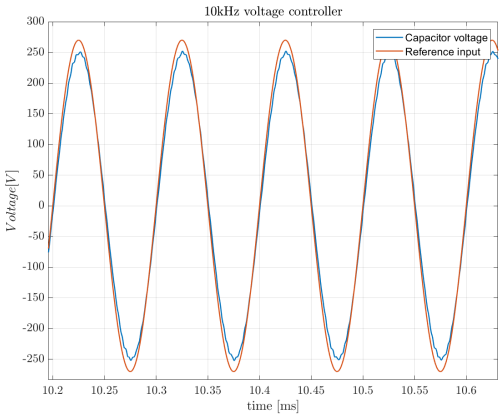
The same set of inputs will be used for the voltage controller, but since the effects of the modulator have been shown, all further simulations will be with the effects of the modulator included. The output of the simulation can be seen in Fig. 5.14.




(a)




(b)




(c)

Figure 5.14: Voltage controller performance for different input references with multilevel modulator

From this, it can be seen that the multi-loop controller can track the reference input, albeit with a small steady-state error. To resolve this steady-state error, a feedforward control can be implemented as described in [66] and [58]. A feedforward is, as the name suggests, not another feedback controller, but feeds the reference input forward to the plant or controller. This eliminates the inherent delay in the feedback controllers and can help eliminate steady-state error. This control structure is illustrated in Fig. 5.16.

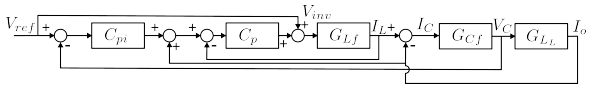



Figure 5.15: New controller structure with feedforward

The results of implementing this can be seen in Fig. 5.16.

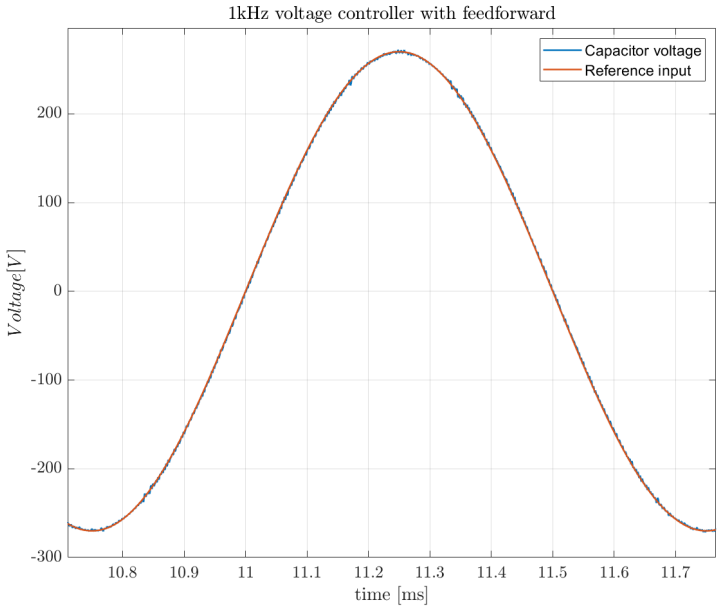



Figure 5.16: Increased tracking performance with feedforwards

From this figure, it is evident that any tracking error is virtually eliminated, and there is no delay between the input and output. The ripple in the output remains unchanged, as the feedforward does not affect the output ripple.

With these simulations, the controllers have been verified to be stable in a simulation based on the most influential system parameters. The real test for the controllers will be implementing them on real-time hardware and tuning the controller to function on there as well.

# 6 Building a FCML Power Amplifier

This chapter discusses the design of the hardware prototype and its realisation. Afterwards, the first measurement results are discussed, along with the issues that were discovered. Then, a redesign is done for a new power stage PCB, and the test results are discussed.

## 6.1 Hardware design

Now that a design has been created, it is time to implement it in a hardware prototype. To achieve this, PCBs will be designed to implement the multilevel flying capacitor switching circuit, as well as the control and sensing, and finally, the LC filter. These can then be produced and assembled, after which they can be used for experimental verification on different types of loads and other input signals. First, the design can be run in open loop, and if that is fully functional, testing can be done to get it working in closed loop.

### 6.1.1 Modular design philosophy

To simplify design and changes, a modular design philosophy is used. All important system functionality is separated into distinct PCBs, which can then be interconnected. The different system components are:

- Motherboard: Houses the microcontroller and some of the sensors needed for closed-loop control. Furthermore, it features high-voltage power connectors and DC-link capacitors, as well as connectors for the other PCBs and output connectors.
- FCML power stage: Has the switches, flying capacitors and the isolated gate drivers for the individual switches.
- LC-filter board: Contains the LC-filter components and the required sensing for the closed-loop control.

All these PCBs will be connected using PCIe edge card connectors. These connectors enable easy swapping of different designs, are available with high power ratings, and are relatively inexpensive. This approach also allows for simpler redesigns of the separate systems. If problems are discovered on one of the boards, it can be redesigned without having to redesign the whole prototype. The design philosophy is evident in Fig. 6.1.

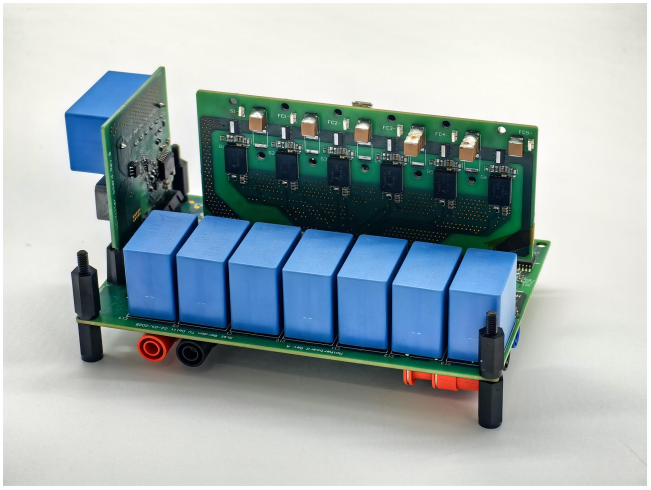


Figure 6.1: FCML converter hardware prototype

In this figure, all the separate PCBs can be seen joined together on the motherboard. The most important components are listed in Tab. 6.1. Some of these component choices will be discussed in detail in the separate sections on the PCBs.

Table 6.1: Important components

| Function | Component choice |
|---|---|
| Switches | EPC2307 200V GaN Fet |
| Flying capacitors | TDK 2.2uF C5750X6S2W225K250KA |
| Gate drive | TI UCC27611DRVT |
| Power and signal isolator | Analog Device ADUM5210CRSZ |
| Microcontroller | TI F28739D |
| DC-link capacitors | TDK B32774X8705K000 |
| Current sensor | Allegro CT415-HSN820MR TMR |
| Voltage sensor | TI AMC3330DWE |
| Filter inductor | Coilcraft 33uH MSS1583-333MED |
| Filter capacitor | TDK 120nF B32656T2124K000 |

### 6.1.2 Power stage PCB

The power stage PCB is a significant component of the system, as it houses both the physical switches and the flying capacitors. Therefore, it needs to be carefully designed to guarantee optimal performance. The PCB can be seen in Fig. 6.2

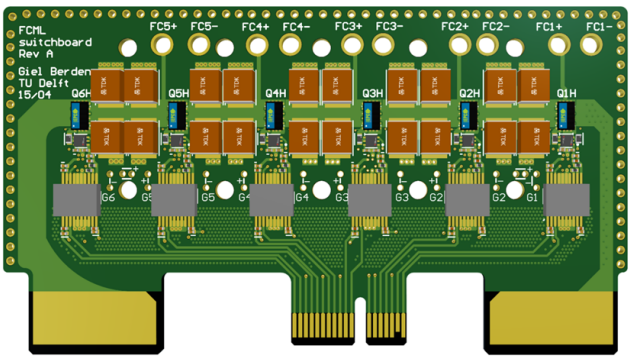



Figure 6.2: power stage PCB

The PCB is mirrored on the other side. One side features the low-side switches, and the other side features the high-side switches. This is done to keep the PCB as compact as possible. The PCB consists of 6 layers, where the inner layers can be used for proper shielding between the isolated grounds on opposite sides of the PCB, while still allowing for significant ground pours to ensure a proper current return path and minimise parasitics.

#### Gate driver circuit design

One difficulty with the power stage design is the floating source potentials in the switches, which are comparable to the high-side switch of a normal half-bridge, except that they apply to both the low-side and high-side floating switches. While there is a way to avoid isolated gate driving per switch, as described in [62], by using cascaded bootstrap drives, this approach also comes with its complications and drawbacks. As cost or component count is not a leading factor in the design, the choice is made to use an isolated gate driver per switch. This consists of an isolated power supply, which is also capable of providing signal isolation for the PWM input from the controller to the gate drive. Each isolator is connected to one switch. The power isolator was selected to be able to supply enough current to the gate drive, determined by the worst-case average switching current for the GaN fet, which can be estimated using the gate charge and the switching frequency:

$$i_{avg} = f_{sw} Q_g. \tag{6.1}$$

According to the datasheet of the EPC2307[63], the worst-case gate charge is 12.3nC. The highest switching frequency within the scope of this design is 200kHz. Therefore, the worst-case average current is only 2mA due to the extremely low gate charge of the GaN technology. This exact specification enables GaN to achieve a very high switching frequency and low switching loss. The power isolators can output a maximum of 30mA, which,

with proper bypassing and decoupling capacitors for both the isolators and the gate drive IC, should present no power supply limitation, even when the quiescent current of the driver is taken into account.

One major concern with driving GaN switches is the small difference between the absolute maximum gate-source voltage and the ideal turn-on voltage. For the EPC2307, $V_{gs,max} = 6\text{V}$ and $V_{gs,on} = 5\text{V}$. Therefore, care must be taken to minimise the parasitic inductance of the gate drive layout as much as possible to prevent ringing and overshoot of the absolute maximum rating. However, research on the reliability of EPC GaN FETs has shown that limited overshoot of the gate voltage does not necessarily lead to instant failure, but will lead to degraded performance and failure over longer periods [67]. Overvoltage is not the only concern when designing the gate drive circuit. A far more impactful problem is the unintended turn-on and turn-off of the switch due to $\mathrm{d}V/\mathrm{d}t$, $\mathrm{d}I/\mathrm{d}t$, combined with an unoptimised common source inductance [62]. Due to the low gate charge, the switches can turn on very quickly, but this also means that they can achieve very high voltage and current slew rates. One way to slow these down is to increase the gate drive resistance at the gate using an external resistor. In the design, this is implemented to allow for changing the gate resistance later during testing.

To minimise parasitics, small components and short traces are used, combined with proper coupling to the isolated ground plane, which is connected to the source of each switch. This ensures a short path to the source and limits the common source inductance.

#### Capacitor bank design

The second important part of this PCB is the flying capacitors themselves. To increase the power density and keep the PCB as compact as possible, ceramic capacitors are used. Electrolytic capacitors are not suitable due to their polarised nature. While film capacitors would be an option, they are generally larger for a given capacitance and are less flexible regarding component layout. Furthermore, the equivalent series inductance (ESL) of these capacitors can be significantly larger due to the longer leads used to connect the capacitors, which increases the length of the current loop. There are some challenges with using ceramics. They suffer from significant DC-bias capacitance derating and are generally not available in high voltage packages compared to film capacitors due to the dielectrics used [68]. Therefore, parallel and series-connected capacitors will need to be used to achieve the voltage and capacitance rating. For instance, the capacitors used are rated for 450V at 2.2$\mu$F, but the datasheet reveals that at 450V, the capacitance is only 390nF. Additionally, the highest voltage capacitor bank has a nominal voltage of 500V. Therefore, series-connected capacitors are required. A script is created to determine the minimum number of capacitors per bank. However, for ease of design, the PCB is designed to accommodate the highest voltage capacitor bank per flying capacitor bank. The capacitor banks consist of four parallel banks of two series-connected capacitors, totalling eight capacitors per bank. This leads to an effective capacitance of 2.48$\mu$F at 500V.

### 6.1.3 Motherboard PCB

The motherboard PCB comprises all the necessary connectors to connect the various boards and the microcontroller. The PCB is shown in Fig. 6.3.

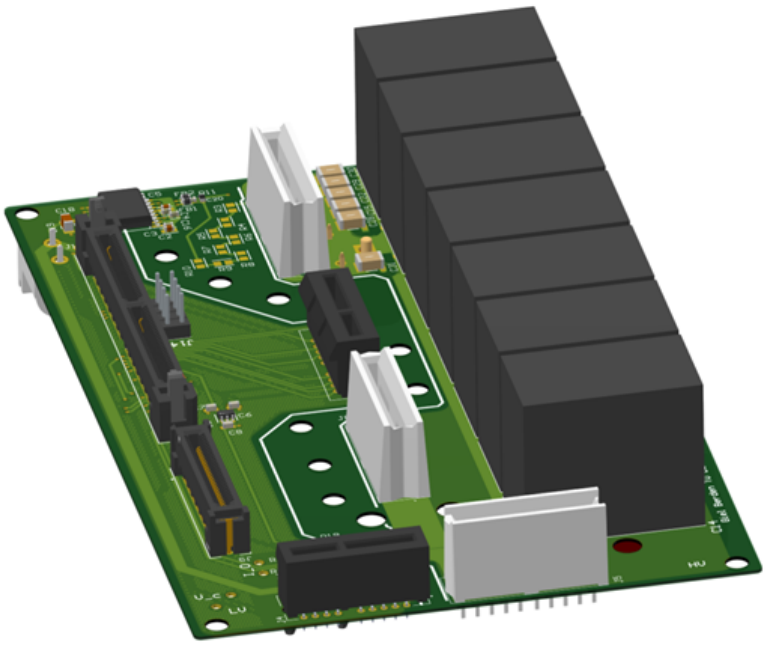


Figure 6.3: Motherboard PCB

As mentioned, the connectors used are PCIE edge card connectors. These are used for both the signal and power connections. Furthermore, the DC-link capacitors are also on this board to provide a stable power supply to the power stage PCB. This capacitor bank is a mix of film capacitors and high-voltage ceramic capacitors.

### Selecting a microcontroller

The controller is also connected through a PCIE connector. The controller used is a TI F28379D on a TI ControlCARD[69]. This is a C2000 series MCU operating at 200 MHz. This controller is chosen due to its 12 PWM modules, with 24 PWM pins in total, which theoretically allows for a 13-level multilevel converter to be driven by a single microcontroller, but only 8 modules are easily accessible. This is enough for the 7-level converter. These modules have built-in options to phase shift all PWM modules internally, which is required for the multilevel converter. In addition to the PWM modules, this controller features other useful modules, including 4 16-bit ADCs that can be multiplexed to 4 pin pairs. It also features a separate processor designed for running control logic, called the Control Law Accelerator (CLA).

### Closed-loop sensor circuit design

To achieve closed-loop control, the control variables must be known; therefore, some sensors are necessary—both the current and the voltage need to be sensed. The voltage is sensed using a high-voltage resistive divider. The output of this divider will then be measured using an isolated op-amp to provide the necessary isolation between the high-voltage path and the low-voltage path, as well as noise immunity. The voltage at the output and the DC-link voltage will be sensed. To select the correct resistor values, the maximum voltage and current allowable are taken into account. The maximum voltage at the output is ±300V. Therefore, the DC bus is at 600V. For safety, 75V is taken as the maximum voltage per resistor. This means that:

$$n_{resistor} = \frac{V_{DC}}{V_{max}} = 8. \tag{6.2}$$

To limit power dissipation in the divider, the maximum current is set at $750\mu$ A. This leads to a resistance of $800k\Omega$, which is rounded off to 1MΩ as a safety factor. This leads to a total resistance of 8MΩ for the upper part of the divider. To calculate the lower resistance value, the peak input voltage range of the op-amp can be used:

$$R_{sense} = \frac{V_{full}}{V_p - V_{full}} R_H = \frac{1.2}{600 - 1.2} 8 \cdot 10^6 \approx 16\text{k}\Omega. \tag{6.3}$$

This same approach can be applied to the output voltage sensor, but the peak voltage can be adjusted to $300V$.

For current sensing, there are many options using various technologies, such as shunt resistors, current transformers, Hall effect sensors, and more. For this project, isolation between the high-voltage current trace and the low-voltage control side is a must. Furthermore, due to the high switching frequency, the output noise immunity is also important. Therefore, an internally isolated sensor with high noise and transient immunity is chosen. The technology used is a tunnelling magnetoresistive (TMR) sensor, which operates based on the change of resistance in a magnetic tunnel junction. When a magnetic field is applied, the magnetic moment in the junction layer changes, affecting the electron tunnelling probability, which leads to a measurable change in resistance[70]. These sensors are relatively new, but they have similar bandwidths and sensitivities in the same package as traditional Hall-effect sensors, at a price comparable to their traditional counterparts. Therefore, one of these sensors is selected. To convert the single-ended output of the sensor to a differential signal so that the 16-bit ADC of the microcontroller can be used, a full differential op-amp with an active multi-feedback filter [71] is designed and implemented to filter the output and convert the signal to a full-range differential signal. This enhances noise immunity and enables higher-order filtering. The circuit diagram of this filter can be seen in Fig. 6.4

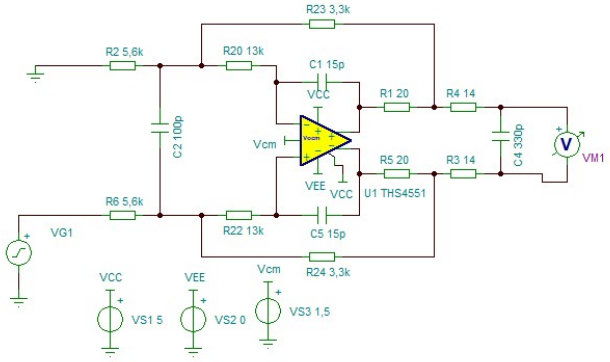



Figure 6.4: Current sensor multi-feedback filter

The gain of this filter is

$$K = -\frac{R_{23}}{R_2}, \tag{6.4}$$

and the transfer function is given as

$$\frac{v_o}{v_i} = \frac{-\frac{1}{C_1 C_2 R_2 R_{20}}}{s^2 + s\frac{1}{C_1}(1/R_{20} + 1/R_2 + 1/R_{23}) + \frac{1}{C_1 C_2 R_{20} R_{23}}} \tag{6.5}$$

Then, an RC filter is added at the input and output to increase the filter performance. The cut-off frequency of this filter is set at 800kHz so that the effective switching frequency ripple at 600kHz can be measured at the inductor. The cut-off frequency is determined by:

$$f_c = \frac{1}{2\pi\sqrt{C_1 C_2 R_{23} R_{20}}}. \tag{6.6}$$

### 6.1.4 LC-filter PCB

The final PCB in the hardware prototype is the LC filter. This PCB is relatively simple as it contains only the LC-filter elements and the sensors. The PCB can be seen in Fig. 6.5

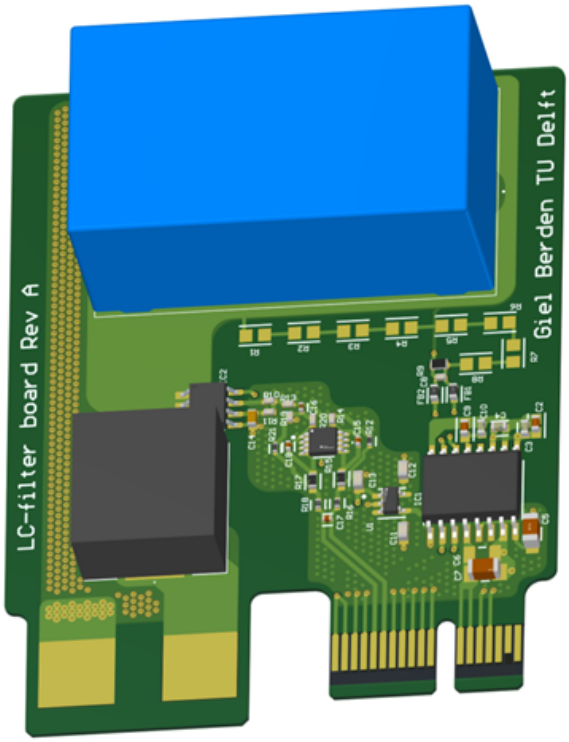



Figure 6.5: LC-filter PCB

The sensors used on this board are the same ones as used on the motherboard PCB. The only real difference is the filter cut-off frequency of the current sensor and the resistor value of the lower branch of the voltage sensor. The PCB is a 4-layer board with separate power and low-voltage grounds. The four layers allow for sizeable ground pours for both grounds, ensuring proper current return paths. The PCIE edgecard signal connector also allows for redundant ground and power input paths to further ensure adequate grounding and facilitates easy connection to the IC's inputs.

### 6.1.5 Heatsink design

As a final part of the design, a heatsink is developed. Due to the design of the switching board, standard heatsinks that are big enough to cool the switches properly, but still fit in the small available area, are not easily available. Therefore, a custom heatsink is designed using CAD and simulated using FEM software. The losses of the switches are estimated using worst-case estimates:

$$P_{loss} = P_{sw} + P_{cond} = 0.5 V_{in} I_D (t_r + t_f) f_{sw} + I_{D,rms}^2 R_{ds,on} = 2.4\text{W} \tag{6.7}$$

The other losses of the switching board should also be taken into account, as these will also increase the temperature of the PCB and the surrounding air. The isolators are at best 10% efficient and can output a maximum of 150mW. Therefore, the loss is taken as 1.5W per device in the worst case.
The design of the heatsink is shown in Fig. 6.6.

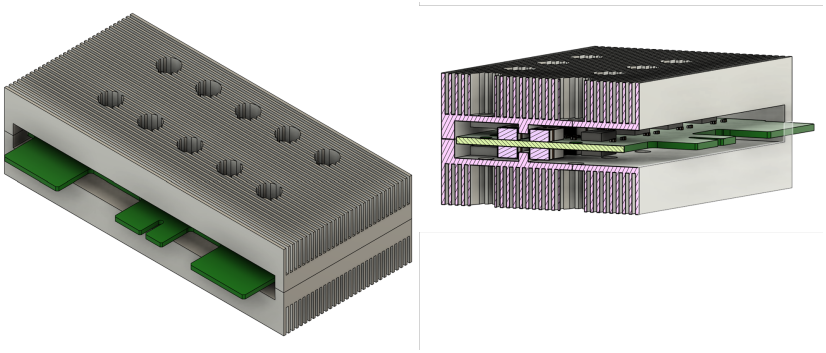


Figure 6.6: Heatsink design

The heatsink features a clamshell design, consisting of two separate halves clamped together with the PCB sandwiched in between. Using this method, the pressure exerted on the PCB can be tuned to ensure proper thermal contact with all components. This design is validated in simulation using a FEM solver. The loss sources are attributed to the separate switches and isolators to accurately model the losses. An interface material between the heatsink and the switches/isolators is also selected, as the case of the switches is connected to the drain of each switch, causing a short circuit if these were to be connected to the heatsink. An isolating gap-filler pad is used, which has a thermal conductivity of 7.8 W/m-K. The heatsink material is set as aluminium 6061, as this is a conventional and cheap material often used for CNC machining. The ambient temperature is set at 40 degrees, and a worst-case switch temperature of 100 degrees is allowed. The results of this FEM analysis can be seen in Fig. 6.7.

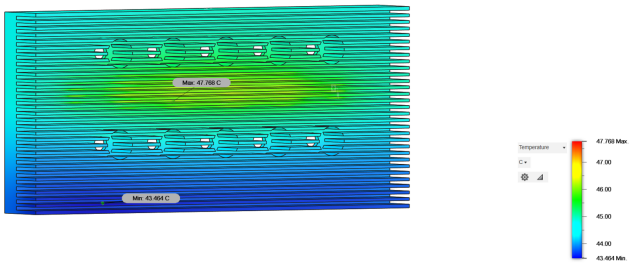



Figure 6.7: FEM simulation output

From this figure, it can be seen that the temperature rise of the heatsink is minimal even under the worst-case heat load. Due to time constraints, this designed heatsink will not be produced. During experimentation, forced-air cooling will be used, and the temperature of the switches will be monitored using a thermal IR gun or a thermal camera.

## 6.2 Software design

With the hardware designed and assembled, software is needed to drive the switches, read out the sensors and execute the closed-loop controller. As described before, a TI C2000 microcontroller is used [69]. This controller will be programmed in the C language using TI's Code Composer Studio. While these microcontrollers can also be programmed in a visual language by using either Simulink or PLECS, using C has increased flexibility and allows for finer control over all modules of the microcontroller. This does come at the cost of higher effort. To better prepare for the software design, flowcharts are made to describe the required functions of the software and the order of execution. In Fig. 6.8, the overall software flow can be seen.

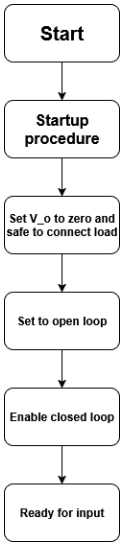



Figure 6.8: Overall software flow

From this flowchart, it is important to highlight the start-up procedure. To start a flying capacitor converter, the capacitors need to be charged to their nominal level. In a laboratory setting, this can be achieved by gradually increasing the input voltage to its nominal voltage. However, if this project is integrated into a more complete product, some sort of start-up procedure is required. The simplest way to do this is to use a bipolar switching pattern at a quarter of the full output voltage [72]. This procedure is again implemented into a flowchart seen in Fig. 6.9.

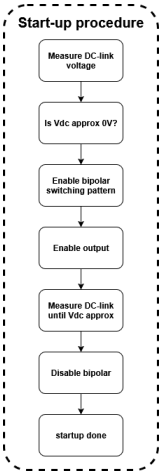



Figure 6.9: Start-up flowchart

This procedure is also implemented in the software, even though it is not strictly required in this laboratory setting.
Finally, the most important part to highlight is the closed loop and the PWM structure. This is done using an interrupt routine. An interrupt routine can be seen as a flag in the software which halts the current process running on the microcontroller and executes the code described in the interrupt request. When this request is completed, the flag is reset, and the processor continues. This means the routine is executed almost immediately and allows for strict and consistent timing of routines. This requires some insight, as setting up multiple routines can cause these strict timing requirements to not be met. These routines can either be triggered by something in the software or in hardware, such as the output of a comparator or clock. In this software design, the interrupt routine triggers a cascade of processes to perform the closed loop. This can be seen in Fig. 6.10.

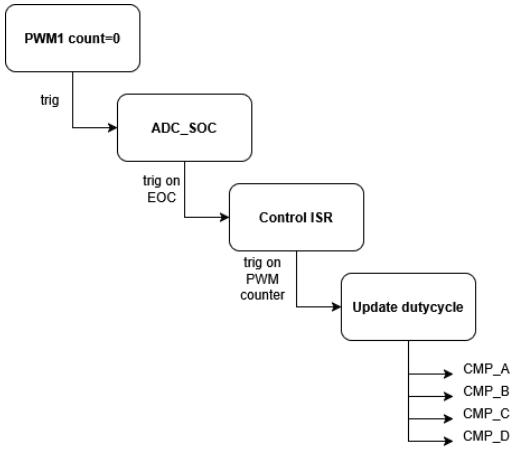



Figure 6.10: Interrupt routine

Here, the interrupt is triggered by the PWM counter reaching 0, which in turn starts a conversion (SOC) on the ADC. When the ADC is done (EOC), the closed-loop control is executed with the new sample as its input. The output of the controller is then used to update the duty cycle of all of the PWM comparators, which then change the switch state of the gate driver. The ADC is configured in differential mode, which allows the full 16-bit range to be used.

The PI-controller is implemented with the help of the TI Digital Control Library [73]. Using this library, a linear PI controller is implemented in Assembly language to maximise performance and execute the control equations in as few clock cycles as possible. This library also enables integrator wind-up protection and pre-warping of the control functions. Furthermore, this controller is not implemented on the main CPU, but on the Control Law Accelerator (CLA) processor. This is a separate processing unit onboard the C2000, designed to execute control laws and manage the sampling process. Direct Memory Access (DMA) is also implemented to retrieve the samples of the ADC directly from memory, minimising any delays from sample to controller. DMA allows certain hardware subsystems, like the CLA, to access the system memory directly without the intervention of the main processor. If this is not used, the processor would be occupied entirely by the data transfer process during the closed-loop process.

## 6.3 First tests and issues

With the PCB designed and assembled, testing can begin. To bring up to converter and discover unknown issues, testing is done in a few steps:

- Low voltage: Ensure all low voltage components are powered and output expected signals.
- Power isolation and gate driving: Ensure all isolators are functional and output the correct voltage and signals on the isolated side. Verify that gate drives are powered, receiving a signal, and driving the gate without any high-voltage power connected.
- Connect high voltage: Connect to high voltage inputs. Starting with low voltage and low power, and increasing gradually while monitoring temperature and other variables.
- High power testing: With the converter working as expected, the output power can be pushed to its rated power for short periods while monitoring the same variables.

First, the switching waveforms of a single half-bridge are measured to verify proper complementary switching with the required dead time. This measurement is illustrated in Fig. 6.11.

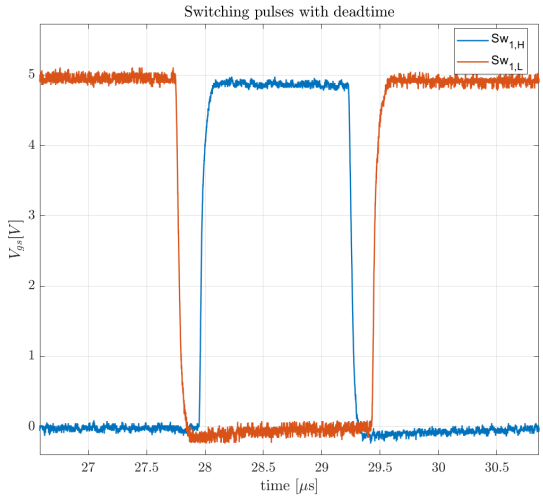
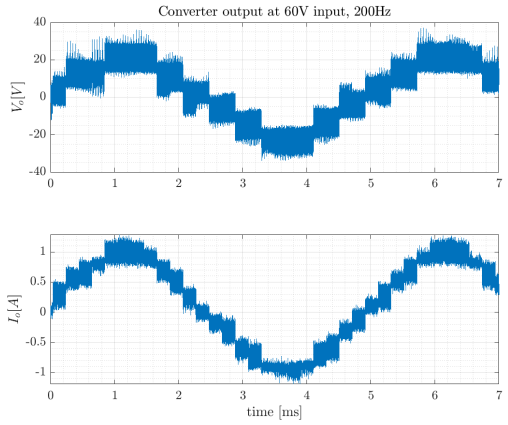



Figure 6.11: Gate voltages of the first upper and lower switches

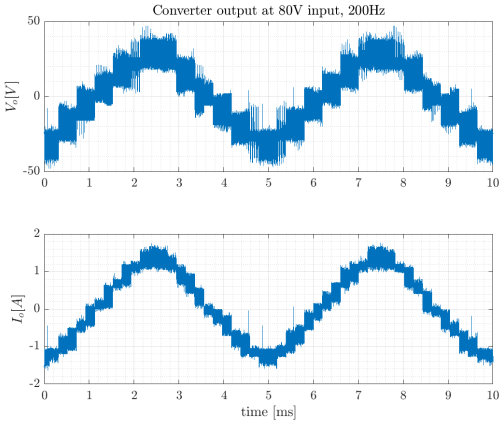
Note that these switching waveforms are generated without high-voltage power and therefore do not exhibit any overshoot or ringing. With the switching waveforms verified, high-voltage input power can be connected. To modulate the converter's output, a function generator is connected to one of the ADCs and used to generate an arbitrary waveform, which serves as the input for the PWM modules on the controller.

### 6.3.1 Low voltage test results

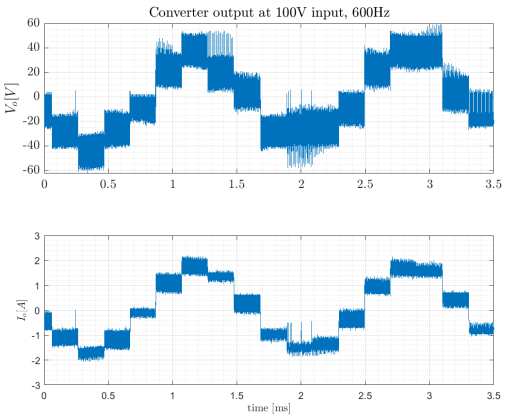
Next, a 20Ω power resistor will be used as a load, and the voltage will be slowly increased from 20V. The input is a sine wave with variable frequency and amplitude. The first results of this can be seen in Fig. 6.12.




(a)



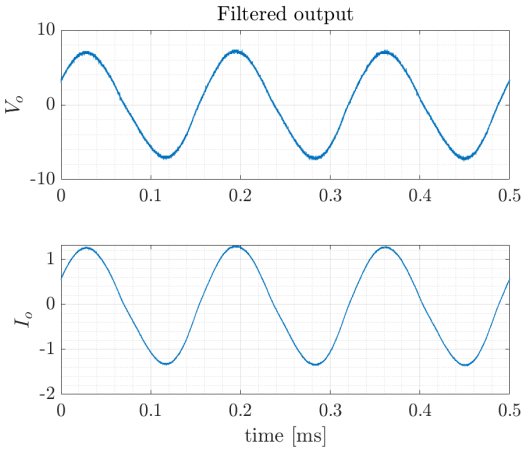

(b)



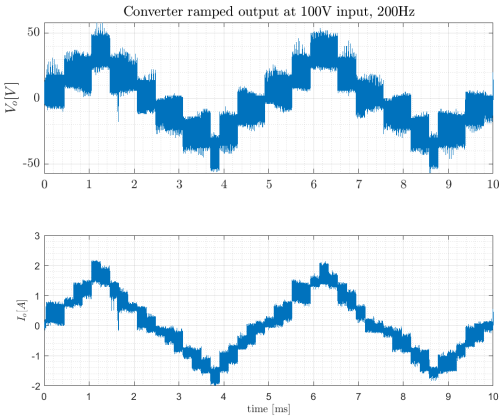

(c)

Figure 6.12: Output waveforms for different input voltages

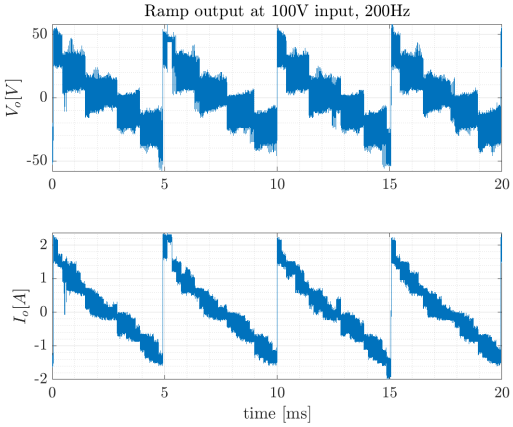
From this figure, it can be seen that at 600Hz input, some aliasing of the ADC starts to occur. Outside of this, the converter accurately follows the input voltage and can generate the seven different output voltage levels using phase-shifted PWM. The principal operation of the flying capacitor multilevel concept has been demonstrated to work for a sine-wave input. In Fig. 6.13, different modulation inputs and the output using a filter can be seen.




(a)




(b)



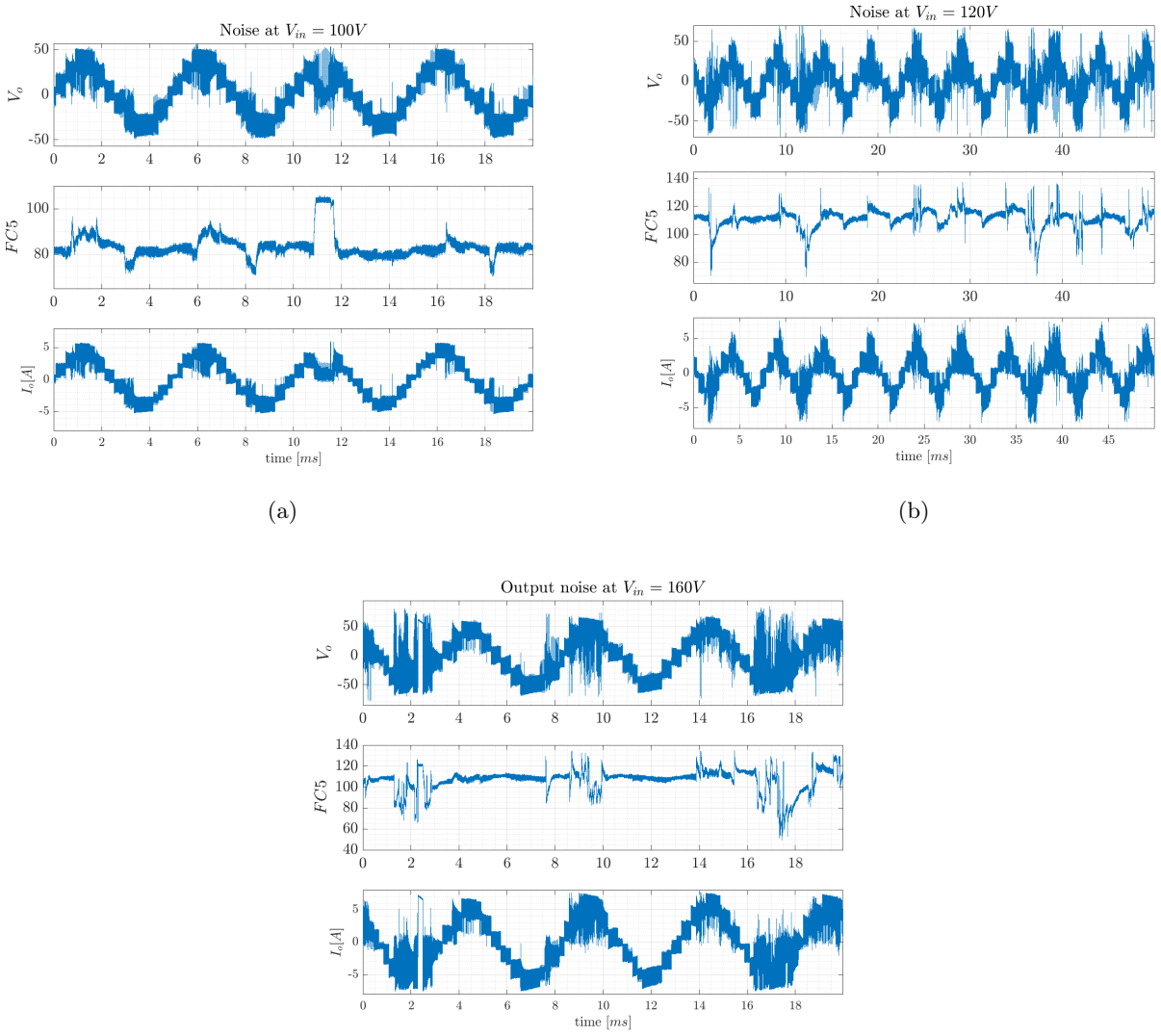

(c)

Figure 6.13: Output waveforms for different modulation inputs and the effects of the LC-filter

From these figures, it is evident that a significant amount of noise is already present in the output voltage, particularly as the output voltage increases.

### 6.3.2 Problems at higher voltage

As indicated in previous sections, the input voltage of the converter has yet to be increased above 100V in the measurements. Unfortunately, when the voltage is increased above 100V, the output becomes increasingly noisy and distorted, as is visible in Fig. 6.14. Outside of electrical measurements, a crackling and arcing noise can be heard, seemingly originating from the power stage PCB.




(a) (b) (c)

Figure 6.14: Noise in the output and unwanted behaviour of the capacitor voltage

From the noisy output, some phenomena can be identified. The noise is primarily detected on the positive peaks and less so on the negative peaks of the output voltage and current. Examining the capacitor voltage, two distinct behaviours can be observed. In Fig. 6.14 (a), the voltage of the capacitor spikes to a peak voltage of 105V, which is 25V higher than the voltage it should be at. Similarly, in Fig. 6.14 (b) and (c), the capacitor voltage drops 45V. This would indicate that the switches are not switching as intended and may not be working as a complementary set. The decrease in capacitor voltage at one node and increase in another could indicate a short-circuit or shoot-through event in the half-bridge, meaning both switches are on at the same time. This could lead to a higher voltage capacitor being connected to a lower voltage one, which would discharge one and charge the other. This matches the behaviour seen in the measurements, which is problematic, as the shoot-through current can become larger than the maximum current and could destroy the switches. Fortunately, the stored energy in the capacitors is relatively low, and the GaN switches used are resilient to short overcurrent events [74], and the rated pulse current of the switches is 130A [63]. Therefore, these events are not yet destructive, but indicate fundamental issues with a part of the design.

This means that testing cannot continue as expected, as the converter cannot be operated at or near its nominal point. To further investigate the underlying issues, the gate voltages can be measured to confirm suspicions that switching events are occurring without the controller sending a gate signal. This data may also indicate the causes of shoot-through or open-circuit events, as observed in the noisy output data. The gate voltage of the high-side switch closest to the output is plotted in Fig. 6.15.

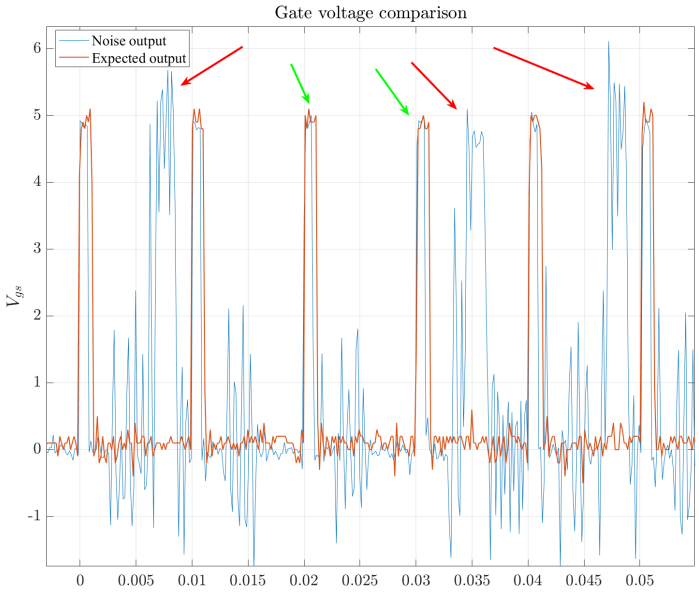



Figure 6.15: Comparison of the gate voltage between the expected output and the measured noisy output. Green arrows indicate correct switching events, and red arrows show unexpected switching events.

From this figure, it becomes clear that there are significant issues regarding switching and noise. There is a considerable amount of noise even when no voltage is applied to the gate, and it can be observed that the switch is turning on when it should not, turning off earlier than it should, or not turning on at all. However, it should also be noted that the gate source voltage, while noisy, is mainly within the maximum rating of the switch at $6V$. This suggests that the problem is not directly related to the gate driver, but rather an issue that occurs before the gate driver and after the power isolator. If the problem were within the layout of the gate driver, one would expect clear ringing around the switching transitions, which is not the case. It could suggest that there is some parasitic coupling between isolated nodes due to common source inductance and fast $\mathrm{d}I/\mathrm{d}t$ switching transitions, injecting noise into other gate driver circuits. Another cause could be complementary turn-on due to high $\mathrm{d}v/\mathrm{d}t$, also known as Miller-induced turn-on. A switch is sensitive to this effect if the ratio between the gate-drain charge and the gate-source charge is larger than one[62]:

$$\frac{Q_{gd}}{Q_{gs}} > 1. \tag{6.8}$$

The Miller ratio of the EPC2307 is 0.34, indicating that it is not sensitive to Miller-induced turn-on and therefore should not cause turn-on issues. Another problem that can be identified from the switching voltages is that the noise on the gate, when the switch is supposed to be off, is above the gate-source threshold voltage. This means the switch is actually turning on partially, but not fully and therefore causes significant dissipative losses. The $R_{ds,on}$ around the gate-source threshold voltage can increase to $20\Omega$[63]. Looking at the same graph, but for the positive half-cycle, the opposite behaviour can be seen in Fig. 6.16.

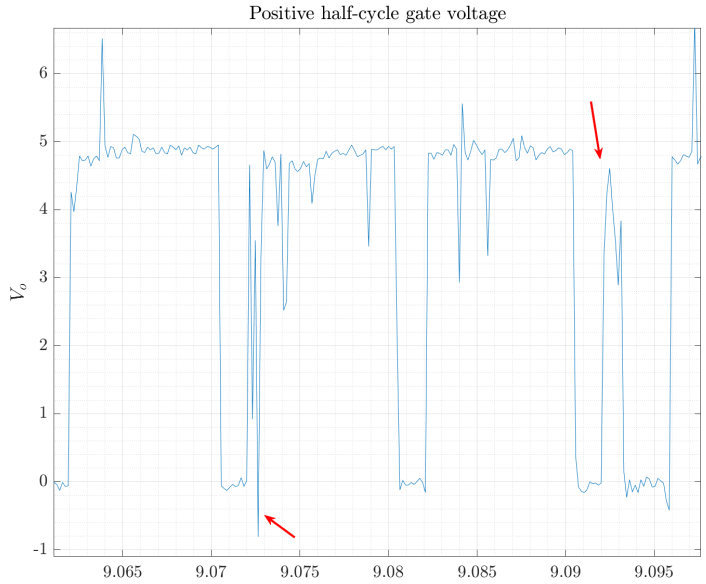



Figure 6.16: Gate source voltage during positive half-cycle noise

Here, the switch turns off when it should be turned on. This likely does not cause serious issues, but it does cause significant distortion in the output and could upset the capacitor voltage balance. It is important to find the root cause of these issues, so they can be addressed and fixed in a new version.

### 6.3.3 Noise and isolation breakdown causes

While it is not possible to precisely identify the source of the arcing sound, as there is no direct damage visible, it is possible to postulate some causes for both the arcing and the noise measured at the gate of the switch. There seem to be significant voltage spikes which correspond in timing with a switch transition of either the opposite side switch or an adjacent switch. This would indicate some form of noise coupling between adjacent circuit nodes. This could be due to high $\mathrm{d}V/\mathrm{d}t$ or $\mathrm{d}I/\mathrm{d}t$ coupling through some common source capacitance or inductance between two adjacent source planes. This noise coupling through to other switching grounds could explain the turn-on and turn-off effects seen in the measurements. The reason this noise can couple through other isolated switching circuits is likely due to the same reason why the arcing sounds can be heard at higher voltages.

When designing the PCB, the layout was optimised for space, and therefore, tolerances between all of the isolated planes were made very small. In the worst case, there was a distance of $< 0.125$mm between two high voltage planes. The voltage difference between these two planes at the rated voltage would be 100V. This layout can be seen in Fig. 6.17.

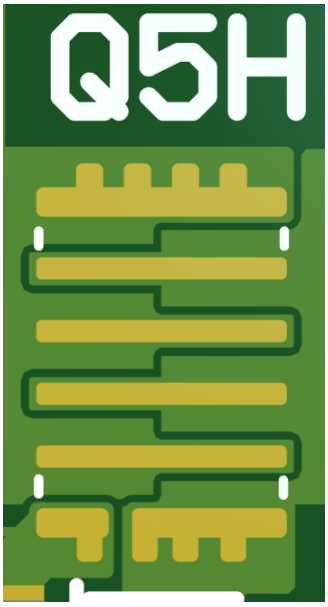



Figure 6.17: PCB component layout and masking

The clearance between the drain and source of this switch is only 0.125mm. In this pursuit of minimisation, too little thought was given to proper high-voltage design based on internationally recognised standards, such as IPC-2221B [75]. This standard states that the minimum spacing between two traces at 100V potential difference on a soldermask-coated trace placed on a fibreglass baseboard should be at least 0.3mm. This is not what was used in the design and could be the reason for the arcing sound. The maximum voltage at the 0.125mm trace spacing is only 40V. Not only is there insufficient space between the high-voltage connection at the drain and source of the switches, but there is also insufficient spacing between the vias used on the isolated source planes, as seen in Fig. 6.18.

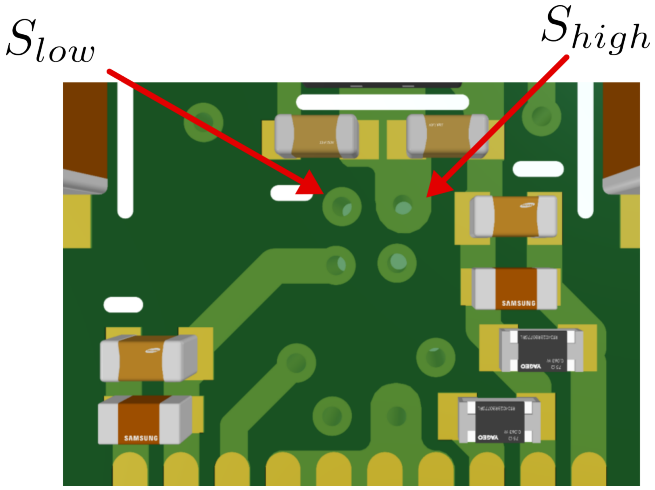



Figure 6.18: Lack of isolation due to close proximity via with 0.2mm clearance

The vias in this figure are only 0.2 mm apart and likely contribute to noise coupling between the isolated nodes, in addition to the lack of spacing in all other areas. The potential difference between these nodes could in theory be as high as $V_{fc,k}$ or $V_{fc,k+1}$. Combining all of the above with the high $\mathrm{d}V/\mathrm{d}t$ and $\mathrm{d}I/\mathrm{d}t$ of GaN switches could present a reasonable explanation for the noise coupling, noise-induced switching and the arcing sound emanating from the PCB during higher voltage operation. All of the spacing issues, parasitic capacitances and parasitic inductances could lead to a sort of resonant tank circuit connecting the sources of opposing switches as illustrated in Fig. 6.19.

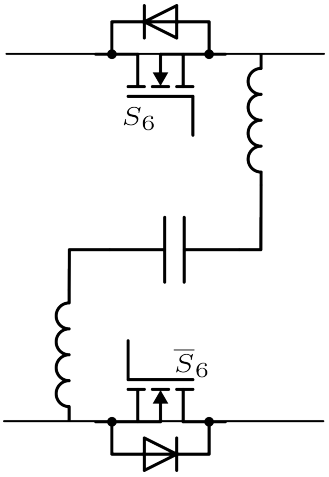



Figure 6.19: Parasitic connections between isolated switches

This resonant circuit could then be excited by all the high-slew-rate switching transitions, which occur at high frequencies, causing noise to be coupled to all other nodes and, in turn, creating the unwanted switching transitions. It could also contribute to a significant amount of common-source-inductance(CSI), which is a significant issue in GaN driving, as the voltage created across the CSI fights against the gate driver voltage [62]. This could be one of the causes of the unwanted turn-off seen in the data.

Even if the above reasoning is incorrect, it is not possible to resolve these issues and push the converter to full power using the presented design. Therefore, a new design will need to be created to address the problems identified and push the system to nominal power output. Then, the closed-loop system can be further developed and tested.

## 6.4 Improving the design based on results

The previous sections indicated fundamental flaws in the design of the converter PCB, but demonstrated that the core concept of the topology is sound. Therefore, the choice is made to redesign the power stage PCB to improve on the discovered flaws and bring the topology closer to its theoretical performance. This section will highlight the major changes made to the board.

### 6.4.1 Rethinking gate driver isolation

In the previous design, a power isolator was used to create the floating switching nodes required for the flying capacitor topology. On this isolated plane, the switches and non-isolated gate drivers were placed. This led to the use of a large isolated ground plane, which was likely a major source of noise coupling and led to a sub-optimal common-source-inductance(CSI) between the switches and nodes and other parasitic elements. As discussed before, CSI is a major problem when designing high-speed GaN gate driver circuits. A more compact solution allowing for a lower CSI and a lower inductance layout is required. Therefore, the Allegro AHV85111 [76] isolated bipolar gate driver is selected. This driver integrates the power isolation, signal isolation and gate driving into a single package. It features a bipolar output, meaning the GaN switch can be turned off using a negative gate voltage for better noise immunity. Although this is not strictly required for the EPC2307 GaNFET [63], it could still be helpful. Furthermore, this driver features a common-mode transient immunity of 100V/ns, which is four times higher than the previous solution. It also simplifies the design of the gate driver layout, as the component count compared to the previous design is almost halved. This allows the parasitic to be minimised and should eliminate the need for vias on the isolated plane. This will minimise the chances of arcing due to isolation breakdown, which was one of the flaws with the previous design.

The only problem with the new gate driver is the need for a 12V supply. Therefore, a small boost converter is designed around the TI TLV61046. This boost converter needs to output enough current to run all of the isolated gate drivers. The worst-case input current for the gate drives is 10mA. If all gate drivers are consuming the worst-case input current, then the required current from the boost converter is 120mA. The IC has an integrated power switch with a peak current of 980mA and should be able to provide 250mA of output current at 12V. The boost converter layout can be seen in Fig. 6.20. When laying out the boost converter, care was taken to keep the inductor current loop as tight as possible and make all power planes large enough to handle the peak current, but no larger than strictly necessary. This is done to avoid increasing parasitic capacitances and inductances.

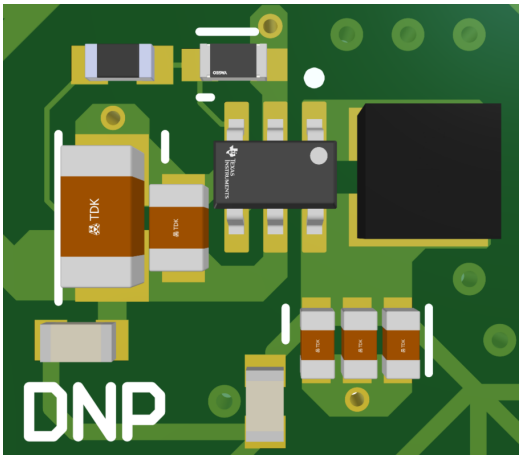



Figure 6.20: 12V boost converter layout

Furthermore, significant output capacitance is added with an effective capacitance of 13 $\mu$F. Not only to minimise any output ripple, but also to increase transient immunity against current draw spikes from the gate drives. While high output capacitance could cause start-up issues, this IC provides a soft-start to slowly charge the output capacitor on start-up, thus avoiding large inrush currents.

### 6.4.2 Improving GaN gate driver layout

With the new gate driver, the layout for the floating nodes needs to be redone. As only the power stage PCB is changed, there is not much room for increasing the size of the PCB. This presents a design trade-off as the new gate driver is wider than the previous solution. Therefore, the flying capacitor banks need to be adjusted. Instead of having two capacitors side-by-side, only 1 capacitor will be used per side to save space. The same capacitance will be reached by stacking the missing capacitors on top of each other. With this layout change, the decision is also made to switch from a 6-layer PCB to a 4-layer PCB to lower cost and complexity.

In combination with a new gate driver, a separate turn-on and turn-off resistor is used in the new layout. This allows for tuning of the turn-on and turn-off behaviour separately. In general, GaN switches should be turned off fast to limit any chance of unwanted turn-on, but turning on very fast can give rise to significant ringing, which can produce an overvoltage on the switch. Thus, the turn-on speed should be limited [62]. This layout enables tuning the behaviour easily. These resistors are laid out in line with the gate of the switch with traces that are as short as possible to minimise any parasitic inductance, but still accessible enough to change the gate resistance. This was an issue with the previous layout, so some space needs to be kept free. The new layout can be seen in Fig. 6.21.

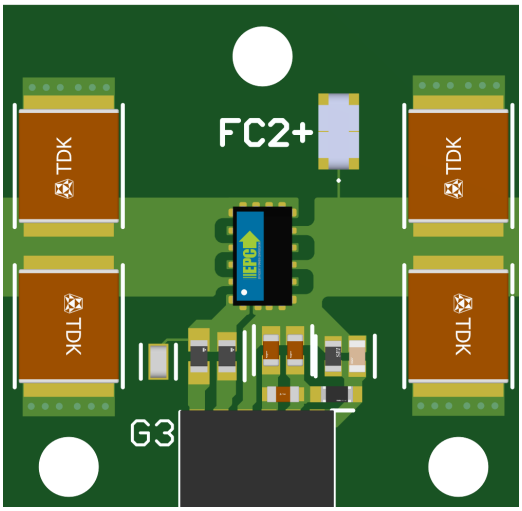



Figure 6.21: Improved floating switch node layout

Outside of the gate driver layout, improvements have been made to the clearance between high-voltage nodes. Vias on or near isolated planes have been fully eliminated, and more clearance is given around the pins of the GaN switch to comply with IPC-2221B [75]. An extra safety margin is also built in as the clearance is designed around a supply voltage of 800V instead of 600V. Additionally, SMD test points are added to allow for safe measurement of important variables, such as the capacitor voltages, gate voltages and drain-source voltages. Finally, a decoupling capacitor on the input of the power section is added to help with transients on the input, and the high-current traces are made thicker to allow for higher power throughput and improved thermal performance. With these changes, the PCB is manufactured and assembled.

## 6.5 First results of the new design

As with the previous design, the assembled PCB can be brought up to working order in a few steps to safely test that all components are functioning as expected. With this design, there is less to test, as the gate driving and isolation are now combined into one. Therefore, the following steps are taken to commission the amplifier:

- Low voltage: Test 12V boost converter and gate drive waveforms without load
- Power testing: Connect HV supplies and start increasing supply voltage and output power
- Stability testing: Measure capacitor balance and thermal behaviour at and above rated power

If these steps are performed successfully, functional testing of the setup can begin. This means increasing the load, measuring efficiency, testing different filters and loads, enabling the closed loop and measuring the output quality in the form of the THD.

### 6.5.1 Gate drives

First, the low-voltage circuits are tested. The 12V boost converter is turned on while no gate drive signals are present, and then the gate drive signals can be turned on. The gate drive voltages are then measured. The resulting gate drive waveforms can be seen in Fig. 6.22

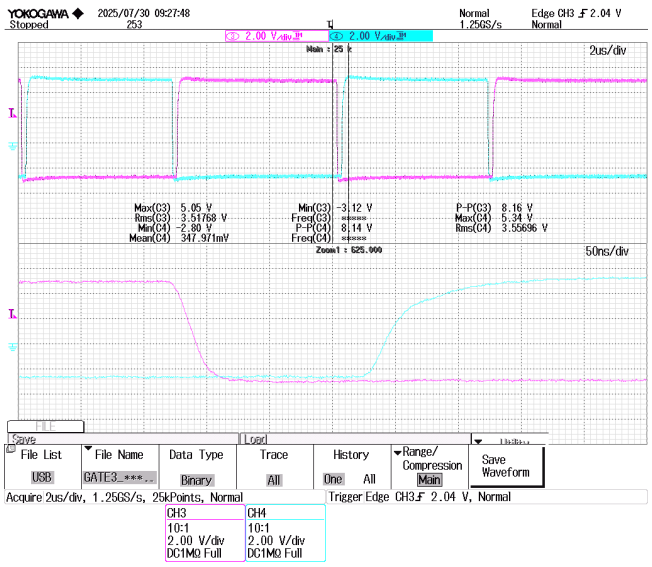



Figure 6.22: Gate drive signals for one switching cell

After some experimenting, a turn-on resistance of 25Ω and a turn-off resistance of 8Ω is found to be adequate. This ensures a relatively slow turn-on without much ringing, but a fast enough turn-off to prevent accidental turn-on. The impact this has on the waveforms is also clearly visible in Fig. 6.22.

### 6.5.2 Applying power

With the gate drives up and running, the input power supplies can be turned on, and the power can be increased. The goal of these tests is to verify that the converter behaves as expected before testing the limits of the setup and comparing it to the requirements. These first tests at the nominal operating voltage of 600V are done with a 100Ω load to limit the current at the output. An LC filter with a cutoff frequency of 20kHz is used. The modulator is set to generate a full-scale sine wave at 350Hz. The results of this first test can be seen in Fig. 6.23.

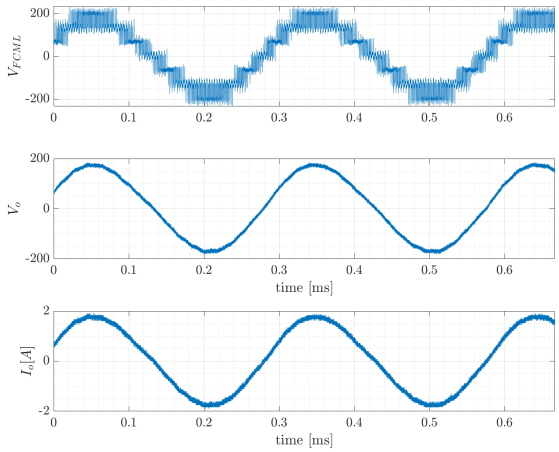



Figure 6.23: First tests at nominal operating voltage

In this figure, a much cleaner waveform can be seen compared to the previous board. Note the lack of noise

and switching in the converter output before it is filtered. While there is still some overshoot in the unfiltered waveform, this does not significantly impact the performance of the filter. At this point, the converter is also outputting 200W on average. This is a significant improvement compared to the 20W of the previous design, but it is not yet the nominal RMS output power of 750W. To test this, the previous load resistance is changed to a 60Ω high-power rheostat. The results of this can be seen in Fig.6.24.

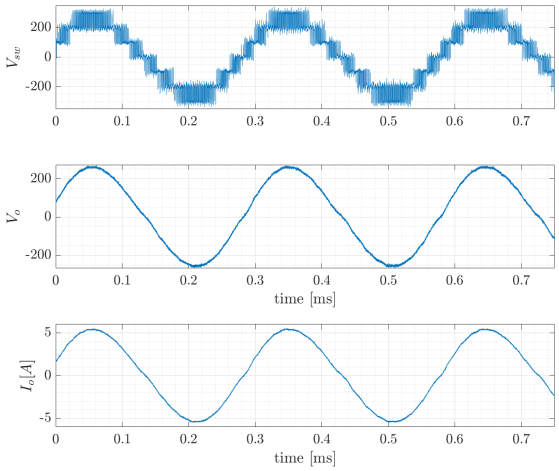



Figure 6.24: Operating at nominal power

At this power, the converter still behaves as expected, although some zero-crossing distortion can be seen in the filtered output voltage and current. At this point, the thermal performance of the system becomes a more important factor, as there is no heatsink present on the switches at the moment of these tests. Therefore, a small fan is used to provide airflow over the switches, and a thermometer is used to monitor the temperature. With a fan and at nominal output power, the switches sit at a temperature of 103 °C in steady state. While this is relatively hot, the EPC2307 GaN switches have a maximum operating temperature of 150 °C. These tests show that the converter is capable of operating at its nominal operating point in steady state without any significant issues.

The next item to check is the capacitor voltage balance. If this variable is also within specifications, then testing can continue. The capacitor balance is measured at the converter's nominal operating point. The results of these measurements can be seen in Fig. 6.25.

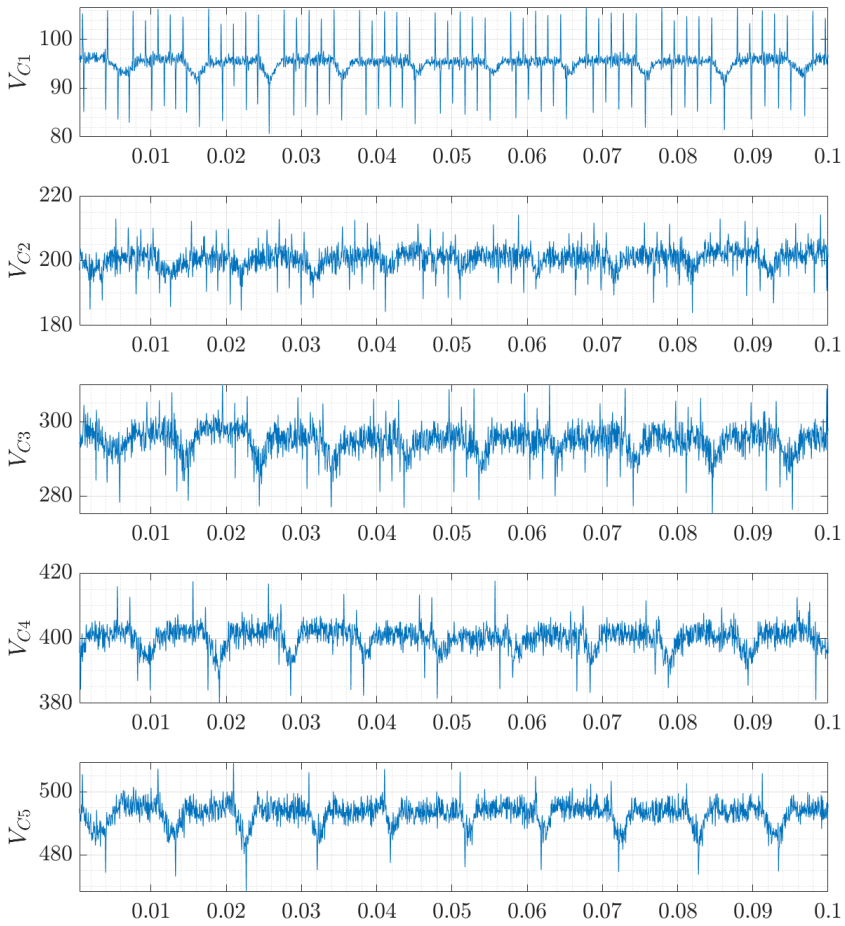



Figure 6.25: Capacitor voltage balance under nominal operating conditions on a resistive load

From this figure, it can be seen that the voltage balance shows significant spikes in the voltage at the effective output frequency of 600kHz. These spikes are not necessarily problematic as the capacitor voltages return to nominal almost instantly, and the voltage, on average, is balanced out. This could theoretically lead to an overvoltage transient on the GaN switches, but GaN is robust against overvoltage transients due to its lack of avalanche breakdown and other mechanisms compared to its Silicon counterparts [62], [67]. The results are averaged out and tabulated in Tab. 6.2.

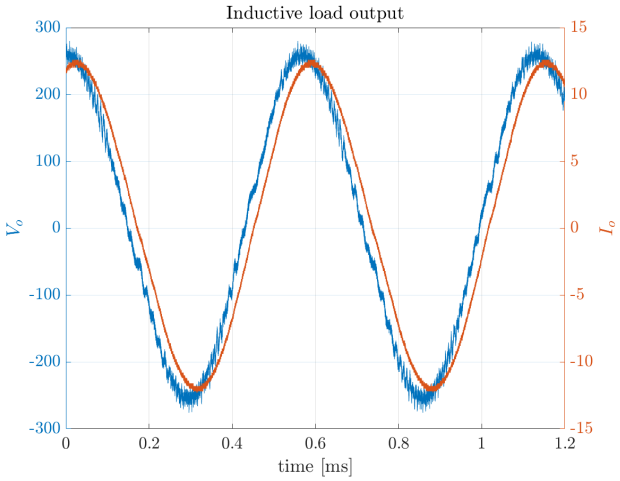
Table 6.2: Capacitor balance

| **Capacitor cell** | **Peak** $\Delta V_c$ | **Avg.** $\Delta V_c$ |
|---|---|---|
| $V_{C1}$ | 42V | 5V |
| $V_{C2}$ | 59V | 12V |
| $V_{C3}$ | 64V | 17V |
| $V_{C4}$ | 74V | 11V |
| $V_{C5}$ | 69V | 10V |

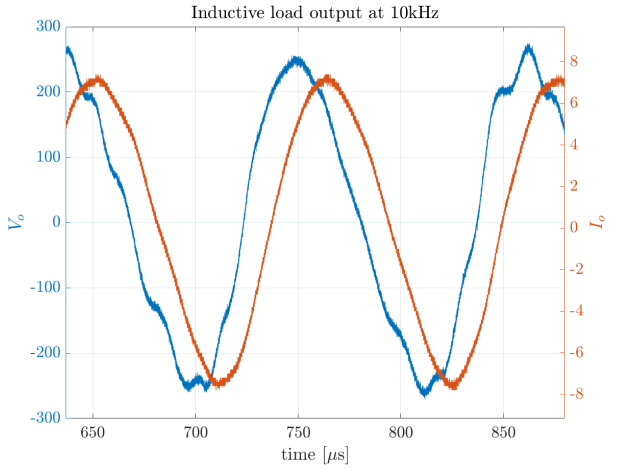
When these results are taken into account, the voltage balance is close to the designed maximum difference of 10V at its nominal operating point. Extra capacitance could be added to decrease the output ripple, but there is an adequate safety margin with regard to the safe operating area of the switches.

As a final test, an inductive load of 400$\mu$H is connected in series with a resistive load. The rheostat needed to

be changed to a lower resistance value due to thermal limitations. This led to a peak output current of more than 10A. This situation roughly mimics the load of an electromechanical actuator, albeit one with relatively low inductance. The point of this test is to verify if the converter still operates as expected under an inductive load. The converter has no issue delivering 10A and RMS powers of 1.5kW. With additional cooling, the switch temperature does not go above 110 °C.




(a)




(b)

Figure 6.26: Output using inductive load at different frequencies. (a) at $f_o = 1.8$kHz and (b) at $f_o = 10$kHz

From these figures, the expected phase shift can be seen clearly. The voltage quality does seem to suffer when an inductive load is used. The output current at higher output frequencies is most likely due to the low-pass filtering effect of an RL circuit. The -3dB point of an RL circuit is:

$$f_c = \frac{R}{2\pi L} = \frac{18\Omega}{2\pi \cdot 400\mu\text{H}} \approx 7.1\text{kHz}. \tag{6.9}$$

So at 10kHz, the output should indeed be lower due to the low-pass nature of the load.

With all these tests, it is shown that the power amplifier works as expected with the redesigned PCB. The amplifier performance can be characterised and further developed.

## 6.6 Measuring efficiency

While the efficiency of this converter is not a primary requirement, it does help to verify the thermal calculations and helps with finalising the design of the heatsink.

To measure the efficiency, a Yokogawa WT500 Power Analyser is used. As the setup is being fed with a bipolar split supply, the supply voltage and current for both sources will be measured and used to compute the

efficiency. Due to the frequency limitation of the power analyser, only the efficiency with the LC filter attached can be properly measured. This also limited the output frequency to 500Hz. To vary the output power, a variable 50Ω rheostat is used. The efficiency is computed as the rms output power divided by the rms input power. The power required by the microcontroller and the gate drive supply is added to the input power. This power does not seem to vary with output power and adds up to 2.25W. The results of these measurements are plotted, and a line is fitted through these data points. This can be seen in Fig. 6.27.

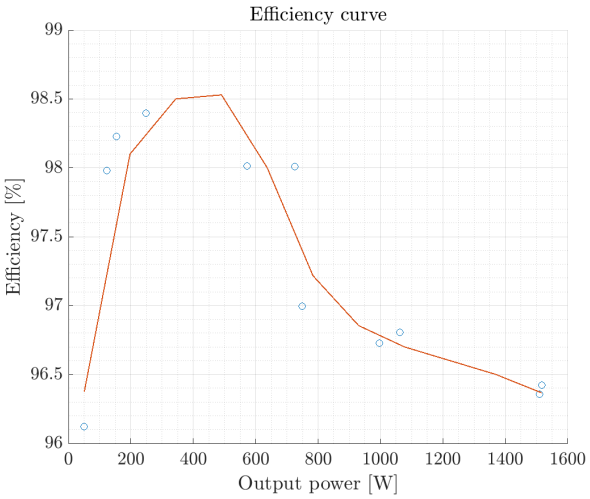



Figure 6.27: Amplifier efficiency including LC filter

From this, it is clear that the efficiency data is not very consistent, but there is a general trend. At low power, the efficiency is low because the losses from the gate drive and microcontroller have a larger impact. As the power increases, this loss is less significant and the efficiency peaks. As the power is further increased, the switching losses, resistive losses and other losses increase with the increased current, thus lowering the efficiency. One reason for the drop-off at higher power could be due to saturation of the filter inductor. Above 1kW, the RMS current through the inductor is above 5.5A, which is above its rated current. This could be a potentially significant source of loss. One side note to add to these measurements is the input power ripple. Due to insufficient decoupling capacitance on the motherboard, the supply current varies significantly at lower frequencies. This could be fixed by adding an external capacitor bank, but the efficiency of the converter is not the main focus of this project. The worst-case efficiency is above 96% and around 98% at rated power. If the rated power is used and the filter losses are ignored, the worst-case losses per switch can be calculated:

$$P_{loss,sw} = \frac{P_{rated}(1-\eta_{rated})}{n_{sw}} = 1.25W. \tag{6.10}$$

Looking back at the previous section, a worst-case switch loss of 1.5W per switch was assumed. This means that the actual worst-case switch efficiency outperforms the worst-case estimate.

The efficiencies measured match those found in the literature for similar high-bandwidth multilevel converters [39]–[41], [77].

## 6.7 The effects of amplifier parameters on THD

The THD of the converter is important, as discussed in the first chapter. From the literature, it is known that a THD between -28dB and -55dB is what could be required in high precision actuators [13]. The THD will be determined using an oscilloscope and analysing the data in MATLAB. The THD is measured at different operating points and compared. It will be compared to the output frequency, output current, and modulation index.

First, the output frequency comparison is plotted in Fig. 6.28. For this dataset, the output power is set to its nominal value, and the modulation index is set to its peak value.

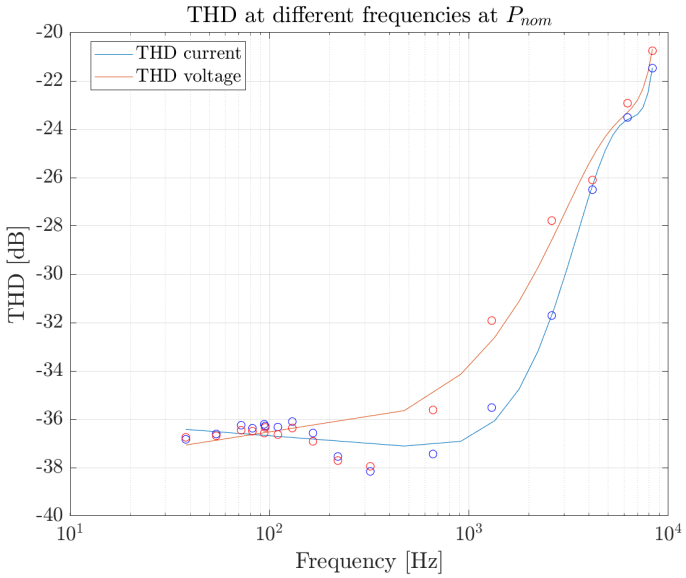



Figure 6.28: THD vs Output frequency at nominal power

From this, it can be seen that a peak THD is reached around 350Hz with a THD of -38dB. At low frequency, the THD is slightly elevated. This is likely due to the aforementioned input voltage ripple due to insufficient decoupling capacitance, which is more pronounced at low output frequencies. As the frequency increases, so does the THD. This can be attributed to multiple factors. One of these factors is the shortened duration the converter spends at a discrete switching level. As this period starts to approach the switching frequency of each cell, the relative modulation resolution gets worse, as there are fewer switching periods to generate the desired waveform and the ratio $\frac{f_{s,mod}}{f_o}$ gets closer to one. This causes increased harmonics and noise at lower frequencies, which are not well attenuated by the filter [78], [79]. While this effect is limited due to the higher effective switching frequency, the PWM modulators are only updated at 100kHz due to hardware limitations. The lower modulation resolution also introduces non-linear distortion sources, such as an increase in quantisation noise.

To improve upon these results, the update rate of the modulator could be improved. This could be done by implementing a multi-rate modulator [61]. This modulator can update the PWM signal at the effective switching rate, in this case 600kHz, which would significantly improve the PWM resolution as it shifts the spectral content produced by the separate modulators. Another option would be to use the high-resolution PWM modulators available on the TI C2000 boards, which could shift the resolution of the modulator from 8-bit to 16-bit [69].

Now, the variance in THD compared to the modulation index, $m$, is measured. The bus voltage is set to the nominal 600V, and the load is adjusted such that the output current at $m = 1$ is equal to the nominal 5A as well. The output frequency is taken as the best result from the previous measurement, which is 350Hz.

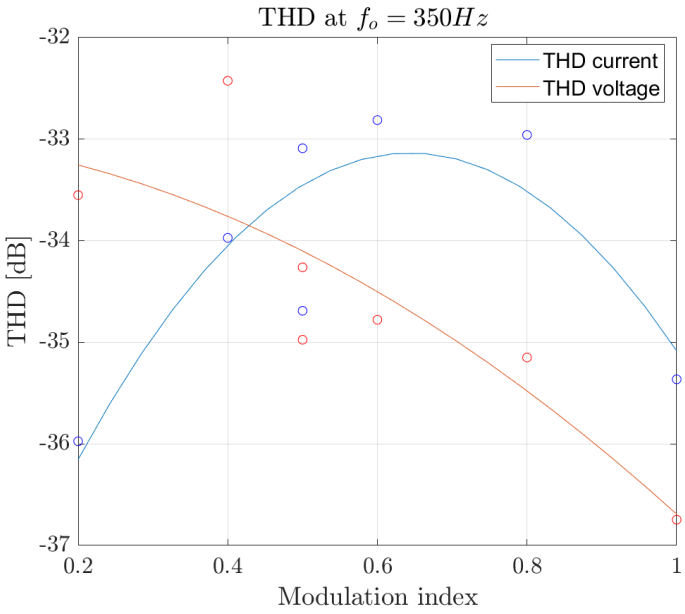



Figure 6.29: THD vs modulation index

From these measurements, it can be seen that the harmonic distortion does not vary as much as would be expected from a 2-level converter. There is only a difference of -4dB. The expectation would be that the THD would improve as the modulator index increases, as the quantisation noise decreases with it. For instance, [13] shows that the THD can vary around -15dB. This relatively low variation could be explained by the multilevel nature of the converter. As the modulation index lowers, the number of switching levels used also lowers. This causes the THD to vary in ways not expected from a 2-level topology.

Finally, the THD is compared to a varying output current. Once again, the input voltage is set at 600V and the output frequency is set at 350Hz, and the modulation index is kept at $m = 1$. The output current is varied by decreasing the resistance of a rheostat. The results of this measurement can be seen in Fig. 6.30

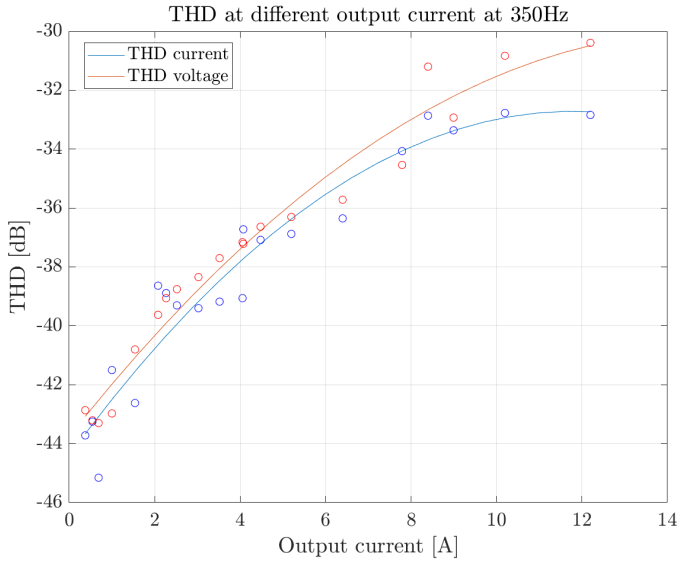



Figure 6.30: THD vs output current

From this data, the THD increases as the current increases. This follows expectations, as at lower currents, the effects of dead-time are less pronounced, and there is less energy going into the parasitics. Furthermore, the flying capacitors have lower voltage ripple, which increases the quality of the output voltage waveform. As the current increases, so does this ripple on the capacitors and at the output. At higher currents, the dI/dt also increases, which excites the harmonics. For the filter, at currents above 10A, the filter inductor used is

significantly saturated and lowering its filtering effectiveness.

To test the sensitivity of the THD to switching frequencies, the same test is done with the current, but at a switching frequency of 200kHz, leading to an effective switching frequency of 1.2MHz. The results are depicted in Fig. 6.31.

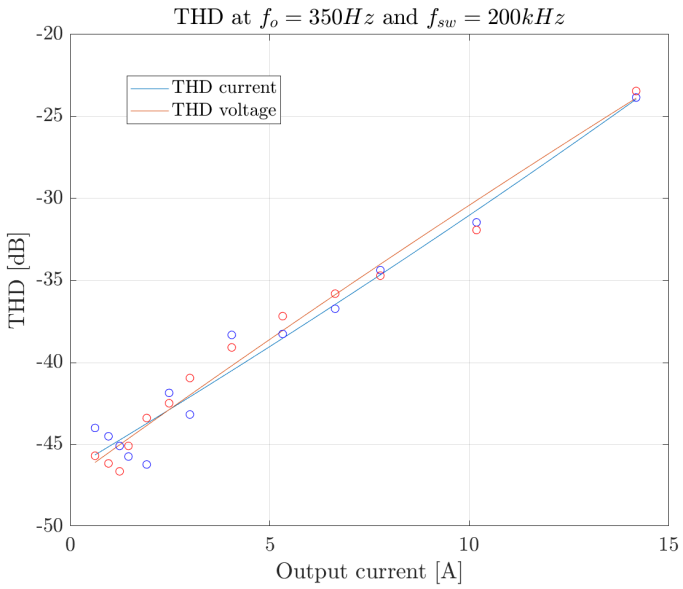



Figure 6.31: THD vs output current at 200kHz switching frequency

From this data, it can be gathered that the THD is worse overall compared to the previous test. While this means that the modulator update frequency is also increased to 200kHz, the relative resolution of the modulator decreases. This once again worsens quantisation, thereby increasing harmonics. One other effect which can explain the worse THD at higher currents, for both low and high switching frequencies, is the variations in switch junction temperature. These EPC2307 GaNFETs can double their relative $R_{ds,on}$ over their operating temperature window. These switches also have very low thermal impedance, causing the switch temperatures to vary quickly during high current switching transitions. This causes the on-state resistance to change over a switching cycle as well. These variations impact the voltage drops across the switch, which worsen the THD. At higher switching frequencies, the losses increase, making the thermal swings more pronounced [8].

From all the tests done with regard to the THD, one thing does become clear. The converter can provide output waveforms with sufficiently low harmonic distortion as required for amplifiers used in high-precision electromechanical actuators at its designed operating point. If the THD results are compared to the literature, it is found that this converter can outperform similar flying capacitor multilevel inverters with regard to THD[40], [41], [77] as tabulated in Tab. 6.3.

Table 6.3: THD comparison between different converters.

| **Converter** | **THD** |
|---|---|
| 13 level[40] | 0.7% |
| 7 level [41] | 0.3% |
| 9 level [77] | 2% |
| 3x3 level [39] | 0.034% |
| This work | 0.0258% |

## 6.8 Pushing to failure

While testing different modulation waveforms, a high slew-rate sawtooth waveform was being tested on an inductive and resistive load. When the DC-bus voltage was increased to around 400V, the GaN switches failed in a violent, explosive manner, resulting in a loud bang and bright flash. The damage of this event can be seen in Fig. 6.32.

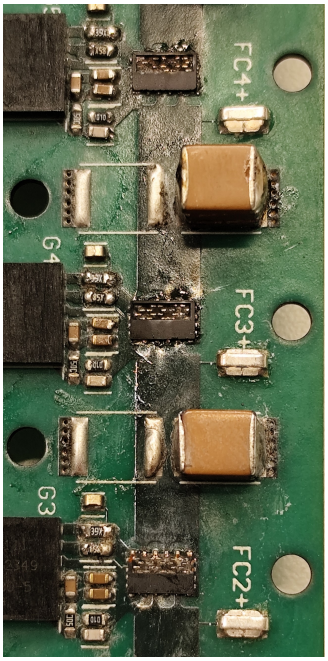



Figure 6.32: Results of destructive event

At first, the suspicion was that the high slew rate caused an inductive back-emf spike, causing a significant overvoltage. However, after some consideration, the situation that led to the failure was recreated in the PLECS simulation of the converter. The output voltage and current of the simulation can be seen in Fig. 6.33

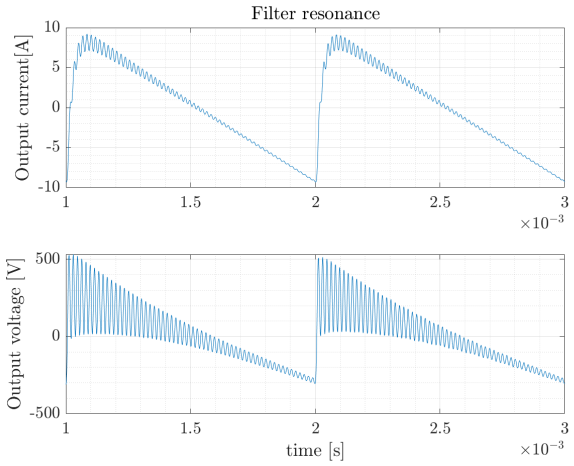



Figure 6.33: Sawtooth output

From this, one issue becomes clear. The output voltage at the high slew-rate part has an overvoltage of almost 600V. This is twice the maximum output voltage. This is by itself already an issue due to the designed clearances and other voltage-limited components. However, this also impacts the capacitor voltage balance. This can be seen in Fig. 6.34.

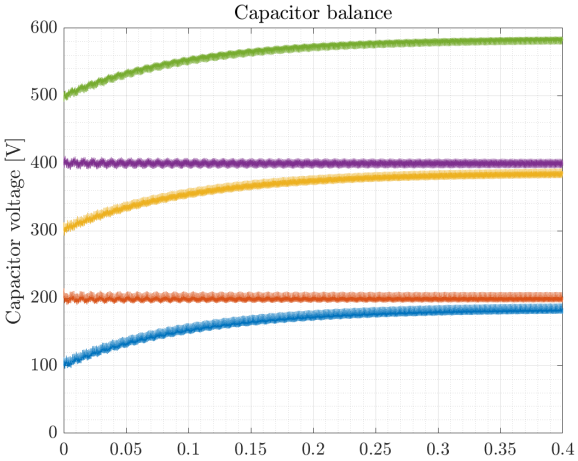



Figure 6.34: Capacitor balance in failure mode

From this simulation of the capacitor voltages, the underlying probable cause of failure becomes clear. The capacitors are losing their voltage balance, thus increasing the switch voltages above their maximum voltage, causing them to fail.

The reason for the voltage spikes is likely the resonance of the filter and the interaction with the inductive load. The high slew rate causes excessive energy at the resonant frequency. This causes the voltage to resonate and ring, causing the overvoltage. To characterise this behaviour, the Q-factor of the LC-filter can be used, which for the filter on the converter is:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = 132. \tag{6.11}$$

Where a higher Q-factor indicates a higher magnitude at the resonant frequency. Using the simulation and this equation, the peak overvoltage has been plotted for a few damping factors. In this simulation, the damping factor is used. Note that the cut-off frequency is kept the same throughout. The results can be seen in Fig. 6.35

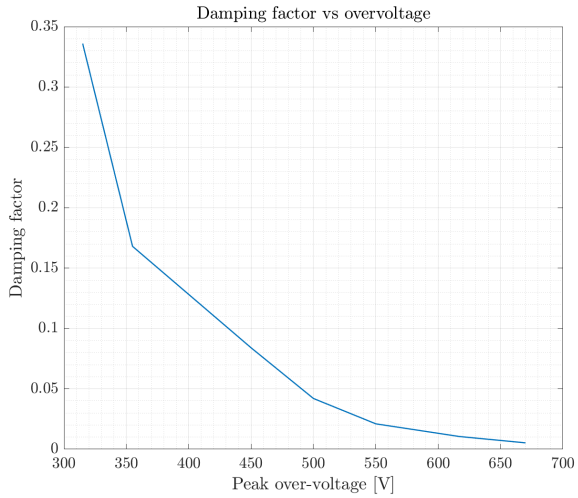



Figure 6.35: Damping factor compared to the overvoltage in simulation

From this, it can be gathered that an increase in Q-factor, or a decrease in damping-factor, has an exponential relation to the overvoltage seen in simulation.

These discoveries could be used as an additional parameter to the LC-filter design space developed in the previous chapter. This could be especially useful if high slew-rate signals at peak voltages, like sawtooth and square-wave signals, are required. These results also show that there is a possible need for monitoring the capacitor voltages when a flying capacitor converter is used as a power amplifier due to its less predictable output requirements, compared to a more predictable application like a motor drive or grid-connected inverter.

## 6.9 Closed loop control

As stated in previous chapters, one of the goals is to achieve closed-loop control of the flying capacitor-based power amplifier. The original design calls for a multi-loop control strategy, which calls for an inner current control loop and an outer voltage control loop based on the needs of the Beat The Heat flux-controller. The inner current controller must sample the ripple on the filter inductor. Due to the high effective switching frequency of 600kHz, the ADC must have a sampling rate of at least 1.2MHz to be able to accurately measure the ripple. While this is technically possible using the TI C2000 controller, it can be challenging to achieve this due to tight timing constraints and memory management. Furthermore, due to a design flaw in the analog front-end (AFE), the output of the current sensor to the controller was extremely noisy, even after the filtering stage, as can be seen in Fig. 6.36.

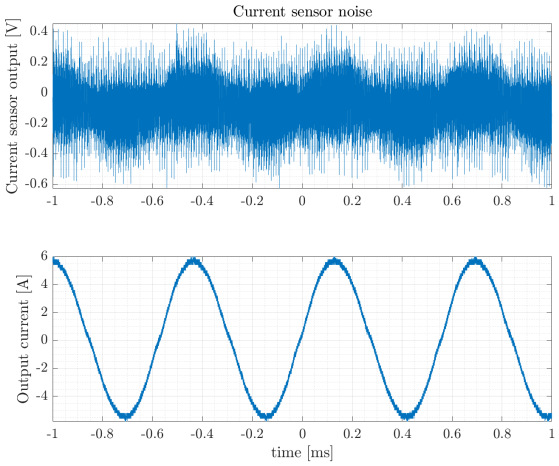



Figure 6.36: Current sensor noise compared to a current probe connected to an oscilloscope

The current sensor should have a cut-off frequency of 800kHz and a gain factor of 0.6 to scale the 5V signal to the 3V input range of the ADC at the max input of 20A to the sensor. If this 800kHz filter is applied afterwards, the results look more like one would expect, as seen in Fig. 6.37

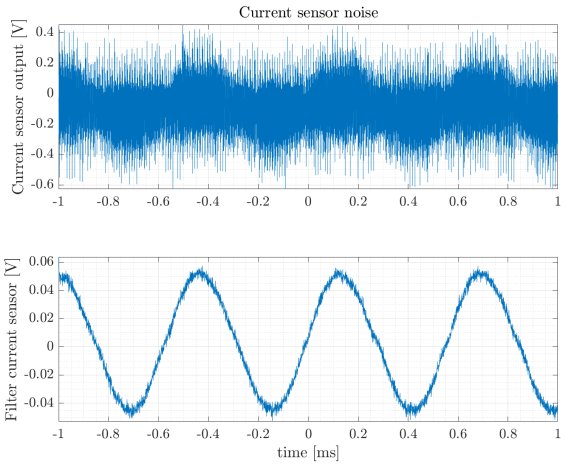



Figure 6.37: Manually filtered current sensor

However, the expected amplitude is also wrong. The sensor has a sensitivity of 100mV/A, so at a 5A peak output should output 500mV, which would translate to 300mV after the filter and gain stage. Due to limited time to spend on attempted solutions, this issue is saved for a later date, and the voltage sensor will be used. This choice is made because the output voltage control is what is required by the project. This could still be achieved by a single control loop using the voltage sensor, likely at the sacrifice of some performance and bandwidth due to the unregulated current.

The AFE of the voltage sensor is more robust due to its internal filtering stage present on the isolation chip, which only requires some input and output capacitors to filter the signal. While this signal still shows some noise, it is usable in the controller and does not require such a high sampling frequency.

For these tests, the input reference signal is generated on the microcontroller through a look-up table. The input signal is a sine wave of different frequencies and modulation depths. The results of the closed-loop voltage control can be seen in Fig. 6.38.

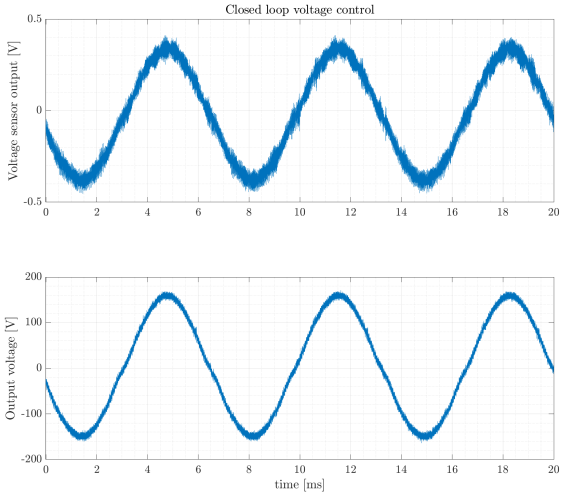



Figure 6.38: Closed loop voltage control

From this figure, significant noise is still observable in the voltage sensor signal. This noise can be coupled to the input of the PI-controller, causing the voltage tracking performance of the controller to degrade. Also, the output voltage is limited to around 180V. This is once again due to the noise. At higher voltage, the noise overwhelms the sensor, and the closed loop becomes unstable. As the voltage is increased, the voltage transients also increase in energy. This is coupling noise into the sensor path, likely in the way of common-mode noise. Therefore, a simple RC common-mode filter is used in an attempt to increase the supply voltage without losing closed-loop performance. The results of this can be seen in Fig. 6.39.

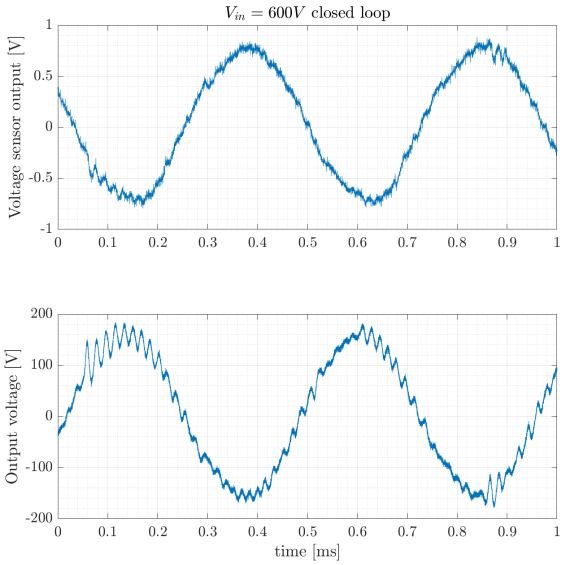



Figure 6.39: Closed loop at 600V input

While the controller is able to remain stable at a 600V input, the output waveform is very noisy and has serious harmonics. However, the closed-loop output frequency is over 2kHz. To improve the performance of

the closed-loop controller, changes need to be made to both the hardware and the software. For the hardware, better noise isolation and filtering are required to minimise the noise coupling into the closed-loop controller. For the software, better characterisation of the controller could improve the noise immunity and digital filtering could be employed.

## 6.10 Beat The Heat hardware prototype

For the part, in collaboration with the Beat The Heat project, the power amplifier is tested on a hardware prototype of the Tunable Magnetic Actuator in the middle. This hardware prototype features two reluctance actuators for compensating for any disturbances and a tunable actuator. All of these actuators feature high inductances ranging from 0.025H up to 0.25H. A picture of this setup can be seen in Fig. 6.40.

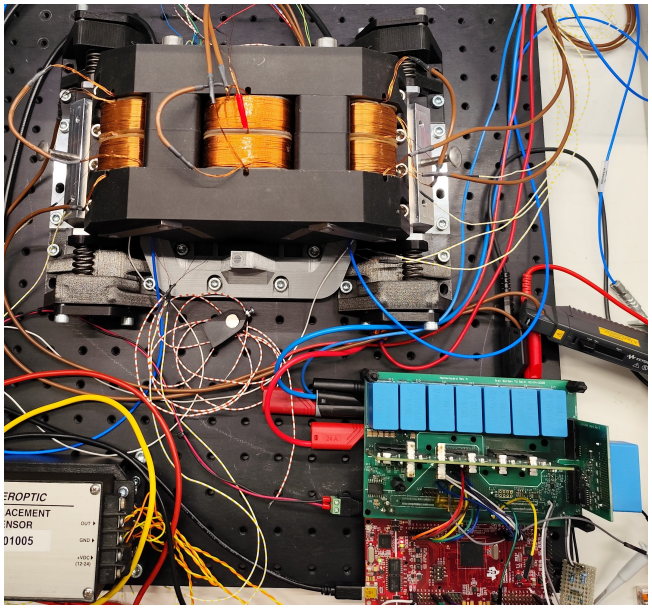


Figure 6.40: BTH hardware prototype connected to FCML power amplifier

The goal with this setup is twofold. First, the amplifier needs to be tested and see if any problems arise due to the large inductances and non-linear inductive behaviour of the tunable actuator. At first, the amplifier will be driven in open-loop, and closed-loop will also be tested. The second goal is to characterise the actuator using the designed power amplifier. As the hardware prototype is relatively large, the power required to drive it is also large. The plan is to drive both actuator types into saturation to generate a BH-loop. This is especially important for the TMA as the behaviour of the BH-loop is used to drive the actuator to a specific remnant magnetisation to generate the required static output force. Another goal is to characterise the mechanical system. This can be done by way of a frequency response function (FRF). This involves exciting the system with an input waveform with certain frequency content and measuring the output response. The transfer function of the system can then be estimated using:

$$H(s) = \frac{X(s)}{Y(s)}. \tag{6.12}$$

To do this for this system, a swept sine is used.

### 6.10.1 Testing the power amplifier

While no real issue with the functionality of the amplifier is expected, it is important to verify that the flying capacitor voltage balance is not affected by the high inductive load. Due to this inductance, the load acts like an RL filter, lowering the current at higher frequencies. This issue is exacerbated by the series connection of the two RA coils. The output at 250Hz can be seen in Fig.6.41.

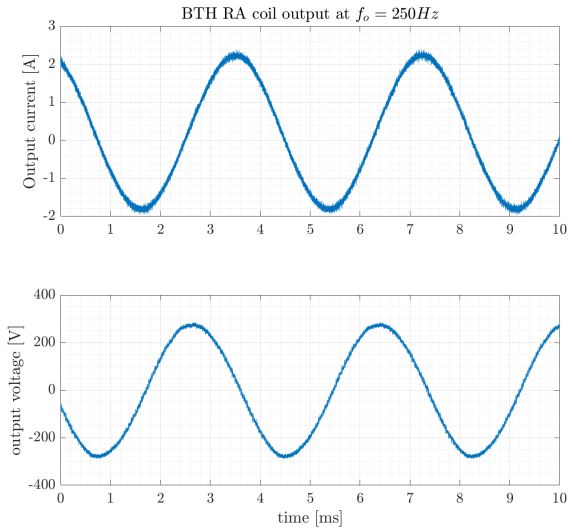



Figure 6.41: Output at 250Hz

The current reaches a peak of 2.5A at 250Hz. Lowering the frequency further also increases the current. The output at 1khz can be seen in Fig. 6.42.

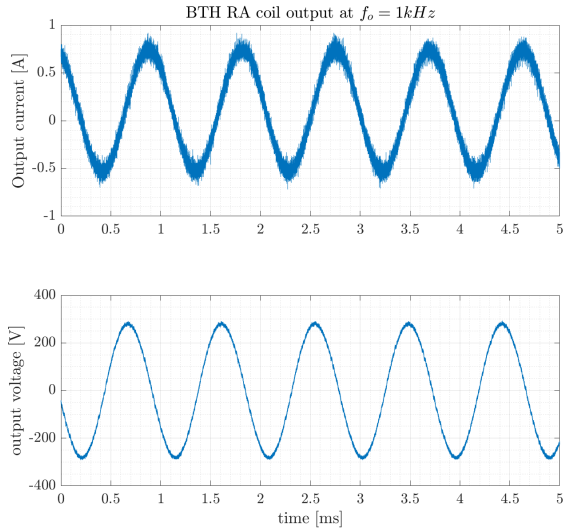



Figure 6.42: Output at 1khz

Here, the output current is even further reduced to peaks of 0.5A.
The capacitor voltage balance is determined at the nominal operating point. Therefore, the output frequency is set at 100Hz, so the output current is 5A. All of the flying capacitor voltages are measured and plotted in Fig. 6.43.

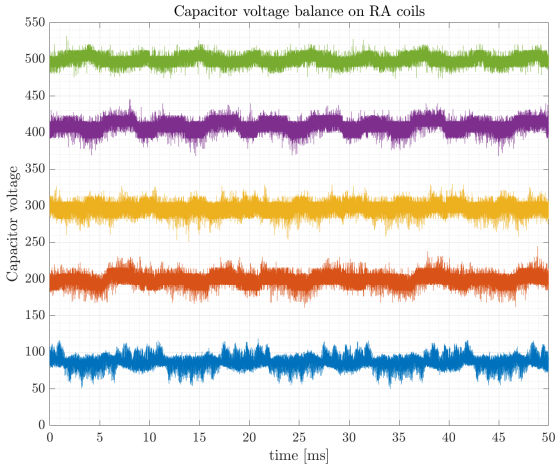



Figure 6.43: Capacitor voltage balance while driving the BTH hardware prototype

From this data, it is clear that the capacitors exhibit significant ripple. However, despite the ripple, the voltages remain stable and balanced with regard to each other. The peak ripple on the capacitors is 20V, which means the worst-case blocking voltage on the switch is 140V. This is still within the 200V limit of the switches and within its safe operating area, as long as currents are lower than 20A [63]. Therefore, the ripple does not endanger the switches, even if it is larger than the designed ripple.

Finally, the closed loop is also tested. The controller was able to keep the loop stable, but showed the same noise issues. Therefore, due to time constraints, this was not further explored as the open-loop amplifier seemed to perform well.

With these results, it has been verified that the converter can drive the Beat The Heat hardware prototype with no issues.

### 6.10.2 Characterising the actuator

As mentioned before, the actuator needs to be characterised to verify the electromechanical design. Mainly, the BH-loop of the tunable actuator is of interest as the flux-controller relies on the hysteresis behaviour of the low-coercive-force magnet. This hysteresis curve can also be used to estimate the hysteretic losses in both actuators. To gather this data, a swept sine is also used. For the TMA coil, a sinewave ranging from 25Hz to 2kHz is used, and for the RA coil, a sinewave ranging from 60Hz to 4kHz is used. The difference in frequency range comes down to the difference in inductances, which impacts the current flowing through the coils and thus the frequency at which the actuator saturates. To measure the BH-loop, the B-field and the H-field need to be measured in some way. The H-field can be derived from the current. For an idealised coil, this can be done as:

$$\oint_C \boldsymbol{H} \cdot d\boldsymbol{l} = \iint_S \boldsymbol{J} \cdot d\boldsymbol{S} \Rightarrow H = \frac{N i_{coil}}{l}. \tag{6.13}$$

The B-field can be measured in two ways. There are Hall effect sensors embedded in the air gap between the coils and the mover. Also, there are sensing coils sandwiched between the coil packs. These sense coils measure the flux through the coil, simply as:

$$\lambda_{coil} = \int V_{coil}\ dt. \tag{6.14}$$

Both of these measurement methods can be combined to improve the quality of the measured B-field. The waveforms of the swept sine wave on the TMA coil can be seen in Fig. 6.44.

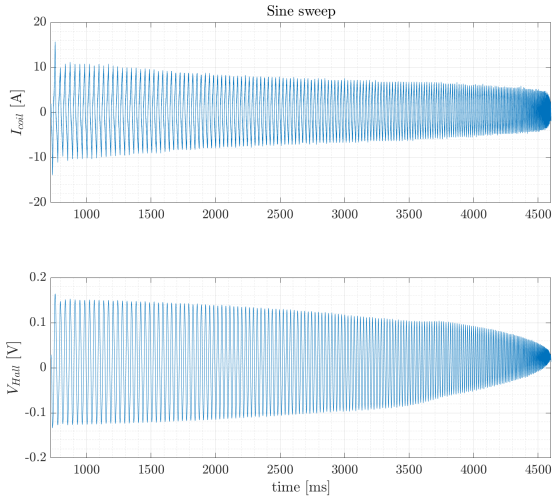



Figure 6.44: Swept sinewave from 25Hz to 2kHz

The saturation of the magnet can already be discerned from this plot. At the low frequency, the current spikes, while the measured B-field does not. This means the H-field is increasing, but there is no meaningful change in the flux density at that point. To properly visualise this, the BH loops are plotted and a few are highlighted in Fig. 6.45.

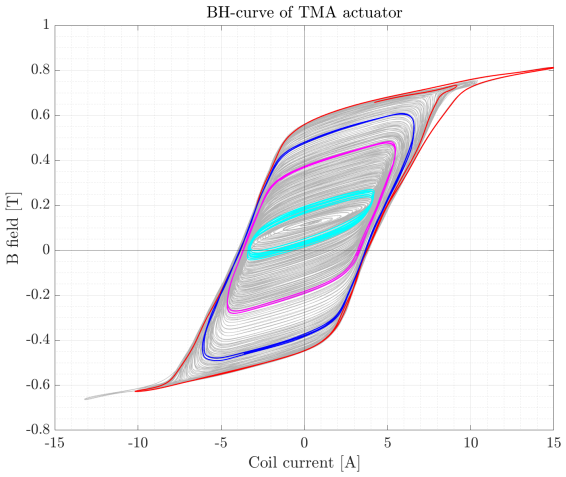



Figure 6.45: BH-loop of the tunable actuator

From this plot, the hysteresis behaviour is visible. The wide nature of the hysteresis loop indicates the low coercivity of the AlNiCo magnet. The major outer loop in red shows the limits of the BH-loop, and the other smaller inner loops show that the magnet can be magnetised to different remnant states. This plot is similar to the PLECS model made in chapter 1 and visible in Fig. 2.2. The actuator was designed to saturate at a magnetic field of 1T. While the measurements show that saturation occurs around 0.8T, this could be because the Hall sensors are not in the magnet but between the pole surface and the mover. Therefore, some field lines may not cross the sensor.

The same test is done for the RA coils. The expectation for this test is a narrow hysteresis curve due to the magnetic hardness of the material used in the actuator. The results of this can be seen in Fig.6.46.

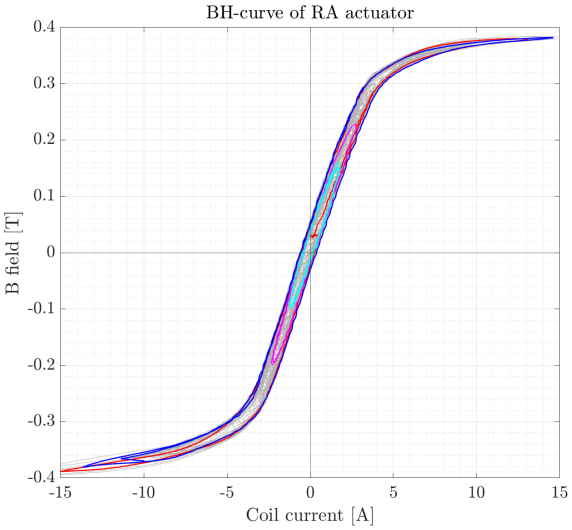



Figure 6.46: BH-loop of the reluctance actuators

The behaviour seen in this plot matches the expected narrowness of the loop. These actuators are not supposed to be magnetised at all, but are used to offset disturbances to the system and control the force dynamically when required. Therefore, the hysteresis loop should be as narrow as possible to minimise hysteresis losses.

All of the tests done in this section show that the designed flying capacitor-based power amplifier can be used to drive the actuators it was designed for, and has performance characteristics that match similar designs found in the literature.

# 7 Conclusion and recommendations

## 7.1 Conclusion

**Actuator specifications and requirements for power amplifiers**

The primary objective of this project was to design and test a high-bandwidth power amplifier based on the identified requirements for high-precision actuators. More specifically, the Beat The Heat project serves as an impetus for the design. Its goal is to design an actuator with minimal heat dissipation by utilising tunable hybrid reluctance actuators. These actuators can be tuned by changing the remnant magnetic field of a low coercive force permanent magnet, such as AlNiCo. Although these actuators do not necessarily require high bandwidths, other types do. Different types of high-precision electromechanical actuators are introduced, and some of their key specifications and parameters are explored through literature. This indicates a need for high-bandwidth converters with increasingly lower distortion and noise limits, with total harmonic distortion as low as 0.001%. Instead of focusing on a single type of actuator, a set of requirements is established for a power amplifier which could be used on a multitude of different actuators. The goal of the project is then to design a power amplifier which can be used for general precision electromechanical actuators.

**Design aspects of multilevel converters**

From the requirements, multilevel converters came forward as an interesting and novel topology for high-bandwidth power amplifiers due to their inherent high effective output frequency, high output signal quality, and lower stresses on the switching transistors. Specifically, a flying capacitor multilevel inverter was chosen as the core of the power amplifier. This topology uses series-connected switches linked together by floating capacitors. Connecting these capacitors in certain patterns generates multiple voltage levels. The core requirements are based around high bandwidth, low noise and distortion and increased output power. In the literature, these requirements are often touted as virtues of the multilevel topologies. However, relatively little is published on using these topologies as power amplifiers and the challenges faced when translating these theoretical designs to the real world. To close this gap, a hardware prototype of a multilevel power amplifier is designed and tested.

Core design aspects of a flying capacitor converter are identified. These consist of the number of switching levels, the size of the flying capacitors and the voltage balance of the capacitors during operation. A 7-level topology is selected to maximise the Figure of Merit of the GaN power switches, while still having an adequate safety margin. A capacitor size of $2.2\mu$F is designed based on expected conditions and verified through simulations. To turn the converter into an amplifier, an LC filter and closed closed-loop controller are designed. The LC filter is developed using a design-space approach. For the controller, a multi-loop strategy is adopted and implemented in simulation.

### Prototype implementation and validation

The results from the hardware prototype showed that the core topology is suitable for use as a power amplifier and can compete with other designs when comparing total harmonic distortion, efficiency, output bandwidth, and output power. The amplifier managed to reach THD's of -38dB at nominal operating points, output bandwidths up to 10kHz, peak output power of 4.5kW and RMS power of 1.7kW, all at a DC-bus voltage of 600V. However, the weak point of the design was the noise generated by the converter, and the improper implementation of noise mitigation techniques in the sensing circuits. This led to deteriorated performance in closed-loop control. It should be noted that the closed loop did function, but the performance was not close to the open loop performance. This is also a design flaw in the prototype, not an inherent problem with the flying capacitor topology. A thorough analysis of the sensing and power circuits is needed to minimise noise and improve the performance of the closed-loop.

This prototype was also tested on the hardware prototype of the Beat The Heat project, which features a tunable magnetic actuator and two reluctance actuators. The amplifier functioned as designed on this setup. It was able to drive all of the actuators and managed to extract the hysteresis loop of the tunable actuator by saturating the AlNiCo magnet, generating a magnetic field of up to 0.8T.

### Practical challenges and considerations

As previously mentioned, there is a gap in the literature between the theoretical designs and hardware prototypes. Through this project, some possible reasons for this have been found. There is a trade-off between the complexity of the design and the performance of a flying capacitor converter. At high effective output frequencies and powers, it becomes increasingly challenging to control the converter through closed-loop control at bandwidths that can make use of the virtues of these topologies. This is a multidisciplinary problem. The embedded system needs larger sampling rates, faster execution of control laws and higher frequency driving of the switches and other control electronics. Proper analog circuit design is required to build noise-immune analog front ends which correctly drive ADCs. Finally, the PCB design and layout become critical at high frequency and high power to limit the generation of noise and EMI. All of these factors combined make it challenging to maximise the possible benefits inherent to multilevel topologies for use in power amplifiers. This is also clear from the results of this project, as the limiting factor in performance was not the topology itself, but the design flaws in the sensing circuits, PCB design and software.

All in all, this project has successfully demonstrated the design and implementation of a multilevel power amplifier that can be used for electromechanical actuators of different kinds and has shown performance in line with the literature. This project has also demonstrated some of the pitfalls with regard to closing the gap between theory and reality, which has limited the performance of the prototype in some regards. However, a lot of knowledge was gained about these pitfalls and how to avoid them in the future.

## 7.2 Further work and recommendations

While this project has come to an end, there is still a lot of progress to be made on this topic. Therefore, some comments on further work and recommendations will be given.

### 7.2.1 Further work

- To properly achieve high closed-loop bandwidths and low distortion, the sensing circuits will need to be redesigned. This should be the first thing that is looked at in further work.
- Add protection features. In the current design, the converter has little in the way of protection, either against overcurrent, overvoltage or other problems. Ways of implementing this should be investigated, so that this prototype is more usable by others.
- Improve input signal generation. Due to the aforementioned noise issues, the reference signals for the amplifier are generated on board the microcontroller to avoid any issues. This is not user-friendly and needs to be changed. Solutions for this should be investigated. A digital solution would be preferable due to inherent noise immunity and flexibility.
- Develop the single-phase amplifier into a three-phase system. Right now, only single-phase/coil actuators can be driven, but 3-phase actuators, like motors, are also of interest.

### 7.2.2 Recommendations

- Instead of long analog sensing lines, convert the noise-susceptible analog circuits to digital with an ADC directly at the sensor interface. This should significantly increase the noise immunity and also the performance, as the onboard ADCs of the TI C2000 can become limiting at the high sampling rates required in these types of high-bandwidth amplifiers.
- While the modularity in the design was a good choice, the implementation could use some work. A slightly more noise-robust implementation should be used in further work. One idea is to use castellated-edge PCBs where only 1 switching cell is placed on a small PCB. This allows for cheaper and quicker fine-tuning of the gate-driving circuit as the PCBs are much smaller. These castellated-edge PCBs can ensure proper low-inductance contact with a motherboard with much shorter trace lengths all around.
- Rethinking the controller. In the current design, a DSP-like microcontroller on a development board is used. While the controller itself is powerful enough, its implementation in both software and hardware leaves a lot to be desired. A custom board for the microcontroller could help to improve noise immunity and overshoot
- Even better isolation. While most issues regarding the isolation were fixed in the second version, when it comes to the high-power side, there is still a significant amount of noise on the low-voltage ground, likely coming from the gate drivers. This causes the ground-referenced ADCs to misbehave as well. Therefore, more isolation could be preferable. One such solution would buffer and isolate all the gate drives, isolating the low-voltage side of the gate drivers from the low-voltage side of the controller, ensuring near total immunity and isolation.

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# A Flying Capacitor Power Amplifier for High Bandwidth Electromagnetic Actuator


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***Abstract*—This article introduces the design of a high-bandwidth 7-level flying capacitor multi-level (FCML) converter for a hybrid reluctance actuator. The converter is designed with GaN MOSFETs. Simulation results demonstrate that the converter can produce a signal with an output frequency range of DC up to 10kHz. This is verified with a hardware prototype. This prototype has managed to achieve THDs of -48dB, a peak efficiency of 98.2% and output powers up to 6kW.**



***Index Terms*—Multilevel converters, DC-DC power converters, and Actuators.**


## I. Introduction

Modern high-precision production processes, such as microchip lithography and others, require incredible precision and accuracy on the nanometer scale. To accomplish this, mechanical motion systems are employed. These are often used for positioning semiconductor wafers or instruments to accomplish various tasks, such as imaging, inspection, or exposure. These systems are driven by various electromechanical actuators such as voice-coils, linear motors, or reluctance actuators [1]. All of these actuators have different power ratings and operating characteristics.

As demand for semiconductors rises, the need for higher processing speed of even smaller features increases with this demand. The higher processing speed means higher acceleration and top speed for the electromechanical actuators, which requires a higher power output and bandwidth from the power amplifiers as depicted in Fig. 1. Furthermore, the decrease in feature size on the wafers means that disturbances have an even larger impact, thus increasing the requirements on the signal-to-noise ratio (SNR) and the total harmonic distortion (THD) [2]. According to [3], the required SNR needs to increase with $\approx$ 20 dB every five years and according to [4] this figure is now at 110 dB of SNR and -100 dB of THD. Some of the actuators in these systems rely on low-friction bearings, such as air- and magnetic-bearings, or are even fully levitating like planar magnetic actuators [5]. The low-friction nature of these actuators causes the system to be very sensitive to disturbances in forces from electromechanical actuators. These forces are proportional to the current being injected from the amplifiers, thus the amplifier needs to have a large bandwidth to compensate and a high SNR to minimise disturbance to the mechanical system. These bandwidths can be as large as 10 kHz [4]. This frequency band is the range where the output distortion has an impact on the mechanical system, as the position controller often has limited control authority at higher frequencies and is therefore unable to dampen any distortion. Any noise above this frequency is generally well attenuated by the mechanical dynamics due to friction and other related effects [1].

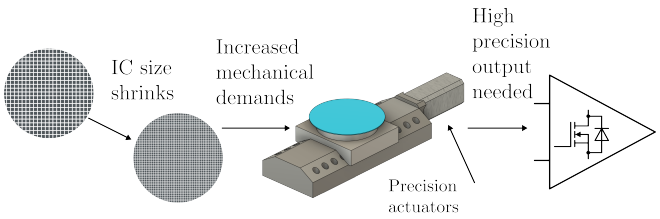


Fig. 1. Changing requirements for wafer and semiconductors have a knock-on effect on all components in the systems.

Such a high bandwidth can be challenging for switched-mode power converters to achieve. Therefore, linear power amplifiers are sometimes preferred due to their inherent low noise and large bandwidth, but they suffer from lower efficiency and consequently lower power output capability. The increasing demand for output power (to increase force and acceleration), low noise, and high bandwidth [2], [3], [5] has caused a push for high-performance digital, switch-mode amplifiers. These amplifiers are already employed in industry to drive semiconductor stages due to their high power density, high efficiency, and lower cost [1]. However, due to their switching nature, they suffer from non-linearity and inherent distortion. This makes adhering to these requirements challenging. Therefore, the amplifier must also rely on a filter to minimise the impacts of these imperfections. Using classical single-level switched-mode amplifiers, the LC filters needed can be quite large. However, this can be improved by either increasing the switching frequency or taking a multilevel approach [6]. A major source of distortion in switched-mode amplifiers is the dead-time required in between the switches to prevent shoot-through on a switching branch [7]. This causes an error in the output voltage of the converter. While power


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amplifiers for these systems usually rely on output current control to directly drive the actuators, the output voltage error still impacts the output current through the load impedance. While a multilevel system does not directly address the issues of dead time, it can lower its impact on it. Furthermore, GaN switches can be used as they have shorter dead-time requirements due to the minimal capacitances in the switch, and can also be pushed to a higher switching frequency. With this work, the goal is to unite theory with practice by designing a high-bandwidth power amplifier based on a multilevel flying capacitor converter.

## II. Flying Capacitor Multilevel Inverter design

As mentioned before, a multilevel power amplifier can be used to reach the demanding requirements for semiconductor manufacturing. The flying capacitor converter functions using floating capacitors charged to different voltages. These capacitors are connected in different configurations to generate the different output voltage levels. More details on the working principles of these converters can be found in [8], [9] and [10].

TABLE I
Power amplifier specifications

| Specification | Value |
|---|---|
| Output voltage | ± 300 V |
| Output power | 1 - 3 kVA |
| Output frequency | DC - 10 kHz |

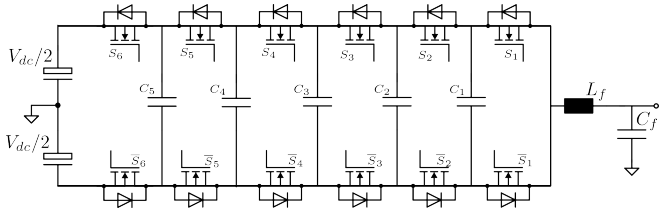


Fig. 2. 7-level flying capacitor circuit

The voltage stress on the individual switches is determined by the voltages of the flying capacitors:

$$V_{sw,k} = V_{c,k} - V_{c,k-1} \tag{1}$$

Where the voltage on the flying capacitors is determined by:

$$V_{c,k} = \frac{kV_{dc}}{n-1}. \tag{2}$$

Here, $k$ is the location of the capacitor in the topology, and $n$ is the number of levels of the converter. Using (1) and (2), the voltage stress on the switches can be simplified to:

$$V_{sw} = \frac{V_{dc}}{n-1} \tag{3}$$

The switch voltage for a 7-level topology combined with the specifications from Table I determines the switch voltage to be 100 V per switch. Note that (3) assumes that the voltage of the capacitors does not vary and is stable. In reality, this is not always the case and will be investigated in the following subsection.

### A. Simulation and capacitor balancing

An important detail of flying capacitor converters is the balance of said capacitors. As demonstrated before, the voltage of the capacitors determines the voltage stress on the switch. Therefore, the capacitors must remain balanced in accordance with (2). There are two ways to deal with this issue: one way is to implement a voltage sensor in each capacitor bank and actively balance the system [11], or one can rely on the natural voltage balancing that occurs in flying capacitor converters [12]–[14]. For this application, the natural balancing method is chosen to keep the hardware design simple and the control overhead low. To verify the capacitor self-balancing, a PLECS-based simulation is developed. The required capacitance per level can be determined in the following way:

$$C_{fc} = \frac{dQ}{dV} = \frac{i_l}{2\delta_v V_{dc} f_{sw}} \tag{4}$$

Where $i_l$ is the total load current, $f_{sw}$ is the switching frequency per switch, and $\delta_v$ is the normalised allowed voltage ripple. In this design, the minimum required capacitance for a ripple of 1.6667 % or 10 V at a switching frequency of 100 kHz at full load. The output voltage in the simulation is seen in Fig. 3. The 7-level distinct output levels can be observed, in conjunction with the filtered output at peak output voltage and load. The capacitor voltage balance at this same load condition

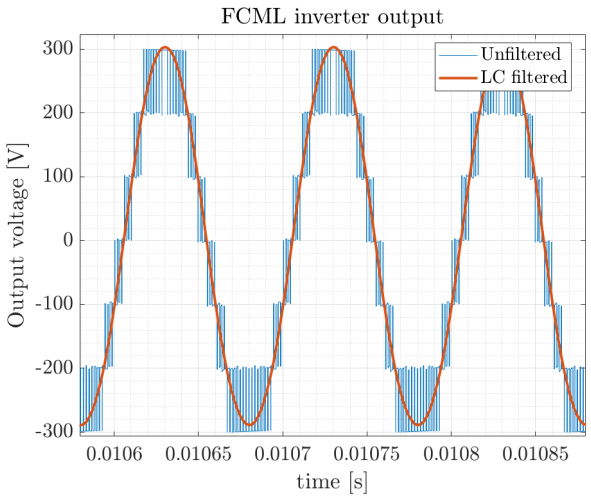


Fig. 3. Simulation output at 10kHz and full load.

can be seen in Fig. 4.

From this figure, it can be seen that the capacitor voltage does vary over a fundamental period, but it is well within the 10 V allowable ripple, as designed. While this may seem conservative, the simulation does not account for all parasitics in the real converter.

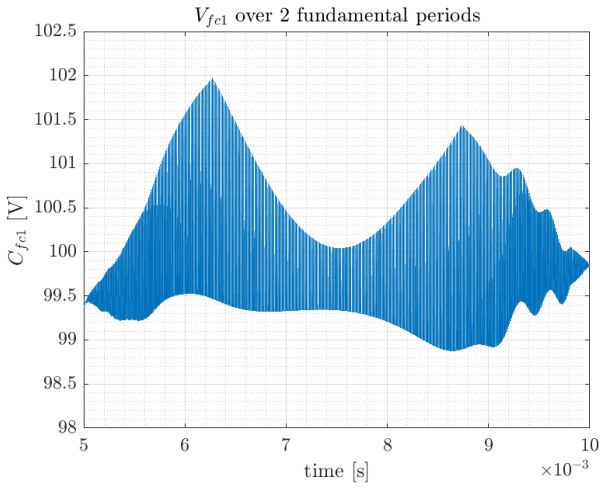


Fig. 4. Flying capacitor 1 ($C_1$ in Fig. 2) voltage balance over a fundamental period.

### B. GaN FET selection

As mentioned, the theoretical switch voltage will be 100 V for a 600 V output, assuming the voltage balance to be relatively stable as demonstrated. Therefore, lower voltage GaN switches can be used to increase the performance of the amplifier due to their higher figure of merit (FOM) compared to their higher voltage counterparts or Si(C) devices [15]. Increasing the number of levels beyond 7 will lower the blocking voltage further, but at a higher design complexity and component cost. The FOM of different switches is compared in Table II based on the following equation:

$$\text{FOM} = (Q_{gd} + Q_{oss})R_{ds,on} \tag{5}$$

Where $Q_{gd}$ and $Q_{oss}$ are the gate-drain and total output charges and $R_{ds,on}$ is the typical on-state resistance of the device. This calculation has been done for various numbers of GaN switches ranging from 650 V down to 100 V from different manufacturers as seen in Table II.

TABLE II
GAN FOM COMPARISON, LOWER FOM IS BETTER

| Device | Voltage [V] | $Q_{GD}$ [nC] | $Q_{oss}$ [nC] | $R_{DS(on)}$ [mΩ] | FOM |
|---|---|---|---|---|---|
| LMG3522 | 650 | 2.9 | 100 | 43 | 4.38 |
| LMG3100R017 | 100 | 2 | 77 | 1.7 | 0.1343 |
| IGC033S10S1 | 100 | 2.8 | 43 | 2.4 | 0.109 |
| GANE3R9-150QBA | 150 | 3.5 | 130 | 3.7 | 0.49 |
| EPC2307 | 200 | 2.5 | 58 | 7.2 | 0.43 |
| EPC2304 | 200 | 2 | 120 | 3.5 | 0.43 |
| EPC2308 | 150 | 1 | 50 | 4.5 | 0.29 |

From this table, it is clear that lower voltage switches have significantly better FOM compared to higher voltage devices. However, as the per-switch voltage will be 100 V due to the 7-level topology, it is prudent to use a device rated for more than 100 V for device safety and longevity. Therefore, a 150 V or 200 V switch should be used. For possible further development, the required output voltage may increase up to 800 V, thus the choice is made to use 200 V devices. Looking back at Table II, there are 2 options available, both from EPC. The EPC2304 [16] and EPC2307 [17] both meet the requirements for this project and have the exact same footprint and are thus interchangeable. For cost and availability reasons, the EPC2307 is chosen for this project.

### C. LC filter component selection

As high THD and low SNR are desirable for this system, an LC filter needs to be designed. To do this, a design space-based approach will be used based on the following inequalities [18]:

- Corner frequency:

$$LC \leq \frac{1}{(2\pi k_f f_{o,max})^2} \tag{6}$$

  Where $k_f$ is the ratio between the corner frequency of the filter and the maximum output frequency. To avoid resonance at the maximum output frequency, the corner frequency of the filter is moved away from this point.
- Output voltage ripple:

$$LC \geq \frac{1}{32\Delta V_c((n-1)f_{sw})^2} \tag{7}$$

  Here, $\Delta V_c$ is the allowable voltage drop, $n$ is the number of levels and $f_{sw}$ is the switching frequency of one switch. This equation determines the maximum product of filter values for a given maximum output voltage ripple.
- Transient voltage drop:

$$L_{min}(C) \leq C(\frac{\Delta V_{drop}}{I_{trans}})^2 \tag{8}$$

  where $V_{drop}$ is the maximum voltage drop due to a transient current and $I_{trans}$ is the maximum transient current. When the output current is required to change suddenly, the output voltage drops in proportion to the filter values and the transient current. This can cause an unacceptable drop in output quality and thus needs to be limited
- Inductor current ripple:

$$L \geq \frac{V_o}{4(n-1)^2 f_{sw}\Delta I_L} \tag{9}$$

  Here, $V_o$ is the output voltage and $\Delta I_l$ is the maximum current ripple. The maximum current ripple needs to be limited as well to keep the output current quality within the requirements.

With these equations, a design space with feasible component values can be generated. The effectiveness of combinations can then be investigated using the previously described PLECS simulation. The design space variables can be found in Table III.

From this, a design space is generated, and a value is selected after simulation. The results of this design space can be seen in Fig. 5

TABLE III
LC-FILTER DESIGN VARIABLES

| Design variable | Value |
|---|---|
| $n$ | 7 |
| $f_{sw}$ | 100 kHz |
| $f_{o,max}$ | 10 kHz |
| $\Delta V$ | 0.5 % |
| $k_f$ | 8 |
| $\Delta V_{drop}$ | 10 % |
| $I_{trans}$ | 5 A |
| $\Delta I_L$ | 20 % |

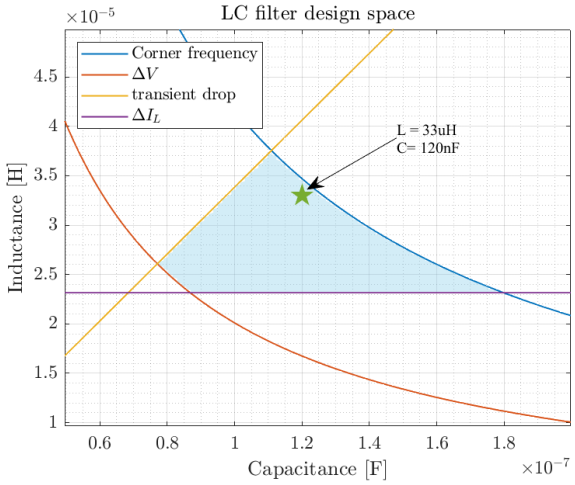


Fig. 5. LC-filter design space

The selected values of 33 µH and 120 nF are partially chosen because they are standard values and therefore have a wider range of options from manufacturers. In simulation, these values lead to a THD of -39dB dB. One should note that these values for an LC filter are relatively small due to the multilevel nature of the power amplifier.

### D. Power amplifier design

One important point when designing with GaN switches is the limited voltage headroom between the recommended gate-source voltage and the absolute maximum rating of the device [15]. This rating, in combination with GaN's ability to have a high switching frequency at high currents, means that it is important to keep the parasitic inductances of the design to a minimum to avoid damaging the switch by way of excessive overshoot. To achieve this, a low inductance vertical layout is adapted from [19]. Except in this design, the switches and capacitors are not separated into smaller boards, but are directly placed on a 6-layer printed circuit board (PCB), which has the integrated isolation and gate-driving circuitry. The GaN switches used are EPC2307 [17] 200 V switches with a $R_{ds,on}$ of 7.2 Ω.

To increase the power density of this converter, multilayer ceramic capacitors can be used. It should be noted, however, that these types of capacitors suffer from capacitance de-rating under DC voltage bias. Therefore, the flying capacitor

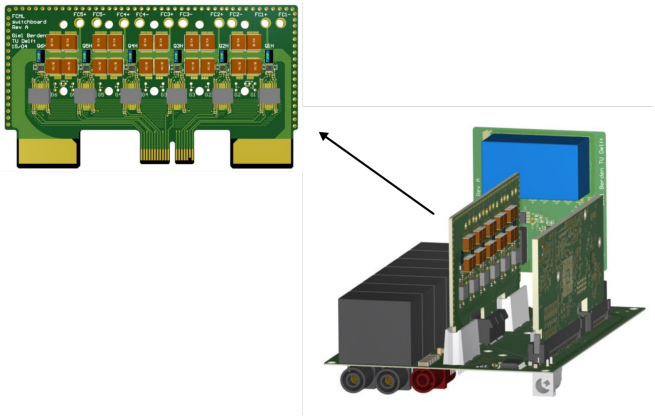

Fig. 6. PCB view of the power amplifier.

cells are comprised of parallel and series-connected capacitor banks, which can either be left unfilled for the lower voltage cells or be fully populated in case of the higher voltage cells. Furthermore, the whole system is designed to use PCIE connectors and cards to connect to a motherboard where the power inputs and outputs and the DC-link capacitor bank are located. While this is not optimal for the power density in $\mathrm{kW\,L^{-1}}$, it facilitates a semi-modular approach where different configurations of multilevel converters can be tested using the same motherboard. Similarly, the LC-filters can be swapped out for different setups, for instance, adding more filter orders. The power amplifier is controlled by a TI C2000 ControlCARD [20], also utilising a PCIE slot.

## III. HARDWARE DEMONSTRATOR AND EXPERIMENTAL RESULTS

The designed power converter is shown in Fig. 7. The figure shows the switch module consisting of six GaN switches on each side. On the right side, the filter board is shown.

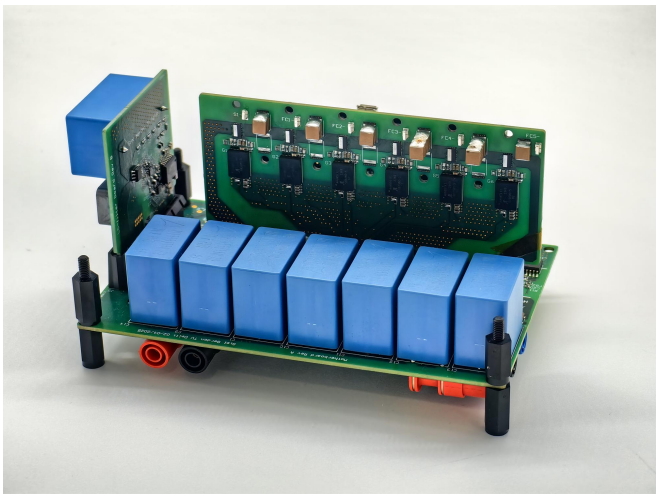

Fig. 7. Designed power amplifier prototype.

First, the capacitor balance at peak output power is studied, so the stability of the converter can be determined. The results of this are found in Fig. 8.

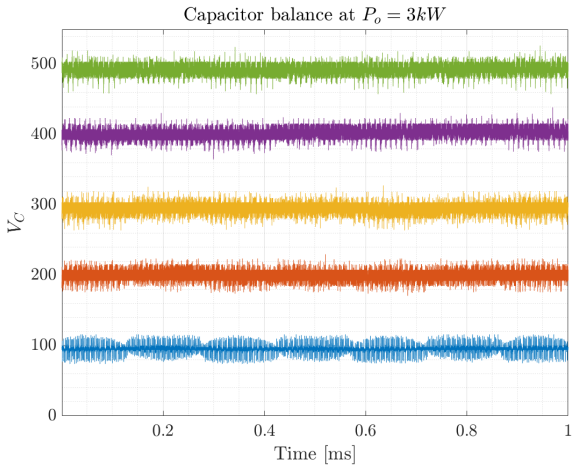


Fig. 8. Capacitor balance under peak load at $f_o = 500Hz$. Measured using Keysight N2791A differential probes

From this figure, a high-frequency ripple can be observed, which has the same frequency as the switching cells. Here, the worst-case ripple is $\pm$ 10V from the nominal voltage. However, over a fundamental output frequency, the balance of the capacitors only shows a 7V ripple, which is within the designed maximum. Next, the THD is measured over a range of varying operating points. It should be noted that during all of these measurements, the DC bus voltage was kept at 600V, and the converter was controlled in open-loop.

First, the THD in relation to the open-loop frequency is measured and plotted in Fig. 9.

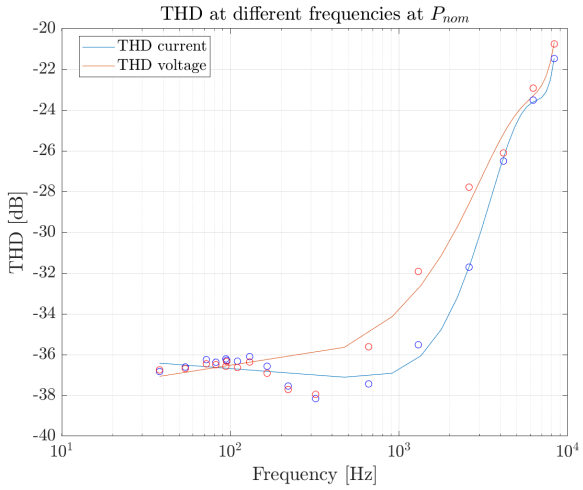


Fig. 9. THD compared to output frequency

The data indicates that the lowest THD occurs around 350Hz, with a THD value of -38dB. As the frequency rises, the THD increases as well. Several factors contribute to this phenomenon. One significant factor is the reduced time the converter spends at each discrete switching level. When this duration nears the switching frequency of each cell, the relative modulation resolution deteriorates. This deterioration happens because there are fewer switching periods available to produce the desired waveform, causing the ratio $\frac{f_{s,mod}}{f_o}$ to approach one. Consequently, this leads to heightened harmonics and noise at lower frequencies, which the filter struggles to attenuate effectively [21], [22]. Although the higher effective switching frequency mitigates this effect to some extent, hardware constraints limit the PWM modulators to a 100kHz update rate. Additionally, the reduced modulation resolution introduces nonlinear distortion sources, such as increased quantisation noise.

Next, the relation between THD and output current is investigated. These results can be seen in Fig. 10. The data

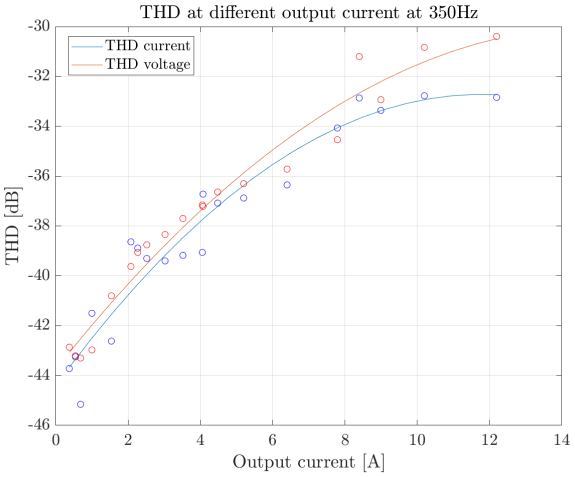


Fig. 10. THD compared to output current

reveals that THD rises with increasing current. This trend aligns with expectations, as the impact of dead-time is less significant at lower currents, and less energy is dissipated in parasitic components. Additionally, the flying capacitors exhibit lower voltage ripple, enhancing the quality of the output voltage waveform. As the current increases, the ripple on the capacitors and at the output also grows. Higher currents result in increased dI/dt, which in turn amplifies harmonics. Moreover, at currents exceeding 10A, the filter inductor begins to saturate, reducing its filtering efficiency.

The converter is designed to operate in closed-loop using the output voltage as the control variable. The control is done by a PI controller. The results of this are plotted in Fig. 11 From this, it becomes clear that there is significant distortion on the output and the output voltage sensor. The noise is likely coupling to the sensor due to improper filtering, which in turn is amplified by the controller.

## IV. Conclusion

This article shows the design of a high-bandwidth power amplifier for an electromagnetic actuator application. The

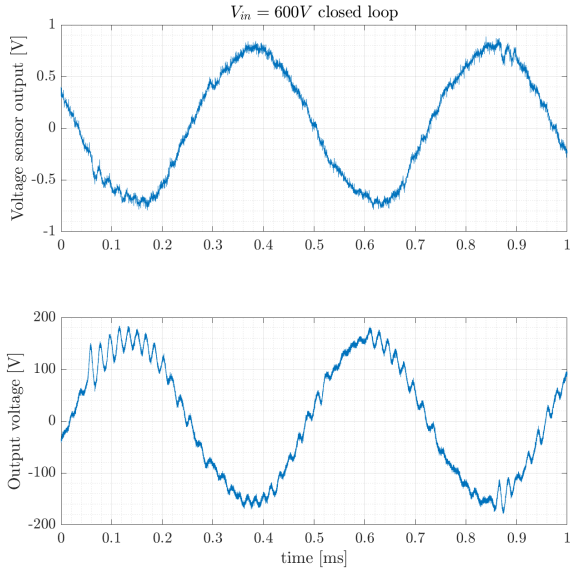


Fig. 11. Closed loop voltage output results

simulation results show that the converter can generate a 10 kHz sine wave as output.

Thereafter, the criteria for selecting GaN switches are given. Various switches with different voltage and current ratings are compared. The results show that the switches with lower voltage have better figure of merit in general.

Thereafter, the design space for the LC filter is defined, and appropriate components are selected. The selection is not only dependent upon the current output but also on the bandwidth requirement of the power amplifier.

Lastly, the power amplifier design is presented, and results are discussed. From these results, it is shown that the amplifier shows performance following the simulations and shows low THD. However, the closed-loop performance is poor and needs to be improved.

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