Radio frequency energy harvesting and low power data transmission for autonomous wireless sensor nodes

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RADIO FREQUENCY ENERGY HARVESTING AND LOW POWER DATA TRANSMISSION FOR AUTONOMOUS WIRELESS SENSOR NODES

RADIO FREQUENCY ENERGY HARVESTING AND LOW POWER DATA TRANSMISSION FOR AUTONOMOUS WIRELESS SENSOR NODES

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K. C. A. M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op dinsdag 22 november 2016 om 12:30 uur

door

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To my wife Juliana and my parents

Andre Luis Rodrigues Mansano

PREFACE

Using my intuition is how I came to write this thesis. I know it seems unreasonable for somebody in engineering to rely on intuition. All the work done in this thesis follows the principles of engineering, exact science and a little bit of intuition. However, why did I decide to face the challenges of a PhD if I used to have a good job in my native country? My intuition told me that I had to explore new territories and new subjects to be successful in my life. This is how I came to do a PhD and eventually to write this thesis.

Andre Luis Rodrigues Mansano
Delft, September 2016

CONTENTS

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INTRODUCTION

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1.1. BACKGROUND

The Internet of Things (IoT) and Wireless Sensor Networks (WSN) have gained significant importance in the electronics industry since these subjects have been introduced. The IoT is a promising application that is dedicated to the communication among electronic devices and the WSN is a network consisting of two or more electronic sensors, defined as nodes, that communicate with each other and to a central hub, without wires. Currently, WSN is considered to be the most favorable way to implement IoT since it does not require cables for communication. Therefore, a simple infrastructure can be deployed. A simple example that illustrates the importance of WSN for the electronics industry is described as follows. Imagine that in a supermarket the temperature of the food in the refrigerators needs to be monitored. Wireless sensors that monitor temperature can be installed in the food package and these sensors will communicate to a central hub that processes and stores the collected information. Since food and package are produced at a very large scale, a large number of electronics has to be produced to satisfy the demand of package suppliers. This example of IoT shows how WSN is a good opportunity to further increase the electronic industry as WSN may require large amounts of devices.

Since most WSN's require a large number of electronic devices, those devices must be cheap and low cost. Today's electronic solutions applied to WSN's are expensive and have high maintenance costs since they require batteries as the main source of energy. In many cases the price of the battery itself is larger than the price of the electronic device. Moreover, the maintenance costs associated with the replacement of batteries and to process the battery waste - more than a million ton of waste is produced per year in Europe as shown in Figure 1.1 - explain the high costs of current solutions. Furthermore, battery supplied sensors are not suitable to applications that require monitoring of areas where human access is very limited.

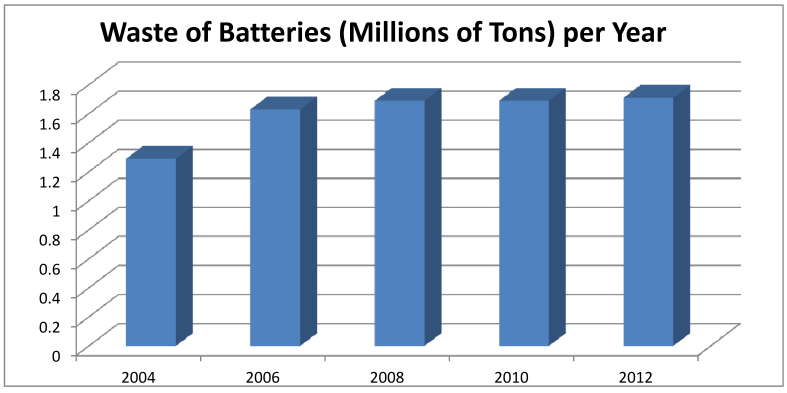

Figure 1.1: Waste of battery per year in Europe. [1]

1.2. CHALLENGES

The most appropriate solution to minimize the costs of wireless sensors and maintenance of the network is to eliminate the use of batteries. Since we want to avoid battery usage, the devices deployed in the WSN have to be energy autonomous, i.e., the sensors must sustain themselves with a source of energy that is available from the environment. Therefore, collecting energy from the environment and converting it into electrical energy (voltage and current) is necessary. The process of collecting and converting energy to the electrical domain is known as Energy Harvesting (EH). An example of energy harvesting is a solar cell that collects light energy and transforms it into electricity. Also, it is possible to collect energy from vibration, flow, temperature and electromagnetic fields such as radio frequency waves (RF). Besides the implementation of the EH, the electronic circuits should also consume less power than current solutions, which will contribute substantially to the realization of energy autonomous wireless sensors.

Most implemented wireless sensors have the same building blocks that are depicted in Figure 1.2. From the diagram we can point out three main blocks that are directly related to energy autonomous operation: the processor, the energy harvester and the (wireless) communication. The processor is intended to process information provided by the sensor and forward it to the memory and wireless communication. The memory is necessary since the data has to be stored and the bitstream has to be synchronized before data transmission. The data processing also consumes power and reducing the power consumption is challenging, however required for autonomous operation.

Most of current solutions usually deploy solar cells or thermal generators as energy harvesters [2, 3] but these sources of energy are not always available in the environment. An alternative is an RF energy harvester (RFEH) that uses a dedicated RF source that remotely provides energy to the sensor. However, existing RFEH's have low power conversion efficiency (PCE). Therefore, improving efficiency of RFEH's is a challenge that has to be faced.

The third major challenge is the wireless communication that often requires high levels of power for data transmission and reception, which prevents autonomous operation of the wireless sensor. Besides the challenge on electronics design, an additional challenge in wireless communication is related to antenna efficiency and interface with environment [4].

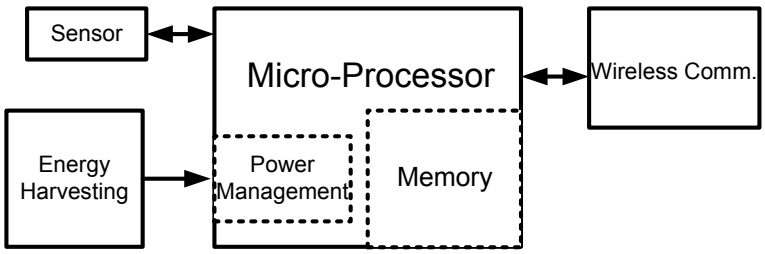

Figure 1.2: Block diagram of a generic wireless sensor.

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1.3. AIM AND THESIS OUTLINE

The aim of this work is to develop new techniques for and the design of energy autonomous wireless sensor nodes with reliable data communication. In order to achieve these goals, we focus on three main aspects: first, the system operation is analyzed and discussed with respect to power consumption; second, radio frequency (RF) energy harvesting is examined and a new solution is proposed to improve the power conversion efficiency. Finally, a new low-power wireless data transmission scheme is presented. Analog signal processing is not the main focus of this work. However, an analog front-end implementation is described as it is part of the autonomous ECG wireless sensor presented in this thesis. The thesis is organized as follows:

- Chapter 2 is dedicated to a review of classical and state-of-the-art wireless sensor node systems and circuits. In this chapter, current solutions at system level, RF energy harvesting and data transmission are presented and discussed.

- In Chapter 3 a new topology for RF energy harvesting is presented, analyzed and experimental results are shown. This chapter gives information about power conversion efficiency and sensitivity that are essential to the design of the autonomous wireless sensors presented in Chapters 5 and 6.

- Chapter 4 is dedicated to the analysis of data transmission and presents techniques to reduce the power consumption of wireless data transmission preserving reliable communication. A new technique is presented to encode Level Crossing ADC data into a single pulse for data transmission. In the second part of the chapter a low-power low-voltage sub-GHz ultra wide band transmitter circuit is analyzed and its implementation is presented.

- In Chapter 5, the implementation of an autonomous wireless sensor node with temperature monitoring is presented and discussed. In addition, the chapter presents the implementation of a receiver (Rx) front-end used to receive the signal transmitted by the implemented wireless sensor. The Rx LNA specification and filter are defined taking into account an estimation of the link budget. In addition, the analog back-end of the receiver is presented. The receiver measurement results are also shown in this Chapter.

- In Chapter 6, an autonomous wireless ECG sensor is presented and discussed. The system topology is presented as well as the building blocks with measurement results and comparisons to previously published works. In this chapter the measurements of the asynchronous data transmission proposed in Chapter 4 are presented as well.

- Chapter 7 concludes the thesis. A summary of all chapters is presented to collect the most relevant information of the work developed in this thesis and its outcomes. In addition, recommendations are made for future work based on the developments presented in this thesis.

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State of the Art Review

This chapter reviews relevant published works that are cited in this thesis and have inspired the development of the works presented in the following chapters. The state of the art will be presented followed by a discussion about its advantages and disadvantages. The review focuses on three different types of circuits and systems. First, the most relevant charge pump rectifier topologies for RF energy harvesting are presented and discussed. Second, impulse radio UWB low power transmitters are discussed with a focus on transmitters designed to operate in the sub-GHz and 3-10 GHz bands. Finally, state of the art wireless sensor node topologies for remote monitoring of slowly varying signals are presented and discussed.

2.1. RF ENERGY HARVESTING

RF Energy Harvesting (RFEH) is an important building block of wireless sensor nodes as it provides power to the sensor circuitry. Typically the RFEH is consisted of a matching/boosting network and a rectifier, or charge pump rectifier. The matching network is the interface between the antenna and the electronics where reactive components are used for impedance transformation. Most of the cases the components of the matching network have to be tuned at a specific frequency and therefore a matching network calibration is highly recommended to optimize matching and efficiency of the RFEH as described in [1]. This section focus in the state of the art review of charge pump rectifier topologies. Rectifiers are very well known as power conversion circuits that convert alternating current (AC) to direct current (DC). In the beginning of the 20th century, rectifiers were usually applied to high-voltage and high-power applications. The same principle of rectifying current and voltage can be applied to RF energy harvesting, where rectifiers convert AC power, captured by an antenna, to DC power that is subsequently delivered to a load. Generally, the rectified voltage is also boosted to achieve higher voltage levels. Thus, the rectifier also operates as a charge pump, and for this reason the term charge pump rectifier (CPR) is commonly found in RFEH literature. An example of a CPR is presented in Fig. 2.1. This is one of the simplest CPR topologies, as it comprises only diodes and capacitors. In the positive half-period of a sinusoidal voltage applied across the anode-cathode junction, the diode conducts current and thus transfers charge to the capacitor connected at the cathode terminal, which stores this charge, thereby increasing its DC voltage. Since the circuit has two diodes, the voltage is rectified in both semicycles. The diode can be seen as a switch with a voltage source (V_D) in series. The equivalent circuits in both half-periods are represented in Fig. 2.2. The diodes have losses, represented by V_D, that limit the CPR output voltage and, consequently, the power conversion efficiency (PCE). The steady-state output voltage of this topology is described by (2.1), where V_{IN} is the input peak voltage.

$$V_{OUT} = 2V_{IN} - 2V_D, \tag{2.1}$$

As can be noticed from (2.1), V_D is an undesired factor and has to be minimized for better power conversion. Various techniques and topologies that have been developed to reduce V_D, increase the PCE and the sensitivity of CPRs will be briefly discussed in this section.

A Schottky diode is a special type of diode built on a metal-semiconductor substrate,

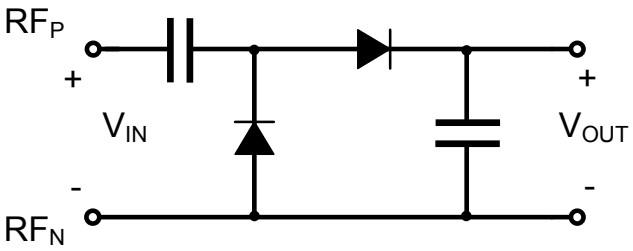


Figure 2.1: Diode capacitor CPR topology (single stage).

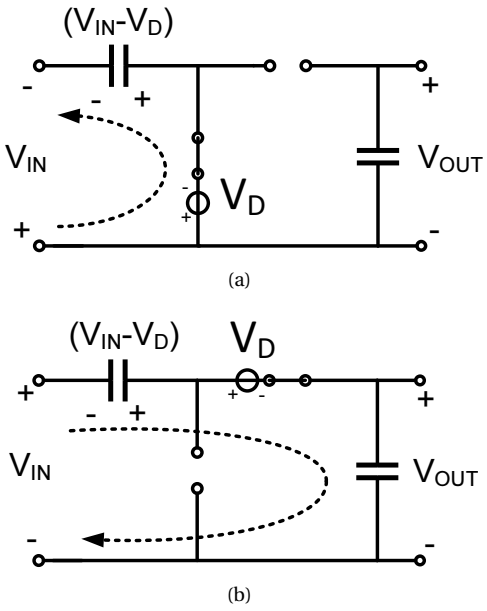


Figure 2.2: Equivalent circuit in negative (a) and positive (b) half-period.

which has a low V_D (0.15V - 0.4V) [2, 3]. One approach is the replacement of conventional diodes, in the circuit of Fig. 2.1, by Schottky diodes. The significant change is in the reduction of diode voltage drop. The advantage of diodes is that they conduct current in one direction only, thus, no flow-back current losses are associated with the use of diodes in case the CPR receives high voltage levels. The main drawback of Schottky diodes is their manufacturing cost. Therefore, these diodes are not always available in CMOS technologies or their use adds to the costs considerably.

Due to the costs and processing disadvantages of Schottky diodes, many research groups have been looking into solutions to reduce CPR losses using standard CMOS processes. An integrated CMOS rectifier has a clear advantage over discrete Schottky diodes as MOS transistors can easily be scaled and have four terminals compared to two terminal diodes. This allows for a much more versatile design approach with many different topology and circuit techniques to design for optimum rectifier efficiency. The CPR in Fig. 2.3(a) replaces diodes by MOS transistors connected as diodes. However, MOS transistors also present a voltage drop, which depends on the threshold voltage (V_{TH}) of the MOS transistor. For this reason, techniques to reduce the threshold voltage have been developed. A known technique is floating gate threshold voltage compensation [4]. This technique consists of MOS transistors connected as diodes with a capacitor connected between the drain and gate terminals. Assuming the initial voltages on these capacitors are zero, before operation, the capacitors must be charged with a voltage close to V_{TH}. After that, the diode connected transistors will have their conduction losses reduced since the capacitors work as series voltage sources, as shown in Fig. 2.3(b), and

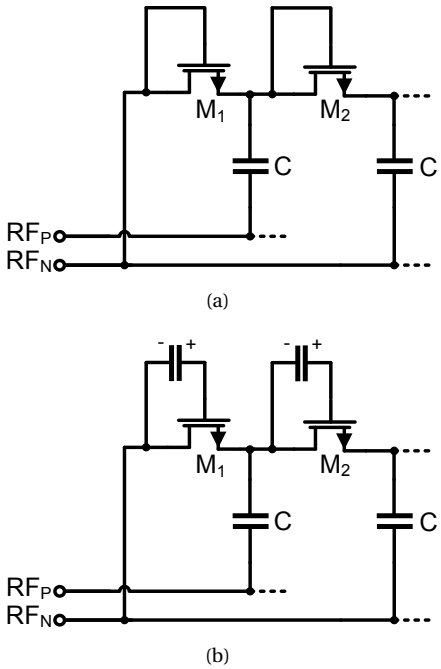
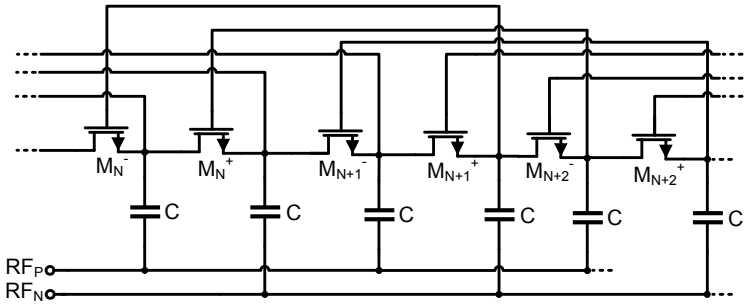


Figure 2.3: (a) diode connected MOS stages (b) diode connected MOS stage with floating gate technique.

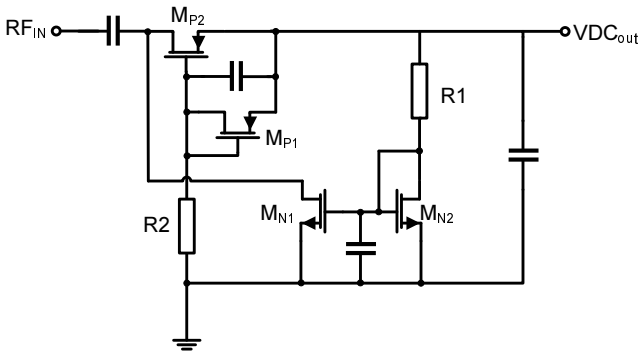
thus drive the gates with higher voltages. The extra voltage allows the transistor channel to be inverted with lower gate-source voltages, thereby minimizing V_{TH} effects.

The advantages of this topology are good V_{TH} compensation and simple circuit implementation. On the other hand, the pre-charging of the capacitors needs to be accurate in order to avoid excessive extra potential, which can lead to negative turn-on voltages. As a consequence, losses due to flow-back current become very significant. Moreover, pre-charging requires a battery, thus making this technique unattractive to truly autonomous solutions.

Other techniques for V_{TH} compensation are presented in Fig. 2.4 (a)-(c) [5–7]. In Fig. 2.4(a) the compensation relies on the output voltages of the succeeding stages that are fed back to the compensated stage [5]. This method does not require pre-charging of the gates and the circuit implementation has moderate complexity. However, it requires a large amount of stages to provide enough voltage for compensation. In the technique presented in Fig. 2.4(b) the threshold voltage of MN1 is reduced by a biasing circuit [6]. MN2 conducts a current that is limited by R1 and a gate-source voltage is produced across MN2. The gate-source voltage of MN2 sets a lower turn-on voltage to MN1. For MP2 the threshold compensation is similar as for MN1. This technique also requires a large amount of stages and it needs extra components, such as transistors, resistors and capacitors, to build the compensation scheme. In both approaches, flow-back current may also increase losses at high input power.



(a)



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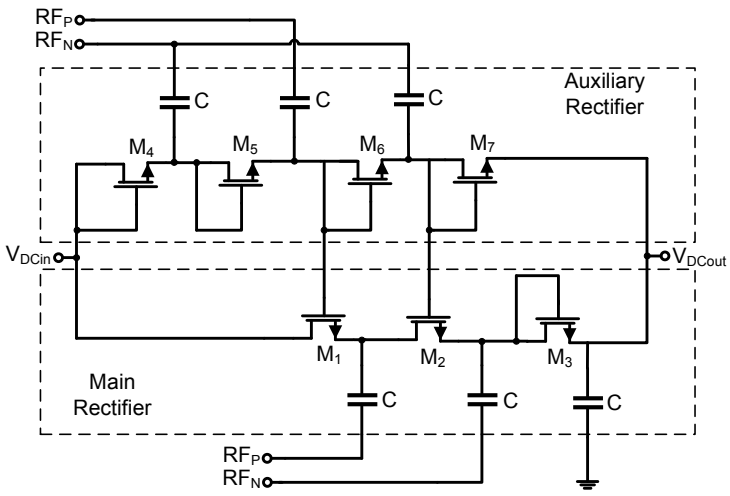

(c)

Figure 2.4: (a)-(c) static V_{TH} compensation techniques [5–7].

Fig. 2.4(c) shows a technique that employs an auxiliary CPR chain for V_{TH} compensation [7]. The compensation is very effective, but chip area is significantly increased and the received power is divided between the main and the auxiliary chain. The charge pump rectifier concepts presented in this section are the basis for the RF energy harvesting scheme that is presented in Chapter 3. Moreover, the RF energy harvesting is part of the integrated systems that have been developed and are presented in Chapters 5 and 6.

2.2. UWB TRANSMITTER

Impulse radio (IR) UWB communication has been used for wireless communication for the first time many decades ago but it became very attractive since the 2000's when the Federal Communication Commission (FCC) in the U.S. allowed its use in unlicensed bands, from 3 to 10 GHz and sub-GHz (up to 950 MHz). Most of the research in Ultra Wide Band circuits and systems focused on high speed data transmission and high accuracy localization. All these works explored the UWB 3-10 GHz band as several sub-bands of 500 MHz can be used in this band. The sub-GHz band, on the other hand, has not been used extensively since only one 500 MHz sub-band is available for communication. Fig. 2.5 shows the block diagram of a UWB transmitter for the 3-10 GHz band that has been employed by [8–10], however with different circuit techniques. The transmitter comprises a baseband pulse generator, a very high frequency (3-10 GHz) local oscillator (LO), a mixer, a power amplifier (PA) and an antenna.

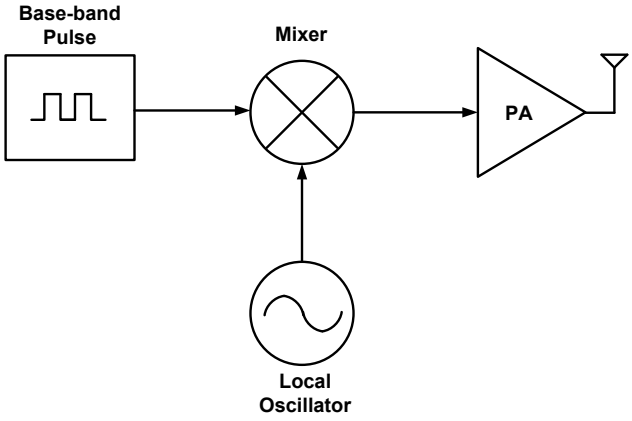

Figure 2.5: Block diagram of a UWB transmitter with local oscillator.

In the topology of Fig. 2.5 typically the generated base band pulse has a bandwidth of 250 MHz (roughly from DC to 250 MHz) as the UWB communication channel bandwidth should be at least 500 MHz wide. Subsequently, the generated pulse has to be up-converted to the desired sub-band for data transmission. This task is attributed to the mixer that up-converts the base-band pulse to the center frequency of the communication channel. However, the mixer typically cannot drive the antenna directly. For this reason, a power amplifier (PA) stage is placed between the mixer and the antenna to buffer the signal and transmit the maximum EIRP allowed by the (FCC) regulation (-41.3 dBm/MHz). The biggest advantages of this topology are the well controlled center frequency of the pulse and the well controlled power that is emitted by the PA, which means that the transmitted signal is easily made compliant to the regulatory mask and communication channel. On the other hand, it has a high power consumption (hundreds of micro-watts to several milli-watts) to generate very high frequencies and guarantee high linearity of the power amplifier. In addition, the mixer has to provide a very high isolation from the LO to the PA and base band pulse generator. In case of LO leakage, a significant narrow band component is transmitted and the maximum EIRP can be vio-

lated, which means that a high level of interference might disturb systems that operate in the same frequency range.

Another UWB transmitter topology, shown in Fig. 2.6, includes a pulse generator, a band-pass filter and a power amplifier. In this topology the generated pulse has a bandwidth that is typically wider than 500 MHz. In case of data transmission within the 3-10 GHz band, the pulse bandwidth can be in the order of several GHz. For sub-GHz operation the pulse bandwidth is typically 1 GHz wide and it is generated by means of digital cells and delay cells. For instance a trigger signal (an edge) can be compared to its delayed version to generate a single pulse with a time duration equal to the delay time. The generated pulse is subsequently "shaped" to the right band by means of the band-pass filter that succeeds the pulse generator. Passive filters are the most commonly used in such an implementation and due to its low driving capability, a PA is needed to drive the antenna. In recent works [11–15] the pulse "shaping" is done in the pulse generator to avoid the use of a high order filter and reduce losses in the signal path.

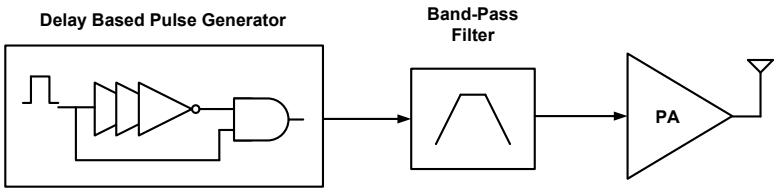

Figure 2.6: Block diagram of UWB transmitter without signal mixing.

The advantages of the topology shown in Fig. 2.6 are lower power consumption, since no local oscillator is needed, and that the PA has to compensate only for small losses of the passive band-pass filter. Moreover, no mixing is implemented, which means that no narrow band components might be transmitted due to leakage. This topology is recently used in low power implementations targeting wireless sensor nodes. The main disadvantage of such an implementation is the high dependency on the performance of the delay cells and the IC technology. To generate an ultra-wide band pulse the technology has to offer very high speed transistors. Moreover, the delays strongly depend on process since they are directly related to the mobility and gate oxide of the transistor.

Since the focus of this work is to implement circuits that can operate from very low power, the solution presented in Chapter 4 is inspired by the topology shown in Fig. 2.6.

2.3. WIRELESS SENSOR NODE FOR SLOWLY VARYING SIGNALS

Low power sensor node design recently has become very attractive to the industry since it allows for implementation of wireless sensors to build a wireless sensor network for remote measurement of quantities. In many cases, physical and medical quantities are converted to the electrical domain and are very sparse in time and vary at a low rate. The speed of signal processing and data transmission required for slowly varying signals are not hard to achieve, which opens the opportunity to minimize power consumption and consequently deploy autonomous solutions. Fig. 2.7 presents the block diagram of state of the art autonomous wireless sensor nodes. Typically, current works implement a single band solution, which means that the same RF signal is used for data communication and energy harvesting [16–18]. In some implementations two distinct frequency bands are used to separate the data link and the energy harvesting link and to benefit from the distinct properties of these different frequency bands [19–22]. In addition, more efficient antenna and antenna interface can be implemented [23]. The sensor as shown in Fig. 2.7 operates in a synchronous fashion controlled by a clock signal (CLK). The quantities to be measured are converted to electrical signals that are pre-conditioned by an analog front-end (AFE) and converted to bits through an ADC. The ADC is synchronized to the digital processor, memory and transceiver since the converted data has to be processed, stored and transmitted in the proper time frame. The system is powered by means of an energy harvester that converts the incoming RF signal to DC power. In addition, the power management unit provides voltage and current references and regulated voltages to the circuits. Besides the clock reference for data synchronization, a local oscillator generates the RF frequency for up/down conversion of data in the transceiver.

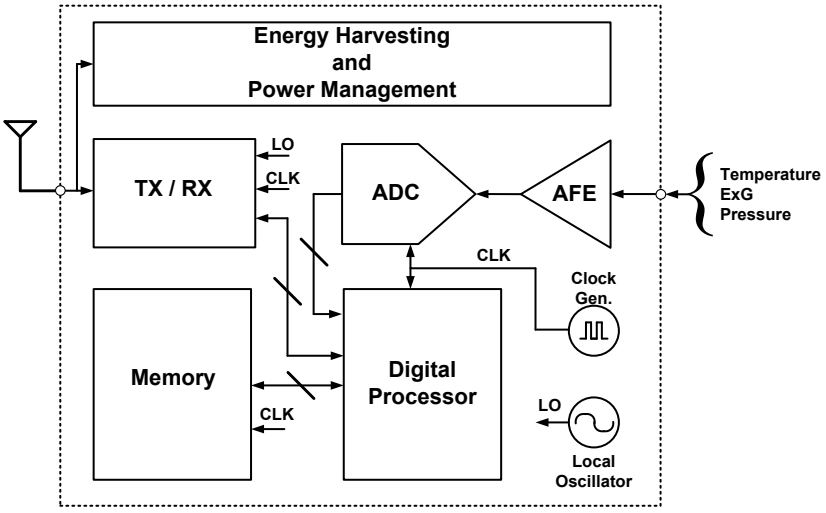

Figure 2.7: Block diagram of state of the art autonomous wireless sensor node.

The advantages of such a topology are compatibility to any type of network since the wireless sensor can receive data from other sensors and store it to send to other sensors or a central hub. The sensor includes memory and a digital processor that allows for en-

cryption of information and support for multi-users access. The main disadvantage is that the power consumption of this topology is still too high for truly autonomous operation. Therefore, the sensitivity of the energy harvester is degraded. Moreover, to keep the power consumption below tens of μW the system requires a power gating technique, which increases the complexity of the system even further. Some implementations use a hybrid solution that combines synchronous and event-driven operation. In this work two design examples of an asynchronous solution are presented, one for temperature monitoring and the other for ECG monitoring based on an event-driven approach that will be detailed in Chapters 5 and 6.

2.4. CONCLUSIONS

In this chapter, the relevant state of the art has been reviewed and advantages and disadvantages has been discussed. The main reviewed topics are RF energy harvesting, UWB transmitter and wireless sensor node for slowly varying signals. In the review of RF energy harvesting, the most relevant charge pump rectifier topologies have been presented and discussed. The UWB transmitter section discussed low power transmitters with a focus on the topologies developed to operate in the sub-GHz and 3-10 GHz bands. Finally, the state of the art wireless sensor nodes topology for remote monitoring of slowly varying signals has been presented and discussed.

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3

RADIO FREQUENCY ENERGY HARVESTING

The design and analytical modeling of a high efficiency energy harvester comprising a passive voltage-boosting network (VBN) and a switching charge pump rectifier (CPR) is presented in this chapter. To improve the power conversion efficiency (PCE), the VBN increases the voltage at the input of the CPR and provides control signals for switching. Unlike traditional Schottky and diode-connected MOS transistor rectifiers, the proposed orthogonally switching CPR (OS-CPR) comprises MOS transistors as voltage-controlled switches. Analytical models for the OS-CPR are developed and presented. Circuit-level optimization techniques are employed to reduce conduction and switching losses. Simulated in a 90nm standard CMOS technology (IBM 9RF), a 5-stage 915 MHz OS-CPR achieves a DC voltage of 1.35 V and a PCE of 11.9% with a 1 MΩ load at -18.2 dBm available input power ($P_{S,AV}$). To show technology scalability of the design, the OS-CPR is also validated using AMS 0.18µm high-voltage (HV) CMOS technology. When benchmarked with traditional rectifiers, the OS-CPR (under similar conditions) achieves a higher PCE and a higher output DC voltage. The OS-CPR is easily scalable to operate over multiple sub-GHz ISM frequency bands.

3.1. BACKGROUND

RF energy harvesting (or simply scavenging energy from radio frequency emissions) has been around for decades, yet only recently have designers begun to unravel its vastly untapped potential: a limitless power source. Broadcasting RF energy to power remote devices is suitable for wireless sensor networks (WSN), RF identification (RFID) and biomedical telemetry applications. In addition, it offers significant advantages over battery-powered solutions (e.g. low operational and assembly costs), amid negligible environmental effects [1–9].

Power originating from RF ambient sources may be unregulated, intermittent and/or small. Thus, in such circumstances it becomes paramount to maximize the power conversion efficiency (PCE) of the energy harvester (i.e., combined efficiency of a voltage-boosting/power matching network and the charge pump rectifier). As many RF systems are designed to operate across multiple ISM bands [10–13] (13.553-13.567, 300-348, 387-464 and 779-928 MHz bands), so should the power conversion circuits.

The energy harvester in this paper comprises a passive voltage-boosting network (VBN) and an orthogonally switching charge pump rectifier (OS-CPR). In turn, the VBN (a series resonant circuit) comprises a loop antenna (viewed as an inductor) tuned to a carrier frequency, f_c, with a tuning capacitor, C_T [14, 15].

The threshold voltage of diodes and diode-connected MOS transistors limits the maximum PCE of a charge-pump rectifier [16, 17], thereby limiting the maximum power delivered to the load, which in turn determines the maximum operational distance of the device. Floating-gate techniques, often used to reduce/cancel the threshold voltage of MOS transistors, require a pre-charge/calibration phase, thus making them unattractive [18]. Designs employing threshold voltage cancelation techniques often present low PCE for high input power levels. In comparison, Schottky diodes (with reduced forward voltage drop) significantly increase the efficiency of the rectifier. However, the high fabrication cost (due to extra masks) associated with Schottky diodes, makes them unaffordable for low-cost solutions [19, 20].

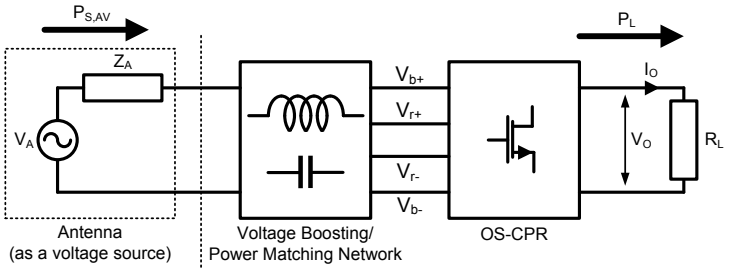


Figure 3.1: Block diagram of the proposed RF energy harvester.

3.2. ORTHOGONALLY SWITCHING CHARGE PUMP RECTIFIER

3.2.1. SYSTEM ARCHITECTURE AND CIRCUIT TOPOLOGY

As in [9, 18, 21], the proposed RF energy harvester comprises a receiving antenna, a voltage boosting/power matching network and a rectifying circuit as shown in Fig. 3.1.

The PCE of the system is defined as,

$$PCE = \frac{P_L}{P_{S,AV}} \tag{3.1}$$

where P_L is the power delivered to the resistive load R_L and $P_{S,AV} = V_A^2/(2\mathrm{Re}\{Z_A\})$ represents the maximum signal power that can be delivered by the antenna to the VBN/OS-CPR.

To adequately drive the OS-CPR, the VBN offers large-swing signals, V_{b+} and V_{b-}, which in turn control the *orthogonal* switching behavior of the rectifier. The resonant circuit of the VBN is modeled by the self-inductance of the antenna, L_A, its series resistance, R_A and capacitance C_T (comprising the sum of the tuning and parasitic capacitances).

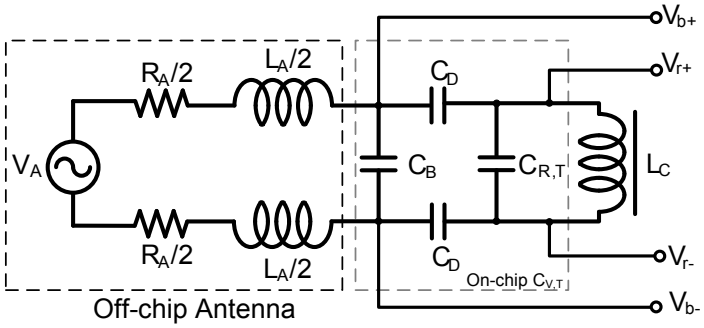


Figure 3.2: Circuit diagram of the voltage boosting network.

As with most charge pump rectifiers [9, 18], flow-back current reduces the PCE. To mitigate this unwanted effect, a capacitive voltage divider limits the maximum input voltage swing (V_{r+} and V_{r-}) applied to the rectifier. The tuning capacitance C_T is

$$C_T = C_B + \frac{C_D C_{R,T}}{C_D + 2C_{R,T}}$$

where C_B denotes the boost capacitance, C_D is the capacitance of the capacitive voltage divider and $C_{R,T}$ is the input capacitance of the rectifier as shown in Fig. 3.2. An inductive choke L_C provides a DC short at the input terminals of the rectifier. This is to ensure a zero DC offset error at the input of the OS-CPR.

Fig. 3.3 presents the rectifier circuitry made up of PMOS transistors as voltage-controlled switches (M_1 and M_2) and capacitors for AC coupling (C_C) and for energy storage (C_{R1} and C_{R2}). To further mitigate flow-back current, parasitic capacitances C_{DC} and resistors R_{DC} set the optimum DC gate potentials of M_1 and M_2. The salient feature of the OS-CPR is its capacity to operate in both weak and strong inversion regions. Further details will be discussed in Section 6.3.

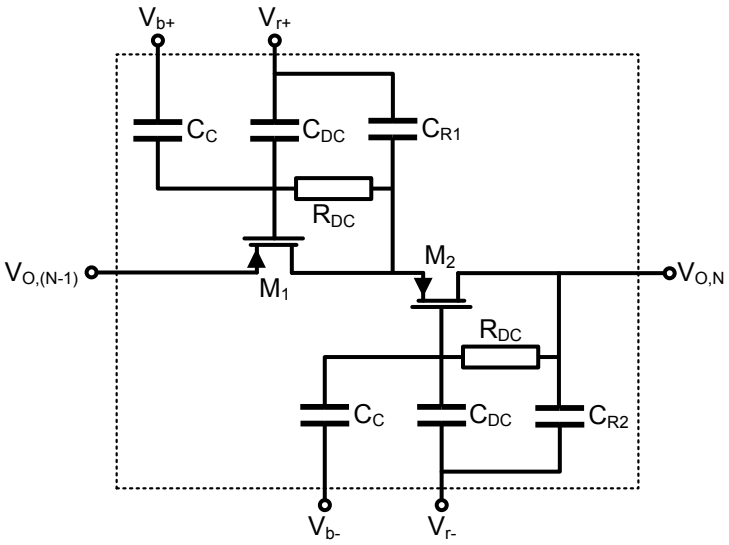


Figure 3.3: Schematic of the orthogonally switching CPR (Nth-stage).

The PCE of an N-stage OS-CPR in terms of its output voltage ($V_{O,N}$) is

$$PCE = \frac{(V_{O,N})^2}{P_{S,AV} R_L} = \frac{(NV_O)^2}{P_{S,AV} R_L} \tag{3.2}$$

where the output voltage (V_O) of a single stage is

$$V_O = 2(V_r - V_{DS,max}) \tag{3.3}$$

and V_r is the input voltage of the OS-CPR, which is defined as

$$V_r = (V_{r+} - V_{r-}). \tag{3.4}$$

In Section 3.3 we will derive the equation for the maximum drain-source voltage ($V_{DS,max}$) of the PMOS transistors (M_1, M_2), thus arriving at the expression for the output voltage of an N-stage OS-CPR.

3.2.2. MODE OF OPERATION

In Fig. 3.3, the differential signal (V_r) applied to the input of the OS-CPR is

$$V_r \approx \left(\frac{C_D}{2C_{R,T} + C_D} \right) V_b \tag{3.5}$$

The differential control signal (V_b) is

$$V_b = (V_{b+} - V_{b-}) \approx QV_A \tag{3.6}$$

where Q is the quality factor of the VBN and V_A is the voltage across the terminals of the antenna. Assuming that $V_{O,(N-1)}$, $V_{O,N}$ and V_{r-} are synchronized, signals V_b and V_r control the switching action of the rectifier as follows.

State 1: When M_1 is ON, M_2 is OFF, $V_{O,(N-1)} > V_{r+}$ and $V_{b+} < V_{b-}$, then C_{R1} is charged to approximately $(2N-1)V_R$. See Fig. 3.4(a).

State 2: When M_1 is OFF, M_2 is ON, $V_{r+} > V_{r-}$ and $V_{b+} > V_{b-}$, then C_{R2} is charged to approximately $2NV_R$, where $2NV_R$ is the output voltage of the N-stage rectifier. See Fig. 3.4(b).

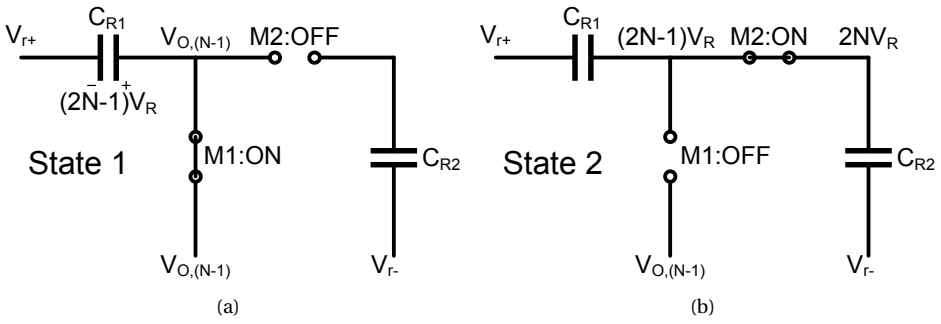


Figure 3.4: State 1 (a) and State 2 (b) of the OS-CPR (N^{th}-stage).

In States 1 and 2, we assume that large signals are present at the gates and sources of M_1 and M_2. This implies that charge is constantly being transferred to C_{R1} (in **State 1**) and C_{R2} (in **State 2**). When operating in the triode (linear) region, M_1 and M_2 experience a lower voltage drop across their drain-source terminals. This minimizes the power dissipation in M_1 and M_2. Compared to the state of the art, the OS-CPR presents higher PCE, especially for lower resistive loads (e.g., < 300 kΩ).

3.3. MODELING AND APPROXIMATIONS

In this section, we use different approximation techniques to derive the expression for the maximum drain-source voltage $V_{DS,max}$ and output voltage $V_{O,N}$ of the OS-CPR in both near and far-field regions.

3.3.1. FAR-FIELD ANALYSIS

In the far field, the PMOS transistors of the OS-CPR operate in the weak-inversion region [22]. In this region, the drain-source current $I_{DS}(t)$ is defined as

$$I_{DS}(t) = I_s \exp\left[\frac{V_{GS}(t) - V_{th}}{nV_T}\right]\left[1 - \exp\left(\frac{-V_{DS}(t)}{V_T}\right)\right] \tag{3.7}$$

where I_s is the product of the aspect-ratio W/L and the weak-inversion saturation current I_{DO}, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, V_T is the thresh-

old voltage of the MOS transistor and n is the subthreshold slope. From (3.7), $V_{DS,max}$ is derived and equals

$$V_{DS,max} = -V_T \ln\left[1 - \frac{I_{DS,max}}{I_s \exp\left(\frac{V_{GS,max}-V_{th}}{nV_T}\right)}\right] \tag{3.8}$$

Note that $V_{DS,max}$ is a function of the maximum gate-source voltage $V_{GS,max}$ and the maximum drain-source current $I_{DS,max}$. $V_{GS,max}$ can be calculated from $V_{GS}(t)$.

$$V_{GS}(t) = \frac{1}{2}[V_O + V_b \cos(\omega t) - V_r \cos(\omega t + \pi)] \tag{3.9}$$

where $\omega = 2\pi/T$ and $T = 1/f_c$. From (3.9), $V_{GS,max}$ becomes

$$V_{GS,max} = \frac{1}{2}(V_O - V_b - V_r) \tag{3.10}$$

To derive the expression for $I_{DS,max}$, we assume that the average voltage across C_{R2} is constant and that the charge Q_D delivered by the PMOS transistor is

$$Q_D = Q_L + \Delta Q_{C_{R2}} \tag{3.11}$$

where $(Q_L + \Delta Q_{C_{R2}})$ is the charge drawn by the load and is equal to $V_{O,N}\,T/R_L$. Thus, charge Q_D is

$$Q_D = \int_{t1}^{t5} I_{DS}(t)\,\mathrm{d}t = \frac{V_{O,N}\,T}{R_L} \tag{3.12}$$

The interval $(t_5 - t_1)$ is the period of conduction of the PMOS transistors and is denoted as Δt. During the period of conduction, the function $I_{DS}(t)$ resembles a triangle with base Δt and height $I_{DS,max}$, as presented in Fig. 3.5. To simplify the analysis, we assume that the integral of $I_{DS}(t)$ over Δt can be approximated by the area under the triangle. In the following subsections, we derive expressions for $I_{DS,max}$ for low and high-ohmic load conditions.

$I_{DS,max}$ FOR LOW-OHMIC LOADS

At instances t_1 and t_5, $I_{DS}(t) = 0$. From (3.12), we can approximate $I_{DS,max}$ by

$$I_{DS,max} = \frac{2\,V_{O,N}\,T}{R_L(\Delta t)} \tag{3.13}$$

Instances t_1 and t_5 are derived from (3.9) when $V_{GS}(t) = 0$.

$$t_1 = \frac{T}{2\pi}\left[\arccos\left(\frac{-V_O}{V_b + V_r}\right)\right] \tag{3.14}$$

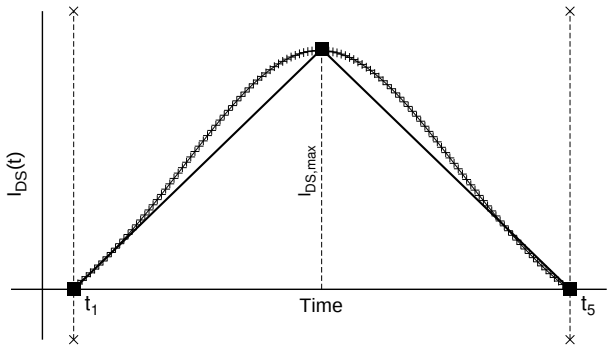


Figure 3.5: The $I_{DS}(t)$ curve and its triangular approximation for the PMOS transistors of the OS-CPR operating in the far field.

$$t_5 = \frac{T}{2\pi}\left[2\pi - \arccos\left(\frac{-V_O}{V_b + V_r}\right)\right] \tag{3.15}$$

To derive the expression for $V_{O,N} = NV_O$, we substitute (3.10) and (3.13) in (3.8) and then (3.8) in (3.3) and solve for V_O. This yields

$$V_O = 2\left[Vr + V_T \ln(1 - K_1)\right] \tag{3.16}$$

where

$$K_1 = \frac{2V_{O,N}}{R_L(\Delta t/T) I_s \exp\left[\frac{1}{nV_T}\left(\left|\frac{V_O - V_b - V_r}{2}\right| - |V_{th}|\right)\right]}$$

Note that the expression for V_O in (3.16) is derived for low-ohmic loads. Now we derive the expression for V_O for high-ohmic loads.

$I_{DS,max}$ FOR HIGH-OHMIC LOADS

In this analysis we use a Taylor series approximation to solve for $I_{DS}(t)$ and derive the expression for $I_{DS,max}$. The 1st-order Taylor series expansion of Q_D in (3.12) is

$$Q_D = \int_{t1}^{t5} [I_1 + I_2 \cos(\omega t)]\, \mathrm{d}t = \frac{\mathrm{V_{O,N}T}}{R_L} \tag{3.17}$$

where

$$I_1 = \frac{I_s V_O}{2nV_T \exp\left(\frac{V_{th}}{nV_T}\right)} \quad \text{and } I_2 = \frac{I_s(V_b + V_r)}{2nV_T \exp\left(\frac{V_{th}}{nV_T}\right)}$$

From (3.17) we derive the expression for $I_{DS,max}$.

$$I_{DS,max} = I_2 + \frac{T}{\Delta t}\left(I_3 + \frac{V_{O,N}}{R_L}\right) \tag{3.18}$$

where

$$I_3 = \frac{I_2}{\pi} \sin\left[\arccos\left(\frac{-V_O}{V_b + V_r}\right)\right]$$

To find $V_{O,N} = NV_O$, we substitute (3.10) and (3.18) in (3.8) and then (3.8) in (3.3) and solve for V_O. This yields

$$V_O = 2\left(V_r + V_T \ln\left(1 - K_2\right)\right) \tag{3.19}$$

where

$$K_2 = \frac{I_2 + \frac{T}{\Delta t}\left(I_3 + \frac{V_{O,N}}{R_L}\right)}{I_s \exp\left[\frac{1}{nV_T}\left(\left|\frac{V_O - V_b - V_r}{2}\right| - |V_{th}|\right)\right]}$$

There are more sophisticated approximants that require more mathematical computations to provide a higher degree of accuracy. These are beyond the scope of this thesis.

3.3.2. NEAR-FIELD ANALYSIS

The orthogonally switching CPR also operates under near-field conditions, where the transistors operate in both the weak-inversion and the strong-inversion region. Fig. 3.6 shows the $I_{DS}(t)$ curve of the PMOS transistors in this case.

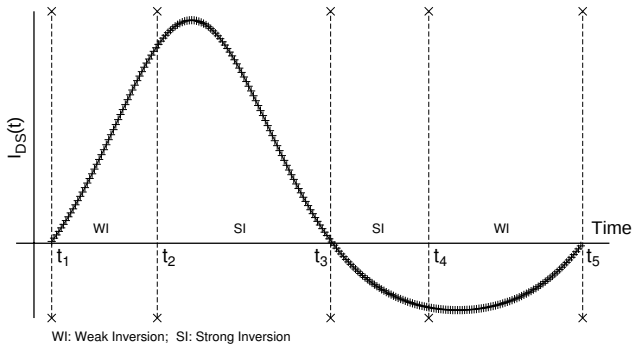


Figure 3.6: The $I_{DS}(t)$ curve of the PMOS transistors of the switching CPR operating in the near field.

Assuming the average voltage across C_{R2} is constant,

$$Q_D = Q_L + \Delta Q_{C_{R2}} + Q_{FB} \tag{3.20}$$

where Q_D is the charge delivered by the PMOS transistors, $(Q_L + \Delta Q_{C_{R2}})$ is the charge $(V_{O,N}T/R_L)$ drawn by the load and Q_{FB} denotes the flow-back current through the PMOS channel. From Fig. 3.6, we can now rewrite (3.20) as,

$$\begin{aligned} Q_D &= \int_{t_1}^{t_2} I_{DS,wi}(t)\,\mathrm{d}t + \int_{t_2}^{t_3} I_{DS,si}(t)\,\mathrm{d}t \\ &= \int_{t_3}^{t_4} I_{DS,si}(t)\,\mathrm{d}t + \int_{t_4}^{t_5} I_{DS,wi}(t)\,\mathrm{d}t + \frac{V_{(O,N)}\,T}{R_L} \end{aligned} \tag{3.21}$$

where $I_{DS,wi}(t)$ (as stated in (3.7)) and $I_{DS,si}(t)$ are the drain-source currents of the PMOS transistors in the weak and strong inversion regions, respectively. $I_{DS,si}(t)$ equals

$$I_{DS,si}(t) = \beta_{si}\left[(V_{GS}(t) - V_{th})\,V_{DS}(t)\right] \tag{3.22}$$

where β_{si} is the beta parameter of the PMOS transistors in strong inversion, which equals $\mu C_{ox}\frac{W}{L}$. The drain-source voltage $V_{DS}(t)$ is

$$V_{DS}(t) = V_r \cos(\omega t) + V_O/2 \tag{3.23}$$

We now derive the equations for the charge delivered to the storage capacitors in each interval. In interval (t_1, t_2), charge $Q_{(t_1,t_2)}$ is given by (3.24). Variables V_A, V_B and V_C are given by

$$\begin{aligned} V_A &= 1/2 V_r (V_b + V_r) \\ V_B &= 1/4(3V_O V_r + V_O V_b - 4V_r V_{th}) \\ V_C &= 1/4(V_O^2 - 2V_O V_{th}) \end{aligned}$$

$$Q_{(t_1,t_2)} = \beta_{si}\frac{(t_2 - t_1)}{2}\left[V_A \cos^2(\omega t_2) + V_B \cos(\omega t_2) + V_C\right] \tag{3.24}$$

$$\begin{aligned} Q_{(t_2,t_3)} = \beta_{si}\Bigg[&(t_3 - t_2)\left(V_A/2 + V_C\right) + \frac{V_A}{4\omega}\sin(2\omega t_3) \\ &- \frac{V_A}{4\omega}\sin(2\omega t_2) + \frac{V_B}{\omega}\sin(\omega t_3) - \frac{V_B}{\omega}\sin(\omega t_2)\Bigg] \end{aligned} \tag{3.25}$$

$$\begin{aligned} Q_{(t_3,t_4)} = \beta_{si}\Bigg[&(t_4 - t_3)\left(V_A/2 + V_C\right) + \frac{V_A}{4\omega}\sin(2\omega t_4) \\ &- \frac{V_A}{4\omega}\sin(2\omega t_3) + \frac{V_B}{\omega}\sin(\omega t_4) - \frac{V_B}{\omega}\sin(\omega t_3)\Bigg] \end{aligned} \tag{3.26}$$

$$\begin{aligned} Q_{(t_4,t_5)} = \frac{I_s}{8(nV_T)^2}\Bigg[&t_5\left(V_D + \frac{(V_b + V_r)^2}{2}\right) + \frac{V_E}{\omega}\sin(\omega t_5) + \frac{(V_b + V_r)^2}{4\omega}\sin(2\omega t_5) \\ &- t_4\left(V_D + \frac{(V_b + V_r)^2}{2}\right) - \frac{V_E}{\omega}\sin(\omega t_4) - \frac{(V_b + V_r)^2}{4\omega}\sin(2\omega t_4)\Bigg] \end{aligned} \tag{3.27}$$

Similarly, the charges delivered to the storage capacitors in intervals (t_2, t_3) and (t_3, t_4) are given by (3.25) and (3.26), respectively. A strong to weak inversion transition occurs at instance t_4. A 2^{nd}-order Taylor series is used to improve the accuracy of the approximation to the charge $Q_{(t_4,t_5)}$ in interval (t_4, t_5) and is given by (3.27). Variables V_D and V_E are defined as

$$V_D = 8(nV_T)^2 + 4nV_T(V_O - 2V_{th}) + V_O^2 - 4V_O V_{th} + 4V_{th}^2$$
$$V_E = 2(V_b + V_r)(2nV_T + V_O - 2V_{th}).$$

In period (t_2, t_4) the PMOS transistors are in the strong-inversion region. The equations for t_2 and t_4 are given as

$$t_2 = \frac{T}{2\pi}\left[\arccos\left(\frac{2V_{th} - V_O}{V_b + V_r}\right)\right] \tag{3.28}$$

$$t_4 = \frac{T}{2\pi}\left[2\pi - \arccos\left(\frac{2V_{th} - V_O}{V_b + V_r}\right)\right] \tag{3.29}$$

At instance t_3, $V_{DS}(t)$ is equal to 0V. Hence, t_3 can be expressed as

$$t_3 = \frac{T}{2\pi}\left[2\pi - \arccos\left(\frac{-V_O}{2V_r}\right)\right] \tag{3.30}$$

We once again substitute the parameters for charge and time instances t_1 through t_5 in (3.21) and collect terms for the output voltage of the N$^{\text{th}}$-stage ($V_{O,N}$) of the OS-CPR operating in the near-field region, producing (3.31).

In the following section, the analytical models of the OS-CPR are verified through simulations using two different sub-micron CMOS processes and measurement results.

3.4. SIMULATION AND EXPERIMENTAL RESULTS

In this section the simulation results and experimental results of the RF energy harvester are presented. The simulations validate the charge pump rectifier modeling, the experimental results prove the energy harvesting concept in an integrated circuit.

3.4.1. SIMULATION RESULTS

The OS-CPR and the VBN are simulated in 0.18μm (HV) and 90nm (RF) CMOS processes (see Table 3.1 for technology characteristics).

We assume an antenna resistance (R_A) of 16 Ω, a value estimated from the trade-off between the size, quality factor and efficiency of the antenna. Equations for the VBN and the models derived in Section 3.3 facilitate the design and optimization of the OS-CPR. The algorithm used for the optimization is described as follows.

Design and Optimization Algorithm of the OS-CPR

1. Calculate the self-inductance ($L_A = R_A Q\omega^{-1}$) and tuning capacitance ($C_T = (\omega^2 L_A)^{-1}$) of the VBN.

Table 3.1: Device Parameters for AMS HV and IBM 9RF

Process	BEOL	Oxide	FET	V_{th}	Capacitor
IBM 9RF	8-Metal	Thin	PFET	-0.22 V	HT-MiM
AMS HV	4-Metal	Thick	PFET	-0.45 V	DM-MiM

2. Calculate the voltage swings of the rectifier (V_r) and control signals (V_b) from (3.5) and (3.6), respectively.

3. Estimate the number of stages (N) from (3.2).

4. Estimate the aspect ratios (W/L) of transistors M_1 and M_2 from the model. Select a C_C capacitance, which has to be bigger than the gate-source capacitance of M_1 and M_2.

5. For minimum ripple, calculate C_{R1} and C_{R2}.

6. Run PSS and PAC simulations.

7. Fine tune C_T and/or the OS-CPR component values for frequency optimization.

8. Repeat steps 3 - 7 for system optimization.

The resulting electrical parameters of the VBN are given in Table 3.2.

Tables 3.3 and 3.4 show the transistor aspect ratios and the component values of the OS-CPR.

$$V_{O,N} = R_L\left[\left(\frac{\beta_{si}}{\pi}\right)\alpha_1 - \left(\frac{I_s}{16\pi(nV_T)^2}\right)\alpha_2\right] \tag{3.31}$$

$$\begin{aligned}\alpha_1 = \Bigg\{ & \frac{1}{4}\left[\arccos\left(\frac{2V_{th}-V_O}{V_b+V_r}\right) - \arccos\left(\frac{-V_O}{V_b+V_r}\right)\right]\left[V_A\left(\frac{2V_{th}-V_O}{V_b+V_r}\right)^2 + V_B\left(\frac{2V_{th}-V_O}{V_b+V_r}\right) + V_C\right] \\ & + \left(\frac{V_A+2V_C}{2}\right)\left[2\pi - \arccos\left(\frac{-V_O}{2V_r}\right)\right] - \left(\frac{V_A/2+V_C}{2}\right)\left[\arccos\left(\frac{2V_{th}-V_O}{V_b+V_r}\right)\right] \\ & + \left(\frac{V_A}{4}\right)\sin\left[4\pi - 2\arccos\left(\frac{-V_O}{2V_r}\right)\right] + V_B\sin\left[2\pi - \arccos\left(\frac{-V_O}{2V_r}\right)\right]\Bigg\}\end{aligned} \tag{3.32}$$

$$\begin{aligned}\alpha_2 = \Bigg\{ & \left[V_D + \frac{(V_b+V_r)^2}{2}\right]\left[2\pi - \arccos\left(\frac{-V_O}{V_b+V_r}\right)\right] + \frac{(V_b+V_r)^2}{4}\sin\left[4\pi - 2\arccos\left(\frac{-V_O}{V_b+V_r}\right)\right] \\ & + V_E\sin\left[2\pi - \arccos\left(\frac{-V_O}{V_b+V_r}\right)\right] - \frac{(V_b+V_r)^2}{4}\sin\left[4\pi - 2\arccos\left(\frac{2V_{th}-V_O}{V_b+V_r}\right)\right] \\ & - V_E\sin\left[2\pi - \arccos\left(\frac{2V_{th}-V_O}{V_b+V_r}\right)\right]\Bigg\}\end{aligned} \tag{3.33}$$

Table 3.2: Parameters of the Voltage Boosting Network

Process	f_c (MHz)	L_A (nH)	R_A (Ω)	C_T (pF)	Q
IBM 9RF	13.56	3000	16	85	16
AMS HV	13.56	8000	16	17	42
IBM 9RF	433.92	165	16	0.8	28
IBM 9RF	915.00	108	16	0.29	38

Table 3.3: Transistor Aspect Ratios (W/L)

Process	f_c (MHz)	W/L
IBM 9RF	13.56	250/0.4
AMS HV	13.56	700/0.2
IBM 9RF	433.92	95/0.5
IBM 9RF	915.00	47/0.5

Table 3.4: Orthogonally Switching CPR Component Values

Process	f_c (MHz)	R_{DC} (kΩ)	C_C (pF)	C_R (pF)
IBM 9RF	13.56	200	5.5	6
AMS HV	13.56	350	8.5	9
IBM 9RF	433.92	200	1	1.2
IBM 9RF	915.00	200	1	0.65

The PCE of the OS-CPR at 13.56 MHz, 433.92 MHz and 915 MHz as a function of the number of rectifier stages for R_L equal to 100 kΩ and 1 MΩ is shown in Fig. 3.7(a) and Fig. 3.7(b), respectively. Beyond a certain number of stages, the PCE decreases because the total voltage drop and the total capacitance (as seen from the input) increase with each additional rectifier stage. Table 3.5 presents the PCE for the optimum number of rectifier stages. Note that all curves with an asterisk are for AMS HV 0.18 μm CMOS.

Table 3.5: PCE and Optimum N for $P_{S,AV}$=-18.2dBm

Process	f_c (MHz)	R_L (MΩ)	N	PCE (%)
IBM 9RF	13.56	0.1/1	4/8	6.7/9.4
AMS HV	13.56	0.1/1	5/5	3.5/11.3
IBM 9RF	433.92	0.1/1	6/6	5/12.7
IBM 9RF	915.00	0.1/1	5/5	5/11.9

Fig. 3.8(a) and Fig. 3.8(b) show the output DC voltage as a function of the available RF input power, $P_{S,AV}$, for an R_L of 100 kΩ and 1 MΩ, respectively. As modeled, the output DC voltage increases with $P_{S,AV}$. Similarly, the PCE as a function of $P_{S,AV}$ for R_L equal to 100 kΩ and 1 MΩ is shown in Fig. 3.9(a) and Fig. 3.9(b), respectively. At high RF input

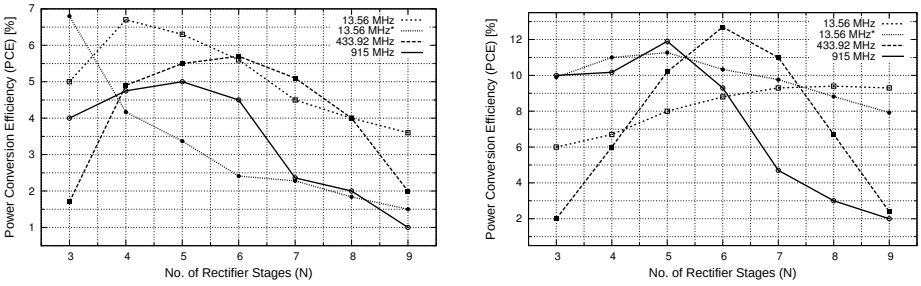


Figure 3.7: Simulated PCE of the OS-CPR as a function of number of rectifier stages. (a) for 100 kΩ R_L and (b) for 1 MΩ R_L at f_c 13.56, 433.92 and 915 MHz, for $P_{S,AV}$ = -18.2 dBm.

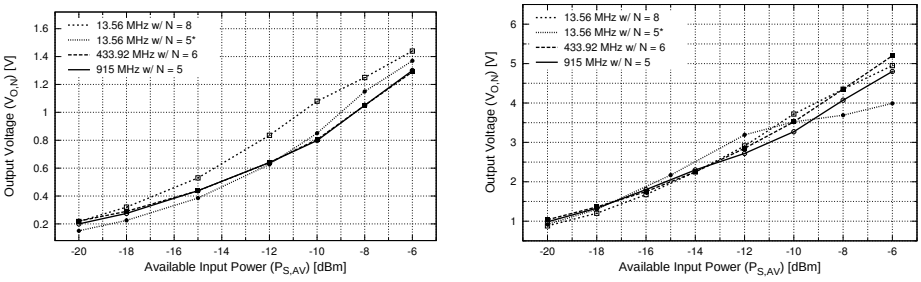


Figure 3.8: Simulated output DC voltage as a function of $P_{S,AV}$, (a) for 100 kΩ R_L and (b) for 1 MΩ R_L.

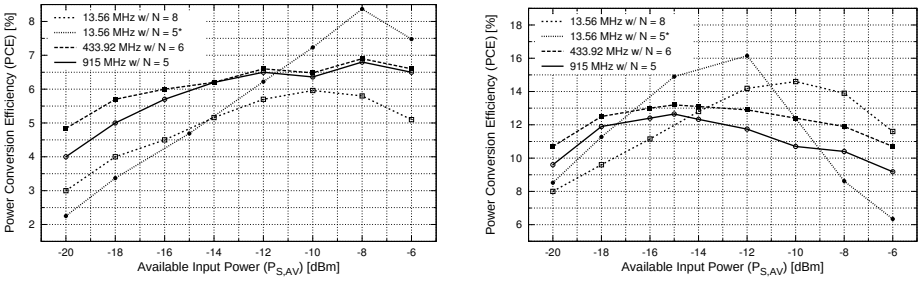
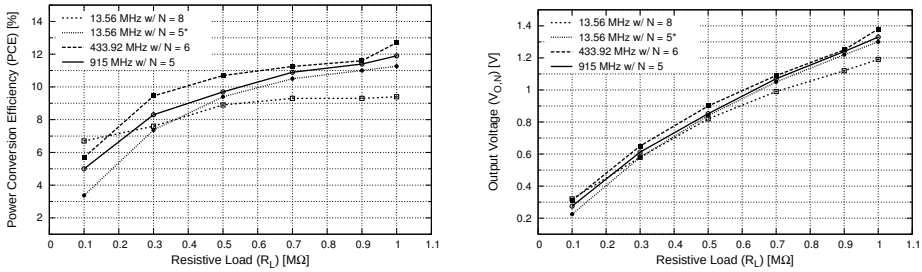


Figure 3.9: Simulated PCE as a function of $P_{S,AV}$, (a) for 100 kΩ R_L and (b) for 1 MΩ R_L at f_c 13.56 MHz, 433.92 MHz and 915 MHz.

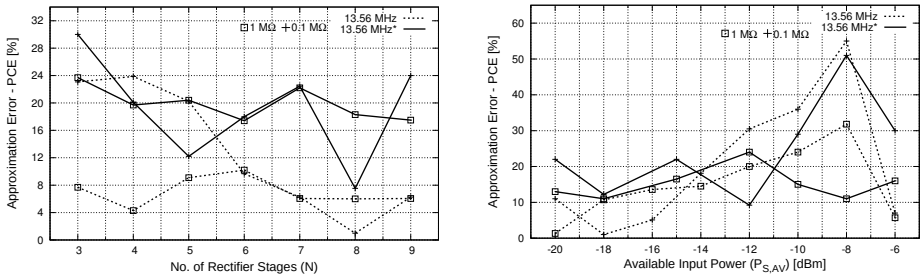
power levels, the PCE decreases because of current flow-back.

The PCE as a function of the resistive load is shown in 3.10(a). Unlike traditional rectifiers, the OS-CPR can operate over a large range (300 kΩ to 1 MΩ) of resistive loads. Fig. 3.10(b) presents the output DC voltage as a function of the resistive load. As modeled



(a) (b)

Figure 3.10: (a) PCE as a function of resistive load and (b) output DC voltage as a function of resistive load for $P_{S,AV}$ = -18.2 dBm at f_c 13.56



(a) (b)

Figure 3.11: (a) Approximation error (PCE) as a function of number of rectifier stages for $P_{S,AV}$ = -18.2 dBm. (b) Approximation error (PCE) as a function of $P_{S,AV}$ for 100 kΩ and 1 MΩ R_L at f_c 13.56 MHz.

in the far-field analysis, the output DC voltage increases with the load resistance.

Fig. 3.11(a) presents the approximation error in PCE (i.e., modeled vs. simulated) as a function of the number of rectifier stages for $P_{S,AV}$ = -18.2 dBm at 13.56 MHz. The peak error in PCE is 29 % for a load resistance of 100 kΩ. This discrepancy of 29 % will reduce with higher-order Taylor series expansions. The approximation error in PCE as function of $P_{S,AV}$ for resistive loads of 100 kΩ and 1 MΩ is shown in Fig. 3.11(b). Note that the peak error in PCE is seen at the transition point from weak to strong inversion mode of operation. Instead of using the weak-inversion model until transition, an analytical model for the moderate inversion regime must be developed. From simulations, we see that the approximation error in PCE as a function of the resistive load (0.1 to 1 MΩ) for $P_{S,AV}$ = -18.2 dBm is 16±4 %.

3.4.2. MEASUREMENT RESULTS

This section describes the measurement results of the RF energy harvester. The circuit that is presented in this chapter has been implemented in silicon using AMS' 0.18μm CMOS IC technology, which is the CMOS IC technology used for all integrated circuits presented in this thesis. In 0.18μm CMOS IC technology, it has been analyzed and concluded that the best efficiency is achieved if the RF energy harvester operates at 13.56 MHz. The low frequency ISM band, compared with higher ISM bands such as 433 MHz and 915 MHz, presents better performance since at high frequencies the parasitic capacitances of the transistors add significant losses. Table 3.6 shows the component values of the designed RF energy harvester for N=5.

As described in Section 3.2 the power conversion efficiency is the ratio between the power delivered to the load and the input power. Although the PCE definition is very clear, the input power can be defined in several ways. In this thesis three definitions of input power are used to present PCE measurement results. The first definition is the theoretical input power ($P_{INtheor.}$), which is the input power defined as $P_{INtheor.} = V_A^2/(2\mathrm{Re}\{Z_A\})$. The second definition is the measured input power at the antenna ($P_{INant.}$). The third definition is the estimated input power at the rectifier circuit (P_{IN}). Most of the references on RF energy harvesting present the power conversion efficiency using P_{IN} as input power definition. Comparing the three definitions, PCE will be the lowest for the $P_{INtheor.}$ since it does not take into account losses in the antenna and loading effects. The highest PCE is seen for an input power P_{IN} that takes into account all the losses in front of the input of the rectifier, therefore P_{IN} is smaller than $P_{INant.}$ and PCE is bigger. For all the measurement results presented in this section, the RF power source at 13.56 MHz is calibrated for a distance of 10 cm (coupling factor of 0.004) between the antenna of the RF source and the antenna of the RF energy harvester. Fig. 3.12 presents the measured output voltage of the RFEH as a function of P_{INant} for $100k\Omega \leq R_L \leq 850k\Omega$. From Fig. 3.12 it can be noticed that the output voltage increases with input power and R_L, which means that a system powered by the RFEH has to operate with very low-power consumption otherwise the sensitivity (minimum input power required for system operation) to the RF source is degraded.

One way of increasing the sensitivity is to increase the power conversion efficiency of the RFEH. Increasing the PCE of the RFEH is not an easy task since the charge pump rectifier is a non-linear circuit that is sensitive to input power and load variations. Fig. 3.13(a) to Fig. 3.15(b) show the PCE behavior as a function of input power for different loads.

One can see that different PCEs are achieved for different loads and input power levels, which indicates that the design of the RFEH strongly depends on the power con-

Table 3.6: RFEH Component Values

Device	Value	Device	Value
C_B	7.5 pF	C_{DC}	≃90 fF
C_D	19.5 pF	R_{DC}	350 kΩ
$C_{R,T}$	≃17 pF	C_{R1}, C_{R2}	9.7 pF
C_C	9 pF	M_1, M_2	750/0.2

sumption of the supplied system and the power received by the antenna. The latter may change due to different coupling factors as a result of variations in distance and/or alignment of antennas.

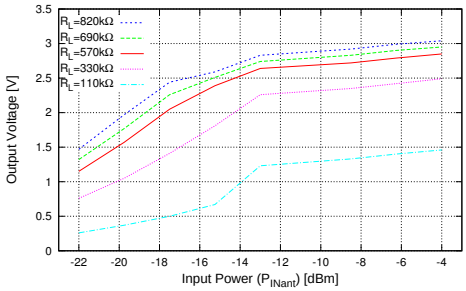
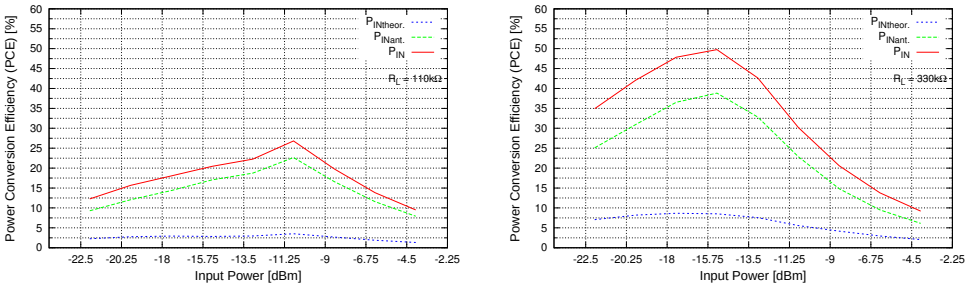
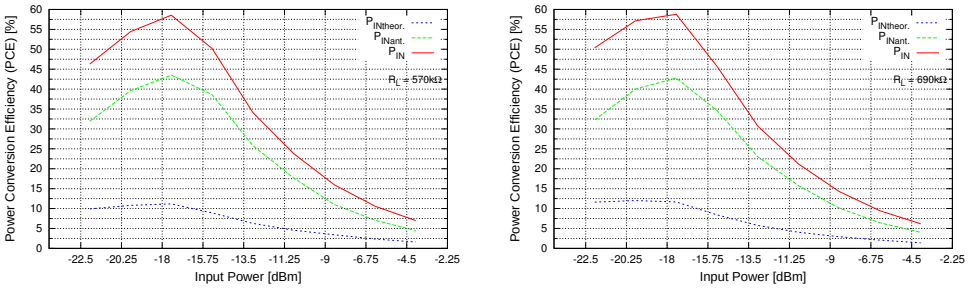


Figure 3.12: Measured output voltage of the RFEH (a) as a function of input power for 110kΩ ≤ R_L ≤ 820kΩ



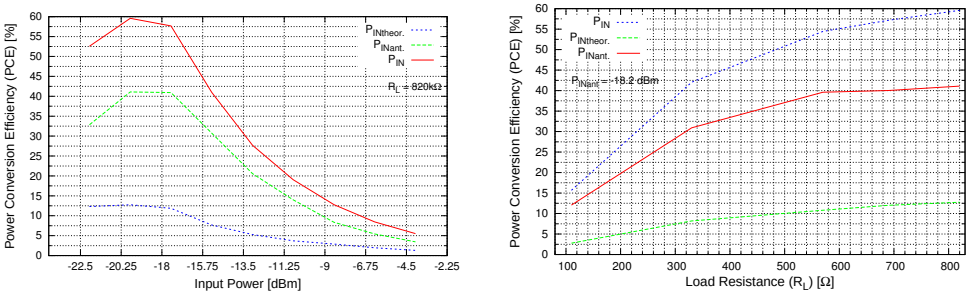
(a) (b)

Figure 3.13: Measured power conversion efficiency of the RFEH as a function of input power for (a) R_L = 110kΩ and (b) R_L = 330kΩ



(a) (b)

Figure 3.14: Measured power conversion efficiency of the RFEH as a function of input power for (a) R_L = 570kΩ and (b) R_L = 690kΩ



(a) (b)

Figure 3.15: Measured power conversion efficiency of the RFEH as a function of input power for (a) R_L = 820kΩ and (b) PCE as a function of R_L for P_{IN} = -18 dBm

The good news is that the more low-power the system is the better is the PCE as shown in Fig. 3.15(b). Concerning input power, the RFEH presents a peak PCE that changes with loading conditions. The lower the input power is, the lower is the voltage to switch on the transistors of the charge pump rectifier. For high input power the transistors may not be completely turned off, which increases flow-back current. In addition, the input impedance of the RFEH changes, which degrades matching with the antenna and therefore the power transferred to the load is not optimum. To optimize matching with the antenna, a control loop is recommended as described in [23].

Table 3.7 compares the OS-CPR to previously published rectifiers in CMOS technolo-

Table 3.7: Summary of the Orthogonally Switching-CPR and Comparison with Previously Published Designs

Specifications	This work	Papotto [9]	Le [18]	Karthaus [19]	Kocer [21]	Mark [23]
Frequency (MHz)	13.56	915	906	869	450	868
Conditions	Standard CMOS	Deep N-Well	Pre-charge Phase	Schottky Diodes	Low-V_{TH}	Control loop
Number of stages	5	17	36	n.a.	16	5
V_{OUT}[§] (V) (R_L = 820 kΩ)‡	2.2	0.9	1.3	n.a.	1.3	2
PCE[§] (%) (R_L = 820 kΩ)‡	40.25	12	8.5	14.5 (at -20.1dBm)	11.2	25
PCE[§] (%) (R_L = 110 kΩ)	13	n.a.	<5	n.a.	n.a.	28
PCE[†] (%) (R_L = 820 kΩ)‡	5	2.25	9.1	n.a.	n.a.	n.a.
PCE (%) (Maximum)	43 @ -17.5 dBm	16.1 @ -15.8 dBm	30 @ -8 dBm	n.a.	16 @ -12.5 dBm	40 @ -17 dBm
Technology (nm)	CMOS (180)	CMOS (90)	CMOS (250)	CMOS (500)	CMOS (250)	CMOS (90)

[§] at $P_{S,AV}$ = -18.2 dBm (far-field region).

[†] at $P_{S,AV}$ = -6 dBm (near-field region).

‡ previous works results are given for R_L = 1 MΩ.

gies. Power conversion efficiency is an appropriate figure-of-merit (FOM) for energy conversion circuits and all reported PCE in Table 3.7 uses P_{INant} as input power definition. First of all it is important to mention that the RFEH implemented in this work can operate at short distances due to low frequency operation while the referred works operate in medium to long distance. Given the results, this work and [23] achieve higher PCE (around 40%)with reduced amount of stages (N=5) compared to the other references due to the fact that voltage boosting technique is employed. Threshold voltage compensation [18] is effective but interface with antenna has also to be optimized. In terms of load adaptability, [23] shows almost flat PCE for wide range of load. Although differences are noticed in the presented RFEH, they have same PCE behavior for wide input power range since the input impedance of the rectifier changes with power. In summary, the RFEH with voltage boosting present better PCE but the PCE is not kept the same for all power and loading conditions if no control loop is implemented.

Besides the previous works cited in the comparison table, more relevant works in RF energy harvesting are published. A dynamic body biasing technique [24] is developed to improve PCE, and hybrid energy harvesting solution that combines solar, vibration and RF energy harvesting [25] is developed. In addition, an ambient RF energy harvesting is developed for flexible wearable wireless sensor devices [26] that is quite relevant for future electronic applications.

3.5. CONCLUSIONS

The design of an orthogonally switching charge-pump rectifier with high power conversion efficiency has been presented. The OS-CPR comprises MOS transistors as voltage-controlled switches. Analytical models and simulation results in 90nm show that a 5-stage 915 MHz OS-CPR with a 1 MΩ load achieves a DC voltage of 1.35 V and a PCE of 11.9% at $P_{INtheor.}$ = -18.2 dBm. Simulations of the RF energy harvester in 90nm and 180nm at 13.56MHz prove that the analytical analysis presents less than 30 % error. Simulation results show that the OS-CPR is both technology and frequency scalable. Measurement results of the RF energy harvester employing a 5-stage OS-CPR designed in 180nm CMOS IC technology have been presented. Three different definitions of input power were presented and included in the power conversion efficiency measurement results. Taking into account the P_{INant} definition, the maximum PCE achieved is 43% at -17.5 dBm input power. This work shows similar PCE compared to [23] as both implementations use voltage boosting technique, however this work is more susceptible to load variations if compared to [23] as no control loop is implemented.

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4

LOW POWER DATA TRANSMITTERS

This work presents an asynchronous event-driven transmitter for wireless ECG sensor nodes. Unlike current solutions for ECG monitoring with autonomous wireless sensors, we propose an asynchronous method to transmit data from an ECG front-end, which is designed with a level-crossing analog-to-digital converter. The 2 output bits (`UD` and `Change`) of the ADC are first combined using a pulse encoder circuit and then transmitted via a backscattering link in the 402-MHz MICS frequency band. The pulse encoder comprises an inverter delay chain controlled by signal `UD`, thereby setting the duration of the pulse.

The design and analytical model of a low-voltage low-power sub-GHz Ultra Wide Band transmitter are presented in the second part of this chapter. Unlike traditional approaches, to maximize peak-to-peak output voltage swing, a series LC network is driven by a voltage pulse. Appropriate pulse shaping is accomplished by a differential-to-single-ended second-order bandpass filter. Analytical analysis is provided and it is validated by circuit and mathematical simulations. Subsequently, the transmitter is designed using off-the-shelf ATF551M4 transistors connected to on-PCB (FR-4) inductors and SMD capacitors. An impulse generator has been implemented to test the proposed low-power transmitter. With a (-10dB) UWB sub-GHz band from 250MHz to 750MHz, the measured energy consumption of the proposed low-power transmitter is 85pJ/pulse for a supply voltage and pulse repetition frequency of 0.15V and 3.3MHz, respectively. Experimental results prove that with the proposed circuit technique a roll-off of 25dB/octave is achieved. The designed transmitter has a ratio between output voltage and supply voltage of 93.3%.

4.1. ASYNCHRONOUS LOW-POWER DATA TRANSMITTER

4.1.1. DESIGN OF ASYNCHRONOUS DATA TRANSMITTER

Wireless body area networks (WBANs) have gained substantial importance in the last few years as remote monitoring of biomedical signals became very attractive to the electronics industry. Moreover, the possibility to integrate WBANs in the internet of things (IoT) is a good opportunity to facilitate and increase the use of telemedicine.

Most of the available solutions are synchronous systems [1, 2] and make use of wireless biomedical sensor nodes (WBSN) that consume large amounts of power, thus requiring batteries or energy harvesting combined with energy storage devices such as super capacitors and rechargeable batteries. The problem is that the batteries and energy storage devices increase the final cost of the sensor rendering it unsuitable for applications in which the sensor is disposable.

An alternative to currently existing solutions is an autonomous WBSN that can sustain itself with energy collected from a remote Radio Frequency (RF) power source without energy storage devices such as super capacitors or rechargeable batteries. Fig. 4.1 shows this concept applied to a WBAN in which the WBSN collects energy provided by the hub and sends back the information requested. The hub is a central unit that sends power to the WBSN in the 13.56MHz ISM band and processes the data provided by the WBSN. The WBSN monitors vital body signs (e.g. temperature and ECG) and sends the data to the hub through a backscattering link in the 402MHz MICS band. In this work the WBSN is equipped with an ECG readout front-end with a level-crossing ADC and a low-power pulse transmitter. The WBSN only transmits data to the hub when the ECG readout detects a level-crossing, which reduces power consumption. Hence, the data transmission is driven by the events generated from the input signal and does not require clock synchronization as it operates asynchronously.

One of the challenges in such a system is that the signal monitoring (analog) front-end needs to provide high resolution data asynchronously. Another challenge is how to transmit the data without pre-processing, storage and synchronization.

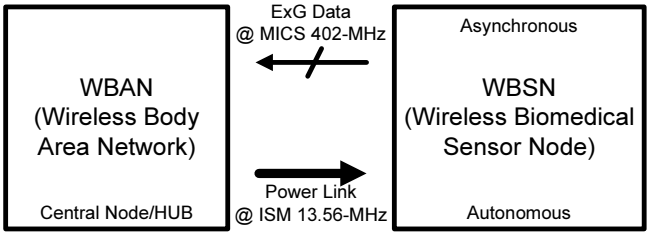


Figure 4.1: Block diagram of a WBAN.

The level-crossing ADC provides 2 binary signals (`Change` and `UD`) that are fed to the low-power data transmitter. As the transmitter is powered by an RF energy harvester [3], to minimize power consumption, the data transmission is only enabled when ADC data conversion is active. The 2 bits provided by the ADC have to be combined and transmitted at once, otherwise information from the ADC is lost. In this section two methods to

encode the ADC data are presented, single pulse mode and multiple pulses mode.

In single pulse mode the 2-bit data stream is combined to generate a pulse with different time duration for upward conversion and downward conversion. This means that the transmitter produces a pulse when `Change` indicates a conversion and `UD` defines the duration of this pulse. In this way 2-bit information can be embedded in a single pulse.

The multiple pulses mode generates a series of pulses when `Change` indicates a conversion. In this case `UD` defines the time duration and number of pulses within one conversion.

The transmitter consists of a digital pulse encoder and a backscattering network. Fig. 4.2 shows the block diagram of the designed pulse encoder. The pulses are generated by comparing `Change` to `ChangeB`, the latter being its complement delayed by six cascaded inverters. The delay time is set by `UD` that makes the pulses longer when it is set to "1". A feedback loop is added to the pulse encoder to implement a 5-stage ring oscillator that is only enabled if `FdbEn` and `Change` are set to "1". The oscillation frequency is defined by `UD` and capacitor C_D.

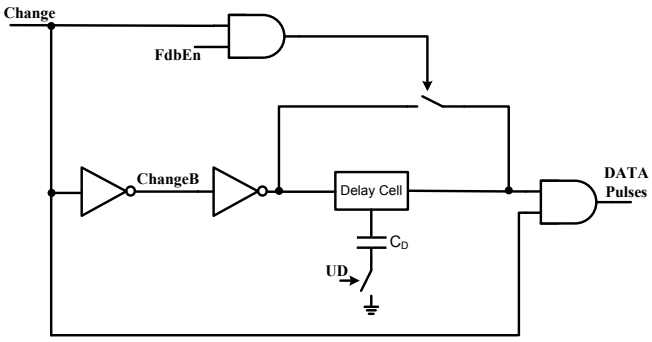


Figure 4.2: Block diagram of the low-power data encoder.

For `UD` equal to "1" (upward conversion) C_D is connected to ground, thus the pulse width is longer. For `UD` equal to "0" (downward conversion) C_D is disconnected from ground, thus the period of the pulses is shorter. This approach might also be used to transmit data with redundancy to improve the bit error rate of the central hub. Fig. 4.3 shows the waveforms of the low-power pulse encoder in two modes of operation.

The first mode is single pulse mode in which the pulse duration equals t_U for upward conversion and t_D for downward conversion. The second mode is multiple pulses mode with period t_{UR} and t_{DR} corresponding to upward conversion and downward conversion, respectively.

Fig. 4.4 presents the circuit designed for backscattering data transmission that is controlled by data pulses through transistor M_1. The pulsed signal implements an on-off-keying modulation of the signal received in the LC network.

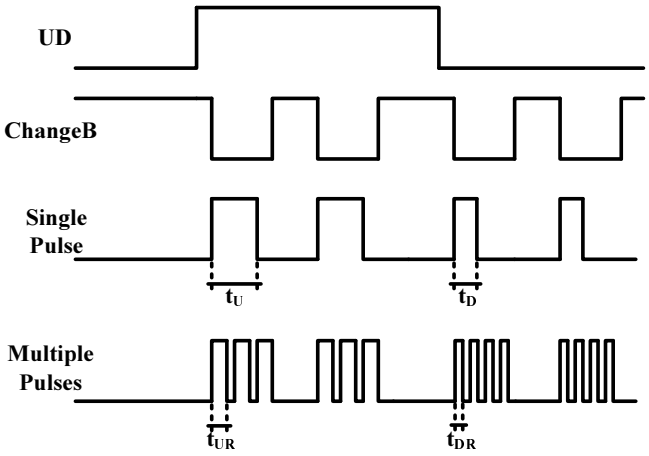


Figure 4.3: Waveforms of the low-power data encoder.

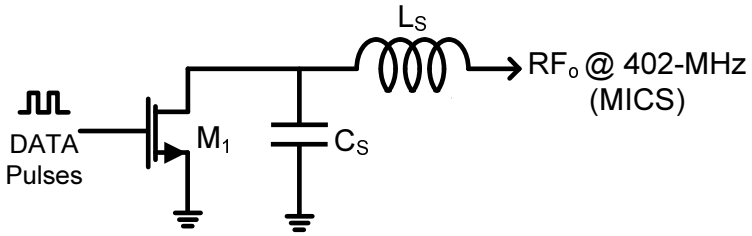


Figure 4.4: Circuit diagram of the backscattering data transmitter.

4.1.2. SIMULATION RESULTS

This section presents the simulation results of the designed asynchronous low-power data transmitter. To test the designed system, a sinusoidal differential 500Hz 10mV peak-to-peak signal is connected to the input of the ECG readout front-end. The selected frequency corresponds to the highest frequency component of an ECG signal.

Fig. 4.5 presents the simulation results of the level-crossing ADC and data encoder. The waveforms show both ADC upward ("UD" is high) and downward ("UD" is low) conversions indicated by UD and Change. Fig. 4.6 shows the data pulse waveforms for (a) UD = 1 and (b) UD = 0.

Fig. 4.7 presents the output current of the backscattering transmitter while data is encoded and Fig. 4.8 shows the power spectral density at the output of the transmitter.

As can be noticed the pulses generate a wide band power spectrum around 402MHz that is 25 dB below the power of the carrier. Therefore, and because of the backscattering employed, the transmitter has a power spectral density that does not generate interference to adjacent MICS channels. The measurement of the asynchronous low-power data transmitter is presented in Chapter 6 as part of the wireless sensor with ECG monitoring developed in this work.

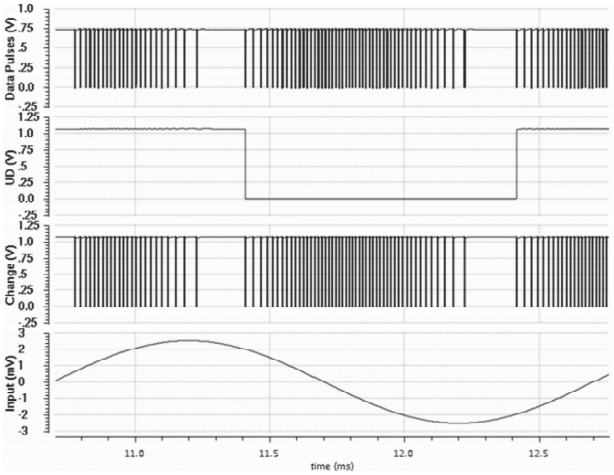
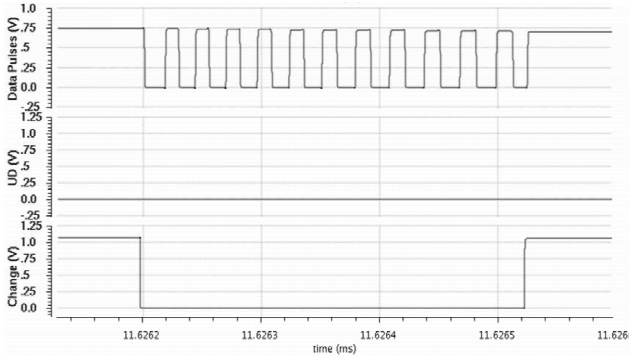


Figure 4.5: Simulated input and output waveforms of the level-crossing ADC and data encoder.

(a)



(b)

Figure 4.6: Encoded data for (a) UD = 1 and (b) UD = 0 in multiple pulses mode.

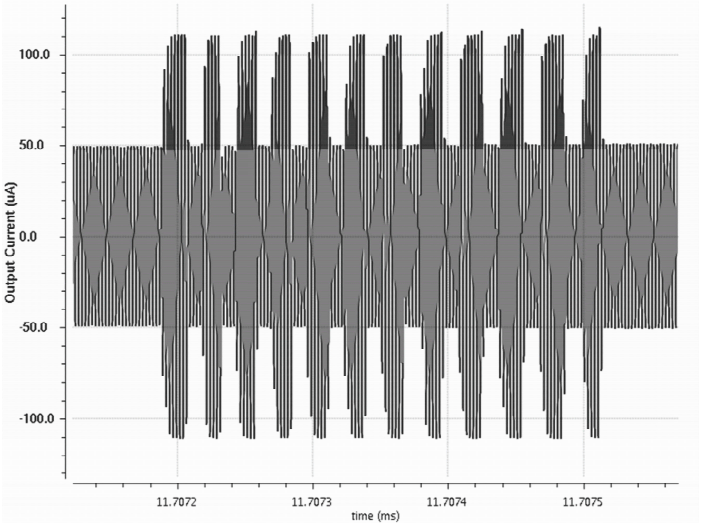


Figure 4.7: Transient simulation of the amplitude modulated 402 MHz carrier for backscattering transmitter in multiple pulses mode and UD = 0.

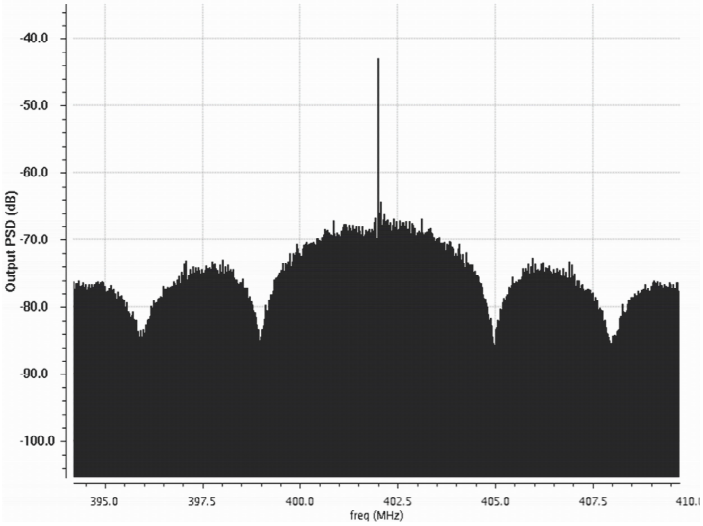


Figure 4.8: Simulated Power Spectral Density of the backscattering transmitter in multiple pulses mode.

4.2. LOW-POWER SUB-GHZ UWB TRANSMITTER

Impulse communication has been around since the 2000's when the Federal Communication Commission (FCC) permitted impulse transmission in two unlicensed bands, 3-10 GHz and sub-GHz (up to 950 MHz) [4]. With the promise to offer both low-power operation and a high channel capacity, impulse radio research efforts have since then been concentrated on the development of transmitters and receivers for ultra-wide band (UWB) communication in the 3-10 GHz frequency range.

Although promising, technical developments of UWB for the 3-10 GHz band have slowed down as the power consumption required for the reception of pulses has turned out to be very high, often too high for portable and, especially, for autonomous wireless sensor applications [5–14].

The use of UWB communication in the sub-GHz band is an alternative solution to reduce power consumption and it appears to be especially attractive for autonomous wireless sensor applications. Moreover, sub-GHz impulse communication can be applied to applications with low data rates (e.g., biomedical signal monitoring) [15, 16], and is suitable for both asynchronous and asymmetrical communication [17, 18].

Though sub-GHz band UWB communication has advantages compared to 3-10 GHz UWB communication, the use of sub-GHz UWB still poses some design challenges. Besides consuming little power and being power efficient, the sub-GHz UWB band high-frequency roll-off at 950 MHz has to be very steep as follows from the FCC mask depicted in Fig. 4.9. This complicates the design of a low-power sub-GHz UWB transmitter.

In this section, a new technique of UWB pulse generation that overcomes the aforementioned challenges is proposed. The circuit description, its analytical analysis and experimental results of the proposed low-power sub-GHz UWB transmitter are presented.

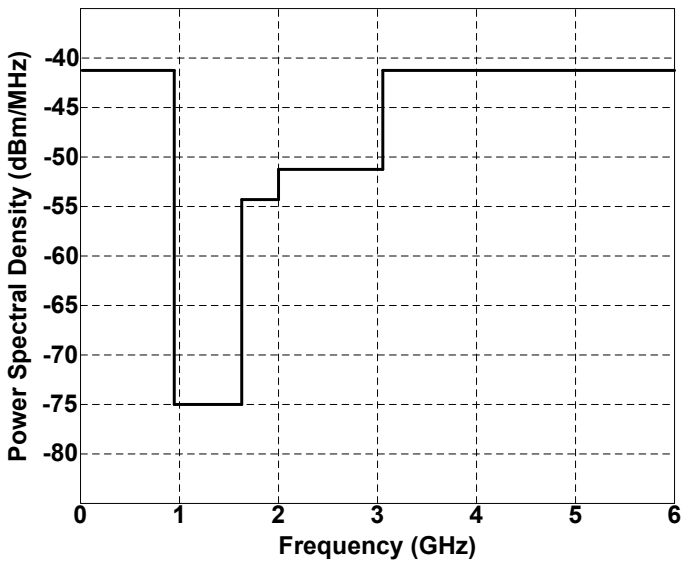


Figure 4.9: FCC regulation mask for UWB transmission.

Fig. 4.10 shows the circuit diagram. Unlike previously published works, the low-power ultra-wide-band transmitter (LPUT) core contains a series LC network, comprising R_S, L and C, which is driven by an impulse voltage source Vip^+. R_S is the series equivalent resistance of the LC network plus the output resistance of the voltage source. Voltage VP^+ and current I_P are coupled into the antenna through capacitance C_L. The antenna impedance, Z_A, is modeled as a resistance, R_A, in parallel with the antenna equivalent capacitance C_A and inductance L_A, as shown in Fig. 4.10. C_A and L_A are included in the antenna model since the antenna has a limited bandwidth, similar to a band-pass filter [19].

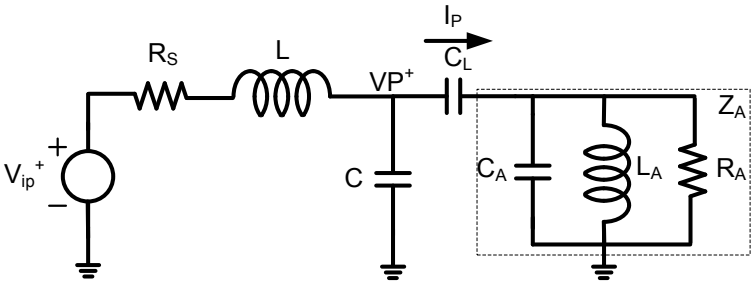


Figure 4.10: Circuit diagram of single-ended input low-power sub-GHz UWB transmitter.

Although the circuit from Fig. 4.10 already generates an UWB pulse, the PSD of VP^+ still contains strong frequency components above 950MHz that couple into the antenna, violating the FCC regulation mask. To generate a pulse that complies with the FCC spectral mask, previous works perform power spectral density shaping by means of a filter [14, 19]. In addition, some designs rely on standard digital cell delays [13, 16]. These methods introduce losses in the transfer function of the pulse shaping network in the transmitter or require high order filters to realize a steep roll-off near 950 MHz.

Fig. 4.11 presents an input differential version of the circuit shown in Fig. 4.10. The circuit has been duplicated and is driven by two impulse voltage sources, Vip^+ and Vip^-. The voltages VP^+ and VP^- have a 180° phase difference as the network is driven pseudo-differentially. The voltage and current signals at the antenna are single-ended since the currents I_P and I_F are subtracted in a single node. Hence, the current at the antenna, I_A, is the difference between I_P and I_F. I_P is generated by VP^+ and I_F is generated by the voltage difference $VP^+ - VP^- = VP_{DIF}$.

The impedance $Z_F = 1/(sC_F)$, ideally, is a short only for high frequency components. A simple qualitative analysis can be made to understand the filtering effect of Z_F; (1) at low frequencies, Z_F is very high, therefore $I_F = VP_{DIF}/Z_F$ is very small. Hence, I_A is not affected by I_F. (2) at high frequencies, Z_F is very low. Consequently, at high frequencies, the difference between I_P and I_F, I_A, becomes very small. This analysis leads us to understand that the upper limit of the PSD depends on C_F, the value of which can be selected to generate a pulse with a PSD that falls within the FCC mask. More details and analysis will be presented in Section 4.3.

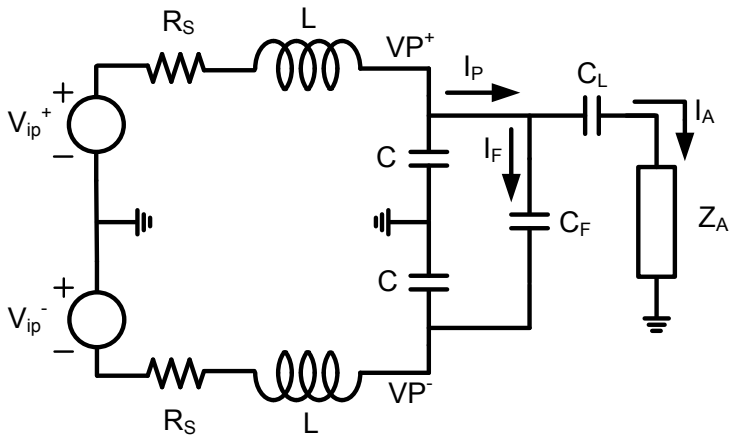


Figure 4.11: Circuit diagram of differential input low-power sub-GHz UWB transmitter.

4.3. ANALYTICAL ANALYSIS OF THE SUB-GHZ UWB TRANSMITTER

In this section, a detailed analysis and model of the low-power sub-GHz UWB transmitter are presented. The aim of the analysis is to derive the voltage across the antenna as a function of the circuit parameters. The voltage across the antenna is defined as,

$$V_A = I_A Z_A. \tag{4.1}$$

The voltage across the antenna depends on variables that are not defined yet, viz. I_A and Z_A, and will be determined in the sequel.

Fig. 4.12 shows the LPUT drawn as a quasi-symmetrical circuit, with quasi-symmetry seen from node P. Analyzing Fig. 4.12, we can redraw the circuit as presented in Fig. 4.13, which simplifies the analytical analysis of currents I_P, I_F and I_A and the voltage at node P. Each network has an equivalent impedance, seen from node P to ground. The impedances can be described in the complex frequency domain as follows;

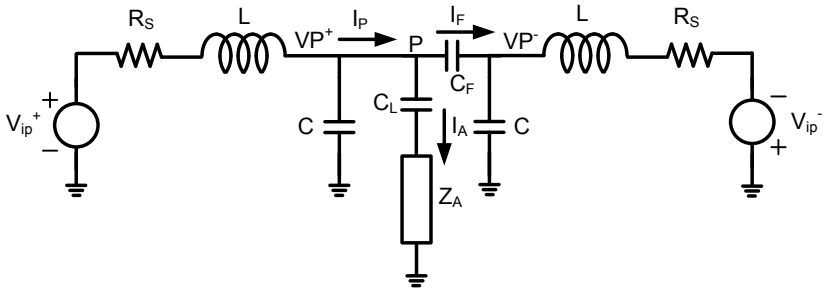


Figure 4.12: Circuit diagram of differential input LPUT as a quasi-symmetrical circuit.

$$Z_{pgA} = \frac{(R_S + sL)}{(s^2LC + sR_SC + 1)}, \tag{4.2}$$

$$Z_{pgB} = Z_{pgA} + Z_F, \tag{4.3}$$

$$Z_{pgC} = Z_A + \frac{1}{(sC_L)}, \tag{4.4}$$

where

$$Z_A = \frac{(sR_AL_A + R_AR_{LA})}{(s^2L_AC_AR_A + s(L_A + C_AR_AR_{LA}) + R_A + R_{LA})} \tag{4.5}$$

and R_{LA} is the series equivalent resistance of L_A. The voltage V_i is given by,

$$V_i = \frac{V_{ip}}{(s^2LC + sR_SC + 1)} \tag{4.6}$$

From Fig. 4.13, the current I_A is defined as,

$$I_A = I_P - I_F. \tag{4.7}$$

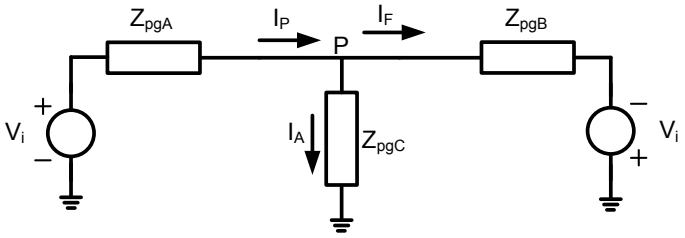


Figure 4.13: Circuit diagram of simplified LPUT as a T-network.

Applying superposition to the circuit of Fig. 4.13, we redraw the circuit as shown in Fig. 4.14(a) and Fig. 4.14(b). From Fig. 4.14(a) the current I_P is defined as,

$$I_P = \frac{V_i}{(Z_{pgC} || Z_{pgB}) + Z_{pgA}} \tag{4.8}$$

Substituting (4.3) in the denominator of (4.8) we obtain

$$I_P = V_i \frac{Z_{pgA} + Z_{pgC} + Z_F}{Z_{pgC}Z_F + 2Z_{pgA}Z_{pgC} + Z_{pgA}Z_F + Z_{pgA}^2}. \tag{4.9}$$

From Fig. 4.14(b) the current I_F can be defined as

$$I_F = \frac{V_i}{(Z_{pgB}) + (Z_{pgC} || Z_{pgA})}, \tag{4.10}$$

which can be rewritten as:

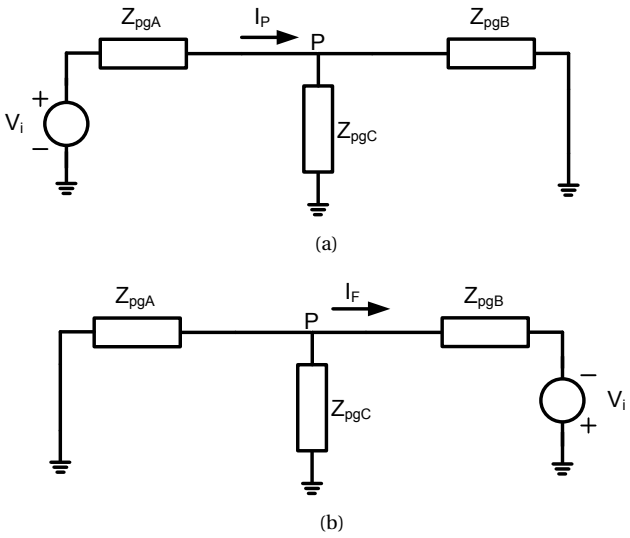


Figure 4.14: Circuit diagrams for superposition analysis of the circuit in Fig. 4.13.

$$I_F = V_i \frac{Z_{pgA} + Z_{pgC}}{Z_{pgC}Z_F + 2Z_{pgA}Z_{pgC} + Z_{pgA}Z_F + Z_{pgA}^2}. \tag{4.11}$$

Substituting (4.9) and (4.11) in (4.7) we obtain

$$I_A = \frac{V_i\, Z_F}{Z_{pgC}Z_F + 2Z_{pgA}Z_{pgC} + Z_{pgA}Z_F + Z_{pgA}^2}. \tag{4.12}$$

Substituting (4.12) in (4.1) and using (4.6) we obtain

$$V_A = \left(\frac{V_{ip}}{(s^2LC + sR_SC + 1)}\right).\left(\frac{Z_F\, Z_A}{Z_{pgC}Z_F + 2Z_{pgA}Z_{pgC} + Z_{pgA}Z_F + Z_{pgA}^2}\right), \tag{4.13}$$

which is the voltage across the antenna as a function of the equivalent impedances and the input voltage. From (4.13), we can conclude that the antenna voltage is roughly zero if Z_F is very low. This analysis makes perfect sense as the network is fully symmetric and the voltage at node P becomes zero when the network is driven by a differential input voltage. Since Z_F is a capacitive reactance, the voltage at node P thus equals zero at high frequencies. In this design, C_F is chosen to set the voltage at node P to zero for frequencies above 1 GHz. This will be demonstrated in Section 4.4.

4.4. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the simulation results that validate the analysis of Section 4.3 are presented. In addition, an experimental implementation is described and measurement results are shown.

4.4.1. SIMULATION RESULTS

The analysis developed in Section 4.3 has to be validated and for this purpose two types of simulations have been conducted:

- Circuit simulation of the transmitter.

- Mathematical simulation with the equations derived in Section 4.3.

The circuit of Fig. 4.11 has been simulated using a circuit simulator. Table 4.1 presents the component values used in the circuit and mathematical simulations. In the circuit simulation, two trapezoidal pulse voltage sources have been used as stimuli. The stimulus waveform is presented in Fig. 4.15 and parameters are given in Table 4.2.

Table 4.1: Component Values and Parameters

Parameter	@500 MHz	Parameter	@500 MHz
L_A (nH)	6.7	L (nH)	12
R_A (Ω)	50	R_S (Ω)	5-8
C_A (pF)	5	C (pF)	2.5
C_L (pF)	10	C_F (pF)	2.5

The mathematical simulation (performed in Matlab) is based on the frequency domain equations derived in Section 4.3. Therefore, the stimulus applied in this simulation is the Laplace transform of a trapezoidal pulse. The Laplace transform of the input stimulus is given by,

$$V_{in}(s) = \left(\frac{A}{T_1 - T_0}\right)\left(\frac{1}{s^2}\right)\exp(-sT_0) - \left(\frac{A}{T_1 - T_0}\right)\left(\frac{1}{s^2}\right)\exp(-sT_1) - \left(\frac{A}{T_3 - T_2}\right)\left(\frac{1}{s^2}\right)\exp(-sT_2) + \left(\frac{A}{T_3 - T_2}\right)\left(\frac{1}{s^2}\right)\exp(-sT_3), \tag{4.14}$$

and

$$V_{iP}(s) = \frac{V_{in}(s)}{(1 - \exp(-sT_P))}, \tag{4.15}$$

where $V_{iP}(s)$ is the Laplace transform of the impulse stimulus with pulse repetition period T_P.

The parameters of (4.14) and (4.15) are presented in Table 4.3.

Fig. 4.16(a) and Fig. 4.16(b) show the time domain results of the circuit and mathematical simulation, respectively.

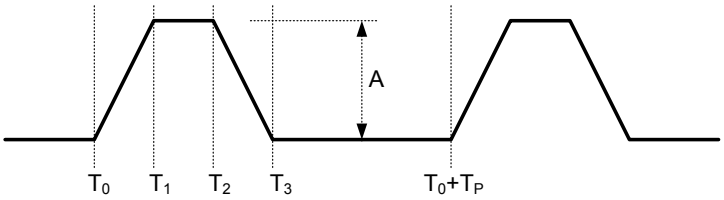


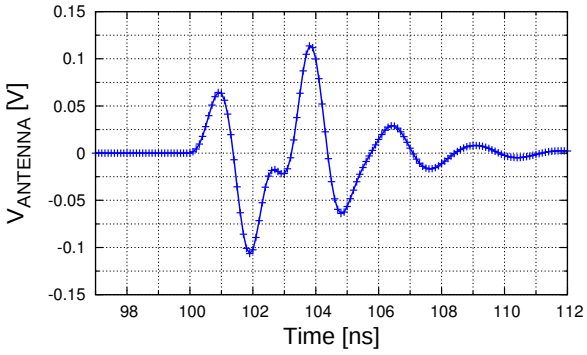
Figure 4.15: Waveform of the input stimulus of the mathematical simulation.

Table 4.2: Electrical Stimulus Parameters

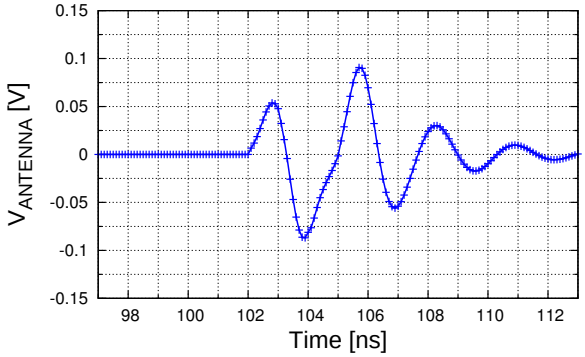
Param.	time (ns)	Param.	time (ns)
t_{RISE}	1	P_W	1
t_{FALL}	1	Tp	100
A	150mV		

Table 4.3: Mathematical Stimulus Parameters

Param.	time (ns)	Param.	time (ns)
T_0	1	T_2	1
T_1	1	T_3	1
A	150mV	Tp	300



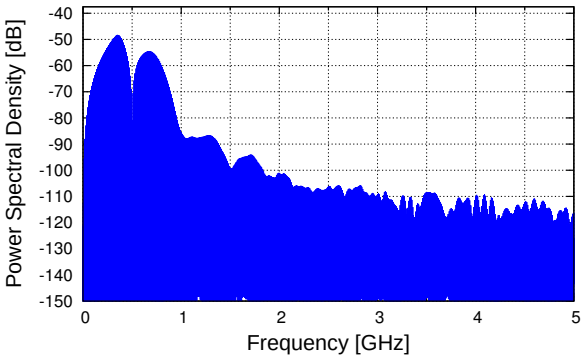
(a)



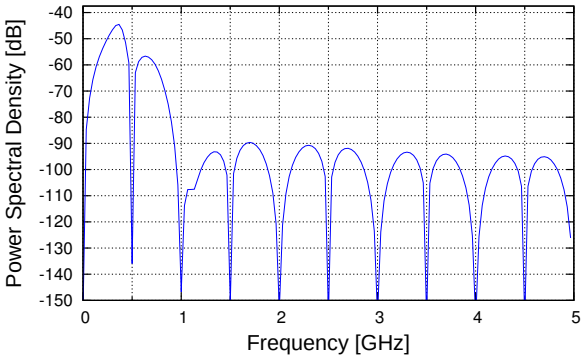
(b)

Figure 4.16: Time domain result of (a) circuit simulation and (b) mathematical simulation.

Fig. 4.17(a) and Fig. 4.17(b) present the power spectral density of the simulated signals. The PSD of the signals from both simulations are very much alike and comply with the FCC mask.



(a)



(b)

Figure 4.17: PSD of (a) circuit simulation and (b) mathematical simulation.

4.4.2. EXPERIMENTAL RESULTS

The low-power sub-GHz UWB transmitter has been realized using high-speed discrete transistors, discrete (SMD) capacitors and on-PCB inductors in line with the circuit diagram shown in Fig. 4.18. The drivers are implemented using high-speed discrete transistors with low threshold voltages in a stacked topology that is suitable for low voltage operation (100mV≤VDD_{RF}≤150mV) and offers high bandwidth. The transistor that has been chosen for this design is the ATF551M4. The threshold voltage (V_{TH}) of this device is roughly 0.35V. Fig. 4.19 shows the schematic of the ATF551M4 including the parasitics due to packaging [20].

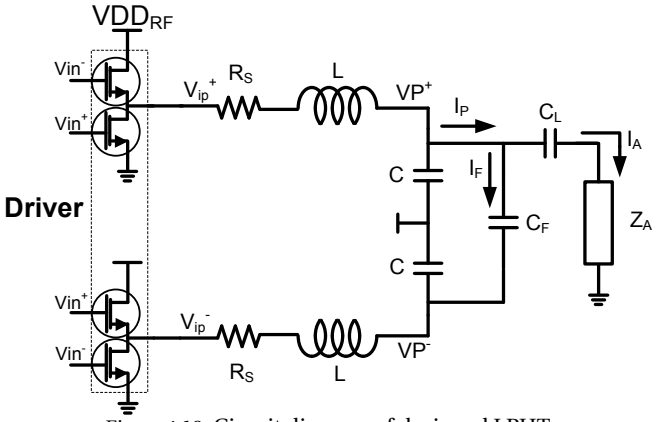


Figure 4.18: Circuit diagram of designed LPUT.

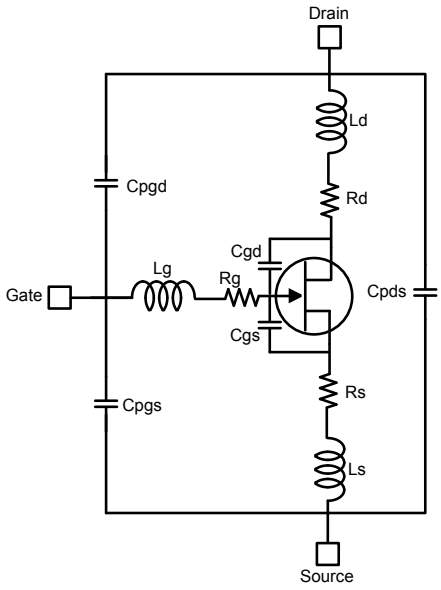


Figure 4.19: Equivalent circuit of the ATF551M4, showing the parasitics due to packaging [20].

The input and output inductances and capacitances of this device are small enough (see Table 4.4) to minimize dynamic power consumption and to keep the amount of high frequency spurs in the transmitted pulse small.

Table 4.4: ATF551M4 Electrical Parameters

Parameter	Value	Parameter	Value
L_g (nH)	0.094	L_s (nH)	.075
R_g (Ω)	2.9	R_{source} (Ω)	0.68
C_{gs} (pF)	0.75	L_d (nH)	0.5
C_{gd} (pF)	0.134	R_d (Ω)	2
C_{ds} (pF)	0.1	V_{TH}	~0.35

For testing purposes only, a differential input stimulus generator has been implemented. The input stimulus generator comprises a pulse generator, a high pass voltage divider, a balun and a level shifter, as depicted in Fig. 4.20. The level shifter is supplied by Vddpulse that is 0.65V (V_{TH} + VDD_{RF} and thus large enough to drive both stacked transistors).

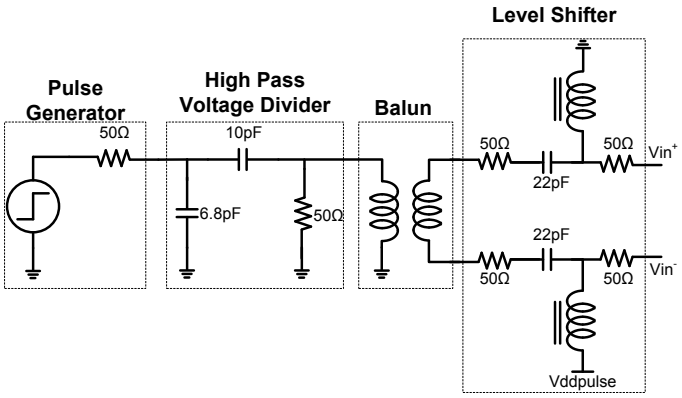


Figure 4.20: Circuit diagram of the stimulus generator.

A photograph of the test bench is shown in Fig. 4.21. Fig. 4.22 shows a photograph of the PCB of the transmitter that includes the level shifter.

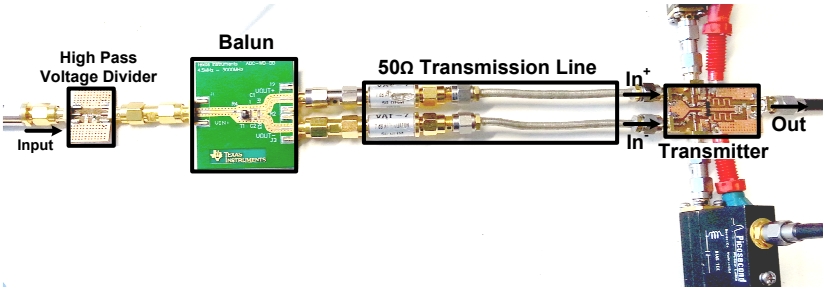


Figure 4.21: Test bench photograph of the low energy sub-GHz UWB transmitter.

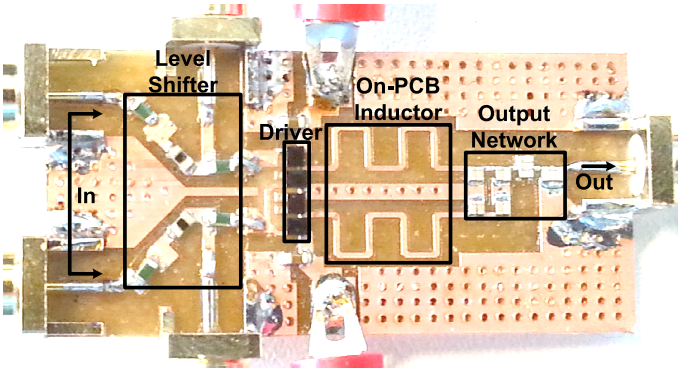
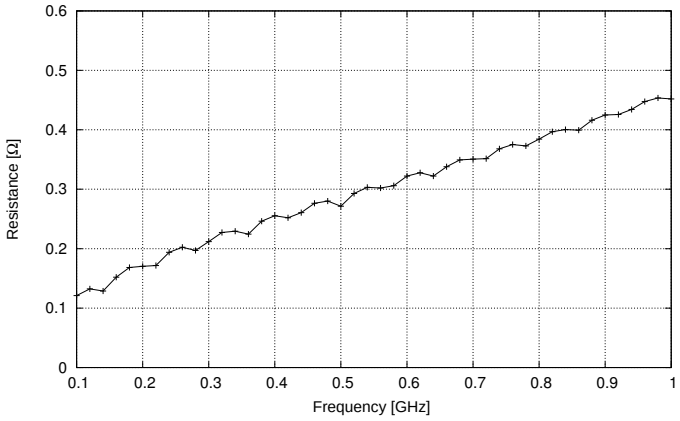


Figure 4.22: PCB photograph of the designed transmitter.

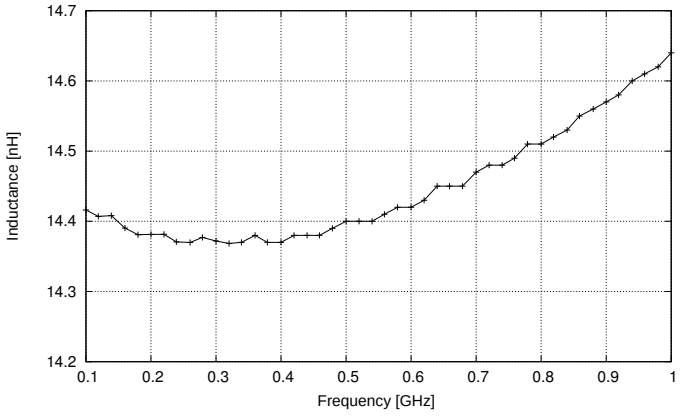
The equivalent series resistance and inductance of the on-PCB inductor, extracted by means of electromagnetic simulation, are presented in Fig. 4.23(a) and Fig. 4.23(b). The physical and electrical properties of the on-PCB inductor are summarized in Table 4.5.

Table 4.5: Physical and Electrical Properties of the on-PCB Inductance

Physical	1/2oz. 1.55mm	Electrical	@500 MHz
Outer dim. (mm^2)	11.16 x 3.12	L (nH)	14.4
Eff. length (mm)	23.1	ESR (Ω)	0.28
Trace width (mm)	0.35	Q-factor	>100
Trace space (mm)	1.95		



(a)



(b)

Figure 4.23: Equivalent series resistance,(a), and inductance, (b), of the on PCB inductor.

Fig. 4.24 and Fig. 4.25 show the measured output voltage waveform of the LPUT and the corresponding power spectral density for VDD_{RF} = 0.15V, respectively. In Fig. 4.24 and Fig. 4.25, some high frequency components (> 1GHz) can be observed while in Fig. 4.17(a) and Fig. 4.17(b) high frequency components are attenuated. The main difference between the measured and the mathematical results is the symmetry of the circuit. The circuit developed on PCB is not ideally symmetrical, therefore the roll-off is less steep than that of the mathematical model. The PSD of the transmitted signal presents a 25dB decay between 500 MHz and 1 GHz, which means a roll-off of 25dB/octave. To measure the power consumption of the LPUT, the RMS current consumption of the driver is measured as well as the level shifter power consumption.

Fig. 4.26 to Fig. 4.28 present the estimated PSD of the transmitted impulse (of Fig. 4.25) after path loss, ground reflection and antenna/receiver matching. The path loss and ground reflection is modeled and simulated using the measured transmitted impulse as

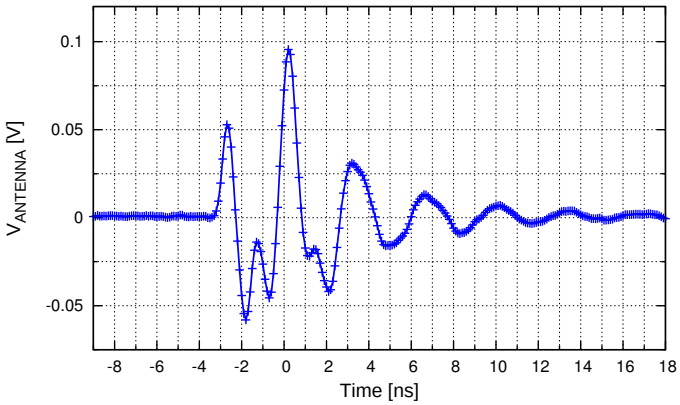


Figure 4.24: Measured output voltage waveform of the LPUT.

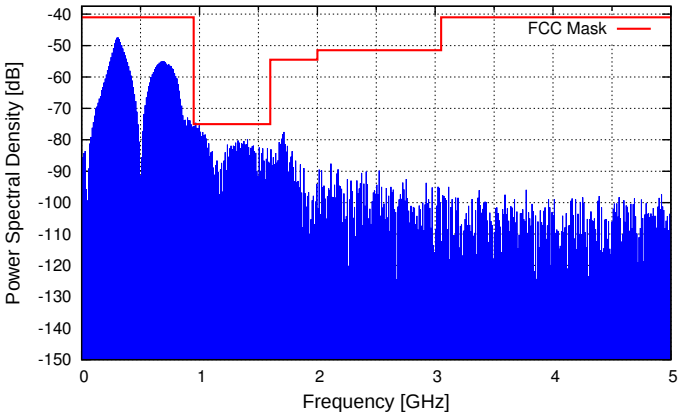


Figure 4.25: Measured output power spectral density of the LPUT.

input. The transmitter-receiver separation distances (d) considered in the analysis are 0.1 m, 1 m, and 10 m with the transmitter and receiver in the same height (h) of 0.1 m, 1 m, and 10 m; the ground reflection coefficient is -1. Fig. 4.26 to Fig. 4.28 show that the PSD peak power decreases with d, while PSD peak power increases with h. This behavior can be explained by the fact that at lower height (h = 0.1 m) the ground reflected signals stronger at the receiving antenna with 180° phase. On the other hand, if the antenna is positioned in higher heights (1 m and 10 m) the reflected signal is attenuated and its effects are minimized.

Table 4.6 summarizes the experimental results of the LPUT. Even lower power consumption can be achieved if transistors with lower input capacitance and lower threshold voltage are employed in the design.

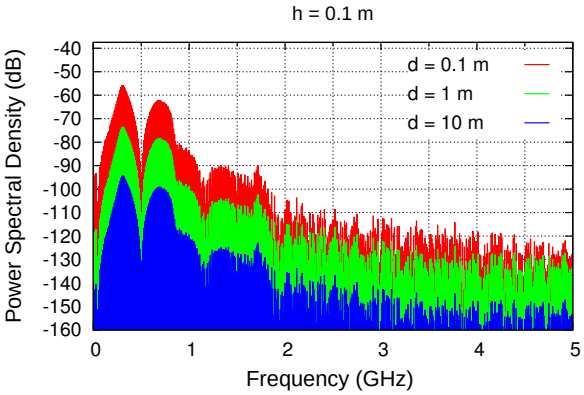


Figure 4.26: Estimated PSD of the LPUT including path loss and ground reflection for $h = 0.1$ m.

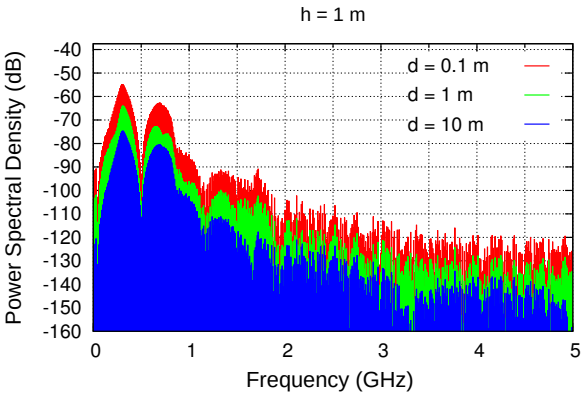


Figure 4.27: Estimated PSD of the LPUT including path loss and ground reflection for $h = 1$ m.

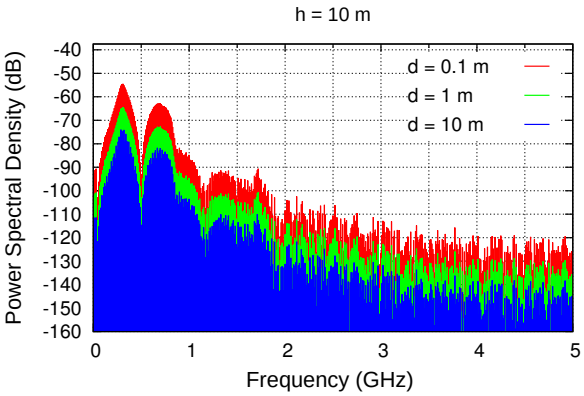


Figure 4.28: Estimated PSD of the LPUT including path loss and ground reflection for $h = 10$ m.

Table 4.6: Performance Summary of the LPUT

Specifications	Value	Specifications	Value
Frequency Band (GHz)	0.25-0.75	$V_{peak-peak}$ (V)	0.14
Power (mW)	0.280	$V_{peak-peak}$/Supply Voltage (%)	93.3
Energy./Pulse (pJ/pulse)	85	PRF (MHz)	3.3
Supply Voltage (V)	0.15/0.65†	Roll-off (dB/octave)	25

† Voltage supply of the level shifter, for testing purposes.

4.5. CONCLUSIONS

Two techniques for realizing asynchronous low-power event-driven data transmission based on backscattering and impulse radio ultra-wide band have been presented. The asynchronous event-driven transmitter for a wireless ECG sensors node has been presented. We have proposed an asynchronous method to transmit data from an ECG front-end that is designed with a level-crossing analog-to-digital converter. The 2 output bits (`UD` and `Change`) of the ADC are first combined using a pulse encoder circuit and then transmitted via a backscattering link in the 402-MHz MICS frequency band. Since the 402-MHz signal is modulated by a pulse, a wide band PSD is generated close to the center frequency. However the difference between the center frequency power and the side band is 25 dB, as the transmitter does not interfere with adjacent channels.

The design of a low-power sub-GHz UWB transmitter (LPUT) has been presented. LPUT analytical models and simulation results that validate the analysis have been demonstrated. The transmitter has been designed with off-the-shelf ATF551M4 transistors, on-PCB inductors and (SMD) capacitors. Measurements results show that the LPUT can operate from a low-voltage power supply (150mV) with an energy consumption of 85pJ/pulse for a peak-to-peak output voltage of 140mV and a pulse repetition frequency (PRF) of 3.3MHz. Measurement results show a roll-off of 25 dB/octave between 500 MHz and 1 GHz.

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5

AUTONOMOUS WIRELESS SENSOR NODE WITH TEMPERATURE MONITORING

A dual-band autonomous wireless sensor node (AWSN) with temperature monitoring is designed in a standard 0.18 µm CMOS technology. The AWSN comprises a high efficiency energy harvester, a power management module, a temperature-to-time converter (TTC) and a passive 402-MHz MICS band OOK transmitter for backscattering transmission. The AWSN demonstrates a sensitivity of -18.2 dBm at 13.56 MHz. The energy harvester achieves an RF-to-DC power conversion efficiency (PCE) of 11.5 %. From 0 to 100 °C, the temperature conversion and temperature accuracy of the TTC are 1.5 µs/°C and 0.21 °C, respectively. The active area of the AWSN is 0.72 mm^2. It consumes 1.5 µW (RMS). In the second part of this chapter, a prototype of a data receiver for the AWSN is presented. Measurements have been conducted to quantify the link losses, which are around 70dB. Given the measured losses, the receiver topology has been defined. The receiver comprises two main blocks: an RF front-end and an LF back-end. The RF front-end includes a low noise amplifier, a surface acoustic wave (SAW) filter and an envelope detector. The LF back-end comprises a voltage buffer, a band-pass filter, a base-band amplifier, an averaging circuit and a comparator. The RF front-end and the LF back-end are powered from a 5V supply with a total power consumption of 100mW.

5.1. DUAL-BAND AUTONOMOUS WIRELESS SENSOR NODE

Today's single-band/channel solutions for personal and body area networks rely on digital logic, ADCs, embedded memory for data management, and often require external elements (capacitors) for energy storage and power management [1–4]. This classical design methodology is relatively inflexible with respect to sensor accuracy and the required power budget tends to exceed what is permissible for autonomous operation. To overcome the shortcomings of the classical design, an ultra low-power, dual-band (MICS and ISM) autonomous wireless sensor node with temperature monitoring is proposed.

5.1.1. AWSN DESIGN

As shown in Fig. 5.1, the AWSN comprises an RF energy harvester, a power management module, a temperature-to-time converter and a 402 MHz (MICS band) OOK backscattering data transmitter. The dual-band approach is chosen to exploit the maximum permissible power transmission at 13.56 MHz and the wide bandwidth for data transmission at 402 MHz, thus providing simultaneous data communication and RF energy harvesting.

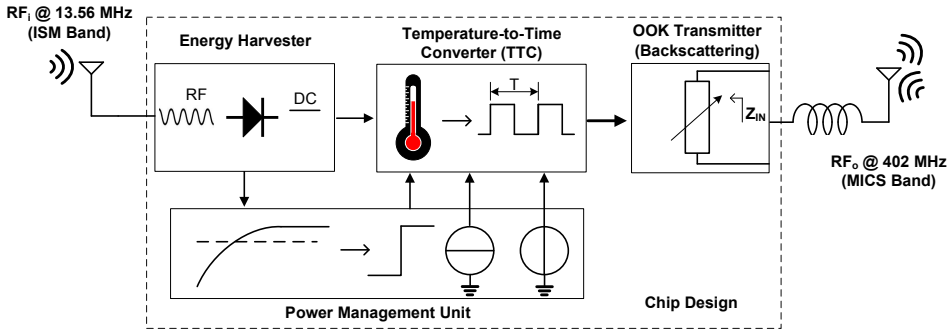

Figure 5.1: Block diagram of the dual-band AWSN with temperature monitoring.

The theoretical model and analysis of the energy harvester have been presented in Chapter 3. The energy harvester comprises a passive voltage-boosting network (VBN) (Fig. 5.2(a)) and an orthogonally switching charge pump rectifier (OS-CPR) (Fig. 5.2(b)).

To adequately drive the OS-CPR, the VBN delivers large swing control (V_{b+} and V_{b-}) and energy signals (V_{r+} and V_{r-}). The resonant circuit of the VBN is modeled by the self-inductance of the antenna, L_A (9.5 μH), its series resistance, R_A (12 Ω), and capacitance $C_{V,T}$ (14 pF) (being the sum of the tuning and parasitic capacitances). An inductive choke L_C provides a DC short at the input terminals of the rectifier to ensure a zero DC offset error at the input of the OS-CPR. A single rectifier stage comprises PMOS transistors as voltage-controlled switches (M_1 and M_2) and capacitors for AC coupling (C_C) and energy storage (C_{R1} and C_{R2}). To reduce any unwanted flow-back current, capacitances C_{DC} and resistors R_{DC} set the optimum values of the gate voltages of M_1 and M_2. From a -18.2 dBm 13.56 MHz RF signal, a 5-stage OS-CPR sets the power supply voltage (V_{DC} = $V_{O,N}$) at 1.2 V.

Fig. 5.3 presents the all CMOS-based power management module.

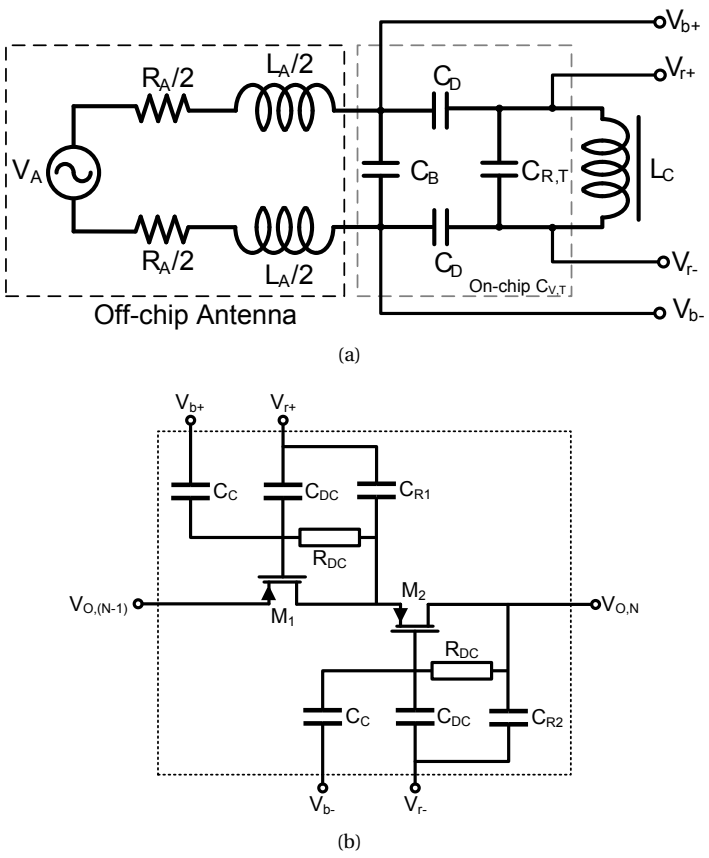

Figure 5.2: The energy harvester comprises (a) voltage boosting network and (b) an orthogonally switching passive charge pump rectifier.

It includes a nanopower voltage reference, a linear voltage regulator and a low-voltage detector (LVD) with hysteresis (0.15 V). The reference produces a sub-1V, stable and temperature-independent voltage. With all the MOSFETs biased in weak inversion and the op-amp A_1 creating a virtual ground at V_{ref}, the current through R_1 is PTAT. Proper selection of R_1, R_2 and N sets temperature-independent voltage V_{ref} at 0.54 V, which is derived by combining PTAT (V_{R2}) and CTAT ($V_{\text{gs},4}$) voltages. Current I_{ref} is steered into M_{10}, generating V_n used to generate nI_{ref}, mI_{ref} and pI_{ref}.

The linear regulator employs a unity gain buffer configuration to set the power supply (V_{DD}) of the AWSN at V_{ref}. Power supplies V_{DC} and V_{DD} are filtered using on-chip decoupling capacitors ($\approx$ 100's of pF).

The low-voltage detector, which comprises switches S_1, S_2 and comparator CM_1, monitors the V_{DC} voltage level. During power-up V_{DC} initially is 0V and increases with time, until it reaches 1.2V. Also V_{ref} initially is 0V. The LVD operates as follows:

1. During power-up: S_1 is closed and the voltage divider formed by M_{11} and M_{12} sets $pV_{DC} < qV_{DC}$. To reduce static power consumption, qV_{DC} is generated from the capacitive divider formed by C_1 and C_2. Voltages qV_{DC} and pV_{DC} are compared by CM_1 and as long as the latter is smaller, the output voltage of the LVD (V_{LVD}) equals V_{DC}.

2. Steady-state: S_1 opens, S_2 closes and V_{ref} is connected to the input of CM_1. Once pV_{DC} equals V_{ref} (i.e. V_{DC} settles to 0.96 V), V_{LVD} goes from V_{DC} to 0 V, thereby enabling the temperature-to-time converter (TTC).

The TTC and the 402 MHz (MICS band) OOK transmitter are shown in Fig. 5.4. Derived from the circuit design presented in [6], the temperature-to-time encoded clock signal is generated by steering a PTAT current (mI_{ref}) into an integrating capacitor (C_T). The slope of the resulting ramp-like analog waveform is compared to two voltage references, V_1=0.35 V for the rising and V_2=0.15 V for the falling edge transitions. The resulting output square wave signal of the TTC has a time period T_{TTC}, which equals

$$T_{TTC} = \frac{C_T \Delta V}{mI_{ref}}, \tag{5.1}$$

where $m = 2$, $\Delta V = V_1 - V_2$. A backscattering return link is formed at 402 MHz when the TTC clock signal drives/switches transistor M_{13}, thereby modulating the backscattered RF power.

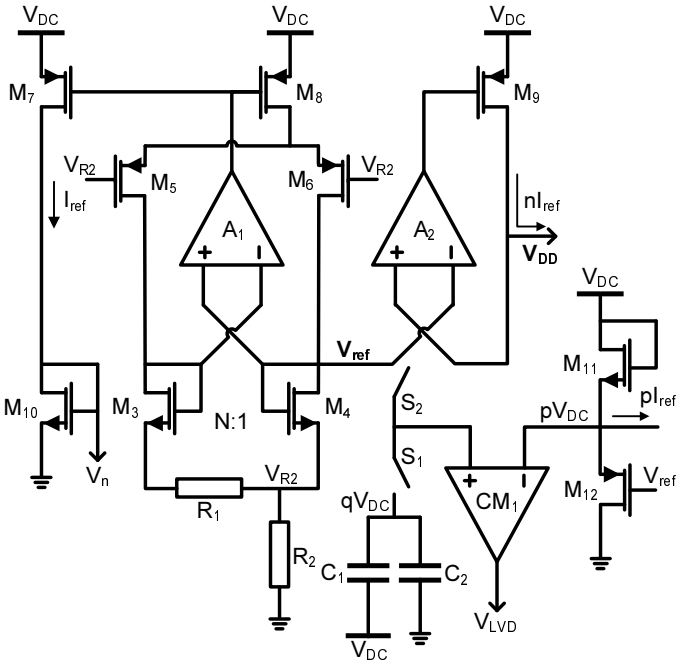

Figure 5.3: Power management module of the AWSN.

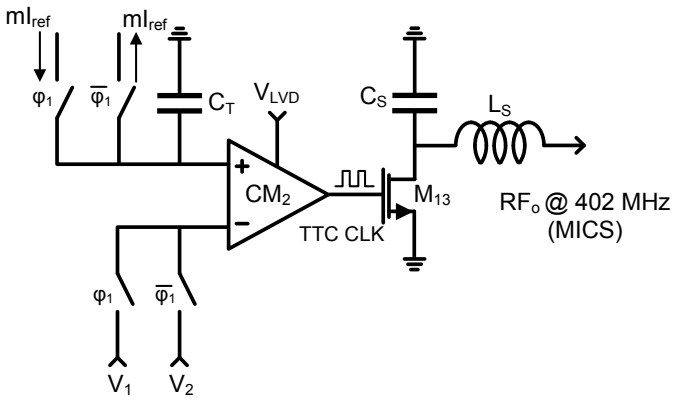

Figure 5.4: Temperature-to-time converter and the 402 MHz (MICS band) OOK transmitter.

5.1.2. MEASUREMENT RESULTS

The AWSN is mounted on a double-sided, FR-4 laminate substrate with a high quality factor coil (antenna) etched on the back plate (see Fig. 5.5). The physical and electrical properties of the customized antenna coil are presented in Table 6.2. The coil is modeled using ADS Momentum.

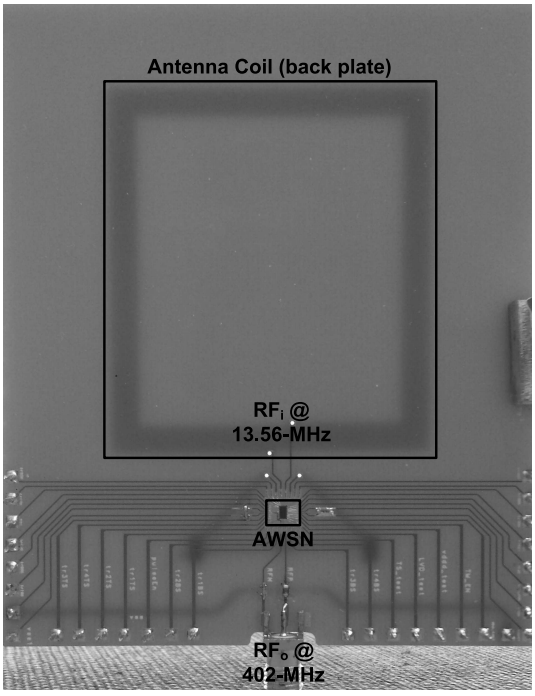

Figure 5.5: The AWSN and the antenna coil on a 1/2 oz. 1.55 mm thick, double-sided FR-4 laminate substrate.

Table 5.1: Physical and Electrical Properties of the Antenna Coil

Electrical	@13.56 MHz	Physical	1/2oz. 1.55mm
L_A (μH)	9.5	Outer dim. (mm^2)	56 x 50
R_A (Ω)	12	Inner dim. (mm^2)	48 x 42
C_A (pF)	2.4	Trace width (mm)	0.25
f_{SR} (MHz)	33	Trace space (mm)	0.25
Q-Factor	67	No. of turns	8

At 13.56 MHz, the measured real and imaginary impedance components of the antenna coil are 12.7 Ω and 810 Ω, respectively (see Fig. 5.6). Simulation and measurement results show less than 5 % discrepancy.

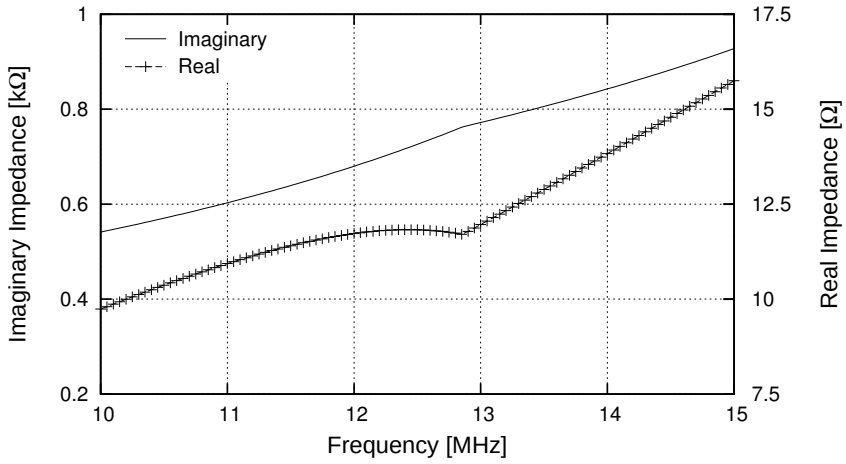

Figure 5.6: Real and imaginary impedance of the antenna coil as a function of frequency.

The microphotograph of the AWSN fabricated in AMS 0.18 μm CMOS technology is shown in Fig. 5.7. The total and the active chip area are 2.64 mm^2 (1.2 x 2.2 mm^2) and 0.72 mm^2 (0.4 x 1.8 mm^2), respectively.

The energy harvester operates over a large range of resistive loads (0.1 MΩ to 0.82 MΩ). As shown in Fig. 5.8, the maximum PCE is 11.5 % for a 0.82 MΩ load. Note that PCE here equals the ratio of the electrical power delivered to the load and the incident electromagnetic power at the antenna.

The temperature conversion, jitter and temperature accuracy of the TTC are 1.5 μs/^{o}C, 320 ns and 0.21 ^{o}C, respectively, from 0 to 100 ^{o}C (see Fig. 5.9). The temperature accuracy ($TTC_{acc.}$) is calculated as the ratio of the jitter to temperature conversion and equals:

$$TTC_{acc.} = \left(\frac{320ns}{1.50\ \mu s/^oC}\right) = 0.21\ ^oC \tag{5.2}$$

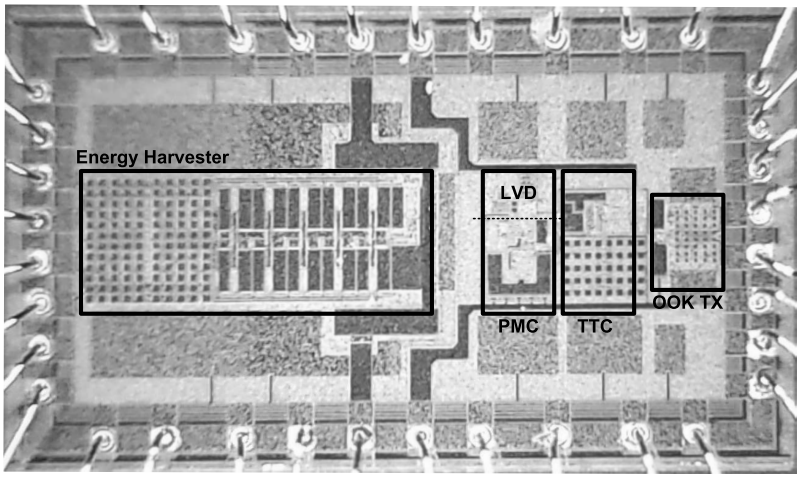

Figure 5.7: Microphotograph of the AWSN in 0.18 μm CMOS.

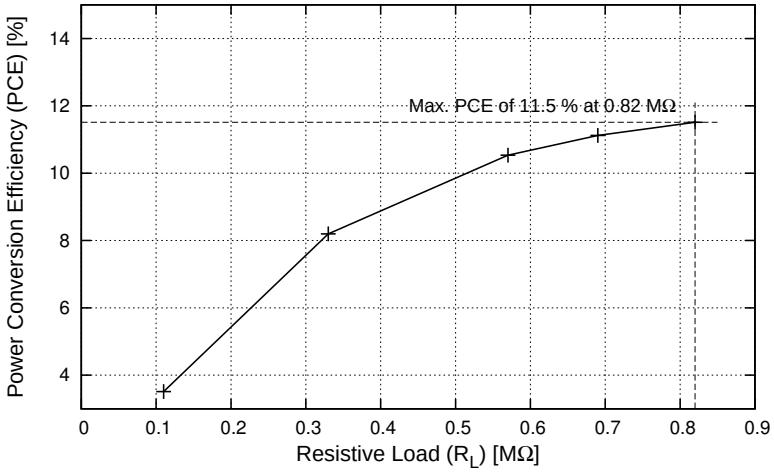

Figure 5.8: PCE of the energy harvester as a function of resistive load.

In compliance with MICS, the minimum clock period of the TTC is set to 20 μs. Fig. 5.10 shows the backscattering signal from the AWSN.

Table 5.2 compares the proposed AWSN to other published designs. This work demonstrates as main characteristics the high sensitivity, high PCE and high TTC accuracy with ultra-low power consumption. Moreover, the AWSN is both technology and frequency scalable.

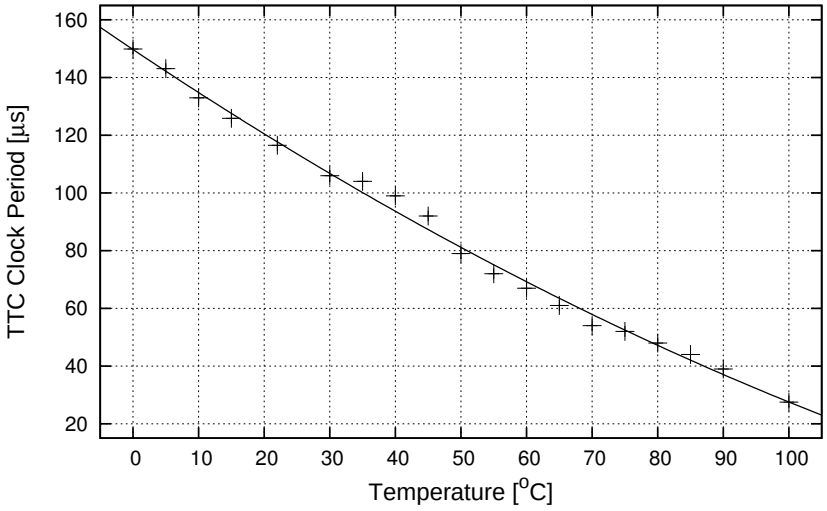

Figure 5.9: Temperature conversion of the temperature-to-time converter. The least-squares polynomial regression shows a conversion accuracy of 1.5 $\mu s/^{o}$C.

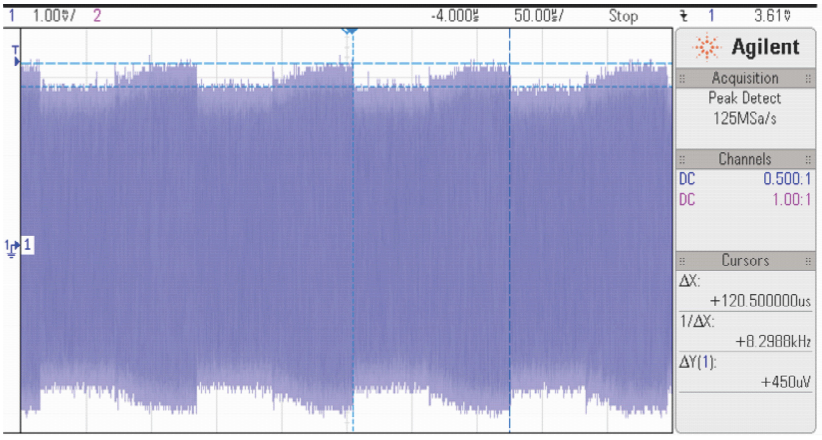

Figure 5.10: Backscattered signal at 402 MHz (MICS band).

5.2. DATA RECEIVER FOR THE AWSN

In the previous section, the design of an autonomous wireless sensor node for temperature monitoring has been presented. The AWSN transmits data in the MICS band and the data should be received by a hub. In this section, a prototype of a data receiver is presented. The data receiver topology is chosen based on signal modulation and signal path losses. Moreover, rejection of interference is taking into account in the design.

Table 5.2: Summary and Comparison of the AWS with Previously Published Designs

Specifications	This Work	[1]	[2]	[3]	[4]
Frequency Bands (MHz)	13.56/402	2400	900/2100	13.56-2450	860-960
Sensitivity (dBm)	-18.2±1	-10.5	-19.7	-10.3	-6
Maximum PCE (%)	**11.5**	-	3	9	-
Conversion Accuracy (μs/^{o}C)	1.5	-	-	-	-
Clock Jitter (ns)	320	-	-	-	-
Temperature Accuracy (^{o}C)	**0.21**	0.37	-	0.34‡	0.20‡
Supply Voltage (V)	1.2	1.5	1.0	1.0	1.0§
Power Consumption (μW)	**1.5**	2.3	2.7†	2.7†	2.4†
Active area (mm^2)	0.72	0.7	1.055	0.95	1.1
Technology - CMOS	C-180	C-130	C-130	C-130	C-180

† Only sensor circuitry.
‡ Values estimated from ENOB.
§ Temperature sensor power supply.

5.2.1. SIGNAL LOSSES

This section describes the estimation and measurement methodology to define signal losses in the air. The total loss is an important parameter to estimate the gain required by the RF front-end in order to detect the data signal. The waveform presented in Fig. 5.10 is the input information signal of the receiver, measured directly from the designed AWSN. The peak-to-peak voltage of the received signal is 6mV with a modulation index of 15%. The maximum bandwidth of the signal is 50 kHz, which is the highest frequency of the output signal of the TTC. Although the signal seems to be large enough to be detected, the actual signal will be attenuated when the signal is transmitted via the air. The loss (S) can be computed by [7],

$$S = \frac{P_t\, G_t^2\, \sigma\, \lambda^2}{(4\pi)^3\, R^4} \tag{5.3}$$

The parameters of Eq. 5.3 are summarized in Table 5.3.
For a distance of 40 cm, 20 cm in both ways, the estimated loss is 70dB for an antenna with 0.5dBi of gain.

LOSSES MEASUREMENT

The link losses have been measured to determine the attenuation of the signal when transmitted via the air. As calculated the link losses should be around 70dB. Fig. 5.11 shows the setup utilized for link loss measurements. The antenna parameters are presented in Table 5.4.

Fig. 5.12 presents the measured received power for a distance of 20 cm. The signal is transmitted at 402MHz with 0dBm. The signal loss for only one way of the link is 31.79

Table 5.3: Summary of Parameters for Loss Calculation

Parameter	Description	Value
S (dB)	Loss	70
P_t (dBm)	EIRP	-16
G_t (dBi)	Antenna gain	0.5
σ	Radar Cross Section AWSN-Antenna	0.0028
λ (m)	Wavelength	0.7463
R (m)	Distance from the source	0.4

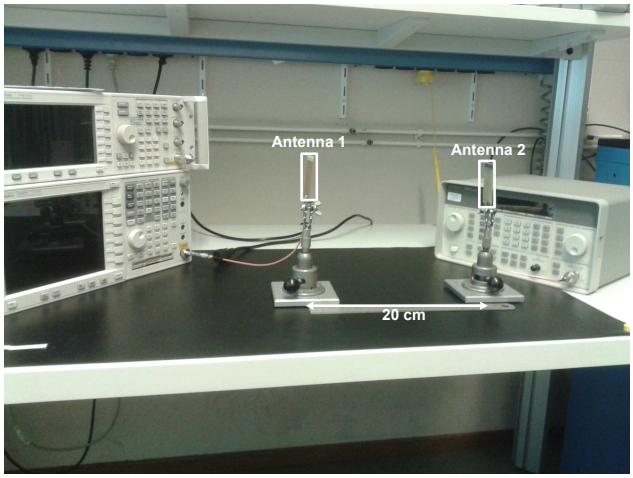

Figure 5.11: Signal losses measurement setup.

Table 5.4: Summary of Antenna Parameters

Parameters	Value	Unit
Frequency	300-500	MHz
Gain	0.5	dBi
Polarization	Linear	
Impedance	50	Ω

dB, which means that the total loss of transmitted and backscattered signal is 2 x 31.79 dB. Therefore, the total attenuation of the signal is roughly 64dB.

The antenna used in the measurements is designed to operate in a wide frequency band from 300MHz to 500MHz. In the measurements, interference has been detected at 395MHz and 405MHz, which indicates that an RF filter is required to suppress the

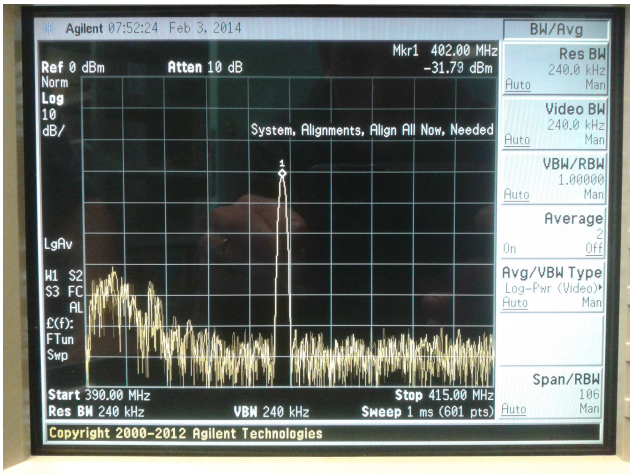

Figure 5.12: Measurement of the received power for a distance of 20cm (one way).

interference signal. More details will be given in Sec. 5.2.2.

5.2.2. DATA RECEIVER TOPOLOGY

The block diagram of the designed receiver is shown in Fig. 5.13. The receiver RF front-end consists of a low noise amplifier (LNA), an RF bandpass filter and an envelope detector for down conversion of the received signal. The low frequency (LF) back-end includes an analog buffer, a base-band band-pass filter, an amplifier, an averaging circuit and a comparator.

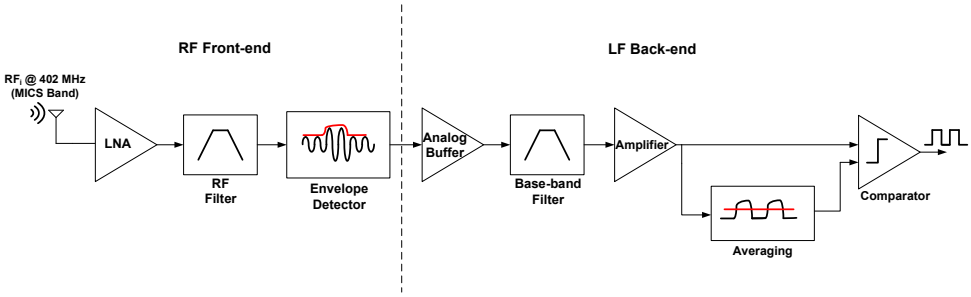

Figure 5.13: Block diagram of the designed receiver.

The RF filter has been included in the design as interference has been detected at the edges of the MICS band. For very high selectivity, a SAW filter has been chosen due to the steep roll-off characteristic of this filter. The signal down conversion is made by an envelope detector since the input signal is modulated using OOK modulation. The sensitivity of the envelope detector is important to define the minimum gain required by the LNA. Since the driving capability of the envelope detector is limited, an analog buffer is placed just after the envelope detector to drive the LF band-pass filter employed to

attenuate any residual RF signal. After filtering, the base-band signal is amplified and compared with its average, generating the output bitstream. The following sections describe in more detail the design of the blocks included in the receiver.

RF FRONT-END

The first circuit described in this section is the envelope detector as it is directly related to the gain requirements of the LNA. Secondly, the SAW filter characteristics are presented. Finally, the LNA design is described based on gain and noise requirements.

As the received signal amplitude is around a few mV, the envelope detector requires a high sensitivity. Therefore, a simple envelope detector comprising a diode and a RC network is not sensitive enough to detect the incoming signals. For this reason, an IC with an active envelope detector is used to achieve high sensitivity. Among the options on offer, the IC ADL5511 has been chosen due to its high sensitivity and large base-band bandwidth. The specifications of the ADL5511 are summarized in Table 5.5. The main property of this device is the minimum signal level that it can detect, which is -29dBm.

Table 5.5: Parameters of the Envelope Detector

Parameters	Value	Unit
Frequency	DC-6	GHz
Envelope Bandwidth	130	MHz
Minimum input level	-29	dBm
Supply Voltage	5	V

The RF filter is implemented with a Surface Acoustic Wave filter. The RF1419 has been chosen as it has low insertion loss and high selectivity. The specifications of the SAW filter are stated in Table 5.6. The SAW filter requires input and output impedance matching at 50Ω. As described in Section 5.2.1 the link loss is 64 dB and the antenna input power (PWR_{IN}) is -16 dBm - 64 dB = -80 dBm, where -16 dBm is the MICS band EIRP. Furthermore, it is known that the SAW filter introduces a loss ($Loss_{SAW}$) of 1.6dB. The sensitivity of the envelope detector (ED_{sns}) is -29dBm, thus the minimum required gain of the LNA is given by

$$G_{min} = ED_{sns} - (PWR_{IN} - Loss_{SAW}). \tag{5.4}$$

Substituting the above values into Eq. 5.4, we obtain G_{min} = 52.6 dB.

A cascade of 3 LNAs is required to achieve the minimum gain of 52.6 dB. The noise figure should be set as low as possible (<1 dB). In this design, the SAW filter is placed after the first LNA stage to keep the noise figure low and prevent interference from saturating the next amplifying stages. The first stage (LNA1) is implemented with the HMC616LP3E that has a 0.5 dB noise figure and 21 dB of gain. For the second (LNA2) and third (LNA3) stages, the LNA MBC131916 with a noise figure of 1.07 dB and gain of 24 dB has been used. With the three cascaded LNAs plus the SAW filter, the theoretical noise figure and gain are 0.5 dB and 65 dB, respectively. LNA1 is 50Ω matched at the input and output of

Table 5.6: Specification of the SAW Filter

Parameters	Value	Unit
Center Frequency	403.5	MHz
Bandwidth	7.5	MHz
Insertion Loss	1.6	dB
Impedance	50	Ω
Out of Band Rejection	≃50	dB

the IC itself, therefore no additional matching network is required. On the other hand, LNA2 is not 50Ω matched, thus an impedance transformation is required. LNA2 has been simulated and the input and the output impedances are (73.186-j102.052)Ω and (101.492-j345.770)Ω, respectively. For 50Ω matching an input and an output network have been calculated. Fig. 5.14 shows LNA2 with the input and the output networks required for impedance matching.

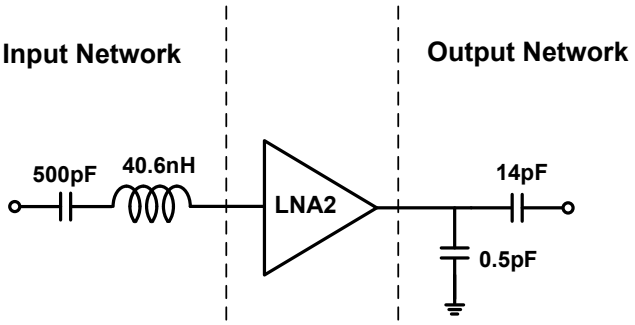

Figure 5.14: Circuit diagram of the designed matching network of LNA2.

At the input, a capacitance of 500pF and an inductance of 40,6nH are placed in series and at the output a capacitance of 0.5pF is connected to ground and a series capacitance of 14pF is connected to the next stage to achieve 50 Ω impedance matching.

LF BACK-END

In the LF back-end, to implement the analog buffer, the amplifier and the comparator, we use the ADA4895-2 operational amplifier that has the following specifications:

- Low off-set voltage (350μV)
- High gain-bandwidth (GBW)(236MHz)
- Low noise (1nV / $\sqrt{\text{Hz}}$)
- High slew-rate (943V/μsecond)

The specification above covers the requirements of the LF back-end for speed, driving capacity and accuracy. Fig. 5.15 shows the complete circuit diagram of the LF back-end.

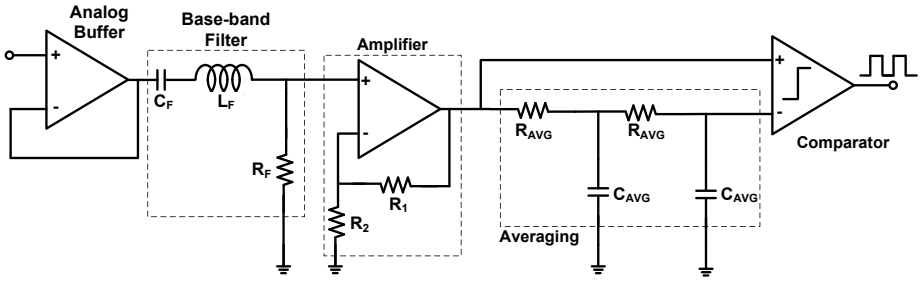

Figure 5.15: Circuit diagram of the LF backend.

The analog buffer is implemented by an operational amplifier as a unity gain amplifier. The high input impedance secures that the output of the envelope detector is not overloaded and the low output impedance ensures that the base-band filter is driven properly. The base-band filter comprising C_F (10 μF), L_F (10 μH) and R_F (15 Ω) is a band-pass filter with lower and upper cut-off frequencies at 1 kHz and 150 kHz. The purpose of the filter is to block any DC voltage coming from the analog buffer while it filters residual RF signal coupled into the base-band signal ($\simeq$50 kHz). The amplifier that includes the opamp, R_1 and R_2 sets a voltage gain of 10 since the voltage coming out of the filter is in order of a few mV. The voltage gain of 10 is sufficient to ensure proper signal comparison as the comparator has a maximum offset voltage of 350 μV. The output of the amplifier is connected to the input of the voltage comparator and the averaging circuit. The amplified voltage is averaged by the second order low-pass filter consisting of R_{AVG} (300 Ω) and C_{AVG} (1 μF) that sets the cut-off frequency at 500 Hz. The filter is chosen to be second order to guarantee that a base-band signal at 2 kHz can be averaged properly. Finally, the bitstream is generated by the comparator that compares the amplified signal with its average. The signal generated by the comparator can be read by an algorithm that detects the frequency of the bitstream and consequently detects the temperature transmitted by the AWSN. This is, however, beyond the scope of this thesis.

5.2.3. DATA RECEIVER MEASUREMENTS

In this section the measurement results of the data receiver are presented. The section is divided into two parts: the first part shows the results of the RF front-end and in the second part, the low frequency back-end measurement results are presented.

RF FRONT-END

Fig. 5.16 shows the measured scattering parameters of the LNA that is connected to the antenna. The noise figure of this LNA is around 0.5 dB, which is low enough to keep the total front-end noise figure below 1 dB.

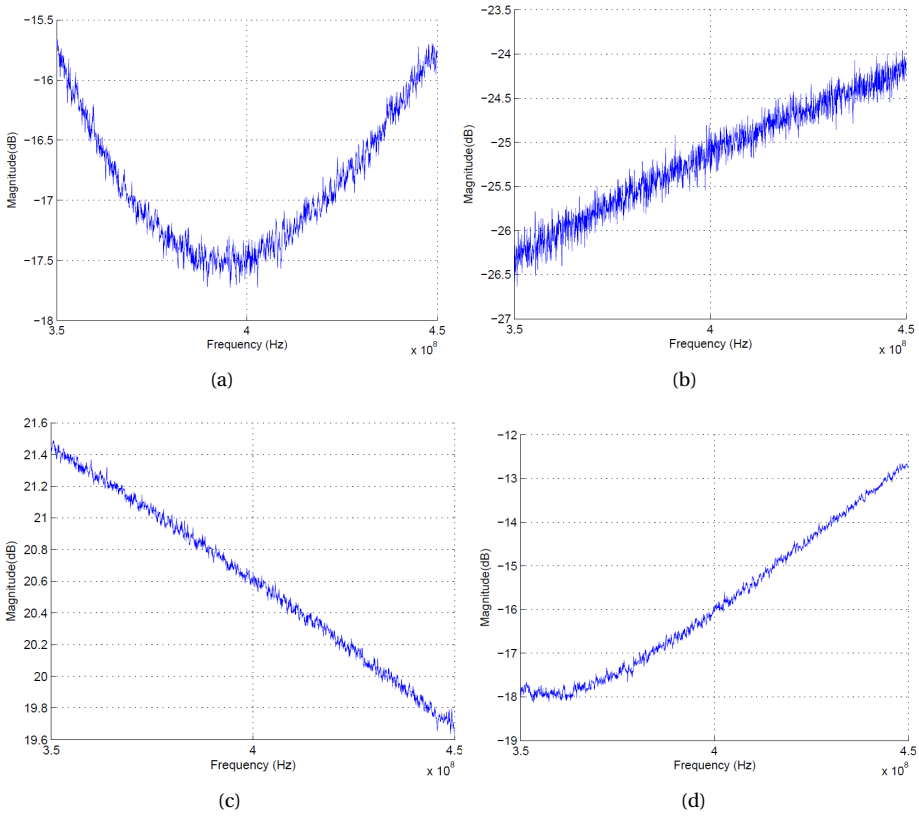

Figure 5.16: The measured (a) S11, (b) S12, (c) S21 and (d) S22 of the input LNA

The measurements have been conducted using 50 Ω as a reference impedance. The measured gain is around 20 dB at 400MHz. The input and output impedances are close to 50 Ω (S11 and S22 < -15 dB), which ensures proper input matching and output matching. Fig. 5.17 depicts the measured S-parameters of the second and third LNA. The gain is roughly 19 dB and the S11 is around -8 dB. Although S11 is above -10 dB, the output impedance is still close to 50 Ω, therefore the selectivity of the front-end is good enough to block side band interference. The behavior of the second and third LNA strongly depends on the PCB and the passive devices of the matching networks.

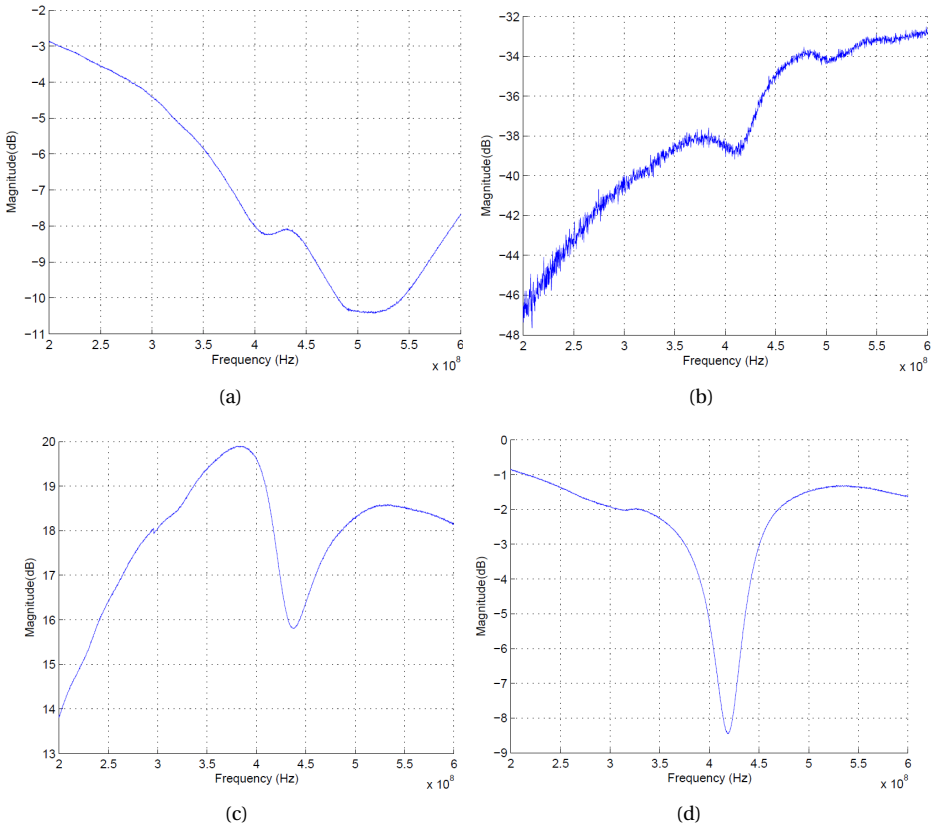

Figure 5.17: The measured (a) S11, (b) S12, (c) S21 and (d) S22 of the second and third LNA

The S11, S21, in band gain and in band noise figure of the complete RF front-end are shown in Fig. 5.18. In Fig. 5.18(b), the measurement is performed using a 40 dB attenuator to prevent that the RF front-end becomes saturated. Fig. 5.18(c) shows the absolute gain of the RF front-end with a calibrated input signal. Fig. 5.18(d) shows the RF front-end noise figure, which is around 0.9 dB.

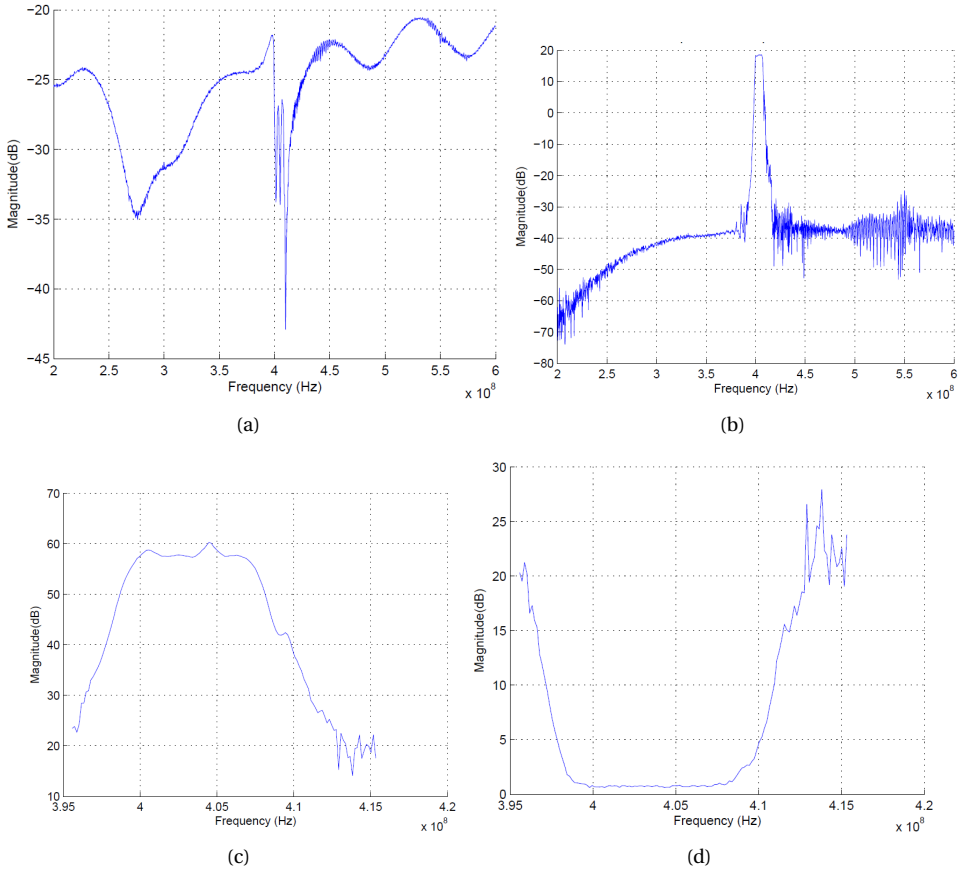

Figure 5.18: The measured (a) S11, (b) S21, (c) in band gain and (d) in band noise figure of the total RF front-end

LF BACK-END

This section presents the measurements of the LF back-end of the data receiver. Fig. 5.19 presents the measured output signal of the envelope detector. After down conversion, the output signal has residue RF components that are filtered out by the base-band filter.

The filtered and amplified base-band signal is shown in Fig. 5.20. In the same figure, the average of the base-band signal is presented.

Both base-band and average signals are compared in the last stage of the LF back-end, generating the output bitstream of the receiver. Fig. 5.21 presents the output of the comparator that corresponds to the bitstream of the data receiver.

In general the data receiver requires very high gain and selectivity to operate in the MICS band. The gain and selectivity requirements (gain > 50dB and selectivity of 4 MHz) of this receiver bring us to the conclusion that this receiver topology is suitable for battery operated receivers, which is appropriate for a network that requires one hub/receiver

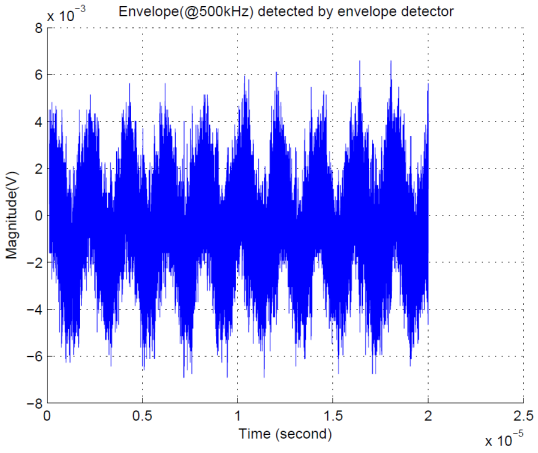

Figure 5.19: Measured output signal of the envelope detector.

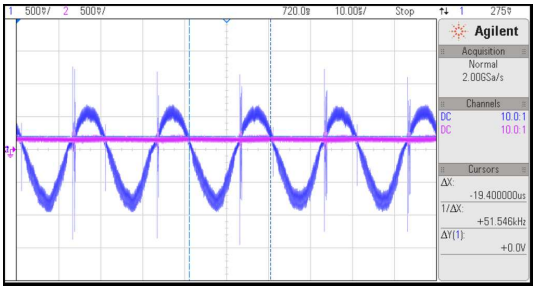

Figure 5.20: Measured base-band signal after filtering and amplification.

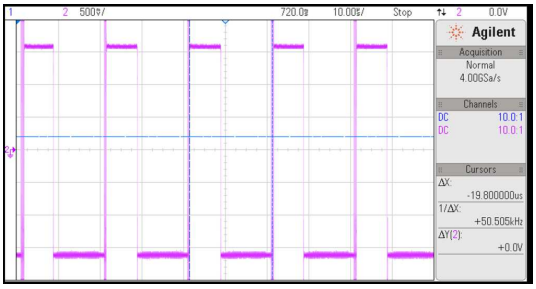

Figure 5.21: Measured bitstream of the LF back-end.

that communicates with peripheral autonomous wireless sensors. The total power consumption of the receiver is 100 mW from a 5V power supply. The LNA amplifiers in the RF front-end accounts for roughly 80% of the total power consumption.

5.2.4. CONCLUSIONS

In this chapter the design of an autonomous wireless sensor node (AWSN) with temperature monitoring has been presented. The AWSN comprises an RF energy harvester, a power management unit, a temperature dependent oscillator and an OOK backscattering transmitter. The AWSN is powered from a -18.2 dBm RF signal at 13.56 MHz and it modulates a 402 MHz signal. The total power consumption of the sensor node is 1.5 μW. In the second part of this chapter, the design of a data receiver to detect the transmitted signal of the AWSN is presented. The receiver consists of three low-noise amplifiers, a SAW filter and an envelope detector. The base-band signal is processed in the analog domain by a 20 dB gain amplifier, a filter, an averaging circuit and a comparator. The total gain of the RF front-end is 57 dB, the noise figure is 0.9 dB over a bandwidth of 4 MHz (within the MICS band). Power consumption is 100 mW from a 5V power supply.

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6

Autonomous Wireless Sensor Node with Asynchronous ECG Monitoring

The design of a 13.56MHz/402MHz autonomous wireless sensor node with asynchronous ECG monitoring for near field communication is presented. The sensor node consists of an RF energy harvester (RFEH), a power management unit, an ECG readout, a data encoder and an RF backscattering transmitter. The energy harvester supplies the system with 1.25 V and offers a power conversion efficiency of 19 % from a -13 dBm RF source at 13.56 MHz. The power management unit regulates the output voltage of the RFEH to supply the ECG readout with V_{ECG} *= 0.95 V and the data encoder with* V_{DE} *= 0.65 V. The ECG readout comprises an analog front-end (low noise amplifier and programmable voltage to current converter) and an asynchronous level crossing ADC with 8 bits resolution. The ADC output is encoded by a pulse generator that drives a backscattering transmitter at 402 MHz. The total power consumption of the sensor node circuitry is 9.7 µW for a data rate of 90 kb/s and heart rate of 70 bpm. The chip has been designed in a 0.18µm CMOS IC process and shows superior RF input power sensitivity and lower power consumption when compared to previous works.*

6.1. INTRODUCTION

Low power sensor node design is an important research topic since remote measurement of physical quantities became very attractive to the industry, especially for medical applications that implement the concept of Wireless Body Area Networks (WBAN). However, it is also known that the power consumption and battery lifetime of today's solutions limit the wider use of wireless sensor nodes in such networks.

Many wireless sensor nodes are designed to be autonomous or increase battery lifetime [1–7]. As an example [5] presents a design that relies on a hybrid energy harvesting solution with external energy storage devices and power gating techniques to bring the power consumption to an average of tens of micro-watts. Although promising, previously designed systems use synchronous sampling and synchronous data transmission [8–12], and thereby consume power even when there is no or little sensor activity. A possible solution to minimize power consumption is the use of asynchronous sensor architectures that sample and transmit data only when an event is detected. An event-driven sensor consumes minimal power unless an event is detected. Therefore, on average, it consumes less power than state of the art synchronous systems. In addition, lower average data rate is required in data transmission due to the nature of the data conversion applied to the asynchronous system. The challenge to design an event-driven sensor is the very low power consumption of the circuits while keeping high linearity. Secondly, also the data transmission must be asynchronous, which makes data encoding more difficult to implement.

The goal of this work is to present the design of asynchronous ECG monitoring and data transmission, which reduces the power consumption of the sensor node (below 10 μW) [13, 14] without the use of power gating and requiring neither external energy storage devices nor a crystal as a time reference. The autonomous wireless sensor utilizes near field communication and is designed in 0.18μm CMOS IC technology with a sensitivity of -13 dBm (at 13.56 MHz), asynchronous 8-bit ECG readout and backscattering data transmission at 402 MHz.

The chapter is organized as follows. In Section 6.2 the design of the autonomous wireless sensor with ECG monitoring is presented. Section 6.3 presents the experimental

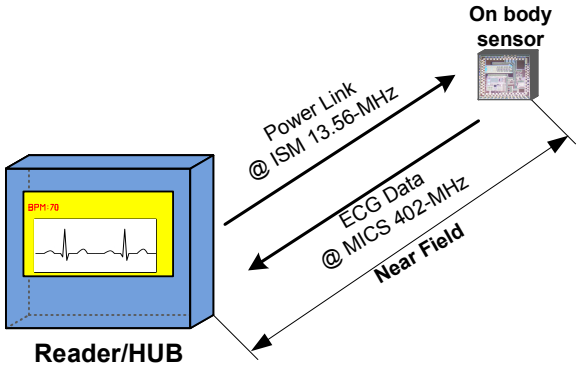


Figure 6.1: Diagram of communication between a hub and a sensor.

results and comparison with the state of the art. Conclusions are drawn in Section 6.4.

6.2. AUTONOMOUS WIRELESS ECG SENSOR DESIGN

This section presents the proposed autonomous wireless sensor with ECG monitoring and describes the main circuits of the system. The designed sensor is suitable for star network topologies since this topology allows near field direct communication from the sensor to the hub while the hub provides power to the sensor, as depicted in Fig. 6.1.

The sensor node, which is remotely powered by the hub, is a peripheral device of the network that sends data to the hub at the detection of an event. The data processing and memory allocation will be done by the hub. Therefore, the sensor node can operate from very little power.

The 13.56 MHz ISM band is used to power the IC since in this band it is allowed to transmit high levels of power. However, the 13.56 MHz ISM band does not allow a bandwidth greater than 13 kHz, which is not enough for the application at hand. On the other hand, the 402 MHz MICS band allows broader band data transmission (>1 MHz) if the signal is transmitted 25 dB below the maximum MICS EIRP thus below 25 uW. In addition, in the ISM band the interference might be very strong since the maximum EIRP is roughly 2 W. We thus propose to use the ISM band for powering the sensor node and the 402 MHz MICS band for data communication.

Fig. 6.2 shows the block diagram of the MICS/ISM band sensor node that comprises an RF energy harvester (RFEH), a power management unit for voltage regulation and bias current generation, an 8-bit analog front-end (AFE) with a level-crossing sampling ADC for ECG data acquisition, a serial pulse encoder and a passive on-off keying (OOK) MICS-band transmitter. The dual-band feature allows for simultaneous backscattering data transmission and energy harvesting. The sensor node employs no duty-cycling/gating techniques and requires only three external components: two antennas (similar to previous works) and an on-PCB tuning inductor designed for 402MHz. No external crystal, resonator or storage capacitor is required, which enhances system integration.

The sensor node design presented in this chapter illustrates that asynchronous operation results in a system with 35 % lower data rate and a 41 % lower power consumption

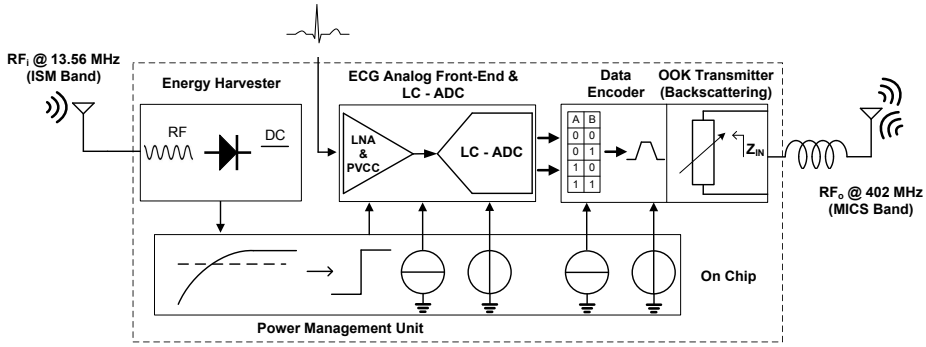


Figure 6.2: Block diagram of the MICS/ISM band sensor node.

than state of the art synchronous system designs.

6.2.1. RF ENERGY HARVESTING AND POWER MANAGEMENT

The theoretical model and analysis of the RF energy harvester designed in this work have been presented in [15] and in Chapter 3 of this thesis. Fig. 6.3 shows the block diagram of the designed RFEH that comprises a passive voltage boosting network and an orthogonally switching charge pump rectifier (OS-CPR). The circuit diagram of the boosting network and on-chip OS-CPR are shown in Fig. 6.4(a) and Fig. 6.4(b).

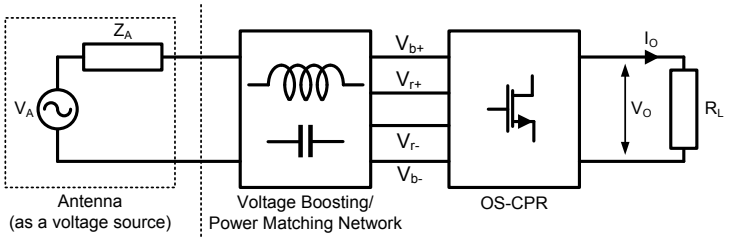


Figure 6.3: Block diagram of the RF energy harvester [15].

To adequately drive the OS-CPR, the boosting network delivers large swing control (V_{b+} and V_{b-}) and energy signals (V_{r+} and V_{r-}). The resonant circuit of the boosting network is modeled by the self-inductance of the antenna, L_A (9.5 μH), its series resistance, R_A (12 Ω) and capacitance $C_{V,T}$ (14 pF), which is the sum of the on-chip tuning capacitance (C_D and C_B) and input capacitance of the rectifier ($C_{R,T}$). An inductive choke L_C provides a DC short at the input terminals of the rectifier to ensure a zero DC offset error at the input of the OS-CPR. In the boosting network design there is a trade-off between the value of $C_{V,T}$ and L_A. If L_A is made too large to increase voltage gain, $C_{V,T}$ has to be

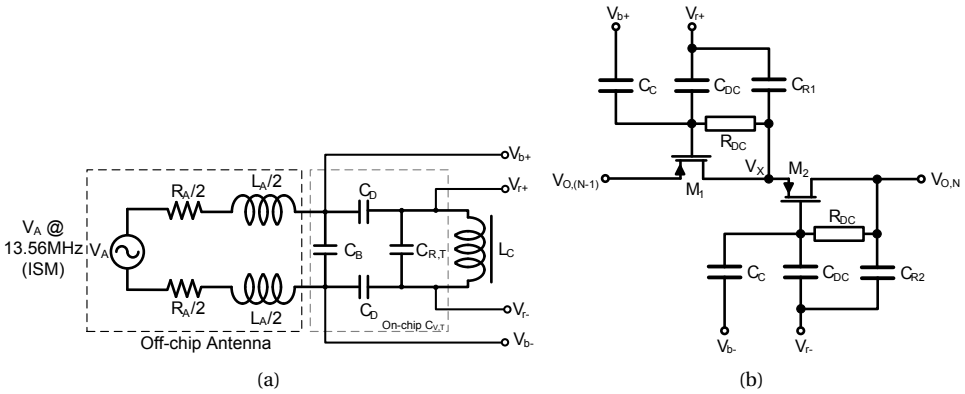


Figure 6.4: Circuit diagram of (a) the boosting network and (b) a single stage of the on-chip rectifier in the RFEH [15].

very small. In such a case, the resonance frequency will be too sensitive to the rectifier input capacitance that changes with the load and input power. Moreover, increasing the value of L_A requires an inductor that is physically bigger and consequently has a larger R_A, which limits the voltage gain of the boosting network.

The rectifier circuitry (of a single stage) is made up of PMOS transistors as voltage-controlled switches (M_1 and M_2) and capacitors for AC coupling (C_C) and energy storage (C_{R1} and C_{R2}). Table 6.1 shows the component values of the designed RFEH, in which the RFEH input impedance of the chip is roughly (16 - j815) Ω.

Table 6.1: RFEH Device Values

Device	Value	Device	Value
C_B	7.5 pF	C_{DC}	≃90 fF
C_D	19.5 pF	R_{DC}	350 kΩ
$C_{R,T}$	≃17 pF	C_{R1}, C_{R2}	9.7 pF
C_C	9 pF	$W/L_{M_1,M_2}$	750/0.2

Fig. 6.5 shows the various voltage waveforms in the charge pump rectifier. Each stage has two different DC voltage levels (V_{CR1} and V_{CR2}) and AC voltages that are provided by the boosting network. Due to DC voltage differences within the stage, the transistors may conduct current in the backward direction in the phase they should be turned off. Known as flow-back current this effect reduces the efficiency of the rectifier. To reduce the flow-back current, parasitic capacitances C_{DC} and resistors R_{DC} set the DC voltages V_{CR1} and V_{CR2} at the gate of M_1 and M_2, respectively, to guarantee that the drain and source potentials are smaller than the gate potential in the off phase.

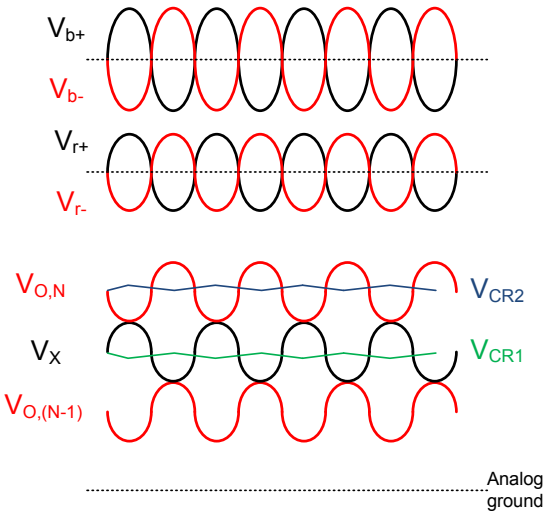


Figure 6.5: Waveforms of the OS-CPR integrated in the RFEH.

The design procedure of the RFEH is [15]:

1. Calculate the self-inductance ($L_A = R_A Q \omega^{-1}$) and tuning capacitance ($C_{V,T} = (\omega^2 L_A)^{-1}$) of the boosting network.
2. Calculate the voltage swings of the rectifier (V_r) and control signals (V_b).
3. Determine the number of stages (N).
4. Determine the aspect ratios (W/L) of transistors M_1 and M_2 from the model.
5. Determine C_C which has to be bigger than the gate-source capacitance of M_1 and M_2.
6. For minimum ripple, calculate C_{R1} and C_{R2}.
7. Run PSS, PAC simulations or transient with dfft analysis.
8. Fine-tune $C_{V,T}$ and/or the OS-CPR component values for frequency optimization.
9. Repeat steps 3-8 for optimization.

From -13 dBm 13.56 MHz input RF power, the output of the 5-stage OS-CPR sets the power supply voltage ($V_{DC} = V_{O,N}$) of the sensor node at 1.25 V for a resistive load of 110 kΩ with 19 % power conversion efficiency. The RFEH shows similar behavior when connected to the equivalent resistance of the sensor circuitry, which is about 150 kΩ.

The all CMOS-based, subthreshold operated power management unit is shown in Fig. 6.6. It includes voltage (V_{REF}) and current (I_{REF}) references and two linear voltage regulators that supply the ECG analog front-end (V_{ECG}) and the asynchronous data encoder (V_{DE}). Proper selection of R1, R2 and N sets temperature-independent voltage reference V_{REF} at 0.54 V, which is derived by combining PTAT and CTAT voltages V_{R2} and $V_{GS,4}$, respectively. Current reference I_{REF} (10 nA) is required for circuits in the ECG AFE and transmitter. Regulated voltages V_{ECG} and V_{DE} vary ≤13 % for 8 dB (-9±4 dBm) change in input power. All power supplies are filtered using on-chip decoupling capacitors.

6.2.2. ANALOG FRONT-END AND LEVEL-CROSSING ADC

As shown in Fig. 6.7, the ECG monitoring front-end comprises a fully-differential low noise amplifier (LNA), a programmable voltage-to-current converter (PVCC) and a current-mode level-crossing analog-to-digital converter (LC-ADC). The sparse ECG signal with long periods of low frequency variation requires the LC-ADC to hold the comparison window for a long time (hundreds of ms). Therefore the LC-ADC in the proposed AFE operates in the current domain instead of the charge domain [16].

The LNA is configured as a band-pass filter with a voltage gain (C_{AC}/C_1) of 34 dB from 0.06 Hz to 950 Hz. Pseudo-resistor R_{PSEUDO} and negative feedback capacitor C_1 set the lower cutoff frequency, and the voltage gain and bandwidth of op-amp A_1 set the upper cutoff frequency. For a 6 mVpp input signal, the input referred noise and total harmonic distortion (THD) values are 3.77 μVrms and 0.15 %, respectively. Switches S_1 set the input common-mode voltage at start-up. To increase the input impedance, a positive feedback loop (via capacitor C_2) is introduced. The PVCC is a fully differential

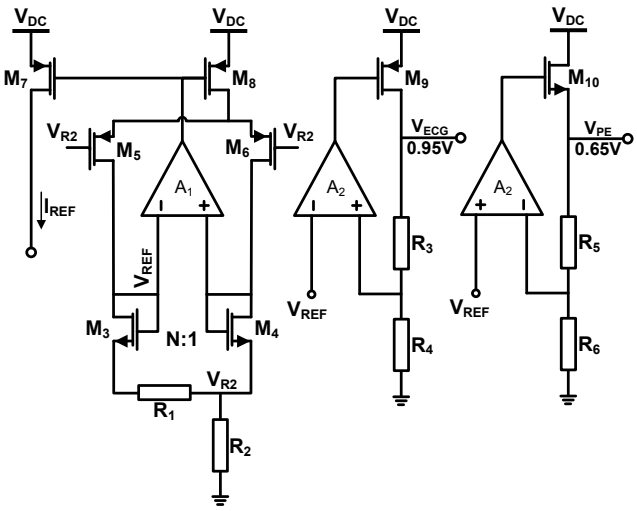


Figure 6.6: Circuit diagram of the power management unit.

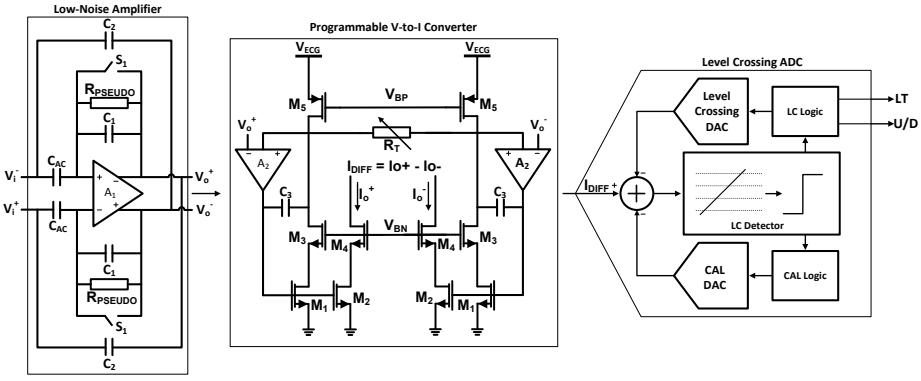


Figure 6.7: Circuit diagram of the ECG monitoring analog front-end [16].

programmable gain (2 μA/V to 16 μA/V) transconductance (voltage-to-current) amplifier. Its output current is fed into the LC-ADC. The LC-ADC employs two complementary DACs. The level-crossing DAC adjusts the comparison window after each conversion by adding/subtracting current at the input node of the level-crossing (LC) detector. The calibration DAC (CAL DAC) cancels any DC offset during system reset. The residue current is fed to the level-crossing detector, which outputs a pulse in case of a level crossing. Unlike uniform sampling, the level-transition (LT) and UP/DOWN (U/D) pulse sequences are generated only when the input signal crosses a predefined threshold level as illustrated in Fig. 6.8. The ECG readout circuits include two RC oscillators on the chip for generating a synchronous clock signal to calibrate the offset of the two DACs, respectively. The oscillators are only enabled for calibration during reset. The offset calibration is a typical foreground calibration that is enabled during system startup or manual re-

setting. The entire ECG front-end achieves a measured SNDR of around 48 dB when a 6 mVpp sinusoidal input signal is applied at the input of the LNA. More details on the ECG monitoring front-end are provided in [16].

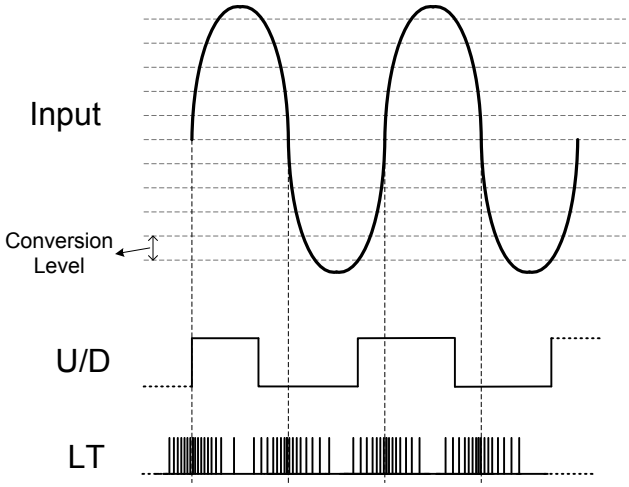


Figure 6.8: Input and output signals of the level-crossing ADC.

6.2.3. ASYNCHRONOUS DATA TRANSMISSION

The level-crossing ADC provides two binary signals (LT and U/D) that are both fed to the low-power data transmitter. As the transmitter is powered by an RF energy harvester, to minimize power consumption, the data transmission is only enabled when ADC data conversion is active [17]. The 2 output bits of the ADC are combined and transmitted simultaneously, otherwise information would be lost. Employing pulse duration modulation (PDM), the 2-bit data stream is combined to generate pulses with different time duration for upward conversion and downward conversion. This means that the transmitter produces a pulse when LT indicates a conversion and U/D defines the duration of this pulse. In this way the 2-bit information can be embedded in a single pulse. Fig. 6.9 presents the circuit diagram of the transmitter that includes a digital pulse encoder and a backscattering network. The pulses are generated by comparing LT to $\overline{\text{LT}}$, the latter being the complement of LT delayed by six cascaded current starved inverters. The delay time is set by U/D that makes the pulses longer when it is set to '1'.

The delay is defined by the current drawn in the inverters and capacitor C_{DL}. For U/D equal to '1' (upward level crossing) C_{DL} is connected to ground, thus the pulse width is longer. For U/D equal to '0' (downward level crossing) C_{DL} is disconnected from ground, thus the duration of the pulses is shorter. Fig. 6.10 shows the waveforms of the low-power pulse encoder: the pulse duration is t_U for upward conversion and t_D for downward conversion. In the circuit designed for backscattering data transmission, the pulsed signal modulates the 402MHz RF signal received in the LC network, implementing ON-OFF-Keying modulation through transistor M_0 (see Fig. 6.9). The values of L_S and C_S are 32 nH and 4.9 pF, respectively.

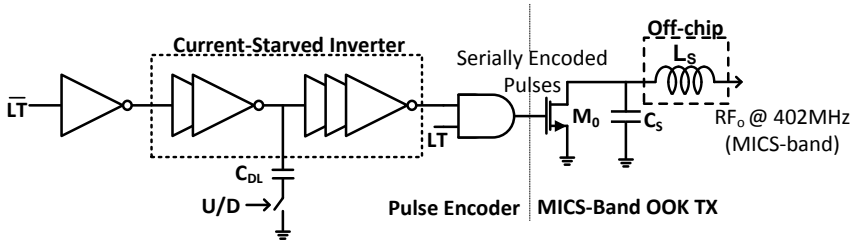


Figure 6.9: Circuit diagram of the asynchronous transmitter.

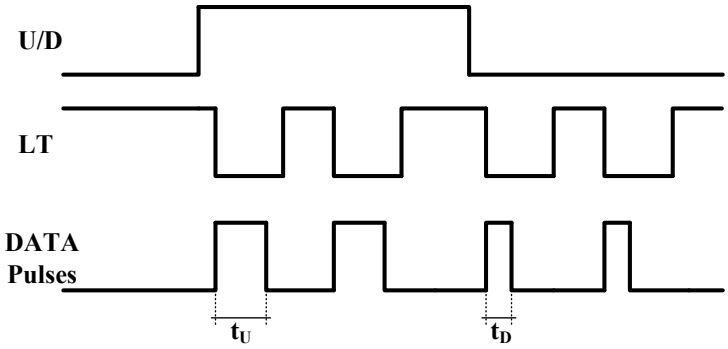


Figure 6.10: Waveforms of the asynchronous encoder.

Fig. 6.11 shows the power distribution, in percentage, of the blocks in the designed sensor node.

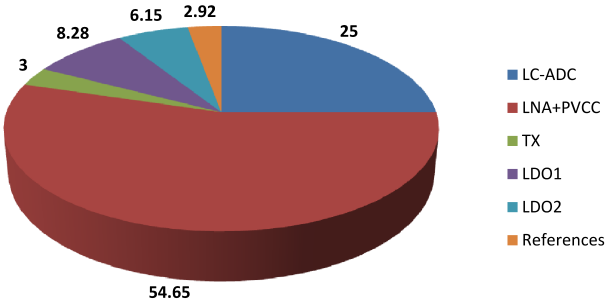


Figure 6.11: Power consumption per block in percentage.

6.3. EXPERIMENTAL RESULTS

Realized in low-cost 0.18μm CMOS IC technology, the ISM/MICS-band autonomous wireless sensor node with the asynchronous 8-bit ECG AFE occupies 1.9 x 2.0 mm^2 and is shown in Fig. 6.12. The sensor node is mounted on a double-sided, FR-4 laminate substrate with a high quality factor coil (antenna) etched on the back plate (see Fig. 6.13). The physical and electrical properties of the customized antenna coil are presented in Table 6.2. The coil is modeled using ADS Momentum. At 13.56 MHz, the measured real and imaginary impedance components of the antenna coil are 12.7 Ω and 810 Ω, respectively. Simulation and measurement results show less than 5 % discrepancy.

The energy harvester operates over a large range of resistive loads (0.1 MΩ to 0.82 MΩ). Defined as the ratio of the electrical power delivered to the load and the power

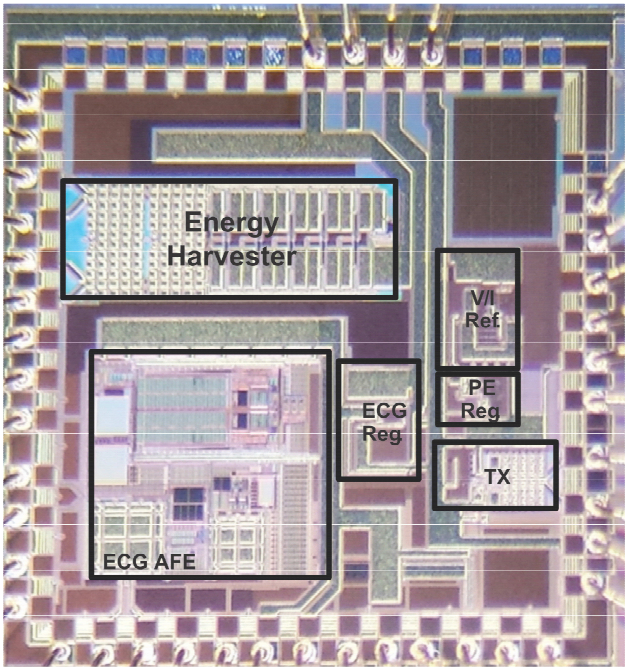


Figure 6.12: Chip micrograph of the autonomous ECG wireless sensor node.

Table 6.2: Physical and electrical properties of the antenna

Physical	1/2 oz. 1.55 mm	Electrical	@13.56 MHz
Outer dim. (mm^2)	56 x 50	L_A (μH)	9.5
Inner dim. (mm^2)	48 x 42	R_A (Ω)	12
Trace width (mm)	0.25	C_A (pF)	2.4
Trace space (mm)	0.25	f_{SR} (MHz)	33
No. of turns	8	Q-factor	67

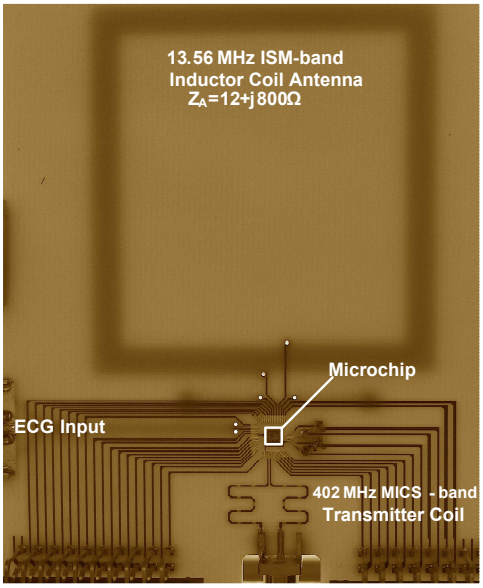


Figure 6.13: FR-4 PCB for sensor node test.

received by the antenna, the power conversion efficiency (PCE) equals 19 % for a 110 kΩ load at -13 dBm input power (P_{IN}), as shown in Fig. 6.14.

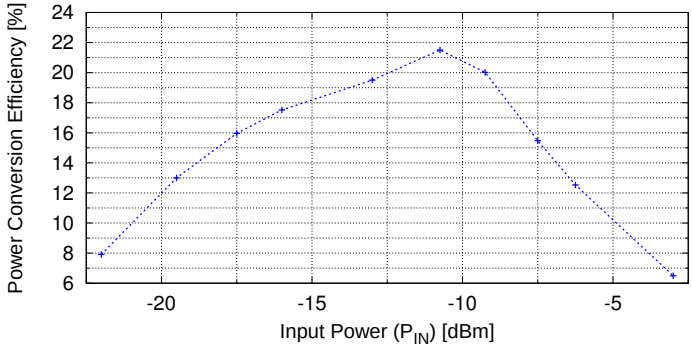


Figure 6.14: Measured RFEH power conversion efficiency as a function of input power for a 110 kΩ load.

The input power has been calibrated by using a Power Network Analyzer (PNA). The two ports of the PNA were connected to two aligned coils, being the same coils used in

the chip test, separated by a distance of 20 cm. After measuring the scattering parameters, the data was inserted in a transformer model to calculate the coupling coefficient. With the coupling coefficient, it is possible to calculate the power received by the antenna taking into account the chip input impedance that is (16 - j815) Ω.

Fig. 6.15 shows the ECG front-end supply voltage (V_{ECG}) and the data encoder supply voltage (V_{DE}) as a function of the input power demonstrating that both supply voltages vary ≤13 % for −13 dBm ≤ P_{IN} ≤ −5 dBm.

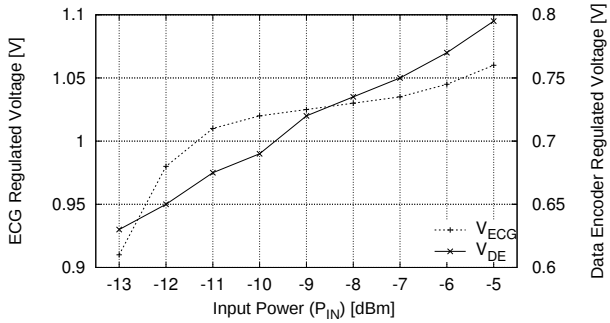


Figure 6.15: Measured ECG monitoring and data encoder supply voltages as a function of input power.

The measured low noise amplifier gain and SNDR of the ECG monitoring front-end over frequency are presented in Fig. 6.16 and Fig. 6.17, respectively. The plot proves the performance of the ECG front-end with 34 dB gain from 0.06 Hz to 950 Hz and 48 dB SNDR for an input voltage of 6 mV. The LC-ADC has magnitude resolution and time resolution. As time resolution is included in the measurement, the overall SNDR is degraded compared to the standalone LNA SNDR.

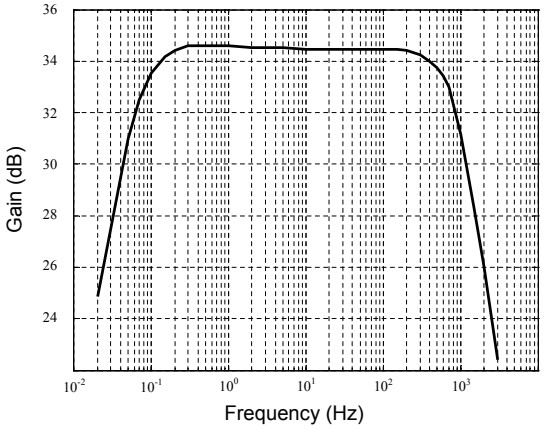


Figure 6.16: Measured gain and bandwidth of the low noise amplifier.

Fig. 6.18 shows the link margin of the system. The link margin is measured using

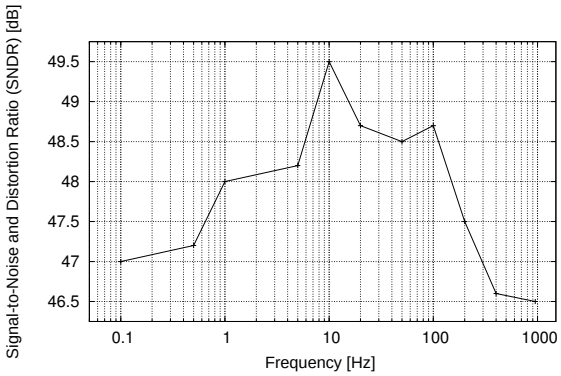


Figure 6.17: Measured total SNDR of the ECG monitoring front-end.

a commercial antenna from YAGEO (Phycomp part no. CAN4313 121 200431B). Since the TX is realized with backscattering, if a reader (hub) transmits the maximum allowed EIRP in the 402-MHz MICS band (-16 dBm), at a distance of 20 cm between the reader and the sensor and using the receiver as presented in this manuscript, reliable detection of the signal is still feasible. The reader receives a power of roughly -76 dBm and an LNA with about 50 dB gain is required to be able to cover distances up to 20 cm. For longer distances the received power is too low, < -80 dBm, and thus a more sensitive envelope detector would be necessary or the LNA would need more than 50 dB of gain. For an EIRP of 2 W at 13.56 MHz, the sensor node can be placed at a distance of 40 cm from the hub to receive an RF power of -13 dBm. At 40 cm the required sensitivity of the MICS receiver is -87 dBm. Beyond 40 cm the sensor node cannot be powered as the ISM RF power received by the antenna is smaller than -13 dBm (i.e., the minimum required RF power).

Fig. 6.19(a) and Fig. 6.19(b) illustrate the measured waveforms of the asynchronous

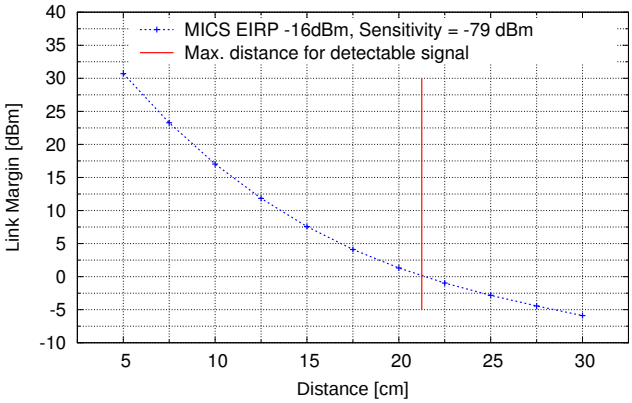
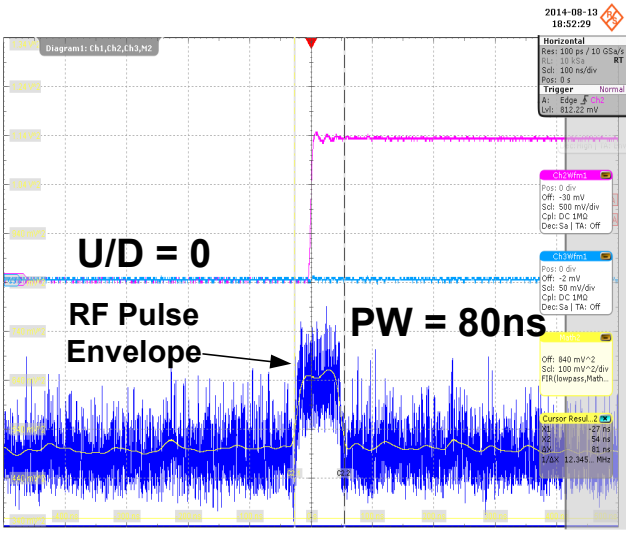
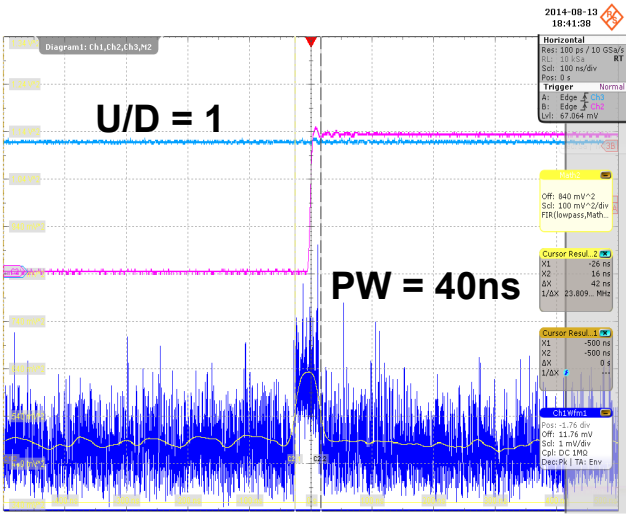


Figure 6.18: Estimated link margin for data transmission in the 402MHz MICS band.

pulse encoder. In Fig. 6.19(a) the output of the pulse encoder is presented for a LT transition with U/D = 0. In this condition the pulse width is 80ns. For a LT transition with U/D = 1, the pulse width equals 40ns, as shown in Fig. 6.19(b).



(a)



(b)

Figure 6.19: Measured encoder output waveforms: (a) 80 ns for U/D = 0 and (b) 40 ns for U/D = 1.

The output signals of the sensor node are shown in Fig. 6.20. In this measurement

an input voltage of 2.5mV peak to peak is applied to the input and the sensor node is remotely powered by an RF signal of -13 dBm.

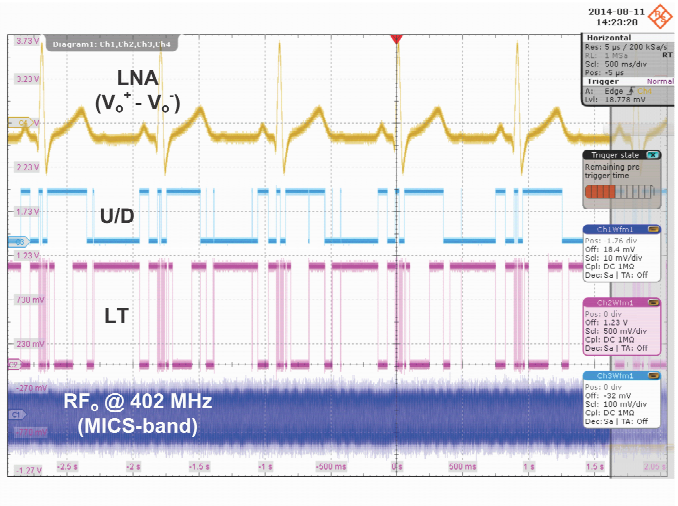


Figure 6.20: Measured output signals of the sensor node.

For system validation, the ECG waveform is reconstructed from the RF signal available from the output of the MICS-band OOK transmitter. Fig. 6.21 shows the measured and reconstructed ECG waveform. In the measurement, the output of the transmitter is connected to an envelope detector, followed by an IF amplifier, as depicted in Fig. 6.22. The IF amplifier amplifies the 25MHz base-band signal and filters unwanted RF noise.

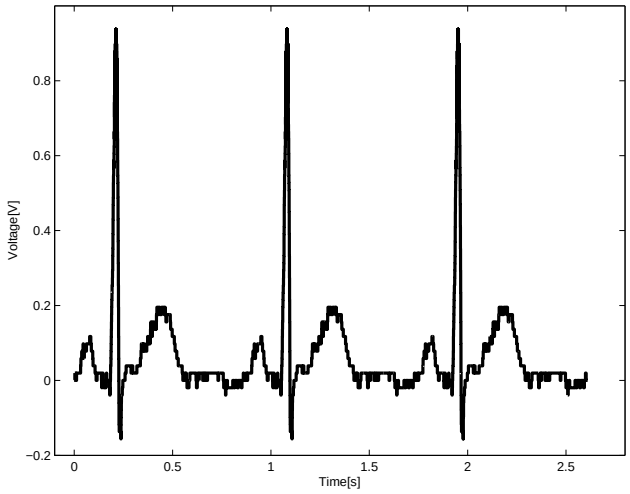


Figure 6.21: ECG signal reconstructed from data transmitted by the sensor node.

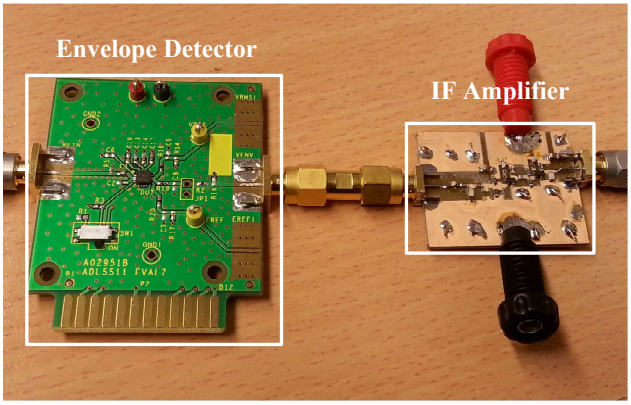


Figure 6.22: Envelope detector and IF amplifier used in the ECG waveform reconstruction.

For the applied ECG signal the ADC converts on average 45k times in one second. Since each conversion includes 2 bits, thus we can say that the sensor has a data rate of 90 kbits per second. This value, however, is not fixed and the date rate depends on the number of conversions made. A higher input frequency would require a higher data rate, but the analog front-end limits the maximum frequency to 1 kHz. Hence, a maximum data rate in the range of hundreds of kb/s is expected. Fig. 6.23 shows the measured power consumption of the sensor node as a function of the data rate.

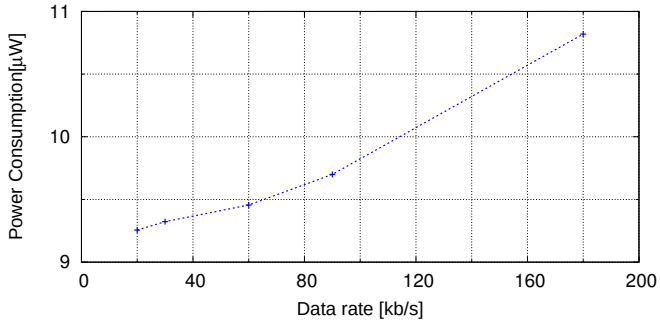


Figure 6.23: Measured power consumption as a function of data rate.

Table 6.3 compares the performance of this work with that of recently published designs. Among the many parameters shown in Table 6.3, this work demonstrates superior design characteristics, such as high sensitivity (-13 dBm), lower average sampling rate and high system integration with three external components. The power consumption is 9.7 μW, which is 41 % lower than the state of the art.

Table 6.3: Summary and comparison of the sensor node with previously published designs

Specifications	**This Work**	[1]	[2]	[3]	[4]
Application	Near-Field ECG Monitoring	Far-Field Neural Recording	Far-Field General purpose	Near-Field ECG Monitoring	Far-Field General purpose
Type of Sensor	ECG	Neural	EEG, EMG	ECG	ECG, EEG and EMG
Type of Energy Harvesting	RF	RF	RF	Battery	RF/Thermal
Sensitivity (dBm)	-13	-8	-12	n.a.	$-10^{\S}$
Supply Voltage (V)	1.25	0.8	1.8	1.2/3	1.35
Number of Analog Channel(s)	1	1	1	1	4
ADC Resolution (bits)	8	8	8	12	8
Input referred noise (V)	16.8μVrms†	14.5μVrms	1.25μVrms	1.5μVrms†	$<2\mu$Vrms
Frequency (MHz)	13.56/402	915	900	13.56	402/433
Data Rate (kb/s)	90	150-800	up to 500	424	200
External Components	1 TX Inductor	n.a.	Storage Capacitor	1 Crystal, NFC IC	2 Crystals, Storage Cap. and TX Inductor
Power Consumption (μW)	9.7	20	16.6	18.24	19
Active blocks for power consumption measurement	1-Ch. FE, 8bit ADC, PE and TX	1-Ch. FE, 8bit ADC, Logic RX and TX	1-Ch. FE, 8bit ADC, Logic and TX	1-Ch. FE, 12bit ADC, MCU, SRAM and FeRAM	1-Ch. FE, 8bit ADC, DSP and 0.013% Duty Cycled TX
Modulation (TX)	OOK	OOK	ASK	ASK	BFSK
Area (mm^2)	1.9x2.0	0.96x1.6	2.0	6.9x6.9	3.3x2.5
Technology CMOS (μm)	0.18	0.13	0.13	0.13	0.13

† Input referred noise calculated for 6mV input voltage.

‡ Including test structure on the PCB such as connectors, trace lines and antennas without size optimization.

§ -10 dBm is used for sensor kick-start only.

6.4. CONCLUSION

A 13.56/402 MHz autonomous wireless sensor node with ECG monitoring has been fabricated in standard 0.18 μm CMOS IC technology. Powered from a -13 dBm RF signal at 13.56 MHz, the energy harvester achieves a maximum power conversion efficiency of 19 %. Asynchronous data encoding has been demonstrated. The total power consumption of the ECG sensor node is 9.7 μW for a data rate of 90 kb/s.

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7

CONCLUSIONS

In this chapter the conclusions of the thesis are presented. Chapters 2 until 6 that describe the review of the state of the art and the technical developments of this work are summarized. The outcomes from the chapters are analyzed and recommendations for future work are presented.

7.1. CONCLUSIONS

In Chapter 2, relevant prior art has been reviewed and advantages and disadvantages of the techniques described therein have been discussed. The reviewed topics are RF energy harvesting, UWB transmitters and wireless sensor nodes for slowly varying signals. In the review of RF energy harvesting, the most relevant charge pump rectifier topologies have been presented and discussed. The UWB transmitter section presented low power transmitters with a focus on the topologies developed to operate in the sub-GHz and 3-10 GHz bands. Finally, state of the art wireless sensor node topologies for remote monitoring of slowly varying signals have been presented and discussed.

The design of an orthogonally switching charge-pump rectifier with high power conversion efficiency has been presented in Chapter 3. The charge pump rectifier (CPR) comprises MOS transistors as voltage-controlled switches. Analytical models and simulation results in 90nm IC technology show that a 5-stage 915 MHz CPR with a 1 MΩ load achieves a DC voltage of 1.35 V and a power conversion efficiency (PCE) of 11.9% at -18.2 dBm available input power. The analytical analysis presents less than 30% difference from circuit simulation results of the RF energy harvester in 90nm and 180nm IC technology when operating at 13.56MHz. Simulation results show that the CPR is both technology and frequency scalable. Measurement results of the RF energy harvester employing a 5-stage CPR designed in 180nm CMOS IC technology have been presented. Three different definitions of input power were presented and included in the power conversion efficiency measurement results. Taking into account the theoretical input power definition ($P_{INtheor.}$), the maximum PCE achieved is 12.5% at -19 dBm input power.

The design of a low-power sub-GHz Ultra-Wide Band transmitter has been presented in Chapter 4. Low-power UWB transmitter analytical models and simulation results that validate the analysis have been demonstrated. The transmitter has been designed with off-the-shelf ATF551M4 transistors, on-PCB inductors and (SMD) capacitors. Measurements results show that the low-power UWB transmitter can operate from a low-voltage power supply (150mV) with an energy consumption of 85pJ/pulse for a peak-to-peak output voltage of 140mV and a pulse repetition frequency (PRF) of 3.3MHz. Measurement results show a roll-off of 25dB between 500 MHz and 1 GHz.

In Chapter 5 the design of an autonomous wireless sensor node (AWSN) with temperature monitoring has been presented. The AWSN comprises an RF energy harvester, a power management unit, a temperature dependent oscillator and an On-Off Keying backscattering transmitter. The AWSN is powered from a -18.2 dBm RF signal at 13.56 MHz and it modulates a 402 MHz signal. The total power consumption of the sensor node is 1.5 μW. In the second part of Chapter 5, the design of a data receiver to detect the transmitted signal of the AWSN has been presented. The receiver consists of three low-noise amplifiers, a SAW filter and an envelope detector. The base-band signal is processed in the analog domain by a 20 dB gain amplifier, a filter, an averaging circuit and a comparator. The total gain of the RF front-end is 57 dB, the noise figure is 0.9 dB with a selectivity of 4 MHz (within the MICS band). The power consumption is 100 mW from a 5V power supply.

Chapter 6 presents a 13.56/402 MHz autonomous wireless sensor node with ECG monitoring, which has been fabricated in standard 0.18 μm CMOS IC technology. Powered from a -13 dBm RF signal at 13.56 MHz, the energy harvester achieves a maximum

power conversion efficiency of 19 %. Asynchronous data encoding has been demonstrated. The total power consumption of the ECG sensor node is 9.7 μW, which is 41% lower power consumption compared to state of the art, for a data rate of 90 kb/s.

In summary, this thesis presents new technical developments regarding circuit design and modeling of RF energy harvesting and sub-GHz UWB transmission. The concepts of the circuits have been demonstrated with stand-alone measurements results and applied to low-power wireless sensor nodes. Moreover, an example of a data receiver for the wireless sensor nodes presented in this thesis has been described.

7.2. RECOMMENDATIONS

In future work, the low power UWB transmitter that operates in the sub-GHz band could be integrated in an IC since silicon integration increases symmetry and the smaller size of the devices reduces dynamic power consumption. Finally, an UWB receiver could be built to detect the data transmitted by the IC that includes an integrated version of the low-power UWB transmitter and signal reconstruction should be included to prove the concepts of the integrated transmitter and the receiver.

The low power UWB transmitter can be integrated into the ECG sensor. With the UWB transmitter embedded in the wireless sensor, a new data modulation scheme should be developed to code the level-crossing ADC output in a single impulse. The advantage of such a system is the fact that the data transmission is active, which increases the operation range. More important is the fact that UWB data transmission requires a short impulse, which allows more sensors (or channels) to be multiplexed during data transmission.

RF energy harvesting can be improved to absorb multi band frequencies, so the narrow band interferences within 250 MHz to 1 GHz are used to provide energy to the wireless sensor node.

As a consequence of the three recommendations mentioned before, the sensor could be tested to operate in a Point-to-Point communication network if the sensor, including transmitter and receiver, has low power consumption and allows for autonomous operation. In this way, the UWB data communication in the sub-GHz band would be a better alternative for Point-to-Point communication compared to 3-10 GHz UWB data communication.

SUMMARY

Since the Internet of Things (IoT) is expected to be the new technology to drive the semiconductor industry, significant research efforts have been made to develop new circuit and system techniques for autonomous/very low-power operation of wireless sensor nodes. Very low-power consumption of sensors is key to increase battery lifetime or allow for battery-less (autonomous) operation of sensors, which contributes to preventing or reducing the high maintenance costs of battery supplied sensors and reduce the amount of discarded batteries.

This thesis, entitled *Radio Frequency Energy Harvesting and Low Power Data Transmission for Autonomous Wireless Sensor Nodes*, presents very low-power consumption circuit and system techniques combined with energy harvesting that allow the creation of autonomous wireless sensor nodes. This work focuses on three main challenges: 1) how to improve energy harvesting efficiency, 2) how to minimize power consumption of data transmission and 3) how to combine low-power techniques and energy harvesting in a system. These challenges are addressed in this thesis with on-PCB and Integrated Circuits (IC) solutions.

The efficiency of radio frequency (RF) energy harvesting is improved by proposing a new topology of a charge-pump rectifier. The proposed topology uses a voltage boosting network to compensate for the voltage drop in the transistors. The new topology is presented and analyzed. Simulation results are compared to the analytical analysis and measurement results of the circuit that has been fabricated in a 0.18um CMOS technology and operates at 13.53 MHz.

Although the efficiency of RF energy harvesting is improved using the above technique, at the same time, low power techniques in data transmission should be developed to save energy. Pulse width modulation and impulse transmission techniques to minimize power consumption have been developed and are presented in this thesis.

The developed pulse modulation circuitry has been fabricated in 0.18um CMOS technology as part of a System on Chip (SoC). The new impulse transmitter topology for low-voltage low-power operation has been fabricated on PCB with micro-wave discrete components. Theoretical analysis, simulations and measurements results are shown to prove the impulse transmitter concept.

The circuits developed are integrated in a SoC with energy harvesting to prove the concept of autonomous wireless sensor nodes. Two sensor nodes have been designed and measured: one for autonomous temperature monitoring and the second for autonomous ECG monitoring. Both designs operate from wireless power without the use of batteries. Finally, the work developed in this thesis is summarized and future research possibilities are discussed.

SAMENVATTING

Omdat het Internet der Dingen (Engels: Internet of Things, IoT) verwacht wordt de halfgeleiderindustrie voort te stuwen worden er aanzienlijke pogingen gedaan om nieuwe circuit- en systeemtechnieken te ontwikkelen voor zelfstandige en zeer energiezuinige draadloze sensor-knooppunten. Een zeer laag vermogensverbruik van de sensoren is de sleutel tot het vergroten van de levensduur van de batterij of tot de batterijloze (autonome) werking van de sensoren en het hiermee verminderen van de hoeveelheid weggegooide batterijen.

Dit proefschrift, getiteld Radio Frequency Energy Harvesting and Low Power Data Transmission for Autonomous Wireless Sensor Nodes, vertaald in Oogsten van Radio-Frequente Energie en Laagvermogen Data-Transmissie voor Autonome Draadloze Sensor-Knooppunten, presenteert zeer vermogenszuinige circuit- en systeemtechnieken in combinatie met het oogsten van energie, hetgeen de realisatie van zelfstandige draadloze sensor-knooppunten mogelijk maakt. Dit werk richt zich op drie hoofd-uitdagingen: 1) hoe de efficiëntie van het oogsten van energie verbeterd kan worden, 2) hoe het vermogensverbruik van datatransmissie geminimaliseerd kan worden en 3) hoe laagvermogenstechnieken en het oogsten van energie gecombineerd kunnen worden in een enkel systeem. Deze uitdagingen worden in dit proefschrift behandeld aan de hand van oplossingen die zijn gerealiseerd op printplaat, middels discrete componenten, of middels geïntegreerde schakelingen (Engels: integrated circuits, ICs)

De efficiëntie van het oogsten van radio-frequente (RF) energie wordt verbeterd door een nieuwe topologie voor een ladingspomp-gelijkrichter voor te stellen. De voorgestelde topologie gebruikt een spannings-oppeppend netwerk om voor de spanningsval over de transistoren te compenseren. De nieuwe topologie wordt gepresenteerd en haar werking geanalyseerd. Simulatieresultaten worden vergeleken met de wiskundige analyse en meetresultaten van een schakeling die in een 0,18 μm CMOS-technologie wordt vervaardigd en werkt op 13,56 MHz.

Alhoewel de efficiëntie van het oogsten van RF-energie verbetert door het gebruik van bovenstaande techniek, dienen er tegelijkertijd laagvermogens-technieken in datatransmissie ontwikkeld te worden om energie te besparen. Pulsbreedte-modulatie- en impuls-transmissie-technieken worden ontwikkeld teneinde het vermogensverbruik te verminderen en worden gepresenteerd in dit proefschrift. De ontwikkelde pulsmodulatieschakeling is vervaardigd in 0,18 μm CMOS-technologie als onderdeel van een Systeem-op-een-Geïntegreerde-Schakeling (Engels: System on Chip, SoC). De nieuwe impulszender-topologie voor laagspannings- en laagvermogens-werking is vervaardigd middels discrete microgolf-componenten op een printplaat. Theoretische analyse, circuitsimulaties en -meetresultaten worden getoond om de juiste werking van het impulszender-concept aan te tonen.

De ontwikkelde schakelingen zijn geïntegreerd in een SoC met een energie-oogster om het concept van een zelfstandig draadloze sensor-knooppunt aan te tonen. Twee

sensor-knooppunten zijn ontworpen en bemeten: één voor het autonoom monitoren van temperatuur en de tweede voor het autonoom monitoren van het elektrocardiogram (ECG). Beide ontwerpen werken op draadloze energie zonder gebruik te maken van batterijen. Tenslotte wordt het werk dat is beschreven in dit proefschrift geanalyseerd en toekomstige onderzoeksmogelijkheden besproken.

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I would like to thank Marion for all her administrative support and being a wonderful person. Thank you to Wil, Ali and Atef that were always there to help me with all technical implementations and tape-outs. Thanks to Prof. John for his collaboration.

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I would like to thank Yongjia. I still remember the rainy day we were walking and thinking about a new collaboration, then we made our ECG sensor that I am really proud of and it is a proof that team work is much more successful, as Prof. Wouter always encouraged us. I hope one day we can work together again.

I want to apologize if I forgot someone and that is why I would like to thank everyone in the Microelectronics group for discussions and for your friendship.

I could not end this section without saying that Juliana, my wife, has the same first name of a Dutch queen and by destiny she came to live in the Netherlands. She left behind her job and the chance to be close to her family. She did that to support me during my PhD studies. Every single word in this thesis is written by me but co-authored by Juliana. This is the type of wife I always wanted, beautiful, smart and very brave. I cannot say only thank you, in fact there is no word to describe my gratitude.

Andre Luis Rodrigues Mansano
Delft, November 2016.

CURRICULUM VITÆ

Andre Luis RODRIGUES MANSANO

28-08-1982 Born in Jaboticabal, Brazil.

EDUCATION

2011–2016 PhD. Microelectronics
Delft University of Technology
Thesis: RADIO FREQUENCY ENERGY HARVESTING AND LOW POWER DATA TRANSMISSION FOR AUTONOMOUS WIRELESS SENSOR NODES
Promotor: Prof. dr. ir. Wouter A. Serdijn

2006–2009 Master in Electrical Engineering
Campinas State University

2001–2005 Bachelor in Electrical Engineering
State University of Sao Paulo

PROFESSIONAL EXPERIENCE

2016–Present **Analog Mixed-Signal IC Designer at Philips Research**

- Design and layout of very-low power and low-noise readout amplifiers for pixel charge detection.
- Design and layout of self-compensated Successive Approximation Ramp Generator for built-in self test structure.
- Application: designs for DNA sequencing reader products.

2015–2016 **Analog Mixed-Signal Test Consultant at NXP Semiconductor**

- Automation, Analysis and application of Defect Oriented Test Simulation System for Analog Mixed-Signal designs.
- Automation, Analysis and application of Voltage Stress simulation for Analog Mixed-Signal designs.
- Analysis of Physical defects on IC Level.
- Physical analysis and defect probability analysis of Angular sensor for ABS brake (KMI7 and KMA32x).

2010–2016 **PhD Candidate at Delft University of Technology**

- Research towards PhD. on RF Energy Harvesting, low-power data transmission and low-power wireless sensor node. Publications are listed in the last section of this thesis.

2007–2010 **Analog Mixed-Signal IC Designer at Freescale Semiconductor**

- Analog design for microcontroller applications, including: linear Regulator, Charge Pump, Low Voltage Inhibit, Power-On-Reset, Low Power Current Source, Band-gap Voltage References, Crystal Oscillator, IRC Oscillator, Soft-Startup, Switched Capacitor Amplifier and Switched Mode Power Supply for micro-controller IC.
- Additional experience, patents and products:
- Mixed Signal Simulations to validate system interface.
- Chip Top integration evaluation regarding IR Drops.
- Feasibility study of discrete power transistor to operate with the designed IC.
- IC Evaluation in the laboratory.
- Charge pump voltage regulator, USPTO 8,519,780.
- Switched-capacitor amplifier circuit, USPTO 8,198,937.
- MPC5668G: Power Management Controller for 32-bit MCU for Gateway Applications. 2007.
- MC56F8006: Programmable Gain Amplifier for Microcontroller Solution. 2009.
- MPC5510: Crystal Oscillator and Power Management for Microcontroller Solutions. 2008.

• HC08XX: Power Management and LCD-Driver
for Microcontroller Solutions. 2010.
• PPC5633MMLQ80: Power Management Controller for
32bit Microcontroller for Automotive Application. 2007.

2005 **Analog IC Designer at Freescale Semiconductor**

• Analog circuits design for power management business line.
Linear Regulator, Charge Pump and Soft-Start-up
for quick-supply products.

LANGUAGE SKILLS

- English, fluent spoken, read and written.
- Portuguese, native spoken, read and written.
- French, advanced listening, reading, intermediate speaking and writing.
- Dutch, basic.

List of Publications

Journal Papers

5. **A.L. Mansano and Wouter Serdijn**, *A 0.15V 250– 750 MHz FCC Compliant Ultra Wide Band Transmitter*, , (Review for re-submission).

4. **A.L. Mansano, Yongjia Li, Sumit Bagga and Wouter Serdijn**, *An Autonomous Wireless Sensor Node with Asynchronous ECG Monitoring in 0.18m CMOS*, Transactions on Biomedical Circuits and Systems, **10**, 602-611, (2016).

3. **Yongjia Li, A.L. Mansano, Duan Zhao and Wouter Serdijn**, *An ECG Recording Front-End with Continuous-Time Level-Crossing Sampling*, IEEE Transactions on Biomedical Circuits and Systems, **8**, 626-635, (2014).

2. **S. Bagga, A.L. Mansano, Wouter Serdijn et al**, *A Frequency-Selective Broadband Low-Noise Amplifier With Double-Loop Transformer Feedback*, IEEE Transactions on Circuits and Systems-I: Regular Papers, **61**, 1883-1891, (2014).

1. **A.L. Mansano, Sumit Bagga and Wouter Serdijn**, *A High Efficiency Orthogonally Switching Passive Charge Pump Rectifier for Energy Harvesters*, IEEE Transactions on Circuits and Systems-I: Regular Papers, **60**, 1959-1966, (2013).

Book Chapter

1. **Wouter Serdijn, A.L. Mansano and Mark Stoopman**, *Wearable Sensors: Fundamentals, Implementation and Applications, Chapter 4.2 Introduction to RF Energy Harvesting*, Elsevier Academic Press, (2014).

Conference Papers

3. **A.L. Mansano, Yongjia Li, Wouter Serdijn and S. Bagga**, *An Asynchronous Event-Driven Data Transmitter for Wireless ECG Sensor Node*, IEEE Biomedical Circuits and Systems Conference, 404-407, Lausanne, 22-24 Oct. (2014).

2. **A.L Mansano, S. Bagga and Wouter Serdijn**, *A 13.56/402 MHz Autonomous Wireless Sensor Node with -18.2dBm Sensitivity and Temperature monitoring in 0.18um CMOS*, IEEE European Solid-State Circuits Conference, 279-282, Venice, 22-26 Sep. (2014).

1. **S. Bagga, A.L. Mansano, Wouter Serdijn et al**, *A Frequency-Selective Nested Dual-Loop Broadband Low-Noise Amplifier in 90 nm CMOS*, IEEE European Solid-State Circuits Conference, 121-124, Bordeaux, 17-21 Sep. (2012).