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Design and processing of silicon and silicon carbide sensors

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DESIGN AND PROCESSING OF SILICON AND SILICON CARBIDE SENSORS

DESIGN AND PROCESSING OF SILICON AND SILICON CARBIDE SENSORS

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
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SUMMARY

Downscaling of transistors, also known as Moore's law, has been the main propelling force behind the microelectronics industry. This trend will eventually come to an end due to physical limitations, hence an alternative is required to further drive technological progress. This gave an incentive to evolve in other directions as well, also known as More than Moore (MtM). This concerns all technologies adding functionality to integrated circuits (IC), all packaged as a single system. This can be done by combining digital and non-digital elements, e.g. analog/RF, passives, microelectromechanical devices (MEMS), and so on. The non-digital elements are not necessarily scalable according to Moore's law. Therefore, in this thesis we investigated the possibilities of using silicon and silicon carbide (SiC) to fabricate a number of sensors, capable of measuring weak signals. This is done by having a multidisciplinary investigation spanning from electrical, to mechanical and optical domains.

In Chapter 2, a bulk micro-machined high sensitivity accelerometer was designed, simulated, fabricated and characterized. By employing non-linear behaviour of four long slender beams to support a proof-mass, an operating point has been obtained where extremely low spring stiffness occurs. An integrated IDT capacitive transducer is used to readout the displacement of the proof-mass. The integration of the capacitive transducer was made possible using trench isolation technique to electrically isolate the electrodes of the capacitor, all fabricated in the same bulk silicon. The devices were capped using Pyrex glass dies. A PCB containing readout ASIC was used to readout the accelerometer. The PCB was then connected to a high-resolution impedance readout system, forming a measurement system. The device, at it its lowest resonance frequency of 8.7 Hz, the capacitive sensitivity and the experimentally characterised noise floor of the readout chip, the theoretically obtainable system resolution equals 17.02 $ng/\sqrt{Hz}$. This work shows that the proof of concept is promising for future iterations.

In Chapter 3, SiC ultraviolet (UV) photodetectors are introduced along with key SiC processing steps. 4H-SiC has a significant advantage over silicon when dealing with certain applications such as UV and harsh environments. Thermally growing SiO_2 is one of the advantages of SiC over other wide bandgap (WBG) semiconductors. The oxidation of SiC was therefore investigated and characterized. The results showed a good fit with the DG-model but needs further investigation as to how the behaviour is in all crystal directions. Furthermore, 4H-SiC etching was also investigated by using the ICP and RIE processes. Subsequent chapters describe the devices which were fabricated using the findings in chapter 3 (except for CMOS devices). Thus these results from these experiments were used to fabricate MSM Schottky sensors for multi-sensing applications using various metallizations. The metals used are Mo, Ta/Pt, Pd, and Ni, where the last two showed the best dark current performance in the range of pA. The devices showed reasonable dark currents at 200 °C where Ni electrodes gave a dark current of ~ 223 pA at 20V bias. Al-

though Pt has a large metal workfunction, the dark current reached ~ 1.52 mA at 200 °C for the same bias. The tantalum adhesion layer has a lower metal workfunction at a value of 4.22 eV, hence a lower Schottky barrier height resulted, at around 0.6 eV. The reason for using Ta as an adhesion layer is because the Pt comes off when doing the Scotch tape test. It was assumed that due to metal stacking, the overall Schottky barrier would increase sufficiently high. The observed metal workfunction is ~ 0.8 eV which is higher than what would be expected for Ta/4H-SiC but is still lacking. Additionally, also the processing has an influence on the SBH. The ideality factors calculated using the standard IV method showed high values which means that the devices need improvement. This can be done for instance by annealing the devices at higher temperatures to improve the metal-semiconductor interface. Other alternatives may be the surface passivation prior to metallization which potentially can result in also lower leakage currents. An example of surface passivation can be done by inserting a dielectric such as aluminium oxide to passivate surface defects, but also preventing diffusion of metals. Although not characterized for its UV behaviour, the Mo metal, showed a Schottky barrier of about 1.2 eV which means that it can be used for optical detection. This metal is useful for high temperature applications and other harsh environments because it is a refractory metal. This allows the device to be used for high temperature applications where the device is used as a PTAT temperature sensor. The W5S5 devices with Mo electrodes were tested up to 200 °C and showed good temperature behaviour. The findings are encouraging to further investigate the device for multi-sensing applications targeted at harsh environments.

In addition to this device, dedicated devices for UV sensing and temperature sensing (SiC CMOS) were developed. The first is an avalanche photodiode which is advantageous for detecting weak ultraviolet signals thanks to its small size, low dark current, high multiplication gain, and high quantum efficiency. Such detectors can be used in a wide range of applications, e.g. corona discharge, flame detection, missile plume detection, UV astronomy, UV LIDAR, and biological and chemical detection. We discussed the design, fabrication, and characterization of a 4H-SiC APD. The devices are based on epitaxial technology to ease the fabrication constraints w.r.t. implantation, activation and etching. This allowed for device fabrication in our own cleanroom facilities. The bevel angles were etched by using the photoresist reflow technique to make lens shape structures, and transferring the side-angles into the SiC semiconductor. As for the temperature sensing, this is based on SiC CMOS technology. The devices are threshold voltage based temperature circuit sensors. The designs of the circuits relied on using LT-spice simulations based on immature PMOS and NMOS models. Here channel length modulation was not taken into account. Nonetheless, this provided a starting point. The layout design was done in L-edit and verified for the design rules using K-layout. The fabrication was done at the Fraunhofer IISB Erlangen, Germany. For some of the wafers, we did the metallization at our own facilities, EKL. Basic measurements up to 200 °C have been done for the temperature sensor which showed good behaviour. Future work should include testing of the devices at high temperatures, well above 200 °C.

SAMENVATTING

Het terugschalen van transistors, ook bekend als de wet van Moore, is de belangrijkste drijvende kracht geweest achter de micro-elektronica-industrie. Aan deze trend zal uiteindelijk een einde komen door fysische beperkingen, zodat een alternatief nodig is om de technologische vooruitgang verder te stuwen. Dit gaf een stimulans om ook in andere richtingen te evolueren, ook bekend als More than Moore (MtM). Hierbij gaat het om alle technologieën die functionaliteit toevoegen aan geïntegreerde schakelingen (IC), allemaal verpakt als één systeem. Dit kan gebeuren door digitale en niet-digitale elementen te combineren, b.v. analoog/RF, passieven, micro-elektromechanische apparaten (MEMS), enzovoort. De niet-digitale elementen zijn niet noodzakelijk schaalbaar volgens de wet van Moore. Daarom hebben we in dit proefschrift de mogelijkheden onderzocht om silicium en siliciumcarbide (SiC) te gebruiken om een aantal sensoren te fabriceren, die in staat zijn zwakke signalen te meten. Dit wordt gedaan door een multidisciplinair onderzoek dat zich uitstrekt van elektrische, tot mechanische en optische domeinen.

In hoofdstuk 2 werd een in bulk microbewerkte hooggevoelige versnellingsmeter ontworpen, gesimuleerd, gefabriceerd en gekarakteriseerd. Door gebruik te maken van het niet-lineaire gedrag van vier lange slanke balken om een proefmassa te ondersteunen, is een werkpunt verkregen waar een extreem lage veerstijfheid optreedt. Een geïntegreerde capacitieve IDT-transducer wordt gebruikt om de verplaatsing van de proefmassa af te lezen.De integratie van de capacitieve uitlezing werd mogelijk gemaakt door gebruik te maken van de sleufisolatietechniek om de elektroden van de condensator elektrisch te isoleren, welk helemaal in hetzelfde bulk silicium werden vervaardigd. De apparaten werden afgedekt met stukjes Pyrex-glas. Een PCB met uitlees-ASIC werd gebruikt om de versnellingsmeter uit te lezen. De PCB werd vervolgens aangesloten op een impedantie-uitleessysteem met hoge resolutie, waardoor een meetsysteem ontstond. Met de laagste resonantiefrequentie van $8,7\ Hz$, de capacitieve gevoeligheid en de experimenteel gekarakteriseerde ruisvloer van de uitleeschip is de theoretisch haalbare systeemresolutie gelijk aan $17,02\ ng/\sqrt{Hz}$. Dit werk toont aan dat de proof of concept veelbelovend is voor toekomstige iteraties.

In hoofdstuk 3 worden SiC ultraviolet (UV) fotodetectoren geïntroduceerd, samen met de belangrijkste fabricage-stappen voor SiC. 4H-SiC heeft een aanzienlijk voordeel ten opzichte van silicium bij bepaalde toepassingen zoals UV en barre omgevingen. De thermische groei van SiO_2 is een van de voordelen van SiC ten opzichte van andere halfgeleiders met brede bandgap (WBG). De oxidatie van SiC werd daarom onderzocht en gekarakteriseerd. De resultaten bleken goed te passen in het DG-model, maar er moet verder worden onderzocht hoe het gedrag in alle kristalrichtingen is. Verder werd ook het etsen van 4H-SiC onderzocht met behulp van de ICP- en RIE-processen. De daaropvolgende hoofdstukken beschrijven de apparaten die werden gefabriceerd met ge-

bruikmaking van de bevindingen in hoofdstuk 3 (behalve voor CMOS-apparaten). De resultaten van deze experimenten werden gebruikt om MSM Schottky sensoren te fabriceren voor multi-sensing toepassingen met behulp van verschillende metallizaties. De gebruikte metalen zijn Mo, Ta/Pt, Pd, en Ni, waarbij de laatste twee de beste donkerstroomprestaties vertoonden in het bereik van pA. De apparaten vertoonden redelijke donkere stromen bij 200 °C waarbij de nikkelelektroden een donkere stroom gaven van $\sim 223\ pA$ bij 20V bias. Hoewel Pt een grote metaalfunctie heeft, bereikte de donkere stroom $\sim 1,52\ mA$ bij 200 °C voor dezelfde spanning. De tantaal adhesielaag heeft een lagere metaalwerkfunctie met een waarde van $4,22\ eV$, vandaar een lagere Schottky barrièrehoogte, rond $0,6\ eV$. De reden om Ta als adhesielaag te gebruiken is dat de Pt loslaat bij het uitvoeren van de Scotch tape test. Aangenomen werd dat door metaalstapeling de totale Schottky-barrière voldoende hoog zou worden. De waargenomen metaalwerkfunctie is $\sim 0,8\ eV$ wat hoger is dan wat verwacht zou worden voor Ta/4H-SiC maar nog steeds onvoldoende is. Bovendien heeft ook de verwerking invloed op de SBH. De idealiteitsfactoren berekend met de standaard IV-methode vertoonden hoge waarden, wat betekent dat de apparaten moeten worden verbeterd. Dit kan bijvoorbeeld worden gedaan door de componenten bij hogere temperaturen te annealen om het metaal-halfgeleider interface te verbeteren. Een ander alternatief is de passivering van het oppervlak vóór de metallisering, die mogelijk ook kan leiden tot lagere lekstromen. Een voorbeeld van oppervlaktepassivering is het inbrengen van een diëlektricum zoals aluminiumoxide om oppervlaktedefecten te passiveren, maar ook om diffusie van metalen te voorkomen. Hoewel niet gekarakteriseerd voor zijn UV-gedrag, Mo-metaal vertoonde een Schottkybarrière van ongeveer $1,2\ eV$, hetgeen betekent dat het kan worden gebruikt voor optische detectie. Dit metaal is nuttig voor toepassingen bij hoge temperaturen en andere barre omgevingen omdat het een refractair metaal is. Hierdoor kan het apparaat worden gebruikt voor toepassingen bij hoge temperaturen waarbij het apparaat wordt gebruikt als een PTAT-temperatuursensor. De W5S5-apparaten met Mo-elektroden werden getest tot 200 °C en vertoonden een goed temperatuurgedrag. De bevindingen zijn bemoedigend om het apparaat verder te onderzoeken voor multi-sensing toepassingen gericht op barre omgevingen.

Naast dit apparaat werden specifieke apparaten voor UV-detectie en temperatuurdetectie (SiC CMOS) ontwikkeld. De eerste is een lawinefotodiode die gunstig is voor de detectie van zwakke ultraviolette signalen dankzij zijn kleine afmetingen, lage donkerstroom, hoge vermenigvuldigingsfactor en hoge kwantumefficiëntie. Dergelijke detectoren kunnen worden gebruikt in een breed scala van toepassingen, b.v. corona-ontlading, vlamdetectie, raketpluimdetectie, UV-astronomie, UV LIDAR, en biologische en chemische detectie. Wij behandelden het ontwerp, de fabricage en de karakterisering van een 4H-SiC APD. De apparaten zijn gebaseerd op epitaxiale technologie om de fabricagebeperkingen ten aanzien van implantatie, activering en etsen te verlichten. Hierdoor konden de apparaten in onze eigen cleanroomfaciliteiten worden vervaardigd. De schuine hoeken werden geëtst door gebruik te maken van de fotoresist-reflowtechniek om lensvormige structuren te maken, en de zijhoeken over te brengen in de SiC-halfgeleider. De temperatuursensoren zijn gebaseerd op SiC CMOS-technologie. De apparaten zijn drempelspanning-gebaseerde temperatuurschakelingsensoren. De ontwerpen van de schakelingen berustten op het gebruik van LT-spice simulaties op basis van onvolwas-

sen PMOS- en NMOS-modellen. Hierbij werd geen rekening gehouden met modulatie van de kanaallengte. Niettemin bood dit een uitgangspunt. Het layout-ontwerp werd gedaan in L-edit en geverifieerd op de ontwerpregels met behulp van K-layout. De fabricage vond plaats in het Fraunhofer IISB Erlangen, Duitsland. Voor sommige wafers hebben we de metallisatie gedaan in onze eigen faciliteiten, EKL. Voor de temperatuursensor zijn basismetingen tot 200 °C gedaan, die goed bleken te zijn. In de toekomst moeten de apparaten worden getest bij hoge temperaturen, ver boven 200 °C.

1

INTRODUCTION

1.1. BACKGROUND

In the last century, physicists such as Richard Feynman have realized the importance of downscaling electronics as was evident from his speech "There's plenty of room at the bottom" [1]. Not long after this, the co-founder of Intel, Gordon E. Moore, has defined Moore's law which states that the number of devices in an integrated circuit (IC) will increase exponentially over time [2]. It is somehow counter-intuitive that the functionality of CMOS devices stays about the same while downscaling and keeping the W/L ratio constant. However, this miniaturization trend is coming to an end due to physical limitations, hence an alternative is required to further drive technological progress. The alternative is to combine the miniaturization of functionality and diversification of functional elements in integrated circuit (IC) devices. This can be done by combining digital and non-digital elements, e.g. analog/RF, Passives, microelectromechanical devices (MEMS), and so on. The non-digital elements are not necessarily scalable according to Moore's law. This is known as More than Moore (MtM) (Figure 1.1) [2–4].

The development of sensors capable of measuring extremely small signals and/or operating in harsh environments enable applications over large spans such as seen in the emerging field of internet of things (IoT) [5]. Here diversification is not only in the form of sensor types but also materials of choice to develop such devices. However, silicon technology is reaching its physical limits and has serious drawbacks in harsh environments, i.e. fails at high temperatures, high pressures, radiation, shock/ high vibration, harsh chemicals, humidity, and biology [6]. Various solutions have been proposed to make silicon technology compatible with harsh environments, e.g. packaging, material selection, additives by fabrication such as adhesion layers, etc. [6]. Furthermore, the solutions proposed in research and industry all have different effectiveness in different harsh environments where material selection and packaging are the best approaches [6]. However, sensor packaging is the most costly step in the realization of the devices where harsh environment compatibility further complicates packaging [7]. Sensors can be integrated into systems for monitoring and performance enhancement but are beneficial

1

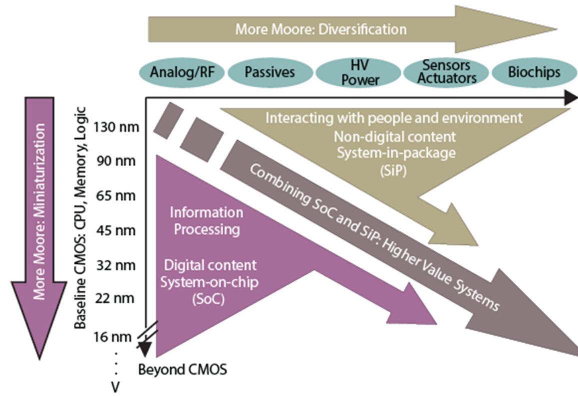

Figure 1.1: The International Technology Roadmap for Semiconductors: Miniaturization and diversification [4].

up to the point where the added value is exceeded by the cost [7]. One way to still use silicon technology for harsh environments lies in how it is utilised. For example, measuring volcanic activity (vibrations/shocks) may be difficult due to large shocks and high temperatures. But if the devices were to be very sensitive, these can be applied at a safe distance. Such device has been fabricated in this work (MEMS accelerometer). Alternative solutions are possible, e.g. harsh environment compatible materials [7]. One very attractive material is silicon carbide (SiC) thanks to its electrical and mechanical properties [8]. The semiconductor material lends itself not only for power electronics but also for sensor and integrated circuit technologies, albeit with some limitations. By combining electronics and sensors, the performance of a system can be greatly enhanced w.r.t. effects such as noise, parasitics, and other unwanted effects. Therefore, in this work we will focus on four aspects. The first is to investigate the detection of extremely small signals associated with gravimetry. The second is to detect low ultraviolet (UV) light. Here we also investigate avalanche photodiodes which potentially can be used for single photon detection. The third is related to measuring high temperatures.

1.2. Highly Sensitive Accelerometer

Silicon technology already proved to be the main propeller of today's electronics advancement. This also goes for MEMS devices which are applied in various fields, e.g. to measure acceleration, pressure, flow or actuation such as physical switching or even thrusters [9–11]. Therefore, the first aspect of this research is the development of an extremely sensitive accelerometer to sense small variations in local gravitational acceleration [12]. Its applications range from studying our planet's behaviour w.r.t. earth crust movement, volcanic eruptions, detection of earth tides, to water and oil pockets. Even though some applications may be harsh environments, i.e. high shocks/high temperatures, the devices can be applied at a safe distance thanks to their high sensitivity. Moreover, such sensing can be used to monitor vibrations in high end machinery where nanometre accuracy is required, e.g. lithography processing machines. Unlike the em-

ployment of large detection devices for gravimetry purposes, developing miniaturised silicon devices allows over large-area detection thanks to its low cost and high sensitivity when well designed. An application may be the internet of things (IoT) to collect data for studying earth activity. To this end, high sensitivity accelerometers can be designed by exploiting geometrical nonlinearity seen in long slender beams, also known as compliant mechanisms [9]. The required gravimeter sensitivities for detecting the smallest changes in gravitational acceleration are in the range of $1-100\ ng/\sqrt{Hz}$ [13].

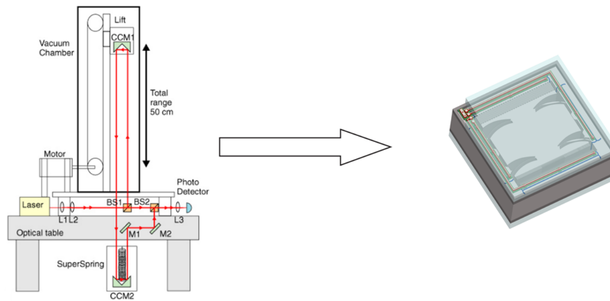

Figure 1.2: Going from large gravimeter devices to a small MEMS accelerometer (Source Large size gravimeter: [14]).

1.3. WIDE BANDGAP SEMICONDUCTOR TECHNOLOGY

A harsh environment is any environment having certain characteristics impeding the normal operation of a sensor or actuation device [6]. One of the most discussed types is the high temperature $> 200\ °C$ where extrinsic silicon reverts to being intrinsic due to the high electron-hole carriers generation. Moreover, the useful mechanical properties are lost at higher temperatures which limits the working range of MEMS devices. Next to high temperatures, optical harsh conditions such as short wavelengths and high radiation conditions can significantly reduce the lifetime of devices [15, 16].

Other harsh environment types are high pressures ($2000-3000\ bar$) as seen in automotive and process industries, high shock/ high acceleration, high radiation, harsh chemical environment, and high humidity [6]. These challenges can be addressed depending on the type of environment through design considerations w.r.t. materials, technology, device fabrication, packaging, and system type [6]. The material aspect of the design can reduce the design constraints and reduce cost if it meets the requirements of specific applications which may include high-temperature capability, high electric breakdown for high power actuation, fast switching, and radiation hardness.

1.3.1. TEMPERATURE SENSING

Temperature sensing using SiC technology can be applied up to $600\ °C$ in many industrial applications, e.g. geothermal power generation, gas turbines, aerospace systems, etc. [17]. Furthermore, real-time monitoring can be enabled by this method allowing

for in-situ changes in processes such as solar panel production. Such sensors can be based on simple diodes or CMOS technology and can be monolithically integrated with SiC electronics [18]. In this work diode based and CMOS based temperature sensors are investigated up to a working temperature of 200°C.

1.3.2. Ultraviolet Photodetection

There are various methods for detecting partial discharge, including pulse current method, optical detection in the infrared and ultraviolet spectral range, acoustic emission, temperature, and pressure changes in the area [19–22]. Gas sensing could also be used to measure chemical reactions occurring in oil-filled transformers [20, 23].

For example, ultraviolet (UV) detection in power grid applications is currently done using UV cameras such as the "UV-260 Corona Discharge Camera" and "DayCor Superb UV imager". Such cameras superimposes the detected UV light on a normal image to show the location [22]. The "DayCor Superb UV imager" has a UV sensitivity of $2.2 \times 10^{-18}\ W/cm^2$ and a minimum visible light detection of 0.1 Lux. The Minimum Discharge detection is 1 pC at a distance of 10 m. The spectral range is kept within $240-280\ nm$ as this corresponds to the solar-blind range allowing for daytime detection. The discharge severity can then be estimated based on the photon number [22]. However, even-though this camera has high specifications, this method is only used at close range while needing someone to operate it. This shows that developing sensors capable of employment over entire grids offer better monitoring of the power grid. Developing UV sensors is not limited to the application in power grids but can range from chemical, environmental, and biological analysis. Furthermore, it can be used for monitoring, e.g. flame and radiation detection, etc. [24]. In some cases such as flame detection, high-temperature thermally stable detectors with high performance are required [24].

Thanks to the wide bandgap of SiC, UV detectors made from it are visible blind ($\approx 400\ nm$), hence no filtering is required [16, 25–27]. Moreover, its high mechanical and chemical stability enable application in high radiation conditions. Such conditions may significantly reduce the lifetime of silicon devices [28–30]. The instability of photodetectors depends on the irradiation type, level of irradiation and its duration. The radiation effects result in changes in spectral responsivity, increase of leakage current, reduction of charge collection efficiency and removal of free carriers from the conductive regions of the device [31]. The swelling and mechanical properties of SiC are of interest in nuclear applications where devices and electronics undergo neutron irradiation [32]. On the other hand, SiC avalanche photodetectors can be sensitive to low UV light levels in the range of $fW - aW/cm^2$ while having a clear distinction from the noise level and maintaining a reliable signal. SiC also has the advantage of good responsivity, high thermal stability, radiation hardness suited for nuclear applications, high response speed, and high-power [24]. Therefore, this work will focus on designing and fabricating SiC UV UV photodetectors.

1.3.3. Silicon Carbide

To aid in the design of more robust sensors, wide bandgap technology offers an excellent alternative to silicon. One of the materials coming on top for this is SiC. Its wide bandgap

not only enables visible blind operation of photodetectors, but thanks to its mechanical and chemical stabilities, it also enables operation in harsh optical environments where short wavelengths affect the stability and lifetime of detectors. Furthermore, this property enables operation in high-temperature regimes where the intrinsic carrier concentration generation doesn't surpass the dopant concentration carriers [33]. However, such properties are also exhibited in other wide bandgap materials as well [33]. One major advantage of SiC over other wide bandgap materials is its oxidation being similar to that of silicon, namely silicon oxide (SiO_2). This allows for growing gate oxide under similar conditions as seen for silicon technology, enabling CMOS compatibility.

Unlike silicon which is diamond-like, 4H-SiC comes in Wurtzite (hexagonal) unit cells. The SiC crystal structure occurs in many phases, also known as polytypism. That is, depending on the stacking sequence along one direction, up to 250 polytypes can be obtained [34, 35]. Each polytype can be envisioned as a corner-sharing tetrahedral where each tetrahedron consists of a silicon atom at the centre and four carbon atoms bonded to the silicon atom [36, 37]. Figure 1.3 illustrates a tetrahedron building block. The three popular polytypes are the 3C-SiC, 4H-SiC, and 6H-SiC. In this work, the focus is on the monocrystalline 4H-SiC. Table 1.1 summarized some of the properties where SiC shows both advantages and disadvantages compared to silicon.

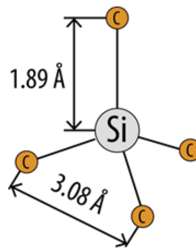

Figure 1.3: SiC tetrahedron building block.

Four key properties of SiC come into play in the case of applications where silicon is not adequate. These are its wide bandgap, high electrical breakdown, high thermal conductivity and high temperature operation capability [27, 38–41]. Its wide bandgap is one of its most important attributes since this is related to photodetection, high temperature operation, and high electrical breakdown ability. The latter two attributes are important in power electronic applications. The energy bandgap represents the minimum energy required by an electron to be excited from the valence band to the conduction band [42]. The excitation can for instance take place for thermal energy or photon energy. The first is what makes SiC high temperature compatible where the intrinsic carrier concentration at 300 K is at $8.2 \cdot 10^{-9}$ for 4H-SiC while this is $1.5 \cdot 10^{10}$ for silicon (see Table 1.1). Thus, in silicon this is limited to operations at temperatures of $\sim 125\,°C$ where extrinsic silicon reverts to intrinsic silicon at temperatures nearing 200 °C [6] compared to 700 °C for 4H-SiC. The energy bandgap is also important for short-wavelength photodetection applications. In the case of silicon with its bandgap of $\sim 1.12eV$, silicon devices require filtering for selective detection of ultraviolet radiation. Another advantage of SiC photodetectors is having a low dark current as this is directly proportional to the intrin-

Table 1.1: Comparison of silicon and SiC polytypes at room temperature [27, 38–41].

Property	**Si**	**3C-SiC**	**4H-SiC**	**6H-SiC**
Bandgap (eV)	1.12	2.3	3.26	3
Thermal conductivity ($W/cm \cdot K$)	1.5	4.5	4.5	4.5
Intrinsic carrier concentration (cm^{-3})	$1.5 \cdot 10^{10}$	6.9	$8.2 \cdot 10^{-9}$	$2.3 \cdot 10^{-6}$
Electron mobility ($cm^2/V \cdot s$)	1350	900	720^{*} 650^{**}	370^{*} 50^{**}
Hole mobility ($cm^2/V \cdot s$)	480	40	120	80
Breakdown field (MV/cm)	0.3	1.2	2	2.4
Dielectric constant	11.9	9.7	9.7	9.7
Saturated electron drift velocity (cm/s)	$1 \cdot 10^7$	$2 \cdot 10^7$	$2 \cdot 10^7$	$2 \cdot 10^7$
Intrinsic electrical resistivity ($\Omega \cdot cm$)	$10^3 - 10^5$	150	$> 10^{12}$	$10^4 - 10^8$

* Electron mobility of SiC along a-axis. ** Electron mobility of SiC along c-axis.

sic carrier concentration and since this is very low for SiC, extremely low dark current generation at room temperature can be obtained, thus allowing low levels of UV light detection. As for the high electric breakdown of SiC, this allows for high electrical fields without triggering an avalanche multiplication at low voltages. This ability is very important in power electronics as well as for avalanche photodetectors. This will be discussed further in Chapter 5.

1.4. Project Objectives and Thesis Outline

This research work will focus on designing and fabrication of various types of sensors as proof of concept. The work is multi-disciplinary where mechanical, electrical, and optical knowledge is used to fabricate devices which are harsh environment compatible, either thanks to their physical or structural properties. In Chapter 2 we focus on developing a highly sensitive accelerometer for applications requiring tilt and vibration sensing. Here, we design and fabricate a MEMS silicon device using high aspect ratio deep reactive ion etching to obtain a large mass supported by four long slender beams. The beams are non-linear allowing for high sensitivity. In Chapter 3 we will introduce ultraviolet detection, photodetectors, antireflective coating, 4H-SiC oxidation, and etching of 4H-SiC. In Chapter 4 we focus on the development of metal-semiconductor-metal (MSM) devices for UV and temperature sensing. In Chapter 5 we introduce a pin photodiode aimed at avalanche operation to detect small UV signals, up to single photons. In Chapter 6 we focus on a CMOS temperature sensor and briefly introduce a simple amplifier circuit in SiC as proof of concept. A conclusion and recommendations chapter is added to give future work outlook.

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2

A HIGH-RESOLUTION MEMS INERTIAL SENSOR

This chapter discusses the design of a highly sensitive accelerometer capable of $ng/\sqrt{Hz}$ *sensitivity. The device can be used for tilt and vibration sensing and is also known as a MEMS gravimeter. First, the requirements for the sensor are defined followed by detailing the design, realisation and testing.*

2.1. INTRODUCTION

The research community is becoming exceedingly more interested in the behaviour of our planet regarding its weather condition, but also other geoscience studies such as earth plate movements, volcanic activity, underground water- and oil pockets [1] or any extremely small variations in local gravitational acceleration. Moreover, such sensing can also be used to monitor vibrations in high-end machines where nanometre accuracy is required, e.g. lithography processing machines. To sense vibrations, MEMS technology can be applied, e.g. highly sensitive accelerometers. Although MEMS devices do not have the high sensitivity seen in the traditional devices such as mechanical gravimeters, the MEMS devices are much smaller while being low cost when produced in high quantities. Moreover, such devices can be combined with the emerging Internet of Things (IoT) [2] to sense over large areas. Since the cost is much lower, the MEMS devices can be placed in a much higher density which may allow for a higher mapping of measured areas. A MEMS-based gravimeter should have a sensitivity in the range of $1-100\ ng/\sqrt{Hz}$ to measure very small changes in gravitational acceleration at low frequencies [1].

Recently researchers have put focus on developing MEMS accelerometers for gravimetry applications. Middlemiss et. Al. designed a highly sensitive accelerometer exploiting nonlinear buckling behaviour observed in compliant mechanisms [3]. Thanks to this, a high mechanical sensitivity within the micromachined structure was obtained and reached a value of $40\ ng/\sqrt{Hz}$ at a resonance frequency of $2.3\ Hz$. However, this work didn't exploit the full potential of MEMS devices lacking the electrical component of MEMS technology. Instead, the read-out of motion was done using a shadow sensor which is comprised of a LED and a photodiode. Furthermore, the device is highly sensitive to temperature variations where $1\ mK$ can result in an error of $0.25\ \mu Gal$, or $0.25\ ng$. To account for this limitation, a servo-control was added for temperature control. An integrated electrical readout as seen in standard applications, i.e. capacitive transduction, would result to reduction in cost and facilitate miniaturization. This could be further enhanced by using onboard integrated ASIC to process the capacitive signal while significantly improving noise level performance [4].

Li, et. Al, have developed a linear spring-based accelerometer for gravimetry applications [5–7]. The device has a sensitivity of $30\ ng/\sqrt{Hz}$ at a resonance frequency of $13.2\ Hz$. The high sensitivity is obtained using a fine/coarse capacitive readout combined with linear springs. However, the realization of this device is complex as it requires wafer stacking and bonding to enable surface capacitive transduction. Furthermore, such configuration introduces fringe capacitances and large parasitic capacitances reducing noise level performance.

Unlike the work of Li, this work uses nonlinear near-zero stiffness springs for further improvement of resolution. By employing a capacitive readout ASIC with higher sensitivity, system resolutions beyond $ng/\sqrt{Hz}$ could be feasible. Furthermore, using nonlinear springs, the dynamic range is not determined solely by the low spring stiffness, i.e. a measurable signal is still feasible even when the device is not in its operating point. It should be noted that both the stiffness and resonance frequency will increase.

Therefore, this work will focus on designing and realization of a compact MEMS ac-

celerometer capable of $ng/\sqrt{Hz}$ detection based on capacitive readout with an open-loop configuration. The beams holding the mass in place are nonlinear, theoretically capable of reaching near-zero stiffness. such behaviour is seen in compliant mechanisms having large elastic deformations by design which allow actuation with precision without having to deal with friction, wear, or backlashes [8]. The difference in this design is the absence of negative stiffness which prevents the device to buckle in a second motion or negative state. By designing the geometry of the four beams properly, the softening of the beams can result in a local region where the spring stiffness is near-zero for a range of displacement values, while an increase in stiffness is observed for displacements out of this range [9]. This is illustrated in Figure 2.1 as a local 'constant region' or 'positive stiffness region' in the force-displacement graph.

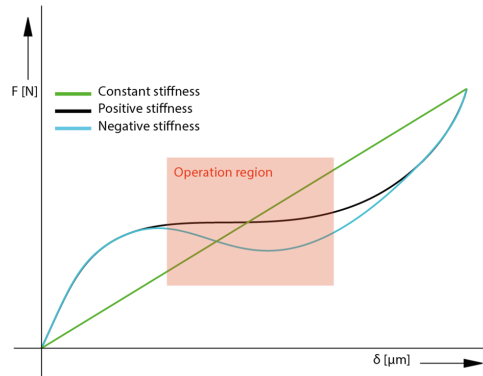


Figure 2.1: Behaviour of linear and nonlinear beams [4].

As mentioned earlier, it's necessary to design the beams such that negative stiffness is avoided. This not only limits the range of motion, hence, reducing the sensing range of the device, but also results in multiple operating points for the same applied force where a snap-through behaviour occurs as illustrated for the negative stiffness spring in Figure 2.1.

2.2. BACKGROUND

2.2.1. MECHANICAL SPRING SYSTEM

Before discussing the design, first relevant basic accelerometer theory will be introduced. This is true for linear behaviour but is used to convey the principle of the nonlinear device. The design will be aided using finite element modelling using COMSOL software. Consider Figure 2.2 where a mass-spring system is shown.

The operation principle of accelerometers is based on Newton's second law. A cantilever with a mass at its tip acts as an accelerometer where an external excitation force (F) such as a shock can be used to displace the mass. The cantilever acts as a spring with a stiff-

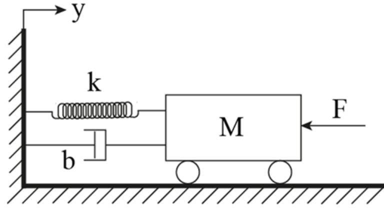


Figure 2.2: Mechanical representation of an open-loop accelerometer [10].

ness (k) while some damping (b) reduces the displacement. After the displacement, the mass will experience a restoring force due to the spring action of the cantilever.

To analyse such systems, one can use the electrical equivalent circuit of the system as illustrated in Figure 2.3. For completion, a noise source is added to account for the Brownian motion noise (white) noise.

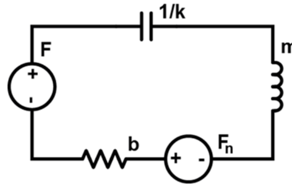


Figure 2.3: Electrical equivalent circuit of the accelerometer representation [11].

This results in the second-order equation (2.1).

$$F + F_n = m \cdot a = m \cdot \frac{d^2x}{dt^2} + b \cdot \frac{dx}{dt} + kx \tag{2.1}$$

Using Laplace transform for s-plane, this results in equation (2.2).

$$\frac{X(s)}{A(s)} = \frac{m}{ms^2 + bs + k} = \frac{1}{s^2 + \frac{b}{m}s + \frac{k}{m}} = \frac{1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.2}$$

The above leads to the formulation of the resonance frequency [10]

$$\omega_n = \sqrt{\frac{k}{m}} \qquad and \qquad \zeta = \frac{b}{2m\omega_n} \tag{2.3}$$

Where ω_n is the natural resonance frequency and ζ is the damping factor.

Here the damping coefficient (b) is determined by gas damping where this can be pressurized to a certain degree to obtain critical damping, provided packaging requirements

are met. The critical damping is important for achieving maximum bandwidth and minimum overshoot or ringing [10]. Moreover, the damping coefficient is temperature dependent which adds to the difficulty of obtaining linear behaviour due to compressibility of the gas in the case an open-loop configuration for the accelerometer is selected.

2

Both the bandwidth (BW) and sensitivity (S) can be determined using the resonance frequency. To measure it, the accelerometer can be dynamically resonating or statically measuring the displacement for a given acceleration. The displacement is related to natural resonance frequency by [10]

$$\omega_n^2 = \frac{k}{m} = \frac{a}{x} \qquad with \qquad x = \frac{F}{k} = \frac{m \cdot a}{k} = \frac{m \cdot g}{k} \tag{2.4}$$

Where g is the gravity constant. As for the sensitivity, this is determined by the inverse of the square of the natural resonance frequency and is obtained by taking equation (2.2) at $s = 0$ as shown by equation (2.5).

$$S = \left.\frac{X(s)}{A(s)}\right|_{S=0} = \frac{1}{\omega_n^2} = \frac{m}{k} \tag{2.5}$$

Equation (2.5) shows that the sensitivity can be high by reducing the bandwidth. This can be done by increasing the proof mass weight or by reducing the suspension beams stiffness.

The trade-off is made for an open-loop accelerometer are between the sensitivity, dynamic range, and bandwidth [10]. Therefore, the key design aspect of an open-loop accelerometer is its mechanical suspension design. Closed-loop control can be added to the design of an accelerometer where the output signal is used to generate a feedback force and apply this onto the proof mass. This counteracts the acceleration resulting in a stationary proof mass and negligible displacement [10]. This design has the advantage of being less sensitive to process variations and by adding temperature sensing one can further reduce the errors in the measurements.

2.2.2. MECHANICAL NOISE

The fundamental detection limit of an accelerometer is determined by the noise of the total system including, the mechanical Brownian motion (white) noise and the electrical noise [12]. Consider equation (2.6).

$$X(s) = \frac{F + F_n}{ms^2 + bs + k} \quad \Rightarrow \quad \frac{X(s)}{A(s)} = \frac{1}{s^2 + \frac{b}{m}s + \frac{k}{m}} = \frac{1}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{2.6}$$

The damping shown in the equivalent circuit in Figure 2.3 accounts for the noise, similar to a resistor in an electrical circuit. Following this analogy, the noise spectral density is given by $4k_B Tb$. Moreover, this can be related to the mechanical quality factor (Q) given by equation (2.7).

2

$$Q = \frac{m\omega_n}{b} \tag{2.7}$$

The noise can be interpreted as an error in the acceleration. Consider equation (2.8) at low frequency $\omega << \omega_n$.

$$a_{n,rms} = \sqrt{\frac{4k_B T b}{m^2}} = \sqrt{\frac{4k_B T b}{m \cdot \left(\frac{Q \cdot b}{\omega_n}\right)}} = \sqrt{\frac{4k_B T \omega_n}{m \cdot Q}} \qquad \left[ms^{-2}Hz^{-1/2}\right] \tag{2.8}$$

Using the above equations one can design an accelerometer that has minimum noise contribution for a given sensitivity. Furthermore, it can be seen that the resonance frequency is an important factor in reducing the noise. The minimum detectable acceleration is inversely proportional to the square-root of the accelerometer proof mass which is the fundamental limit for silicon accelerometers regardless of the sensing method [10]. The signal-to-noise ratio (SNR) is then given by equation (2.9).

$$S^2 = \frac{a^2}{a_n^2} = \frac{a_n^2 mQ}{4k_B T\omega_n} \tag{2.9}$$

From the above equation, it shows that the resonant frequency should be kept as minimum as possible while meeting the required bandwidth for the specific sensing application. This can be done by increasing the proof mass weight while reducing the spring constant or stiffness. The SNR equation also shows that the quality factor Q should be as large as possible for maximizing the SNR [10]. Next to mechanical noise there is also the electrical noise component. This is dependent on the capacitive interconnect and readout ASIC as will be explained in later text.

2.3. Nonlinear Beam Design

2.3.1. Design of a single nonlinear beam

As shown in Figure 2.4, the accelerometer in our design uses four slender beams to suspend the mass in the centre of the frame. Here the beams are initially curved while both ends have inclination angles of α and β. Finite Element Analysis (FEA) is employed for designing the device based on initial parameters such as the required mechanical sensitivity, the fabrication limitations, and any other general design rules for compliant mechanisms. The simulations were carried out using COMSOL for displacements in the y-direction, x-direction, and z-direction. The outcomes are the force-displacement curves, the mechanical stiffness and the resonance frequencies. The overall design of the mass-beam device was done modularly.

Consider Figure 2.4 showing the suspended mass and Table 2.1 listing the geometry design parameters used in the simulations. Here angles α and β are defined as per Table 2.1.

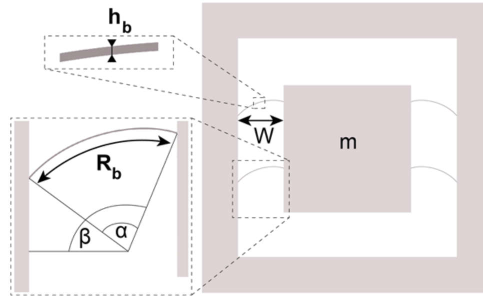


Figure 2.4: Illustration of the mechanical structure and the geometry design parameters.

Table 2.1: Mechanical geometry design parameters.

Parameter	**Symbol**	**Setting**
Device thickness	t	$300\ \mu m$
Mass weight	m	$35-69.9\ mg$
Beam height	h_b	$4-6\ \mu m$
Beam radius	R_b	$3000-4500\ \mu m$
Beam sector angle	α	51.4^o
Beam inclination angle	β	103.2^o
Inner frame dimensions	f_i	$10 \times 10\ mm^2$
Outer frame dimensions	f_0	$15 \times 15\ mm^2$
Spacing W between mass and inner frame	W	$3500-4500\ \mu m$

A simple yet effective relation between the mass and the spring stiffness is given by equations (2.10) and (2.11).

$$F = m \cdot a = m \cdot g \quad \Rightarrow \quad m = \frac{F}{9.81} \tag{2.10}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}} = 2\ Hz \quad \Rightarrow \quad \frac{k}{m} = 16\pi^2 \quad \Rightarrow \quad m = \frac{k}{16\pi^2} \tag{2.11}$$

The above relation is only useful at the operating point where a linearisation is done. This can be used as an indication for determining the stiffness at a given mass.

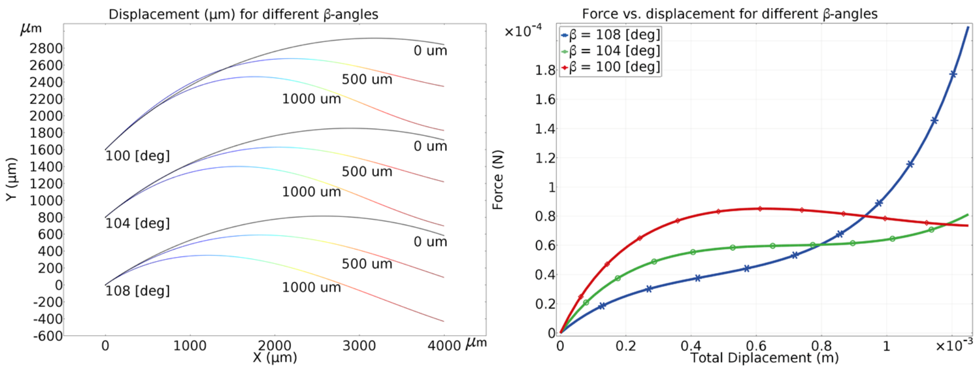
To obtain the nonlinear behaviour, the geometry design parameters are changed iteratively until the desired force-deflection behaviour is obtained. The aim is to design a device having a frame of $15 \times 15\ mm^2$ where the mass-beam structure is within $10 \times 10\ mm^2$. This means that the beams can be about $4-5\ mm$ long to fit within these constraints. Moreover, the mass should have a minimum width (x-direction) to reduce deflections in unwanted directions. To further restrict unwanted deflections, the beams should be as straight as possible while still maintaining a low stiffness at the operating region. This means that the beams should have a large radius and be as close to a straight beam as

possible when the sector and inclination angles are adjusted for the beam to fit the required spacing (W) between mass and inner of the frame. By combining the radius, the inclination angle and the sector angle, the desired force-displacement behaviour and lower spring stiffness of the beam can be obtained. Other parameters are the beam thickness and length, where the latter is set by its radius and spacing W between mass and inner of the frame.

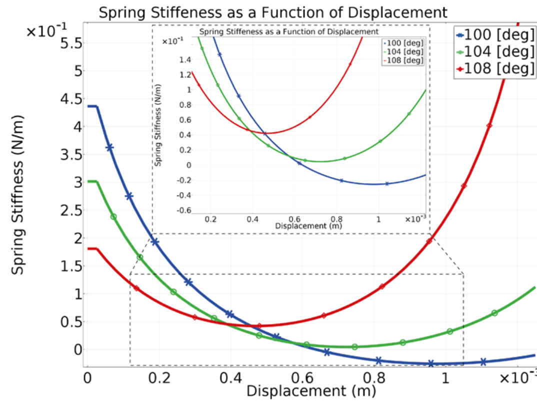
It should be noted that without design guidelines, the task becomes tedious due to a large number of degrees of freedom given by the geometrical parameters. Hence, the first objective is to formulate design guides to obtain the desired force-displacement behaviour.

SECTOR AND INCLINATION ANGLES

The first design parameters are the sector and inclination angles. Consider Figure 2.5.



(a) Beam bending. (b) Force-displacement relation.



(c) Spring Stiffness as a function of displacement.

Figure 2.5: Single beam at different inclination angles.

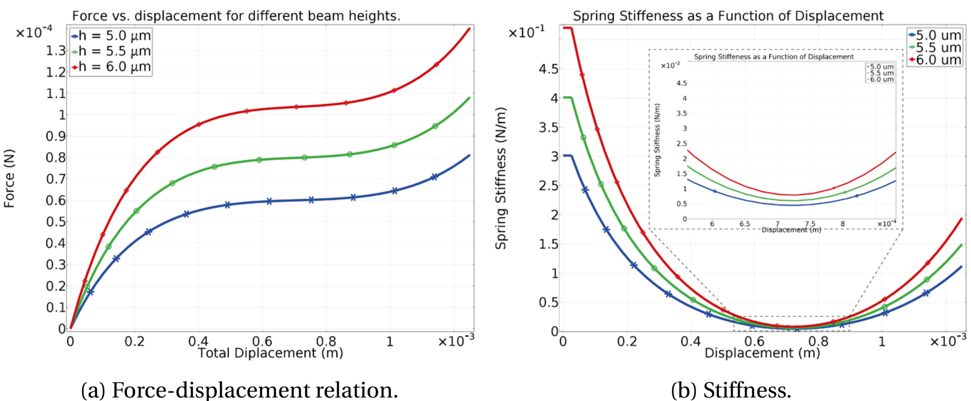
Figure 2.5a shows three beams with increasing sector and inclination angles as defined in Figure 2.4. Here, the bent shapes of the beams for different deflections are shown.

Notice that the larger the inclination angle at the fixed tip, the larger this also becomes at the moving tip. Here the sector angle of the beams is increased to fit the beam within the available spacing W at 4000 μm while maintaining the radius at a constant value of 4500 μm. Furthermore, an indicative effect is the “S-shape” of the bent beam. It indicates a spring softening effect in the beams which becomes more apparent at higher inclination angles. However, as the inclination angle further increases at both sides, the S-shape from the bending becomes less prominent resulting in the bottom spring. Figure 2.5b shows the force-displacement behaviour indicating that the higher the inclination angle, the flatter the near-constant force region becomes. The low inclination angle shows that multiple operating points exist for the same applied force. The inclination angle at 104° shows the best behaviour but can further be improved. To do this a close look at the spring stiffness is needed. Figure 2.5c shows the spring stiffness, obtained by taking the derivative of the force-displacement relation (see equation (**??**) in Appendix A). The inclination angle of 104° indeed shows the lowest stiffness without becoming negative.

Another option for fitting the beam within the spacing W can be by adjusting the radius instead of the sector angle. By doing so the inclination angle at the moving tip of the beam can be kept relatively constant while the inclination angle at the fixed side may be changed. However, this method may be more complex to achieve the desired results but is nonetheless a useful method.

BEAM HEIGHT AND LENGTH

Once the desired force-displacement behaviour is achieved, the height of the beam and its length can be changed. These parameters are useful for determining both the size of the beams and the mechanical robustness during fabrication and application of the device. Moreover, the beam geometry also determines the mass size and with that, the size of the device. Consider Figure 2.6 showing the simulations for different beam heights.



(a) Force-displacement relation.

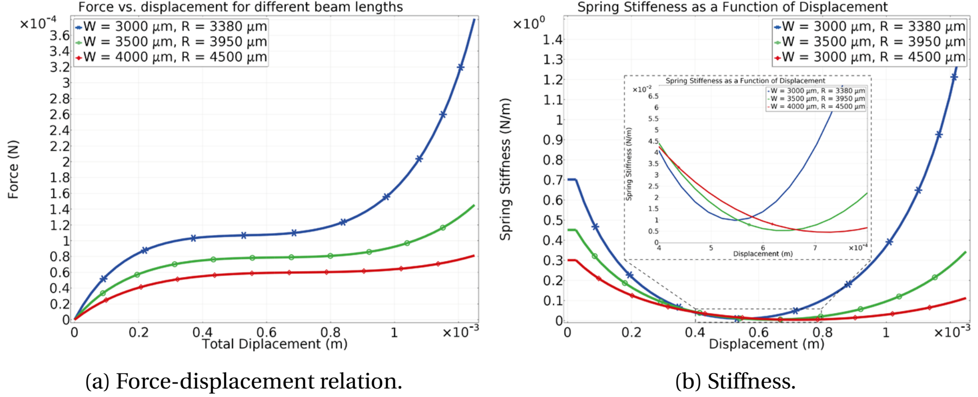
(b) Stiffness.

Figure 2.6: Single beam at different beam heights.

Figures 2.6a-2.6b show that required force scales down with decreasing beam height (thickness). This enables smaller mass size, hence smaller devices. However, the thinner

the beams become, the more challenging the fabrication becomes. The devices will also be very fragile.

The length of the beam has a similar effect on the force-displacement behaviour and is set by the spacing W and the radius of the curved beam. Consider Figures 2.7. Here the beam length is varied using the curve radius while maintaining the sector and the inclination angles at constant values of 54.31^o and 104°, respectively. The spacing W is varied in steps of 500 μm from 3000 – 4000 μm. As for the beam height, this is 5 μm.



(a) Force-displacement relation.

(b) Stiffness.

Figure 2.7: Single beam at different beam lengths (spacing W).

Figure 2.7a shows that not only the force decreases but also an increase in the displacement range is shown. This means that the beam length can be used to increase the dynamic range of the device and measure a larger range of acceleration. Figure 2.7b shows the stiffness as a function of the displacement. Similar to Figure 2.7a, a shift in the operating region is observed. However, the stiffness does not become negative which means that larger devices will have better performance.

2.4. DESIGN AND SIMULATIONS OF THE ACCELEROMETER

At this point, the design of the total accelerometer can be done. Recalling two basic requirements: the resonance frequency is targeted to be $\sim 2\ Hz$ while the mass-beam structure should fit within the given geometric constraints of $10 \times 10\ mm^2$. Recalling the relations given by equations (2.10) and (2.11), repeated here for ease. The equations give the minimum mass required for the mass deflection to reach the operating region of 1 g. Furthermore, the resonance frequency is also related to the minimum mass size. Both equations are useful at a linearised operating point.

$$F = m \cdot a = m \cdot g \quad \Rightarrow \quad m = \frac{F}{9.81} \tag{2.12}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k(x)}{m}} = 2\ Hz \quad \Rightarrow \quad \frac{k(x)}{m} = 16\pi^2 \quad \Rightarrow \quad m = \frac{k(x)}{16\pi^2} \tag{2.13}$$

This means that by designing each beam, as described in the previous section, to have a certain stiffness, equations (2.12) and (2.13) can be used to define the mass required at the operating region. Since the geometrical size of $10 \times 10\ mm^2$ is known, a relation between the spring stiffness and the force generated by the gravitational acceleration can be plotted. The maximum mass which can be obtained within the geometrical constraints (simplified), is given by

$$m_{max} = \rho_{Si} \cdot v_m = 2330\ [kg/m^3] \cdot [(10 \cdot 10^{-3}) \cdot (10 \cdot 10^{-3}) \cdot (300 \cdot 10^{-6})] = 69.9\ mg \quad (2.14)$$

Where ρ_{Si} is the density of silicon and v_m is the volume of the mass having the units of kg/m^3 and m^3, respectively. Through this method, the spring stiffness at the operating point can be designed while matching is done for the mass to reach the required force at the operating point. Consider Figures 2.8 showing the force-displacement relation and the spring stiffness of a single beam.

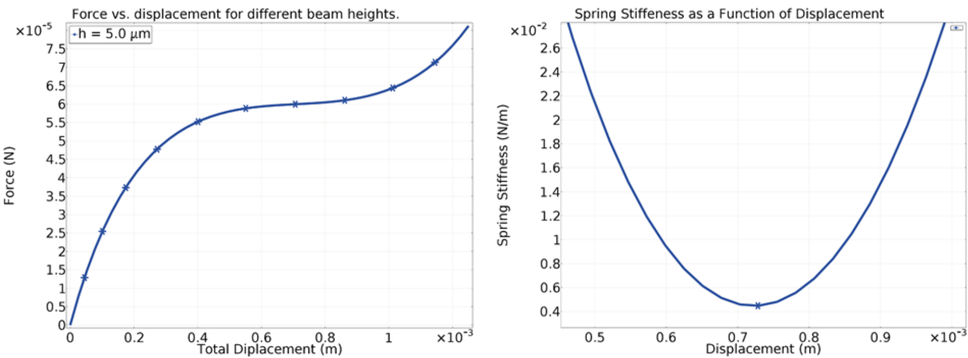


Figure 2.8: (a) Force and (b) stiffness behaviour as function of displacement of a single beam.

Knowing that spring stiffness can be summed, four beams at 2 Hz should have a mass of 115 mg which is far above the maximal attainable mass given the geometric constraints. Here the force should also be $1.13 \cdot 10^{-3}\ N$ to set the operating point at 1 g whereas Figure 2.8(a), it shows a force of approximately $6 \cdot 10^{-5}\ N$. Summing this for four beams it gives $2.4 \cdot 10^{-4}\ N$ which corresponds to an acceleration of 2.09 ms^{-2}. This acceleration is far below 1 g and concludes that the beams have a stiffness that is too high. Using the design guides, the beam is redesigned to fit the requirements needed for 1 g operating point and a resonance frequency of 2 Hz. Table 2.2 sums the design parameters of the mass-beam structure.

Figures 2.9(a) 2.9(b) show the force- and spring stiffness as a function of displacement for the four-beam-mass structure.
The operating point of 1 g is at a displacement of 584 μm in the above figure. The resonance frequency is determined at the operating point where the first mode is at 2 Hz. The second mode lies at 8487 Hz, thus sufficiently far from the first frequency mode.

Table 2.2: MFour-beam-mass structure design parameters.

Parameter	**Symbol**	**Setting**
Device thickness	t	300 μm
Mass weight	m	45.95 mg
Beam height	h_b	5.55 μm
Beam radius	R_b	4000 μm
Beam sector angle	α	56.3^o
Beam inclination angle	β	104.8^o
Inner frame dimensions	f_i	$10 \times 10\ mm^2$
Outer frame dimensions	f_0	$15 \times 15\ mm^2$
Spacing W between mass and inner frame	W	3570 μm

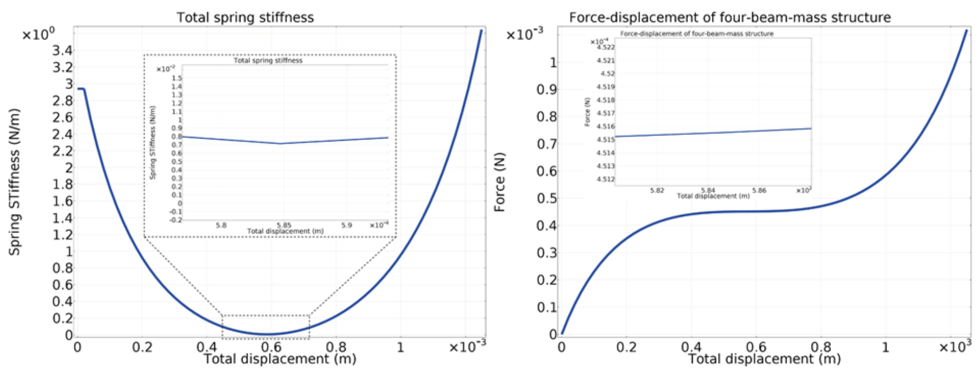


Figure 2.9: a) Force and b) spring stiffness vs. displacement of the four-beam-mass structure.

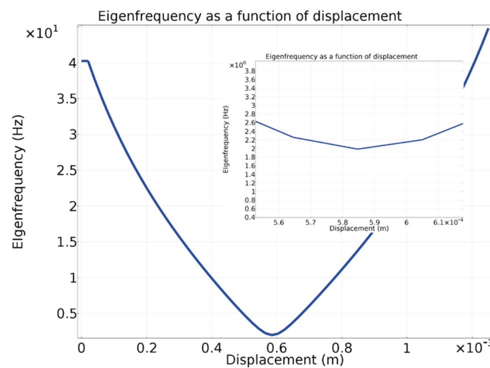


Figure 2.10: Eigenfrequency of the mass-beam structure as a function of displacement.

Recalling from equation (2.13), the spring stiffness is displacement dependent. Here the resonance frequency is the square root of the spring stiffness and mass ratio. Figure 2.10 is obtained from the spring stiffness relation.

The simulations were also done to obtain the spring stiffness in both the x- and z-directions in the same manner as for the y-direction. Here the direction of the prescribed displacement was changed to the unwanted directions. The proof mass was first set to the deflection corresponding to the operating point of 1 g in the y-direction by a prescribed displacement imposed on the mass. The resulting reaction forces and spring stiffness in these directions were then determined from the operating point with a deflection of $\sim 800\ \mu m$ The lowest stiffness at the 1 g operating point in the z-direction is $2 \cdot 10^4$ times higher than in the y-direction. The estimated error caused by the out of plane displacement, a displacement of 50 μm in the y-direction would result in a displacement of 3 nm at a tilting angle of 34°. The resulting capacitive error is then $1 \cdot 10^{-3}$ %. As for the stiffness in the x-direction, this is initially similar to that in the y-direction and increases beyond a value of $1.2 \cdot 10^5\ N/m$ after 20 μm of displacement, owing to spring stiffening. A tilt with respect to the vertical axis can be applied to the device, resulting in a decreased y-component acting on the proof mass. By doing so, the operating point and stiffness are changed accordingly. Thanks to the high stiffness in the z-direction, the response of the sensor is not compromised by the out-of-plane force. The amount of deflection and thus the spring constant can be varied in this way, providing a trade-off between bandwidth and sensitivity.

2.5. TRANSDUCER DESIGN

Sensors in general can be classified according to transduction type for measuring the signal of interest. In this case, multiple read-out methods can be applied to convert the mechanical signal (displacement of the proof mass) to the electrical domain where data processing and communication takes place. The methods may include: piezoelectric, piezoresistive, optical, thermal, magnetic, and electrostatic. Each transaction type has its advantages and disadvantages. The transduction should be selected not only based on signal readout type, but also the best fitting method for fabrication. In this work, we selected the capacitive method based on its advantages for fabrication and readout. It is fairly easy to integrate into the device, can be directly used to translate the mechanical signal into an electrical one, and has low-temperature dependency.

The capacitive transducer used is a lateral comb drive structure where th electrode fingers slide into place after the release of the mass-beam structure. This helps in maximizing the number of electrode fingers which would otherwise be limited by the fabrication. Moreover, the structure helps in reducing the damping caused by air surrounding the fingers. This can be explained by the Couette flow, occurring for lateral motion, being much less dissipative compared with the squeeze film damping. Thanks to this and the main objective of measuring mechanical signals in the sub 20 Hz range, the fluid inside the gaps has enough time to displace. This also prevents the air to act like a spring, which stores and releases energy at higher frequencies [13]. The damping can be further reduced by using vacuum packaging.

The sensitivity of the capacitive transducer was maximised thanks to the number of IDT electrode fingers. For this analysis, a simplification of the capacitive change is used

where a linear addition of parallel plate equivalents is used. This is given by equation (2.15).

$$\Delta C_{tot} = \frac{2N\epsilon_0\epsilon_r t(y_0 - y)}{d} \tag{2.15}$$

Where N is the number of fingers, ϵ_0 is the permittivity of vacuum, ϵ_r is the relative permittivity, t is the thickness of the substrate, $(y_0 - y)$ is the displacement in the y-direction, and d is the gap between the IDT fingers. From this equation, it can be concluded that the change in capacitance is maximised by maximising the number of fingers within the geometrical constraints ($10x10\ mm^2$) and by reducing the gap d between the IDT fingers.

Capacitive simulations have been performed to investigate the electric field distribution and verify that the absolute value of the electric field does not exceed the dielectric strength of air. To simulate the capacitive response, an interdigitated (IDT) electrode was placed across a second moving electrode. The capacitance/displacement behaviour is included in Figure 2.11. As can be concluded from this result, the capacitance varied from 35.58 pF to 33.47 pF. The values on the y-axis however show larger values for the capacitance, because the trench for electric isolation is also included in this value. From this result, it can be concluded that the capacitive response as a function of deflection is highly linear with a large capacitive change per nm distance. Taking the first-order derivative of the capacitance versus displacement characteristic in the linear region yields a sensitivity of 2.55 aF/nm in the displacement region of interest.

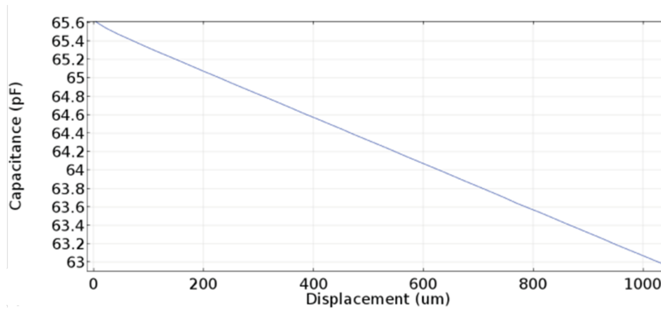


Figure 2.11: Capacitance vs. displacement behaviour.

The high degree of linearity in the capacitive response is thanks to the large number of fingers. The non-linear effect of the fringing electric field on either side of the electrode array is suppressed by the large contribution to the total capacitance of the normal components of the field between the parallel electrode fingers. Figure 2.12 shows the electric field distribution, where the fringing electric field (boundary) effects are visible. Furthermore, it can be noted that the aspect ratio of the structure is high: The width of each finger equals only 70 μm, whereas the thickness of the structure equals a wafer thickness of 300 μm. The large width of each finger suppresses the non-linear effect caused by fringing fields at the beginning and end of the IDE finger array, while the large height of each IDE finger suppresses the fringing fields on front- and backside of the wafer.

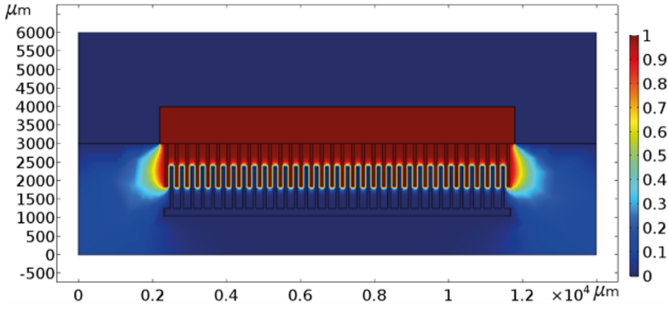
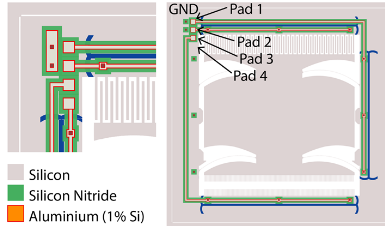


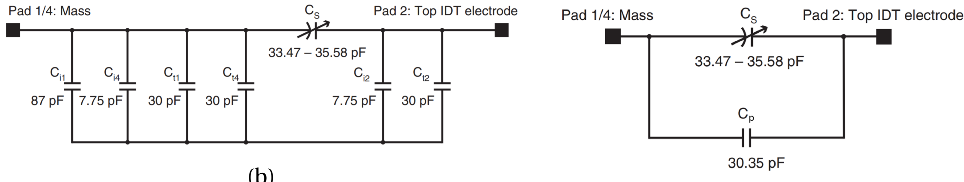
Figure 2.12: Potential distribution of the IDT

2.5.1. PARASITIC CAPACITANCES

The IDT structure is fabricated from the same substrate as the mass/beam system. Therefore, electrical isolation was realized using trenches filled with a dielectric [14]. As a result of the isolation, parasitic capacitances between the mainframe and the IDT electrode regions inevitably arise. Another parasitic capacitance contribution is caused by the metal traces connecting the different potential regions with the probe pads. Both sources of parasitic capacitances are illustrated in Figure 2.13a and included in the equivalent circuit shown in Figure 2.13b. The equivalent circuit model is based on the actual way of interfacing the sensor where the dielectric material is silicon nitride (Si_3N_4) for both the trenches and interconnect parasitics.



(a)



(b)

(c)

Figure 2.13: a) The device including trenches and interconnect, b) Isolation trenches (denoted with subscript t) and interconnect (denoted with subscript i) parasitic capacitances associated with each connection pad, and c) Parasitic capacitance across the sense capacitor in case of floating GND.

The equivalent circuit model illustrates the capacitances as these will appear across the

connection pads. The subscript including an 'i' denotes a parasitic caused by the metal trace whereas a subscript including 't' denotes a parasitic caused by an isolation trench. The parasitics on either side of the sensor capacitance C_s can be simplified to one parallel capacitor by omitting the ground connection, reducing the total parasitic capacitance. This is illustrated in Figure 2.13c. In this case, the parasitic capacitance will be in parallel to the sense capacitance which is an undesired effect. This is because there will be charge redistribution from the measurement signal over the parallel capacitor, hence resulting in worse system performance compared to the parasitic capacitance being connected to the ground, as shown in Figure 2.13b. The best method of connecting the sensor is summarized by Figure 2.14, thus including the connected ground.

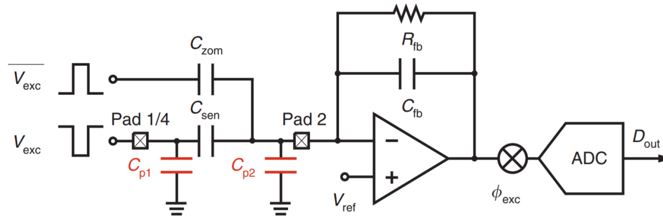


Figure 2.14: Device and its readout.

To operate the capacitive sensor, a square-wave signal V_{exc} is applied, at a frequency higher than the corner frequency defined by R_{fb} and C_{fb}. Simultaneously, the zoom-in capacitor, C_{zom}, is excited by a signal, the inverse of V_{exc}, to cancel the baseline capacitance, thus maximizing the use of the capacitance to voltage converter's (CVC) available dynamic range. The sensing signal-induced capacitance changes to modulate the excitation current. The resulting amplitude modulated AM signal is then amplified and demodulated back to in-band. As the modulated sensing signal is processed by the amplifier in high frequency where the $1/f$ noise is not dominating, the noise performance of the CVC gets improved. Finally, the voltage signal is digitized by an analog-to-digital converter (ADC).

2.6. FABRICATION

2.6.1. FABRICATION CONSIDERATIONS AND GEOMETRY

Since the electrodes are made from bulk silicon, both electrodes of this transducer consist of low-ohmic silicon, which requires electrically isolated regions to facilitate the readout process. This is done by etching trenches nearly 100 μm deep and filling these with LPCVD silicon nitride for isolation and mechanical connection purposes. This is illustrated in Figure 2.15.

It should be noted that the trench width is ~ 3 μm which is set by the etch feasibility for an etch depth of ~ 100 μm. Selecting narrow trench width promotes the mechanical adhesion. Figure 2.16a shows a SEM image of the etched trench with a depth of 97.3 μm and a width of 3 μm. Figures 2.16b-2.16d show the images of the trench before and after being filled with Si_3N_4 as an isolator.

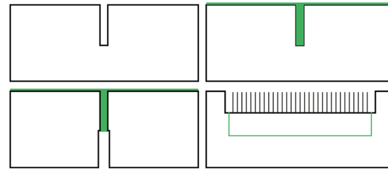


Figure 2.15: Cross-section of the electrical trench isolation. (Top-left) Top trench etch, (top-right) Filling with isolation material, (bottom-left) Bottom etch to remove the remaining silicon, and (bottom-right) resulting top view of silicon IDT island.

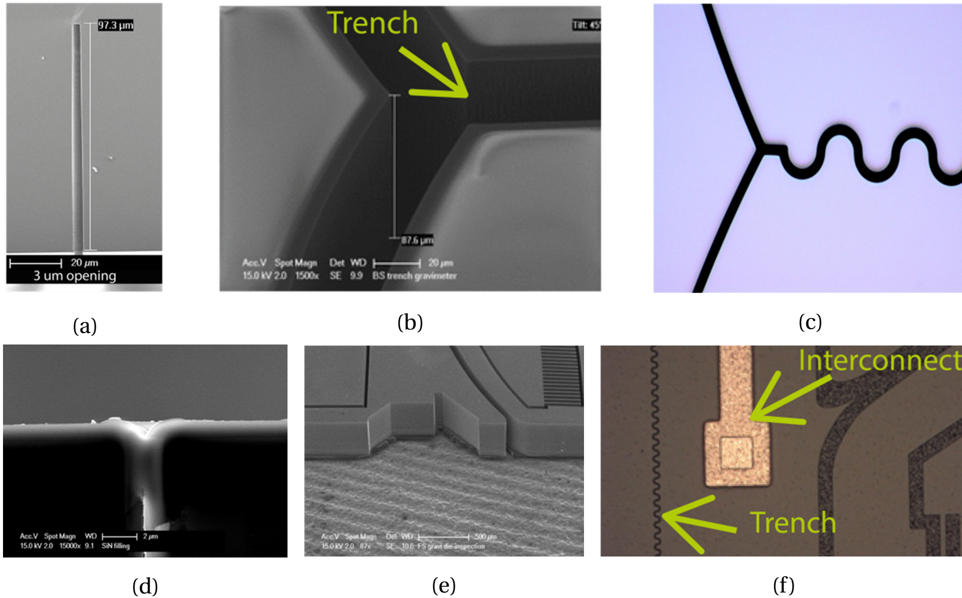


Figure 2.16: a) Etched trench 97.3 μm deep and 3 μm wide, b) Top view (SEM) of etched trench, c) Top view (microscope) of etched trench, d) Etched trench filled with Si_3N_4 as the isolator, e) DRIE etched structures before release and f) A microscope image in which the metal trace and the isolation trench can be seen.

The spring stiffness in unwanted directions (x- and z-direction) is at least two orders of magnitude larger with respect to the y-direction. Additional structures are included to limit large translation and rotations and to prevent electrodes from touching. Stopping structures are included in the design to prevent the electrodes from short-circuiting in the lateral direction as a result of large forces. The target chip area of $10x10mm^2$ needs to be taken into account when designing the capacitive transducer for maximum sensitivity, which restricts for example the maximum number of fingers in the IDT array. The IDT has been designed with finger widths and air gaps of 70 μm and a capacitive sensitivity of $2.52 \cdot 10^{-9}$ F/m, which corresponds to 2.52 aF/nm. The overlap between the fingers starts at 1040 μm and decreases for increasing deflection. Figure 2.17 summarize the geometrical design.

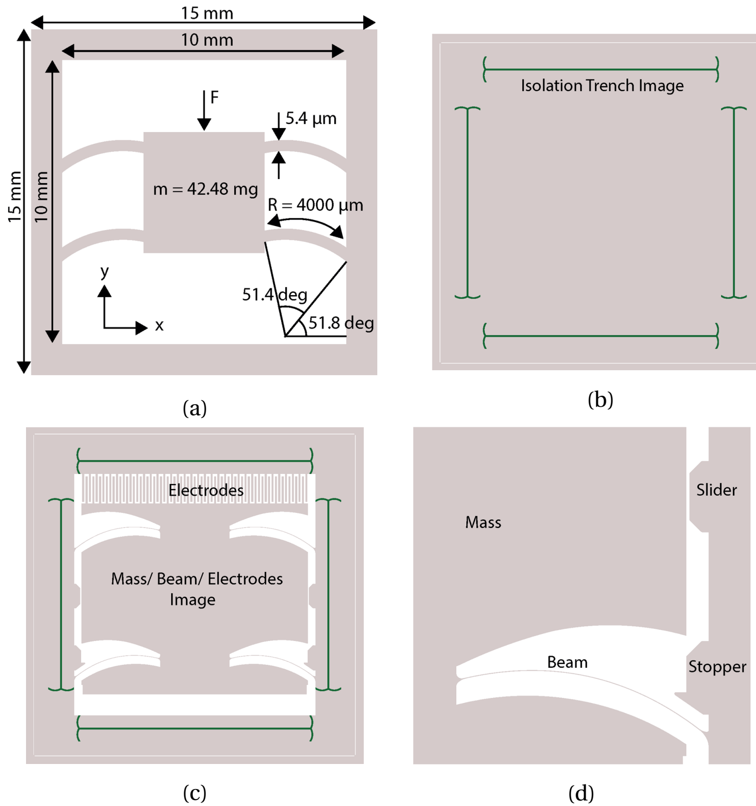


Figure 2.17: a) Geometry of the mass/spring system, b) Trench isolation image, c) Mechanical device with IDT electrodes, and d) Designed slider and stopper structures.

2.6.2. PROCESSING

The fabrication was performed in a CMOS compatible cleanroom and using MEMS microfabrication starting with 4-inch p-type silicon wafers (300 μm thick) with a resistivity of 10 Ωcm. First, electrical isolation steps for separating the electrodes from the bulk were done. The steps consisted of (1) etching silicon from the front-side through trench formation, (2) filling the trenches using low pressure chemical vapour deposition (LPCVD) silicon nitride (Si_3N_4) for electrical isolation and mechanical adhesion, and (3) etching the remaining silicon from the backside to complete the electrical isolation. The latter was achieved after the definition of the mass/beam structures in the silicon. After every pattern etching step, a cleaning procedure was performed to remove any organic material such as the photoresist or polymer used for wall passivation in the deep reactive ion etch (DRIE) etching process.

Figures 2.18a-b show the first electrical isolation step where a silicon oxide (SiO_2) masking layer was deposited on the front-side of the substrate, patterned using standard lithography, and etched using reactive ion etching (RIE). After this, a DRIE step was per-

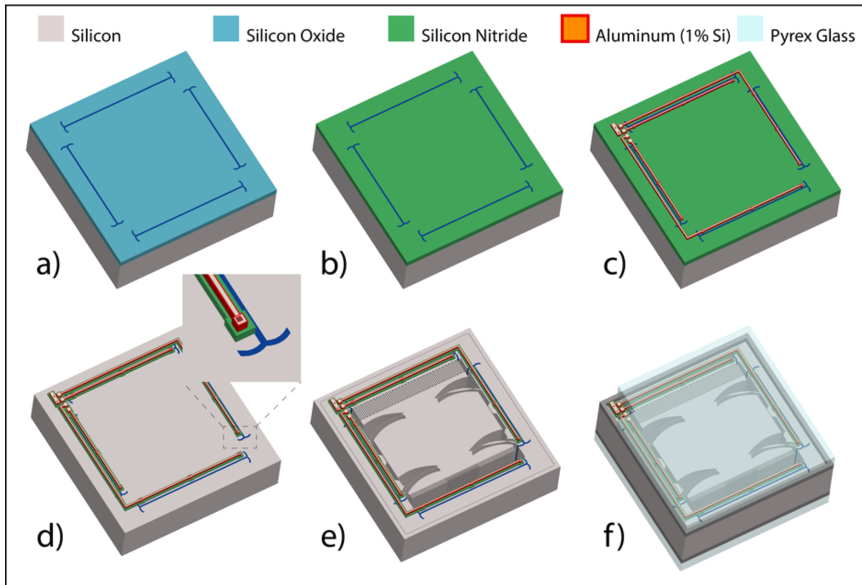


Figure 2.18: Process flow of the mass/beam system: a) Hard mask deposition and trench isolation patterning/etching, b) Trench filling with Si_3N_4, c) Metal interconnects on the front (and back-side hard mask with mass/beam patterns which is not shown here), d) removal of excess Si_3N_4, e) Released device, f) Final packaged device.

formed to etch 100 μm deep trenches. Subsequently, the substrate was cleaned after which the SiO_2 masking layer was then removed using 1:7 Hydrofluoric acid (HF) wet etching. The etched trenches were then filled with the isolation material in three steps. Each of these steps consisted of a deposition followed by a planarization without masking until the substrate was exposed. This method helps in minimising the risk of voids forming and in achieving a more uniform surface, which is an advantage during the later contact metallisation step. Before the last deposition step a boron implantation step was performed for ohmic contact formation with a dose of 10^{15} cm^{-3} at an energy of 20 keV. Because the Si_3N_4 layer is also used as an isolation layer between metal interconnect and substrate, after the third deposition, no subsequent planarization etching was performed, as illustrated by Figure 2.18c. The annealing step of the implantation was then carried out simultaneously with the last LPCVD deposition step at 800 °C. To connect the device to the outer world, contact openings were etched into the Si_3N_4 layer. Subsequently, a 1 μm aluminium layer (Al) with 1 % Si was deposited for metal interconnects and was patterned using standard lithography and inductively coupled plasma (ICP) etching for metals (Figure 2.18c). After this, the excess Si_3N_4 was removed (Figure 2.18d).

To complete the electrical isolation and define the mass/beam structures, two DRIE etching steps were performed. The steps consisted of the deposition of SiO_2 masking layers at the front-side and back-side, respectively. Starting with the back-side, the masking layer was patterned with isolation trenches to complete the electrical isolation. This

was achieved using standard lithography followed by RIE and DRIE etching steps. Similarly, the front-side was patterned with the mass/beam structures. The DRIE etching step was performed until a through-wafer etch was achieved. The last steps were the removal of any unwanted materials such as the passivation layer by an oxygen plasma, the Al capping layer by ICP etching, and the SiO_2 hard masks by vapour HF etching. After the vapour etching, the devices were released manually through vibrations during which the released halo-structures detached from the substrate (figure 2.18e). Figure 2.19a shows a picture of the device as it was realised using this procedure.

2.6.3. PACKAGING AND ASIC INTEGRATION

The last step in the realization of the devices is the packaging, wirebonding, and mounting on the measurement PCB together with the ASIC readout chip. The packaging shields the mass/ beam system from air flow, which may damage the device. Because the device is based on using large displacement behaviour, it is desired to use a packaging solution that allows visual inspection. Therefore, the device is packaged between Pyrex glass dies (2.18f). Furthermore, since the sensor is bulk micro-machined, the moving parts have the same thickness as the rest of the die, in this case, the frame. To allow the mass to move freely within the glass-silicon-glass stack, silicon spacers are used to have a controlled and known separation between the mass/beam system and the outer glass dies. The stack of glass outer dies, spacers, and MEMS-chip is glued together by ultraviolet (UV) curable Norland Optical Adhesive.
The readout ASIC has a measurement range of 80 fF. Although the readout ASIC has a 10 pF on-chip capacitance and a digital-to-analog converter (DAC) to compensate the baseline and the parasitic capacitance of the sensor, such as the ones originating from the isolation trenches and interconnecting metal traces. To minimise the parasitic capacitance or inductance in the packaging scheme further, the sensor has been directly wire-bonded onto a PCB housing the ASIC and I/O to the DAQ system. These wirebonds will introduce (minimal) parasitic capacitance and inductance, but since the variation in C around an equilibrium position is of main interest, these parasitics will not affect the measurement. The PCB has numerous options for capacitive readout, such as capacitance offset compensation and connections for bridge readout. The PCB is shown in Figure 2.19b before soldering the ASIC and wirebonding the accelerometer to it. Figure 2.19c shows the wire-bonded accelerometer. A picture of the 'daughter PCB' with the readout ASIC and die embedded in the main PCB is included in Figure 2.19d. The ASIC chip is shown in Figure 2.19e.

2.7. RESULTS AND DISCUSSION

The devices were tested at room temperature by measuring the capacitive response at different tilt angles. This was done by clamping the PCB onto a manual tilting stage and increasing the tilt from a horizontal starting position. Accordingly, Earth's gravitational acceleration of 1 g is scaled with the sine of the tilt angle. As a result, bringing the proof mass to the 'biasing point' where low spring stiffness occurs can be performed in a highly controllable manner. As a test signal, the mechanical shaker from Brüel & Kjaer (model

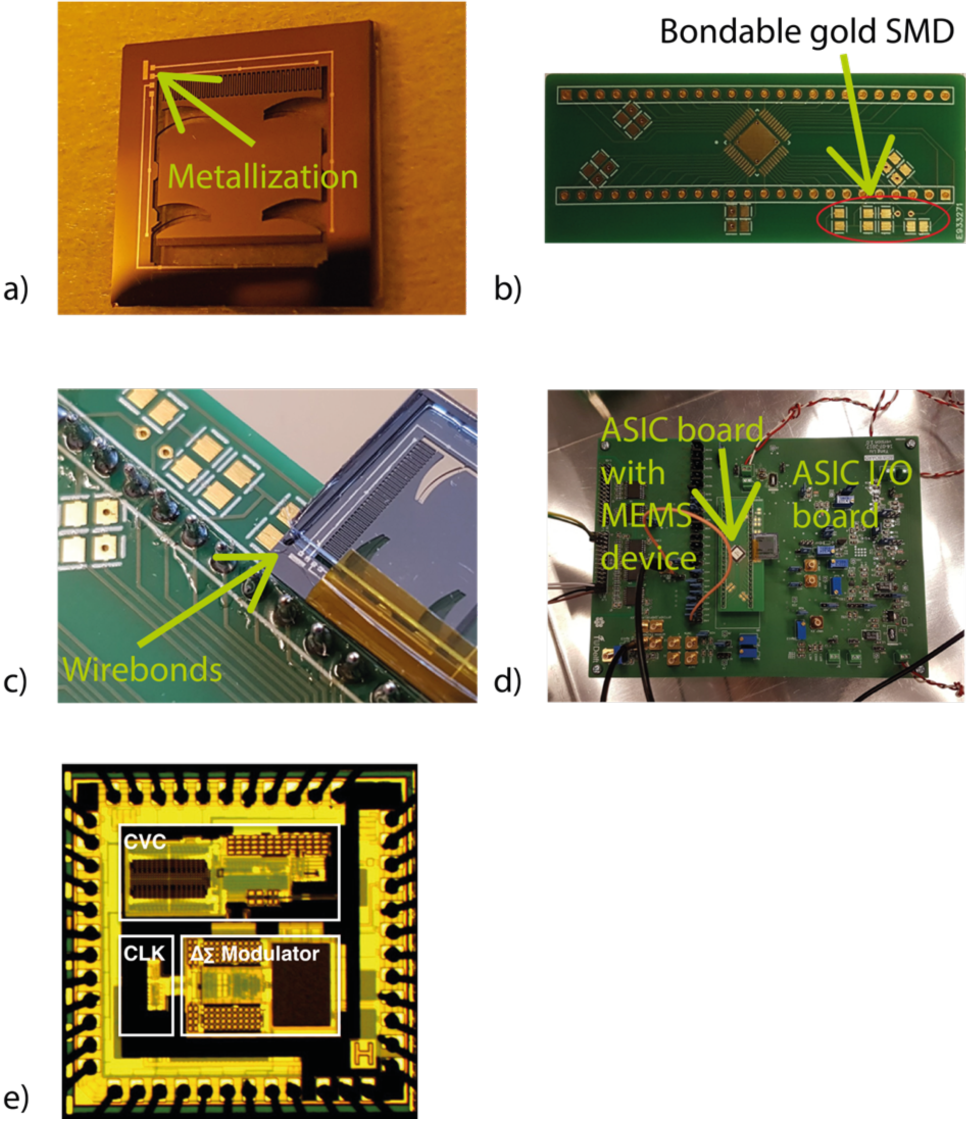


Figure 2.19: a) Final device after release, b) Interconnect PCB on which the ASIC is situated; the bondable gold SMD pads (circle) are used to wirebond the mass/beam system die on, c) UV glued and wire-bonded accelerometer on top of the daughter PCB and, d) Daughter PCB in the measurement setup, along with the metal box to shield the setup from external EMI interference, e) ASIC chip.

4810) was used, exciting a sinusoidal signal in the frequency range of the first resonance frequency of the devices. This range was determined by observing the displacement amplitude of the proof mass while manually varying the excitation frequency. When the

excitation signal passes the resonance frequency, resonance in the mass beam system is triggered and the movement of the proof mass shows a periodic behaviour.
The readout chip makes use of a Sigma-Delta-based ADC with a sample rate of 2 MS/s. The digital bitstream is decimated by averaging a specific number of bits, which returns to the concept of over-sampled data converters. By choosing the decimation factor, there will be a trade-off between the sample rate in the time domain and the resolution per sample. The decimation factor used here equals 10^4. Subsequently, MATLAB was used to further analyse the measurement data. The first measurement result is illustrated in Figure 2.20a, showing two seconds from a five-second interval during a frequency sweep for a range of $5-9$ Hz in the time domain. Despite the presence of noise and drift, the periodic signal of the resonance behaviour can be recognised. The noise was probably caused by interference from the surroundings, such as 50 Hz disturbance or Electromagnetic Interference (EMI) from the measurement equipment to the exposed wire bonds. When determining the average period of the time domain signal, it can be concluded that the frequency corresponds to the 8.7 Hz resonance frequency value.

Frequency domain: Tilt measurements After the time domain signal were analysed based on the discrete sample, the PSD of the signal was derived by applying an FFT operation on the data. For the analysis of the mechanical spectrum of the sensor chip, the effect of different tilt angles was investigated in this series of measurements. The tilt of the sensor was varied from 23° to 34°. For every measurement, a sweep of the mechanical excitation signal was performed while the capacitance was simultaneously sampled. The spectrum of the measurement results is included in Figures 2.20b-c. Here the resonance frequency can be clearly distinguished from the noise level, and is decreasing with increasing tilt angle. This response on the tilt angle can be expected from the combination of a fixed proof mass in combination with a softening spring. With increasing deflection, which is in turn caused by a larger tilt, a larger value for the gravitational force is working on the proof mass. The capacitive transducer is designed for device operation in line with the acceleration under test. Since we apply a tilt in this series of measurements, it can be expected that, due to the finite stiffness in the 'out-of-plane' direction, the magnitude of the capacitive response is influenced. The tilt measurements are used to identify the location of the resonance frequencies. In a final application, the tilt will be 90°, resulting in no 'out-of-plane' movement. The tilt measurements show that the resonance frequency of the sensor is tunable by varying the tilt. As a result, the mechanical sensitivity, being a direct function of the stiffness and thus implicitly related to the resonance frequency, of the sensor is also tunable. The lowest resonance frequency obtained with the fabricated sensor chip is 8.7 Hz with a tilt angle of 34°.

To further investigate the relation between the tilt angle and the resonance frequency, both figures are plotted against each other in Figure 2.20d. The plot in this figure was obtained by taking the maximum values from Figure 2.20c. It can be concluded from this result that the resonance frequency is highly sensitive to the tilt angle. Every 1° of increased angle results in a drop in the resonance frequency by approximately 1 Hz, which is significant in this low-frequency range. The degree of linearity can be explained by the simulation result included in Figure 2.10. The resonance frequency equals the square root of the stiffness over the mass, the first one being simulated to show a linear behaviour with deflection and the second one being constant. This measurement

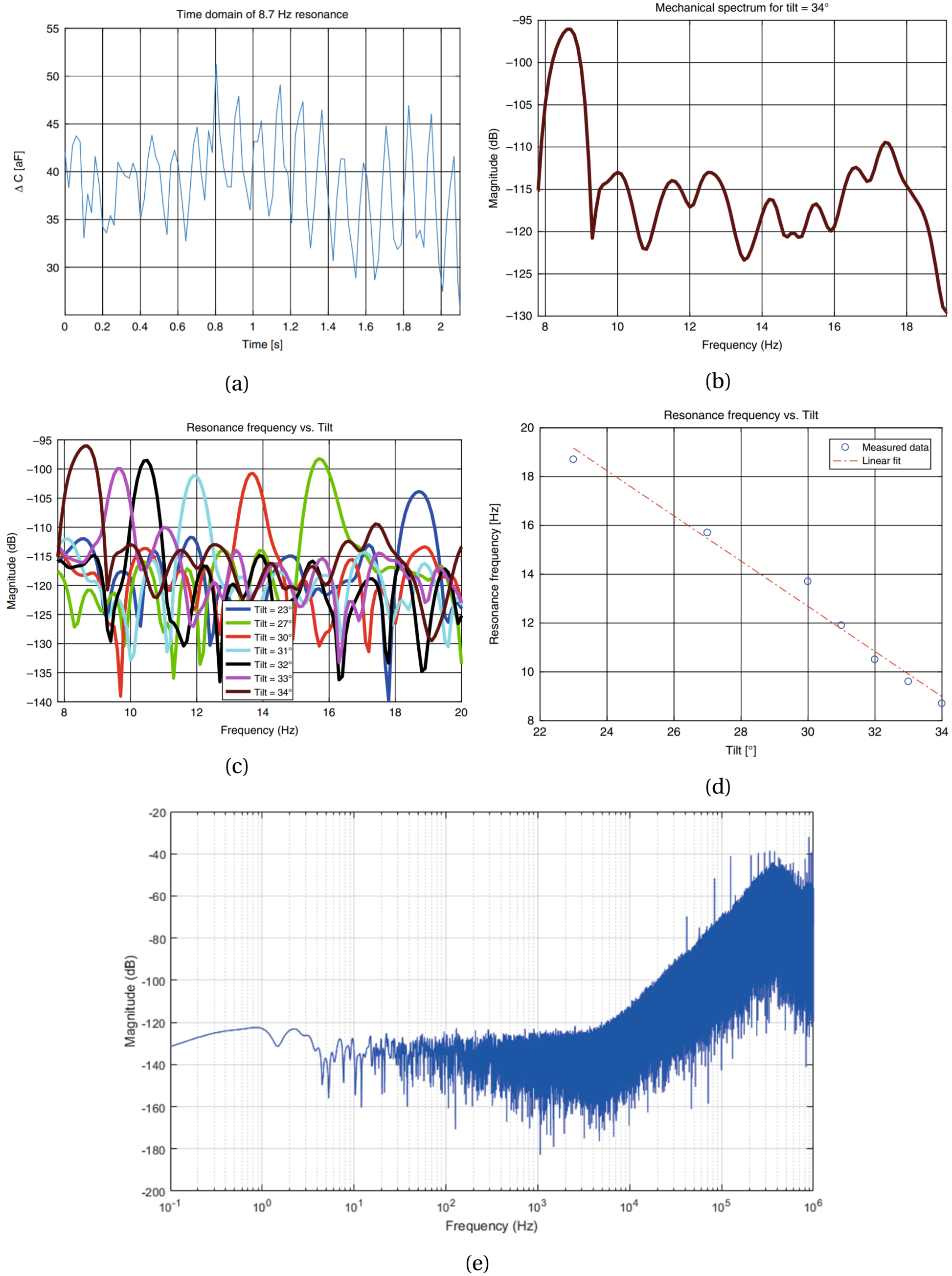


Figure 2.20: a) Measurement during resonance of the device at a tilt angle of 34° (time domain), b) Measurement during resonance of the device at a tilt angle of 34° (frequency domain), clearly showing the resonance tone at 8.7 Hz, and c) Mechanical spectrum of the device for tilts ranging from 23° to 34°, d) Resonance frequency as a function of the tilt, and e) Noise floor of the capacitive readout scheme.

shows again that by applying a tilt to the sensor chip, a trade-off can be carried out over the dynamic range, in terms of the operational bandwidth and measurement range, and mechanical sensitivity.

Sensitivity analysis of the measurement system The minimum detectable acceleration is determined by transferring back the total noise in the measurement system to the input. The two noise sources considered in a capacitive accelerometer are the thermal-mechanical noise and the noise originating from the analogue front-end electronics [12]. Determining the input-referred resolution is done by dividing each noise contribution by the sensitivities applicable, in this case, the mechanical- and capacitive sensitivities. The first one is dictated by the resonance frequency, whereas the second one is taken from the design of the IDT structure. The thermal-mechanical noise comes back to the derivation of the fluctuation-dissipation theorem [12], which means that the damping mechanism in the system produces a noise density based on the damping constant and temperature. In the design of this sensor, no additional damping was added, which means that the mass can move freely within its structure. The only damping available is that of the intrinsic damping of the material and that of the surrounding air. To analyse the thermal-mechanical noise, also called Brownian motion noise, the following derivation, which is already translated from force noise via displacement noise to acceleration noise, was used. The formula is described by Senturia [11].

$$a_n = \sqrt{\frac{4k_B T\omega_0}{m \cdot Q}} \qquad \left[ms^{-2}Hz^{-1/2}\right] \tag{2.16}$$

where k_B is the Boltzmann constant, T the absolute temperature, ω_0 the angular resonance frequency, m the mass and Q the quality factor. The latter is given by

$$Q = \frac{f_0}{f_2 - f_1} \tag{2.17}$$

Where f_0 is the resonance frequency, and f_1 and f_2 are the $-3\ dB$ frequencies on either side of the tone. Using frequencies f_0, f_1 and f_2 of 8.7 Hz, 8.3 Hz and 9 Hz, respectively, the quality factor is ~ 12.43. Using this in equation 2.16 yields 4.03 $ng/\sqrt{Hz}$. This value can be reduced using packaging where the air damping is minimized. Using the lowest resonance frequency of the device, the mechanical sensitivity is given by

$$S_{mech} = \frac{x(m)}{a(ms^{-2})} = \frac{1}{(2\pi 8.7)^2} = 3.35 \cdot 10^{-4}\, m/\ ms^{-2} \tag{2.18}$$

On the other hand, the capacitive sensitivity is determined by the IDT structure. According to the ASIC specifications, the resolution of the capacitive readout within a BW of 20 Hz, including the current-to-voltage converter and ADC of the ASIC chip is 0.137 $aF/\sqrt{Hz}$. The accelerometer IDT has a capacitive sensitivity of 0.2 aF/nm corresponding t a noise level of 0.054 $nm/\sqrt{Hz}$. Dividing this value by the mechanical sensitivity gives $1.62 \cdot 10^{-7}\, ms^{-2}/\sqrt{Hz}$ and by normalizing this value using the gravitational constant of ~ 9.81 m/s^2, this gives 16.54 $ng/\sqrt{Hz}$. Assuming no correlation between both the mechanical and

electrical noises, both input-referred noise power sources can be added. By taking the square root this yields an input-referred system resolution of 17.02 $ng/\sqrt{Hz}$.

2.8. CONCLUSION

In this work, a c-silicon bulk micro-machined mass/beam system has been designed, simulated, fabricated, tested and characterised. The device was processed, capped using glass dies, and wire bonded to a PCB containing a readout ASIC. The realised MEMS device with an integrated capacitive transducer was packaged and directly wire-bonded to a high resolution impedance readout system forming a measurement system. By using the non-linear force/displacement characteristic of the beams, an operating point has been created with extremely low stiffness. The vertical displacement of the proof mass is readout by a capacitive transducer which is integrated into the same bulk micro-machined silicon die. This is possible thanks to the trench isolation technique, which electrically separates both parts of the silicon bulk while keeping lithographic lateral resolution. The presented concept shows the potential for an integrated platform of an extremely compact MEMS + ASIC gravimeter, both on the package level, or even a monolithically integrated CMOS in the MEMS device.

When combining the lowest resonance frequency of 8.7 Hz, the capacitive sensitivity and the experimentally characterized noise floor of the readout chip, the theoretically obtainable system resolution equals 17.02 $ng/\sqrt{Hz}$. This figure for the theoretically obtainable resolution shows that the integration of the non-linear buckling-based compliant mass/beam system with the bulk micro-machined capacitive transducer yields a concept for a high resolution MEMS-based accelerometer. The proof of concept is promising for future iterations to yield a low-power, miniaturised and integrated MEMS solution for high-resolution acceleration measurements. Although stoppers have been designed to make the device robust against shocks, robustness testing and more extensive packaging design is open for future research. This work shows that the proof of concept is promising for future iterations.

2

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3

SIC UV DETECTOR AND KEY PROCESS STEPS

In recent years applications requiring optical detection have gained tremendous attention, particularly UV detection, thanks to its promising applications in civil and military fields. SiC ultraviolet detectors can effectively detect UV radiation thanks to their wide bandgap and can be applied in harsh environments thanks to the robustness of SiC. The detectors exhibit high quantum efficiency in the UV range from $200-400\ nm$*, high visible rejection ratio, low dark current and high speed. In this chapter, we introduce ultraviolet detection, the UV detectors, and some key SiC process steps.*

3.1. UV Detection Background

Optoelectronic devices are interesting thanks to their promising applications in civil and military fields [1, 2]. Unlike detection in long wavelength radiation detection, ultraviolet detection is of particular interest for use in corona discharge, flame detection (e.g. in engines), defence warning systems, missile guidance, communications, space-to-space communication, satellite guidance, space science, environmental monitoring, water treatment and healthcare [1–3].

Consider Figure 3.1 illustrating a common classification of UV radiation and showing its range which lies in 10 – 400 nm with a photon energy distribution of 3.1 – 124 eV [1, 4]. [5–8]. This classification is used because of the effects of UV radiation on the biosphere [9].

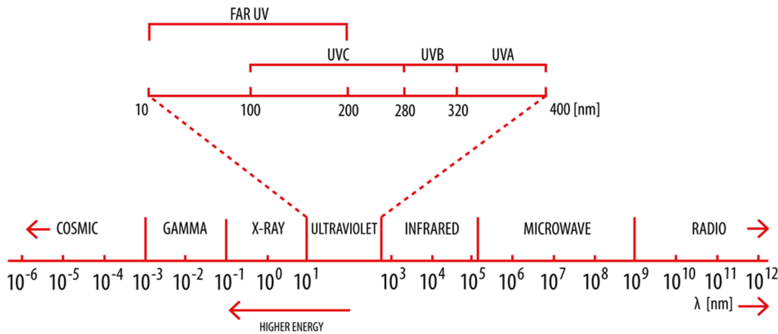

Figure 3.1: The electromagnetic spectrum with highlighted UV range.

Detectors operating in the spectral range above UVA are referred to as solar-visible [5]. A special part of the spectral range is the deep UV (DUV) range extending from 220 to 280 nm [5, 7]. DUV radiation from the sun is mostly absorbed by the ozone layer leaving longer wavelengths than 280 nm (UVC) to reach earth. This region is classified as solar-blind region (SBR) with little background interference allowing for robust signal detection [1]. Far UV radiation, also known as vacuum UV (VUV) is absorbed by the oxygen in the atmosphere [10]. Figure 3.2 illustrates photodetector classification [1, 9, 11].

Optical detectors come in two classes, namely photon (quantum) and thermal detectors. Photon detectors are photomultiplier tubes (PMTs), photoresistors, photodiodes, phototransistors and charge-coupled detectors (CCDs). Thermal detectors include thermocouples, bolometers and pyroelectric detectors. All thermal detectors measure heat due to photon absorption. Traditionally UV detection has been done using photomultiplier tubes (PMTs), thermal detectors, photodiodes or charge-coupled devices (CCDs). PMTs are capable of detecting very weak optical signals such as scintillation light thanks to their high gain and low noise [1, 10]. Moreover, the devices exhibit high responsivity, low dark current, low transport delay and high stability. However, PMTs react to a wide spectral range, need stable and high voltage biasing, are large and expensive and are susceptible to background radiation. Another major limitation of PMTs is the effect

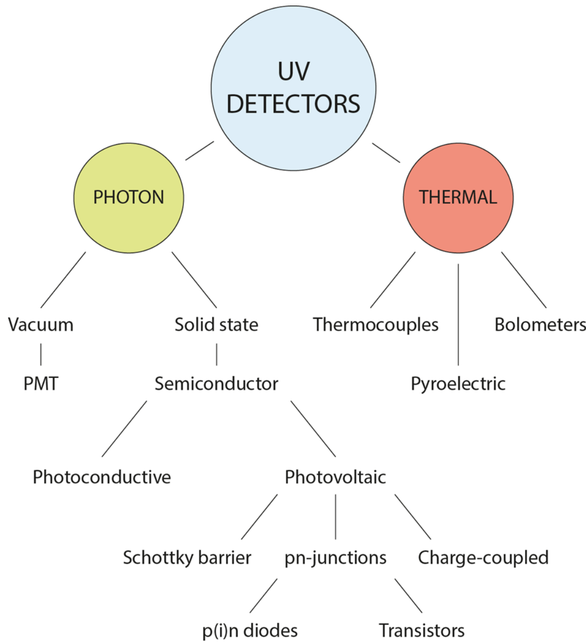

Figure 3.2: Photodetector classification.

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of magnetic fields on the responsivity, hence magnetic shielding is required for applications such partial discharge detection [12, 13]. Thermal detectors are generally used for calibration purposes but lack speed and are wavelength-independent [10]. Photodiodes and CCDs are solid state devices making them suitable for system integration. The devices require moderate bias while exhibiting better frequency response, linearity, low noise, high sensitivity to light and high operation speed [10]. Moreover, the devices are insensitive to magnetic field making them suitable for application such as corona discharge [10]. The maturity of silicon technology and ease of integration with CMOS readout circuits allow for low cost making them suitable for UV applications. However, the devices are limited to small area due to dark current being proportional to area, exhibit rapid increase in dark current at elevated temperatures, have poor temperature stability and require amplification at low illumination levels [14]. Moreover, current signals are not sufficient to drive circuits, hence amplification is always required. Furthermore, CCDs have lower detection range due to photon saturation charge as compared to photodiodes and deliver less noise [15].

Many of the above disadvantages can be overcome thanks to the properties of wide bandgap (WBG) semiconductors such as GaN, AlN and SiC. WBG semiconductor detectors can effectively detect UV radiation thanks to their wide bandgap and robustness in harsh optical conditions. Compared to silicon detectors, WBG detectors exhibit high quantum efficiency in the UV range of 200-400 nm, high visible rejection ratio, low dark current and high speed [16]. However, WBG materials still have obstacles to overcome process-wise, e.g. high dopant activation energy, ohmic contact formation, etching, etc.

Hence, pn-junction based devices have complex fabrication steps limiting their development as opposed to traditional silicon detectors. In this work, SiC is investigated for the fabrication of detectors based on epitaxial layer stacking. This overcomes the need for activation energy as epitaxial layers can be doped in-situ. Furthermore, formation of ohmic contacts can be done using rapid thermal annealing (RTA) allowing for good ohmic contacts [17, 18]. Thanks to its properties SiC can overcome many of the drawbacks of traditional detectors such as PMTs. Its wide bandgap, high thermal conductivity, mechanical stability and chemical stability not only enable UV radiation detection but operate under harsh conditions such as high temperatures. Moreover, silicon detectors undergo damage and degradation arising from exposure to high energy photons such as UV radiation. SiC detectors can withstand harsh optical conditions allowing for a longer lifetime while insuring long operation stability without premature degradation [10, 19]. Furthermore, its high electron saturation velocity and lower permittivity promise high-speed operation.

3.2. Ultraviolet Detectors

Semiconductor detectors can be based on three operation principles: resistive, Schottky and pn-junction based [1, 5, 8]. Consider Figure 3.3 showing photoconductor structures.

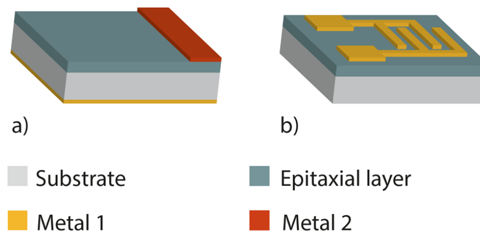


Figure 3.3: Photoconductor structures.

The photoconductor also referred to as a photoresistor, is an ohmic photodetector. As shown in Figure 3.3a the device has a simple design comprised of two electrodes on each side of the semiconductor. The absorption o f light is done on a single highly doped layer. An alternative is the metal-semiconductor-metal (MSM) structure shown in 3.3b where the device is comprised of a pair of ohmic electrodes on the top surface of a highly doped semiconductor absorbing layer. The MSM structure allows for simple fabrication. Apart from the buffer layer, only one layer is required for absorbing photons. This allows for fabricating SiC devices using commercial substrates with epitaxial stacked layers which relaxes the constraints on fabrication requirements, i.e. etching, implantation and annealing. Furthermore, the simple structures are CMOS compatible.

The fundamental principle of photocurrent generation in semiconductors is similar in all device types. Electrons in the valence band can be excited when incident photons with high enough energy are absorbed. When the electrodes are biased, the electrical field will drive the photo-generated e-h pairs to separate and move towards the elec-

trodes resulting in a photocurrent in the external circuit proportional to the photon lux [5]. In the absence of incident photons, the dark current (e-h pair generated by thermal energy) of a photoconductor is given by

$$I_d = \frac{V}{R_d} \tag{3.1}$$

Where R_d is the resistance of the material in the dark. Since the conductivity is dependent on the incident photons with sufficient energy, the resistance of the semiconductor will drop resulting in a photocurrent given by

$$I_p = V\left(\frac{1}{R_i} - \frac{1}{R_d}\right) \tag{3.2}$$

Where R_i is the resistance is the resistance under illumination. Figure 3.4 illustrates the I-V characteristics of the photoconductor in the dark and under illumination [6].

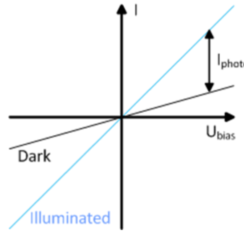


Figure 3.4: I-V characteristics of a photoconductor

The full expression for the photocurrent in a photoconductive device is given by [20]

$$I_p = \left(\frac{P_{opt}}{h\nu}\right) q\eta G = \left(\frac{P_{opt}}{hc}\right) \lambda q\eta G \tag{3.3}$$

With

$$G = \frac{\mu\tau V}{s^2} \tag{3.4}$$

Where P_{opt} is the incident optical power, V is the applied voltage, q is the electron charge, η is the quantum efficiency (QE), $h\nu$ is the photon energy, λ is the wavelength, c is the speed of light, G is the photoconductive gain, μ is the electron mobility, τ is the carrier lifetime and s is the inter-electrodes spacing.

The performance of the photoconductor depends on a number of physical parameters. For instance, a trade-off between a high gain G and a fast response has to be found for longer recombination lifetime of the holes making the device slower. The photoconductive nature of the device is that it requires a bias which inherently adds dark current to the noise contributions which reduces the minimum detectable optical signal. Moreover, the electric field effects such as space charge limited current, avalanche and dielectric breakdown, limit the photocurrent and therefore become an issue for scaling down

of photoconductor devices for higher-end applications. The scaling down is further limited by the area required for optical sensing to obtain any useful optical signal especially for devices with metallic electrodes which reflect light. This drawback can be reduced through transparent electrodes such as Indium Tin Oxide (ITO) or 2D materials such as graphene. Further enhancement of the device can be achieved by using nano-materials on the top surface to obtain higher photoconductive gain and responsivity [21].

Some of the drawbacks such as the large area requirement render the device only useful for applications with slower speeds. Furthermore, the output signal of the device will also depend on previously detected signals due to a photomemory effect. The photoconductive nature of the device also gives rise to a nonlinear relation between the resistance and illumination E_i as given by equation

$$R = AE_i^{-\alpha} \tag{3.5}$$

Where A and α are constants depending on the semiconducting material and the processing used to manufacture the device. Since the device changes resistance it is also highly temperature dependent adding to the uncertainty of the optical signal in the form of thermal noise.

MSM configuration can also be applied to the Schottky detector. The electrodes are then fabricated in an interdigitated configuration on top of a low doped absorption layer. Furthermore, the electrodes need a high metal workfunction to obtain a high Schottky barrier which is beneficial for lowering leakage current [22]. The MSM configuration results in the formation of two back-to-back diodes. Thanks to this, biasing will always result in one diode in forward mode while the other will be in reverse mode. Figure 3.5a illustrates this.

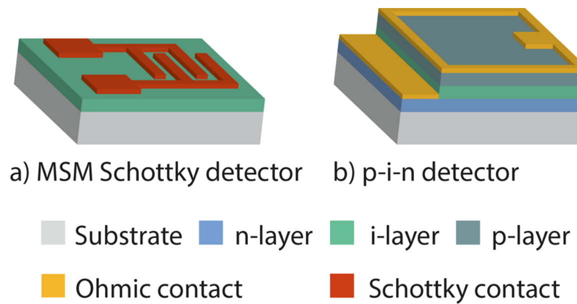


Figure 3.5: Photodetector structures.

Unlike the photoconductor, the devices allow for high-speed operations thanks to low capacitance per unit area [23]. The device speed is further enhanced by appropriate IDT design [24]. Furthermore, this device exhibits very little persistent photoconductivity (PPC) as opposed to photoconductors with the same configuration [5, 24]. PPC is a phenomenon where photocurrent response remains after removal of optical source for long periods [25]. MSM devices have an additional advantage over photoconductors

and pn-junction based detectors, namely ohmic contact is not required. This simplifies the fabrication while remaining CMOS compatible [23, 24]. The limitations of Schottky contact devices include higher leakage current compared to pn-junction based devices and limited maximum responsivity due to top metal electrode(s). Furthermore, the top metal will reduce the external quantum efficiency [24].

Traditionally, p-i-n devices are fabricated in silicon where the different regions are defined by implantation. However, for wide bandgap materials, this is not an option due to implantation limitations. Figure 3.5b illustrates a general structure of p-i-n based devices. This device also exhibits fast response but are slower due to drift time in the depletion region, diffusion of carriers and the relatively high depletion region capacitance. An advantage of these devices is their ability to operate in avalanche mode or even near breakdown (Geiger-mode). This allows for high sensitivities even in the range of single photon detection.

3.3. ANTIREFLECTIVE COATING

A vital part of a photodetector design is its antireflective coating (ARC) to reducing reflectance and increase its efficiency. In this work, silicon oxide (SiO_2) has been used as an ARC layer. Aluminium oxide (Al_2O_3) is considered in the text for comparison purpose. Therefore, (wet) thermal oxidation experiments of 4H-SiC wafers were carried out to define an oxidation model.

The interaction of incident light and the semiconductor material of the device has a major influence on the quantum efficiency and is characterized by four optical components, namely: absorption, reflectance, transmittance and refraction [26–28]. Figure 3.6 gives an illustration.

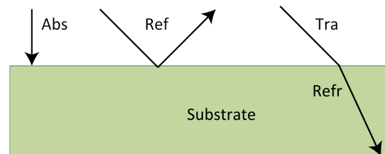


Figure 3.6: light interaction of a material.

3.3.1. ABSORPTION

Materials through which light can travel freely or with some attenuation are defined as transparent or semitransparent. On the other hand, a material is defined as opaque when light is completely reflected or absorbed. Hence, semiconductors are semitransparent depending on their respective bandgap energies. Therefore, absorption of light is set by two components, namely: absorption coefficient (α) and its reciprocal ($1/\alpha$), defined as penetration depth. The absorption coefficient of any material indicates its ability to absorb photons at a given wavelength. The penetration depth refers to the travel length of light through a material before its completely attenuated. Therefore, the absorbing layer(s) should have a thickness at least equal or larger than the penetration

depth for a given wavelength range. Compared to other WBG semiconductors such as GaN and ZnO, SiC has better penetration depth in the range of interest [29–31]. The penetration depth of SiC is around $1-5\mu m$ for the spectral range of $250-300nm$ while the other materials show penetration depths around $0.1\mu m$ for the same range. This means that most of the photons in this range are absorbed at the surface and result in high surface recombination, lowering the quantum efficiency. Therefore, SiC detectors will have higher QE for solar-blind applications. Hence, the absorption layer of the MSM device needs to have a thickness of $1-5\mu m$ to be sufficient for absorbing photons at $290nm$. Thanks to this, the possibility of native oxidation and the maturity of SiC technology, SiC is the better choice. Figure 3.7 shows the absorption coefficient as a function of wavelength. The data is obtained from the parameter files used by the Sentaurus TCAD simulation software.

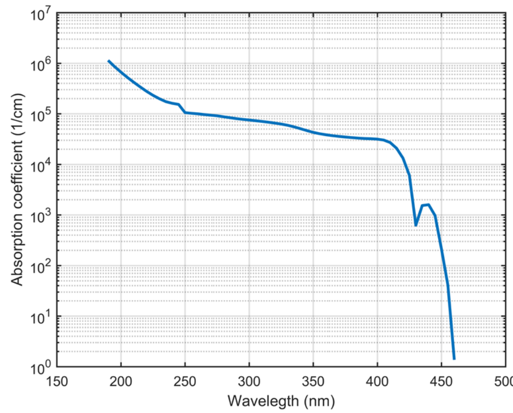


Figure 3.7: Absorption coefficient of 4H-SiC as a function of wavelength.

3.3.2. Refraction, Transmittance and Reflection

Light travelling from one medium into another experiences a change in propagation direction. That means light transmittance will experience refraction as shown in Figure 3.8. The bending degree of light is expressed by the refractive index (n), a constant obtained by taking the ratio of the sine of incidence angle to the sine of refraction angle. The refraction law, also known as Snell's law, can be derived using the speed of light in each medium with their respective angles of incidence and refraction. Consider equation (3.6).

$$\frac{v_1}{\sin(\theta_1)} = \frac{v_2}{\sin(\theta_2)} \tag{3.6}$$

Where v_1 and v_2 are the speeds of light in medium one and medium two, respectively. θ_1 and θ_2 are the incident and refractive angles, respectively. The equation can be rewritten in terms of refractive indices of the materials. The refractive index is a measure

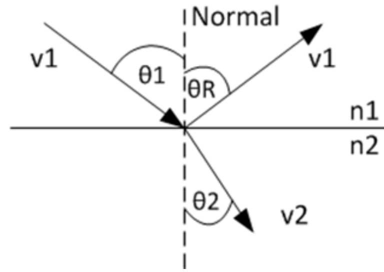


Figure 3.8: Representation of an incident beam of light. $v1$ and $v2$ are the velocities of light in mediums one and two, respectively. $\theta 1$, $\theta 2$ and θR are the incident, refractive and reflection angles of the light, respectively.

3

of the amount of bending light undergoes when it enters a medium and is expressed by equation (3.7).

$$n = \frac{c}{v} \tag{3.7}$$

Where c is the speed of light in vacuum and v the velocity of the corresponding medium. Figure 3.9 shows the refractive index as a function of wavelength for 4H-SiC. The data is obtained from the parameter files used by the Sentaurus TCAD simulation software.

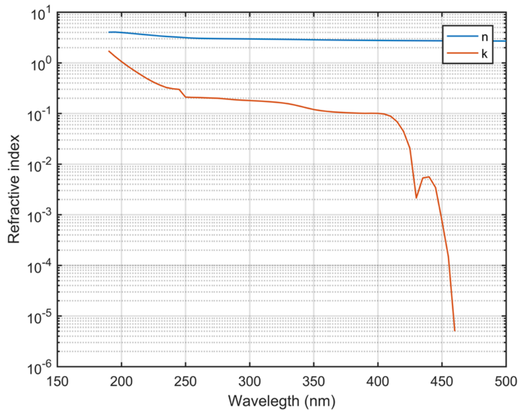


Figure 3.9: Complex refractive index of 4H-SiC. The blue line is the real part (n) of and the red line is the imaginary part (k) of the refractive index.

Using equations (3.6-3.7), Snell's law can be expressed by equation (3.8).

$$\frac{\frac{c}{n_1}}{\sin(\theta_1)} = \frac{\frac{c}{n_2}}{\sin(\theta_2)} \quad \Rightarrow \quad n_1 \cdot \sin(\theta_1) = n_2 \cdot \sin(\theta_2) \tag{3.8}$$

The angles are taken with respect to the normal, where the law of refraction assumes that the incident and refractive rays lie in the same plane at the point of incidence. Whenever light is travelling from a low n-value to a high n-value, light will bend close to the normal, thus the refraction angle will be less than the incidence angle. Equation (3.8) can be used to quantify the dispersion in a medium. Furthermore , the refractive index is dependent on the wavelength of the incident beam.

The refractive index has, next to the propagation angle, an important relation to absorption. When there is absorption, light will propagate and attenuate according to the extinction coefficient k. The coefficient is the imaginary part of the complex refractive index and is expressed by equation(3.9) where n is the real part.

$$\bar{n} = n + ik \tag{3.9}$$

Both parts of the complex refractive index of a thin film material can be obtained using Ellipsometry.

Reflection

Reflection is the bouncing of light rays from a smooth surface, without absorption or refraction (see Figure 3.8). The law of reflection states that light will be reflected with the same angle as the incident angle on the surface of the material. This is expressed by equation (3.10).

$$\theta_1 = \theta_R \tag{3.10}$$

To calculate the amount of optical power reflected from a surface, reflectance R is calculated. There are two cases to take into account, the s-polarized and p-polarized light. The s- and p- polarized light refer to incident light which is polarized with its electric field, either perpendicular or parallel to the incident plane. The two polarizations are orthogonal to one another which means that an incident electromagnetic wave can be decomposed in both components, namely: s- and p-polarization components. Equations (3.11-3.12) show the reflectance of s- and p-polarizations, respectively.

$$R_s = \left(\frac{n_1 \cdot \cos(\theta_1) - n_2 \cdot \cos(\theta_2)}{n_1 \cdot \cos(\theta_1) + n_2 \cdot \cos(\theta_2)} \right)^2 \tag{3.11}$$

$$R_p = \left(\frac{n_1 \cdot \cos(\theta_2) - n_2 \cdot \cos(\theta_1)}{n_1 \cdot \cos(\theta_2) + n_2 \cdot \cos(\theta_1)} \right)^2 \tag{3.12}$$

The above equations are known as Fresnel equations for perpendicular and parallel (s and p) polarized light. It should be noted that for this analysis the imaginary part is ignored since we are only concerned with reflection. This means that the extinction coefficient k is completely ignored. Furthermore, to simplify the analysis, we consider the case where $\theta_1 = \theta_2 = 0$, thus perfectly perpendicular to the incidence plane known as

reflection at normal incidence. This can be expressed in terms of the refractive indices of the two mediums according to equation (3.13).

$$R_s = R_p \quad \Rightarrow \quad \left(\frac{n_1 \cdot \cos(\theta_1) - n_2 \cdot \cos(\theta_2)}{n_1 \cdot \cos(\theta_1) + n_2 \cdot \cos(\theta_2)}\right)^2 = \left(\frac{n_1 \cdot \cos(\theta_2) - n_2 \cdot \cos(\theta_1)}{n_1 \cdot \cos(\theta_2) + n_2 \cdot \cos(\theta_1)}\right)^2 \tag{3.13}$$

Which leads to the relation given by (3.14).

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \tag{3.14}$$

3

3.4. ANTIREFLECTIVE COATING FOR 4H-SIC

As discussed in the previous section, the interaction of light with the sensor knows absorption, reflectance, transmission and refraction. The effect of reflection is the reduction in responsivity of the device and a drop in the quantum efficiency. To analyse this effect on 4H-SiC substrate, consider Figure 3.10 showing SiC coated by an ARC layer with a thickness of d_1.

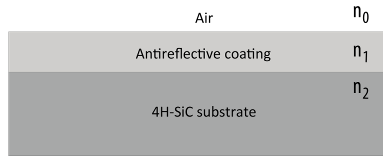


Figure 3.10: Air/4H-SiC interface.

It should be noted that the extinction coefficient (k) of the absorbing material is not considered since this is related to absorption, whereas reflection is only related to the real part (n) of the complex refractive index. By using the previously derived equations, the reflectance of 4H-SiC can be visualized as shown in Figure 3.11. The air is considered as the top layer having a refractive index close to that of vacuum, at a value of one.

Notice that the reflectance for the optical range of $190 - 500nm$ varies from $36 - 21\%$. At $290nm$ this is about 25%. To reduce the reflectance, an intermediate layer between the air and 4H-SiC is needed, i.e. an anti-reflective coating. There are several dielectric materials including SiO_2, Al_3O_2 and ZnO which can be applied as an ARC layer [32, 33]. Since SiO_2 is readily available, this material will be used in the fabrication of the photodetectors.

For normal incidence illumination, the expression of the reflected energy is then given by equation 3.15 [33].

$$R = \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos(2\theta)}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos(2\theta)} \tag{3.15}$$

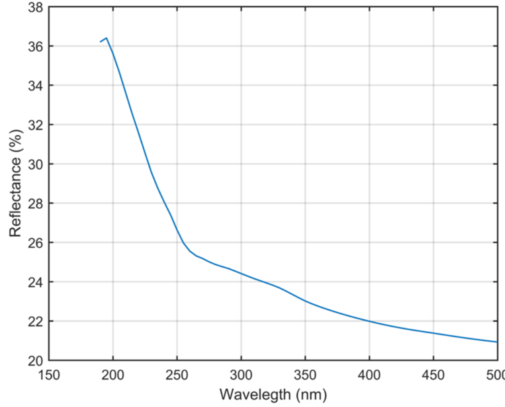


Figure 3.11: Reflectance of air/4H-SiC interface.

With the reflection coefficients $r_1$and r_2 given by (3.16)

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \qquad and \qquad r_2 = \frac{n_1 - n_2}{n_1 + n_2} \tag{3.16}$$

Where n_0, n_1 and n_2 represent the refractive indices of air, ARC coating and 4H-SiC, respectively. The phase shift θ caused by the ARC coating is given by (3.17)

$$\theta = \frac{2\pi n_1 d_1}{\lambda_0} \tag{3.17}$$

The minimum reflectivity for a single coating layer is fulfilled for (3.18)

$$R_{min} = \left(\frac{n_1^2 - n_0 n_2}{n_1^2 + n_0 n_2} \right)^2 \qquad where \qquad n_1 = \sqrt{n_0 n_2} \tag{3.18}$$

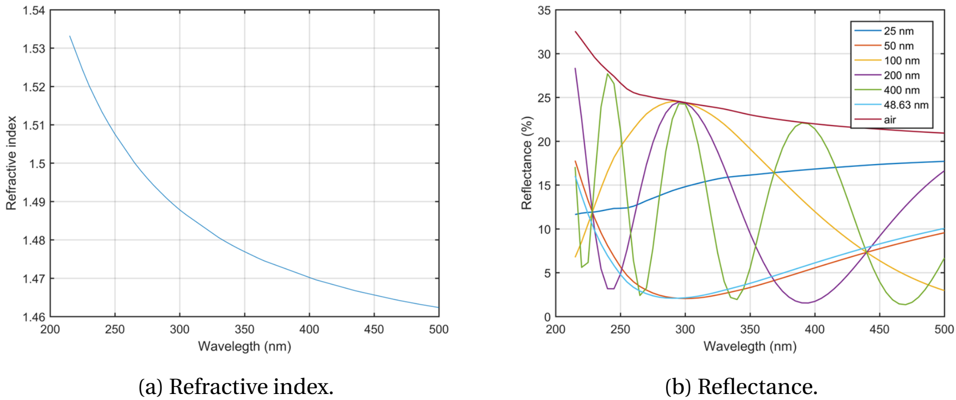
Furthermore, a rule of thumb for the thickness of the ARC layer is given by equation (3.19) [33].

$$n_1 d_1 = \frac{\lambda_0}{4} \tag{3.19}$$

By using the above equations, the reflectivity can be minimized for a wavelength λ_0. It should be noted that the calculated reflectivity will increase for wavelengths other than λ_0. In the case of solar cells, this would be considered disadvantageous, which would require multi-coating solutions to tackle this problem. However, in the case of photodetectors, this is advantageous since the photodetector can become selective.

SILICON OXIDE ANTIREFLECTIVE COATING

Consider the refractive index of SiO_2 shown in Figure 3.12a [34, 35]. It should be noted that there is no previous work showing the UV range values for the extinction coefficient of SiO_2. Using the equation from the previous section, the different layer thickness can be evaluated for the ARC layer. Figure 3.12b shows this.



(a) Refractive index.

(b) Reflectance.

Figure 3.12: SiO_2 ARC layer refractive index and reflectance at various layer thickness.

Figure 3.12b shows the reflection at normal incidence for various thicknesses, at the wavelength range of $215-500$ nm. Comparing the reflection with and without, it clearly shows that a properly chosen ARC with the proper thickness can significantly reduce the reflectance. The optimal thickness of SiO_2 ARC layer is calculated using equation (3.19) and is 48.63 nm. This value is close to that of 50 nm which will be the thickness of the ARC layer of the MSM device. This results in a reflectance of about 2.1% compared to that of about 25% at 290 nm. Furthermore, it can also be noticed that for some layer thickness, e.g. 400 nm, there is a selectivity that would be highly useful for filtering purposes. However, in the case of 290 nm wavelength, it is best to choose 50 nm SiO_2 thickness as an antireflective coating.

For the APD photodiode in Chapter 5 a thicker layer will be used to properly passivate the device. This will be done according to the equation (3.18) which results in Figure 3.13. From this figure, it shows that the reflectance behaviour is like a sinusoid for varying thickness. The APD will feature a 632 nm SiO_2 layer for passivation and anti-reflection.

ALUMINIUM OXIDE ANTIREFLECTIVE COATING

As mentioned before, Al_2O_3 is a good alternative and may even have slightly better ARC performance. Here we show that it has merit to be considered for future work. Figure 3.14a shows the refractive index of (Al_2O_3). Similar to SiO_2, there is no known extinction coefficient at the spectral range of interest. This means that there is no absorption associated with Al_2O_3. Figure 3.14b shows the reflectance for different Al_2O_3 ARC layer thickness at normal incidence for the spectral range of $215-500$ nm. Again a comparison is made between no ARC layer and different Al_2O_3 thickness. The optimal thickness

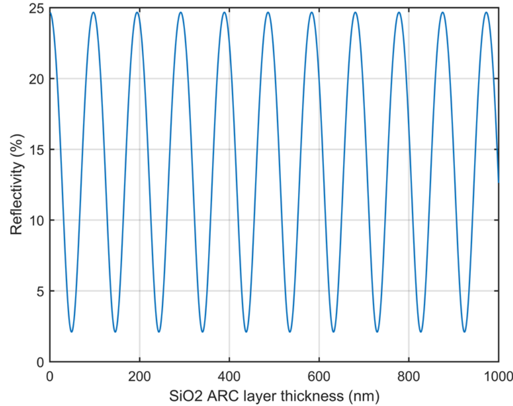
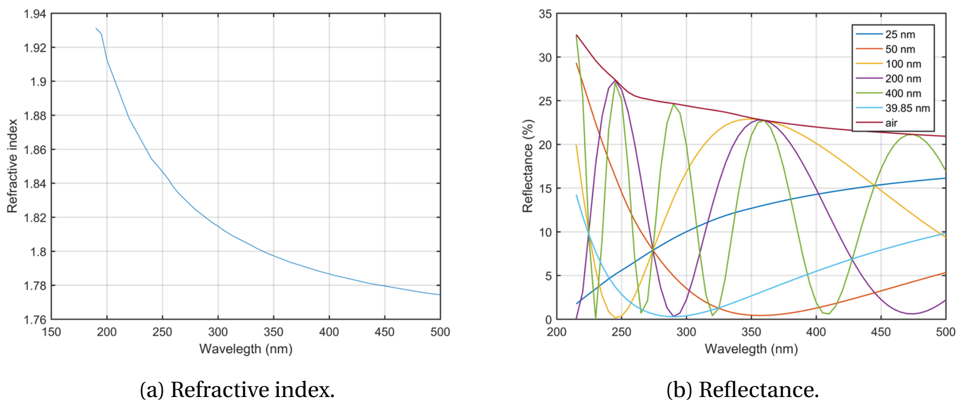


Figure 3.13: Reflectivity as a function of SiO_2 thickness.

is calculated using equation (3.19) which is 39.85 nm. The reflectance at the optimum thickness of the Al_2O_3 layer is about 0.29% compared to 25% at 290 nm.



(a) Refractive index.

(b) Reflectance.

Figure 3.14: Al_2O_3 ARC layer refractive index and reflectance at various layer thickness.

Another interesting observation is the reflectance at 200 nm Al_2O_3 ARC layer thickness. It can be seen that the reflectance is very low for 290 nm wavelength while increasing for other wavelengths. The reflectivity is barely higher than for the optimum thickness at a value of 0.31% while still lower compared to the SiO_2 ARC layer with the lowest reflectance. Furthermore, the reflectivity in the spectral range from 350 – 420 nm is high which helps in suppressing responsivity in this region. This means that Al_2O_3 is more suitable as an antireflective coating since it both reduces the reflection and shows a filtering property at the wavelength of operation. It should be noted that the above analysis for both types of antireflective coatings is done at normal incidence. This is done to reduce the complexity of manual calculations at different incidence angles.

3.5. WET THERMAL OXIDATION OF SILICON CARBIDE

An important process step in the fabrication of electronics is the use of thermal oxidation to grow a thin layer of SiO_2. Furthermore, thermal oxidation allows for precise control of gate oxide in device fabrication while reducing cost in terms of using oxide from processes, e.g. chemical vapour deposition (CVD) and pyrogenic oxidation [36]. This property, similar to silicon, is a unique advantage of SiC, giving it an advantage over other wide bandgap semiconductors such as gallium nitride (GaN). SiO_2 is applied for two main purposes: electrical insulation and dopant diffusion barrier, i.e. device isolation, gate oxide, sacrificial layer, etc. Figure 3.15 shows the unit cell of SiO_2.

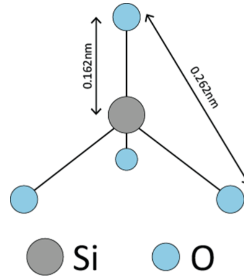
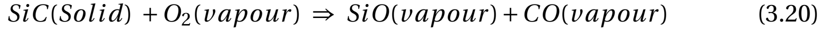


Figure 3.15: SiO_2 unit cell where a silicon atom has four bonds with oxygen atoms.

The unit cell of SiO_2 consists of a silicon atom with bonds to four oxygen atoms in a tetrahedron configuration [37]. SiO_2 can be obtained using thermal oxidation (wet or dry) or by chemical vapour deposition (CVD) methods where the best quality is obtained thermally. The process allows for clean/pure and intrinsically good insulators where the interface of Si/SiO_2 is excellent with low electric defects allowing for good gate oxide. The purity is enhanced by good cleaning before oxidation and adding hydrochloric acid (HCl) which reacts with mobile ions (contamination such as sodium and potassium). This results in excess chlorine (Cl) in oxide film but is less disadvantageous as this doesn't allow in charge move around from contaminants.

Thermal oxidation is called dry or wet depending on what reactant is used, O_2 or H_2O (vapour), respectively. The reactant gas is supplied to the wafer surface at a high temperature (> 800 °C) and a particular partial pressure. In Si processing dry oxidation is preferred for critical steps (gate oxide) because wet oxidation results in denser and less pure oxide. The latter is faster. However, in our case where the oxidation of SiC substrates is considerably slower than that of $Si-$substrates, we use wet oxidation. After the oxidation, a nitrogen ($N2$) annealing step is done to reduce surface states. Because SiC is a compound semiconductor consisting of $Si-$ and $C-atoms$, the oxidation will be more complex than for $Si-$substrates [38]. The chemical reaction of SiC oxidation can be either active or passive depending on the oxidising conditions, i.e. oxidising species, temperature, and total/partial pressure of of the oxidant. Active oxidation occurs at low oxygen partial pressures where a non-protective oxide film is expected as a result of SiO vapour formation [38]. This is given by (3.20).



$$SiC(Solid) + O_2(vapour) \Rightarrow SiO(vapour) + CO(vapour) \tag{3.20}$$

As for passive oxidation, this occurs at high oxygen partial pressures where a protective SiO_2 film is formed [38]. This is given by (3.21).

$$SiC(Solid) + (3/2) \cdot O_2(vapour) \Rightarrow SiO_2(solid) + CO(vapour) \tag{3.21}$$

Both oxidation behaviours occur at high temperatures. As can be expected, thermal oxidation of SiC undergoes several steps: 1) transport of reactant gas to the wafer surface, 2) in-diffusion of gas through the native/grown-oxide on the surface, 3) reaction with SiC atoms at the SiO_2/SiC interface, 4) out-diffusion of product gasses through the oxide layer, and 5) removal of the product-gasses form the oxide surface [39, 40]. Steps 2-4 are considered as the oxidation rate-controlling steps.

There have been many models established since the first model, by Deal and Grove (Fairchild Semiconductor), i.e. Massoud's empirical relation, interfacial Si emission model, and the Si and C emission model [39, 41–44]. The models predict the oxide thickness depending on the duration of oxidation, type of reactant (H_2O) or O_2), temperature, partial pressure, and doping. However, there is a discrepancy between the results of various researchers which can be attributed to differences in process conditions and doping, but more importantly, surface orientation. Thermal SiO_2 growth varies strongly w.r.t. crystal orientation, similar to Si, with the exception of more orientations: (0001) Si-, (11$\bar{2}$0) a-, (1$\bar{1}$00) m-, and (000$\bar{1}$) C-face [43, 45].

Deal and Grove [46] came up with the first kinetic mechanism/model for oxide growth whereas future models are usually an extension thereof, adding terms for accounting for the error in approximation (more on this later on). The model assumes a 1D structure based on two parameters which can be extracted from experimental results. In this work, we apply the D-G model without resorting to complex models to find the parameters of oxidation, while still having a reasonable prediction of oxide thickness. Thus we only consider the first three steps in the oxidation similar to $Si-$oxidation. Hence, the D-G model describes three steps in oxidation: 1) transport of oxygen to the wafer surface 2) oxygen diffusion through the oxide which is formed on the wafer to the $Si/SiO2$ interface 3) oxygen reaction with SiC atoms at the SiO_2/SiC interface.

Equations can be written for the first steps using Fick's law and Henry's law in terms of oxygen flux [46]. For our work, we jump right to the steady state solution for the flux of oxygen which is converted to the rate of oxide growth using the density of oxygen atoms in SiO_2 (N) as shown in (3.22-3.23)

$$\frac{t_{ox}}{dt} = \frac{J_{SS}}{N} \tag{3.22}$$

Thus

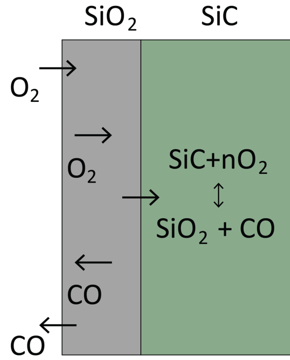


Figure 3.16: Reactions that take place in SiC during thermal oxidation. The steps are from top to bottom (Figure adapted from [39]).

$$J_{SS} = \frac{Hk_sP_g}{1+\frac{k_s}{h}+\frac{k_st_{ox}}{D}} \Rightarrow \frac{dt_{ox}}{dt} = \frac{Hk_sP_g}{N\left(1+\frac{k_s}{h}+\frac{k_st_{ox}}{D}\right)} \quad where\ h = \frac{h_g}{HkT} \tag{3.23}$$

Where J_{SS} is the steady-state oxygen flux. Here H is Henry's gas law constant, k_s is the rate coefficient for the reaction at the $Si-SiO_2$ interface, P_g is the partial pressure of the reactant in the gas phase, h is the effective transfer coefficient, D is the diffusion coefficient of reactant gas in SiO_2, t_{ox} is the oxide thickness, N is the density of oxygen atoms in SiO_2 ($N = 2.2x10^{22}cm^{-3}$ and $4x10^{22}cm^{-3}$ in for dry and wet oxidation, respectively), $h_g(= D/\delta)$ is the mass transfer coefficient, δ is the boundary layer thickness, k is the Boltzmann's constant and T is the absolute temperature.

To solve the equation we need to rearrange and integrate both sides of the equation for the oxide thickness from t_o (initial oxide thickness) to t_{ox} on the left side, and from 0 to t (time) on the right side. We start from t_o because we want to add the possibility of an initial oxide layer present on the SiC wafer. This is given by equation (3.24)

$$\int_{t_o}^{t_{ox}} \left(1+\frac{k_s}{h}+\frac{k_st_{ox}}{D}\right)dt_{ox} = \int_0^t \frac{Hk_sP_g}{N}dt \Rightarrow \int_{t_o}^{t_{ox}} (2t_{ox}+A)dt_{ox} = \int_0^t Bdt \tag{3.24}$$

Integrating and rearranging yields (3.25-3.26)

$$t_{ox}^2 + At_{ox} = B(t+\tau) \tag{3.25}$$

$$A = 2D\left(\frac{1}{h}+\frac{1}{k_s}\right); \qquad B = \frac{2DHP_g}{N} = \frac{2DC^*}{N}; \qquad \tau = \frac{t_o^2+At_o}{B} \tag{3.26}$$

Where τ is the initial time-constant which is a function of the initial thickness, hence it can be seen as an offset to the oxidation time before starting at t_o. For silicon, in the case of wet oxidation at starting point, τ can be neglected. Here C^* is the effective solubility limit in the oxide, related by Henry's law to the partial pressure in the atmosphere by (3.27)

$$C^* = H \cdot P_g \tag{3.27}$$

3

Using the above equations, the differential equation (3.23) can be written as

$$\frac{dt_{ox}}{dt} = \frac{B}{2t_{ox} + A} \tag{3.28}$$

Looking closely at equation (3.28), there is a linear regime for

$$\frac{dt_{ox}}{dt} \approx \frac{B}{A} \quad and \quad t_{ox} = \frac{B}{A}(t+\tau) \quad For \quad t_{ox} << \frac{A}{2} \tag{3.29}$$

Where B/A is referred to as the linear rate constant. Likewise, once dealing with thick oxide, there is a parabolic regime where there is a second-order equation. This is given by

$$\frac{dt_{ox}}{dt} \approx \frac{B}{2t_{ox}} \quad and \quad t_{ox}^2 = B(t+\tau) \quad For \quad t_{ox} >> \frac{A}{2} \tag{3.30}$$

Hence B is called the parabolic rate constant. The two constants B/A and A, are experimentally determined because not all quantities in the above equations are easily found. To determine the constants, we can use equation (3.28). By rearranging, integrating, and setting $t_{ox} = t_o$ and $t = \tau$, the initial time constant τ is given by

$$\tau = \frac{t_o^2 + At_o}{B} \tag{3.31}$$

The oxidation time and oxidation thickness can be found as

$$t = \frac{t_{ox}^2 - t_o^2}{B} + \frac{t_{ox} - t_o}{B/A} \quad and \quad t_{ox} = \frac{A}{2}\left(\sqrt{1 + \frac{4B}{A^2}(t+\tau)} - 1\right) \tag{3.32}$$

The equations (3.29) and (3.29) for the linear and parabolic regimes can also be seen as the estimations for very short and long oxidation times. Thus

$$t_{ox} \approx \frac{B}{A}(t+\tau) \quad For \quad t << \frac{A^2}{4B} \tag{3.33}$$

And

$$t_{ox} \approx \sqrt{Bt} \quad For \quad t >> \tau \quad and \quad t >> \frac{A^2}{4B} \tag{3.34}$$

It should be noted that even though the model is in full agreement with wet oxidation of silicon, this is not true for dry oxidation. However, as will be seen from the experimental results, this is not an issue for SiC for when wet oxidation is applied. To account for this, an assumption of 23 nm initial oxidation is used which is determined empirically [47]. In this work, we didn't add 23 nm as initial oxidation but only assumed 1 nm native oxide. To fit the model to the oxidation results, a multiplication factor to determine B is used. Furthermore, the model assumes the parameters B and A/B obtained from experimental results for a particular temperature and pressure. Thus to account for such changes, one would have to redo the experiments or look closely at the individual parameters such as D and k_s which are temperature-dependent. k_s is also affected by the crystal orientation and doping concentration. This is because the number of $Si-Si$ bonds per unit area change for different directions (similar for Si) [39]. As for the doping, there are less Si atoms available at the substrate surface.

3

In this work, we did not study the behaviour under changing conditions and only studied the thickness as a function of oxidation time. The crystal orientations studied are the (0001) Si and (000$\bar{1}$) C of highly doped ($10^{20}cm^{-3}$) n-type $4H-SiC$ substrates obtained from SiCC in China. Future work should include the study of all effects of SiC oxidation to get a better understanding. This will also help in properly simulating the oxidation with tools such as TCAD.

3.5.1. METHOD

The experiments were carried out on highly doped n-type $4H-SiC$ wafers with a doping concentration of ($10^{20}cm^{-3}$). Here wet oxidation has been used at a temperature of 1100 ^oC , followed by a lithography step to obtain structures for height measurements. After this, a wet etch step was performed using BHF to transfer the patterns into the SiO_2 layer. This was followed by the removal of the photoresist and measurements were carried out using a surface profiler (dekTak) to measure hills and valleys for both Si- and C-face orientations. This method allowed for a simple, yet accurate characterization procedure where the transparency of SiC is not an issue. Table 3.1 summarizes the oxidation durations and results thereof.

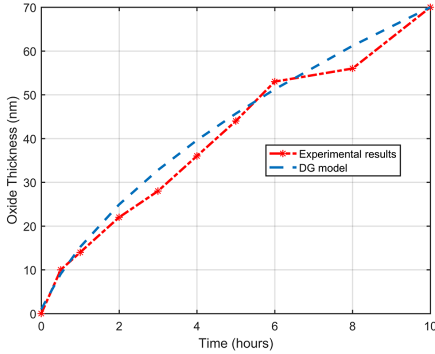
Table 3.1: Wet thermal oxidation at 1100 °C for various durations.

$t_{ox,1}(min)$	$T_{ox,Si}(nm)$	$T_{ox,C}(nm)$	$t_{ox,2}(min)$	$T_{ox,Si}(nm)$	$T_{ox,C}(nm)$
30	10	120	30	14	224
60	15	213	60	22	395
120	20	377	120	36	672
180	28	512	180	53	913
240	33	630	240	56	1082
300	38	750	300	70	1152

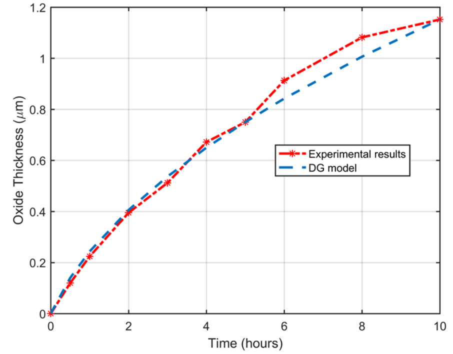
The oxidation was done in two steps each time, described by $t_{ox,1}$ and $t_{ox,2}$. Using the equations we have extracted the parameters for both Si- and C-face of the substrate. Table 3.2 lists these. Figures 3.17a and 3.17b shows the plot of the data fitted by the model.

Table 3.2: D-G parameters for wet thermal oxidation of SiC at 1100 °C for various *Si* and *C* crystal orientations.

$4H-SiC$	B/A	B
(0001) $Si-face$	20.697 nm/h	735 nm^2/h
(000$\bar{1}$) $C-face$	0.3453 $\mu m/h$	0.1991 $\mu m^2/h$



(a) Si-face oxidation.



(b) C-face oxidation.

Figure 3.17: SiCC oxidation results compared to the DG-model prediction.

It shows that the model is in good agreement for the extracted parameters and initial thickness assumption. As was mentioned a multiplication factor was used for the calculation of B which is 1.5 and gives a better fit of the model for both crystal orientations. To summarise, the model is a 1D representation and thus would not be adequate for substrates that are not simply planar but have some topography. The model will also not be accurate for highly doped substrates and a multiplication factor needs to be used. Therefore, more complex modelling should be investigated to obtain an accurate model which can predict oxidation in all directions.

3.6. Dry Etching of SiC

An important process step in device fabrication is the etching of structures in semiconductor materials, where either wet or dry chemistry can be used. However, wet chemical etching of SiC is extremely hard to achieve due to its high mechanical and chemical stability [48]. A method to still achieve wet chemical etching is to use molten sodium hydroxide/potassium ($NaOH/KOH$) eutectic. Alternatives can be anodic or electrochemical etching. However, the better option is to use dry etching, i.e. inductive coupled plasma (ICP), reactive ion etching (RIE) and deep reactive ion etching (DRIE). Of course these processes give varying results depending on the etch conditions and gasses used in the process. This is depending on the used etchers, reactants, power, temperature and pressure. In this work, we used ICP etching to obtain via structures, while RIE was used to obtain MESA structures for isolation purposes. These were used for the MSM and APD devices, respectively, and will be discussed in the next chapters.

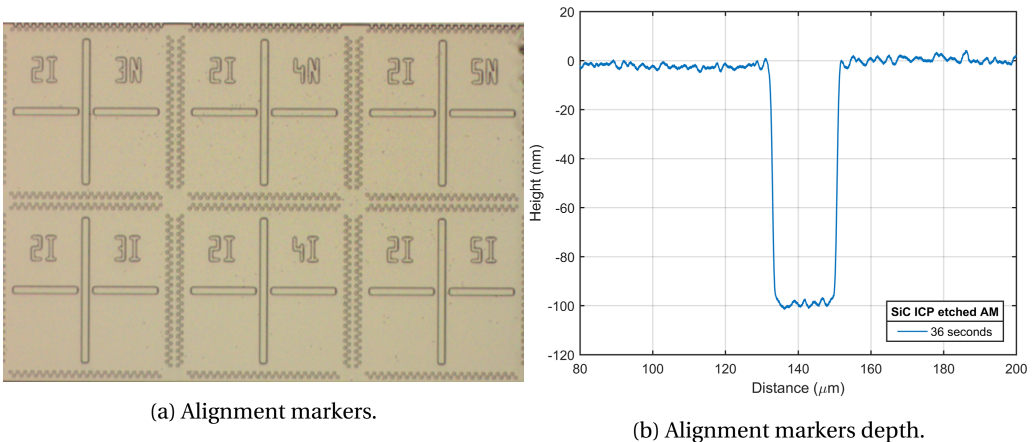
3.6.1. ICP ETCHING

ICP etching is one of the main etch processes used to etch silicon. This is usually used for shallow structures such as alignment markers which are merely 120 nm in depth. In this work, we used the ICP etching for the alignment markers in all processes. The processing of the SiC substrates is one similar to the RIE process (see next section) where the wafers are first coated with a metal layer at the backside, followed by a SiO_2 hard mask deposition. This is then patterned using BHF and the photoresist is removed. The last steps are the etching, removal of the SiO_2 hard mask, and measurements. The recipe is based on Chlorine (Cl2)/Hydrogen bromide (HBr) chemistry. Table 3.3 shows the etch parameters.

Table 3.3: Dry etching conditions for the ICP processing.

Process	ICP
Platen temperature	25 °C
RF power	50 W
ICP power	500 W
Gas 1	$Cl2/30\ sccm$
Gas 2	$HBr/40\ sccm$
Pressure	5 $mTor$

The first experiment was done to pattern alignment markers on $4H-SiC$ substrates and is shown in Figures 3.18.



(a) Alignment markers.

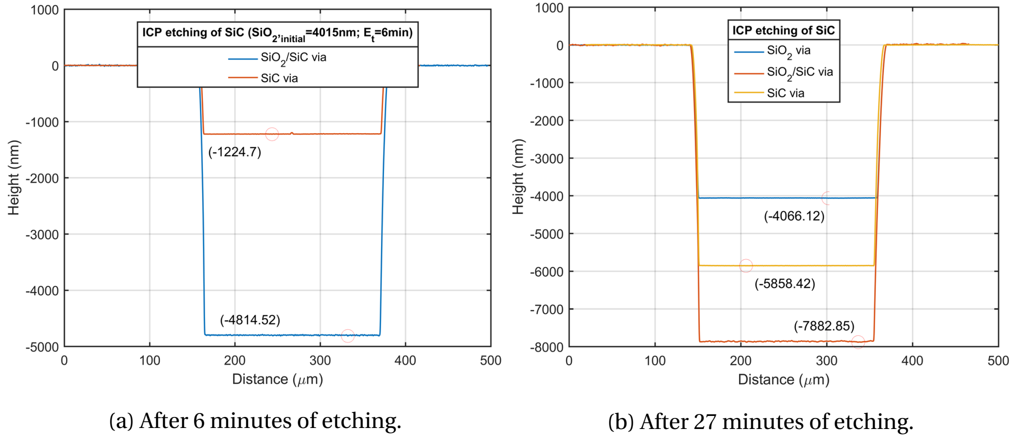
(b) Alignment markers depth.

Figure 3.18: Contact aligner alignment markers etched in $4H-SiC$.

This resulted in an etch rate of (3.35)

$$Etch\ rate\ SiC_{36sec} = \frac{t_{SiC,etched}}{d} = \frac{100}{36} = 2.78\ nm/s \tag{3.35}$$

It should be noted that the etch rate of SiC showed an increase with duration. The shortest showed an etch rate of 2.78 nm. Figures 3.19 show the surface profiler measurements from two etch instances.



(a) After 6 minutes of etching.

(b) After 27 minutes of etching.

Figure 3.19: ICP etching of 4H-SiC substrates.

The etch rates for 6 $minutes$ and 27 $minutes$, respectively, are given by (3.36-3.37)

$$Etch\ rate\ SiC_{6min} = \frac{t_{SiC,via}}{d} = \frac{1225}{360} = 3.4\ nm/s \tag{3.36}$$

$$Etch\ rate\ SiC_{27min} = \frac{t_{SiC,via}}{d} = \frac{5858}{1620} = 3.62\ nm/s \tag{3.37}$$

This is also true for the etch rate of SiO_2 which is given by (3.38-3.39)

$$Etch\ rate\ SiO_{2,6min} = \frac{t_{SiO2,init} - (t_{SiO2,via} - t_{SiC,via})}{d} = \frac{4015 - (4814 - 1224)}{360} = 1.18\ nm/s \tag{3.38}$$

$$Etch\ rate\ SiO_{2,27min} = \frac{t_{SiO2,init} - (t_{SiO2/SiC,via} - t_{SiC,via})}{d} = \frac{4066 - (7883 - 5858)}{1620} = 1.26\ nm/s \tag{3.39}$$

Since the etching is somewhat unpredictable, RIE is was used as an alternative.

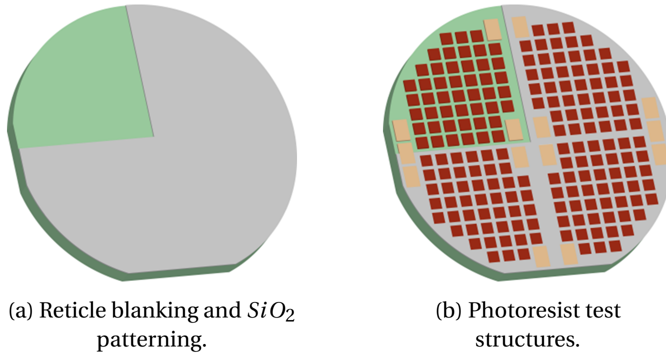
3.6.2. RIE ETCHING

The DRIE process, also known as the Bosch process, is a key process in the development of MEMS structures. This is the deep reactive ion etching where each etch cycle consists of two steps: semi-isotropic RIE etch of silicon and wall passivation. The semi-isotropic RIE etching is done using reactive gasses such as SF6. The passivation is done using a type of polymer. In literature, there have been reports of using a mixture of $SF6$ and O_2 to enhance the etch process [49, 50]. However, this process may also result in contamination where the etch chamber is coated by a SiO_2 layer. This occurs because of the O_2 reacting to the semi-isotropic RIE etched Si atoms which are deposited on the walls. To keep the processing clean, the etching of SiC should be followed by a DRIE etch process where the regular cycling of etching and passivation is used. This way, the built-up of contaminants is minimized. Next to the reactant mixture, the bias power and temperature of etching were also controlled. However, in this work we are not interested in deep structures, therefore anisotropic etching is not a requirement. We use a constant flow of $SF6/O_2$ chemistry [50] which was determined through a series of experiments to optimize the etch rates without etching the photoresist masking layer at a fast rate.

Etching requires in general a masking layer to enable selective bombardment. For Si etching, SiO_2 hard mask or a thick layer of photoresist are adequate where the first is usually used for through-wafer etching, similar to the work in Chapter 2 of this thesis. However, when dealing with materials such as SiC, etching is not as trivial due to the high mechanical stability of the material, Hence, it is preferable to use metal masking for the etching. Unfortunately, this is not allowed in the DRIE etchers in our facilities because it becomes a contamination source. Here the masking layer is also etched where the etched material is re-deposited, resulting in micro-masking. Furthermore, metal can deposit on the etch chamber walls and may be re-deposited on wafers which are subsequently processed using other recipes, which may lead to micro-masking and making processing unpredictable for other users. Hence in this work, we use a combination of SiO_2 and photoresist. This has another benefit where we can determine the etch rate of both masking layer types, simultaneously.

It should be noted that before starting the etching experiments, a 1 μm $Al(1\%)$ layer is deposited at the backside of the wafer. Thanks to this layer, the SiC substrate is not transparent for the detectors used by the deposition and etching tools. We chose to deposit a thick layer because one of the steps is the removal of SiO_2 using BHF which also attacks Al. Furthermore, the deposition of the metal on the BS of the SiC substrate was done by using a Si carrier wafer. This prevents the formation of a 'metal ring' at the FS of the SiC substrate. Therefore, after the $Al(1\%)$ deposition, each etch experiment starts with the deposition of a 4 μm SiO_2 hard mask. This layer is first patterned using reticle blanking of a negative photoresist (NLOF) layer to remove the photoresist only in one quadrant. This is followed by a BHF etch step to remove the oxide, completely exposing the SiC surface in the selected quadrant. This not only allows for etching SiC, but also in subsequent steps, the etching of photoresist and SiO_2. This is illustrated in Figure 3.20a.

The steps for patterning test structures on the entire wafer are: 1) coating the FS (Si-face) of the substrates with a thick photoresist layer (XT12), 2) exposure using a mask with test structures (DRIE-test), 3) dry etching, 4) resist stripping/cleaning, and 5) height



(a) Reticle blanking and SiO_2 patterning.

(b) Photoresist test structures.

Figure 3.20: Process for etching experiments.

measurements using the dektak surface profiler. Figures 3.20b illustrates the patterned photoresist structures on the entire substrate, partly on the exposed SiC surface and the rest on the rest of the substrate. Figure 3.21 shows the resulting structures used for the height measurements. The black dots are silicon haze from the $Al(1\%Si)$ layer.

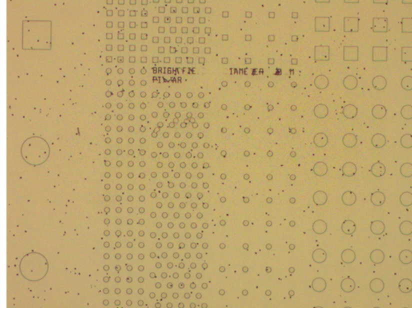


Figure 3.21: Test structures to determine the etch rate using ICP and RIE processing.

Table 3.4 summarizes the etch conditions used for our process. More on etching using this process will be discussed in the chapter on the APD devices.

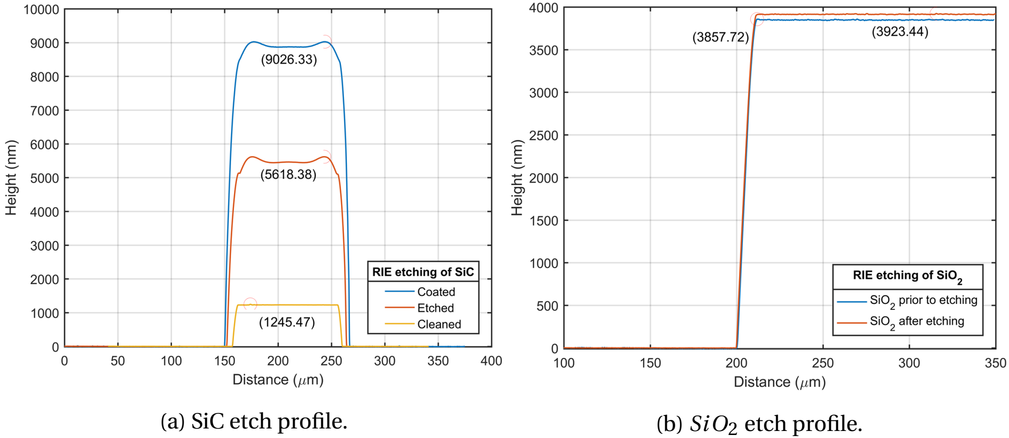
Table 3.4: Dry etching conditions for the RIE processing.

Process	RIE
Platen temperature	0 °C
Power	1000 W
Gas 1	$SF6/270\ sccm$
Gas 2	$O_2/30\ sccm$
Pressure	25 $mTor$

The temperature was set low to slow down the etch rate of the photoresist. At high temperatures it was observed that the photoresist was burned too fast, thus losing the structures. This was also true for different combinations of reactant concentrations. Here

adding a higher percentage of oxygen resulted in a higher etch rate of SiC but also faster burning of photoresist. Thus the ideal balance used is the 0.10.9/0.1 ratio of $SF6/O_2$ at a platen temperature of 0 °C and power of 1000 W.

Figure 3.22a shows the result of one such experiment. Note that the x-axis values do not match because of the needle of the surface profiler. This will always add an offset. From the shown heights we can calculate the etch rates for both SiC and PR, as well as the selectivity. Furthermore, from Figure 3.22b we can also obtain the etch rate of SiO_2 which helps in selecting an appropriate SiO_2 thickness when used as a hard mask for the etching process. The etch rates are (3.40-3.41-3.42)



(a) SiC etch profile.

(b) SiO_2 etch profile.

Figure 3.22: Etch profile of test structures using the RIE process.

$$Etch\ rate\ SiC = \frac{t_{SiC,etched}}{d} = \frac{1230}{1200} = 1.025\ nm/s \tag{3.40}$$

$$\begin{aligned} Etch\ rate\ PR = \frac{t_{PR,init} - (t_{PR,etched} - t_{SiC,etched})}{d} = \\ \frac{8864 - (5444 - 1230)}{1200} = 3.875\ nm/s \end{aligned} \tag{3.41}$$

$$\begin{aligned} Etch\ rate\ SiO_2 = \frac{t_{SiO2,init} - (t_{SiO2,etched} - t_{SiC,etched})}{d} = \\ \frac{3857 - (3923 - 1230)}{1200} = 0.97\ nm/s \end{aligned} \tag{3.42}$$

Thus the selectivity for SiC : PR is 1 : 3.78 while for SiC : SiO_2 this is 1 : 0.95. It should be noted that the results from etching in the rapier are reproducible where the etch rate barely changes. In the ICP etcher, this was different where longer etching resulting in higher etch rates. Thus it's recommended to use RIE etching based on $SF6/O_2$ chemistry instead of ICP based on $Cl2/HBr$.

3.7. Chapter Summary

In this chapter, UV detection is introduced along with photodetectors. The required antireflection coating was also discussed and showed that SiO_2 is a good choice for that. Thermally growing SiO_2 is one of the advantages of SiC over other WBG semiconductors. The oxidation of SiC was therefore investigated and characterized using the DG-model. Furthermore, 4H-SiC etching was also investigated by using the ICP and RIE processes. The results of this chapter were used to fabricate the devices in this work.

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4

MSM SCHOTTKY SENSOR

The metal-semiconductor-metal (MSM) Schottky device can be used for multiple sensing applications. In this work we investigate optical and temperature sensing mechanisms.

4.1. INTRODUCTION

THIS chapter describes the MSM device. The motivation behind the selection of this device lies in its multi-sensing capability. Here we introduce only two types, namely optical and temperature sensing. However, the same structure may be useful for other sensing applications such as magnetic, and gas. Schottky contact diodes can be obtained by using intrinsic or low doped semiconductors. The electrodes are required to have a metal work function, high enough to obtain Schottky barrier behaviour [1]. The contacts can be made as interdigitated electrode fingers (IDT) which result in back-to-back diodes. Furthermore, by combining this with semiconductors having a wide bandgap, UV photodetection is enabled [1–3]. The biasing of the two diodes will always result in reverse operation of one diode while the other is in forward bias enabling the conduction of the current. As was discussed in the previous text for the photoconductor, the device is simple to fabricate but has additional advantages such as low dark current, low junction capacitance, high bandwidth (BW) and is CMOS compatible [1, 4, 5].

As menstions, next to UV detection, temperature sensing can also be done using the MSM device, making it as a multi-sensing platform. This is enabled by adding a highly doped layer under the low doped layer. By adding contacts to it, the device can be used either as a temperature sensor or even as a magnetic sensor, where the bottom layer acts as a Hall plate. The device will need further investigation/optimization for practical use. However, here we can show that it's feasible for the device to be considered for multi-sensing applications.

4.1.1. METAL SEMICONDUCTOR SCHOTTKY CONTACT

To analyse the behaviour of the MSM device, first consider the metal-semiconductor (MS) Schottky diode shown in Figure 4.1. The device consists of low doped semiconductor with a metal top layer. An additional metal layer is used as an ohmic contact.

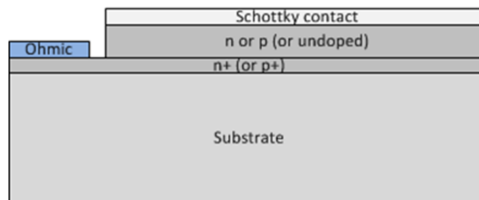


Figure 4.1: Metal-semiconductor Schottky contact.

As was mentioned in earlier text, when a metal is brought into contact with a semiconductor the electrical behaviour at the junction either takes the ohmic or Schottky characteristics. However, this device type is asymmetrical in the sense that the Schottky junction is only one-sided. Figures 4.2a-b show the band diagram of a metal and a n-type semiconductor before and after equilibrium. Here χ_s is the semiconductor electron affinity, ϕ_s is the semiconductor work function, ϕ_m is the metal work function, ϕ_B is the Schottky barrier height, V_{bi} is the built-in voltage, and W is the space charge region (SCR) width along the distance x. Figure 4.2a shows the Fermi levels of the metal and semiconductor before equilibrium is reached. Upon contact between the two materials,

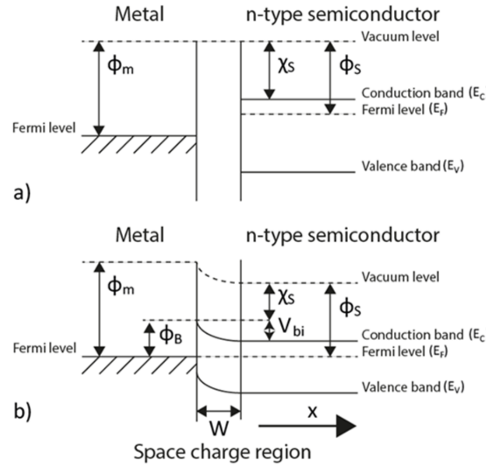


Figure 4.2: Band diagram of a metal and n-type semiconductor: a) before equilibrium and b) after equilibrium.

4

the Fermi energy level becomes constant throughout the structure reaching an equilibrium. This is thanks to the flow of electrons from the semiconductor into the lower energy states of the metal leaving positively charged ions behind, thus creating a depletion region (SCR). It should be noted that Figure 4.2b assumes the metal work function to be larger compared to that of the semiconductor else an ohmic contact will be the result. For p-type semiconductors this is the opposite. Table 4.1 summarizes the requirements for Schottky and ohmic contacts for both semiconductor types. Table 4.2 lists the work functions of several metals and the resulting barrier height for 4H-SiC having an electron affinity of 3.6 eV [6].

Table 4.1: Schottky contact workfunctions requirement.

Semiconductor	**Schottky (rectifying)**	**Ohmic**
n-type	$\phi_m > \phi_s$	$\phi_m < \phi_s$
p-type	$\phi_m < \phi_s$	$\phi_m > \phi_s$

As a result of the shown band bending, a potential barrier ϕ_B known as the Schottky barrier is seen by the electrons in the metal side trying to move to the semiconductor. Ideally, the Schottky barrier height is given by

$$\phi_B = \phi_m - \chi_s \tag{4.1}$$

The equation shows the Schottky contact dependence on the semiconductor electron affinity (χ_s) and the metal work function (ϕ_m). χ_s is given by

$$\chi_s = \phi_s - \left(E_c - E_f\right) \tag{4.2}$$

Table 4.2: Relevant metals and their workfunctions.

Metal	**Workfunction (ϕ_m) eV**	**Barrier height 4H-SiC (ϕ_B eV)**
Au	5.10	1.50
Ag	4.26	0.66
Al	4.28	0.68
B	4.45	0.85
Cr	4.50	0.90
Cu	4.65	1.05
Ni	5.15	1.55
Pt	5.65	2.05
Pd	5.12	1.52
Mo	4.60	1.00
W	4.55	0.95

On the other hand, after the band bending the electrons from the semiconductor side will also see a built-in potential barrier known as the built-in voltage V_{bi} given by

$$V_{bi} = \phi_m - \phi_s = \phi_B - \left(E_c - E_f\right) \tag{4.3}$$

As explained before, the semiconductor should be low doped to achieve Schottky barrier behaviour. The reason behind this is the dependence of the built-in voltage on doping similar to the pn-junction. This dependence is shown in equations (4.4-4.5).

$$E_c - E_f = \frac{k_B T}{q} ln\left(\frac{N_c}{N_d}\right) \tag{4.4}$$

Yielding

$$V_{bi} = \phi_m - \chi_s - \frac{K_B T}{q} ln\left(\frac{N_c}{N_d}\right) = \phi_B - \frac{K_B T}{q} ln\left(\frac{N_c}{N_d}\right) \tag{4.5}$$

Where k_B is the Boltzmann's constant, T is the temperature and N_d is the donor concentration. The built-in voltage is the barrier seen by electrons in the semiconductor which prevents further flow of electrons into the metal. N_c is the effective density of states in the conduction band and is given by

$$N_c = 4\sqrt{2}\frac{\sqrt[3]{\pi m^* k_b T}}{h^3} \tag{4.6}$$

Where m^* is the effective electron mass and h is the Planck's constant ($h = 6.63 \cdot 10^{-34} m^2 \cdot kg \cdot s^{-1}$). Figure 4.3 shows the built-in voltage dependence on the doping concentration of n-type 4H-SiC according to equation 4.5. Here we assumed Nickel is used as a Schottky metal contact at a temperature of $300K$. To calculate the effective density of states, the anisotropic nature of the 4H-SiC should be considered since the effective mass varies for different crystal orientations.

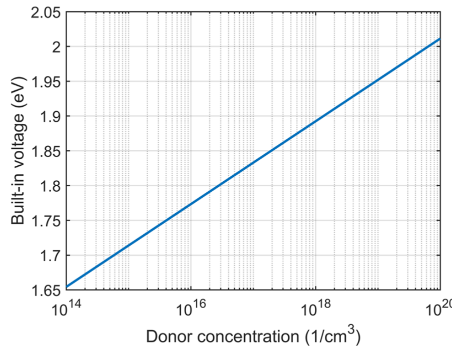


Figure 4.3: Built-in voltage as a function of the donor concentration in the n-type semiconductor.

The asymmetrical design of single Schottky contact diodes allows for operation in forward and reverse modes. The Schottky barrier height changes accordingly as shown in Figures 4.4a-b.

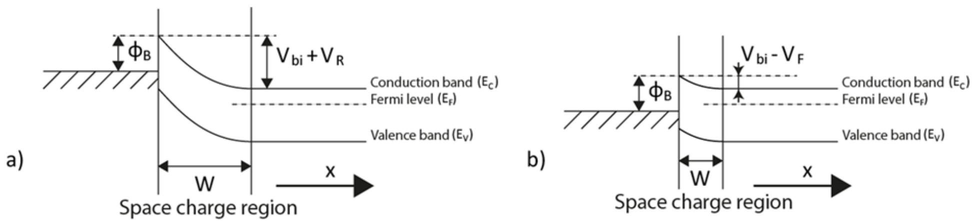


Figure 4.4: Ideal band diagram of a metal and n-type semiconductor: a) under reverse bias and b) under forward bias.

The electrons in the semiconductor will easily diffuse across the SCR into metal for a sufficiently reduced barrier height due to forward bias ($V_{bi} - V_F$). On the other hand, for $V_{bi} + V_R$ the barrier will be increased blocking the electrons. Furthermore, the above diagrams are very similar to those of a pn-junction resulting in a similar I-V characteristics with exponential behaviour. However, the current mechanism in the MS junction is due to the flow of majority carrier electrons as opposed to the pn junction, allowing for high speed operation. The high speed is also thanks to the one-sided depletion region of the Schottky diode. Similar to a pn junction the electrostatic properties, the electric field and SCR width, can be determined starting with Poisson's equation. Consider

$$\frac{dE}{dx} = \frac{\rho(x)}{\epsilon_0 \epsilon_r} \tag{4.7}$$

Where $\rho(x)$ is the SCR volume density and $\epsilon_0\epsilon_r$ is the permittivity of the semiconductor. Integrating the above equation yields

$$E = \int \frac{qN_d}{\epsilon_0 \epsilon_r} dx = \frac{qN_d x}{\epsilon_0 \epsilon_r} + C_1 \tag{4.8}$$

To solve for the integration constant, assume the electric field at the SCR edge of the semiconductor to be zero.

$$C_1 = -\frac{qN_d x}{\epsilon_0 \epsilon_r} \tag{4.9}$$

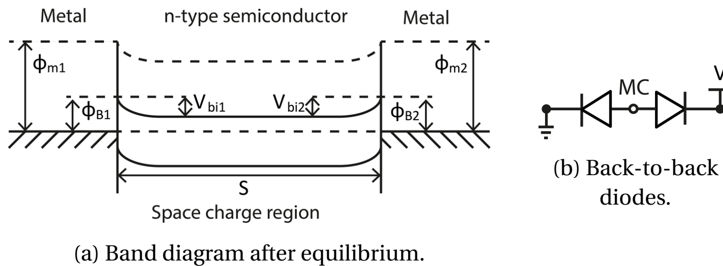
Assuming the SCR starts at $x = 0$ and extends to $x = W$, the electric field at any pointy in the x-direction can be written as

$$E = -\frac{qN_d(W - x)}{\epsilon_0 \epsilon_r} \tag{4.10}$$

The SCR width can be determined by assuming a highly doped p layer to represent the metal in a p^+n junction. The SCR in the n-type semiconductor under a reverse bias then becomes

$$W = \sqrt{\frac{2\epsilon_0 \epsilon_r (V_{bi} + V_R)}{qN_d}} \tag{4.11}$$

It should be noted that the photo-generated e-h pairs outside the SCR will recombine before reaching the electrodes. Charge carriers generated in the SCR will be collected at the electrodes before recombination takes place. Now that the single junction contact is introduced, this can be extended with a second contact. Consider Figures 4.5a showing the MSM band diagram after equilibrium and the back-to-back diodes.



(a) Band diagram after equilibrium.

(b) Back-to-back diodes.

Figure 4.5: MSM device representations.

As can be seen from Figure 4.5 the two contacts to the semiconductor are symmetrical of nature. However, when a bias is applied to the device this symmetry is broken where one barrier height is increased and the other is lowered. This results in an operation where one diode is always reverse biased and the other forward biased allowing the flow of charge carriers to form a current in an external circuit. As a consequence, the MSM Schottky device will exhibit non-linear I-V characteristics. This method allows for a low dark current, hence the minimum detectable signal capability is enhanced. Of course, to

keep the dark current as low as possible, the crystal quality of the semiconductor should be high as possible while the electrodes should have a high metal work function to obtain a high Schottky barrier height [7]. Similar to the single Schottky contact, high speeds can be achieved thanks to the low junction capacitance and high BW is available.

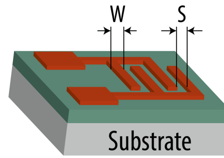


Figure 4.6: MSM structure.

Consider Figure 4.6 illustrating a MSM device where L is the length of a single finger electrode, S is the separation between the opposing electrodes and W is the widths of the finger electrodes. In this work, we have used only one width for simplicity, but two widths can be used. This enables asymmetry by geometrical design to enhance the performance of the device. Changing the width of both electrodes can also have a significant influence on the performance similar to increasing the bias voltage [8]. A Au/ZnO MSM device was designed with two electrode widths where one electrode was fixed and the other decreased [9]. The device showed at a ratio of 20 : 1 an enhancement in the responsivity from 0.3 mA/W to 20 mA/W at the same conditions, while operating in photovoltaic mode at 0 V as a self-powered device. Moreover, the device showed an enhanced operation speed. The effect of electrodes asymmetry was explained as a strong influence on the electrical field distribution built in the Schottky junction where the electrical field can prevent the recombination of photo-generated e-h pairs, and separate the photogenerated carriers more efficiently.

4.1.2. MS SCHOTTKY CONTACT CURRENT MECHANISMS

The current mechanisms in Schottky contact devices is thanks to three main mechanisms: thermionic emission (TE), thermionic field emission (TFE) and field emission (FE) [7]. Figure 4.7 illustrates these effects.

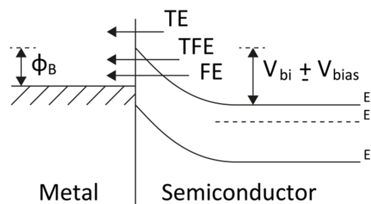


Figure 4.7: Schottky contact current mechanisms.

Thermionic emission describes the electron flow over the potential barrier when the charge carriers gain enough thermal energy while assuming the barrier height to be larger than the thermal voltage (kT/q). This is dominant in moderately doped semiconductors operating at room temperature and is used to describe the current density-

voltage characteristics of the MS Schottky contact. The current density given by TE is according to equation (4.12).

$$J = J_s\left(exp\left(\frac{qV}{k_B T}\right) - 1\right) \tag{4.12}$$

Where V is the applied voltage. The saturation current J_s is given by

$$J_s = A^{**} T^2 exp\left(-\frac{q\phi_B}{k_B T}\right) \tag{4.13}$$

Where A^{**} is the effective Richardson constant. This equation allows for the calculation of the barrier height using the I-V characteristic of a MS Schottky device. J_s is found experimentally.

Thermionic field emission results from high electric field application to the semiconductor under temperatures relatively higher than room temperature. As a result, the current density due to this mechanism will be higher as compared to TE and FE mechanisms.

Field emission, also known as quantum tunnelling, is due to the narrowing of the potential barrier as a result of a high electric field giving the electrons a higher probability of tunnelling through the barrier. This mechanism is more dominant for high doping concentrations in the semiconductor or at low temperatures. The tunnelling current is given by

$$J_t = J_{ts} exp\left(-\frac{q\phi_B}{E_{00}}\right) \tag{4.14}$$

Where J_{ts} is the tunnelling saturation current and E_{00} is the characteristic tunnelling energy related to the tunnelling effect transmission probability. E_{00} is given by

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_d}{\epsilon_s m^*}} \tag{4.15}$$

This parameter helps predict which mechanism will be dominating depending on three conditions given by the ratio $E_{00}/k_B T$ as shown by

$$Condition\,1: \frac{E_{00}}{qk_B T} \leq 0.2 \tag{4.16}$$

$$Condition\,2: 0.2 < \frac{E_{00}}{qk_B T} \leq 5 \tag{4.17}$$

$$Condition\,3: \frac{E_{00}}{qk_B T} > 5 \tag{4.18}$$

From these equations it should be possible to calculate at room temperature and see that TE dominates at $N \leq 3 \cdot 10^{17}\ cm^{-3}$ and TFE at $3 \cdot 10^{17}\ cm^{-3} \leq N \leq 2 \cdot 10^{20}\ cm^{-3}$. At

higher doping levels FE becomes dominant. Recombination in the SCR and recombination in neutral region under forward bias also contribute to the current. For this work TE is considered since low doped semiconductors are used for the fabrication of the MSM Schottky devices. There are other effects in the device associated with the metal-semiconductor contact. Such can be the image-force, interface layers, traps and other defects, etc. Such effects may be discussed when relevant for the characterization of the device.

4.2. DESIGN FOR UV DETECTION

THE MSM device design is mainly focussed on the UV sensing part because the geometrical parameters of the device influence it more than it should influence the temperature behaviour. Consider Figure 4.8 showing the basic MSM structure.

4

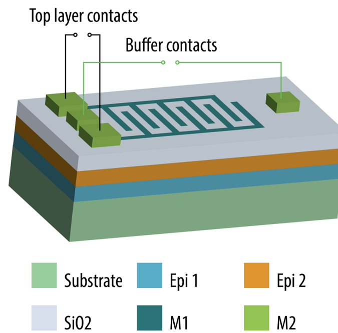


Figure 4.8: 4H-SiC MSM sensor for multi-sensing applications

The MSM device is fabricated using two epitaxial layers on top of a highly doped n-type 4H-SiC monocrystalline substrate. As an electrode material, a metal layer will be deposited and patterned. Next to the metal layer, an ARC layer will be deposited and patterned to increase the efficiency of the device. The physical parameters for the basic design are listed in Table 4.3. To see the effects of these parameters on device performance, we simulated using TCAD Sentaurus.
In the simulations only nickel has been used as the electrode material. The material type affects the Schottky barrier height which in turn affects the dark current and noise performance. It has a theoretical workfunction of 5.15 eV, which results in a barrier height of 1.85 eV which is assumed to be ideal. Here, the electrodes are assumed to be reflective (opaque), i.e. no absorption takes place in the semiconductor at the electrode sites. The latter results in big losses since the effective exposed area is significantly smaller compared to the total surface area. A method to overcome this is the use of semi-transparent electrodes. In this work, we simulated for nickel as the metal layer while in the experimental work we also fabricate using other metals, i.e. platinum (Pt), palladium (Pd) and molybdenum (Mo). Another parameter which affects the performance of the device is its size, adding not only to photocurrent, but also to noise. The simulations assume a single size while three different sizes have been fabricated.

Table 4.3: Geometrical parameters for the basic design used in the simulation.

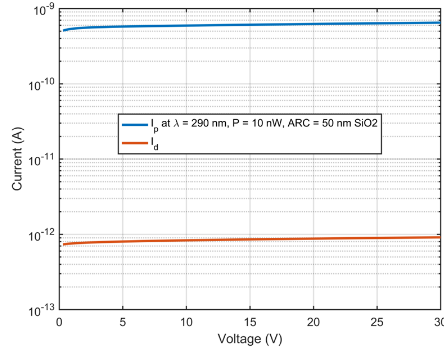
Parameter	Setting
Size	$250x250\,\mu m^2$
Electrode material	Nickel
Finger width	$5\,\mu m$
Finger spacing	$5\,\mu m$
SiO_2 ARC thickness	$50\ nm$
Epitaxial (absorption) layer	n-type
Epitaxial layer doping concentration	$10^{16}\ cm^{-3}$
Epitaxial layer thickness	$5\,\mu m$
Substrate (n-type) doping concentration	$10^{20}\ cm^{-3}$

The voltage is swept from $0-30V$ where one of the diodes is always in reverse bias while the other is always in forward bias. At higher voltages, the depletion region between the opposing electrode fingers is assumed to be completely depleted. Furthermore, we assume the incident light to be unpolarised and set the optical power density to $16\mu W/cm^2$. This results in $10nW$ for the given device surface dimensions. Figure 4.9a shows the IV-response of the basic MSM device. As can be seen, the dark current is less than $1pA$ at $30V$ biasing. The photocurrent is almost three magnitudes higher with a value of $0.65nA$, giving a photo-to-dark ratio of $7\cdot10^2$. Figures 4.9b-4.9c show the spectral response and quantum efficiency (QE) of the basic device, respectively.
The photodetector shows a typical response in the UV spectral range. The responsivity at the wavelength of $290nm$ is $0.0648A/W$ compared to $0.0574A/W$ when there is no antireflective coating. This is an increase of about 12.9%. The quantum efficiency of the device with and without an antireflective coating is 27.71% and 24.54%, respectively. This efficiency is low due to the large area covered by the electrodes. Therefore, semi-transparent electrodes should be used. Furthermore, the efficiency also drops due to some reflection from the antireflective coating and from recombination processes in the 4H-SiC material. The QE drops to $< 0.01\%$ at the cut-off wavelength of $400nm$. Thanks to this, the device is completely visible-blind.

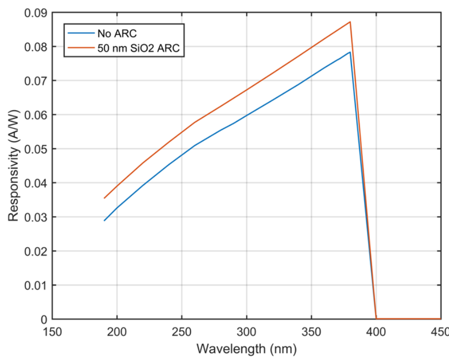
4.2.1. Absorption layer

Next to the metal layer, the absorption layer has a significant on performance in terms of thickness and doping concentration. Therefore, both physical parameters should be selected to achieve the best results in terms of responsivity, quantum efficiency and more importantly, low dark current and noise contributions to the output signal. Recalling from section 3.3.1, a thickness of $1\ \mu m$ should suffice. As for the doping concentration, this should be as low as possible, starting from $10^{14}\ cm^{-3}$ for the n-type material. Similar to the previous simulation, the optical power intensity of the unpolarised light is set to $16\ \mu W/cm^2$ and the voltage is swept from $0-30\ V$. Figures 4.10 show the responses of the MSM device for varying absorption layer thickness.

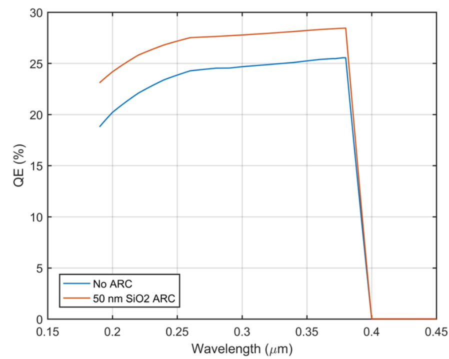
Figure 4.10a shows that the photocurrent is about the same for layer thickness starting



(a) IV-response as a function of voltage.



(b) Responsivity as a function of wavelength.

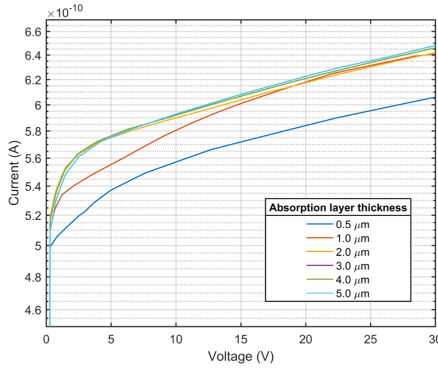


(c) QE as a function of wavelength.

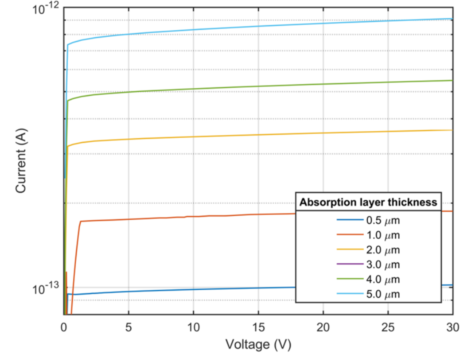
Figure 4.9: Response of the $250x250\mu m^2$ MSM basic device.

from 3 μm. The dark current response shown in Figure 4.10b is lowest for the thinnest absorption layer and increases for thicker layers similar to the photocurrent. Therefore, the responsivity increases for thicker absorption layers as shown in Figure 4.10c. The lowest thickness of 0.5 μm strongly diverts from the other responses because of the penetration depth of UV light. As mentioned before, the penetration depth at the spectral range of $270-300$ nm is $1-5$ μm which results in the absorption of most photons in the 4H-SiC material. By having thicker layers, an improvement in the responsivity and efficiency of the device can be seen. Figure 4.10d shows the quantum efficiency of the device which gives the same conclusion, namely that thicker layers will give better performance. Therefore, for this work, the absorption layer thickness of 5 μm is used.

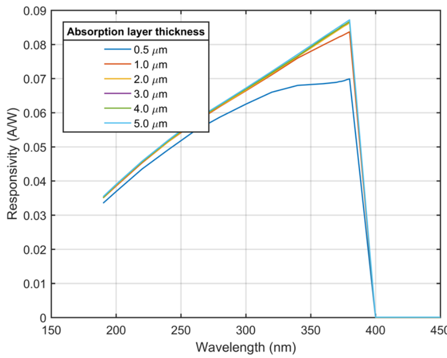
Continuing on the previous simulations, the doping concentration of the absorption layer has a strong effect on performance. Here, as was mentioned, the dominant current mechanism of a Schottky contact is thermionic emission. The doping concentration condition for this is given by $N \leq 3 \cdot 10^{17} cm^{-3}$. Higher doping concentrations would result in the reduction of the Schottky barrier and results in a more ohmic contact be-



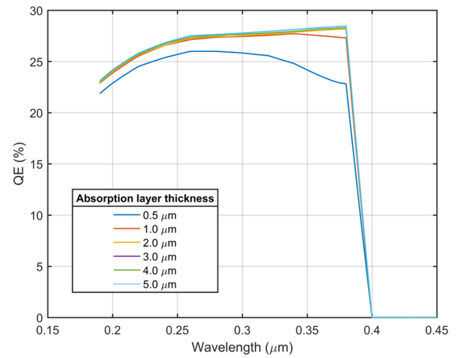
(a) Photocurrent response as a function of voltage.



(b) Dark current response as a function of voltage.



(c) Responsivity as a function of wavelength.



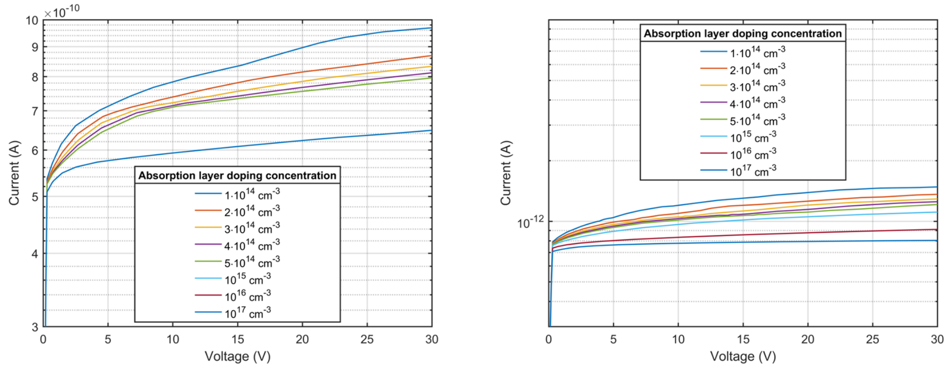
(d) QE as a function of wavelength.

Figure 4.10: Response of the $250x250$ µm^2 MSM device for different absorption layer thickness.

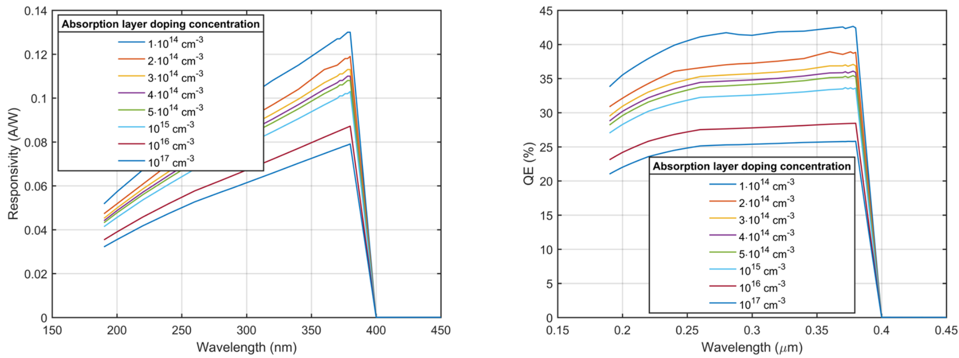
haviour. Therefore, the simulations for the doping concentration will be limited to the given doping concentration condition. Using the same simulation conditions as before, Figures 4.11 show the response of the MSM device for different doping concentrations.

As can be seen from Figure 4.11a, the highest photocurrent is at the lowest doping concentration, whereas the lowest dark current is given by the highest doping concentration. The latter is shown in Figure 4.11b. Figure 4.11c shows the responsivity of the device for different layer doping concentrations. Following the IV-response, the responsivity of the device increases for lower doping concentrations. At the wavelength 290 nm this is approximately 0.1 A/W for the lowest doping concentration. A similar increase can be expected for the quantum efficiency as shown in Figure 4.11d.

The simulation results show that a higher responsivity and quantum efficiency can be achieved. The efficiency increases from 25.31% to 41.43% for the doping concentrations $10^{14} - 10^{17} cm^{-3}$. However, the dark current also increases with lower doping concentration and is $> 1 pA$ for $10^{14} cm^{-3}$. Selecting an appropriate doping concentration is set by the trade-off between the responsivity, efficiency and the dark current. For this project,



(a) Photocurrent response as a function of voltage. (b) Dark current response as a function of voltage.



(c) Responsivity as a function of wavelength. (d) QE as a function of wavelength.

Figure 4.11: Characteristics of $250x250\ \mu m^2$ MSM device for different absorption layer doping concentrations.

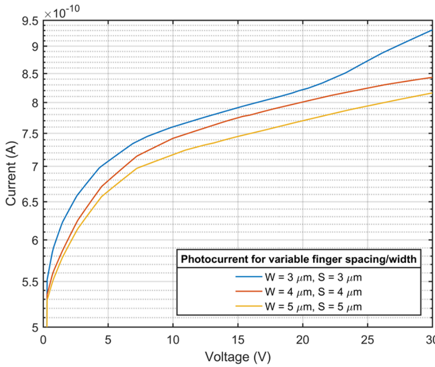
it is decided to take a middle way to have an increase in the responsivity efficiency while keeping the dark current as low as possible. Therefore the doping concentration which is used is $4\cdot10^{14}cm^{-3}$ to have low dark current $< 1pA$ and an efficiency at 34.72% compared to 27.71% in earlier simulations. Even lower doping could have been selected but due to uncertainty in the epitaxial layer processing, we avoided this.

4.2.2. ELECTRODES FINGER SIZES AND SPACING

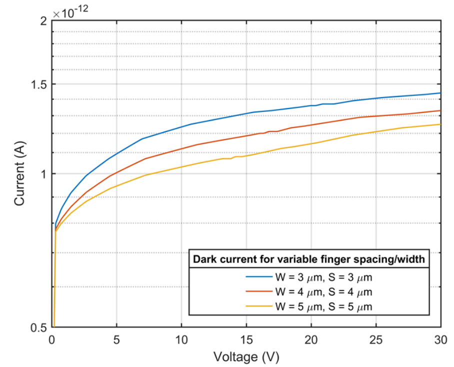
Aside from the materials, the width and spacing of the electrodes also have a significant effect on the performance of a MSM device. To investigate this, simulations have been performed according to the parameters listed in Table 4.3. The doping concentration used is $4\cdot10^{14}cm^{-3}$. The finger width and spacing simulated for are: 3 μm, 4 μm and 5 μm. Consider Figures 4.12 showing the responses of a MSM device for variable electrode finger/spacing. The width and spacing is kept equal.

As can be seen from Figures 4.12a and 4.12b, both photo- and dark- currents, increase for

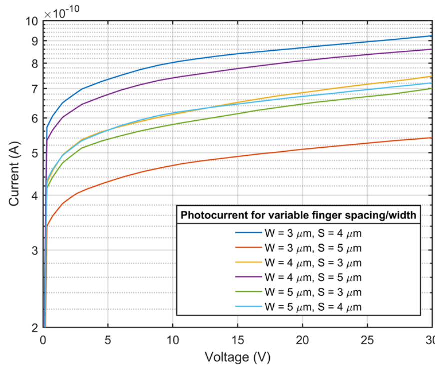
downsizing the width and spacing of the electrodes. Thus the current increases when the finger width and gap decrease simultaneously. This may be because the charge carrier collection efficiency improves [10]. If however the spacing is kept constant, then the dark current will increase for larger finger width while the photocurrent will decrease. The latter happens because of the fill factor where a larger area is covered by the electrodes, hence less absorption occurs. The responses are shown in Figures 4.12c and 4.12d.



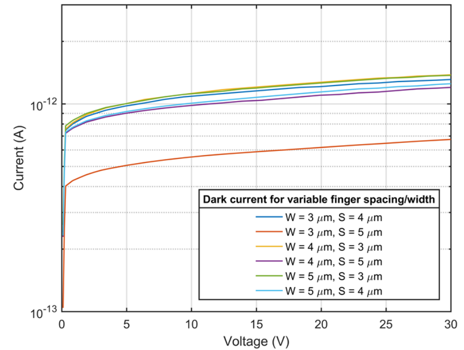
(a) Photocurrent response as a function of voltage (symmetrical).



(b) Dark current response as a function of voltage (symmetrical).



(c) Photocurrent response as a function of voltage (asymmetrical).



(d) Dark current response as a function of voltage (asymmetrical).

Figure 4.12: Characteristics of the 250x250 μm^2 MSM device for different electrode and spacing dimension.

4.3. Fabrication

After the MSM device designs were made and validated using simulations, the resulting structures were transferred to mask designs with various geometries based on performance and mask area. The mask design of the UV sensors consists of the three images: 1) Via, 2) Device, and 3) Interconnect. An example is shown in Figure 4.13.

The first mask is designed for etching via windows to connect to the buffer layer. This

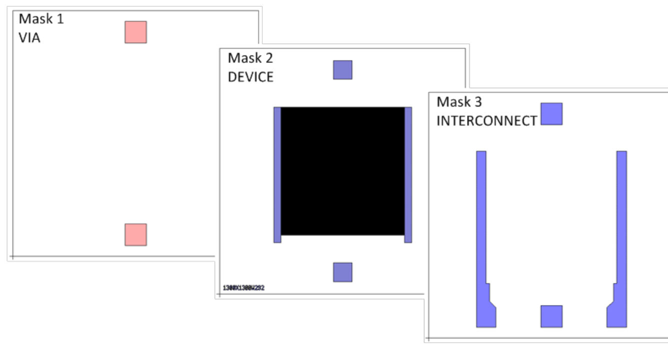


Figure 4.13: Example of the three-mask design.

method allows for the devices to work not only in MSM mode, but also in MS/single diode mode for the devices with vias. The masks contain various device types, including arrays and different versions of each device type. Each version has geometrical variations. Furthermore, the masks are divided in four quadrants with identical designs. This method allows for fabrication of the same devices in the same process but with different metals. Through this method, comparisons between the metals can be made to see which has the best performance. Consider Figure 4.14a illustrating the used commercial 4H-SiC substrate with two epitaxial layers.

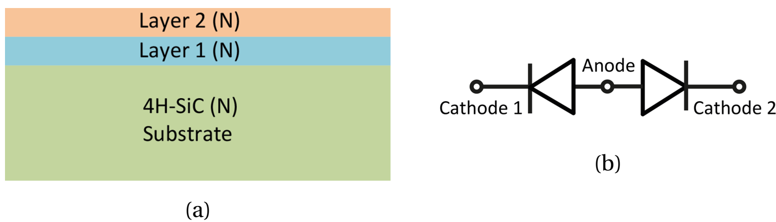


Figure 4.14: a) 4H-SiC substrate with epitaxial layers, and b) the back-to-back (MSM) diodes.

The first and second epitaxial layers are the buffer and absorption layers, respectively. The buffer layer also serves as a contact layer for operating several MSM devices in single diode modes by using the anode connection. This is illustrated in Figures 4.8 and 4.14b.

The substrates used for the fabrication of the MSM devices are purchased from a commercial vendor, Dongguan Tianyu Semiconductor Technology (TYSIC) located in China. Table 4.4 summarizes the specifications of two substrates.

As can be seen from Table 4.4, there is an uncertainty in the epitaxial growth where the doping and thickness of the layers can vary significantly. Therefore two substrates were purchased to account for the uncertainty. Fortunately, the thickness of the absorption layer is sufficiently thick unlike the thin layers used for the APD fabrication (see Chapter 5).

Table 4.4: Specifications of 4H-SiC substrates with epitaxial layers.

Substrate 1: n-type, $d = 345\ \mu m$, $Resistivity = 0.0216(\Omega \cdot cm)$		
Layer	**Thickness** (μm)	**Doping** (cm^{-3})
n-type	5	$(1-4) \cdot 10^{14}$
n-type	1	$1 \cdot 10^{19}$
n-type	0.5	$1 \cdot 10^{18}$
Substrate 2: n-type, $d = 356\ \mu m$, $Resistivity = 0.021(\Omega \cdot cm)$		
Layer	**Thickness** (μm)	**Doping** (cm^{-3})
n-type	5	$(2-6) \cdot 10^{14}$
n-type	1	$1 \cdot 10^{19}$
n-type	0.5	$1 \cdot 10^{18}$

4.3.1. Processing steps

Consider Figure 4.15 showing an overview of the MSM device fabrication.

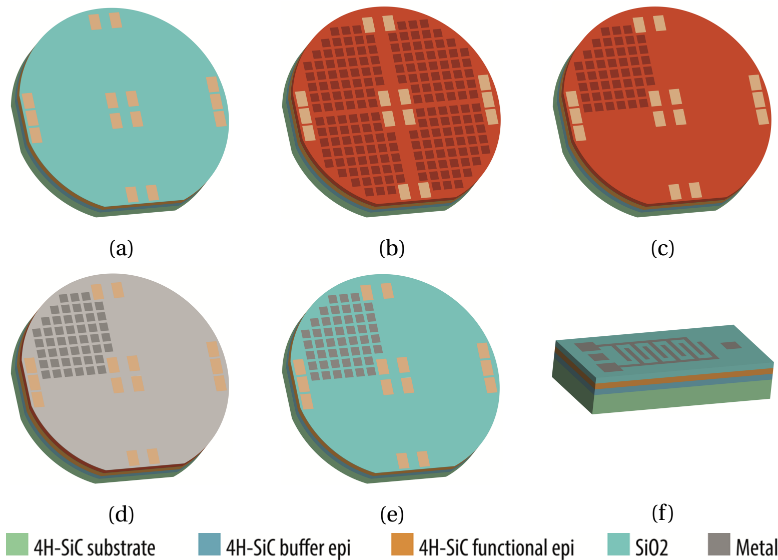


Figure 4.15: Overview of MSM device process flow. a) Definition of alignment markers in SiC, b) Contact openings to the ohmic layer, c) First region lift-off lithography, d) First region metal evaporation, e) First region lift-off process completion, and f) Resulting device structure before overlay metallization.

Before starting the fabrication steps first a sacrificial SiO_2 layer was grown using thermal oxidation and subsequently removed. The latter was done by immersing the substrates in a 1 : 7 Hydrofluoric acid (HF) solution followed by standard rinsing and drying. This step was done to remove any surface damaged/scratches. Subsequently, the fabrication

starts with defining alignment markers in the substrate. This work aims at comparing various device designs. Moreover, four different metals will be compared. Therefore, the substrates required extra contact aligner alignment markers to enable processing of four different regions on the substrate. The alignment markers are fabricated using standard lithography and ICP etching using a chlorine based recipe. It should be noted that the substrates are transparent thanks to their wide bandgap. Therefore, optical detection in machinery was achieved thanks to the deposition of an Al (1%Si) layer on the backside of the wafer. The backside is the carbon-side.

After etching the alignment marker in the substrate a standard cleaning step was done to remove the photoresist mask. Subsequently, the process for opening contacts to the buffer (anode) layer were done. This is illustrated in Figure 4.16. The first epitaxial layer is a standard layer used by the manufacturer. The second and third epitaxial layers were specified.

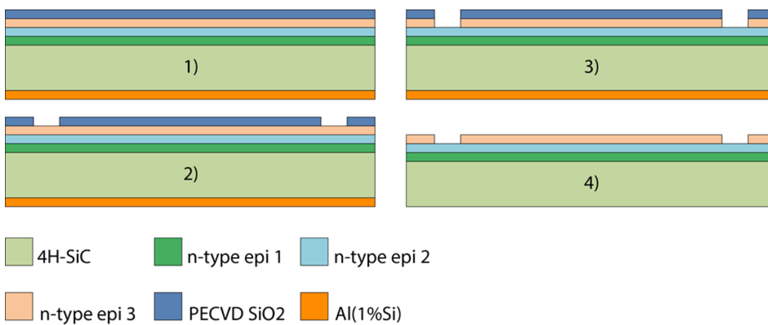


Figure 4.16: MSM device contact opening to buffer layer.

The first step is the deposition of PECVD SiO_2 hard mask. This is required because 5 μm of SiC needed etching. Here the thickness of the hard mask was based on the etch results described in Chapter 3. Subsequently, a standard lithography step was done followed by immersing the substrate in HF to etch the contact openings in the hard mask and expose the 4H-SiC top layer. First, the photoresist was removed then this was followed by the ICP etching using a chlorine based recipe, as shown by the third step in Figure 4.16. Before the removal of the SiO_2 hard mask at the front side, a height measurement of the etched contact opening was done to register the etch rate (see Chapter 3). After the removal of the SiO_2 using HF, this was repeated to find out what the selectivity is for the used recipe. Finally, the Al(1%Si) capping layer at the backside of the substrate was removed using an aluminium etchant. This was followed by a poly-Si etch step to remove silicon haze resulting from the 1%Si in the Al layer. An example of silicon haze, when not removed, can be seen in Figure 3.21 in Chapter 3.

As stated earlier, four metals are used in four regions of the wafer, namely: Mo (can also be used for Gr growth), Ta/Pt, Pd and Ni. Therefore, the steps for getting the metal structures are repeated four times as illustrated in Figures 4.15c-e. Only graphene growth has extra steps which will be discussed later on. Consider Figure 4.17 showing the second part of the fabrication. As shown in step one, before starting the IDT metallization

steps, first the antireflective coating is grown. The wafers are thermally oxidised (wet) at 1100 °C to grow a ~ 50 nm of SiO_2. The growth rate of the oxide can be found in Chapter 3.

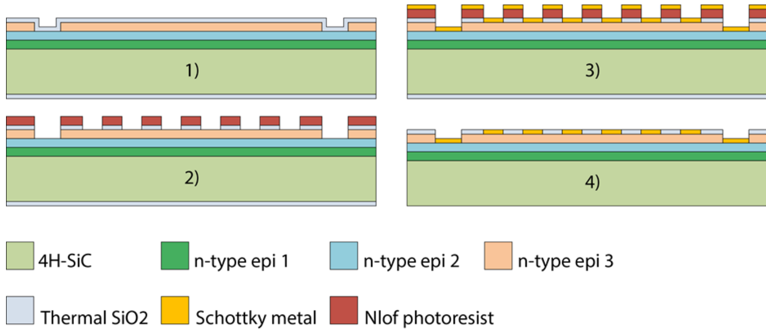


Figure 4.17: MSM device IDT Schottky metal definition.

Steps 2-4 are repeated for each metal. Here first a standard lithography step is done using negative photoresist to enable lift-off processing. After this, the required metal is deposited using sputtering or evaporation. Lastly, the photoresist is removed (lift-off) using N-methyl-2-pyrrolidon (NMP) at 70 ^{o}C followed by rinsing in DI water for 10 minutes and a drying step. Notice that the SiO_2 layer at the backside is removed. This happens after the many time of immersing the substrate in an HF solution.

Molybdenum was used to grow graphene, The layer was grown at a temperature of 50 ^{o}C and low power to prevent the photoresist from degassing/burning. The other metals all were deposited using evaporation at low temperature. Before the evaporation on SiC substrates first tests were performed on silicon substrates with and without an SiO_2 to characterize the metals for their sheet resistance and adhesion. The adhesion was tested using scotch-tape method. Here the the metals passed the test excellently without any delamination. This was repeated for the process wafers and similar results were obtained. Table 4.5 summarizes the conditions for the metal depositions.

Table 4.5: Schottky metal deposition conditions.

Metal	**Thickness** (nm)	**Sheet resistance** (R_s)	**Method**
Mo	50	7.45 ± 0.53	Sputtering
Ta/Pt	5/5	70.43 ± 1.76	Evaporation
Pd	10	130.4 ± 5.47	Evaporation
Ni	10	38.38 ± 2.09	Evaporation

The layers are this thin for research purposes to investigate the transmittance effect of very thin metal layers [11, 12]. Thanks to this, semi-transparent electrodes have been obtained and will be compared to CVD based graphene electrodes. It should be noted that thanks to the large number of fingers, the resistance of the contacts drops. The research on semi-transparency of electrodes is outside the scope of this thesis.

As for the risk of thin layers w.r.t. to measurement needles and wirebonding, there is a thick overlay (interconnect) layer. This is obtained in the last step of the fabrication. Consider Figure 4.18 showing the process steps for forming the interconnect of the devices.

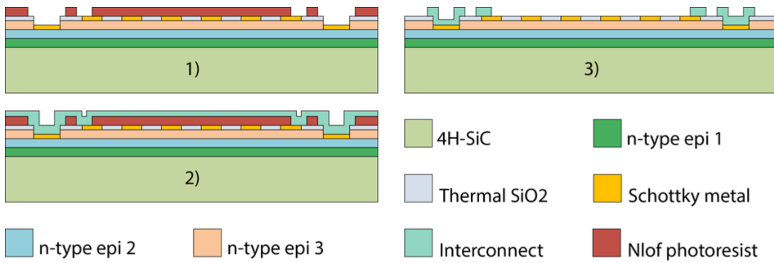


Figure 4.18: MSM device interconnect definition.

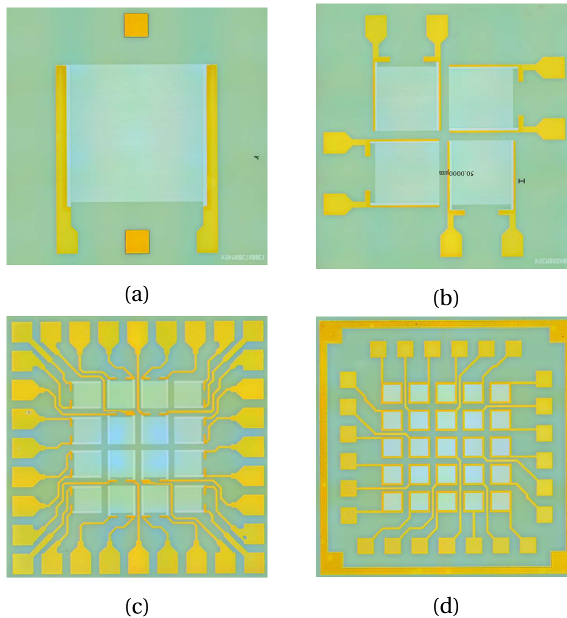


Figure 4.19: Examples of fabricated devices. a) Large MSM device with extra connections to the buffer layer, b) Medium MSM device in array of four, c) Small MSM device in array of 16, and d) Single Schottky diodes in array of 16.

As can be seen from the figure, the first step is a lithography step used to define the structures in the negative photoresist mask. This is then followed by metal evaporation of a Cr/Au layer. The layer thickness is 15/150 nm. The excess metal is then removed by lift-off by immersing the substrate in NMP at 70 ^oC. Finally, this is followed by rinsing in DI water for 10 minutes and a drying the substrates. Figures 4.19 show pictures of some of the fabricated devices.

4.4. RESULTS AND DISCUSSION

THE characterization of the fabricated MSM devices has been done on wafer level and for single dies. The first was useful to determine the dark current behaviour of the devices which in turn determines the minimum detectable signal. Moreover, the Schottky barrier height of the devices can be determined and compared to theoretical values. To do this, IV and IVT measurements have been carried out. As for the IVT measurements, these can be used to determine the operating characteristics at elevated temperatures but also to see what the dark current mechanisms could be. Furthermore, the IVT measurements were also done by forcing two known currents through the individual diodes of the MSM device to see the behaviour as a temperature sensor.

4.4.1. IV CHARACTERISTICS

The IV measurements at room temperature were carried out using a probestation connected to a B1500A Semiconductor Device Analyzer from Keysight. Since the devices have very low dark currents, the range of the measurement was set to 10 pA and a hold time of $2-3$ $seconds$. The analyser is set to sweep the biasing voltage from -20 V to 20 V while measuring the resulting dark current. It should be noted that the devices are at the limits of the measurement tool which makes it challenging to find the correct dark current levels for comparison. Therefore, some of the analysis is of the Schottky parameters is done for elevated temperatures where the measurement data is more reliable. The measurements at higher temperatures were done using the 4156C Precision Semiconductor Parameter Analyzer which has lower specifications compared to the B1500A Semiconductor Device Analyzer, hence the results at lower temperatures may be off to some degree.

The smallest obtained feature size is 2 μm with adequate spacing between the electrode fingers due to fabrication limitation.The limitation is the result of lift-off process which is less accurate. Nevertheless, the yield of the fabricated devices is high. As stated, IV measurements are challenging at lower temperatures where the small devices show dark currents in the range of femto amps, while at higher temperatures much higher dark currents can be observed, hence easier to measure. Therefore, for some of the analysis we used the data obtained at 200 °C. Figures 4.20 show the responses of a $1300x1260$ μm^2 MSM having W5S5 features, at different temperatures.

As can be seen, the devices show low dark currents even at higher temperatures, especially for palladium and nickel. It can be seen that even molybdenum has good response at low temperatures where the dark current is in the range of pico amps. For smaller devices, this will be even smaller, with currents of tens of femto amps. This shows that the devices can be used for very low light detection. Furthermore, at high temperatures the devices still exhibit good performance, including smaller ones. Figures 4.21 show the dark current response of the devices at 200 °C.

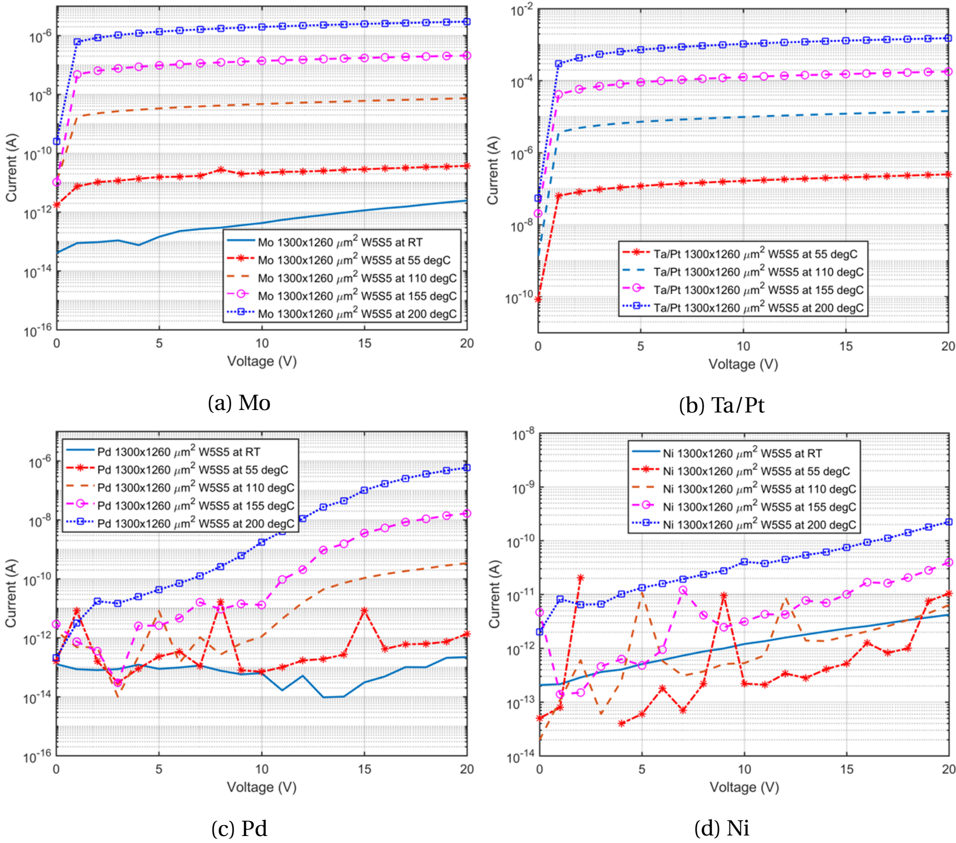
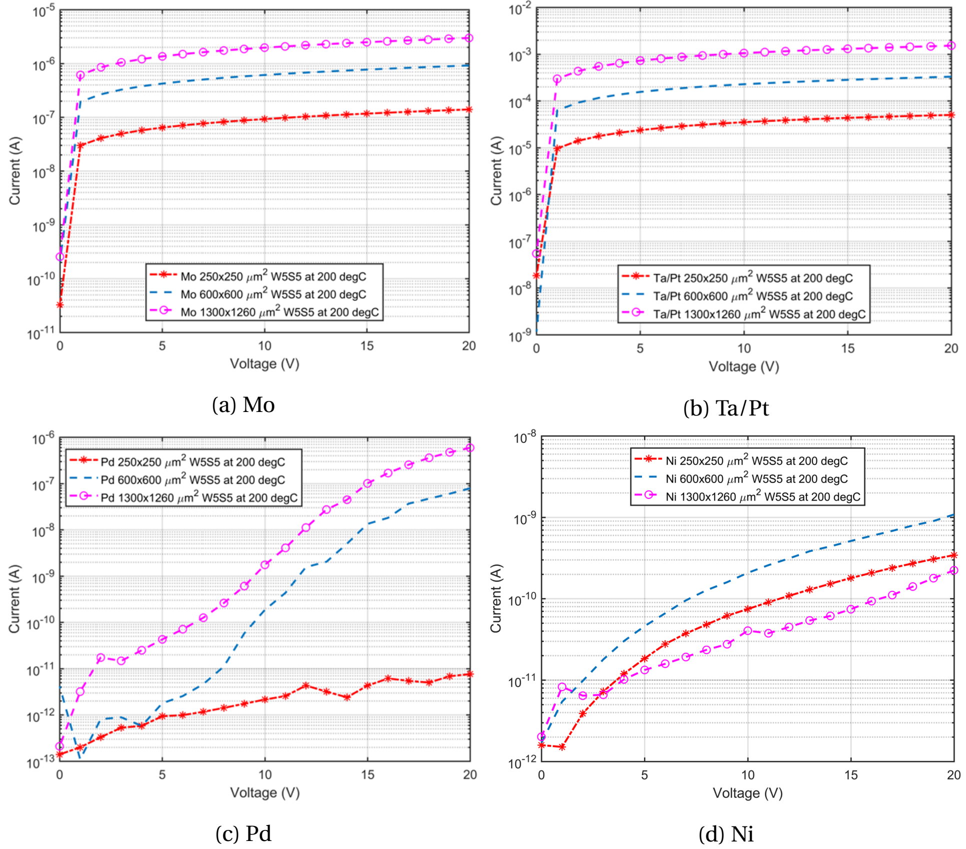


Figure 4.20: MSM device electrode geometries comparison for each metal at various temperatures.

As can be expected, the dark current increases for increasing sizes. Notice that for Ni device of 1300x1260 μm^2, the 600 μm device shows higher dark current compared to the smaller device. This is could be attributed to a possible measurement error or a defective device. One of the interests was to see the finger size effects on performance. Consider Figure 4.22a showing the dark current for Ni devices having different finger feature sizes. Again large devices are used since these are easier to measure.



(a) Mo

(b) Ta/Pt

(c) Pd

(d) Ni

Figure 4.21: Device size comparison for different metals.

Looking at Figure 4.22a, the dark current will be higher for decreasing feature sizes of the IDT fingers while keeping W/S ratio constant. Furthermore, asymmetrical designs ($W \neq S$) where $S > W$ will result in lower dark currents. These can be summarized by

$$(1)\ \frac{W}{S} = constant;\ W = S\downarrow;\ I_d\uparrow; \quad (2)\ \frac{W}{S}\downarrow;\ I_d\uparrow\ and \quad (3)\ W \neq S;\ W < S;\ I_d\downarrow \quad (4.19)$$

That being said, the finger size will also affect photocurrent generation. Figure 4.22b shows the performance of a large device ($1300x1260\ \mu m^2$) with different metals. It shows that nickel has the lowest dark current with a value of $\sim 223 pA$ at 200 °C and $20V$. This indicates that the nickel device has the highest Schottky barrier compared to devices with the other metals. On the other hand, Ta/Pt has the worst performance where the dark current is considerably higher at a value of $\sim 1.52\ mA$ at 200 °C and $20V$ which is 7 orders of magnitude larger. The values associated with molybdenum and palladium are $2.79\ \mu A$ and $591\ nA$, respectively. Although platinum has a high metal workfunction

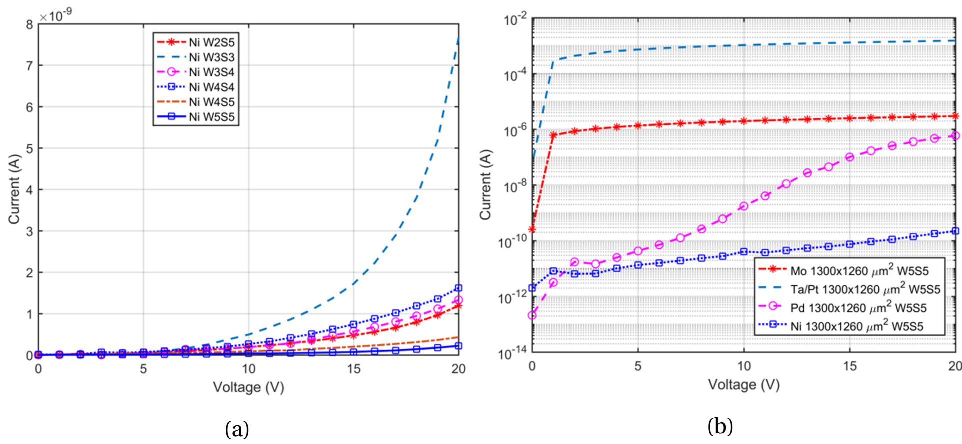


Figure 4.22: a) Finger size comparison of nickel MSM devices with different IDT finger sizes at 200 °C for 1300x1260$\mu\ m^2$ devices, and b) 1300x1260 μm^2 W5S5 MSM devices using different metals at 200 °C.

of 5.65 eV, the tantalum adhesion layer has a lower metal workfunction at a value of 4.22 eV, hence a lower Schottky barrier height will be the result at around 0.6 eV. Ta was first deposited followed by Pt. The reason for using Ta as an adhesion layer is because the Pt comes off when doing the Scotch tape test. It was assumed that due to metal stacking [13], the overall Schottky barrier would increase sufficiently high. The observed metal workfunction is 0.8 eV which is higher than what would be expected for Ta/4H-SiC but is still lacking. Additionally, also the processing has an influence on the SBH. On the other hand, molybdenum has a higher Schottky barrier than expected. Therefore, a more closer analysis should be done to determine the actual Schottky barrier heights for all used metals.

4.4.2. SCHOTTKY BARRIER HEIGHT

The large devices have an added feature to enable single diode mode instead of the MSM back-to-back diode functionality. This also enables using the MSM device as a two parallel diode device. Consider Figure 4.23 showing the device performance in single diode mode and normal MSM device operation using different metals at 200 °C.
As can be seen, the dark current responses for either single and normal MSM (double) modes are similar. Therefore, the analysis for obtaining the Schottky parameters will be carried out using single mode device operation. This allows for using forward bias measurement results whereas normal MSM devices are always in reverse bias. The devices used for this are the 1300x1260 μm^2 with feature size W5S5 for all used metals.

To determine the transport mechanisms of Schottky diodes one needs to characterize the diodes for their electrical performance where the Schottky barrier height and ideality factor are of interest [14]. These values are obtained by performing forward. There are several methods for extracting approximate values of the barrier height, which include the standard IV method [15], Cheung's method [16] and Norde method [17]. The first method assumes ideal diode characteristics while the other methods are more suited

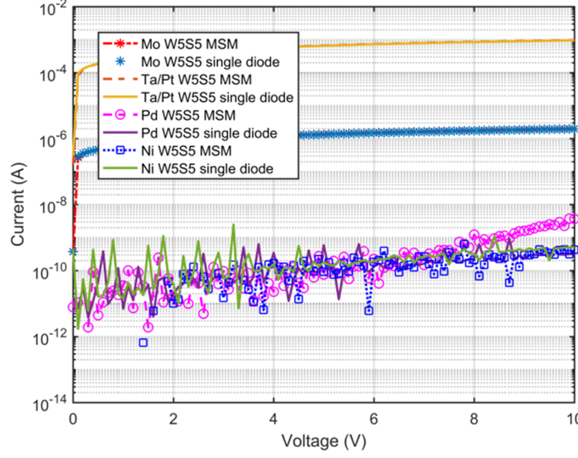


Figure 4.23: Dark current response comparison of single and double diode mode MSM .

for practical diodes. In this work we will use the standard IV and Norde methods. The calculation of these parameters is based on thermionic emission theory following the current transport equation (4.20).

$$I = I_s\left[exp\left(\frac{qV}{nk_BT}\right) - 1\right] \tag{4.20}$$

Where I_s is the saturation current, q is the electronic charge, V is the applied voltage, n is the ideality factor, k_B is the Boltzmann constant and T is the absolute temperature. The saturation current is given by (4.21)

$$I_s = AA^{**}T^2 exp\left(-\frac{q\Phi_B}{k_BT}\right) \tag{4.21}$$

Where A is the device area, A^{**} is the Richardson constant and Φ_B is the Schottky barrier height. The Richardson constant is given by (4.22)

$$A^{**} = \frac{4\pi m^* q k_B^2}{h^3} \tag{4.22}$$

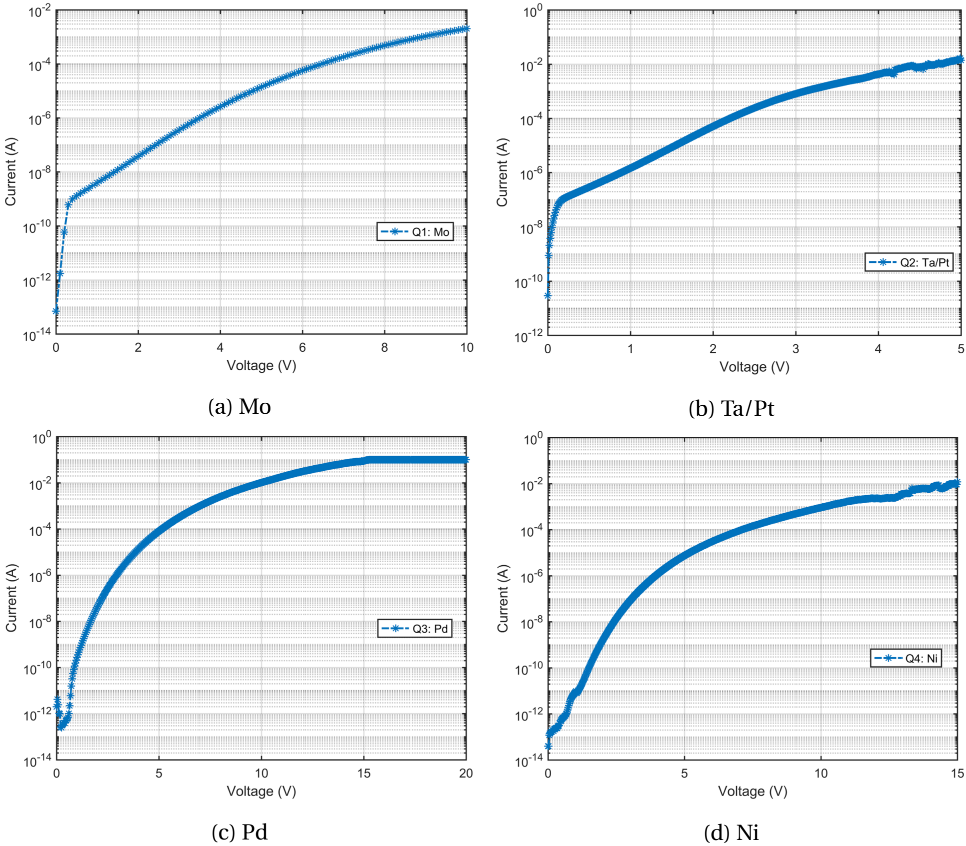
Where m^* is the electron effective mass. Here A^{**} only depends on m^*. The theoretical value for $4H-SiC$ is then 146 A/cm^2K^2 [18]. The ideality factor is given by (4.23)

$$n = \frac{q}{k_BT}\frac{dV}{d(lnJ)} = \left[1 + \frac{d\Delta\phi}{dV} + \frac{k_BT}{q}\frac{d(ln(AA^{**}))}{dV}\right]^{-1} \tag{4.23}$$

Rearranging equation (4.21) as (4.24) gives the Schottky barrier height

$$\phi_B = \frac{k_BT}{q} ln\left(\frac{AA^{**}T^2}{I_s}\right) \tag{4.24}$$

By taking the natural logarithm of the current and plotting it against the applied voltage, the saturation current can be obtained. This is done by fitting a linear line over the linear region of the curve, for at least five orders of magnitude, and reading the value at the y-intercept. Furthermore, the ideality factor can be calculated from the slope which is given by q/nkT. Figures 4.24 show the IV-graphs of the devices for all four materials.



(a) Mo (b) Ta/Pt

(c) Pd (d) Ni

Figure 4.24: Conventional method for obtaining Schottky parameters.

Using the above equations the Schottky barrier heights and ideality factor values were extracted and added to Table 4.6. The ideality factors are high which means that the devices need improvement. This can be done for instance by annealing the devices at higher temperatures to improve the metal-semiconductor interface [19]. Other alternatives may be the surface passivation prior to metallization which potentially can result in also lower leakage currents [20]. An example of surface passivation can be done by inserting a dielectric such as aluminium oxide to passivate surface defects, but also preventing diffusion of metals [21].

Table 4.6: Conventional method.

Mo	Ta/Pt	Pd	Ni
$\phi_B = 0.93\ eV$ $n = 15.76$	$\phi_B = 0.74\ eV$ $n = 11.37$	$\phi_B = 1.06\ eV$ $n = 6.23$	$\phi_B = 1.11\ eV$ $n = 7.56$

From literature it shows that the Schottky barrier heights may be off [6]. Averine et al. proposed a modified version of the conventional method to use under forward and reverse bias [15]. To do this, equation (4.20) can be rearranged to (4.25) and simplifies for $V > 0.5\ V$ to (4.26)

$$\frac{Iexp(qV/k_BT)}{exp(qV/k_BT)-1} = I_s exp(qV/nk_BT) \tag{4.25}$$

$$Iexp(qV/k_BT) = I_s exp(qV/nk_BT) \rightarrow ln[Iexp(qV/k_BT)] = ln(I_s) + qV/nk_BT \tag{4.26}$$

The natural logarithm of equation (4.26) is then plotted against the voltage. The plot should give a straight line for values $> 3V_{th}$ where the y-intercept is $ln(I_s)$. The ideality factor can be obtained from (4.27)

$$n = \frac{q}{k_BT}\frac{dV}{dln\left(\frac{Iexp(qV/k_BT)}{exp(qV/k_BT)-1}\right)} \tag{4.27}$$

Or from the slope of the line for values $> 0.5\ V$. This is related by (4.28)

$$slope = \frac{1}{n \cdot V_{th}} \tag{4.28}$$

Table 4.7 lists the values under forward bias.

Table 4.7: Averine method.

Mo	Ta/Pt	Pd	Ni
$\phi_B = 0.94\ eV$ $n = 0.96$	$\phi_B = 0.75\ eV$ $n = 0.97$	$\phi_B = 1.10\ eV$ $n = 0.95$	$\phi_B = 1.11\ eV$ $n = 0.93$

As Table 4.7 shows, The values for the barrier height are close to those obtained form the standard method. However, this method gives ideality factors lower than unity which is by definition not possible.

Norde [17] has proposed an alternative method to extract the barrier height. The model is used in the case a diode has a high series resistance due to the base material. Moreover, in case the device has a ‘less’ ohmic back contact, the current transport will be affected. The latter is true for the measured devices. The barrier height can be extracted using equation (4.29)

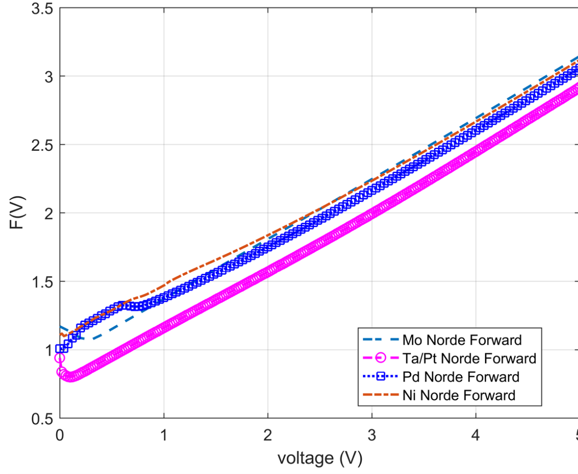


Figure 4.25: Norde method for extracting the Schottky barrier height.

$$F(V) = \frac{V}{2} - \frac{1}{\beta} ln\left(\frac{I}{AA^{**}T^2}\right) \tag{4.29}$$

By plotting this function against the voltage and assuming $V_D > k_B T/q$, the barrier height can be extracted from the minima of the curve. The barrier height is expressed as (4.30)

$$\phi_B = F(V_o) + \frac{V_o}{2} - \frac{k_B T}{q} \tag{4.30}$$

Where V_o is the voltage at which the minima occur. A slight modification to the equations for double Schottky contact devices is given by [17] as (4.31), (4.32) and (4.33).

$$F(V_o) = \frac{\phi_1 + \phi_2}{2} + \frac{k_B T}{q} ln(2) \tag{4.31}$$

$$\phi_1 = F(V_o) + \frac{V_o}{2} - \frac{k_B T}{q} ln(2) \tag{4.32}$$

$$\phi_2 = F(V_o) - \frac{V_o}{2} - \frac{k_B T}{q} ln(2) \tag{4.33}$$

Since the only interest is the front contact, the equations can be used as they give essentially the same result. Figure 4.25 shows the $F(V)$ $vs.$ V plots of the different devices in forward bias. Table 4.8 summarizes the results of the methods. The values for the Schottky barrier heights obtained by Averine and Norde methods are in good agreement. The metal workfunction is calculated assuming ideal cases.

Table 4.8: Norde method.

Mo	Ta/Pt	Pd	Ni
$\phi_B = 1.07\ eV$	$\phi_B = 0.8\ eV$	$\phi_B = 1.01\ eV$	$\phi_B = 1.10\ eV$

4.4.3. UV CHARACTERIZATION

As was discussed in the previous section, the dark current of the devices at room temperature is within fA (Pd and Ni) while at higher temperatures this could reach nA or even μA levels. The response under UV illumination was done for the large Pd and Ni MSM devices since these had good characteristics as compared to the Ta/Pt with a very large dark current. The Mo devices were not measured. For the measurements, we used a setup build around a deuterium lamp and a monochromator and measured at a wavelength range of 210-410 nm. The bias voltage is 20V. Figure 4.26a shows the setup illustration.

The light source power density was measured using a commercial GaP photodiode with a known responsivity as shown in Figure 4.26c. The resulting current was converted and amplified using a transimpedance amplifier circuit based on the OPA602 amplifier with a feedback resistor. This is illustrated in Figure 4.26b.

The dark currents of the Pd and Ni devices at 20V are 0.2pA and 4pA, respectively. The photocurrents at the same bias are both approximately 1nA at an optical power of approximately $4.5 \cdot 10^{-7}\ W/cm^2$ at 270nm. This corresponds to a photo-to-dark-current ratio (PDCR) of $9.1 \cdot 10^4$ and 249 for the Pd and Ni devices, respectively. Consider Figures 4.27 showing responses of the MSM devices at room temperature.

As can be seen, the responses drop drastically for wavelengths above 300 nm and show very low response beyond 400 nm. Hence a large UV to visible rejection is obtained. Here Ni shows the highest responsivity at 0.13 A/W for the large devices. Additionally, smaller devices (600 μm) were also measured and showed good responsivities with the highest at 0.03 A/W for the Pd devices. Therefore there is very little difference between the two metals in terms of UV response. Furthermore, there is a sharp drop in response up to 300 nm which can be attributed to the antireflective coating.

4.4.4. PTAT MSM SENSOR

Applications such as oil and gas exploration, geothermal energy sources, health monitoring in aircraft engines, and industrial processes require sensors and electronics to operate in extremely high temperatures, typically beyond 500 °C where Si technology is not adequate [22, 23]. Furthermore, such sensors require a readout system which is also exposed to harsh conditions. This means that the electronics need to be packaged such that the effect of temperature will be minimum, which adds to the complexity. Alternatives are sensors based on other materials such as WBG semiconductors. The sensors can be combined with electronics that are capable of withstanding high temperatures and other harsh environments. This can be achieved using SiC semiconductor as the base material for both aspects where the ultimate goal is monolithic integration.

This thesis work investigates two temperature sensor types where the second one is dis-

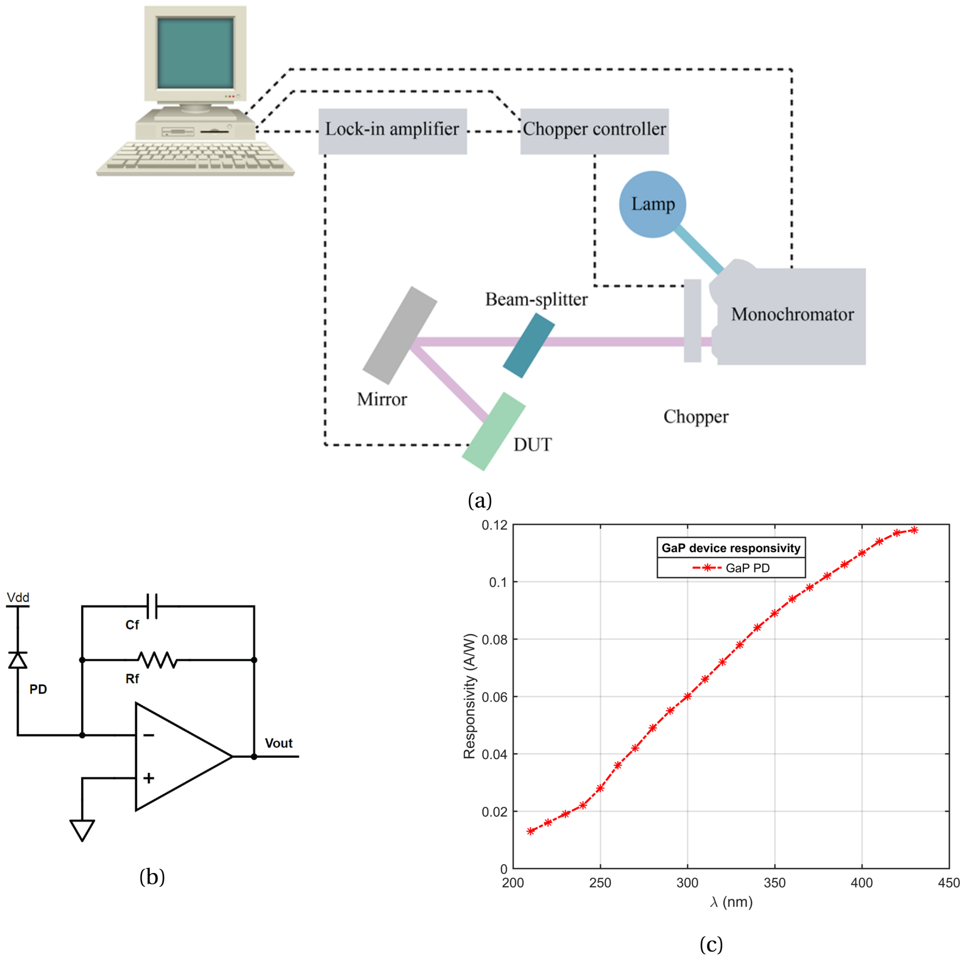
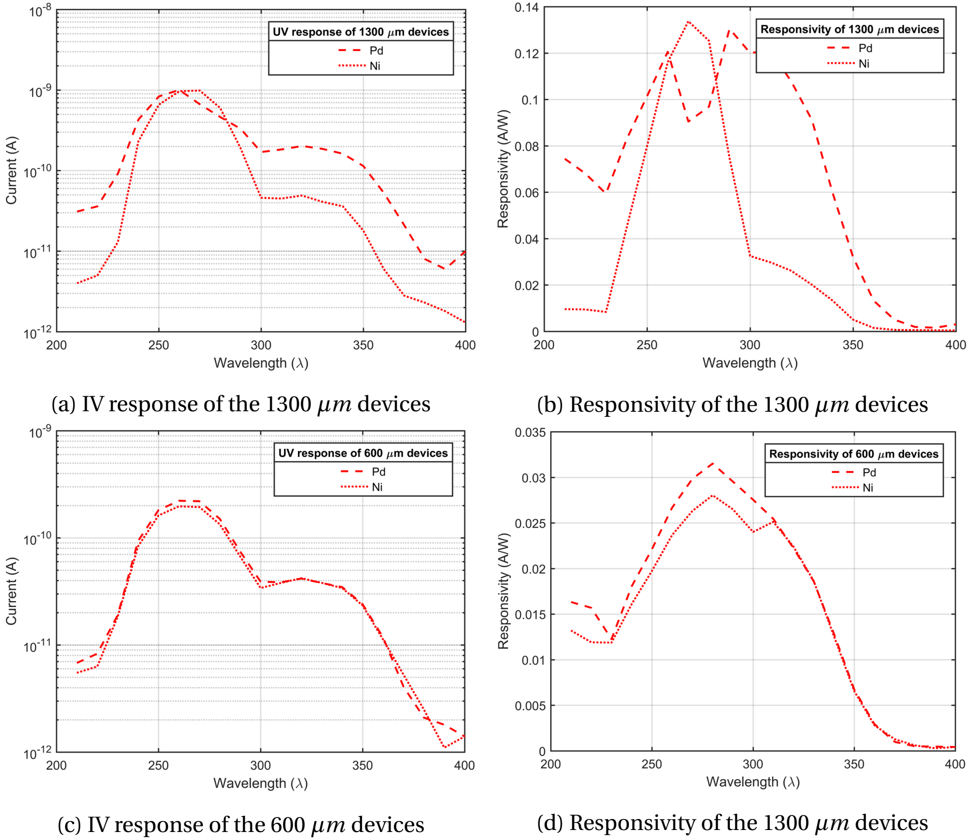


Figure 4.26: a) Setup illustration, TIA circuit used for the measurements, and c) Responsivity of the GaP device.

cussed in Chapter 6. The MSM device can be used for multi-sensing applications where temperature sensing is an additional option. The device can be used in its parallel configuration through the extra connection to the highly doped buffer layer. Through this, the device acts as a proportional to absolute temperature (PTAT) device [24]. The temperature range for which it was characterized is 25-200 °C. Consider equation (4.34) for the voltage drop across a diode in forward conduction.

$$V_d = n\frac{kT}{q} ln\left(\frac{I_d}{I_s}\right) + R_S I_d \tag{4.34}$$

Where kT/q is the thermal voltage, given by the Boltzmann's constant, temperature, and



(a) IV response of the 1300 μm devices

(b) Responsivity of the 1300 μm devices

(c) IV response of the 600 μm devices

(d) Responsivity of the 1300 μm devices

Figure 4.27: IV response and responsivity of devices with various metals and sizes.

electron charge. I_s is the saturation current, R_S is the parasitic series resistance, and n is the ideality factor. By biasing the two back to back diodes with two currents, I_{d1} and I_{d2}, there will be a voltage drop across each of the diodes. By taking the difference of these two voltage drops, a temperature-dependent voltage will be obtained. This is given by (4.35).

$$V_{d2} - V_{d1} = n\frac{kT}{q} ln\left(\frac{I_{d2}}{I_{d1}}\right) + R_S(I_{d2} - I_{d1}) \tag{4.35}$$

Thus there is no dependence on the saturation current which has a nonlinear temperature dependence. The output will be linearly dependent on temperature if the product $R_S(I_{d2} - I_{d1})$ is negligible and n is constant. To improve this, the fabricated devices should be optimized. The sensitivity of the device is controllable by increasing the current ratio R between the two currents, I_{d1} and I_{d2}. However, the series resistance starts to play an important role when the ratio is too large. Here we did only one measurement on a Mo device which shows temperature dependence. Figure 4.28 shows this.

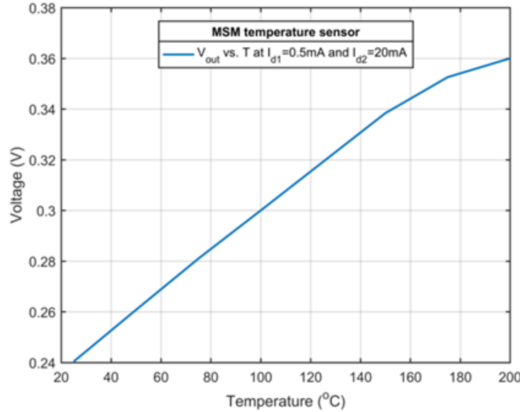


Figure 4.28: Temperature behaviour of the MSM working as a PTAT.

The device shows good temperature dependence. Future work should include optimization of the device to obtain a more linear dependence over a wider temperature range.

4.5. CHAPTER SUMMARY

In this chapter, MSM Schottky sensors for multi-sensing applications were fabricated using 4H-SiC substrates and various metals. The metals used are Mo, Ta/Pt, Pd, and Ni, where the last two showed the best dark current performance in the range of pA. The devices showed reasonable dark currents at 200 °C where Ni electrodes gave a dark current of ~ 223 pA at 20V bias. Although Pt has a large metal workfunction, the dark current reached ~ 1.52 mA at 200 °C for the same bias. The tantalum adhesion layer has a lower metal workfunction at a value of 4.22 eV, hence a lower Schottky barrier height resulted, at around 0.6 eV. The reason for using Ta as an adhesion layer is because the Pt comes off when doing the Scotch tape test. It was assumed that due to metal stacking, the overall Schottky barrier would increase sufficiently high. The observed metal workfunction is ~ 0.8 eV which is higher than what would be expected for Ta/4H-SiC but is still lacking. Additionally, also the processing has an influence on the SBH. The ideality factors calculated using the standard IV method showed high values which means that the devices need improvement. This can be done for instance by annealing the devices at higher temperatures to improve the metal-semiconductor interface. Other alternatives may be the surface passivation prior to metallization which potentially can result in also lower leakage currents. An example of surface passivation can be done by inserting a dielectric such as aluminium oxide to passivate surface defects, but also preventing diffusion of metals. The UV responses were measured for the Pd and Ni-based devices at a bias of 20V. Both devices showed similar responsivities at 270 nm whereas the PDCR is better for the Pd device. At higher temperatures Ni devices should have the preference since its dark current is considerably lower as compared to the Pd devices. Although not characterized for its UV behaviour, surprisingly the Mo metal, showed a Schottky barrier of about 1.2 eV which means that it can be used for optical detection. This metal is useful

for high temperature applications and other harsh environments because it is a refractory metal. This allows the device to be used for high temperature applications where the device is used as a PTAT temperature sensor. The W5S5 devices with Mo electrodes were tested up to 200 °C and showed good temperature behaviour. Therefore, this work demonstrates the potential of the devices to be used as a multi-carrier device capable of measuring not only optical signals, but also applicable for temperature measurements targeted at harsh environments. Future work should include the improvement of the device fabrication to improve the ideality factor.

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5

4H-SiC AVALANCHE PHOTODIODE

Avalanche photodiodes (APDs) are important in fields requiring ultra-low light or even single-photon detection. 4H-SiC APDs are advantageous for detecting weak ultraviolet signals thanks to their small size, low dark current, high multiplication gain, and high quantum efficiency. Such detectors can be used in a wide range of applications, e.g. corona discharge, flame detection, missile plume detection, UV astronomy, UV LIDAR, and biological and chemical detection. In this chapter, we discuss the design, fabrication, and characterization of a 4H-SiC APD. The devices are based on epitaxial technology to ease the fabrication constraints w.r.t. implantation, activation and etching. This allows for device fabrication in our own cleanroom facilities.

5.1. Introduction

Many key applications require low UV light detection, e.g. corona discharge, flame detection, missile plume detection, UV astronomy, UV LIDAR, environmental monitoring, and biological and chemical detection [1–3]. Although Si photodetector technology can be used for such applications, it still requires filtering for the UV range [3]. As for other wide bandgap materials, e.g. group III-nitrides, these are promising but still lack in technology maturity such as the defects density. Hence SiC APDs exhibit better performance in terms of dark current, gain, and reliability [3]. Therefore, this study focuses on 4H-SiC APDs. To understand the subject, we first introduce some of the state of the art devices, then briefly the device operation principle. After this, we discuss the design, fabrication, and characterization of the devices. The APDs can be used as single photon avalanche photodiodes (SPAD). However, in this work we will limit the characterization to IV measurements, hence no single-photon measurements are done.

5.1.1. State of The Art

Avalanche photodetectors are an adaptation of the p-i-n based diodes. The detectors are usually fabricated using stacking of epitaxial layers in-situ doped. This allows fabrication of devices with deep multiplication regions whereas conventional doping cannot be used [4–7]. Researchers have identified various methods for designing and optimization of APDs.

Xin X. et al. presented a 50 µm 4H-SiC p-n^--n^+-SPAD operating at 280 nm with a bias of 117 V. The p-region is for ohmic contact, n^-- region for absorption and multiplication while the bottom n^+-region is used for the electrical field termination. The detector based on a bevelled mesa featuring off-mesa bonding pad and showed a dark current as low as 17 fA, 49 fA and 147 fA at 50%, 90% and 95% of breakdown bias, respectively. Its quantum efficiency is 28% and 32% at 280 nm and 270 nm, respectively, while its UV to visible rejection ratio exceeds 1400. Dark count rate was measured to be 14 kHz and 27 kHz at single photon detection efficiencies of 1.9% and 2.6%, respectively [4]. This device is an improved version of an earlier design not featuring a bevelled mesa structure. The structure was based on p^+-p-n stacking sequence showing breakdown at 78 V and a dark count rate of 650 kHz [6]. Hu J. et al. further improved the design showing dark currents of 20 fA and 57 fA at 80 V and 90% of breakdown voltage, respectively. Its quantum efficiency was much higher reaching 43% at 270 nm and a UV to visible rejection ratio exceeding 6100. At the reverse bias of 116.8 V its single-photon detection efficiency increased to 2.83% [7].

Vert A. et al. fabricated a n^+-n^--n-n^--$p+$-SPAD featuring separate absorption ($n-$) and multiplication ($n-$) regions separated by a n-layer. This approach was adopted to terminate the electric field in the n-layer without extending to the top absorbing layer. Hence, generated carriers travel by diffusion to the multiplication region. The dark current was estimated at 400 fA (0.75 nA/cm^2) for a device diameter at 260 µm and biasing at 375V. Its quantum efficiency was 13% while having a gain of 1000 and having dark count probability of $4x10^{-4}$ at an efficiency of 9.4% [5].

Cai X. et al. proposed a design with separated regions to reduce both power dissipation and complexity of circuit design. Traditionally, lowering the voltage can be done by re-

ducing the thickness of the absorption layer. However, since SiC is not as efficient as traditional semiconductors, a different approach was taken. Here a separated-absorption-charge-multiplication (SACM) structure was adopted. This allows for a wide absorption layer while the electrical field can be confined with a thin multiplication region. Avalanche operation was achieved already at 67 V showing a high gain of 10^6. Its quantum efficiency was 80% at 270 nm while its UV to visible rejection ratio reached 10000. For reverse biasing of 50 V, the dark current level remained at 0.1 pA (29 pA/cm^2) [8]. Further investigations of Cai X. et al. showed optimization of SPAD detectors through variation of multiplication and absorption layers [9, 10]. Thicker layers lead to lower primary dark current, larger positive temperature coefficient and higher external quantum efficiency [10]. This is thanks to the suppression of dark current count resulting from tunnelling effects. Kou J. et al. proposed optimization strategies for SACM devices through layer thickness and doping concentration optimization [9]. The doping of the absorption layer modulates the photo-generated carrier transport and affects the responsivity. Therefore this should be kept at intrinsic level of 10^{15} cm^{-3}. As for the depletion region concentration, this should be 10^{18} cm^{-3} to properly regulate the electric field distribution. Thanks to this the depletion region can be completely terminated by the charge control layer. To improve the dark current behaviour, the doping concentration of the multiplication layer should also be kept close to intrinsic level. Since the mesa angle has a significant effect , it should be in the range of $10-20$ deg for optimal edge breakdown suppression [9].

Moreover, the angle of the bevel structure has a major effect of the dark current [11]. Chong E. et al. studied this effect and concluded that a small-slope bevelled mesa results in a more uniform dark current level in the linear region, regardless of the active area. The dark count was shown to be orders of magnitude lower for smaller slope angle [11]. Bevelled mesa based detectors have one common drawback. The dark current is proportional to the area thus large-area detection is not feasible. Zhou X. et al. fabricated a large-area detector for very low light detection while maintaining a low dark current. The bevelled mesa used for edge breakdown suppression is fabricated using photoresist reflow technique [12]. However, if the reflow is performed at a fixed temperature, this will result in sawtooth-like patterns on the mesa side-walls, causing larger dark currents. This may be the result of non-uniform thermal field in different surface tension. The work of Zhou X. et al. showed a low dark current of 1 pA(0.2 nA/cm^2) with a high external quantum efficiency of 81.5% at 274 nm. This was achieved by using a variable-temperature photoresist reflow technique where the temperature was ramped up from 90 to 145 $degC$ using 5 $degC/minute$ [12].

APD detectors are like any other device susceptible to temperature effects. However, Zhou D. et al. showed a design to operate at elevated temperature with good results. The presented device is a 4H-SiC SPAD consisting of n^+-n-n^--p^+-layers. The detector was characterized for room temperature and 150 $degC$. It showed quantum efficiencies of 53.4% and 63.3% at 290 nm and 295 nm, respectively. Its single photon efficiency drops only slightly at elevated temperature from 6.17% to 6%. However, its dark count rate increases significantly from 22 to 80 kHz [13].

5.2. BACKGROUND

THE pn-junction photodiode is one of the first developed junction semiconductor devices. It is a simple structure consisting of a p-type layer on top of a n-type layer or substrate. By bringing the two layer types together, a potential barrier will exist under equilibrium and there will be no net current flow through the diode. Figure 5.1 shows an illustration of the device along with its electrical symbol.

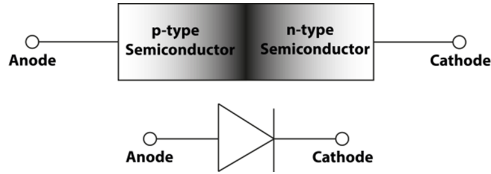

Figure 5.1: pn-junction diode illustration and its electrical symbol.

The device has a response to incident photons in the form of free charge carriers generation. Each incident photon generates an e-h pair which are separated by an electrical field which in turn is generated by reverse biasing the device. Here the electrons at the p-side move through the depletion region towards the n-type side while the holes at the n-type side move towards the p-type side for collection, hence a small electric current will flow.

However, like any technology there are drawbacks. The first drawback of the pn-junction is the flow of a large dark current, hence restricting low light level detection. The depletion region of the device is essentially a capacitor that is too large due to the small width of the SCR. This results in limiting fast response detection and high frequency modulation. Another disadvantage is having a low QE at long wavelengths, although this is not an issue in this work for the application of UV sensing.

5.2.1. THE PIN- JUNCTION

To overcome some of the limitations associated with the pn-junction, an intrinsic layer is added between the p- and n-type layers as illustrated in Figure 5.2.

The depletion region is enhanced by the width of the intrinsic layer. First, this can be tailored to reduce the capacitance of the junction for the same optical sensing area, enabling faster response and higher frequency modulation with bandwidths typically in the range of 10 MHz. The capacitance is then typically in the order of pF. This is because the capacitance of the device becomes bias independent as shown in equation (5.1).

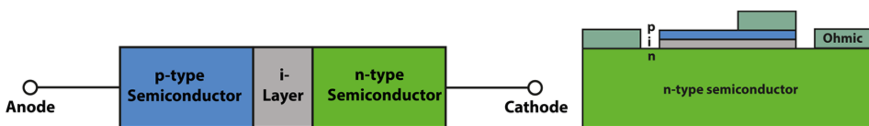

Figure 5.2: pin-junction diode illustrations.

$$C = \frac{\epsilon_0 \epsilon_r A}{W} \tag{5.1}$$

Thanks to low doping of the layer, the electrical field becomes uniform which also presents further diffusion of charge carriers and enables lower noise [14]. Moreover, the SCR becomes nearly independent of the applied bias which is beneficial for a stable operation and an increased breakdown voltage Vbr. The QE of the device is also enhanced through the design of the intrinsic layer. Here the photons are mostly absorbed in the intrinsic layer. It should be noted that even though more e-h pairs can be generated for a larger W, this will also result in a slower response as shown by equation (5.2).

$$T_{drift} = \frac{W}{V_d} \tag{5.2}$$

The reason for this is due to the transit time of the photo-generated charge carriers which will reduce the response time of the photodiode. This results in a trade-off between speed and responsivity of the device due to reduced photon absorption in the case of smaller W.

For good ohmic contact to the device, an additional n+ and p+ layer can be used as a connection to the metals for low contact resistances [14]. This property also usually results in a higher detection compared to Schottky photodiodes mainly due to their lower dark current (related to noise) [15]. Next to this, depending on the specific design, responsivity can be significantly increased at reverse voltages in Schottky and p-n photodetectors [15]. However, the increased bias also reduces the UV to visible ratio.

This type of device has been used in various research and showed good performance. 6H-SiC UV pin-junction photodetectors are already commercially available [16]. Here the n^+ layer always has a high doping concentration, typically $> 10^{19}\ cm^{-3}$. An example of such devices showed an extremely low reverse current, and a peak responsivity of $150-175\ mA/W$ range at $270\ nm$. This corresponded to a $70-85$ % quantum efficiency. Another work showed a 4H-SiC based pin PD was designed to have a responsivity of $0.13\ A/W$ at a wavelength of $270\ nm$, an EQE of ~ 61 % and a UV-to-visible ratio exceeding 10^3 for the wavelength of $270\ nm$ and $380\ nm$. The PD's usually require passivation which is done by coating with a SiO_2 layer for passivation and anti-reflection. The SiO_2 layer has an absorption at $\lambda < 200\ nm$ [17, 18]. However, surface recombination plays an important role, especially for far UV photodiodes [17]. Thus the control of the semiconductor to SiO_2 interface is important for the design [17]. The thickness of the SiO_2 layer should also be as thin as possible to improve the penetration depth of the photons with higher energy. This can be the case for VUV photodiodes [17]. In another research, the performance of a pn-device was improved without the need of this passivation layer. Here a 4H-SiC pn-junction UV-photodetector was designed and achieved a responsivity of $0.03\ A/W$ at $280\ nm$. The photocurrent was found to be four orders of magnitude larger than the dark current [19].

Since the pin photodiode is a multi-layer device, some care should be taken into the design. The absorption losses in the field free layers should be avoided as much as possible.

This can be accomplished by using very thin p- and n- layers. Furthermore, when selecting a wide bandgap for the doped top layer, it should have absorption in a spectral range that allows for light absorption in the intrinsic layer.

5.2.2. THE AVALANCHE PHOTODIODE

An important disadvantage of the pn and pin-junctions is the lack of gain, i.e. a successfully absorbed photon only generates a single e-h pair. Amplifying the output signal using an external gain will add a significant amount of noise which will drown weak signals of very low optical input signals. In the past another type of devices were used for this, e.g. a photomultiplier (PMT), i.e. a vacuum tube which meets the high sensitivity requirement. However, the PMT has a bulky design, low QE, limited linearity, a narrow spectral operation region and generates heat. The limitations of the PMT and pin photodiodes can be overcome using a pin photodiode designed to have an internal gain, also known as avalanche gain, hence the name avalanche photodiode (APD).

To achieve the internal gain, a large reverse bias voltage is applied to the pin diode near its breakdown voltage. The pin device is however modified to achieve this result by adding a thin layer of p-type doped material between the intrinsic and n-type layers as illustrated in Figure 5.3. Here the electrical field is shown to be maximum at the pn^+-junction.

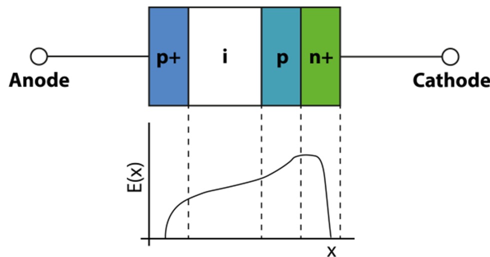

Figure 5.3: Avalanche pin-junction illustration and the electrical field across the layers.

The increased reverse bias allows for a higher electric field close to the junction breakdown enabling impact ionization [14]. Each time that a photon is absorbed, it will generate an e-h pair. The electric field then accelerates the electron which gains enough kinetic energy to cause impact ionization resulting in an avalanche multiplication of electrons, i.e. an internal gain is obtained. The APD knows some adaptations which include hetero-structured devices and multi-quantum well. It also presents many advantages such as high speed, high sensitivity, high responsivity, high internal gain and even low noise. For example 4H-SiC APDs exhibit low noise thanks to the large ionization coefficient ratio of ~ 10 between holes and electrons [17, 20]. The APD can also be based on other types of junctions such as the MS junction [14], but is by far based on the pin-junction. The latter shows trade-offs between the maximum achievable responsivity, speed, and operating voltage [14, 20].

Off course the APD also has disadvantages. The multiplication effect not only results in

a higher photocurrent, but also in a higher dark current and lower noise performance, while also adding noise from the multiplication process itself. The bandwidth of the device becomes smaller while the response time increases due to the avalanche build-up time and holes transit time through the absorption region.

The devices can be improved using various techniques. A pin-junction photodetector was fabricated and showed a dark current density of 63 nA/cm^2 at 90 pA, a QE of 40 % and a gain of 1000. The same device was optimized using a recessed-window structure and by improving the antireflection (AR) coating layer [21]. The work showed a responsivity of 136 mA/W at 262 nm, with an EQE of 60 %, avalanche gains of over 10^6, an excess noise factor characterized by k value of ~ 0.1, and a spatially uniform response [22]. The pin-junction device performance can be further improved by using a separate absorption and multiplication (SAM) structure [20]. A SAM-APD has separate high-field multiplication and absorption regions and by optimizing the thicknesses and doping concentrations of these layers, some of the issues associated with the pin-structure APD can be solved [20]. For instance, the SAM-APD structure injects only a single type of carrier into the multiplication region which reduces the multiplication noise that arises from the stochastic nature of the multiplication process [20]. The fabricated device achieved an optical gain higher than $1.8x10^4$ at 90 % of the breakdown voltage of about 55 V. At 42 V reverse bias and 270 nm wavelength, the peak responsivity increased to 0.203 A/W, corresponding to a maximum EQE of ~ 93 % [20].

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Aside from the avalanche operation, there is the Geiger mode where the devices are operated just beyond their breakdown. This is illustrated in Figure 5.4

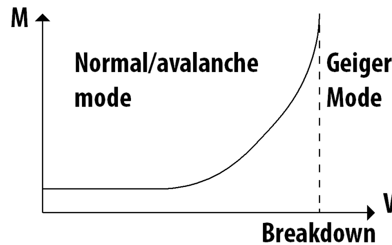


Figure 5.4: Illustration of gain-voltage curve for working modes of an avalanche photodiode [1].

The gain of the devices becomes high, typically in the range of $10^3 - 10^6$. In this operation both electrons and holes will experience multiplication by impact ionization, resulting in a self-sustained avalanche process. Thanks to this, even a single charge carrier could result in an avalanche current, hence single-photon counting is then possible.

Of-course this operation needs to be reset each time after the device has detected a signal. This is done using a quenching circuit which reduces the applied bias after an avalanche event by quenching the rising avalanche current. There are many types of quenching circuits where two popular ones are the passive and active quenching circuits. The most basic circuit for quenching consist of a load resistor connected in series with the photodiode. Such circuits are called passive. Here the reverse bias voltage will

be completely across the diode when there is no avalanche current flowing. As soon as an avalanche current starts to flow, there will a voltage drop across the series load resistor in response to this current flowing through it. This results in decreasing the voltage across the diode, hence the current is quenched [23]. However, there are two main drawbacks to this circuit. The first is the after-pulsing effects which occurs when the voltage across the diode starts to rise immediately after the quenching event. This is an issue because not all trapped carriers may be released, before reaching the operating point again. Furthermore, the device speed is limited because of the RC time constant with R being the quenching resistor. It stands to reason that the time constant can be reduced by reducing the load resistance. However, this may result in the steady-state current level being too close to the threshold voltage where the avalanche is initiated. Hence, the photo-sensitive and quench-stages may overlap and cause a higher error rate [24].

To mitigate the after-pulsing effects and reduce the time constant, one can use active quenching. The after-pulsing effects are mitigated by reducing the total charge of the device, hence the probability of those carriers being trapped in the multiplication region will be less. The circuit uses a comparator to detect the avalanche pulse and reduce the bias and increase it again after a predetermined time [24]. Such an approach is attractive for monolithic integration where the comparator should have a fast response.

5.3. DESIGN

FIGURE 5.5 shows the used structure for the ADP device.

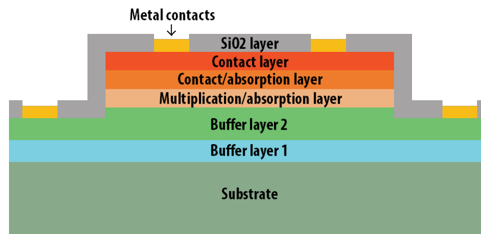


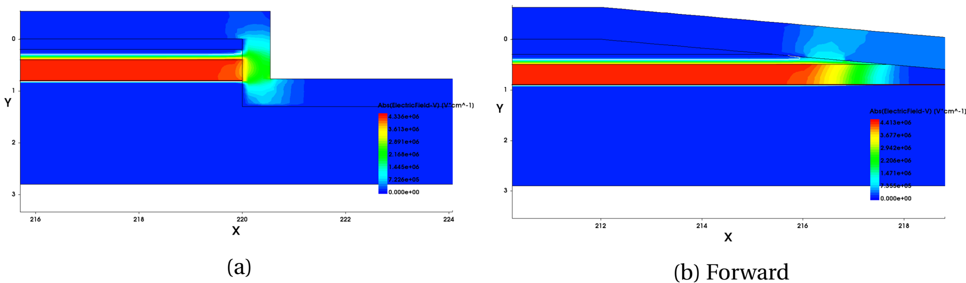
Figure 5.5: APD (SPAD) basic structure.

As can be seen from the figure, the device consists of a buffer layer, multiplication layer, contact/absorption layer and a contact layer. The first buffer layer is a standard manufacturer grown layer. Furthermore, there is a passivation/ARC layer (see Chapter 3) and a metal layer. The buffer layer is usually in the range of a few microns with a high doping, close to that of the substrate. The high doping is also required for good ohmic contacts. The multiplication region should be thick enough for absorption where the total thickness of the layers from top to the multiplication region should be close to 1 micron because of the penetration depth of SiC. We kept this lower to allow deep UV absorption, to some extent. The layer also needs to be low doped. As for the first contact layer (from bottom-up), there will be an electric field present so the layer can be viewed as an absorption layer which will aid in the multiplication process. The charge carriers will diffuse into the multiplication region for this. The top layer should be as thin as possible

to reduce absorption losses, since it will be field free. Furthermore, both contact layers should have high doping. The top layer will form the ohmic contact.

5.3.1. KEY PARAMETERS AND FACTORS

The performance of the device will be strongly determined by the structural choices in terms of layers, thickness, and doping concentrations. Aside from these, the device is also influenced by the edge termination which we will use. Edge termination is critical for reliable operation of devices requiring high voltage operation. It is used to prevent electric field crowding at the edges. If this happens, then surface/edge breakdown may occur. To this end, there are several technologies that have been applied, e.g. planar field, guard rings, and (bevelled) mesa termination. Planar edge termination is applied using implantation which is not straightforward for SiC in terms of implantation energy needed and activation energy. Furthermore, the damage caused by the implantation cannot be completely recovered by the annealing process. As for the mesa termination, this is a well-established process that isolates devices by etching. The etching is typically done using ICP or RIE etching which results in fairly straight walls. However, this method still has 'sharp' edges where the electrical field can be very high. This is illustrated in Figures 5.6.



(a)

(b) Forward

Figure 5.6: Electric field at the edge for MESA a) without and b) with bevel angle.

To overcome this issue, bevelled mesa etching can be applied where the mesa has a positive or negative angle [1]. This has shown that the electrical field will not cause surface breakdown as would be by regular mesa. The bevelled mesa is achieved using photoresist reflow technique a seen for micro-lens fabrication [25]. After the etching, the semiconductor will inherit the photoresist structure. This will be discussed further in the fabrication section. Figures 5.6 show that the electrical field is not extending outside the epitaxial layers at a high strength as compared to a vertical MESA.

Another important factor is the surface passivation of the device which is used for reducing surface leakage. This leakage may be a large dark current component in APD devices. Moreover, it increases with higher bias. Surface leakage is linked to face/interface defects which will reduce the reliability of the device. The surface leakage is enhanced due to the dry etching process used to etch the mesa. However, this damage can be reduced by thermally growing a sacrificial oxide layer and removing this [7]. In this work we used

SiO_2 passivation with a thickness of 632 nm, which is also serving as an antireflective coating (see Chapter 3).

5.4. FABRICATION

After the APD epitaxial stack was defined, substrates were purchased from Tianyu Semiconductor Technology (TYSIC), located in China. The specifications of the substrate are listed in Table 5.1. As the table shows, there is a tolerance issue concerning the thickness and doping concentrations. However, it is still acceptable. Figure 5.7 shows the doping profile of the substrate.

Table 5.1: Specifications of the 4H-SiC substrate for the APD process.

Substrate: n-type, $d = 350 \pm 25\ \mu m$, $Resistivity = 0.0215(\Omega \cdot cm)$		
Layer	**Thickness** (μm)	**Doping** (cm^{-3})
n-type	0.1-0.3	$\geqslant 1.5 \cdot 10^{19}$
n-type	0.2	$2 \cdot 10^{18}$
p-type	0.4	$2 \cdot 10^{15}$
p-type	2	$\geqslant 1 \cdot 10^{19}$
p-type	0.5	$1 \cdot 10^{18}$

* Layers of the epi-stack are listed from bottom to top.

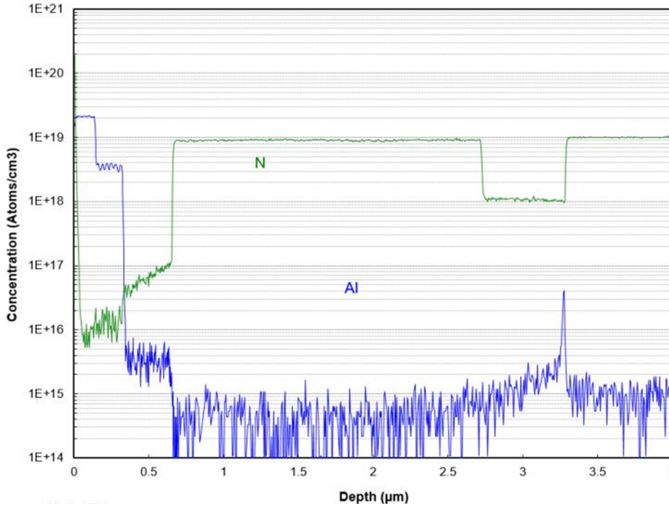


Figure 5.7: Doping profile of the 4H-SiC substrate for the APD process.

The designs were transferred onto a five-reticle mask design for fabrication. Figure 5.8 gives an illustration of this.

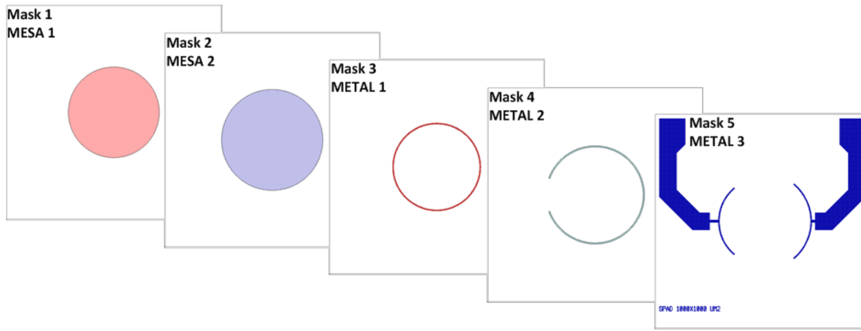


Figure 5.8: Illustration of the five-mask APD design.

The first two masks are used to etch the mesa structures, the third for the metal contact to the top p-layer, the fourth to the n-type region (buffer layer), and the last one is the overlay metallization for wirebonding. Furthermore, the wafer fabrication, is divided into four regions, similar to the MSM device fabrication. Here each region has undergone a difference in the photoresist reflow to obtain different bevel angles for the first MESA structure. The other steps are similar for all regions.

The fabrication steps are illustrated in Figures 5.9. In a nutshell, the fabrication consists of defining MESA 1(Figure 5.9a), MESA 2 (Figure 5.9b), p-contact (Figure 5.9c), n-contact (Figure 5.9d), and overlay contact (Figure 5.9e).

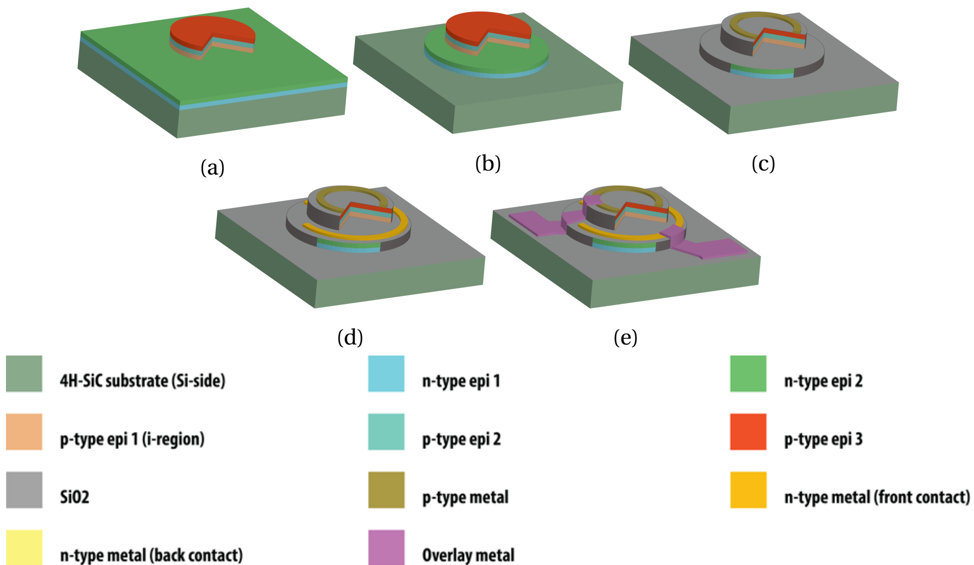


Figure 5.9: Fabrication steps of the APD devices.

The process starts with a $silicon^+$ cleaning process to remove any contamination on the 4H-SiC substrate. Before moving further, an aluminium layer is deposited at the backside of the wafer to make the wafer opaque for optical detection in fabrication tools. The layer should be sufficiently thick to account for any etching in BHF baths when processing SiO_2 layers. This is followed by etching a zero layer in the substrate to allow alignment of subsequent lithography steps. The zero layer does however have extra alignment markers to allow the four-region fabrication scheme. Figure 5.10 illustrates this.

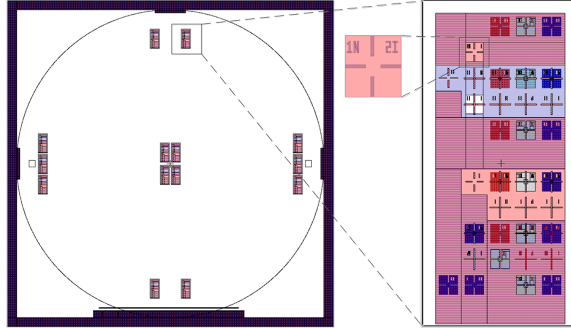


Figure 5.10: Zero layer alignment markers. There are 12 extra alignment markers to allow alignment per region.

The process steps for the alignment markers starts with photoresist coating, image transfer of the zero layer into the photoresist mask, ~ 120 nm ICP etching of SiC using the Chlorine-based recipe (see Chapter 3), and photoresist stripping. An example of the etched alignment markers is shown in Figure 3.18a in Chapter 3.

Since we use a four region process, before we start with the formation of the first MESA structures, each time we process a region we need to protect three regions from etching. Thus prior to each MESA 1 lithography step, we first deposit a 4 μm PECVD SiO_2 hard mask is deposited on the top surface of the substrate. This is followed by removing the oxide from the targeted region on the substrate. The removal is done using reticle blanking, similar to the MSM fabrication. This process consists of negative photoresist coating, exposure using the stepper, BHF etching of the layer, and photoresist stripping. The wafer is then coated with a positive photoresist layer. The layer should have sufficient thickness because it needs to be at least > 4.65 μm to account for the etch rate. However, the reflow process allows for the photoresist to take a lens-like shape where the thickness will be higher in the middle (see for example the height measurements in Figure 5.17a). Figures 5.11 illustrate the process for MESA 1 in each region.

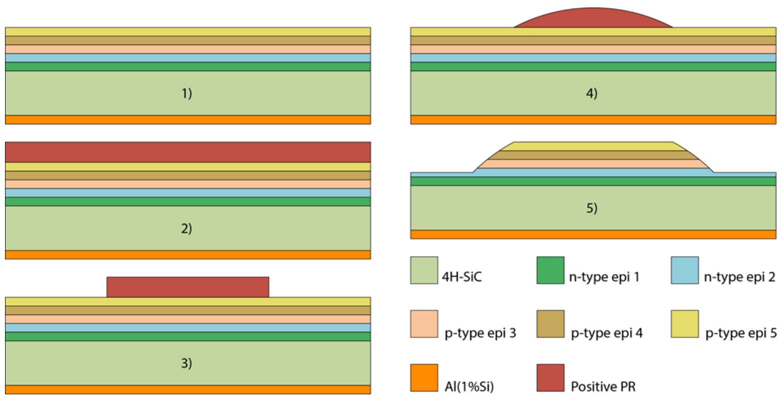


Figure 5.11: MESA 1 process flow. 1) Starting structure, 2) positive PR coating, 3) PR patterning, 4) PR reflow, 5)Structures are etched and PR is removed.

The four regions will have different bevel angles for MESA 1. This is done by using > 4, 8, and 12 μm photoresist thickness. The photoresist is then reflowed at a temperature of 160 °C for one hour for sufficient reflow [25]. One region doesn't undergo the reflow process (step 4 in Figure 5.11) to have nearly straight walls instead of a bevel angle. The reflow process is generally used to form lens shapes in Si for photonic applications [25, 26]. By coating a thick layer of photoresist and heating it up in an oven (after development), the photoresist will reshape into a lens-like structure. This is illustrated in Figure 5.16a. Figures 5.12 illustrate MESA 1 structures in the region without reflow process. It should be noted that figure on the right side is exaggerated to better illustrate the shape of the MESA.

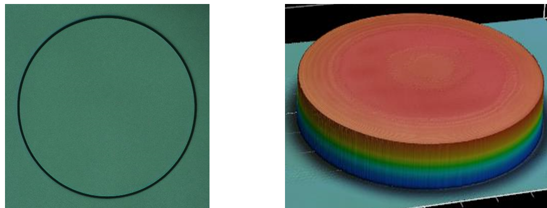


Figure 5.12: Resulting MESA 1 structure in the region without reflow processing. The figures are from after etching and cleaning.

It should be noted that the etch process is not a Bosch process because we only use the etching step without the side-wall passivation, hence no cycling occurs but a continuous etching is done. The etch process is thus RIE (see Chapter 3).

Figure 5.13 shows the thickness of the resulting structure in the resist before etching, resist after etching, and after cleaning. Nonetheless, since we used the RIE etch process, we did not get vertical walls but rather at an angle.

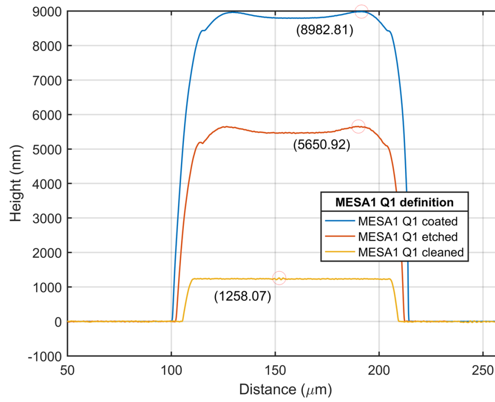


Figure 5.13: MESA 1 height measurements in the region without reflow.

The angle which we obtained was calculated to be ~ 14.1^o. On the other hand, the other three regions did undergo the reflow process. This comes immediately after development and hard baking of the positive photoresist. Figures 5.14 illustrate some of the resulting structures in the > 4 μm region.

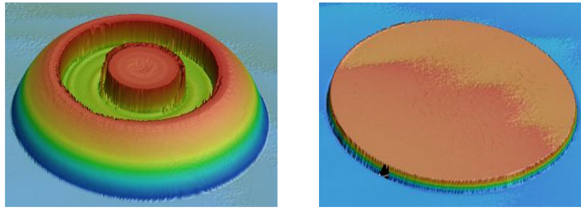


Figure 5.14: Region with the 4 μm reflow process. The left figure is after reflow nd etching while the right figure is after.

As can be seen, when the photoresist is not sufficiently thick, the resist will be uneven after reflow and doesn't form the lens shape. However, if the thickness is still sufficient with respect to the etch rate, then it doesn't affect the result since we are only interested in the bevel angle at the MESA edge. The angle after etching is ~ 5.1^o. Figure 5.15 shows the height measurements of the structures.

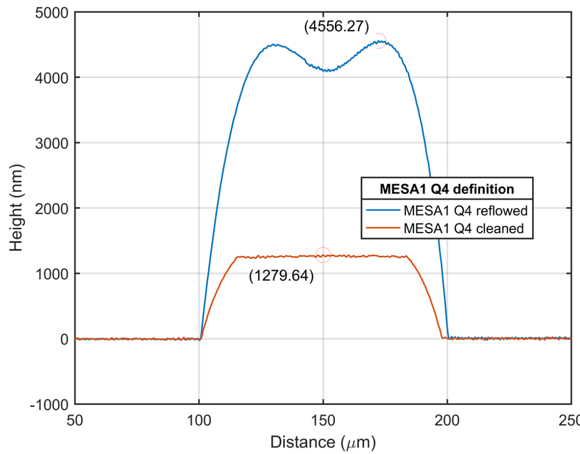


Figure 5.15: MESA 1 height measurements in the regions using reflow. The used PR thickness is > 4 μm.

The remaining two regions were coated with thick photoresist layers of 8 and 12 μm, respectively. Figures 5.16 show examples of the structures after reflow (Figure 5.16a), etching (Figures 5.16b-5.16c), and cleaning (Figure 5.16d).

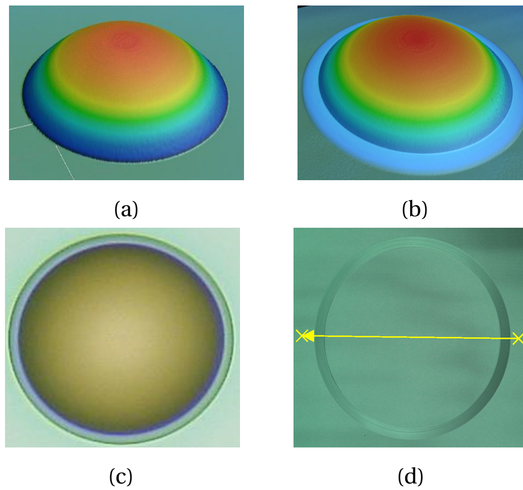


Figure 5.16: Resulting structure after reflow and etching of 8 and 12 um photoresist structures.

The structure thickness measurements for the reflowed regions are shown in Figures 5.17. The resulting angles are 5.9^o and 7.7^o for photoresist height of 8 and 12 μm, respectively.

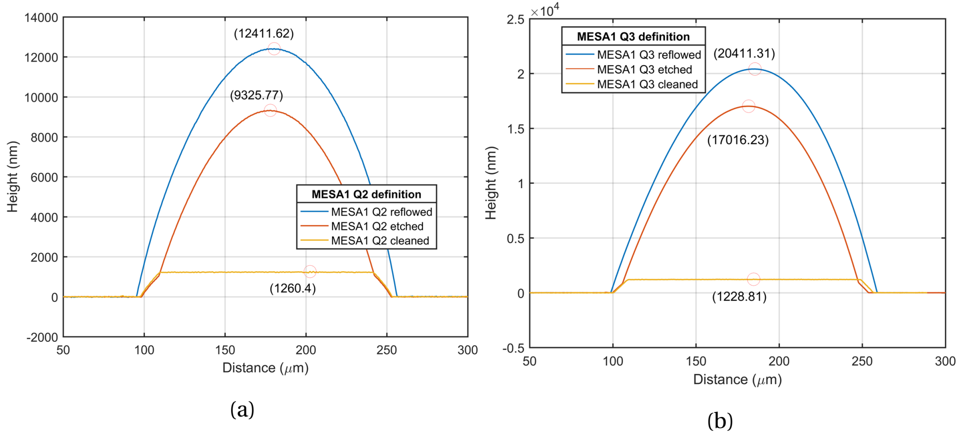


Figure 5.17: MESA 1 height measurements in the regions using reflow. The used PR thickness is 8 and 12 μm, respectively.

After etching the first MESA in all four regions, the second mesa process steps were done. Consider Figure 5.18 showing the process flow for MESA 2. Because the second MESA is etched deeper in the substrate, and no reflow is required, a PECVD SiO_2 hard mask is deposited and used for the transfer of the structures. This is followed by a lithography step and a wet etch step using BHF to transfer the layer into the hard mask. After this, a RIE etch step is done to transfer the pattern in the SiC substrate. Subsequently, the wafer is cleaned and the SiO_2 hard mask is removed using BHF.

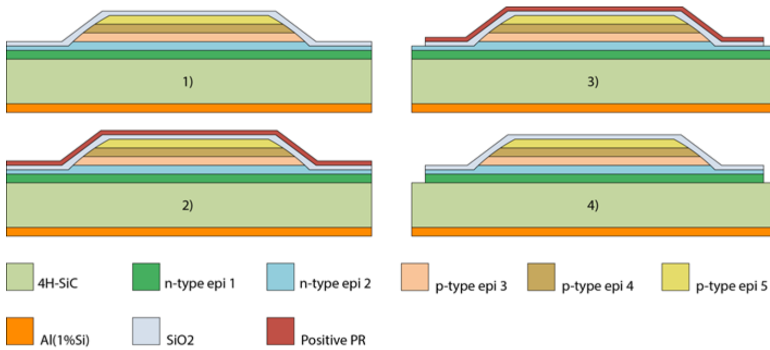


Figure 5.18: MESA 2 process flow. 1) PECVD SiO_2 hard mask (HM) deposition, 2) HM patterning, 3) PR removal, and 4) HM patterning and subsequent etching of MESA 2 in SiC.

Since the wafer has undergone several process steps, surface damage may occur in the form of scratches, etch damage, etc. To remove this, a sacrificial thermal oxidation step was done to grow a thin layer of oxide and remove this using BHF. Subsequently, the fabrication is started with another thermal oxidation followed by a deposition of LPCVD SiO_2. The oxide layer is used as both an antireflection layer and passivation layer. Hence,

the total layer thickness is according to the calculated value of the antireflective coating seen in section 3.4 of Chapter 3.

The remaining fabrication steps are done to define the contacts of the devices. Both contacts to the p- and n-type regions were defined using lift-off processing, similar to the MSM devices in Chapter 4. Figure 5.19 illustrates the process flow.

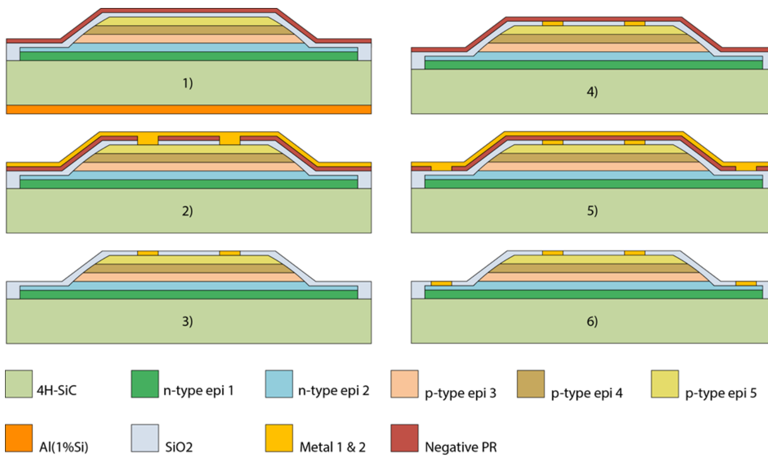


Figure 5.19: Contact definition process flow. 1) M1 Nlof PR patterning, 2) M1 evaporation, 3) M1 Lift-off, 4) M2 Nlof PR patterning, 5) M2 evaporation and 6) M2 Lift-off.

For each of the two metals, the steps are 1) lithography using negative photoresist, 2) BHF transfer of the patterns from photoresist into the SiO_2 layer, 3) beam evaporation of required metals and 4) removal of photoresist using NMP (lift-off), hence a metal pattern is transferred in the SiO_2 opened windows. Both metallization stacks of the contacts consist of Ni/Ti/Al/Au (35/50/150/100 nm) [2, 12, 13]. Figures 5.20 show the resulting structures. From the figures, we can clearly see that the bevel angle of MESA 1 changes for different photoresist thickness.

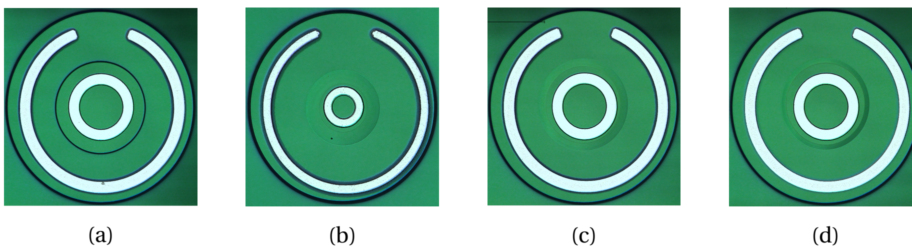


Figure 5.20: Metal one and metal two structures. a) Region without reflow, b) > 4 μm reflowed region, b) 8 μm reflowed region, and b) 12 μm reflowed region

The substrate subsequently undergoes a rapid thermal annealing (RTA) step at 850 °C for three minutes in N_2 ambient. This step is done to form ohmic contacts to the n-

and p-type regions. After this, the third and final metallization step is done for overlay formation. Similar to the previous metallization steps, first the substrate undergoes a lithography step using negative photoresist. Here we do not need to etch the SiO_2 layer, thus a metal evaporation step is done immediately after this. The stack consists of Ti/Au (200/800 nm). The process flow is shown in Figure 5.21.

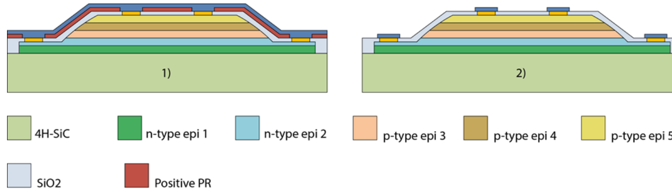


Figure 5.21: Overlay definition process flow.

5

An example of the final structure of the APD device is shown in Figure 5.22a. Figures 5.22b-5.22c show the contact form at the edge of the device.

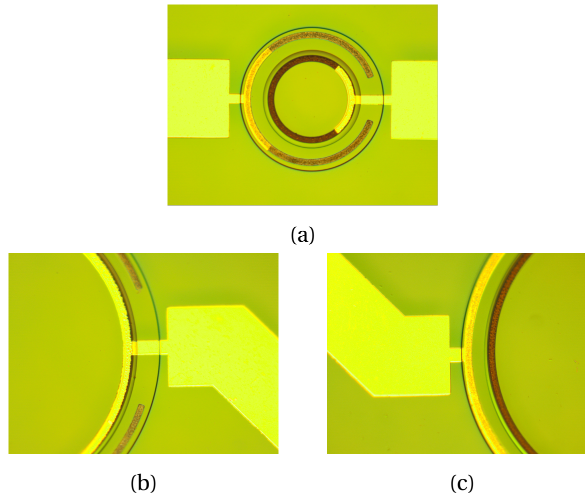


Figure 5.22: 4H-SiC device after overlay definition. a) Complete device, b) Top contact, and c) Bottom contact.

5.5. RESULTS AND DISCUSSION

The APD devices were measured at die level and the measurements are limited to the IV characteristics. Here we used the same setup as for the MSM devices. The devices were brought into a breakdown using a high voltage source where the output of the devices was read-out using a lock-in amplifier in combination with a chopper. The UV response was measured at 270 nm. Figures 5.23 show the leakage and dark currents of four devices, each corresponding to one of the etched regions.

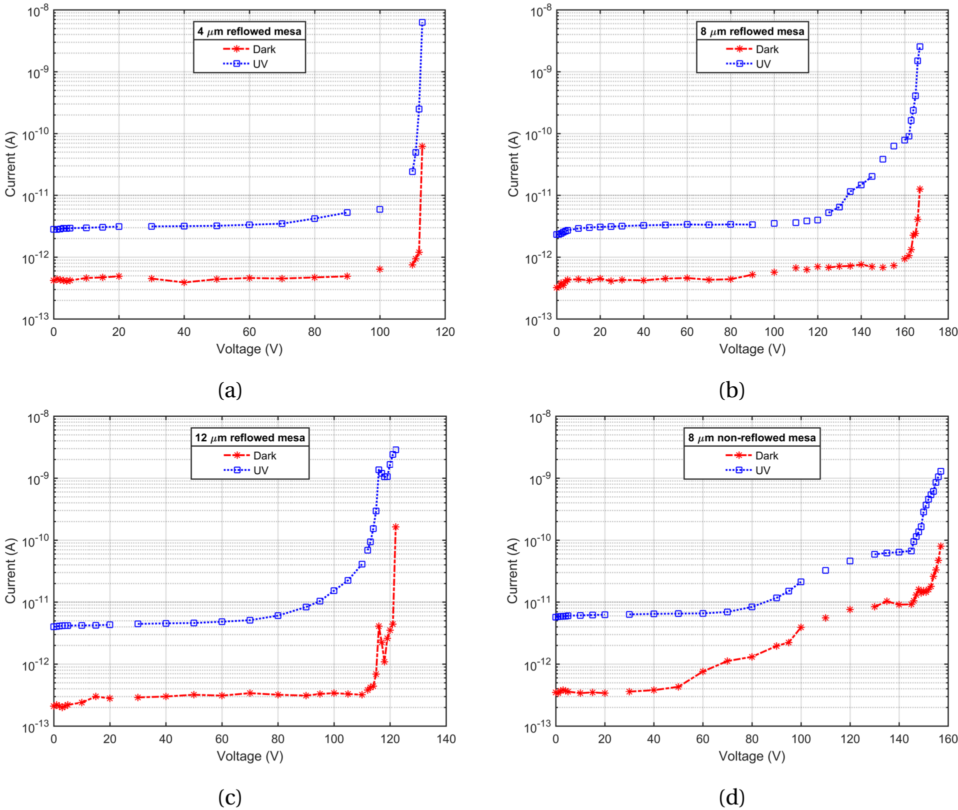


Figure 5.23: I-V responses of APD devices with a) > 4 μm reflowed region, b) 8 μm reflowed region, c) 12 μm reflowed region, and d) region without reflow,

As can be seen, all devices with reflowed mesas show leakage currents in the range of sub pA for reverse bias voltages lower than 100 V. The leakage currents are 0.64 pA, 0.57 pA and 0.34 pA for 4 μm, 8 μm and 12 μm reflowed mesas, respectively. This corresponds to current densities of 1.848 nA/cm^2, 1.645 nA/cm^2 and 0.982 nA/cm^2 for an area of $3.464 \cdot 10^4$ μm^2, respectively. From this, it can be concluded that the higher the bevel angle of reflowed resist, the lower the leakage current will be. If we compare this to the devices with non-reflowed resist, the leakage current is considerably smaller.

To reach the avalanche breakdown, the voltage should be sufficiently high to reach the

critical electrical field at 3.2 MV/cm. As can be seen from Figures 5.23, avalanche breakdown starts at 110 V, 160 V, and 113 V, for 4 μm, 8 μm and 12 μm reflowed mesas, respectively. Taking the currents at half the avalanche breakdown voltages and at avalanche, the gain is calculated to be 2246, 891, and 597 for for 4 μm, 8 μm and 12 μm reflowed mesas, respectively. The device with no reflow has a gain of 208. Although the device with the smallest bevel angle has shown the largest leakage current, it has the highest gain. This shows that the optimal devices are with the smallest bevel angles. Furthermore, the avalanche breakdown occurs earliest for the smallest bevel angle which allows for lower voltage operations. This makes it more suitable for constructing arrays.

5.6. Chapter Summary

Avalanche photodiodes are important in fields requiring ultra-low light or even single-photon detection. 4H-SiC APDs are advantageous for detecting weak UV signals thanks to their small size, low dark current, high multiplication gain, and high quantum efficiency. The devices were simulated and showed good avalanche behaviour. In this chapter we discussed the design, fabrication, and testing of a 4H-SiC APD. The devices are based on epitaxial technology to ease the fabrication constraints w.r.t. implantation, activation and etching. This allowed for device fabrication in our cleanroom facilities. The bevel angles were etched by using the photoresist reflow technique to make lens shape structures and transferring the side-angles into the SiC substrate. Even-though the smallest bevelled angle device showed the highest leakage current, this is still not as impact-full as the gain it shows. Here the device with the smallest bevel angle showed the largest gain at an earlier breakdown voltage. This renders it suitable for array fabrication.

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6

TOWARDS SIC CMOS SENSORS AND ELECTRONICS TECHNOLOGY

In this chapter, we give an introduction towards SIC CMOS technology for sensors and electronics realization as a feasibility study. This is based on SiC technology for power devices. Here we focus on a CMOS based temperature sensor fabricated at Fraunhofer IISB Erlangen, Germany. The design was based on basic LT-spice models and the layout was done using L-Edit. The temperature sensors are tested for their basic temperature behaviour. Due to time-constraints, we onluy introduce the SiC CMOS technology to show some of the exciting possibilities. The full characterization is future work.

6.1. Introduction

Silicon carbide sensors for harsh environments are been developed over the years while SiC CMOS remains in research-phase due to its immaturity. The latter is required for monolithic integration of devices with their respective circuits to obtain systems capable of harsh environment operation. To this end, circuits should be developed using this technology. This not only helps to reduce packaging complexity, as would be the case for Si technology, but also by tailoring the circuits for the device at hand and reducing noise sources. The used SiC CMOS technology is developed by Fraunhofer IISB in Erlangen, Germany, which have experience with SiC power electronics, photodiodes, and recently low power CMOS. However, the latter is still in development and needs much investigation.

The SiC CMOS technology is based on n-type 4H-SiC substrates in which N-well (NW), P-well (PW), shallow-N (SN), and shallow-P (SP) are implanted. Their process requires much higher temperatures for dopant activation, as well as rapid thermal annealing (RTA) steps to form ohmic contacts. The gates are formed using poly-Si. Table 6.1 gives an overview of the used SiC technology.

Table 6.1: Overview of FH SiC CMOS technology.

Parameter	**Setting**
Gate oxide	Thermal, 50 nm
Gate type	Poly-Si, 500 nm
n-type epi	$5-8\cdot10^{14}cm^{-3}$
N-well	$3\cdot10^{15}cm^{-3}$
P-well	$1\cdot10^{17}cm^{-3}$
Metal 1	Al, 700 nm
Silicides n-type	NiAl
Silicides p-type	AlTi

The CMOS technology is designed based on their provided models for PMOS and NMOS devices and are valid only for the fixed temperatures of 25 °C, 50 °C, 100 °C, 150 °C, 200 °C, 250 °C, 300 °C, 350 °C. The models describe only the I-V characteristics in the first quadrant, the body-diode is not modelled. Furthermore, they are only optimized for the saturation region where the current in the subthreshold region is overestimated. And the minimum length should be $\geq 6\mu m$ where channel length modulation is not modelled. The supply voltage (V_{dd}) is 20 V.

6.2. Threshold voltage based temperature sensing

In CMOS technology, the most popular researched temperature sensors are based on the proportional-to-absolute temperature (PTAT) scheme to utilize the temperature- dependent characteristics of the pn-junction [1–4]. Here, the circuit takes advantage of the voltage difference between two forward-biased diodes of bipolar junction transistors (BJT) which occurs due to a difference in current or area [4]. The disadvantage of this method is that it requires on-chip dynamic element matching, trimming, or post fabri-

cation calibration to achieve the required matching between the individual current mirrors for good accuracy. This results in large area, large power consumption, and higher complexity [3, 4]. The latter is important for SiC-CMOS technology because complexity should be avoided due to the immaturity of the technology.

In this work, we do not focus on the readout scheme for the sensor but rather on the sensor itself. To this end, we have tested two types of sensors for high temperature applications. The first device is the diode-based temperature sensor which was discussed in Chapter 4. Both devices were tested for their temperature behaviour, up to 200 °C. Due to time-constraints, the characterization of the devices was not done and is future work. Nonetheless, this work introduces the SIC CMOS technology for sensors and low power electronics. Here, we present a MOS temperature sensor structure based on silicon technology [1]. In silicon, this device is compact and is linear with respect to temperature. The 2nd and 3rd order temperature non-linearities can be mitigated thanks to proper sizing of the MOSFETs, hence a highly linear voltage output signal can be obtained [1]. The sensor can be designed to occupy small die area and have low power consumption. Moreover, the threshold voltage expressed at the output is highly linear over practical temperatures of silicon technology. The sensors still exhibit small nonlinearity due to the finite output impedance of the MOS transistor. However, in this work we aim to use SiC-CMOS technology where the practical range is much higher. Furthermore, since we aim for a proof of concept, and without having a mature technology and its models, we do not strive to optimize the structure. Consider equation (6.1) giving the expression for the threshold voltage equation which is widely used in simulators.

$$V_{TH}(T) = V_{TH,0} + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{BSeff}\right) \cdot \left(\frac{T}{T_0} - 1\right) \tag{6.1}$$

Where T_0 is the base temperature at $300K$. $KT1$, $KT1L$, and $KT2$ are process dependent constants, L_{eff} is the effective gate length, and $V_{BS_{eff}}$ is the effective body to source voltage. In the ideal case, the output voltage is linearly dependent on absolute temperature whereas the proportionality constant is not temperature dependent.The wide range of operation of this structure is thanks to the VDD-independent self-stabilized inverse-Widlar architecture. The tested structures are presented in Figures 6.1.

Note that the structures are similar except for $M6$. The additional MOSFET as a start-up device to eliminate undesired operating points. In this work we added circuits with and without the extra device. It should not affect the temperature-dependent characteristics of the circuit. The output voltage is proportional to the threshold voltage of the n-channel devices. The sizing of the transistors is critical to the operation of the circuit where designers in Si technology usually focus on linearity and power consumption. $M2$ is important for the power consumption and voltage headroom. Therefore, this is usually smaller compared to $M1$. As for $M4$ and $M5$, these form a current mirror and determine the currents I_1 and I_2. The devices are kept the same so that the current mirror has a gain of one to mitigate the 2nd order temperature non-linearities [1].

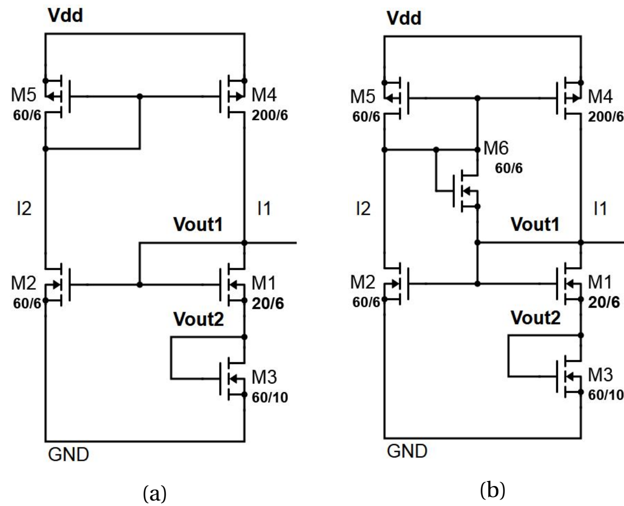


Figure 6.1: Temperature sensor based on the inverse Widlar current mirror a) without and b) with start-up device.

Recalling equation (6.1), the threshold voltage is dependent on V_{BSeff} which is the effective body to source voltage. This voltage is temperature dependent and therefore, by connecting the body of the devices to their respective sources, one can mitigate this nonlinearity. However, since $M1$ doesn't have that option, we focussed on expressing the output voltage mainly in the threshold voltage of $M2$. This means that by increasing the size of $M2$, the power consumption will be higher, but is not an issue for this work. This also means that the current mirror should be used to reduce the dependence on the threshold voltages of $M1$ and $M3$. This is reflected in the expression for the voltage output (V_{out}). The analytical expression (6.2) is obtained using the square-law device model where the channel length modulation is neglected.

$$V_{out} = \frac{V_{tn2} \cdot \left(1 + \sqrt{\frac{(W/L)_1}{(W/L)_3}}\right) - (V_{tn1} + V_{tn3}) \cdot \sqrt{\frac{(W/L)_1}{(W/L)_2}}}{1 + \sqrt{\frac{(W/L)_1}{(W/L)_3}} - \sqrt{\frac{(W/L)_1}{(W/L)_2}}} \tag{6.2}$$

Where M is the current mirror gain. This equation shows the linear dependence on the threshold voltage. Furthermore, there is no V_{dd} in the expression, hence the device is power supply independent. In practice, there will be some dependence due to a finite output impedance [2]. Its linearity is also affected by this. Consider Figure 6.2 showing the simulated circuit (with start-up device) using the FH MOS models.

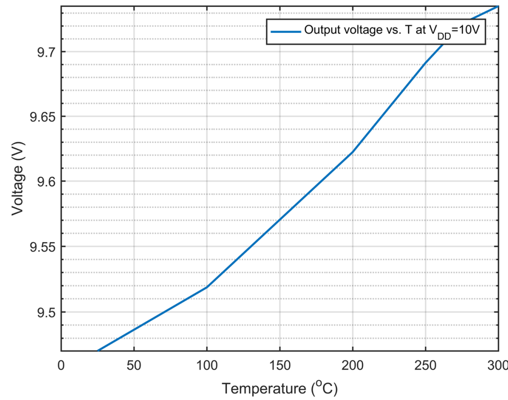


Figure 6.2: Simulated output voltage vs. temperature.

The circuit did not show V_{dd} independence and the curve is not smooth. This could be attributed to the immaturity of the provided models. However, thanks to this we could have a base design for fabrication. Figures 6.3 show the layout for both devices.

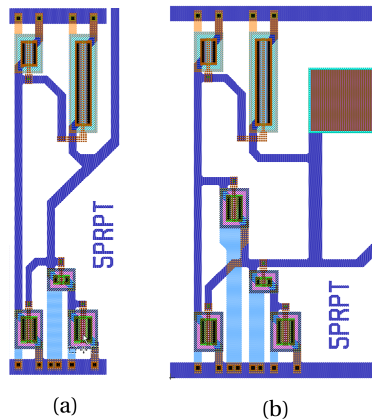
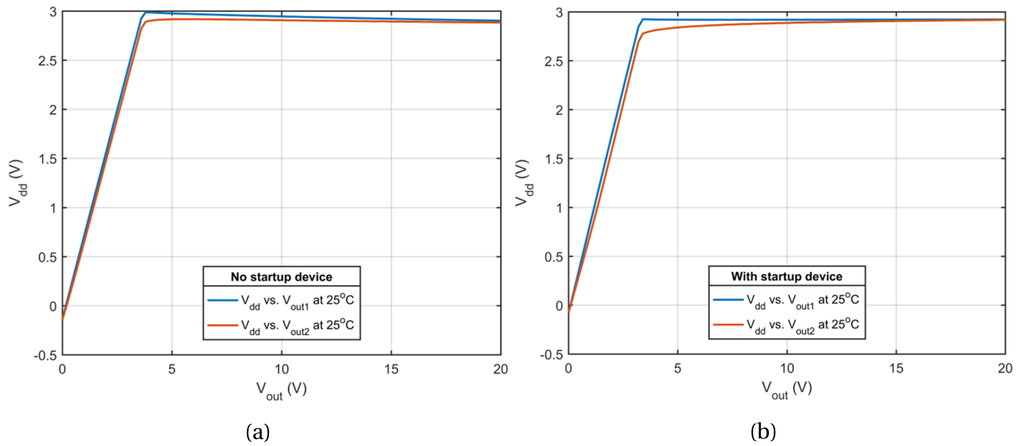


Figure 6.3: Temperature sensor layout a) without and b) with start-up device.

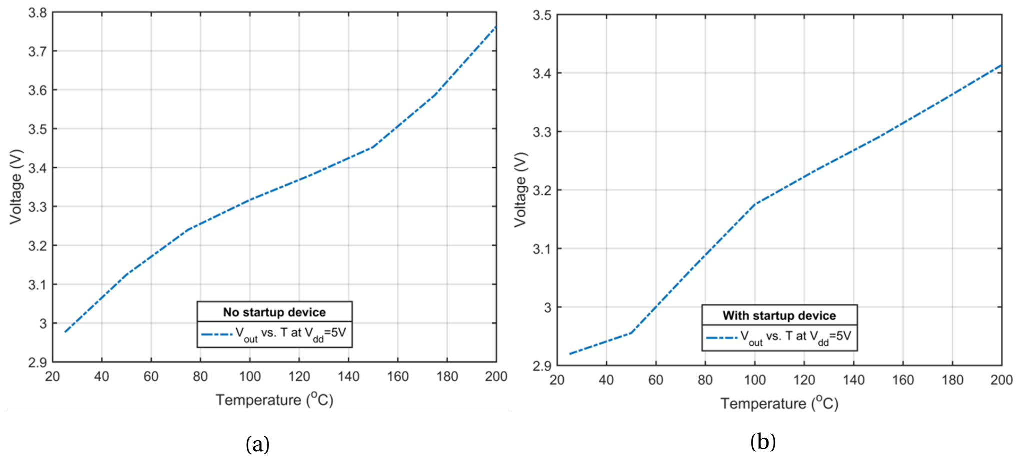
The basic measurements of the fabricated devices showed very small dependence on V_{dd} as mentioned in literature. Figures 6.4 show the output voltages Vs. V_{dd} at 25 °C for both circuits.



(a) (b)

Figure 6.4: V_{dd} vs. V_{out} at room temperature for the circuits a) without and b) with start-up device.

As can be seen, both outputs have nearly the same values thus we only use V_{out1}. The temperature curves for circuits are shown in Figures 6.5.



(a) (b)

Figure 6.5: V_{out} vs. T at V_{dd} for the circuits a) without and b) with start-up device.

The circuit with the start-up device shows good linearity above 100 °C. To be able to say more about this, additional measurements of other devices should be made at a wider temperature range.

6.3. CHAPTER SUMMARY

In this chapter, we introduced SiC CMOS technology which was used to fabricate the threshold voltage based temperature sensors. The designs of the circuits relied on using

LT-spice simulations based on immature PMOS and NMOS models. Here channel length modulation was not taken into account. Nonetheless, this provided a starting point for us. The layout design was done in L-edit and verified for the design rules using K-layout. The process as a whole was done at the Fraunhofer IISB Erlangen, Germany. For some of the wafers, we did the metallization at our facilities, EKL. Basic measurements up to 200 °C have been done for the temperature sensor which showed good behaviour. Future work should include testing of the devices at high temperatures, well above 200 °C.

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7

CONCLUSIONS AND RESEARCH OUTLOOK

This chapter summarizes the conclusions of the work done in this thesis. The research objectives were to develop various sensors for high sensitivity and harsh environment applications.

7.1. SILICON SENSOR

The first sensor, a bulk micro-machined high sensitivity accelerometer was designed, simulated, fabricated and characterized. By employing non-linear behaviour of four long slender beams to support a proof-mass, an operating point has been obtained where extremely low spring stiffness occurs. An integrated IDT capacitive transducer is used to readout the displacement of the proof-mass. The integration of the capacitive transducer was made possible using trench isolation technique to electrically isolate the electrodes of the capacitor, all fabricated in the same bulk silicon. The devices were capped using Pyrex glass dies. A PCB containing readout ASIC was used to readout the accelerometer. The PCB was then connected to a high-resolution impedance readout system, forming a measurement system. The device, at it its lowest resonance frequency of 8.7 Hz, the capacitive sensitivity and the experimentally characterised noise floor of the readout chip, the theoretically obtainable system resolution equals 17.02 $ng/\sqrt{Hz}$. This work shows that the proof of concept is promising for future iterations.

Recommendations for future work

- The fabrication of the devices was on the edge of feasibility. A larger die size would allow for thicker beams which would not only relax the fabrication constraints but also increase the reliability of the overall device.
- Use a different isolation method to avoid large parasitic capacitances. This will result in better performance of the device. Next to this, the isolation method should be improved to enhance the structural strength of the device. An alternative to having a capacitive readout while relaxing the fabrication is to use parallel plate capacitance. This can be done by using metal IDT on either side of the device and on the glass wafers which are used to encapsulate the device.
- Integration of the read-out ASIC to have a system in package (SiP). This can help reduce interference causing noise.

7.2. SILICON CARBIDE SENSORS

4H-SiC has a significant advantage over silicon when dealing with certain applications such as UV and harsh environments. UV detection doesn't require filtering when using WBG semiconductors. Thermally growing SiO_2 is one of the advantages of SiC over other WBG semiconductors. The oxidation of SiC was therefore investigated and characterized. The results showed a good fit with the DG-model but needs further investigation as to how the behaviour is in all crystal directions. Furthermore, 4H-SiC etching was also investigated by using the ICP and RIE processes. The results from these experiments were used to fabricate MSM Schottky sensors for multi-sensing applications using various metallizations. The metals used are Mo, Ta/Pt, Pd, and Ni, where the last two showed the best dark current performance in the range of pA. The devices showed reasonable dark currents at 200 °C where Ni electrodes gave a dark current of ~ 223 pA at 20V bias. Although Pt has a large metal workfunction, the dark current reached ~ 1.52 mA at 200 °C for the same bias. The tantalum adhesion layer has a lower metal workfunction at a value of 4.22 eV, hence a lower Schottky barrier height resulted, at around 0.6 eV. The reason for using Ta as an adhesion layer is because the Pt comes off when doing the

Scotch tape test. It was assumed that due to metal stacking, the overall Schottky barrier would increase sufficiently high. The observed metal workfunction is ~ 0.8 eV which is higher than what would be expected for Ta/4H-SiC but is still lacking. Additionally, also the processing has an influence on the SBH. The ideality factors calculated using the standard IV method showed high values which means that the devices need improvement. This can be done for instance by annealing the devices at higher temperatures to improve the metal-semiconductor interface. Other alternatives may be the surface passivation prior to metallization which potentially can result in also lower leakage currents. An example of surface passivation can be done by inserting a dielectric such as aluminium oxide to passivate surface defects, but also preventing diffusion of metals. Although not characterized for its UV behaviour, the Mo metal, showed a Schottky barrier of about 1.2 eV which means that it can be used for optical detection. This metal is useful for high temperature applications and other harsh environments because it is a refractory metal. This allows the device to be used for high temperature applications where the device is used as a PTAT temperature sensor. The W5S5 devices with Mo electrodes were tested up to 200 °C and showed good temperature behaviour. The findings are encouraging to further investigate the device for multi-sensing applications targeted at harsh environments.

In addition to this device, dedicated devices for UV sensing and temperature sensing (SiC CMOS) were developed. The first is an avalanche photodiode which is advantageous for detecting weak ultraviolet signals thanks to its small size, low dark current, high multiplication gain, and high quantum efficiency. Such detectors can be used in a wide range of applications, e.g. corona discharge, flame detection, missile plume detection, UV astronomy, UV LIDAR, and biological and chemical detection. We discussed the design, fabrication, and characterization of a 4H-SiC APD. The devices are based on epitaxial technology to ease the fabrication constraints w.r.t. implantation, activation and etching. This allowed for device fabrication in our own cleanroom facilities. The bevel angles were etched by using the photoresist reflow technique to make lens shape structures, and transferring the side-angles into the SiC semiconductor. As for the temperature sensing, this is based on SiC CMOS technology. The devices are threshold voltage based temperature circuit sensors. The designs of the circuits relied on using LT-spice simulations based on immature PMOS and NMOS models. Here channel length modulation was not taken into account. Nonetheless, this provided a starting point. The layout design was done in L-edit and verified for the design rules using K-layout. The process as a whole was done at the Fraunhofer IISB Erlangen, Germany. For some of the wafers, we did the metallization at our own facilities, EKL. Basic measurements up to 200 °C have been done for the temperature sensor which showed good behaviour. Future work should include testing of the devices at high temperatures, well above 200 °C.

Recommendations for future work

- Further investigation of SiC oxidation and etching. This allows for better prediction of the oxidation in all directions. It is important to improve the etching rates and masking.
- Further improvement of the Schottky diodes in terms of their Schottky barrier heights and ideality factors. As for temperature sensing, refractive metals would

be investigated as these are more suited for harsh environments.

- The APD device should be improved in terms of operation voltage to allow lower voltage operation for low power applications. This can be done by improving the epi-stack through simulations.
- The APD device should be further characterized for its behaviour towards single-photon detection.
- Improve the understanding of SiC CMOS circuits by further investigation of technological parameters. The models need further improvement.
- The temperature sensor circuits need to be characterized at high temperatures and also investigate their reliability.

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2. **El Mansouri, B.**, Middelburg, L.M., Poelma, R.H., Zhang, G.Q., van Zeijl, H.W., Wei, J., Jiang, H., Vogel, J.G., and van Driel, W.D.: 'High-resolution MEMS inertial sensor combining large-displacement buckling behaviour with integrated capacitive readout', Microsystems & Nanoengineering, 2019, 5, (1), pp. 1-14

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