# The Zoom ADC

## An Evolving Architecture

Eland, Efraïm; Mehrotra, Shubham; Karmakar, Shoubhik; van Veldhoven, Robert; Makinwa, Kofi A.A.

**DOI**
10.1007/978-3-031-28912-5_10

**Publication date**
2023

**Document Version**
Final published version

**Published in**
Biomedical Electronics, Noise Shaping ADCs, and Frequency References

**Citation (APA)**
Eland, E., Mehrotra, S., Karmakar, S., van Veldhoven, R., & Makinwa, K. A. A. (2023). The Zoom ADC: An Evolving Architecture. In *Biomedical Electronics, Noise Shaping ADCs, and Frequency References: Advances in Analog Circuit Design 2022* (pp. 179-201). Springer. https://doi.org/10.1007/978-3-031-28912-5_10

# The Zoom ADC: An Evolving Architecture


**Efraïm Eland, Shubham Mehrotra, Shoubhik Karmakar, Robert van Veldhoven, and Kofi A. A. Makinwa**

**Abstract** Zoom ADCs combine a coarse SAR ADC with a fine delta-sigma modulator ($\Delta\Sigma$M) to efficiently obtain high energy efficiency and high dynamic range. This makes them well suited for use in various instrumentation and audio applications. However, zoom ADCs also have drawbacks. The use of over-ranging in their fine modulators may limit SNDR, large out-of-band interferers may cause slope overload, and the quantization noise of their coarse ADC may leak into the baseband. This chapter presents an overview of recent advances in zoom ADCs that tackle these challenges while maintaining high energy efficiency. Prototypes designed in standard 0.16 μm technology achieve SNDRs over 100 dB in bandwidths ranging from 1 to 24 kHz while consuming only hundreds of μWs.

## 1 Introduction

Audio applications often require analog-to-digital converters (ADCs) with high dynamic range (DR), high energy efficiency, and low area [1–4]. By combining a low-power successive-approximation register (SAR) ADC with a high-resolution delta-sigma modulator ($\Delta\Sigma$M), zoom ADCs can meet all these requirements [1–6]. The SAR ADC coarsely determines the references of the fine $\Delta\Sigma$M, drastically reducing loop filter swing and enabling energy-efficient design. The overall digital output is then obtained by simply summing the outputs of both converters.

E. Eland (✉) · S. Mehrotra
Delft University of Technology, Delft, the Netherlands

NXP Semiconductors, Eindhoven, the Netherlands
e-mail: efraim.eland@nxp.com

S. Karmakar · K. A. A. Makinwa
Delft University of Technology, Delft, the Netherlands

R. van Veldhoven
NXP Semiconductors, Eindhoven, the Netherlands



P. Harpe et al. (eds.), *Biomedical Electronics, Noise Shaping ADCs, and Frequency References*, https://doi.org/10.1007/978-3-031-28912-5_10

Proposed ΔΣMs with finite impulse response (FIR) DACs and negative R-assisted integrators are also capable of satisfying the requirements of audio applications [7–10]. An FIR DAC essentially filters out the fed-back quantization noise and thereby also relaxes loop filter swing. However, it introduces an extra delay in the feedback path, which requires an additional compensation path to maintain stability and restore NTF [7, 10]. This delay also limits the extent to which the loop filter's input swing can be reduced. Similarly, the swing at the virtual ground of an active integrator can be reduced by connecting it to a negative resistance [8, 9]. This effectively increases the integrator's gain and improves its linearity. However, since the negative resistance is realized by an active circuit, it also produces noise and consumes power. Furthermore, foreground calibration is required to ensure good matching between the negative resistance and the integrator's equivalent input resistance. In comparison, zoom ADCs seem to present a good tradeoff between design complexity, energy efficiency, resolution, and no need for calibration.

However, zoom ADCs also have drawbacks. In order to absorb SAR ADC non-idealities, their fine ΔΣMs are usually designed to provide at least ±1 LSB of over-ranging [2, 4–6]. In the case of a 1-bit ΔΣM, this means that the modulator's DAC must span at least three SAR LSBs, leading to a significant loss of SQNR. Another issue is the leakage of the SAR ADC's quantization noise, to which zoom ADCs, like other MASH ADCs, are susceptible. This is because summing the outputs of the SAR ADC and the ΔΣM tacitly assumes that the signal transfer function (STF) of the latter is exactly unity, which will usually not be the case, especially at high frequencies [6]. These issues can be mitigated by increasing the modulator's OSR or by using a digital noise cancellation filter. But both approaches inevitably increase power consumption [2, 6]. Furthermore, previous zoom ADCs also suffered from limited robustness to out-of-band interferers.

This chapter gives an overview of the evolution of zoom ADC architectures for instrumentation and audio applications that tackle these issues and is organized as follows: first, the system-level design for zoom ADCs is discussed (Sect. 10.2). Different techniques used in recent zoom ADCs for instrumentation and audio applications (1–24 kHz BW) are explained to solve the zoom ADC's drawbacks such as susceptibility to out-of-band interferers (Sect. 10.2.1), loss of SQNR due to over-ranging (Sect. 10.2.2), and SAR quantization noise leakage (Sect. 10.2.3). This is followed by the discussion of challenges in the amplifier design for DT zoom ADCs (Sect. 10.3). Recent CT zoom ADCs are discussed next (Sect. 10.4), with a focus on amplifier nonlinearity (Sect. 10.4.1) and DAC drivers (Sect. 10.4.2), followed by a CT zoom ADC design example (Sect. 10.4.3). This chapter closes with a conclusion and comparison with state-of-the-art ADCs (Sect. 10.5).

## 2 System-Level Design of the Zoom ADC

A dynamic zoom ADC [4], as shown in Fig. 1a, consists of an $N$-bit SAR ADC, which performs a coarse conversion and outputs an $N$-bit code $k$. This digital value

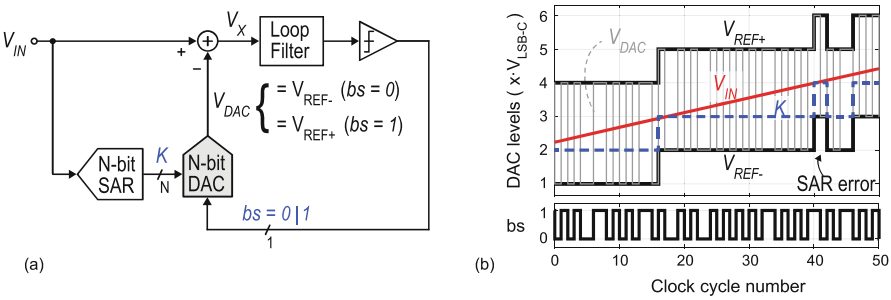


**Fig. 1** (**a**) Simplified block diagram of the dynamic zoom ADC. (**b**) Time-domain waveforms of different signals in the zoom ADC with an over-ranging of $M = 1$

$k$ is then used to determine the high and low references of a fine $\Delta\Sigma$M, respectively, as

$$V_{\mathrm{REF+}} = (k + 1 + M) \bullet V_{\mathrm{LSB,C}} \tag{1}$$

$$V_{\mathrm{REF-}} = (k - M) \bullet V_{\mathrm{LSB,C}} \tag{2}$$

where $V_{\mathrm{LSB,C}}$ is the quantization step size corresponding to the $N$-bit SAR and $M$ is an over-ranging factor. The fine $\Delta\Sigma$M DAC toggles between these references depending on the bitstream output of the comparator (bs), essentially zooming in on the signal, and operating as a conventional 1-bit $\Delta\Sigma$M, but achieving a significantly higher signal-to-quantization noise ratio (SQNR) due to the small step size. Figure 1b shows the resulting signals in the case of $M = 1$.

As compared to one of the first incremental zoom ADCs proposed in [5], the parallel operation of the SAR and fine $\Delta\Sigma$M in a dynamic zoom ADC effectively allows a much higher bandwidth. If $M = 0$, no error can be tolerated in the coarse SAR conversion since a conversion error would lead to the $\Delta\Sigma$M references not straddling the input signal, thus leading to $\Delta\Sigma$M overload. Over-ranging, i.e., making $M > 0$, is used to relax the accuracy requirements of the SAR ADC [4].

As the SAR ADC uses a separate capacitive DAC, its quantization levels will also exhibit some mismatch with respect to those of the main DAC used by the $\Delta\Sigma$M to set the fine references. Any error made by the SAR ADC due to its noise, linearity, and offset will result in an error in the coarse code $k$. Without over-ranging, the overall accuracy of the zoom ADC would, therefore, be limited by both the SAR ADC and $\Delta\Sigma$M DAC. Over-ranging ensures that the fine references of the $\Delta\Sigma$M are still valid for a given input as long as the error in the SAR conversion is below M LSBs. Thus, the SAR ADC does not limit the overall accuracy. This is illustrated in Fig. 1b, where despite the error in $k$, the input remains bounded by the fine references. It must be noted that although over-ranging relaxes the SAR ADC constraints, the main $N$-bit $\Delta\Sigma$ DAC must still be designed to achieve the intended

target linearity. This is enabled by implementing data-weighted averaging (DWA) in the $N$-bit $\Delta\Sigma$ DAC.

The relaxed requirements on the SAR ADC due to over-ranging greatly simplify its design. Furthermore, zooming reduces the swing at the input of the loop filter, relaxing the linearity and driving requirements of the $\Delta\Sigma$M integrators, thus allowing the use of simple energy-efficient inverter-based operational transconductance amplifiers (OTAs).

## 2.1 Asynchronous SAR ADC

The time-domain operation of a dynamic zoom ADC is shown in Fig. 2a, b. The coarse ADC is an $N$-bit synchronous SAR ADC, whose conversion time takes $N$ clock cycles of the DT$\Delta\Sigma$M ($N = 5$ in Fig. 2). The references are set by $k$, which represents the signal's value at the moment of the coarse ADC's sampling $V_{in}(t_{s,C})$. This is used to compare it with the sampled input of the DT$\Delta\Sigma$M at its sampling moment ($t_{s,F}$), which is $V_{in}(t_{s,F})$. In the case of an $N$-bit coarse SAR ADC, the input is sampled at $t_{s,C}$, and the corresponding $k$ is available $N$ cycles later. Assuming $k$ sets the references immediately, the minimum difference $\Delta t = t_{s,F} - t_{s,C}$ is $N$ clock periods. However, this $k$ value will be used for the next $N$ cycles. Thus, the maximum $\Delta t$ would be $2N$ clock cycles. This requires more over-ranging, i.e., $M > 1$, to achieve proper operation, as shown in Fig. 2b. A higher $N$ is desirable to reduce the $\Delta\Sigma$M input range and increase energy efficiency. However, it raises $\Delta t$. As shown in Fig. 2a, when the input signal changes too fast to be tracked by

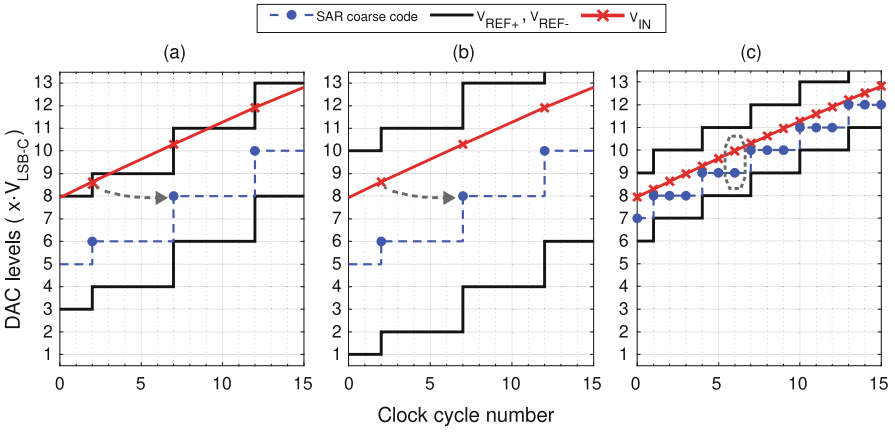


**Fig. 2** Time-domain operation of the dynamic zoom ADC for a fast-changing input. (**a**) Coarse code and corresponding fine reference are updated at every five cycles by a 5-bit SAR ADC for (**a**) $M = 2$ and for (**b**) $M = 4$. (**c**) Fine reference is updated every cycle by a 5-bit asynchronous SAR, with an over-ranging of $M = 1$ [6]

the coarse SAR ADC, it can extend beyond the modulator's stable input range, as in the case of large out-of-band interferers. The duration of the coarse conversion also puts a limit on the maximum full-scale input frequency ($f_{\text{in,max}}$), thereby making the $\Delta\Sigma$M susceptible to overload in the presence of large out-of-band interferer signals. This is because the references of the DT$\Delta\Sigma$M are only updated once every $N$ clock cycles, while the $\Delta\Sigma$M assumes that the signal rests in between these set reference levels between two reference update moments. The stable input range of $\Delta\Sigma$M can be expressed as [4]:

$$f_{\text{in,max}} < \alpha \frac{2M+1}{2N\left(2^N-1\right)\pi} f_s \tag{3}$$

Equation (3) represents the relation of $f_{\text{in,max}}$ to $f_s$, $M$, and $N$, which are parameters of the coarse conversion, and $\alpha$, which defines the topology-dependent stable input range of the $\Delta\Sigma$M and is $\leq 1$. It can be seen that a higher $N$ or a lower $f_s$ reduces $f_{\text{in,max}}$.

An asynchronous SAR ADC is a better alternative, because after being triggered by a clock edge, synchronous to $f_s$, its internal execution of the binary search algorithm is self-timed. In [6], the asynchronous SAR ADC's total conversion time was much less than half a clock cycle, allowing it to update the $\Delta\Sigma$M references every clock cycle as shown in Fig. 2c; hence, $\Delta t$ was $0.5/f_s$. We can express $f_{\text{in,max}}$ in this case as [6]:

$$f_{\text{in,max}} < 2\alpha \frac{2M+1}{\left(2^N-1\right)\pi} f_s \tag{4}$$

The dependency of $f_{\text{in,max}}$ on $N$ is less drastic in (4) compared to (3). It is seen that a synchronous SAR ADC limits $f_{\text{in,max}}$ dramatically. Although this can be alleviated by increasing $M$, or reducing $N$, both would result in increased $\Delta\Sigma$M input swing and quantization noise and therefore degraded energy efficiency. An asynchronous SAR ADC offers higher $f_{\text{in,max}}$ and thus improves the robustness to out-of-band interferers. This allows the use of $M = 1$, as reported in [1–3, 6] and shown in Fig. 2c. This directly reduces the input swing of the $\Delta\Sigma$M and improves its linearity, and thus its energy efficiency, which is usually limited by nonlinearity.

## 2.2 SQNR Recovery

An example waveform for $M = 1$ (minimum over-ranging) is shown in Fig. 3a, when the fine references $V_{\text{REF+}}$ and $V_{\text{REF−}}$ are updated at the sampling rate. For $M = 1$, the DAC of a 1-bit $\Delta\Sigma$M will then span 3-$V_{\text{LSB,C}}$. So even with this minimum over-ranging, the modulator's quantization error will increase by 3×, reducing its SQNR by ~9.5 dB compared to the case with no over-ranging. Although this can be restored by increasing the OSR, it comes at the expense of increased power consumption.

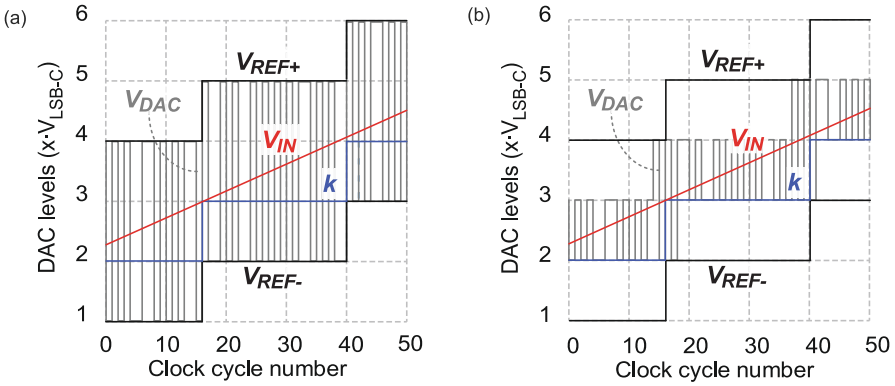


**Fig. 3** SAR output (k) and ΔΣM DAC swings with $M = 1$ for (**a**) a 1b quantizer and (**b**) a 2b quantizer

To recover the lost SQNR and to effectively utilize the two intermediate levels, a 2-bit quantizer can be used, as shown in Fig. 3b [1]. It should be noted that the DAC itself remains unchanged, and so does the data-weighted averaging (DWA) scheme required to obtain high linearity [11]. The resulting reduction in quantization noise enables a corresponding decrease in OSR to achieve the same SQNR, which, in turn, leads to reduced analog and digital power consumption, a significant reduction in comparison to the slightly larger power consumption of the two additional comparators of the 2-bit flash quantizer.

## 2.3 SAR Quantization Noise Leakage

As shown in Fig. 4, a zoom ADC can be modeled as a 0-N MASH ADC by splitting its DAC into two halves, one driven by the SAR ADC and the other driven by the ΔΣM. The overall digital output $Y_{\mathrm{OUT}} = k + Y_{\Delta\Sigma\mathrm{M}}$ can then be expressed as [1]:

$$Y_{\mathrm{OUT}} = V_{\mathrm{IN}}(z) + Q_{\mathrm{SAR}}(z) \bullet (\mathrm{STF} - 1) + Q_{2-\mathrm{bit}} \bullet \mathrm{NTF} \tag{5}$$

where $Q_{\mathrm{SAR}}$ and $Q_{2\text{-bit}}$ represent the quantization noise of the SAR and the ΔΣM quantizer, respectively. As expected, $Q_{2\text{-bit}}$ is shaped by the NTF. However, the cancellation of $Q_{SAR}$ is limited by *STF-1*, which is equal to *-NTF* for a feedforward DT loop filter. Since the quantization noise of a 5-bit ADC is quite tonal, it leaks into the output spectrum of the zoom ADC, referred to as "fuzz" in the literature [6]. The in-band fuzz degrades the SNDR of the ADC and limits its bandwidth.

SAR ADC quantization noise can be reduced by increasing OSR, at the expense of higher power consumption, especially in a switched-capacitor implementation [4]. Alternatively, a digital noise cancellation filter can be used to process $k$ before

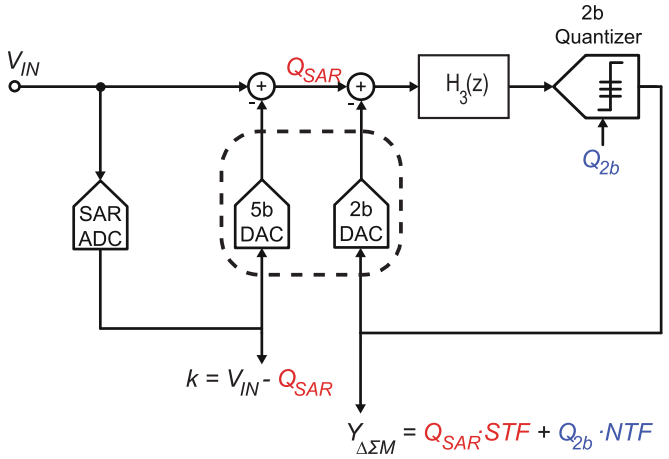


**Fig. 4** Intuitive block diagram of the coarse-fine operation in the *N*-bit DAC

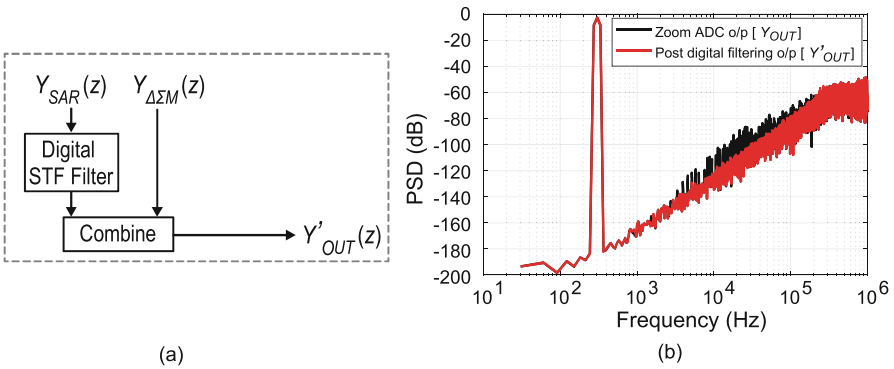


**Fig. 5** (**a**) Fuzz filtering using a digitally matched STF filter. (**b**) The resulting zoom ADC output spectrum

combining it with $Y_{\Delta\Sigma M}$ [6], as in MASH architectures. As shown in Fig. 5a, this involves passing the output code of the SAR ADC ($k$) through a digital filter matched to the STF before combining it with the bitstream output. This results in almost perfect fuzz suppression, as shown in Fig. 5b. However, the required digital STF filter increases the complexity and power consumption. Furthermore, any mismatch between the analog STF and the reconstruction filter will degrade the fuzz suppression performance, therefore likely requiring calibration.

In [1], a low-power fuzz cancellation technique is proposed. It is based on the observation that, from (5), $Q_{SAR}$ leakage can be prevented by ensuring that the modulator has a unity STF. One way of doing this is by implementing an input feedforward path [12]. As shown in Fig. 4, the modulator's input is the residue of the SAR ADC. Thus, this can be extracted and added to the input of

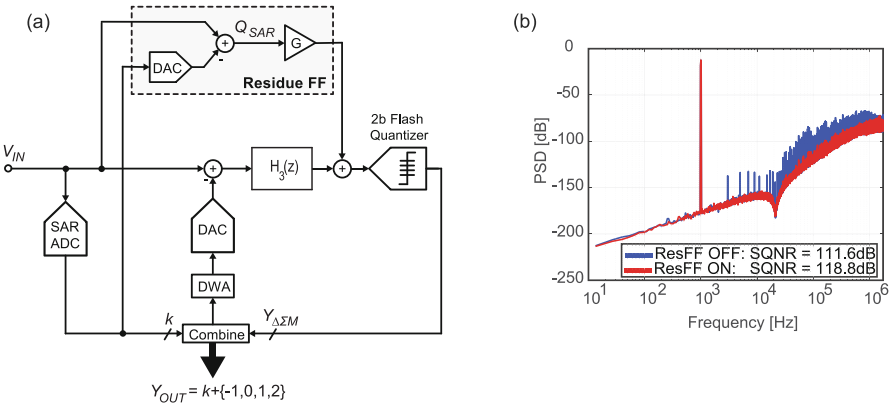


**Fig. 6** (**a**) Block diagram of a zoom ADC with third-order ΔΣM with 2-bit quantizer, 5-bit SAR ADC, and residue feedforward [1]; (**b**) Output spectrum of the zoom ADC

the modulator's quantizer. Rather than extracting the small residue at the input of the SAR ADC's comparator, which would require complex circuitry, a simpler approach is to generate a replica. This can be done by subtracting the output of a replica of the SAR DAC from the input signal, as shown in Fig. 6a. Since the 2-bit quantizer of the ΔΣM has a well-defined gain ($K_q$), the output of the residue feedforward path is scaled by a factor $G = 1/K_q$ for optimal fuzz suppression.

Although the fuzz reduction techniques proposed in [1, 6] show excellent fuzz suppression in simulations, measurement results show that the amount of fuzz suppression is limited by the mismatch between the primary and the cancellation paths. Another technique proposed in [3] uses a 4-bit passive noise-shaping SAR (NS SAR) [13] as a coarse ADC, which effectively decorrelates and shapes the tonal quantization noise of the basic SAR ADC, and thus reduces the fuzz enough to obtain a thermal noise-limited output spectrum.

At the end of the SAR conversion cycle, the residue signal which is readily available on SAR DAC is extracted with a gain of 2 and then passively integrated with a gain of 0.4 to achieve first-order noise shaping (NS) in the SAR ADC. Passive integration preserves the energy efficiency of the SAR ADC while improving its SNDR significantly. This modest NS is sufficient to decorrelate and suppress the tonal quantization noise of the 4-bit SAR ADC to enable a thermal noise-limited output spectrum for the zoom ADC. The simulated output spectrum of the 4-bit noise-shaping SAR ADC is shown in Fig. 7b; it shows the suppression of the tonal quantization noise of the SAR ADC (~9 dB). The output spectrum of a zoom ADC with a 4-bit NS SAR and a third-order CIFF loop filter with a notch at 19 kHz is shown in Fig. 8 [3]. It is shown that the improvement in SQNR is ~7 dB while only using four additional capacitors, a few switches, and digital logic, without requiring any calibration.

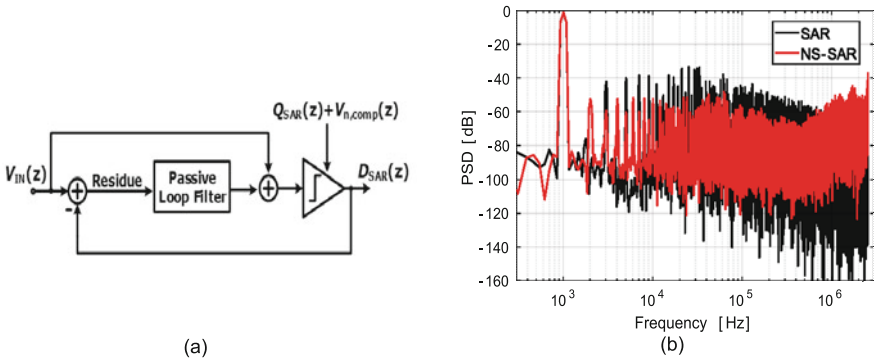


**Fig. 7** (**a**) Block diagram of 4-bit noise-shaping SAR ADC [3] and (**b**) output spectrum of the noise-shaping SAR ADC

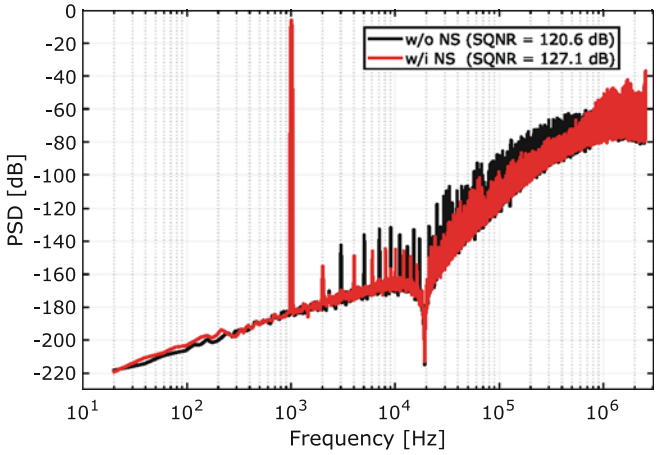


**Fig. 8** Output spectrum of a zoom ADC with third-order loop filter and 4-bit SAR ADC w/i and w/o noise shaping [3]

## 3 Amplifiers in DT Zoom ADCs

Amplifiers in switched-capacitor integrators for high-resolution ADCs require fast settling, low thermal and 1/*f* noise, and excellent energy efficiency. This sub-section discusses the different amplifiers that have been used in DT zoom ADCs as well as the circuit techniques (auto-zero, CDS, and chopping) needed to meet these requirements.

A pseudo-differential inverter-based OTA is used in [4] for its energy efficiency. Auto-zeroing is used to reduce the effect of offset and 1/f noise, whereas differential sampling is used to improve the overall CMRR. To mitigate the effect of PVT variations, a dynamic biasing scheme for inverter-based OTAs is used for the first

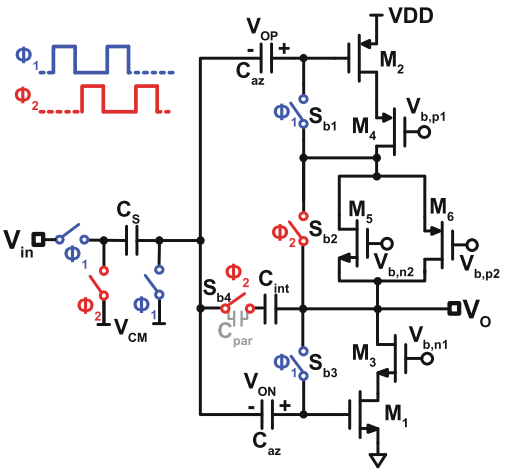


**Fig. 9** Proposed inverter-based integrator with auto-zeroing

integrator of a zoom ADC in [4], as shown in Fig. 9. Instead of switching the floating current source through cascode transistors [5], switches $S_{b1-3}$ are introduced. During the sampling phase $\varphi_1$, diode connections are established around the input transistors ($M_{1-2}$) via $S_{b1}$ and $S_{b3}$, and the floating current source ($M_{5-6}$) forces the same bias current (125 $\mu$A) through the input and cascode ($M_{3-4}$) transistors. At the same time, the bias voltages as well as the offset and the 1/*f* noise are sampled on the auto-zeroing capacitors $C_{az}$ (2 pF each). In the integration phase $\varphi_2$, diode connections are broken by opening the switches $S_{b1}$ and $S_{b3}$, and the floating current source consisting of $M_5$ and $M_6$ is simply bypassed by $S_{b2}$. Since there is no switching capacitive load to the biasing circuit, its power consumption can be minimized. Furthermore, the proposed biasing scheme results in a much more compact design by eliminating two large cascode transistors. A simple SC common-mode feedback (CMFB) circuit as in [14] is adequate to avoid output common-mode drift in the pseudo-differential implementation. Though very effective for *1/f* noise and offset suppression, this technique uses relatively large auto-zero capacitors to fulfill the noise requirements.

In [6], a correlated double sampling (CDS) scheme is implemented in a second-order zoom ADC to suppress the offset of $OTA_1$ [15], as shown in Fig. 10. A simple current-starved OTA with cascodes is used as the first integrator for its high energy efficiency, DC gain, and PSRR, as shown in Fig. 10. While the input is shorted to the outer plate of $C_S$ during phase $\varphi_1$, $OTA_1$ is connected in unity feedback and samples its offset and 1/*f* noise on the other plate. During $\varphi_2$, this offset is effectively canceled, while the input is integrated. Due to the finite DC gain of $OTA_1$, the offset sampled at the virtual ground node due to unity feedback is $V_{OFF} \cdot A/(1 + A)$. As a result, an input-referred offset of approximately $V_{OFF}/A$ remains. A typical offset of a few millivolts will be suppressed to a few microvolts if the OTA gain is around 60 dB. Compared to [4], this architecture omits the use of large auto-zeroing caps while achieving similar levels of 1/*f* noise and offset suppression. However, due

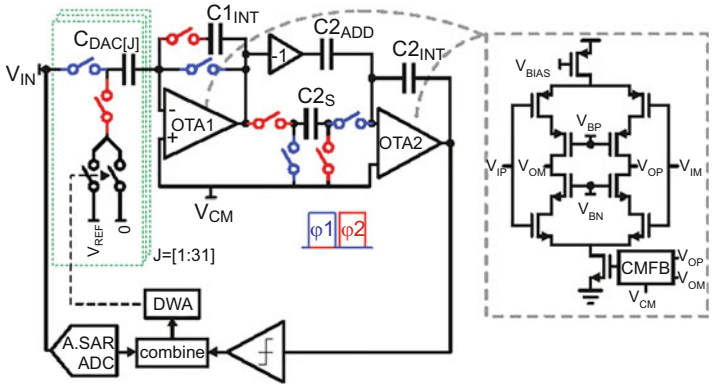


**Fig. 10** Simplified single-ended block diagram of a second-order zoom ADC [6]

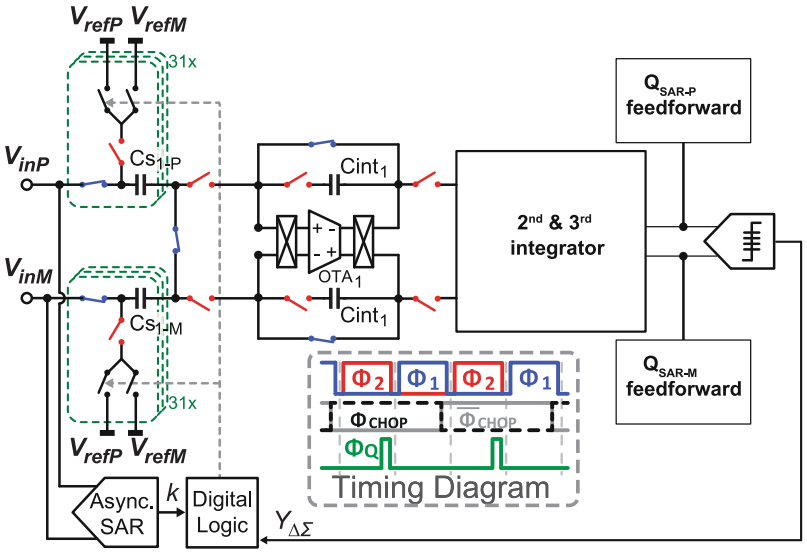


**Fig. 11** The first integrator of a zoom ADC with third-order loop filter as proposed in [1]

to its pseudo-differential sampling operation, its CMRR is limited compared to the fully differential sampling used in [4].

To improve CMRR and reduce area, while still reducing $1/f$ noise and offset, [1] uses chopping and differential sampling, as shown in Fig. 11. The input is sampled using a fully differential sampling network. The sampling switches are bootstrapped to maintain high linearity [16], and thick oxide switches are used in the bootstrapping circuitry, thereby reducing complexity. The first-stage OTA is similar to the one used in Fig. 10 [6].

While the input is being tracked during phase $\varphi_1$, $OTA_1$ is configured in unity feedback and is disconnected from the loop filter. At the end of $\varphi_1$, the input is sampled onto $C_S$, whereas $OTA_1$, having had enough time to settle, is chopped [15]. Chopping $OTA_1$ while it is disconnected from the loop filter prevents chopping artifacts from coupling to the input signal. Since the chopper switches are connected to the input pairs of $OTA_1$, they are quite large (31× minimum size) to minimize their impact on OTA settling time and noise. The noise contributed by the output chopper switches is significantly lower, and so these are minimum-size devices.

## 4 Continuous-Time Zoom ADCs

Previously discussed zoom ADC designs employed switched-capacitor (SC) front-ends that required input and reference drivers capable of delivering large signal-dependent peak currents. For high linearity applications (>100 dB), the power dissipation of the drivers for DTΔΣMs will be higher than that of the ADC itself due to the large sampling capacitors ($C_s$), in some cases necessitating on-chip buffers, at the expense of chip area and power consumption [17]. It is well known that ADCs based on continuous-time delta-sigma modulators (CTΔΣMs) generally do not require anti-aliasing filters, while their resistive input impedance imposes relaxed requirements for the input driver [17], as illustrated in Fig. 12.

In contrast to SC integrators, in which charge is transferred in exponentially decaying pulses, and only the result at the end of the integration period matters, the charge transfer in a CT integrator is a continuous process. Therefore, the linearity of this process depends on the linearity of the integrator's amplifier. This subchapter will describe two different amplifier architectures that were used in zoom ADCs [2, 3] to reach high linearity.

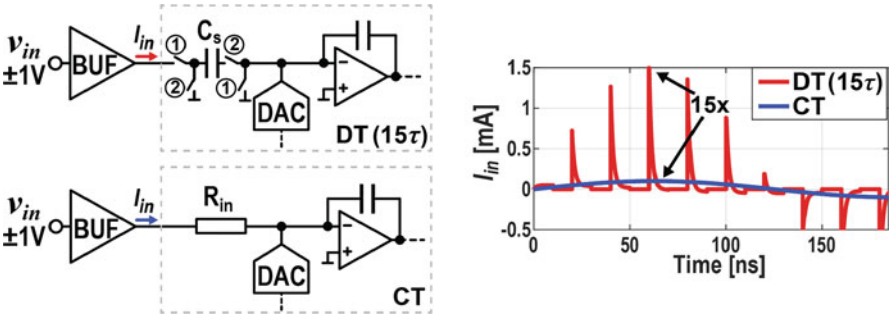


**Fig. 12** Block diagram and buffer current output of a DT and CT zoom ADC

## 4.1 Amplifiers in CT Zoom ADCs

In a CT loop filter, the first integrator's linearity is the most critical. This is often realized with a fully differential amplifier (Fig. 13a). However, the linearity of a fully differential amplifier is worse than that of its pseudo-differential counterpart (Fig. 13b). This is because the fixed tail current makes the amplifier's transconductance ($gm$) compressive. Simulations were made to compare the linearity of the proposed amplifier with that of its fully differential counterpart. Both the amplifiers are biased in weak inversion, have the same $I_{\text{bias}}$ and device sizing, and thus have the same power consumption and $gm$. In Fig. 13, the nonlinear components of their differential output currents are shown after being normalized to the tail current ($I_{\text{bias}}$). It can be seen that the proposed pseudo-differential amplifier is much more linear than its fully differential counterpart. It requires 2× less power for the same linearity. However, removing the tail current source makes a pseudo-differential amplifier difficult to bias robustly. The dynamic biasing techniques proposed for SC designs [4, 18, 19] are not suitable for CT operation. Furthermore, pseudo-differential amplifiers usually suffer from poor power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) [4].

The proposed pseudo-differential amplifier is shown in Fig. 14. Chopping is often employed to reduce $1/f$ noise in audio CTΔΣMs. In [2], a capacitively coupled inverter-based pseudo-differential amplifier incorporating chopping is proposed. As shown in Fig. 14, it uses ac coupling capacitances ($C_c$) and large resistors ($R_b = 3\ \text{M}\Omega$) to bias its input transistors at the desired current levels and simultaneously block input common-mode variations. The biasing voltages ($V_{\text{bni}}$, $V_{\text{bpi}}$, $V_{\text{bnc}}$, and $V_{\text{bpc}}$) are generated by a constant-$gm$ biasing circuit.

The combination of $R_b$ and $C_c$ behaves like a high-pass input filter. Setting its corner frequency below the audio band (<20 Hz) would require extremely large resistors and/or capacitors making this approach difficult to integrate. Instead, choppers are used to up-modulate audio signals to $f_{\text{chop}}$ before this filter and then demodulate them back into an output DC. In this way, the high-pass filter's corner frequency only has to be lower than $f_{\text{chop}}$. To avoid folding down the quantization

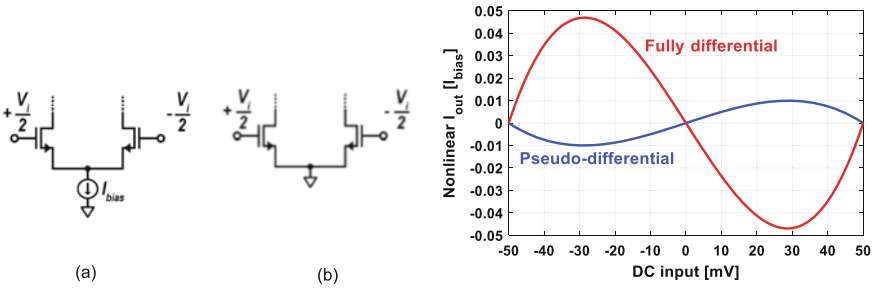


**Fig. 13** Nonlinear components of $I_{\text{out}}$ for a fully differential (**a**) and a pseudo-differential (**b**) amplifier

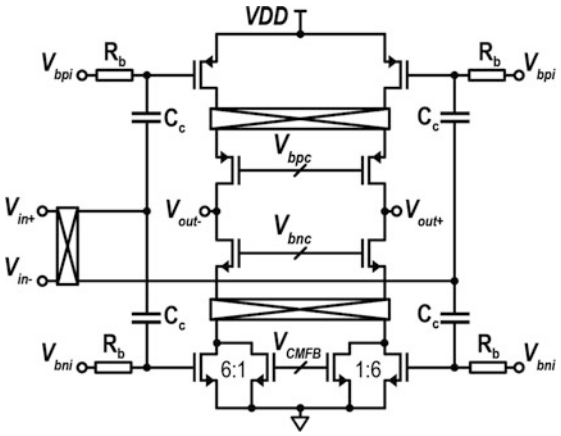


**Fig. 14** Simplified schematic of the proposed amplifier in [2]

noise present at the virtual ground node, the choppers are driven at the sampling frequency ($f_{\text{chop}} = f_s$) [7, 20]. Since the output choppers are placed in a high bandwidth node between the input devices and the cascodes, the DC gain reduction due to these is negligible.

For linearity, the coupling capacitors ($C_c = 2$ pF) are implemented as metal fringe capacitors and designed to be much larger than the gate capacitances of the input transistors to minimize signal attenuation. The polysilicon biasing resistors ($Rb = 3\ \text{M}\Omega$) are chosen to ensure that the high-pass corner frequency is much less than $f_s$. In the layout, $R_b$ is placed under $C_c$ to reduce the total area of the four $R_b$–$C_c$ pairs to 0.01 mm$^2$.

The NMOS input transistors are split in a 6:1 ratio, with the smaller branch being used for common-mode feedback (CMFB). A CT CMFB circuit is used to sense and stabilize the amplifier's output common-mode voltage [18]. The input and output choppers also chop the offset and low-frequency noise contributed by the CMFB loop itself.

The total power consumption of the amplifier is 205 $\mu$W, including the chopper drivers, biasing, and CMFB circuits. Its nominal and minimum DC gains are 60 and 55 dB, respectively, over process, voltage, and temperature (PVT) (−55 °C–150 °C and 1.6–2 V). The amplifier's simulated CMRR is greater than 70 dB up to 1 kHz. Its simulated PSRR is greater than 100 dB up to 1 kHz and greater than 50 dB for higher frequencies due to chopping.

To improve the linearity compared to [2] (Fig. 15a) and, in turn, the energy efficiency, the zoom ADC in [3] implements the tail resistor linearization technique in the OTA [21] (Fig. 15b). This preserves all the merits of the pseudo-differential (PD) OTA while significantly improving its linearity and thus reducing its power.

Instead of having a zero tail impedance, as shown in the PD OTA, which gives its *gm* an expanding characteristic and makes it more linear than the conventional OTA, the TRL OTA sets an optimum tail impedance ($R_{\text{tail}}$). With the optimum $R_{\text{tail}}$, the dominant third-order nonlinearity of the OTA (when the input transistors are biased

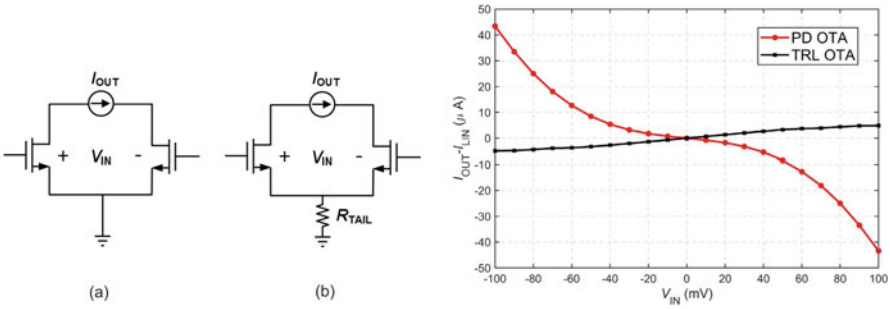


**Fig. 15** Linearity comparison between pseudo-differential OTA and TRL OTA

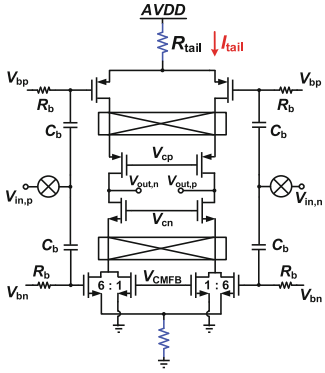


**Fig. 16** Tail resistor-linearized OTA

in weak or moderate inversion) can be canceled, thereby improving its linearity significantly.

To illustrate this, the output characteristics ($I_{out}$-$I_{lin}$ vs. $V_{in}$) of the PD OTA and the TRL OTA are biased in weak inversion with the same transistor sizes, and $I_{tail}$ (112 μA) is plotted in Fig. 15. The value of $R_{tail}$ to maximize the linearity of the TRL OTA is calculated using (6) [21] and is further optimized based on the simulation results.

$$R_{\text{tail}} = \frac{\eta V_T}{2I_{\text{tail}}} \tag{6}$$

In Eq. (6), $I_{tail}$ is the bias current of the amplifier, $V_T$ is the thermal voltage, and $\eta$ is a process-dependent ideality factor. For the same $I_{tail}$ and $g_m$, the TRL OTA is ~17× more linear than the PD OTA as shown in Fig. 15. This allows for a significant reduction in $I_{tail}$ and allows it to be determined solely by the thermal noise considerations. The schematic of the tail resistor-linearized (TRL) OTA is shown in Fig. 16.

### 4.2 DAC Drivers

The DAC of the CT zoom ADC is one of its most critical blocks, as it directly impacts its total input-referred noise, total harmonic distortion (THD), and clock jitter sensitivity. An NRZ DAC is preferred for high energy efficiency and low jitter sensitivity. The input voltage is converted to a current ($I_{\text{in}}$) via $R_{\text{in}}$, as shown in Fig. 17. After subtracting the DAC current ($I_{\text{DAC}}$), their difference ($I_{\text{OTA}}$) is then integrated. The maximum value of $I_{\text{OTA}}$ defines the output current requirements of the OTA and hence its power consumption. The maximum input current ($I_{\text{in,max}}$) for a sinusoidal input with amplitude $V_{\text{in,max}}$ is:

$$I_{\text{in,max}} = \frac{V_{\text{in,max}}}{R_{\text{in}}}$$

Figure 18 shows $I_{\text{OTA}}$ and $I_{\text{DAC}}$ for NRZ and RZ DACs for a zoom ADC based on a 3-bit coarse ADC. For an NRZ DAC, the difference between $I_{\text{in}}$ and $I_{\text{DAC}}$ is constant and decreases as the resolution of the coarse DAC is increased. For an RZ DAC, however, this difference is much larger, since $I_{\text{DAC}}$ is sometimes zero, and so $I_{\text{OTA}}$ should be as large as $I_{\text{in,max}}$.

There are two ways to implement a two-level NRZ DAC: as a current DAC (I-DAC) or as an R-DAC. However, an I-DAC will generate extra distortion due to the interaction between the nonlinear output impedance of its current sources and the voltage swing at the virtual ground of the OTA. An R-DAC is not only more linear, but it also has lower thermal and 1/*f* noise [22]. Thus, an R-DAC is used in [2, 3].

ISI refers to the signal-dependent errors that occur at code transitions due to the mismatch between finite rise/fall times of the currents generated by the unit elements of the R-DAC. The use of DWA makes this problem even worse because it increases the number of unit element transitions in the DAC and introduces even-order distortion [23]. In these works [2, 3], a novel ISI reduction technique is proposed to solve this problem.

In the output of the differential R-DAC unit element shown in Fig. 19, there are four different transition edges: $t_{\text{rp}}$, $t_{\text{rn}}$, $t_{\text{fp}}$, and $t_{\text{fn}}$. If the total amount of positive and negative DAC output currents within one period would match, there would be no nonlinear ISI error [23]. One approach to achieve this is to match a rising edge

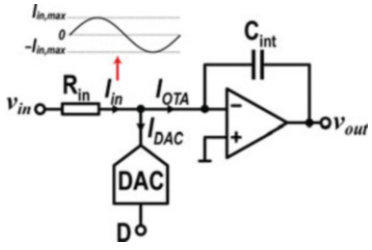


**Fig. 17** $I_{\text{DAC}}$ and $I_{\text{OTA}}$ for NRZ and RZ DACs

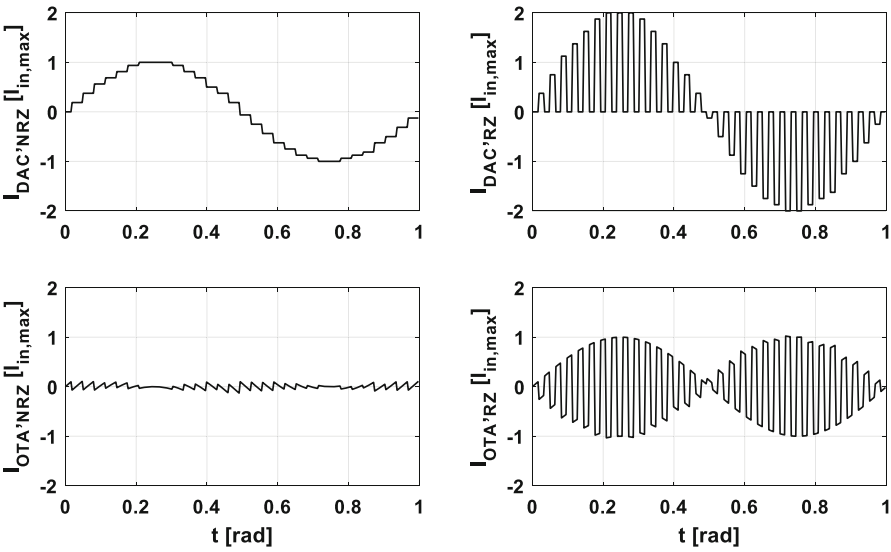


**Fig. 18** $I_{DAC}$ and $I_{OTA}$ for NRZ and RZ DACs

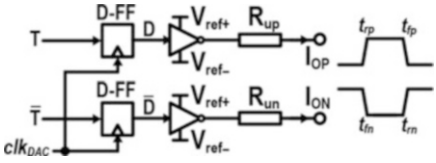


**Fig. 19** Schematic of an R-DAC cell

with its corresponding falling edge (match $t_{rp}$ and $t_{fn}$, and match $t_{rn}$ and $t_{fp}$) [7, 24]. However, this is hard to guarantee in practice since the speed of the rising edges is set by PMOS drivers, while the speed of the falling edges is set by NMOS drivers. Thus, background calibration is often necessary for this approach [7, 24].

Alternatively, we note that to avoid ISI, it is only necessary to match the rising and falling edges of the positive and the negative half DACs (match $t_{rp}$ and $t_{rn}$, and match $t_{fp}$ and $t_{fn}$). This is comparatively easy to achieve because the edges that need to be matched are generated by the same type of devices. However, the positive and the negative DAC unit resistors also need to match, as they also influence the resulting rise and fall times. Simulations indicated that the 1% matching needed for low DWA in-band noise (IBN) is also more than enough to achieve $< -120$ dB HD2. The positive and negative half DACs should then be laid out next to each other. Noting that the ON resistances of the DAC switches are much smaller than $R_{up}$ and $R_{un}$, the matching requirements on the driver inverters can be relaxed to 5%. The switch driving signal asymmetry, which is also a source of ISI error, is reduced by using two separate flip-flops to drive $D$ and $\overline{D}$, as shown in Fig. 19.

### 4.3 Example: A CT Zoom ADC with a Coarse NS SAR

A CT zoom ADC with 106.6 dB $\text{SNDR}_{\text{MAX}}$ in a 24 kHz BW is proposed in [3]. To reach a thermal noise-limited design, the target SQNR of 120 dB SQNR is reached by using a 4-bit SAR ADC with a third-order $\Delta\Sigma$M with local feedback and a 2-bit quantizer (Sect. 10.2.2), as simulated in Fig. 20.

The proposed CT zoom ADC is shown in Fig. 21. Since this zoom ADC uses a 4-bit coarse ADC, the tonal quantization noise of the SAR ADC and its internal swings will increase as compared to previous zoom ADCs with a 5-bit coarse ADC [2]; this puts more stringent requirements on the linearity of the individual OTAs. Through the use of analog techniques such as passive noise shaping in the coarse SAR ADC (Sect. 10.2.3) and tail resistor linearization in the $\text{OTA}_1$ (Sect. 10.4.1), high linearity is achieved without compromising energy efficiency. To reduce the effect of ISI, DAC drivers with matched rise and fall times are used (Sect. 10.4.2).

For a 1 kHz, −0.35 dBFS input signal, the measured SNDR and THD of the 4-bit SAR ADC with NS "OFF" are 30.3 dB and − 30.4 dB, respectively (Fig. 22). With NS "ON," its in-band quantization noise is suppressed by about 9.5 dB, while its SNDR and THD improve by 14.5 dB and 14.6 dB, respectively. Turning NS "ON" effectively suppresses in-band fuzz and improves the SNDR and THD of the zoom ADC by 1.2 dB and 5.5 dB, respectively. The tone at $f_s/2$ with NS "ON" comes from the SAR ADC as it toggles predominately between two levels while resolving the residue. The proposed ADC achieves a competitive Schreier figure of merit ($\text{FOM}_\text{S}$) of 183.4 dB and $\text{FOM}_{\text{SNDR}}$ of 182.7 dB, together with the lowest in-band noise and distortion spectral density (NDSD = −150.4 dBFS/Hz) among state-of-the-art audio ADCs.

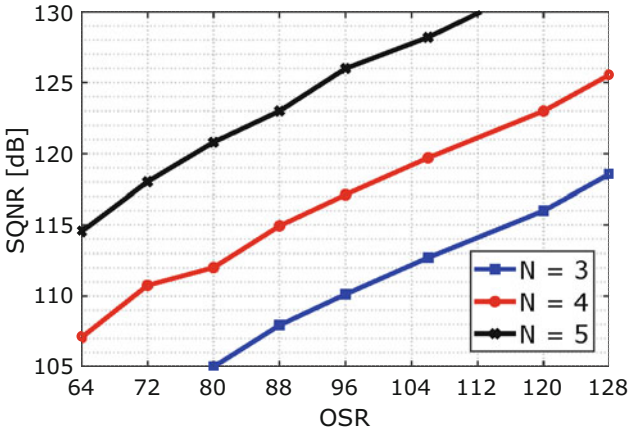


**Fig. 20** OSR vs. SQNR for a third-order CT zoom ADC with notch and 2-bit quantizer

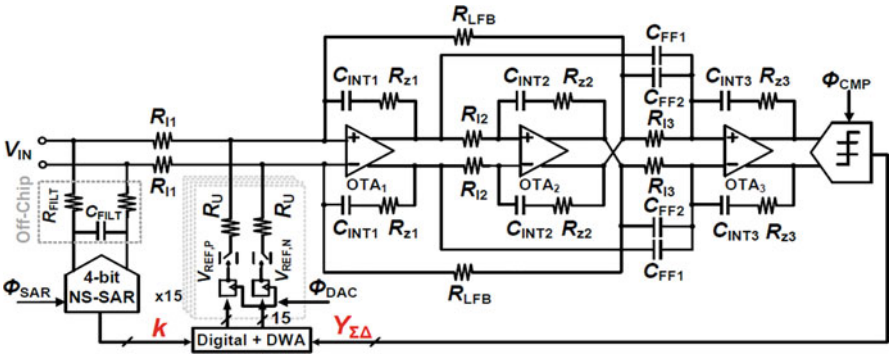


**Fig. 21** Simplified schematic of the proposed CT zoom ADC

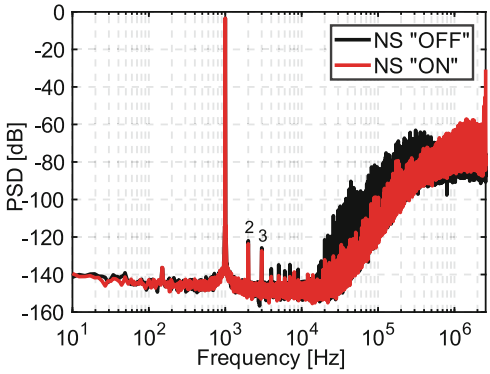


**Fig. 22** Measured PSD of zoom ADC ($2^{21}$ points, 8 averages, Blackman-Harris window)

## 5 Conclusions

This book chapter describes the evolution of zoom ADCs for high-resolution instrumentation and audio applications. The use of an asynchronous SAR ADC as a coarse converter drastically improves the immunity to out-of-band interferers while keeping the over-ranging at $\pm 1$ LSB. The use of a 2-bit flash quantizer in the fine $\Delta\Sigma$M fully recovers the SQNR loss (~9 dB) due to the use of 1 LSB over-ranging and improves the immunity to out-of-band interferers while keeping the benefits of over-ranging such as relaxed specifications for the SAR ADC intact. To improve the impact of fuzz on linearity, techniques that rely on the suppression of the SAR quantization noise, such as an NS SAR, are preferred over techniques that rely on cancellation, due to their low power, low area, and tolerance to circuit mismatch. For the DT zoom ADCs, differential sampling, together with chopping OTA$_1$, is preferred over auto-zeroing and CDS, due to its benefits in terms of CMRR, low offset, and low 1/*f* noise. CT loop filters for high-resolution zoom ADCs improve

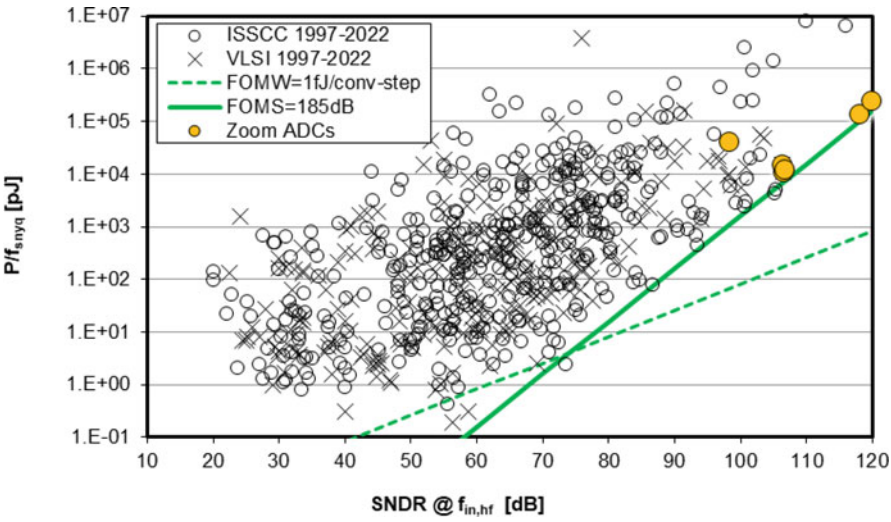


**Fig. 23** ADC survey

the requirements for the input and reference buffers due to their resistive load and are preferred over DT loop filters. A tail resistor-linearized OTA improves the linearity of the first-stage integrator by nearly 17× as compared to a tail current source, allowing it to be biased solely for noise, and thus improves the energy efficiency of the ADC. Matching rise and fall times in the DAC drivers improves the overall linearity of the system.

These advances in zoom ADCs lead to high resolution at very high energy efficiency (Schreier DR and SNDR FoMs >180 dB) as shown in Fig. 23 and Table 1 and make them well suited for instrumentation and audio applications. In recent publications, however, other architectures reach better energy efficiency and lower area, at similar resolution and bandwidth. So, what future approaches can be taken to evolve the zoom ADC towards even higher performance? Is a combination of architectures the key, or could a more "digital" zoom ADC lead to improved performance in advanced technology nodes? Only silicon will tell us the answer to these questions.

**Table 1** Table of comparison

| | [3] | [25] | [26] | [27] | [1] | [8] | [2] | [6] | [4] |
|---|---|---|---|---|---|---|---|---|---|
| Architecture | CT Zoom | DT PPD | CT | CT FIRDAC | DT Zoom | CT 3-level | CT Zoom | DT Zoom | DT zoom |
| Tech (nm) | 160 | 180 | 28 | 65 | 160 | 65 | 160 | 160 | 160 |
| Area ($mm^2$) | 0.36 | 0.03 | 0.07 | 0.39 | 0.27 | 0.28 | 0.27 | 0.25 | 0.16 |
| Supply (V) | 1.8 | 1.8/1.1 | 1.8/1.0 | 1.2 | 1.8 | 1.2 | 1.8 | 1.8 | 1.8 |
| Power ($\mu$W) | 590 | 203.5 | 116 | 139 | 440 | 134 | 618 | 280 | 1120 |
| $f_s$ (MHz) | 5.12 | 5.80 | 6.144 | 7.2 | 3.5 | 8 | 5.12 | 2 | 11.29 |
| BW (kHz) | 24 | 20 | 24 | 24 | 20 | 24 | 20 | 1 | 20 |
| $SNR_{max}$ (dB) | 107.2 | 106.7 | 100.7 | 102.0 | 107.5 | 101.0 | 108.1 | 119.1 | 106 |
| $SNDR_{max}$ (dB) | 106.6 | 105.4 | 100.6 | 100.9 | 106.5 | 99.4 | 106.4 | 118.1 | 103 |
| DR (dB) | 107.3 | 108.8 | 104.4 | 104.8 | 109.8 | 103.5 | 108.5 | 120.3 | 109 |
| $FoM_{SNDR}$[a] (dB) | 182.7 | 185.3 | 183.7 | 183.3 | 183.1 | 181.9 | 181.5 | 183.6 | 175.5 |
| $FoM_S$[b] (dB) | 183.4 | 188.7 | 187.5 | 187.2 | 186.4 | 186.0 | 183.6 | 185.6 | 181.5 |

[a]$FoM_{SNDR} = SNDR + 10\log_{10}(BW/Power)$; [b]$FoM_S = DR + 10\log_{10}(BW/Power)$

## References


1. E. Eland, S. Karmakar, B. Gönen, V.R. Veldhoven, K. Makinwa, A 440-μW, 109.8-dB DR, 106.5-dB SNDR discrete-time zoom ADC with a 20-kHz BW. IEEE J. Solid State Circuits **56**(4), 1–2 (2021)
2. B. Gönen, S. Karmakar, V.R. Veldhoven, K. Makinwa, A continuous-time zoom ADC for low-power audio applications. *IEEE Journal of Solid-State Circuits* **55**(4) (2020)
3. S. Mehrotra, E. Eland, S. Karmakar, A. Liu, B. Gönen, V.R. Veldhoven, K. Makinwa, *A 590 μW, 106.6 dB SNDR, 24 kHz BW continuous-time zoom ADC with a noise-shaping 4-bit SAR ADC* (ESSCIRC Conference 2022 – 48th European Solid-State Circuits Conference (ESSCIRC), Milan, 2022)
4. B. Gönen, F. Sebastiano, R. Quan, V.R. Veldhoven, K. Makinwa, A dynamic zoom ADC with 109-dB DR for audio applications. IEEE J. Solid-State Circuits **52**(6) (2017)
5. Y. Chae, K. Souri, K. Makinwa, A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset. IEEE J. Solid-State Circuits **48**(12) (2013)
6. S. Karmakar, B. Gönen, F. Sebastiano, V.R. Veldhoven, K. Makinwa, A 280 μW dynamic zoom ADC with 120 dB DR and 118 dB SNDR in 1 kHz BW. IEEE J. Solid-State Circuits **53**(12) (2018)
7. S. Billa, A. Sukumaran, S. Pavan, Analysis and design of continuous-time delta–sigma converters incorporating chopping. IEEE J. Solid State Circuits **52**(9), 2350–2361 (2017)
8. M. Jang, C. Lee, Y. Chae, *A 134 μW 24 kHz-BW 103.5db-dr ct ΔΣ modulator with chopped negative-R and tri-level fir DAC* (IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, 2020)
9. M. Jang, C. Lee, Y. Chae, Analysis and design of low-power continuous-time delta-sigma modulator using negative-R assisted integrator. IEEE J. Solid State Circuits **54**(1), 277–287 (2019)
10. A. Sukumaran, S. Pavan, Low power design techniques for single-bit audio continuous-time delta sigma ADCs using FIR feedback. IEEE J. Solid State Circuits **49**(11), 2515–2525 (2014)
11. R. Baird, T. Fiez, Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging. IEEE Trans. Circuits Syst. I, Reg. Papers **42**(12), 753–762 (1995)
12. J. Silva, U. Moon, J. Steensgaard, G.C. Temes, Wideband lowdistortion. IET Electron. Lett **37**(12), 737–738 (2001)
13. Y.-Z. Lin, C.-Y. Lin, S.-C. Tsou, C.-H. Tsai, C.-H. Lu, *20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC With Passive Signal-Residue Summation in 14nm FinFET* (2019 IEEE International Solid-State Circuits Conference – (ISSCC), 2019)
14. Y. Chae, G. Han, Low voltage, low power, inverter-based switched-switched capacitor. IEEE J. Solid State Circuits **44**(2), 458–472 (2009)
15. C. Enz, G. Temes, Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization. Proc. IEEE **84**(11), 1584–1614 (1996)
16. A. Abo, P. Gray, A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter. IEEE J. Solid State Circuits **34**(5), 599–606 (1999)
17. K. Nguyen, R. Adams, K. Sweetland, H. Chen, A 106-dB SNR hybrid oversampling analog-to-digital converter for digital audio. IEEE J. Solid State Circuits **40**(12), 2408–2415 (2005)
18. M.S. Akter, R. Sehgal, F. Goes, K.A.A. Makinwa, K. Bult, A 66-dB SNDR pipelined split-ADC in 40-nm CMOS using a class-AB residue amplifier. IEEE J. Solid State Circuits **53**(10), 2939–2950 (2018)
19. S. Lee, W. Jo, S. Song, Y. Chae, A 300-μW audio ΔΣ modulator with 100.5-dB DR using dynamic bias inverter. IEEE Trans. Circuits Syst. I Reg. Papers **63**(11), 1866–1875 (2016)
20. H. Jiang, B. Gönen, K.A.A. Makinwa, S. Nihitanov, *Chopping in continuous-time sigma-delta modulators* (Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2017), pp. 1–4
21. S. Pan, K.A.A. Makinwa, A 10 fJ·K$^2$ Wheatstone bridge temperature sensor with a tail-resistor-linearized OTA. IEEE J. Solid State Circuits **56**(2), 501–510 (2021)

22. P. Shettigar, S. Pavan, Design techniques for wideband single-bit continuous-time $\Delta\Sigma$ modulators with FIR feedback DACs. IEEE J. Solid State Circuits **47**(12), 2865–2879 (2012)
23. L. Risbo, R. Hezar, B. Kelleci, H. Kiper, M. Fares, Digital approaches to ISI-mitigation in high-resolution oversampled multi-level D/a converters. IEEE J. Solid State Circuits **46**(12), 2892–2903 (2011)
24. T. He, M. Ashburn, S. Ho, Y. Zhang, G. Temes, A 50 MHz-BW continuous-time $\Delta\Sigma$ ADC with dynamic error correction achieving 79.8 dB SNDR and 95.2 dB SFDR. IEEE ISSCC Dig. Tech. Papers, 230–232 (2018)
25. C.Y. Lee, U.-K. Moon, *A 0.0375mm2 203.5$\mu$W 108.8dB DR DT single-loop DSM audio ADC using a single-ended ring-amplifier-based integrator in 180nm CMOS* (2022 IEEE International Solid-State Circuits Conference (ISSCC), 2022), pp. 412–414
26. C. Lo, J. Lee, Y. Lim, Y. Yoon, H. Hwang, J. Lee, M. Choi, M. Lee, S. Oh, J. Lee, *A 116$\mu$ W 104.4dB-DR 100.6dB-SNDR CT $\Delta\sum$ audio ADC using tri-level current-steering DAC with gate-leakage compensated off-transistor-based bias noise filter* (2021 IEEE International Solid-State Circuits Conference (ISSCC), 2021), pp. 164–166
27. S. Mondal, O. Ghadami, D.A. Hall, *A 139 $\mu$ W 104.8dB-DR 24kHz-BW CT $\Delta\Sigma$M with chopped AC-coupled OTA-stacking and FIR DACs* (2021 IEEE International Solid-State Circuits Conference (ISSCC), 2021), pp. 166–168