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Ibrahim, Tariq; Beikmirza, Mohammadreza; Alavi, Morteza S.; de Vreede, Leo

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A fully passive harmonic rejection quadrature mixer for TX observation with 20 dBm OIP3 and 800 MHz IF bandwidth

Tariq Ibrahim , Mohammadreza Beikmirza, Morteza S. Alavi and Leo de Vreede

Department of Microelectronics, Faculty of Electrical Engineering, Mathematics & Computer Science, Delft University of Technology, Delft, Zuid-Holland, The Netherlands

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Corresponding author: Tariq Ibrahim;

Email: t.ibrahim-2@tudelft.nl

Abstract

A wideband harmonic rejection (HR) voltage-domain mixer using resistive scaling is presented featuring excellent linearity and high intermediate frequency (IF) bandwidth. Thin-oxide devices with constant gate-to-source voltages (V_{GS}) are utilized to maximize the switching linearity. A novel switching core topology providing low-impedance IF outputs is proposed to support wideband in-phase (I) and quadrature (Q) mixer outputs when capacitively loaded by an analog-to-digital converter (ADC). Eight LO clock phases, each with a 25% duty cycle, are on-chip generated for quadrature down-conversion and HR. By cleverly activating and organizing the mixer branches, the mixer's input impedance at radio frequency (RF) can be kept perfectly constant throughout all eight clock phases, enhancing the mixer's linearity. The TSMC 40 nm-CMOS realized mixer reaches 20.9 dBm OIP3 at an IF of 50 MHz with a conversion loss of 22.5 dB. It offers an 800 MHz 3-dB IF bandwidth when connected to a differential capacitive loading of 0.15 pF, with a total power consumption of 40.7 mW drawn from a 1.1 V supply. The mixer targets linear wideband base station observation receiver applications.

Introduction

The fifth-generation cellular networks (5G) enforce stringent requirements on the spectral purity of wireless signals. As such, the transmit signal must typically have a minimum adjacent-channel-power-ratio (ACPR) of -45 dBc [1]. Therefore, 5G transmitters (TX) target nominal ACPR levels of -50 dBc. To achieve such a level with an energy-efficient power amplifier (PA), cellular base station transmitters employ a correction loop consisting of a directional coupler, filter, attenuator, down-converting observation receiver, and a digital pre-distorter unit (Figure 1(a)).

To allow accurate determination of the TX nonlinearities at these large ACPR levels, the down-converting path in such a TX setup must offer at least 60 dBc spurious-free dynamic range (SFDR) to the ADCs, with $3\times$ or $5\times$ the bandwidth of the modulated TX signal (to include the IM3 and IM5 products). To achieve this, practical TX observation loops take a fraction of the TX output signal using a directional coupler. Filtering is applied before the mixer to avoid unintended down-conversion of the harmonic content in the TX signal to the baseband by the harmonics of the mixer LO. Next, high attenuation occurs before the mixer to relax the mixer linearity requirements. The mixer is usually implemented in the current-domain to limit the voltage swings on its intermediate nodes increasing linearity. However, doing so requires linear-IF amplification after the mixer core to drive the capacitive input of the ADC ($C_{in} \sim 0.15$ pF) with sufficient voltage swing (e.g., up to 0.2 V). These later requirements combined with 60 dBc SFDR translate to an OIP3 of the observation receiver of 7 dBv or 20 dBm when referred to a $50\ \Omega$ load. The linear-IF amplification (e.g., a trans-impedance-amplifier (TIA) following the mixer core) becomes more challenging and power-hungry with increasing modulation bandwidths. More specifically, in sub-6 GHz 5G systems, the transmitter modulation bandwidth can reach 400 MHz, which yields 200 MHz in-phase and quadrature-phase signal representations. However, since the observation receiver also needs to include the IM3 and IM5 products, its actual bandwidth must approach 1 GHz, making the linearity, bandwidth, and power consumption of the observation receiver more and more a concern.

In this work, by introducing a new passive voltage-domain mixer topology capable of providing very high OIP3 and large IF bandwidth and harmonic rejection (HR), we aim to drastically simplify the topology of an observation receiver and avoid the need for power-hungry wideband linear-IF amplification. Moreover, the need for a directional coupler, filter, and attenuator can also be omitted when adequately addressed in the down-converting mixer design. Additionally, when aiming for co-integrating of the proposed mixer with a digital transmitter [2, 3], the clock generation can be shared (Figure 1(b)). This observation receiver configuration makes classical mixer performance parameters like IIP3 and conversion loss rather arbitrary since they entirely

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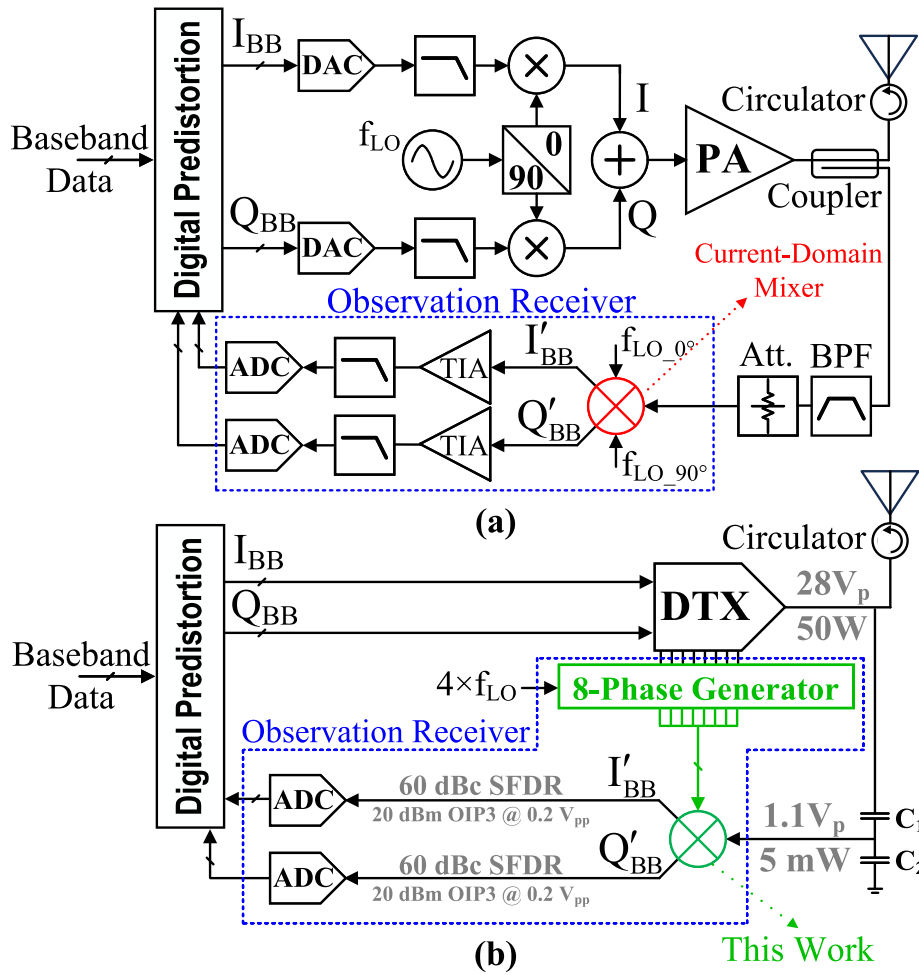


Figure 1. Block diagram of a transmitter with an observation receiver containing the down-converting mixer and a digital pre-distorter (DPD) unit for an (a) analog intensive transmitter and (b) envisioned digital intensive transmitter.

depend on the applied attenuation in the correction loop. Furthermore, since the correction loop aims to model the PA transfer function rather than monitor the TX signal itself, the noise contributions of the observation receiver are averaged out over time, relaxing the mixer noise figure requirement. Moreover, since filtering in Figure 1(b) is omitted, HR needs to be included in the mixer. Finally, since base station transmitters typically use an isolator in their output, a simple capacitive voltage divider with $C_2 \gg C_1$, as shown in Figure 1(b), can be used to simplify the hardware configuration and allow co-integration with the transmitter.

HR in mixers is typically achieved by using multiple sub-mixers in parallel with phase-shifted LO clocks and scaled currents for their switching cores [4]. This approach allows the mimicking of an N-sampled sinewave LO [5]. These current-domain mixers mostly employ TIAs in their RF and/or IF path, which is one of the causes that their in-band linearity is typically limited to <10 dBm in terms of IIP3 [6–10]. To date, HR voltage-domain mixers in sub-6 GHz bands have been demonstrated with an OIP3 up to 13 dBm [12]. Here, OIP3 is the fairer metric to compare, given the conversion loss. In these voltage-domain mixers, the limiting factor for the linearity is the variation of the on-resistance (R_{on}) of the mixer switches, due to their dependence on the gate-to-source (V_{GS}) voltages, which fluctuate with the RF input signal [5, 12]. In addition, both current and voltage-domain-type mixers using TIAs are restricted by IF bandwidth limitations [6–10].

To overcome the above challenges, we propose a new voltage-domain passive HR mixer topology for observation receiver applications in which the gate-to-source voltages (V_{GS}) of mixer switches' always remain constant to achieve high OIP3. Furthermore, by properly designing and scaling the mixer branches while using eight LO phases with a 25% duty cycle, the input impedance of the proposed mixer switching core can be kept constant throughout all LO phases, further boosting its linearity. Finally, the proposed mixer core provides low IF output impedance, allowing the direct wideband handling of capacitive loading by subsequent “I” and “Q” ADCs without any intermediate gain stage and, thus, lower power consumption.

Proposed voltage-domain mixer

Mixer concept

The concept of the proposed voltage-domain mixer can be understood best by considering the simplified schematic of Figure 2(a), representing a single mixer branch with, for now, a virtual ground connected to the node IF_{out} . Only one of the resistor branches is active (contributing current to IF_{out}) at any of the eight LO phases (Figure 2(a)). In this simplified topology, resistors R_1 , R_2 , and R_3 are sized such that the current flowing from IF_{out} to the virtual ground, resulting from an activated branch with resistors R_1

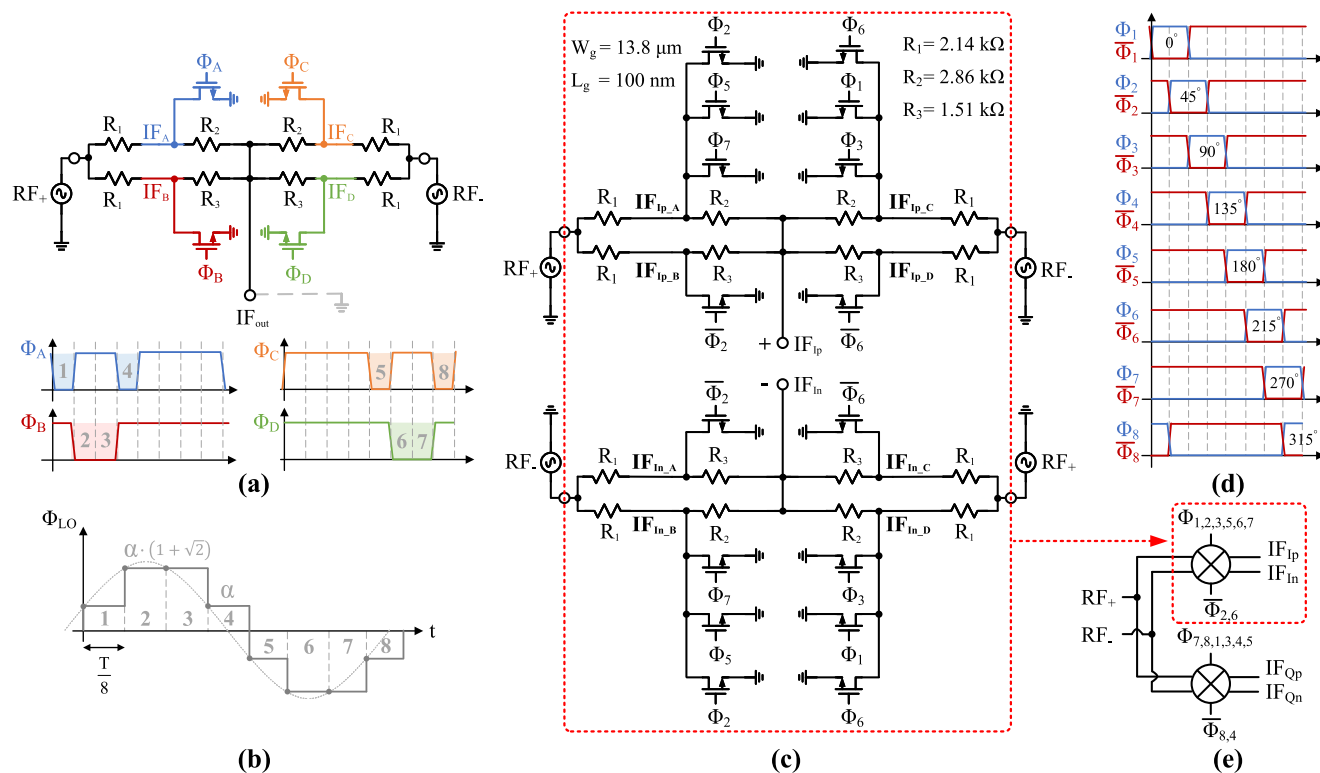


Figure 2. (a) Simplified topology and related LO phases; (b) effective harmonic-reject LO waveform; (c) full proposed voltage-domain mixer topology (I-only); (d) eight-phase 25% duty cycle LO waveforms; (e) extended I/Q mixer topology.

and R_2 , is a factor $1 + \sqrt{2}$ lower than that of an activated branch with resistors R_1 and R_3 , thereby implementing the scaling for HR of the LO waveform (see Figure 2(b)). The proposed configuration benefits from all switches having a well-defined V_{GS} referenced to ground. Therefore, avoiding undesired R_{on} modulation due to the RF input or IF output signals, yielding a strongly improved linearity.

The mixer in Figure 2(a) avoids both RF and LO feed-through to the IF port, as it effectively constitutes a double-balanced mixer (the right-hand side of the schematic in Figure 2(a) uses 180° rotated phases for both the RF and LO clock signals compared to the left-hand side). However, IF_{out} is a current summation node; therefore, any common-mode error appearing on the RF or LO ports will directly couple to the IF. To remedy that, the mixer topology is duplicated while flipping the polarity of the RF inputs to arrive at the final proposed mixer topology, shown in Figure 2(c). The resulting differential outputs IF_{Ip} and IF_{In} are now free of both differential as well as common-mode RF and LO input signals. Additionally, they provide a convenient differential signal to drive the subsequent ADC stages. Furthermore, since the use of different duty cycles to drive the switches (as in Figure 2(a)) is problematic in practical circuit implementations, it is beneficial to maintain the same 25% duty cycle across all clocking phases, yielding better phase synchronization between the different clock-paths and, thus, better linearity and HR. This requires splitting each of the two switches controlled by Φ_A and Φ_B in the simplified topology of Figure 2(a), into three separate switches controlled by 25% duty cycle LO signals $\Phi_{1,3,6}$ and $\Phi_{2,5,7}$ respectively (see Figure 2(d)).

To obtain useful representations of the IF output signals, the virtual ground in the simplified topology needs to be replaced. The most trivial way to do so is to introduce TIAs at these positions.

However, practical TIAs will introduce linearity, bandwidth, and power-budget constraints. Since in our observation receiver the mixer conversion gain is not a concern, and all RF and LO signals are already canceled at the IF port, we can remove the virtual ground and use the network terminals IF_{Ip} and IF_{In} directly as the output nodes (Figure 2(c)). With this change, the signals are now all in the voltage-domain. Doing so, resistors R_1, R_2 , and R_3 need to be re-sized to include the IF port impedance in order to maintain the proper HR ratios of Figure 2(b). The effect of the IF port impedance will be further analyzed in “Theory and derivations” section.

The extension to a differential quadrature down-conversion mixer is achieved by duplicating the mixer core topology once more and phase-shifting the LO by 90° (Figure 2(e)). The loading of the input nodes RF_+ and RF_- by the total I/Q mixer now remains perfectly constant throughout all phases of the LO cycle (thus vs. time), again contributing to the linearity of the proposed mixer.

Clock generation

Figure 3 shows a block diagram of the implemented on-chip clock generation chain. A single-ended 50% duty cycle LO clock at frequency $4 \times f_{LO}$ is fed to the chip. An on-chip balun designed as a double-tuned transformer is implemented to produce differential LO signals. A phase-aligner and two consecutive divide-by-2 stages are implemented to generate eight-phase 50% duty cycle LO clocks at f_{LO} . The clock dividers are implemented using D-Latches in a C^2 MOS (clocked CMOS) topology [13]. AND/OR gates devised solely from symmetric NAND gates are then implemented to create eight-phase 25% duty cycle LO waveforms at f_{LO} . Consequent phase-aligning stages are implemented for better phase synchronization. Buffers are implemented as needed

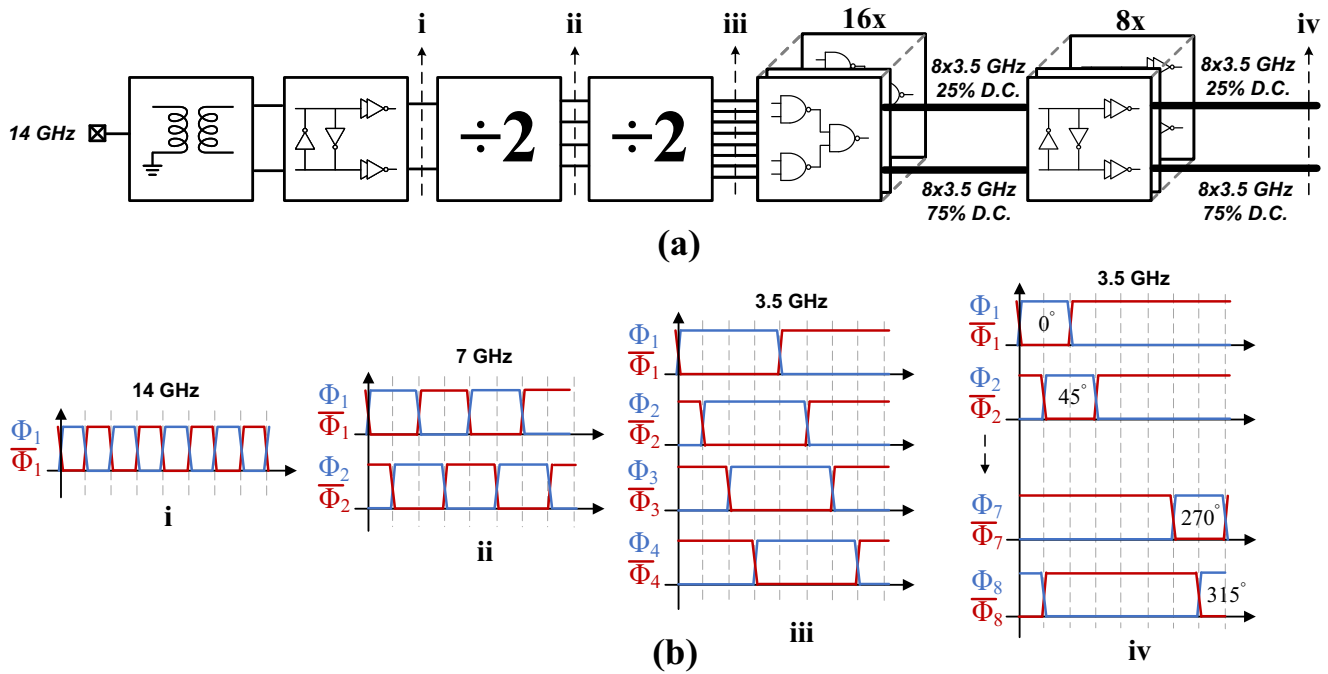


Figure 3. (a) Block diagram of the implemented on-chip clock generation chain; (b) from left to right: (i) input 14 GHz clock, (ii) intermediate 7 GHz clock phases after first divider, (iii) intermediate 3.5 GHz clock phases after second divider, (iv) final 3.5 GHz clock phases after 25% duty cycle generation.

throughout the clocking chain and are not explicitly shown in this block diagram.

Theory and derivations

Input impedance

The extension of the proposed mixer topology to an I/Q mixer, as shown in Figure 2(e), has the extra advantage of keeping the input impedance of the total I/Q mixer constant across time. This can be deduced by considering the input impedance of the I and Q mixers during each of the eight LO clock phases. Figure 4 showcases both the I and Q mixers including the IF port's capacitive load during the first (or fourth) LO clock phase (Φ_A in Figure 2(a)) as an example, from the four branches in the I mixer connecting the RF inputs (RF_+ and RF_-) to the in-phase IF output (IF_{ip}), only one branch is conducting. Similarly, only one branch of the four branches in the I mixer connecting the RF inputs (RF_+ and RF_-) to the out-phase IF output (IF_{in}) is conducting. This holds for every other LO clock phase (see Figure 2(a)), where the one conducting branch in the I mixer swaps between a branch that includes R_2 (as in Figure 4) or a branch that includes R_3 . Thus, the input impedance of the I mixer (and similarly the Q mixer) is always switching between two levels that are determined by whether a branch including R_2 or a branch including R_3 is conducting in each of the eight LO clock phases for the I and Q mixer, alongside the related shunt resistances and capacitive load at the IF port. These two impedance levels are coined Z_A and Z_B . During a single clock phase, when the I mixer has a branch conducting that includes R_2 , the Q mixer will have a branch conducting that includes R_3 (as can be seen in Figure 4) and vice versa.

This impedance behavior is visualized in Figure 5 across one full LO cycle. For the I mixer, the single-ended input impedance seen by the RF inputs (RF_+ or RF_-) across one LO cycle is shown in Figure 5(a) and 5(b), respectively. This shows that the input

impedance of the I mixer alone will not be constant and will vary with a period half of that of the LO, providing even-order harmonic content that would limit the mixer's linearity. For the Q mixer, the single-ended input impedance seen by the RF inputs (RF_+ or RF_-) across one LO cycle is shown in Figure 5(c) and 5(d), respectively. The total input impedance of the proposed I/Q mixer is, therefore, the parallel combination of the input impedance of the I and Q mixers and is shown in Figure 5(e) and 5(f). This combined input impedance is constant across time and thus boosts the mixer's linearity. This result only holds in an I/Q mixer with eight LO clock phases. Thus, an I/Q mixer with more LO clock phases (i.e., more samples per LO cycle following the proposed concept) will not have a constant input impedance across time.

To derive the I/Q mixer's total input impedance, we need to determine the two impedance levels Z_A and Z_B . The impedance Z_A is the impedance seen by RF_+ during the first, fourth, fifth, and eighth phases of the LO, which by design is a single conducting branch with R_2 and three off branches and can be written as:

$$Z_A = \left(R_1 + R_2 + R_2 \parallel \frac{R_3}{2} \parallel \frac{1}{j\omega_{bb} \cdot 2C_L} \right) \parallel \frac{R_1}{3}. \quad (1)$$

Similarly, the impedance Z_B can be derived as the impedance seen by RF_+ during the second, third, sixth, and seventh phases of the LO, which by design is a single conducting branch with R_3 and three off branches and can be written as:

$$Z_B = \left(R_1 + R_3 + R_3 \parallel \frac{R_2}{2} \parallel \frac{1}{j\omega_{bb} \cdot 2C_L} \right) \parallel \frac{R_1}{3} \quad (2)$$

where the frequency term $\omega_{bb} = |\omega_{rf} - \omega_{lo}|$ translates the base-band impedance to the LO frequency due to the mixing action of the switches.

The total constant RF single-ended input impedance of the overall I/Q mixer is the parallel combination of Z_A and Z_B (as visualized in Figure 5(e) and 5(f)). Substituting Z_A and Z_B

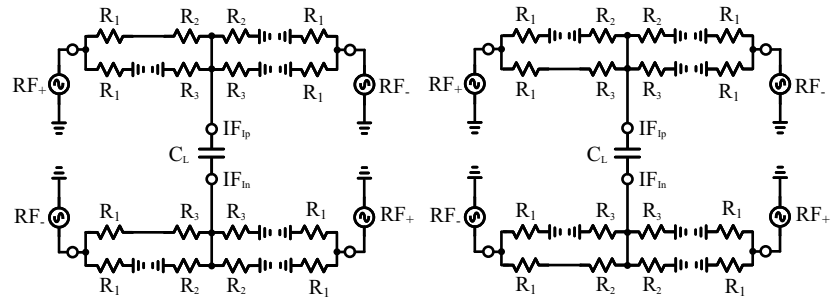


Figure 4. Circuit diagram including IF port capacitive load during first LO clock phase for the (a) I mixer and (b) Q mixer.

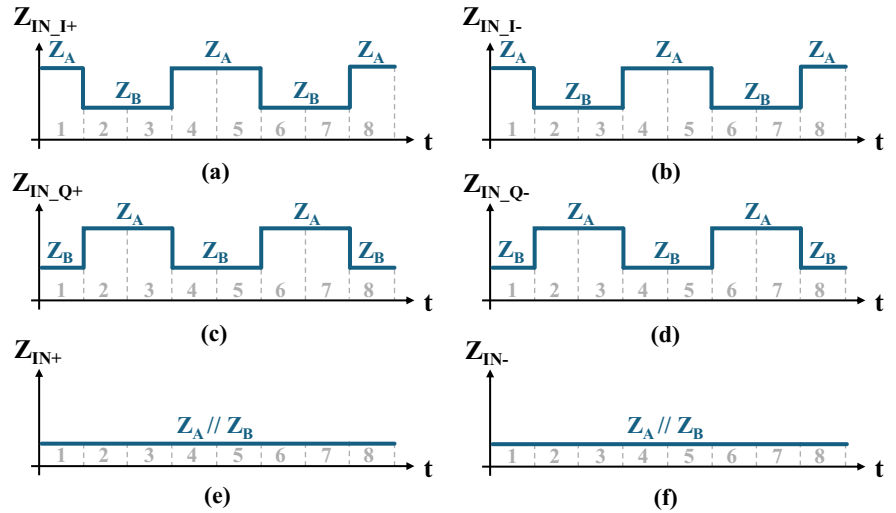


Figure 5. (a) I mixer RF₊ single-ended input impedance; (b) I mixer RF₋ single-ended input impedance; (c) Q mixer RF₊ single-ended input impedance; (d) Q mixer RF₋ single-ended input impedance; (e) I/Q mixer RF₊ single-ended input impedance; (f) I/Q mixer RF₋ single-ended input impedance.

with their derived expressions from (1) and (2), respectively, we can write the total constant single-ended RF input impedance of the overall I/Q mixer seen by RF₊ or RF₋ with respect to ground as:

$$Z_{in} = \left(R_1 + R_2 + R_2 \parallel \frac{R_3}{2} \parallel \frac{1}{j\omega_{bb} \cdot 2C_L} \right) \times \parallel \left(R_1 + R_3 + R_3 \parallel \frac{R_2}{2} \parallel \frac{1}{j\omega_{bb} \cdot 2C_L} \right) \parallel \frac{R_1}{6}. \quad (3)$$

Figure 6 plots the mixer's single-ended input impedance versus input RF frequency using the resistor values provided in Figure 2 and $C_L = 150$ fF. The calculated mixer's single-ended input impedance from (3) matches well with the simulated results using ideal switches, where the small deviation between the two curves is due to the steady-state approximation taken in (1) and (2), which was used to simplify the derivation, especially since the input impedance in (3) is dominated by the $\frac{R_1}{6}$ term from the six "off" branches, significantly reducing the effect of the error due to this approximation. Furthermore, in an observation receiver application, the goal is to have a high enough mixer's input impedance to avoid significantly loading the PA, thus, an exact derivation is not necessary. The simulated mixer's input impedance decreases when using real switches due to the extra on-resistance and the off-capacitance, it decreases slightly more at higher RF frequencies mainly due to the off-capacitance.

Referring back to the digital intensive transmitter envisioned in Figure 1, the total single-ended input impedance seen looking into the observation receiver path can be written as:

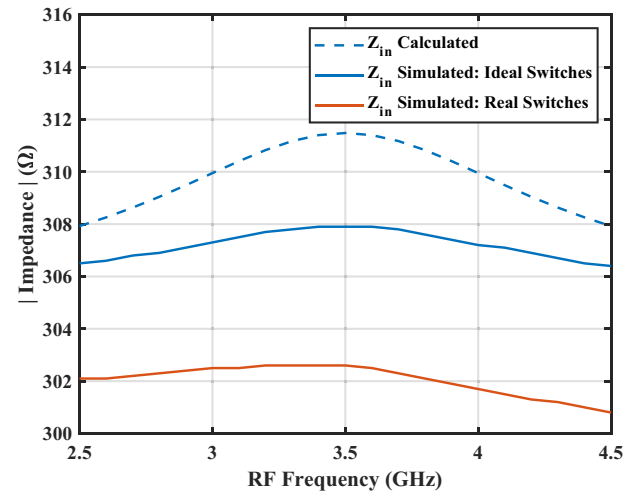


Figure 6. Mixer's single-ended input impedance.

$$Z_{rx} = \frac{1}{j\omega_{rf} \cdot C_1} + Z_{in} \parallel \frac{1}{j\omega_{rf} \cdot C_2}. \quad (4)$$

Maximizing this input impedance can be achieved by minimizing C_1 . Assuming $C_1 = 10$ fF and taking $Z_{in} \approx 302 \Omega$ from Figure 6, it can be directly calculated that $C_2 = 195$ fF is needed to achieve sufficient attenuation from $28 V_p$ to $1.1 V_p$. For a PA with $28 V_p$ and $50 W$ peak output power (as in Figure 1), a load impedance of $\approx 8 \Omega$ is needed. Substituting by the aforementioned values in (3), Z_{rx} changes the impedance seen by the PA to $7.9996 \Omega - j0.014 \Omega$.

A change so minuscule that it should not affect the efficiency of the PA. Furthermore, the matching network can be tuned slightly to account for this shift in the impedance seen by the PA. Finally, with a $1.1 V_p$ singled-ended input signal to the mixer and $Z_{in} \approx 302 \Omega$, the total input RF power drawn by the mixer from both the RF_+ and RF_- terminals is equal to 4 mW, a value too minuscule (compared to the total PA peak output power) to cause any significant degradation of the transmitter's system efficiency.

Output impedance

In the observation receiver line-up shown in Figure 1(b), the down-conversion mixer is followed by an ADC, which presents a capacitive load to the down-conversion mixer outputs. Thus, the IF output impedance of the down-conversion mixer needs to be low enough to allow a large IF bandwidth.

The instantaneous output impedance of either the I or Q mixer varies with time between two values depending on which of the two unique branches is conducting in each of the eight phases of the LO (similar to how the input impedance of either the I or Q mixer varied with time in Figure 5). To derive the mixer's output impedance, we need to determine these two alternating values of the output impedance. The single-ended output impedance looking into one of the output nodes in Figure 2(c) when a branch that includes R_2 is conducting and all the other branches are not can be written as:

$$R_{out,1} = (R_1 + R_2) \parallel R_2 \parallel \frac{R_3}{2}. \quad (5)$$

Similarly, the single-ended output impedance looking into one of the output nodes in Figure 2(c) when a branch that includes R_3 is conducting and all the other branches are not can be written as:

$$R_{out,2} = (R_1 + R_3) \parallel R_3 \parallel \frac{R_2}{2}. \quad (6)$$

The instantaneous output impedance of the mixer is alternating between the two impedance values (5) and (6) with the same frequency as that shown in Figure 5, namely $2 \times f_{LO}$. In the intended down-conversion observation receiver application, the IF output is at a much smaller baseband frequency than the LO. As such, we can approximate the mixer's baseband output impedance as the average between two impedance values in (5) and (6). This averaged output impedance determines the mixer's baseband output impedance and, therefore, determines the mixer's baseband bandwidth. The total differential baseband output impedance of either the I or Q mixer is:

$$R_{out} \approx \left((R_1 + R_2) \parallel R_2 \parallel \frac{R_3}{2} \right) + \left((R_1 + R_3) \parallel R_3 \parallel \frac{R_2}{2} \right). \quad (7)$$

The IF bandwidth can then be simply defined as:

$$BW = \frac{1}{2\pi R_{out} C_L}. \quad (8)$$

Conversion loss

The IF output of the mixer is the result of the multiplication of the RF input with the fundamental component of the LO waveform. Assuming a single-tone RF input with an amplitude of one, the conversion loss of the total mixer is then directly equal to the magnitude of the fundamental component of the effective LO waveform shown in Figure 2(b). To determine that magnitude, we

can decompose the effective LO waveform into four separate waveforms shown in Figure 7(a), where the duty cycle of each waveform is exactly 12.5%. The amplitude of the four waveforms is set by the two resistive scaling ratios TF_1 and TF_2 and depends on the eight phases of the effective LO waveform. For simplicity, the IF port capacitive loading will only be included in the succeeding sub-sections. TF_1 represents the voltage transfer function from the RF inputs to one of the IF outputs in Figure 4 when a branch including R_2 is conducting and can be written as:

$$TF_1 = \frac{\left(R_2 \parallel \frac{R_3}{2} \right)}{R_1 + R_2 + \left(R_2 \parallel \frac{R_3}{2} \right)}. \quad (9)$$

Similarly, TF_2 represents the voltage transfer function from the RF inputs to one of the IF outputs in Figure 4 if a branch including R_3 is conducting and can be written as:

$$TF_2 = \frac{\left(R_3 \parallel \frac{R_2}{2} \right)}{R_1 + R_3 + \left(R_3 \parallel \frac{R_2}{2} \right)}. \quad (10)$$

All of the decomposed LO waveforms in Figure 7(a) are of 12.5% duty cycle, thus, applying Fourier transform would yield a fundamental coefficient of $2 \cdot \sin\left(\frac{\pi}{8}\right)/\pi$. Consequently, the vector representation of the fundamental components of the four decomposed LO waveforms is shown in Figure 7(b). Finally, to derive the fundamental component of the effective LO, we perform a vector summation of the fundamental components of the decomposed waveforms. Thus, the magnitude of the conversion loss can be written as:

$$A_L = \frac{\alpha_1 \cdot \left(R_2 \parallel \frac{R_3}{2} \right)}{R_1 + R_2 + \left(R_2 \parallel \frac{R_3}{2} \right)} + \frac{\alpha_2 \cdot \left(R_3 \parallel \frac{R_2}{2} \right)}{R_1 + R_3 + \left(R_3 \parallel \frac{R_2}{2} \right)} \quad (11)$$

where α_1 and α_2 are equal to 0.1865 and $\sqrt{2}/\pi$, respectively.

The blue curves in Figure 8 show the result calculated from (11) perfectly matching the mixer's simulated conversion loss without the capacitive load and with ideal switches. The mixer displays no frequency dependence yet due to not including the capacitive load.

Switch parasitics

To ease the precise clocking of the entire mixer core, all the switches used in the mixer are identical and are sized as shown in Figure 2(c), with dummy switches added to equalize the capacitive load seen by each clock line. The switches need to be sized big enough such that their on-resistances (R_{on}) acts as an effective "short" to ground for the off branches when the switch is turned on but should also not be over-sized as a bigger switch adds a higher off-capacitance (C_{off}) which would affect the branches HR performance. In TSMC 40 nm technology, the selected switch with $W_g = 13.8 \mu m$ and $L_g = 100 nm$ has an on-resistance of 50Ω and an off-capacitance of $5 fF$. The reasoning for not using minimum gate length in the switches is to reduce channel length modulation with drain voltage variation which would introduce a secondary source of nonlinearity. This is highlighted in Figure 9, where the OIP3 improves by increasing the switches' channel length (while keeping W_g/L_g constant to maintain the same R_{on}) until the effect of the larger off-capacitance added by the larger switches start to dominate.

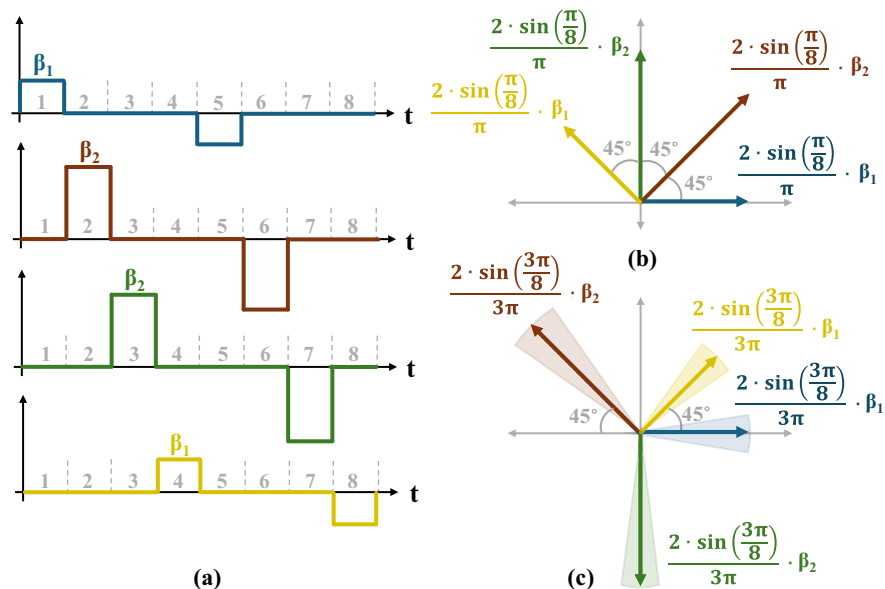


Figure 7. (a) Decomposed LO waveforms; (b) vector representation of the fundamental component of the decomposed LO waveforms; (c) vector representation of the third harmonic of the decomposed LO waveforms with phase error.

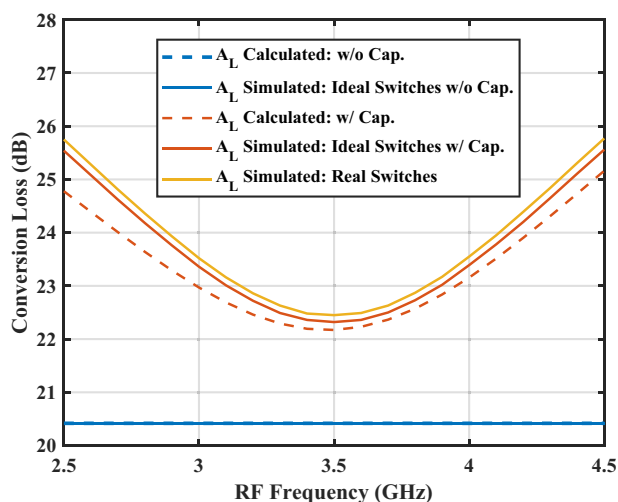


Figure 8. Mixer's conversion loss.

So far, the parasitic on-resistance and off-capacitance of the switches have been neglected in the above derivations of the mixer, since their effect is mostly secondary. The on-resistance of the switch should be small compared to the values of R_1 , R_2 , and R_3 . However, as previously stated, the parasitic off-capacitance can have some impact on the previously equated mixer performance parameters.

For the output impedance, we are only interested in the effective baseband impedance so the parasitic off-capacitance can be neglected. For the input impedance, the parasitic off-capacitance can play a role as we're interested in the RF impedance; however, from (3), we can see that the input impedance is mainly dominated by R_1 from the six branches that are "off", thus the effect of the parasitic off-capacitance is also negligible for the input impedance.

The conversion loss will be the most affected by the parasitic off-capacitance as it affects the transfer functions of the two mixer

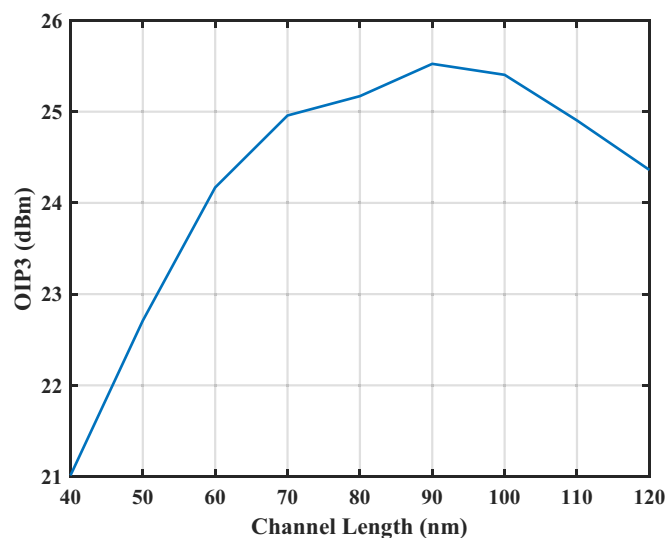


Figure 9. Mixer's OIP3 vs. switches' channel length (constant W_g/L_g).

branches at the fundamental carrier frequency (f_{LO}). Furthermore, the effect of the IF port loading capacitor C_L must also be included.

To determine the branch transfer function while including the effect of the capacitances, it is convenient to use two transfer functions. The first transfer function (TF_A) is the transfer from one of the RF input ports to one of the intermediate mixing nodes $IF_{pA:D}$ and $IF_{nA:D}$ as defined in Figure 2(c). The second transfer function (TF_B) is the transfer from one of the intermediate mixing nodes $IF_{pA:D}$ and $IF_{nA:D}$ to one of the IF output summation nodes IF_p and IF_n as defined in Figure 2(c). It is important to note that the mixing has already occurred at the intermediate mixing nodes $IF_{pA:D}$ and $IF_{nA:D}$, meaning the scaled IF components are already created. Thus, only the baseband frequency is of interest in TF_B . TF_A including the effect of the capacitances can thus be

written as:

$$TF_{A1} = \frac{\left(R_2 + R_2 \parallel \frac{R_3}{2} \parallel \frac{1}{j\omega_{rf} C_L} \right) \parallel \left(\frac{1}{j\omega_{rf} 3C_{off}} \right)}{R_1 + \left(R_2 + R_2 \parallel \frac{R_3}{2} \parallel \frac{1}{j\omega_{rf} C_L} \right) \parallel \left(\frac{1}{j\omega_{rf} 3C_{off}} \right)} \quad (12)$$

$$TF_{A2} = \frac{\left(R_3 + R_3 \parallel \frac{R_2}{2} \parallel \frac{1}{j\omega_{rf} C_L} \right) \parallel \left(\frac{1}{j\omega_{rf} C_{off}} \right)}{R_1 + \left(R_3 + R_3 \parallel \frac{R_2}{2} \parallel \frac{1}{j\omega_{rf} C_L} \right) \parallel \left(\frac{1}{j\omega_{rf} C_{off}} \right)} \quad (13)$$

where TF_{A1} and TF_{A2} denote TF_A in a conducting branch including R_2 and R_3 respectively.

Similarly, TF_{B1} can be written as:

$$TF_{B1} = \frac{\left(R_2 \parallel \frac{R_3}{2} \parallel \frac{1}{j\omega_{bb} C_L} \right) \parallel \frac{1}{j\omega_{bb} 3C_{off}}}{R_2 + \left(R_2 \parallel \frac{R_3}{2} \parallel \frac{1}{j\omega_{bb} C_L} \right) \parallel \frac{1}{j\omega_{bb} 3C_{off}}} \quad (14)$$

$$TF_{B2} = \frac{\left(R_3 \parallel \frac{R_2}{2} \parallel \frac{1}{j\omega_{bb} C_L} \right) \parallel \frac{1}{j\omega_{bb} C_{off}}}{R_3 + \left(R_3 \parallel \frac{R_2}{2} \parallel \frac{1}{j\omega_{bb} C_L} \right) \parallel \frac{1}{j\omega_{bb} C_{off}}} \quad (15)$$

where TF_{B1} and TF_{B2} denote TF_B in a conducting branch including R_2 and R_3 respectively.

Finally, the total conversion loss including the effect of the capacitances can be written as:

$$A_L = \alpha_1 \cdot TF_{A1} \cdot TF_{B1} + \alpha_2 \cdot TF_{A2} \cdot TF_{B2} \quad (16)$$

where α_1 and α_2 are equal to 0.1865 and $\sqrt{2}/\pi$, respectively, as previously determined in (11).

The red and yellow curves in Figure 8 plot the mixer's conversion loss versus input RF frequency; both calculated from (16) and simulated using ideal and real switches. The mixer's capacitive load is now included and the ideal switches now also include a 5 fF off-capacitance. The small deviation between the calculated result and the simulated one with ideal switches is due to the steady-state approximation taken in (12)–(15). The deviation between the simulations with ideal switches (including off-capacitance) and real switches is due to the switches' on-impedance as well as finite switching times.

Harmonic rejection

The previously derived equation for the conversion loss implicitly uses a steady-state approximation. While this approximation does not produce significant error for the fundamental component (and thus for the conversion loss), it does yield a significant error in the third harmonic (and thus for the HR). Consequently, the phases of the down-converted tones provided by the mixer branches are no longer dependent only on their clock phases (as in Figure 7(b)) but also on the phase error of the branches due to the capacitances. These phase errors do not affect the down-conversion of the fundamental component significantly but do degrade the HR. This is visualized in Figure 7(c) where the shaded regions represent the phase error in the mixer branches, the total vector summation of the third harmonic components no longer perfectly cancels. Furthermore, the relative phase in the previous steady-state based equations become inaccurate as the mixer is inherently a switching circuit, which never reaches steady-state conduction for its intermediate nodes. Thus, these steady-state equations cannot be used to determine the HR when (C_{off}) and (C_L) are included.

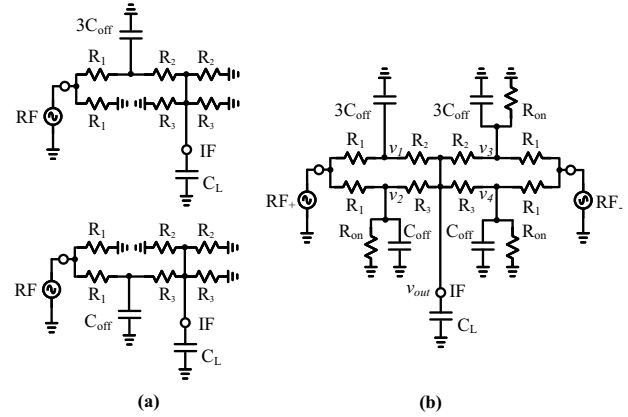


Figure 10. (a) Equivalent mixer quad assuming ideal R_{on} when a branch with either R_2 (top) or R_3 (bottom) is conducting; (b) equivalent mixer quad assuming real R_{on} when a branch with R_2 is conducting.

Instead, the transience of the intermediate mixing nodes needs to be taken into account. Figure 10(a) shows the path between the RF input and the IF output of a mixer quad during the first (or fourth) LO phase as an example. The differential equation describing the output IF voltage as a function of time ($v_{out}(t)$) assuming a single tone sinusoid input with frequency ω and phase φ is:

$$a \cdot v_{out}(t) + b \cdot v'_{out}(t) + c \cdot v''_{out}(t) = \sin(\omega t + \varphi) \quad (17)$$

where a , b , and c are functions of R_1 , R_2 , R_3 , C_L , and C_{off} which are defined in Appendix A.

Consequently, the solution of such a second-order differential equation can be written as:

$$v_{out}(t) = \rho(t) + c_1 \cdot e^{-\beta_1 t} + c_2 \cdot e^{-\beta_2 t} \quad (18)$$

with c_1 , c_2 , β_1 , β_2 , and $\rho(t)$ given in Appendix A.

Using (18), the output IF voltage can be determined for each LO clock phase, where the initial conditions of the differential equation are determined from the preceding LO clock phase.

The above equation provides a much more accurate result for the phase responses of the two scaling branches for the third (and higher) harmonic. The only approximation left is the neglect of the on-resistance of the mixing switches. To address this, Figure 10(b) shows the signal path between the RF input and the IF output of the mixer quad during the first LO phase as an example, while including the on-resistance of the mixing switches. As can be seen, for a single scaling branch in a single LO clock phase, the off-capacitance of each of the four switches now plays a role. Furthermore, both differential RF inputs need to be considered. The resulting differential equation describing the output IF voltage as a function of time now becomes a fifth-order differential equation, which is too cumbersome to solve analytically. Instead, applying Kirchhoff's current law (KCL) at both the intermediate mixing nodes (v_1, v_2, v_3 , and v_4) as well as the IF output voltage node (v_{out}), we can write a system of five first-order differential equations (defined in Appendix B) that can be solved numerically. Similar to (18), the system is solved for a single LO clock phase where the initial conditions are determined from the preceding LO clock phase. This system was solved numerically using fourth-order Runge-Kutta (RK4) and provides the most accurate phase for the third and higher harmonics.

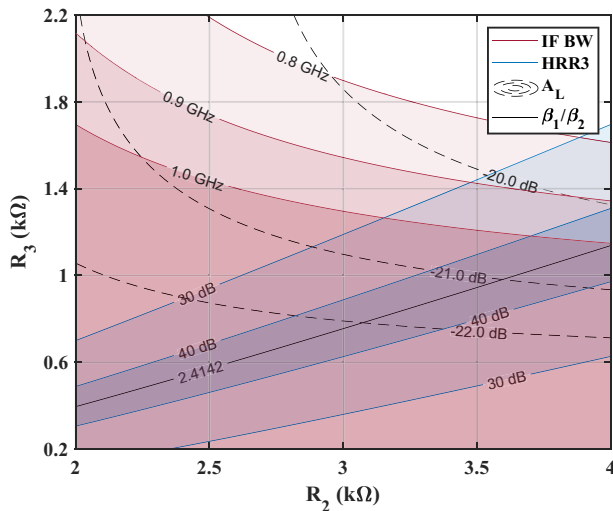


Figure 11. Mixer design contours for IF bandwidth, third harmonic rejection ratio, and conversion loss vs. R_2 and R_3 for a chosen R_1 value.

Design charts

Informed design decisions for the proposed mixer can be made based on the derivations in the previous subsections. It can be deduced from (3) that the input impedance is mostly dominated by the value of R_1 . Thus, R_1 should be chosen large enough to limit the RF input power. Secondly, the length of the switch should be chosen large enough such that the C_{off} dependence on its drain voltage is minimized. The width of the switch should be large enough such that R_{on} is much smaller than values of R_1 and R_2 . Thirdly, with an initial switch size resulting in a certain R_{on} and C_{off} , the values of R_2 and R_3 need to be chosen such that they satisfy both the IF bandwidth and HR requirements together. This selection can be eased by considering Figure 11, in which the IF bandwidth, HR, and conversion loss contours are plotted using the approximating resistive equations defined in (11). It visualizes that there is a trade-off between the IF bandwidth (requiring a small output impedance as defined in (7), i.e., small values of R_2 and R_3) and the conversion loss. Furthermore, in this resistive approximation, there are no phase errors, thus perfect HR is guaranteed as long as the magnitude scaling ratio between the two branches (see (9) and (10)) is equal to $1 + \sqrt{2}$, as illustrated by the solid black line in Figure 11 plotting the contour at which this ratio is equal to $1 + \sqrt{2}$.

While the approximate resistive equation defined in (11) is a good way to illustrate the HR concept, it is inaccurate since the phase errors of the two scaling paths were not included. As such, Figure 12 provides the design contours again, but now with the HR plotted by numerically solving the system of five first-order differential equations described in the previous subsection (and defined in Appendix B). We see that the trade-off between the IF bandwidth and the conversion loss still exists, but we also see that the HR ratio is no longer only dependent on the magnitude ratio between the two scaling paths but also starts to depend on the phase error introduced by these two scaling paths. The solid black line in Figure 12 gives the trajectory where the ratio between the down-converted component at the IF output node (IF_p and IF_n as defined in Figure 2(c)) after mixing with the LO third harmonic from each of the two scaling paths equals one. In case of no phase error, the HR should thus peak along this trajectory where the ratio is equal to one. In Figure 12, we see that the HR does indeed peak along this

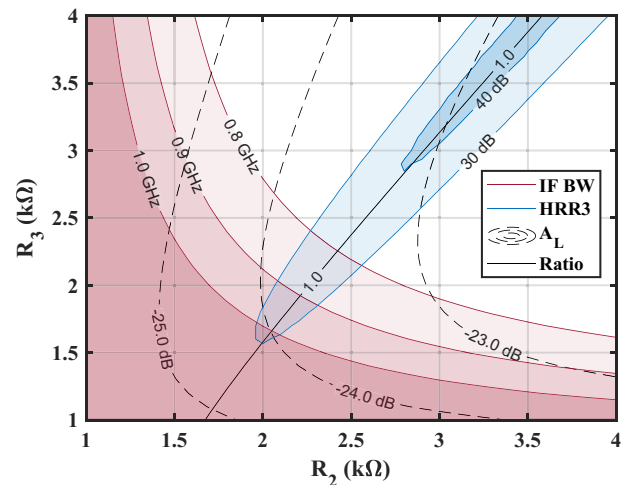


Figure 12. Mixer design contours for IF bandwidth, third harmonic rejection ratio, and conversion loss vs. R_2 and R_3 for chosen R_1 , R_{on} , and C_{off} values.

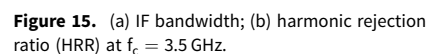
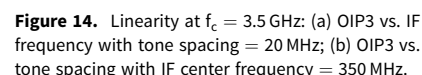
trajectory; however, it peaks more for higher values of R_2 and R_3 , indicating a lower phase error for these values.

It should be noted that in all the equations derived, the values of C_{off} and R_{on} were approximated as constant, determined as the average value inside each LO clock phase, where in reality they depend on the drain voltage, thus affecting the phase error of the scaling paths and the HR. Furthermore, any errors in phase or duty cycle of the LO clocks will also affect the HR. Consequently in a practical design, starting with the selected values of R_2 and R_3 from the design contours, simulations need to be run with the full switch model and the implemented clock generator. Any phase errors introduced in the clock generation circuitry can be beneficial if it cancels out the phase errors introduced by the two scaling paths, thus boosting HR. The final chosen values of R_1 , R_2 , and R_3 as shown in Figure 2(c) were fine-tuned by simulating the post-layout extracted mixer and clock generation chain combined.

Mixer implementation and measurements

The mixer, including the eight phase LO generation (Figure 2(d)), was implemented using thin-oxide transistors in TSMC 40 nm-CMOS technology. The mixer core occupies an area of $27 \times 27 \mu\text{m}$. Including the LO generation circuitry, the total mixer area is $133 \times 57 \mu\text{m}$ (Figure 13(a)). All subsequent measurements are performed at a carrier frequency of 3.5 GHz targeting mMIMO base station applications. The mixer's power consumption, including clock generation, is 40.7 mW from a 1.1 V supply.

Conversion loss, linearity, and HR measurements were performed using the setup shown in Figure 13(b). The output losses due to cable connections and board traces were de-embedded. The measurement setup includes three single-tone signal generators where one source is used to generate the LO signal and the other two are used in combination with a power combiner to generate a two-tone RF input signal to the mixer. An off-chip balun is used after the power combiner to convert the generated single-ended two-tone signal into a differential one. The outputs are measured differentially with a high input impedance oscilloscope or single-ended with a source analyzer, the remaining outputs are terminated either with an open-circuit or 50Ω impedances, respectively, depending on the instrument being used.



(MSOS804A) with an input impedance of $1\text{ M}\Omega\parallel 14\text{ pF}$ connected at the I-mixer's outputs, the outputs of the Q-mixer were connected to an open-circuit termination in this measurement as shown in Figure 13(b). This measurement yielded a conversion loss of 22.5 dB, which matches well with simulations in Figure 8, indicating the fabricated resistor ratios are accurate. Thus, confirming the targeted IF bandwidth of 800 MHz for the original intended differential capacitive loading of 0.15 pF, since the bandwidth (8)

Table 1. Performance comparison with wideband highly linear mixers

Design	This work	[12]	[5]	[6]	[9]	[10]	[11]
Technology	40 nm CMOS	32 nm SOI	45 nm SOI	28 nm HPC	65 nm CMOS	65 nm CMOS	22 nm FDSOI
Mixing domain	Voltage	Voltage	Voltage	Current	Current	Current	Voltage
I/Q paths	Yes	No	No	Yes	Yes	Yes	Yes
RF frequency (GHz)	3.5	3.5	3	2	2	2	1
3 dB IF BW (MHz)	800	200	80	130	425	200	16
Conversion gain (dB)	-22.5	-7.5	-10	32.4	40	33.5	13
HRR (dB)	30^b	40 ^a	35 ^a	–	–	–	–
Harmonics rejected	2	2	6	–	–	–	–
In-band OIP3 (dBm)	20	13	8	–	–	–	–
In-band IIP3 (dBm)	–	–	–	-12	-12.5	-7.5	10
Supply voltage (V)	1.1	1.1	1	1.8/1.2	1.8/1.2	1.8/1.2	0.8
Power (mW)	40.7	80	160	37.2	72	34	0.6

^aMeasured with GSSG probes.^bMeasured with bond wires.

only depends on the same resistor ratios. The measured IF bandwidth is shown in Figure 15(a). The deviation from simulation is due to the non-perfect RF input balun's response as well as input-output (IO) and electrostatic discharge (ESD) circuitry. The targeted IF output voltage swing of $0.2 V_{pp}$ for a maximum RF-input swing of $2.68 V_{pp}$ was also confirmed.

Using a source analyzer (R&S FSUP50) with 50Ω IF port loading, the measured OIP3 proved to be 20 dBm across the mixer's IF bandwidth (Figure 14(a)); a comparable performance was also achieved versus RF tone-spacing (Figure 14(b)). This is lower than the simulated linearity of the intrinsic mixer core ($OIP3 > 24$ dBm), this deviation could be explained by the impact of the IO-interconnect parasitics (bond wires and the nonlinearity due to the ESD protection circuits).

The third harmonic rejection ratio (HRR3) was measured to be around 30 dB over the mixer's IF bandwidth (Figure 15(b)). This somewhat reduced HRR3 was associated with an imbalance introduced by the on-chip balun connection. When including the balun imbalance and nonlinearity caused by the ESD protection within our simulations, they align well with the measurements.

Conclusions

A novel highly linear wideband harmonic-reject voltage-domain mixer topology is proposed and implemented in CMOS 40 nm. By circumventing the nonlinearity introduced by the variation of the mixer's switches' on-impedance and the need of power-hungry wideband linear-IF amplification, excellent linearity performance is achieved, making it an interesting candidate for the implementation of highly linear, wideband, low-power base station observation receiver applications. The realized mixer (despite its ESD and interconnect parasitics) offers excellent performance in terms of OIP3 (20 dBm) and IF bandwidth (800 MHz) while offering HR and quadrature down-conversion functionality, placing it favorably among previously reported state-of-the-art mixers when considering observation receiver applications, as can be concluded from Table 1.

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Competing interests. The author(s) declare none.

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Appendix A

Assume C_2 is the off-capacitance of the switch in a branch including R_2 , and C_3 is the off-capacitance of the switch in a branch including R_3 . Thus, C_2 and C_3 can be written as:

$$C_2 = 3 \cdot C_{\text{off}}$$

$$C_3 = C_{\text{off}}.$$

The coefficients of the second-order differential equation (17) describing the mixer's IF output voltage as a function of time when R_{on} is neglected are presented below:

$$a = 1 + \frac{R_1 + R_{2,3}}{R_{2,3} \parallel \frac{R_{3,2}}{2}}$$

$$b = C_L \cdot (R_1 + R_{2,3}) + R_1 \cdot C_{2,3} \cdot \left(1 + \frac{R_{2,3}}{R_{2,3} \parallel \frac{R_{3,2}}{2}} \right)$$

$$c = R_1 \cdot R_{2,3} \cdot C_L \cdot C_{2,3}$$

where $R_{2,3}$ and $C_{2,3}$ are equal to R_2 and C_2 when a branch with R_2 is conducting and are equal to R_3 and C_3 when a branch with R_3 is conducting. Similarly, $R_{3,2}$ and $C_{3,2}$ are equal to R_3 and C_3 when a branch with R_2 is conducting and are equal to R_2 and C_2 when a branch with R_3 is conducting.

The time-dependent term $\rho(t)$ in the analytical solution (18) of this second-order differential equation is:

$$\rho(t) = \frac{1}{\sqrt{b^2 - 4ac}} \cdot \left(\frac{\omega \cdot \cos(\omega t + \varphi) - \beta_1 \cdot \sin(\omega t + \varphi)}{\beta_1^2 + \omega^2} - \frac{\omega \cdot \cos(\omega t + \varphi) - \beta_2 \cdot \sin(\omega t + \varphi)}{\beta_2^2 + \omega^2} \right)$$

where the coefficients β_1 and β_2 are defined as:

$$\beta_1 = \frac{b + \sqrt{(b^2 - 4ac)}}{2c}$$

$$\beta_2 = \frac{b - \sqrt{(b^2 - 4ac)}}{2c}.$$

Finally, the constants of the analytical solution (18) of this second-order differential equation are:

$$\psi_1 = v_{\text{out}}(0) - \rho(0)$$

$$\psi_2 = \rho'(0) - v'_{\text{out}}(0)$$

$$c_1 = \frac{\psi_1 \cdot \beta_2 - \psi_2}{\beta_2 - \beta_1}$$

$$c_2 = \frac{\psi_1 \cdot \beta_1 - \psi_2}{\beta_1 - \beta_2}.$$

Appendix B

Assuming a differential single-tone sinusoid input with frequency ω and phase φ , by applying KCL at the four intermediate mixing nodes (v_1 , v_2 , v_3 , and v_4) as well as the IF output voltage node (v_{out}) in Figure 10, one can arrive at the following system of five first-order differential equations:

$$v'_{\text{out}}(t) = \frac{\frac{v_1(t)}{R_2} + \frac{v_2(t)}{R_3} + \frac{v_3(t)}{R_2} + \frac{v_4(t)}{R_3} - v_{\text{out}}(t) \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right)}{C_L}$$

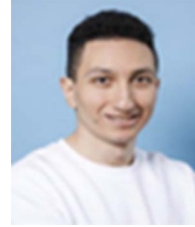
$$v'_1(t) = \frac{\frac{\sin(\omega t + \varphi)}{R_1} + \frac{v_{\text{out}}(t)}{R_2} - v_1(t) \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right)}{C_2}$$

$$v'_2(t) = \frac{\frac{\sin(\omega t + \varphi)}{R_1} + \frac{v_{\text{out}}(t)}{R_3} - v_2(t) \cdot \left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_{\text{on}}} \right)}{C_3}$$

$$v'_3(t) = \frac{\frac{-\sin(\omega t + \varphi)}{R_1} + \frac{v_{\text{out}}(t)}{R_2} - v_3(t) \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_{\text{on}}} \right)}{C_2}$$

$$v'_4(t) = \frac{\frac{-\sin(\omega t + \varphi)}{R_1} + \frac{v_{\text{out}}(t)}{R_3} - v_4(t) \cdot \left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_{\text{on}}} \right)}{C_3}.$$

This system of five first-order differential equations was defined for a mixer quad during one of the phases of the LO when RF_+ is connected to an IF output through a conducting branch consisting of R_2 , as shown in Figure 10. Similar equations can be written using KCL for the three remaining unique phases (namely, RF_+ connected to the IF output through a branch consisting of R_3 and RF_- connected to the IF output through a branch consisting of either R_2 or R_3). The IF output can thus be determined by numerically solving the respective system of differential equations in their respective LO clock phase, using initial conditions from the preceding LO clock phase.



Tariq Ibrahim received his M.Sc. degree (cum laude) from the Delft University of Technology, Delft, The Netherlands, in 2022, where he is currently pursuing his Ph.D. degree. His broad research interests span RF integrated circuits with a special focus on efficient linearization techniques for wideband digital transmitters (DTX).



Mohammadreza Beikmirza received his Ph.D. from the Delft University of Technology, Delft, The Netherlands, in 2023, where he continued his research as a postdoctoral fellow until 2024. He is currently with Nokia Bell Labs in Stuttgart, Germany.



Morteza S. Alavi is an associate professor at Delft University of Technology. His primary research interests include designing single-chip RF integrated circuits (RFICs) for wireless and cellular communication systems and CMOS wireline transceivers. He is a co-author of the book "Radio-Frequency Digital-to-Analog Converter," published by Elsevier in 2016.]



Leo C. N. de Vreede received the Ph.D. degree (cum laude) from the Delft University of Technology, Delft, The Netherlands, in 1996. He is a Full Professor at the Delft University of Technology, where he is responsible for the Electronic Research Laboratory (ERL/ELCA). He has (co)authored more than 170 IEEE-refereed conference papers and journal articles. He holds several patents. His current interests include (digital-intensive) energy-efficient/wideband circuit/ system concepts for wireless applications. Dr. de Vreede was a (co)recipient of the IEEE Microwave Prize in 2008 and a Mentor of the Else Kooi Prize Awarded Ph.D. Work in 2010 and the Dow Energy Dissertation Prize Awarded Ph.D. Work in 2011. He was a recipient of the TUD Entrepreneurial Scientist Award in 2015.