MSc thesis in Electrical Engineering

High Conversion Ratio Hybrid Boost Converter

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Yi-Jan Chiu: High Conversion Ratio Hybrid Boost Converter

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Abstract

DC-to-DC converters have been used in portable electronic applications such as laptops and mobile phones where power efficiency is very important. In these applications, basic converters like buck and boost converters are used. However, the conversion ratio of conventional boost converters is not high. To achieve a high conversion ratio, the duty cycle of the conventional boost converters must be increased drastically, which increases the conduction loss. This thesis presents a topology to tackle this issue. A control system is designed and the pulse frequency modulation (PFM) method is used. In this thesis, a complete analysis of this topology, such as efficiency evaluation and stability analysis, is provided. This circuit is designed in 180nm BCD technology. Simulation results show it has a wide load range (0 to1.8A), high line regulation 0.8%/V, load regulation 2.9%/A, while achieving 88.1%, 93.0%, and 94.8% when CR = 5, CR = 4.5, and CR = 3.7, at I_{out}= 1.2A respectively.

Contents

1 Introduction

1.1 Boost Converter

A boost converter is a type of DC-DC converter that increases the voltage level of a DC input voltage to a higher output voltage level. It works by storing energy in an inductor during the switch's ON time and releasing it to the output during the switch's OFF time. The output voltage can be regulated by controlling the duty cycle of the switch.

Boost converters are a commonly used type of converter in various applications, such as electronic device power supplies, LED lighting, and renewable energy systems. They are popular in power electronics due to their ability to output a higher voltage than the input voltage. Moreover, in renewable energy systems such as solar power, boost converters can be used to elevate the voltage of the generated power to a level suitable for grid connection.

Boost converters are a popular choice for many applications due to their simplicity. However, maintaining high power efficiency is the biggest challenge for high conversion ratio boost converters. The duty cycle D, inductor average current I_L, and output current I_{out} are interrelated as follows:

$$I_L = \frac{I_{out}}{(1-D)} \tag{1}$$

As the conversion ratio rises, the duty cycle of the switch also increases, causing higher current passing through the inductor and switches. This, in turn, leads to higher conduction losses. Furthermore, the elevated voltage stresses on the power semiconductor devices can exacerbate the conduction loss issue, making it even more challenging to maintain high power efficiency.

The challenges discussed above necessitate a new approach to designing high conversion ratio boost converters. The selection of appropriate topologies and components is crucial, as each topology comes with its own limitations, benefits, and trade-offs. Thus, designing an efficient and cost-effective power management circuit requires a thorough evaluation process.

1.2 Thesis Objectives

The primary objective of this thesis is to design a high conversion ratio boost converter that achieves high efficiency while avoiding the use of additional off-chip components to minimize cost. To accomplish this objective, the research will begin with a comprehensive review of existing literature on high conversion ratio boost converters, examining their design principles and operation.

Table 1.1 list the performances of converters published in the literature.

	Analog Devices MAX98390	Huang ISSCC'21	Shin ISSCC'18	Lin ISSCC'20
Input voltage	2.7-5.5	6	2-4.2	2-4.4
Output voltage	10	30	3-5	9-20
Conversion ratio	$\frac{1}{1-D}$	$\frac{2-D}{1-D}$	$\frac{2-D}{2-2D}$	$\frac{2}{1-D}$
Capacitor charging	-	$\varphi 1$	$\varphi 2$	interleave
Number of switches	2	3	5	6
Max. voltage stress	V_{out}	$V_{out} - V_{in}$	$2V_{out} - V_{in}$	V_{out}

Table 1.1: State-of-the-art boost converter comparison [1][2][3][4].

To overcome the high conduction loss issue in high conversion ratio, several alternative topologies have been proposed in the literature. The topology presented in reference [2] is highlighted as a promising solution, as it provides a relatively high conversion ratio without requiring many components. Additionally, the use of a flying capacitor that is charged during phase 1 helps ensure sufficient charge for high conversion ratio applications, making it a more reliable solution.

The specifications of this work are shown in below table.

Supply voltage	14.4V
Supply current	1.2A
Efficiency	90%
Line regulation	1%
Load regulation	3%

Table 1.2: Targeted specifications for proposed boost converter.

1.3 Thesis Organization

This thesis is structured as follows. Section II provides an overview of the state-of-the-art topology design and gives a detailed description of the proposed topology. This section also covers the modeling method for the topology and discusses stability issues. Section III demonstrates the circuit implementation of the proposed boost converter. Section IV shows simulation results, and Section V gives conclusions and discusses possible improvements that could be made in the future.

2 Architecture Overview

This chapter introduces the proposed boost converter's architecture and analyzes the power stage and feedback loop. The first section provides a brief overview of the state-of-the-art topology design, which gives a context for the proposed topology and sets the stage for its evaluation. The proposed topology is described in greater detail in the second section, including its working principle, loss analysis, and the derivation of the modeling. The comparison of different topologies also evaluates the trade-off between efficiency and the cost of the proposed topology in relation to other existing solutions. Finally, timing analysis and small signal analysis of the feedback loop are discussed.

2.1 Converter Architectures

2.1.1 Conventional Boost Converter

The conventional boost converter and the waveform are shown in Figure 2.1.

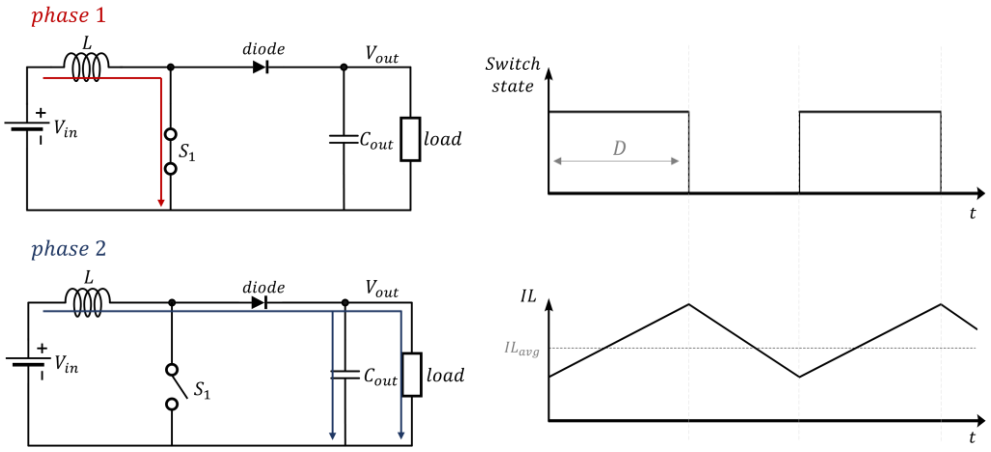

Figure 2.1: Conventional boost converter and waveform of inductor current and switch.

In phase 1, switch S_1 is closed, and the input voltage is applied to the inductor. As per Kirchhoff's circuit law, the inductor current can be expressed as follows:

$$\frac{dI_L}{dt} = \frac{V_{in}}{L} \tag{2}$$

In Phase 2, S_1 opens, and the inductor current starts to decrease gradually while delivering charge to the output capacitor. The inductor current can be expressed as follows:

$$\frac{dI_L}{dt} = \frac{V_{in} - V_{out}}{L} \tag{3}$$

In steady state, the inductor current becomes periodic. Therefore,

$$\frac{V_{in}}{L} \times DT = \frac{V_{in} - V_{out}}{L} \times (1 - D)T \tag{4}$$

where D represents the duty cycle:

$$D = \frac{T_{on}}{T} \tag{5}$$

The equation (4) relates the input voltage V_{in} to the output voltage V_{out} through the conversion ratio CR, which is defined as the ratio of the output voltage to the input voltage. It can be expressed as:

$$CR = \frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{6}$$

This equation shows that the conversion ratio depends on the duty cycle, and as the duty cycle approaches 1, the conversion ratio approaches infinity. However, a duty cycle of 1 is not achievable in practice, as it would require the switch to remain closed indefinitely, resulting in an infinite inductor current and infinite output voltage.

In proposed application, a duty cycle of 0.77 is needed to obtain the desired conversion ratio of approximately 4.5 with a conventional boost converter. Unfortunately, this results in significant conduction losses and necessitates the use of a high voltage-rated switching device, further compounding the problem.

2.1.2 Prior-art Design

Reference [2] proposes a topology, as shown in Figure 2.2, which utilizes a flying capacitor and additional switch to decrease both duty cycle and voltage stress.

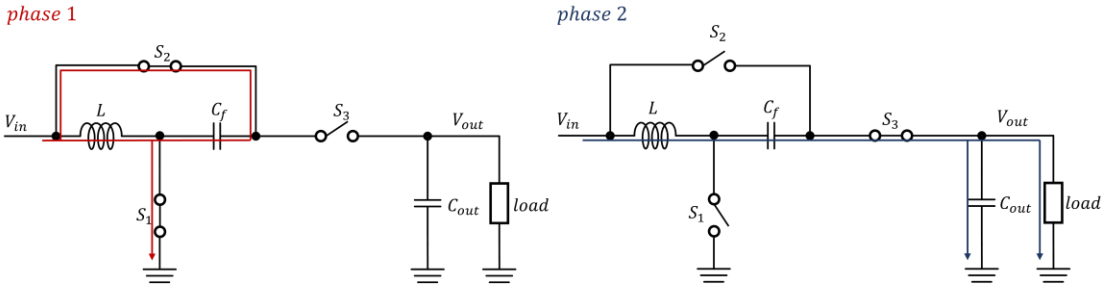

Figure 2.2: Prior art boost converter [2].

The flying capacitor serves two primary purposes in the proposed topology. First, it provides charge to the load during phase 2, ensuring that the charge supply to the output node is sufficient even conversion ratio goes high. Secondly, it reduces the voltage across the inductor. The capacitor is charged to V_{in} during phase 1. This effect results in a higher conversion ratio in this topology.

The inductor behaves the same as the conventional converter in phase 1:

$$\frac{dI_L}{dt} = \frac{V_{in}}{L} \tag{7}$$

During phase 2, thanks to the capacitor charged to V_{in}, the slope of the inductor current is reduced as follows:

$$\frac{dI_L}{dt} = \frac{2V_{in} - V_{out}}{L} \tag{8}$$

Conversion ratio CR can be derived from equation (7)(8):

$$CR = \frac{V_{out}}{V_{in}} = \frac{2 - \mathrm{D}}{1 - \mathrm{D}} \tag{9}$$

This effect alleviates the problem in the conventional converter. In our application, the conversion ratio is 4.5. Compared to traditional boost converters, this topology reduces the average inductor current by 21% and reduces the conduction loss.

Although this topology improves the duty cycle and inductor average current, the conduction loss is still significant, especially in high conversion ratio and high current applications. Consequently, a new topology has been proposed that aims to improve the conversion ratio even further and minimize conduction losses.

2.2 Proposed Boost Converter Architecture

2.2.1 Working Principle

The proposed topology, as shown in Figure 2.3, features several modifications from the prior art topology. Four resistors, namely S_1 through S_4, and an extra capacitor, C_{F2}, are included in the circuit. These additions enable the flying capacitor, C_F, to charge up to $2V_{in}$.

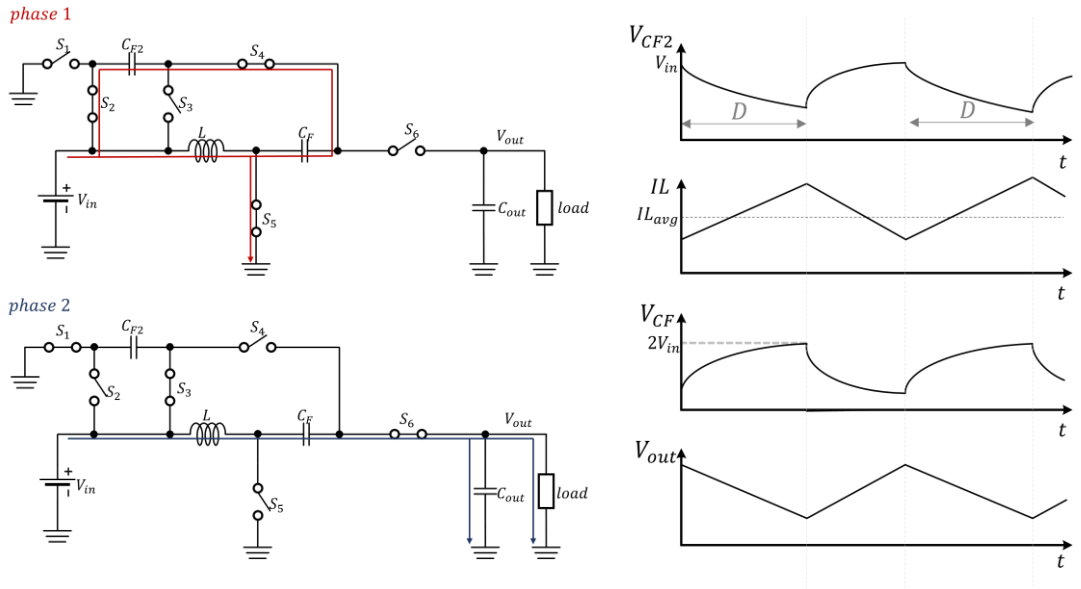

Figure 2.3: Proposed boost converter topology and the waveform of inductor current and capacitors.

The relationship between the input and output voltage can be calculated as follows:

$$CR = \frac{V_{out}}{V_{in}} = \frac{3 - 2\mathrm{D}}{1 - \mathrm{D}} \tag{10}$$

Figure 2.4 depicts the variations in the inductor current and duty cycle across the three different topologies. The inductor current plays a crucial role in determining the conduction loss and power efficiency of the boost converter. Notably, the proposed boost converter exhibits the flattest slope of the inductor current during phase 2, highlighting the significant impact of the additional resistors and capacitors on the inductor current. The decrease in the duty cycle achieved through the extra components effectively reduces the average inductor current, leading to lower conduction loss and a more efficient operation of the converter. In contrast, the other two topologies display a steeper slope of the inductor current during phase 2, indicating higher average inductor current and conduction loss. These findings affirm the superiority of the proposed topology in terms of efficiency.

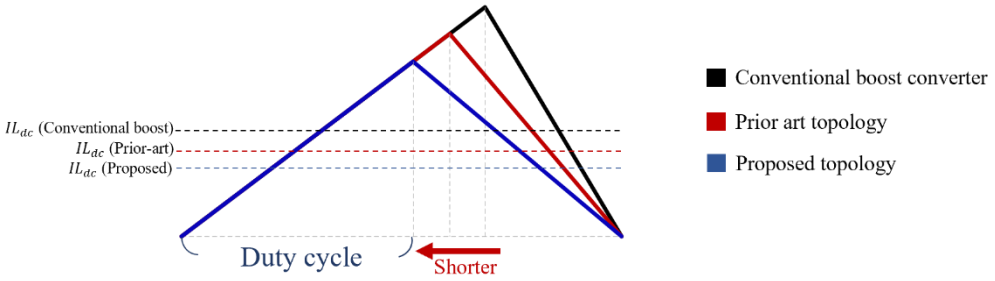

Figure 2.4: Analysis of inductor current and duty cycle in different topologies.

Among these topologies, the proposed one exhibits the lowest duty cycle and average inductor current. Although it includes the highest number of switches compared to the others, later analysis will demonstrate that this trade-off is justifiable due to the improvement in power efficiency.

	Conventional Boost Converter	Huang ISSCC'21	Proposed Topology
Conversion ratio	$\frac{1}{1-D}$	$\frac{2-\mathrm{D}}{1-D}$	$\frac{3-2\mathrm{D}}{1-D}$
Duty cycle when CR=4.5	0.77	0.71	0.6
Inductor current	$4.34I_{out}$	$3.44I_{out}$	$2.5I_{out}$

Table 2.1: Comparison of inductor current and duty cycle.

2.2.2 Loss Estimation

A. Gate charge loss

Gate charge happens while charging and discharging the gate capacitance of power transistors. During one cycle, the power dissipation is given by:

$$E_g = CV^2 \tag{11}$$

B. Switching loss:

Switching loss is considered one of the main losses from switches. It happens when the power transistors switch from on to off state and vice versa. The switching loss is defined as follows:

$$P_{sw} = P_{tr} + P_{tf} \tag{12}$$

where P_{tr} and P_{tf} are the switching loss turns on and off the switch, respectively.

C. Conduction loss

Conduction loss is a type of energy loss that occurs in the conducting components of a power converter, such as switches and inductors. Its impact is particularly pronounced in high conversion ratio converters due to the high voltage differences across the switches and the high current flowing through them. Hence, it is the majority of power loss in a converter and can have a significant impact on its efficiency.

The proposed boost converter has a target efficiency of over 90%. To estimate its efficiency and compare it with the topology in reference [2], the following steps were taken:

First, the conduction loss was evaluated since it dominates the overall efficiency of the boost converter due to the high output voltage and current. The switches were sized to limit conduction loss caused by switches to 5% of the total power.

Secondly, the minimum area for the switches was determined by allocating the area based on their resistance and current while meeting the requirement of limiting conduction loss. This step aimed to minimize the area of the switches while still achieving the efficiency target.

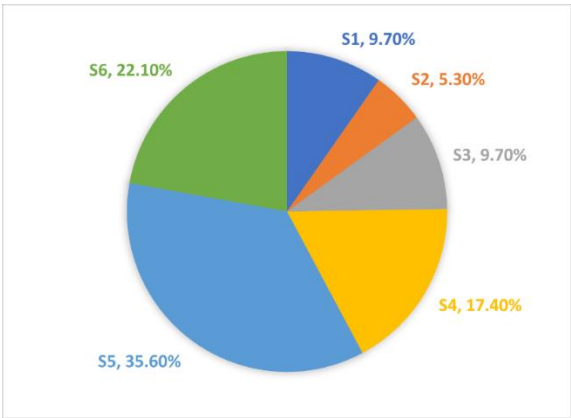

Figure 2.5: The proportion of the area of each switch counts.

According to the results of the minimum area calculation, the proposed boost converter has an area of $0.589\mu m^2$ while meeting the 5% conduction loss limitation. The area distribution of each switch is presented in Figure 2.5.

Table 2.2 shows that the topology in reference [2] has lower conduction loss in its switches while occupying the same area. However, it's important to note that the effect of conduction loss caused by the inductor equivalent series resistance has not been considered yet. Since the inductor carries a large current, the impact of conduction loss caused by the inductor cannot be overlooked.

	Huang ISSCC'21	Proposed topology
Area	$0.589\mu m^2$	
switches' conduction loss (watt)	0.73	0.86

Table 2.2: Comparison of switch's conduction loss in the same area.

Figure 2.6 illustrates the equivalent model of the inductor. Except for the inductor, resistance, and capacitor parallel with it. There are known as equivalent series resistance (ESR) and equivalent series capacitance.

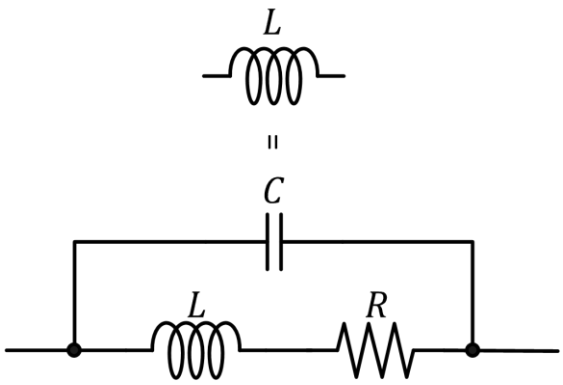

Figure 2.6: Equivalent circuit of an inductor.

The relationship of power inductor's price and its ESR is shown in Figure 2.7. Results show that the inductors with the best price-performance ratio are between 5m-10mΩ.Total inductor resistance can be expressed as follows:

$$R_{ind} = R_{ESR} + R_{bondwire} + R_{PCB} \quad (13)$$

Due to inductor is out-chip, it's necessary to include bond wire resistance and PCB resistance. The bond wire resistance and PCB resistance can both contribute to the conduction loss in the inductor, and it's important to accurately estimate this loss to ensure that the overall performance of the system meets the design requirements.

The resistance of the bond wire is typically around 50mΩ, while the resistance of the PCB is around 10mΩ. These values can vary depending on the specific design of the system and the materials used, but they are commonly used as a rule of thumb.

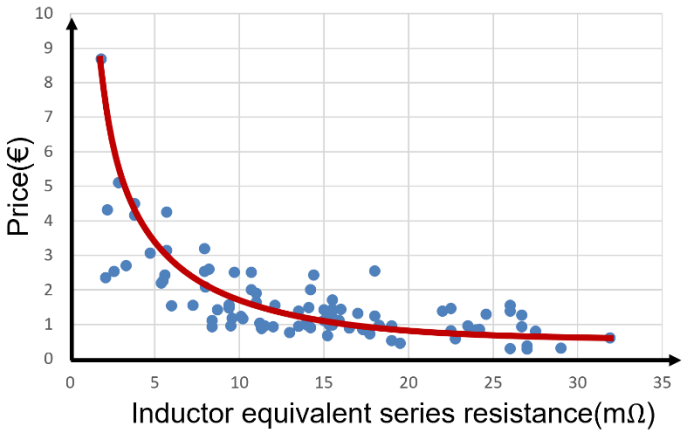

Figure 2.7: Power inductor's price and its equivalent series resistance.

In summary, the proposed topology offers an improved efficiency compared to the prior-art design. The analysis took into account various factors such as switching loss, conduction loss, gate charge loss, and the resistance present in the inductor. The results, which considered the inductor ESR of 5mΩ, the paralleled bond wire of 6.25mΩ, and the PCB resistance of 10mΩ, show that the proposed topology has a 0.3% higher efficiency under the same area.

	Huang ISSCC'21	Proposed topology
Efficiency (%)	92.8	93.1

Table 2.3: Power efficiency of two topologies under the same area.

2.2.3 Modelling

The PWM switch model is commonly used to analyze the stability of DC-DC converters, as it provides a simple and efficient way to obtain the equivalent model [6]. However, the PWM switch model assumes a constant current direction, which makes it unsuitable for stability analysis of proposed converter where the direction of the current is not constant.

Therefore, another method called state-space average modeling is used to estimate the transfer function of the converter and perform stability analysis [7][8].

State-space average modeling uses a different method to obtain equivalent circuit. It has several steps as shown below:

A. Find out the state equations in each phase.
B. Average the equations from step one by using the duty ratio.
C. Add perturbed signals and remove the product of $AC \times AC$ terms.
D. Convert the equations back to the S domain.

By following these steps, control to output transfer function (G_{vd}) can be calculated as follows:

$$G_{vd} = \frac{\widehat{v_{out}}}{\hat{d}} = \frac{-LI_L S + (1-D)(V_{out} - 2V_{in})}{S^2 LC_{out} + S\frac{L}{R_{out}} + (1-D)^2} \tag{14}$$

Note that in the transfer function, a right half plane (RHP) zero gives a -90° phase shift and increases the gain, creating a stability challenge. The standard method to tackle RHP zero is reducing the bandwidth below the RHP zero [9]. Detailed compensation methods will be discussed in the next section.

The calculation results can be verified by SIMPLIS. Bode plot of calculation and simulation results are shown in Figure 2.8, proving that simulation results match our calculation results.

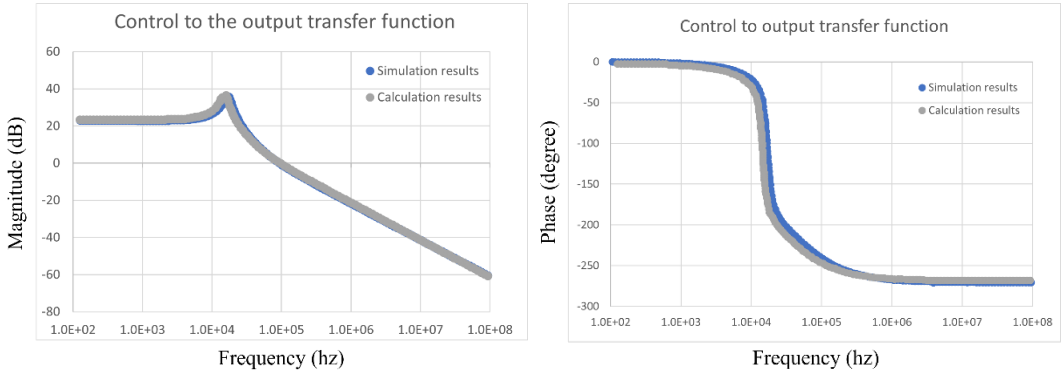

Figure 2.9: Control to the output transfer function.

2.3 Close Loop Architecture

Boost converters require feedback loops to ensure stable and regulated output voltage. The feedback loop is responsible for adjusting the duty cycle based on the difference between the actual output voltage and the desired output voltage. This is particularly important in this system where the boost converter is powered by a lithium-ion battery, as the voltage variation depends on the capacity of the battery, as shown in Figure 2.10 [10][11].

Additionally, the boost converter is supplying power to a speaker, the output current is directly related to the volume, causing changes in the output voltage. This can lead to the speaker malfunctioning or even being damaged. Therefore, feedback is essential in the system to ensure good line and load regulations, which enables the boost converter to deliver a stable output voltage to the load, regardless of changes in the input voltage or output current.

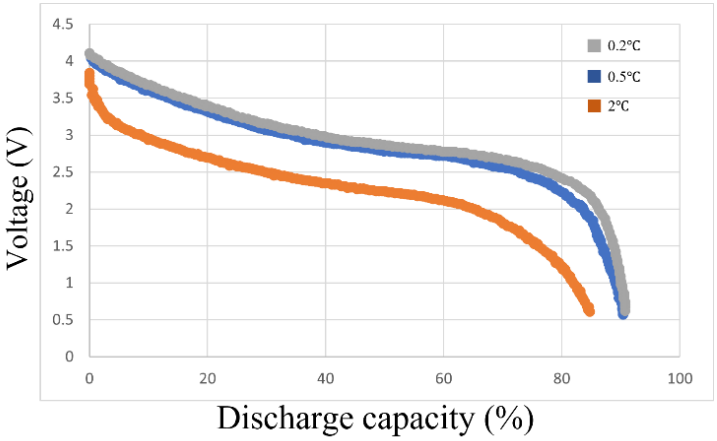

Figure 2.10: Relationship between voltage and capacity [11].

2.3.1 Feedback Loop

Figure 2.11 shows the schematic of the converter. It contains two feedback loops: the current loop and the voltage loop. The inductor current is detected and transformed into V_{IL} voltage signal. In the voltage loop, the output voltage is detected by the resistor chain with gain K. It then sends to the compensator as an error voltage [12]. As the voltage V_{IL} is higher than the error voltage V_{err}, the comparator generates a pulse and triggers the constant time block.

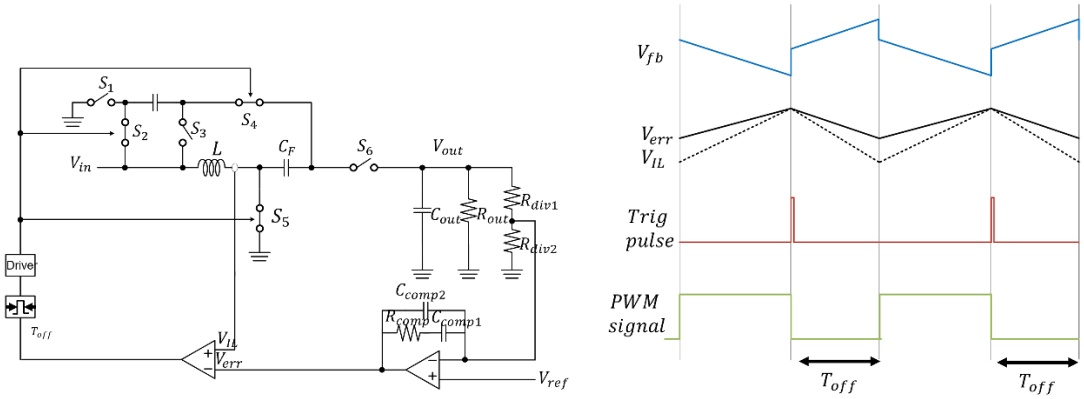

Figure 2.11: Feedback loop and its working principle.

The block diagram is illustrated in Figure 2.12. Total loop gain $T(s)$ can be expressed as follows:

$$T(s) = \frac{T_v(s)}{1 + T_i(s)} \tag{15}$$

$T_i(s)$ and $T_v(s)$ are the current and voltage loop gain functions respectively.

The current and voltage loop gain function can be expressed as follows:

$$T_i(s) = FmG_{di}(s)R_i \tag{16}$$

$$T_v(s) = KA_v(s)FmG_{di}(s)R_o(s) \tag{17}$$

Where Fm is the gain of comparator, R_i is gain of current sense, $G_{di}(s)$ is gain function from duty cycle to inductor current.

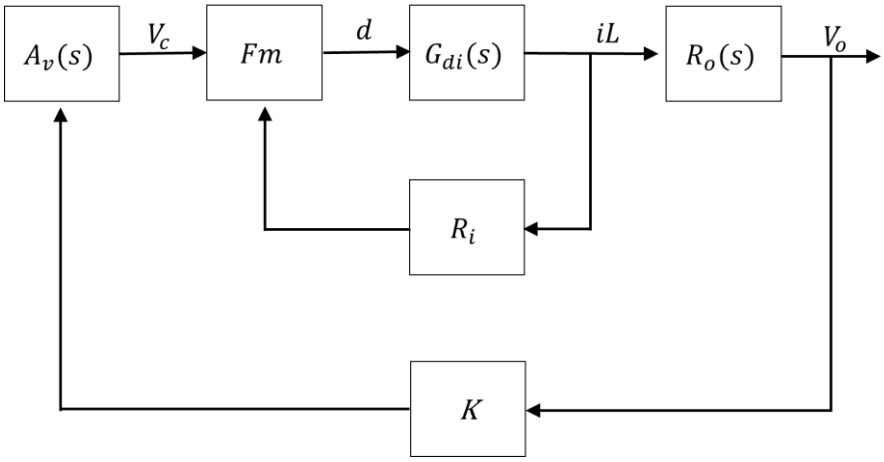

Figure 2.12: Block diagram including power stage and feedback.

Meanwhile, two feedback loops separate and transform the complex conjugate pole into two real poles. The frequency of new poles can be calculated as follows:

$$f_{p\_low} \cong \frac{R_{out}(V_{out} - 2V_{in}) + I_{out}}{2\pi C_{out}(V_{out} - 2V_{in})} \tag{18}$$

$$f_{p\_high} \cong \frac{R_i Fm(V_{out} - 2V_{in})}{L} \tag{19}$$

The frequency of RHP zero is also known:

$$f_{RHPZ} = \frac{(1 - D)(V_{out} - 2V_{in})}{2\pi L I_L} \tag{20}$$

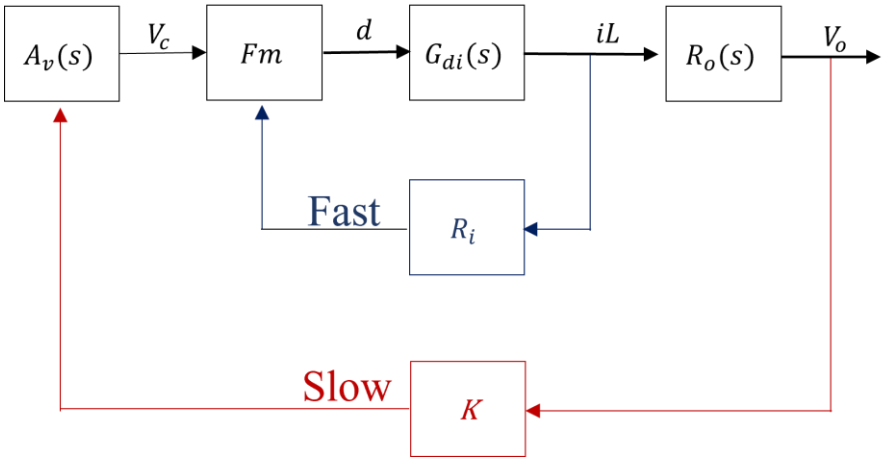

Figure 2.13: Feedback loop and their speed.

2.3.2 Compensator Design

To ensure stability in the feedback loop of the boost converter, a compensator has been included. The compensator increases the low-frequency loop gain to provide high DC regulation and adjusts the crossover frequency f_c to ensure stability by adding an extra zero. Separating the pole f_{p1} and zero f_{z1} improves the phase margin, which is important for stability. The Type II compensator is used in this thesis, and its circuit schematic and transfer function are illustrated in Figure 2.14.

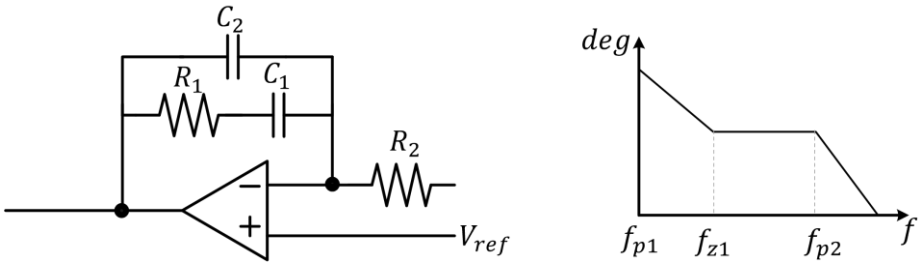

Figure 2.14: Type II compensator and phase in bode plot.

Transfer function and poles and zero frequency can be expressed as follows:

$$H(s) = \frac{(1 + R_1C_1S)}{(R_2C_1S) \times (1 + R_1C_2S)} \ , if\ C_1 \gg C_2$$

$$f_{p1} = \frac{1}{2\pi R_2C_1}$$

$$f_{p2} = \frac{1}{2\pi R_1C_2} \qquad (21)$$

$$f_{z1} = \frac{1}{2\pi R_1C_1}$$

To summarize the results of the previous derivation, it has been found that the high-frequency pole f_{p_high} in the current loop has little effect on stability, while the phase margin is primarily determined by the low-frequency pole f_{p_low} and the right-half plane zero f_{RHPZ}. To compensate for the loss of phase, a zero f_{z1} has been added near the low-frequency pole. Moreover, to avoid any further decrease in the phase, the pole f_{p2} has been placed at a frequency higher than the right-half plane zero f_{RHPZ}.

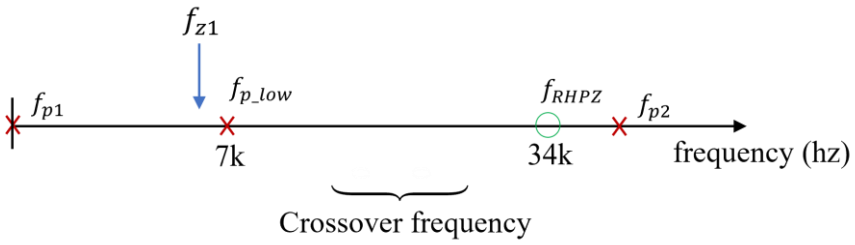

Figure 2.15: Positions of poles and zeros.

Figure 2.16 shows the bode plot of the inverter with an input voltage of 3.6V, an output voltage of 14.4V, and an output current of 1.2A. The crossover frequency f_c is 31kHz, and the phase margin is 56°.

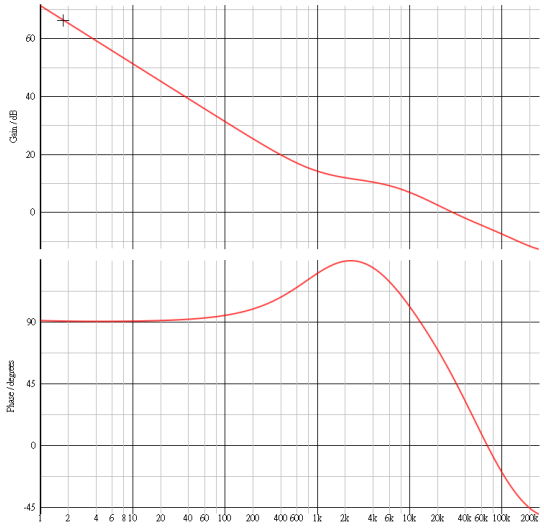

Figure 2.16: Bode plot of converter with compensator.

2.4 Transient Response

The crossover frequency f_c is a crucial factor that influences the transient response of DC-DC converters. As depicted in Figure 2.17, when the output current abruptly changes from 1.2A to 1.8A, the output voltage drops due to the converter's limited ability to react instantaneously. This happens because, at the initial stage, the output capacitor supplies power to the load. Although increasing the output capacitor's size can mitigate this issue, it leads to higher area, cost, and response time, as reported in [16][17].

To estimate the converter's response time, t_r, Equation (22) is used, which indicates that t_r is inversely proportional to the crossover frequency:

$$t_r \cong \frac{0.3}{f_c} \tag{22}$$

For proposed converter, the response time is approximately 9 microseconds, which yields a crossover frequency of around 32 kHz. The derived crossover frequency not only validates the accuracy of the analysis presented in the previous section but also emphasizes the significant effect of the crossover frequency on the transient response in DC-DC converters [15].

Once the feedback loop is activated, it regulates the output voltage. However, the stability, bandwidth, and load regulation of the feedback loop all have a significant impact on the output voltage's fluctuations. In particular, the frequency of the right-half-plane zero, f_{RHPZ}, which is inversely proportional to the output current, causes the phase margin to decrease to 40°, leading to ringing in the output voltage.

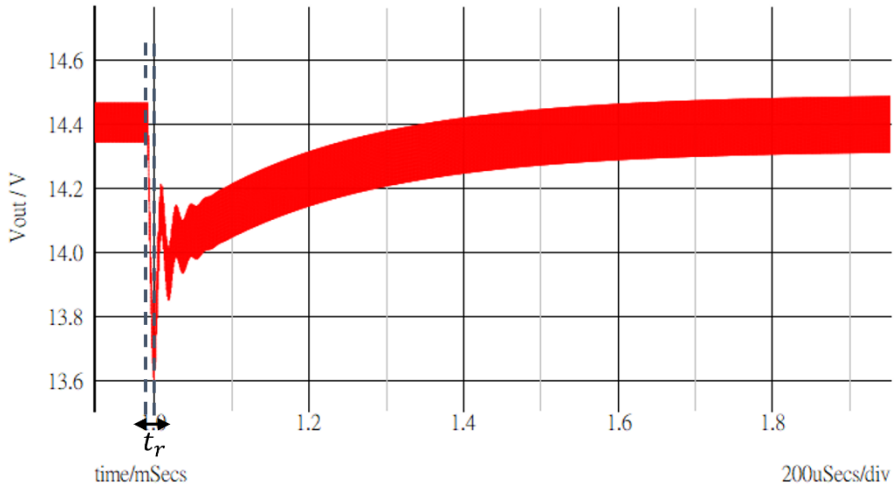

Figure 2.17: Transient response when I_{out} increase from 1.2A to 1.8A.

3 Circuit implementation

3.1 Current-sensing Technique

Shunt sensing is one of the most common ways to sense inductor current, as shown in Figure 3.1. The sensing resistor R_{sense} contributes to conduction loss, which is proportional to the inductor current. This can have a significant impact on the efficiency of the power converter, especially when the inductor current is high.

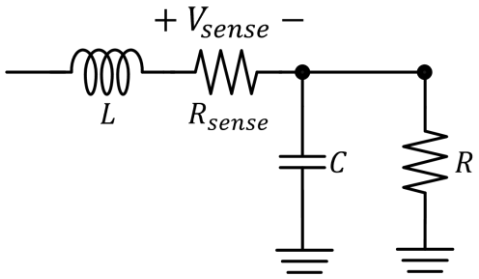

Figure 3.1: Implementation of shunt sensing.

The filter-sense scheme is adopted to avoid the additional conduction loss caused by the sensing resistor [18]. In this scheme, the RC components act as a filter, which eliminates the poles and zeros in the circuit, ensuring that the voltage across the inductor V_c is directly proportional to the inductor current I_L.

The implementation of the filter-sense scheme is shown in Figure 3.2, where an RC component is added in parallel with the inductor. The relationship between detection voltage V_c and RC can be expressed as follows:

$$V_c = \frac{V_L}{1 + sR_{sense}C_{sense}} = I_L \frac{(R_{ESR} + sL)}{1 + sR_{sense}C_{sense}} = I_L R_{ESR} \frac{1 + s(\frac{L}{R_{ESR}})}{1 + sR_{sense}C_{sense}} \quad (23)$$

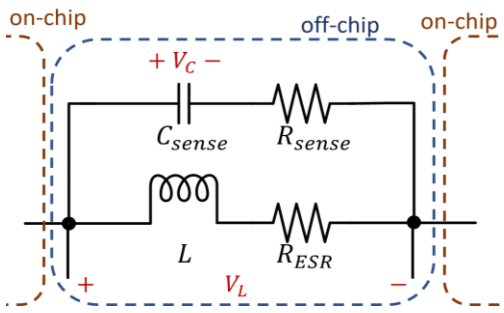

Figure 3.2: Inductor current is detected by RC low pass filter.

3.2 Current Loop Gain

The current loop gain is used to amplify the voltage across the capacitor V_c in current sensing circuit. It allows for a more accurate measurement of the inductor current. As shown in Figure 3.2, voltage V_c is sensitive to the resistance of R_{sense} so that poles and zeros can eliminate each other. In such cases, an alternative amplifier scheme can achieve the desired amplification level are used, as shown in Figure 3.3.

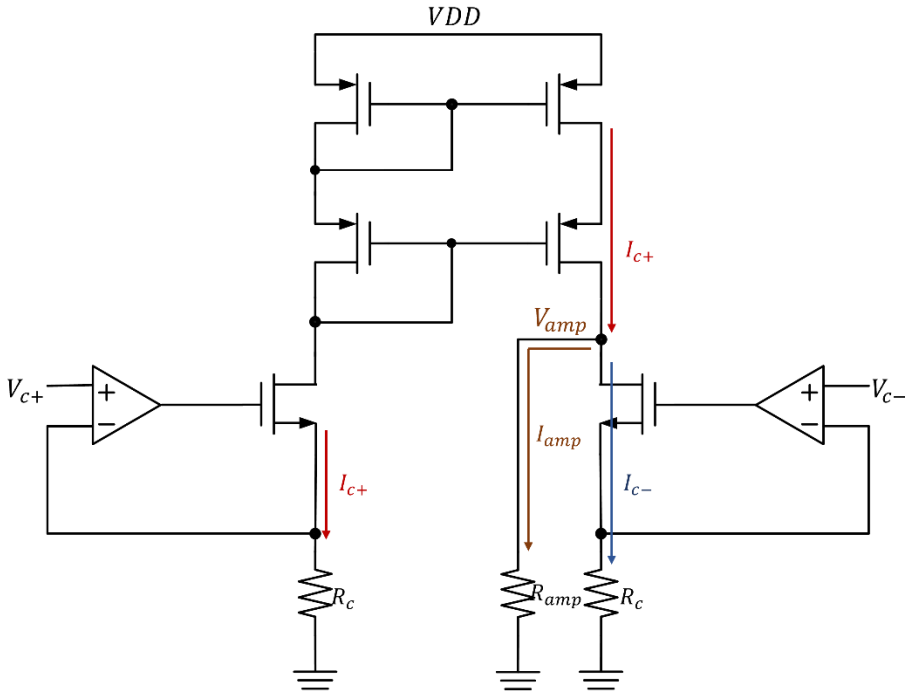

Figure 3.3: Circuit schematic to amplify signal.

The voltage across the capacitor V_c is connected to the positive input of the amplifier, called V_{c+} and V_{c-}, respectively. The high input resistance of the amplifier helps to unacted the value of RC current sensing components. The amplifier converts the V_{c+} signal into a current signal and copies it to the right path, where it is subtracted from the V_{c-} signal to produce a voltage signal V_{amp}. The ratio of R_c and R_{amp} determines the current gain of the amplifier, which can be adjusted to achieve the desired voltage level in the current measurement.

$$V_{amp} = \left(\frac{V_{c+}}{R_c} - \frac{V_{c-}}{R_c}\right) \times R_{amp} = (V_{c+} - V_{c-}) \frac{R_{amp}}{R_c} \tag{24}$$

Figure 3.4 shows the simulation results for the current measurement circuit, where $R_{amp} = 20 \times R_c$. The choice of this ratio is a trade-off between accuracy, and stability, and is based on various factors such as the value of the inductor's equivalent series resistance, inductor current, and duty cycle.

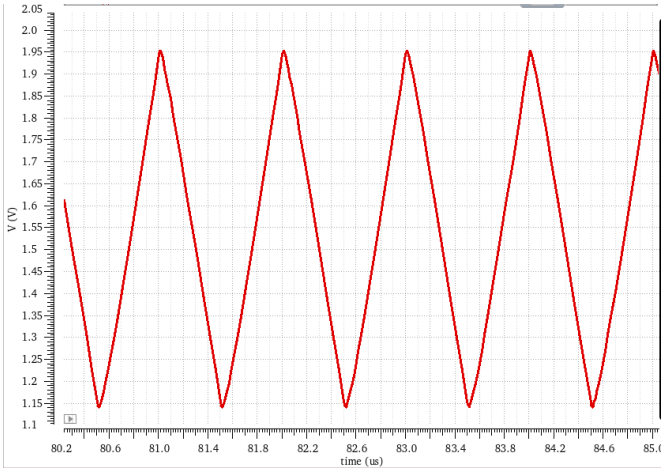

Figure 3.4: Simulation result of current loop gain block.

3.3 Comparator

The comparator is used to trigger the constant time block and control the switching of the boost converter. Hysteresis comparator with positive feedback can achieve faster transient response by adding transistors M_{n2} and M_{n3}.

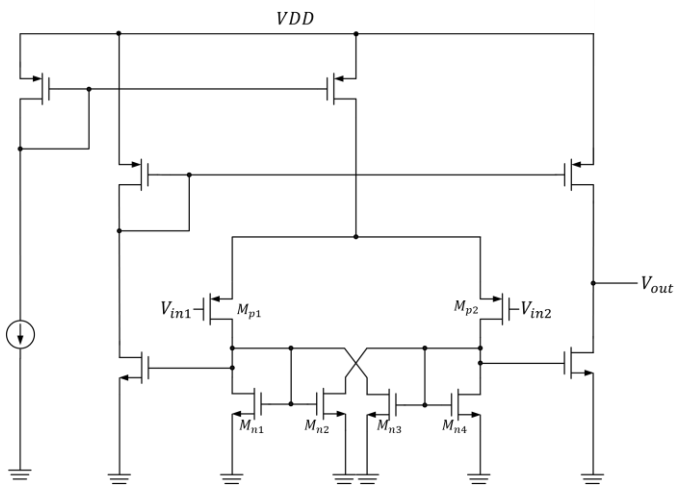

Figure 3.5: Hysteresis comparator with positive feedback.

The delay of the comparator is a crucial factor that can negatively affect the phase margin of the converter. The relationship between delay and lost phase margin can be derived as follows:

$$\frac{Delay}{Period} = \frac{lost\ PM}{360°} \tag{25}$$

Despite using a hysteresis comparator with positive feedback, simulation results indicate that it still experiences a delay of 14ns. This delay can result in a deterioration of the phase margin by 5.04° while consuming 0.25mW of power, as demonstrated in Figure 3.6.

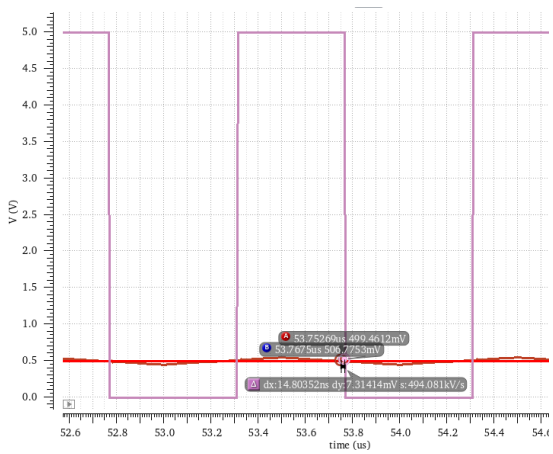

Figure 3.6: Comparison delay of hysteresis comparator.

In order to further reduce the comparison delay, a transimpedance amplifier (TIA) stage is utilized. The TIA stage is implemented by inserting a resistor R_{boost} between the input and output of an inverter, as depicted in Figure 3.7. This leads to a decrease in the amplitude of the signal swings, which in turn reduces the delay time. As illustrated in Figure 3.8, the up delay and down delay are decreased to 1.9 ns and 3.6 ns, respectively. This reduction in the comparison delay can improve the stability of the circuit without requiring additional power consumption.

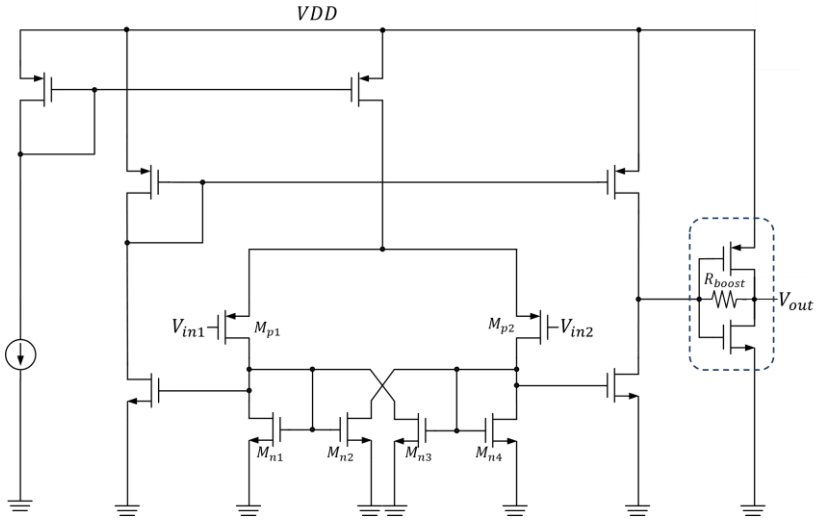

Figure 3.7: Circuit schematic of improved hysteresis comparator.

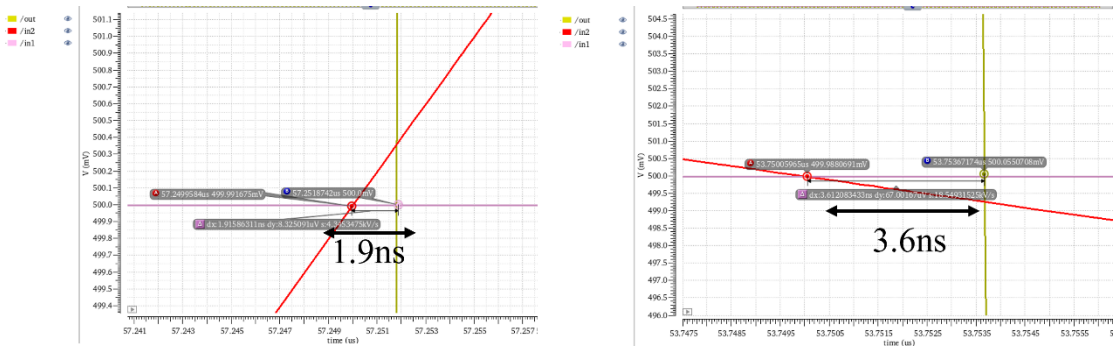

Figure 3.8: Simulation results of improved hysteresis comparator.

4 Simulation Results

The power efficiency of the converter is shown to vary with changes in conversion ratios and loading conditions, as demonstrated in Figure 4.1. The highest efficiency is observed at lower output currents, between 0.2-0.4A, as efficiency decreases gradually with higher output current due to increased conduction loss. The converter achieves a power efficiency of 88.1%, 93.0%, and 94.8% when the conversion ratio is 5, 4.5, and 3.7, respectively, at $I_{out} = 1.2A$.

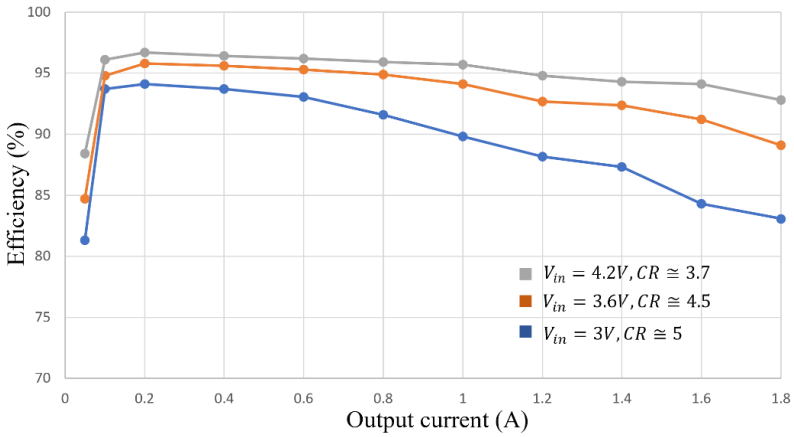

Figure 4.1: Power efficiency of the proposed converter.

Figure 4.2 shows the output voltage level of the converter under different output currents. The load regulation of the converter is calculated as the change in output voltage per unit change in output current. The results show that the load regulation of the converter is approximately -2.9%/A, which indicates that the output voltage decreases by 2.9% for every 1A increase in output current. This load regulation is better than the converter in reference [1], which has a load regulation of -3.0%/A.

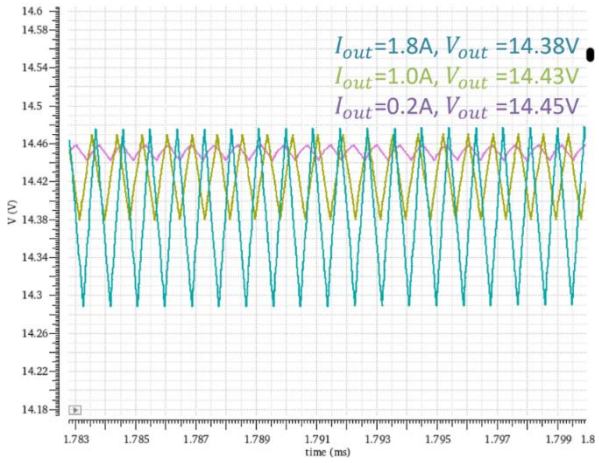

Figure 4.2: Load regulation.

Figure 4.3 shows the output voltage level of the converter with different input voltage. The line regulation of the converter is calculated as the change in output voltage per unit change in input voltage. The results show that the line regulation of the converter is approximately 0.8%. This line regulation is better than the converter in reference [1], which has a line regulation of 1.0%.

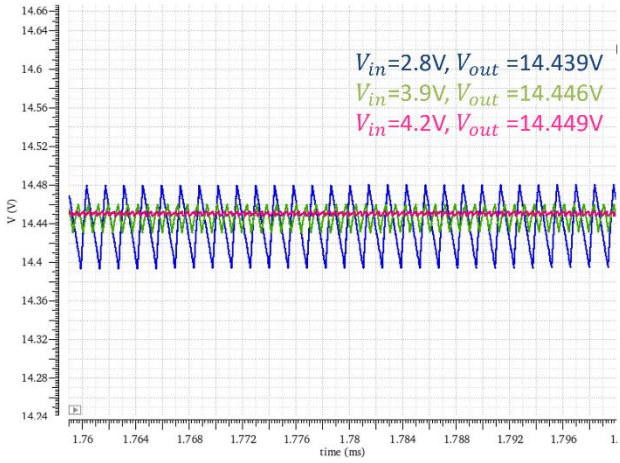

Figure 4.3: Line regulation.

Table 4.1 displays the average output voltage of the converter under different corners. The table shows that the average output voltage changes under different corners, indicating that the output voltage is affected by these environmental and process variations.

	TT	SF	FS	FF	SS
$\overline{V_{out}}$ (V)	14.41	14.40	14.42	14.42	14.40

Table 4.1: Output voltage under the different corners.

5 Conclusions and Future Work

This study aimed to design a high conversion ratio boost converter suitable for mobile applications by evaluating various topologies from existing literature. To achieve better power efficiency under high conversion ratio, a novel topology was proposed, which involved the integration of additional resistors and capacitors to lower the duty cycle and average inductor current. The resulting converter exhibited improved power efficiency compared to existing solutions and avoided the use of additional off-chip components to minimize cost. Additionally, the pulse frequency modulation (PFM) method is implemented in the feedback loop.

Table 5.1 summarizes the achieved performance and gives a comparison with state-of-the-art performance.

	This work (Pre-layout)	Analog Devices MAX98390	Huang ISSCC'21	Shin ISSCC'18	Lin ISSCC'20
Input voltage	2.7-5.0	2.7-5.5	6	2-4.2	2-4.4
Output voltage	14.4	10	30	3-5	9-20
Conversion ratio	$\frac{3-2D}{1-D}$	$\frac{1}{1-D}$	$\frac{2-D}{1-D}$	$\frac{2-D}{2-2D}$	$\frac{2}{1-D}$
Capacitor charging	both	-	$\varphi 1$	$\varphi 2$	interleave
Number of switches	5	2	3	5	6
Maximum voltage stress	$V_{out}-V_{in}$	V_{out}	$V_{out}-V_{in}$	$2V_{out}-V_{in}$	V_{out}
Max efficiency	96.7%	90%	97.4%	97%	93.5%

Table 5.1: State-of-the-art boost converter comparison.

5.1 Future Work

Even though the proposed topology in this thesis has achieved the design targets and has demonstrated higher efficiency compared to prior art design, there is still room for improvement. Some possible areas for improvement are:

- As shown in Figure 4.2, the converter's switching frequency increases when operating with a light load, which results in decreased efficiency. The simulation results show that the converter has higher power efficiency under light-load conditions, but this is due to the reduction in conduction loss rather than switching loss. To address this issue, the constant block should be triggered during the on-time as a constant on-time feedback loop. This change will help reduce the switching loss and improve the overall efficiency of the converter.

- As mentioned in the sections 2.3 and 2.4, the maximum crossover frequency of boost and buck-boost converters is limited by f_{RHPZ}. This results in low bandwidth and slow response time. A feedback loop with a variable f_{RHPZ} would help to increase the bandwidth and accelerate the response time, improving the transient response of the converter.

6 Reference

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