# Low-Power Readout IC for a PMUT-based

# Bladder Scanner

By

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### Abstract

For this project, the operating principle is to transmit an ultrasound wave into the bladder, and estimate the bladder volume by measuring the time interval between the first echo (front wall of the bladder) and the second echo (back wall of the bladder). An ASIC is designed to drive the ultrasound transducer to generate ultrasound pulses, and process the signal (reflected echo) received by the transducer. The ASIC includes 8 transmit/receive front-end circuit, a beamformer, and cable drivers. Each front-end circuit consists of a high-voltage pulser, transmit/receive switch, low-noise amplifier and time-gain compensation amplifier. After layout and tape-out (TSMC 0.18µm), the ASIC has been measured and verified.

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# **1. Introduction**

# 1.1 Project background

Urinary incontinence (UI), which means the loss of bladder control, is an embarrassing problem for elderly people and paraplegia patients. It is more common than people thought. According to a survey, UI was reported by 12.3% of women and 5.4% of men [1.1]. There are several solutions for it, one of which is the use of diapers. But this is expensive, obstructive and has an environmental impact. Treatments are also expensive and involve training, medication, and operations, which all are  $2^{nd}$  and  $3^{rd}$  line treatments. Many UI patients would benefit from a device that could warn them before involuntary urination happens.

### **1.2 Application and prototype device**

A Bladder monitor is a device that automatically warns the user or caretaker when the bladder is (nearly) full. It is a wearable device based on ultrasound technology, which means it is safe and non-invasive. When it is working, it generates ultrasound pulses towards the bladder. The echo from the front wall and back wall of bladder return at a time interval. By measuring that time interval we can estimate the volume of the bladder and based on that we can decide to generate an alarm or not. The working principle is shown in Fig 1-1.



Fig 1-1: Working principle of Bladder scanner [1.2]

A prototype of a bladder monitor has been developed by Novioscan. The Urika Bladder Monitor (UBM) Mini beta prototype uses piezo-electric transducers. The transducers are actuated with electric pulses and generate an ultrasound

wave. The reflected echo are converted into a voltage signal by transducers and is then amplified and digitized. The data is transferred wirelessly to a tablet/phone.



Fig 1-2: UBM Mini prototype[1.2]



Fig 1-3: Block diagram of prototype system [1.3]

The prototype contains a small box (part A) that can be worn on the hip and connects to a separate box (part B) that contains the transducer. Part A contains the electronics that excite the transducer and measure the echo received by the transducer. Part B is fixed to the belly of the patient. Part A and part B are connected using a cable.

The readout circuit of the prototype includes drivers for 8 PZT transducers, T/R switch, a multiplexer, a low-noise amplifier (LNA), TGC (Time Gain Compensation) amplifier, and an ADC. It can excite 8 transducers and measure the echo subsequently, but not simultaneously, and it excludes beamforming. A CPLD (Complex Programmable Logic Device) generates control signals for the system and receives data from the ADC. An SD card is used for data logging. The system also includes a wireless transceiver, volatile memory, and a position sensor. The power consumption of the system is dominated by the wireless communication, which consumes more than 60 percent of total power when all raw data are sent over the bluetooth interface. Fig 1-4 shows the power breakdown per single measurement. Based on the information provided by Novioscan, the calculated active current consumption of analog frontend only is about 300 mA. The active time of the analog frontend and ADC for every single measurement is 0.45 ms. This can be calculated as follows:

$$T = \frac{S}{V} = \frac{2 * 0.35 m}{1540 m/s} = 0.45 ms$$

Where S is two times the maximum detection depth and V is the speed of sound in human body. For wireless communication, the power consumption is derived from an advertisement packet. The power consumption of the low-voltage multiplexer, accelerometer and SD-card are not included.



Fig 1-4: Power breakdown per single measurement (1/min) [1.3]

Several aspects of this prototype need to be improved: First, it contains a box which needs to be worn on the hip, which is not very convenient for the patient. Second, it measures the echo subsequently but not simultaneously, so it excludes beamforming. In this application, beamforming is an important function for the monitor to find the position of the bladder.

# **1.3 Project target**

The goal of this project is to design an application-specific integrated circuit (ASIC), which can drive 8 elements and receive the signal simultaneously. It should be fit into a smaller device as shown in Fig 1-5. The ASIC should be able to steer the ultrasound beam from -45° to +45°. The dynamic range should be 60 dB, with 20 dB variable gain. The beamformer samples the signal at a certain frequency so a sampling frequency needs to be determined. The signal frequency is at 2~2.5 MHz (more details in chapter 2), so a sampling frequency of 10 MHz is enough. To achieve these targets, the ASIC should consist of high-voltage pulsers, T/R switches, LNAs, TGCs, a beamformer and an ADC. The high-voltage supply will be generated off-chip, and functions like position sensing and wireless communication will be excluded. Since the device would be battery powered, the power consumption of the circuits needs to be minimized. The requirements of the ASIC are listed in Table 1-1.



#### Fig 1-5 UBM micro

Specifications	Requirements
Power consumption	Minimal
Beam steering angle	-45° ~ +45°
Dynamic range	60 dB
Variable gain	20 dB

#### Table 1-1: Specifications and requirements of the ASIC

Dynamic range	60 dB
Variable gain	20 dB
Number of channels	8
Noise	< transducer noise
High-voltage supply	30 V
Sampling frequency	10 MHz
Signal frequency	2~2.5 MHz

# **1.4 References**

[1.1] Irwin, Debra E., et al. "Population-based survey of urinary incontinence, overactive bladder, and other lower urinary tract symptoms in five countries: results of the EPIC study." European urology 50.6 (2006): 1306-1315.

[1.2] The Noivoscan Team and G. Rijnders, "NovioScan voor POC," ed, 2015.

[1.3] Internal communication of Novioscan BV.

# 2. Ultrasound transducers

### 2.1 Piezoelectric ultrasound transducers

A piezoelectric ultrasound transducer can transfer energy between the mechanical domain and the electrical domain based on the piezoelectric effect. When an ultrasound wave, which is basically a mechanical pressure wave, is applied to a transducer, polarization of the electrical dipoles in the transducer dielectric occurs along with geometric deformation [2.1]. This creates a net dipole moment and generates an electric field between the two electrodes of the ultrasound transducer, the polarity of which depends on the polarity of the ultrasonic wave [2.2]. Conversely, if an electric pulse is applied to the two electrodes of the transducer, it will vibrate and generate an ultrasound wave. The most widely used Piezoelectric ultrasound transducers are bulk PZT transducers, which is a ceramic perovskite material that shows a conspicuous piezoelectric effect.

### **2.2 PMUT devices**

Piezoelectric Micro-machined Ultrasound Transducers (PMUTs) are an alternative to widely used bulk PZT transducers. Bulk piezoelectric transducers, like bulk PZT transducer (Fig 2-1 (a)), are using thickness variation to generate an ultrasound wave. The resonant frequency of the transducer depends on the thickness of the piezoelectric layer, therefore limits the transducer size for specific applications. As shown in Fig 2-1(b), when a PMUT is transmitting (or receiving), a membrane is vibrating, bent back and forth to generate ultrasound wave[2.3]. Compared to a bulk transducer, the main advantage of a PMUT is its higher bandwidth, which leads to more extensive applications. Moreover, the resonant frequency of a PMUT heavily depends on the size and intrinsic stress of the membrane generated during fabrication, rather than thickness of the piezoelectric layer. The development of PMUT is a potential solution for integrated ultrasound transducer, in which the ultrasound transducer is integrated with supporting electronic circuits. Nowadays, the requirement of miniaturized ultrasound devices is growing, which makes PMUT a promising technology in the future.



Fig 2-1: Typical cross-sectional structures of (a) a bulk piezoelectric ultrasonic transducers; (b) PMUTs [2.3]

### 2.3 ATL P4-1 probe

The initial plan was to use PMUT transducers for the prototype since it could be integrated with the ASIC in the future. The expected resonance frequency of the PMUT is 2 MHz. However, because of the fabrication issues, unfortunately, the PMUT devices will not be ready in the time frame of this project. A commercial ATL P4-1 probe is chosen as an intermediate step to be able to obtain experimental results within the time frame of the project. The design is based on the characteristics of this probe. The ATL P4-1 ultrasound probe is a 96-element phased array transducer for PHILIPS/ATL High Definition Imaging (HDI) series systems. It is used for deep abdominal and obstetrics application with a frequency range from 1 to 4 MHz [2.4], close to the resonance frequency of the PMUT, which will be connected to the ASIC in the future. In this project, we will use 8 out of 96 elements in the array to verify the beamforming function.



Fig 2-2: ATL P4-1 probe

The electrical impedance of a single element has been measured using an impedance analyzer (Fig 2-3). Based on the measurement data we have built an equivalent circuit model for the transducer using ZView 2, which is a software used for data fitting and model extraction [2.5]. Fig 2-4 gives a typical ultrasound transducer model. It includes an RLC resonance tank which consists of Rs, Ls, Cs. A shunting capacitor Cp is in parallel with RLC resonance tank. The values are chosen automatically by the software, Rs  $\approx$  652.9  $\Omega$ , Ls  $\approx$  46.8 uH, Cs  $\approx$  88 pF, Cp  $\approx$  262 pF. Fig 2-5 shows the modeled impedance plot (magnitude and phase) compared to the measured impedance (magnitude and phase).



Fig 2-3: Impedance analyzer



Fig 2-4: Typical impedance model of ultrasound transducer with model parameters



Fig 2-5: Modeled impedance plot (FitResult) compared to the measured impedance

If we use these parameters to calculate the resonance frequency of the RLC circuit, then

$$f = \frac{1}{2\pi\sqrt{LC}} \approx 2.4 \ MHz$$

As we can also see from the fitting result, the central frequency of the transducer is about 2.4 MHz. Cp is 262 pf, which is mainly the capacitance of the 2 meters of coaxial cable (around 100pF/m).  $R_s$  is 652.9  $\Omega$ , so the signal source could be considered as a voltage source. The electrical model the transducer element in the receive mode is shown in Fig 2-6. The voltage source is inserted in the RLC branch.



Fig 2-6: Electrical model of the transducer element in the receive mode

# **2.4 References**

[2.1] J. Karki, "Signal Conditioning Piezoelectric Sensors", Texas Instrument Application Report, SLOA033A, Sept. 2000.

[2.2] R. S. C. Cobbold, Foundations of Biomedical Ultrasound: Oxford University Press, 2006.

[2.3] Qiu, Yongqiang, et al. "Piezoelectric micromachined ultrasound transducer (PMUT) arrays for integrated sensing, actuation and imaging." Sensors 15.4 (2015): 8020-8041.

[2.4] "ATL P4-1 | Forums, Questions, Discussions and Help | MedWrench", *MedWrench*, 2017. [Online]. Available: http://www.medwrench.com/?equipment.view/equipmentNo/6028/ATL/P4-1/.

[2.5] Scribner Associates, Inc., ZView, http://www.scribner.com/software/general-electrochemistry/68-general-electrochemistr/376-zview-for-windows.html (November 2016).

# 3. ASIC System-level design

# 3.1 System architecture

The system architecture is shown in fig 3-1. It includes 8 transducers, 8 transducer front end circuits, a beamformer and a 10-bit ADC. Each front end includes a high-voltage pulser which can excite the transducer with 30 V pulses; a T/R switch which can separate the low-voltage circuit from these high-voltage pulses and switch the transducer connection between pulser and LNA; an LNA which provides part of the gain while introducing noise lower than that of the transducer; two TGCs which provide extra programmable gain; a T/R Timing block which controls the transmit and receive timing. The steering angle of the beamformer is set by a shift register. The outputs of the ASIC are 10-bit parallel digital codes as well as differential analog outputs buffered by two on-chip cable drivers.

There are 4 different voltage supplies given to the ASIC. HV\_VDD is a 30 V supply for the pulsers. VDD5V is a 5 V supply. VDDD and VDDA are both 1.8 V supplies. VDDD supplies power to the digital circuits and VDDA to the analog circuits. There are 3 pins for ground connection, HV\_GND is the ground for the high-voltage circuits, GNDA is the analog ground and GNDD is the digital ground.



Fig 3-1: System block diagram

### **3.2 Transmitting scheme**

The ATL P4-1 probe consists of 96 transducer elements, but in this project, only 8 of them are connected to the ASIC; the others are not used. Each of the 8 elements can be pulsed separately with 30 V pulses generated by the pulser in each channel. The transmit direction can be steered by setting different pulse timing to the elements. Fig 3-2 shows the working principle [3.1]. The element on the right most side is pulsed first. An ultrasound wave spreads out from this element like a ripple on water (largest semicircle). The second element on the right is pulsed next, and generates a wave a little bit later than the first one because it starts later. The procedure continues for the rest of the elements, and multiple waves add up to one single wave front traveling at a certain angle. The transmitting angle can be steered by changing the timing of the pulses. The relation between delay timing and steering angle can be calculated as:

$$T_d = \frac{Pitch \cdot \sin(\theta)}{V_s}$$

 $T_d$  is the delay timing, pitch means the spacing between neighboring elements,  $\theta$  is the steering angle, and  $V_s$  is the speed of sound in human tissue.



Fig 3-2: Principle of transmit steering

#### 3.3 Signal processing scheme

The block diagram of the receiving signal processing architecture is shown in Fig 3-2. It consists of 8 channels followed by a beamformer and an ADC. Each channel includes an LNA and two TGCs. When receiving, ultrasound echoes captured by the transducers are transformed to the electrical domain and amplified by the LNA. The LNA boosts the signal to a proper level to overcome the noise of the following circuits. Then the signal is further amplified by the TGCs, which is basically a variable gain amplifier used to compensate for the energy lost when the ultrasound wave propagates through human body [3.2]. At the output of the TGCs, a beamformer combines all the signals from the different channels. To do so, the beamformer samples and stores the signal of each channel and combines the samples at a proper timing so as to add all signals of different channel constructively. By setting different delay timing

for different channels, the beam direction can be steered. This is a reversed process of transmit steering. The targeted steering angle ranges from  $+45^{\circ}$  to  $-45^{\circ}$ . After the summation, the analog signal is converted to a digital signal by an ADC.



Fig 3-2: Receive signal processing architecture

#### 3.3.1 Time-gain-compensation scheme

The Time-gain-compensation is used to compensate for the power loss when ultrasound signal traveling through the human body. The ultrasound echo reflected from the back wall of the bladder is weaker than the echo reflected from the front wall. In an ideal case, the gain increases gradually with time. However, this requires many gain steps and complex control circuits. In this project, we apply a 3-step compensation scheme for simplicity, each step providing 10 dB gain.



Fig 3-3: (a) ideal TGC scheme, (b) 3-step TGC scheme

#### 3.3.2 Beamforming scheme

To be able to steer the receive beam from +45° to -45°, the beamformer is introduced. The working principle of the beamformer is to apply a delay to the signal of each receive channel so that a signal coming from a particular angle is constructively summed [3.3]. As depicted in Fig 3-4, the ultrasound echo wave front which comes from a particular direction can be assumed as a straight line, assuming the element pitch of the transducer array is small compared to the target distance. The relation between steering angle and delay timing can be calculated using the same equation in section 3.2. Since the signal frequency is about 2.4 MHz, the sampling frequency is set to 10 Ms/s (10 million samples per second) for each channel.



Fig 3-4: Beamformer working principle.

### 3.3.3 Analog to digital conversion

The signal received by each channel is constructively summed by beamformer, giving an overall analog output which represents the detection result of the current beam angle. This analog output is converted to a digital signal by an ADC. Since the beamformer is running at 10 Ms/s, the overall analog output also changes every 100 ns, the ADC should run at this frequency as well. For this application, the required resolution is approximately 10-bit, which corresponds to 60 dB dynamic range. The power consumption of the ADC should be minimized.

# **3.4 References**

[3.1] "File:Phased array beam.svg - Wikimedia Commons", *Commons.wikimedia.org*, 2017. [Online]. Available: https://commons.wikimedia.org/wiki/File:Phased\_array\_beam.svg.

[3.2]Z.YU, *Low-Power Receive-Electronics for a Miniature 3D Ultrasound Probe*. TU Delft, Delft University of Technology, 2012.

# 4. Transistor-level design

In chapter 2, the characteristics of transducer have been discussed, and in chapter 3 the system-level decisions have been made. There are requirements for different blocks in the system. Based on these requirements we proceed with the transistor level design, which will be discussed in this chapter.

### 4.1 HV-Pulser design

The ASIC is connected to 8 transducers, each of which should be able to send a pulse independently, so we put a HVpulser in each channel. The requirements are based on the characteristics of the transducer. The design requirements and circuit implementation are discussed below.

#### 4.1.1 Design requirements and choices

To generate an ultrasound wave of sufficiently high pressure, high-voltage pulsers are required. We excite the transducer with a 30 V peak-to-peak square wave at 2~2.5 MHz. The output current of each pulser should be able to charge and discharge the load between 30 V and 0 V at this frequency. The high-voltage supply will be provided off-chip, and the transmit timing should be controlled by a low-voltage signal. There are several solutions to convert a low-voltage control signal to high-voltage domain [4.1.1][4.1.2]. However, the solutions either require a high V<sub>gs</sub> (30 V) or a extra high-voltage supply. The source-gate voltage of a double diffused metal oxide semiconductor (DMOS) transistor in our technology cannot exceed 5 V [4.1.4], and an extra high-voltage supply is also not desired in this application. In this project, a push-pull structure with level-shifters is chosen [4.1.3].

#### **4.1.2 Pulser Implementation**

The high-voltage pulser architecture is shown in Fig 4.1-1. It includes an output stage and two level shifters. The output stage consists of a high-voltage NMOS transistor (M8\_HV) and a high-voltage PMOS transistor (M7\_HV). They work as an inverter which can push the drain voltage to the high-voltage supply (30 V) or pull it down to HV\_GND (0 V) [4.1.3]. The DMOS transistors are designed such that they can endure very high  $V_{ds}$ , but be aware that the maximum  $V_{gs}$  is only 5 V.

The HV\_NMOS and HV\_PMOS need to be driven by signals which determine the transmit timing, transmit beamforming, and frequency. TXN and TXP are the signals driving the HV\_NMOS and HV\_PMOS, respectively. The reason for using two signals instead of one is that they are driving different transistors and some timing restrictions are required, which will be discussed later. Both of them are 0~1.8 V signal, so we need level shifters to lift the voltages to a proper level.

The circuit of the level shifter for the HV\_PMOS is shown in Fig 4.1-2 (a). To drive the HV\_PMOS, this circuit transfers the 0~1.8 V pulse at the input to a 25~30 V pulse at the output, which is connected to the gate of HV\_PMOS.

M1\_HV and M2\_HV are high-voltage transistors because they need to endure 30 V drain to source voltage. M3, M4, M5, M6 are low-voltage devices because the maximum  $V_{ds}$  they will handle is 5 V. The W/L ratio of the two diode-connected transistor M4 and M6 is chosen to ensure that the drain voltage of these transistors will not go below 25 V.

The circuit of level shifter for HV\_NMOS is shown in Fig 4.1-2(b). It is a simpler circuit because it only needs to shift  $0 \sim 1.8$  V input to  $0 \sim 5$  V output. All four transistors are low-voltage transistors. The TXP and **TXP** are complementary to each other, same for TXN and **TXN**.



Fig 4.1-1: High-voltage Pulser architecture.

The output transistors M7\_HV and M8\_HV must not turn on simultaneously, which means TXP should go high before TXN goes high, and TXN should go low before TXP goes low. For this purpose, we have built a T/R timing circuit, which generates proper signals as well as controls the transmit and receive timing. As shown in Fig 4.1-3, the input signal TX\_HIGH is transformed and becomes TXP and TXN. For TXP, the falling edge is delayed, and for TXN, the rising edge is delayed. This is achieved by placing unbalanced inverters, which have one long and narrow transistor while the other one is short and wide. The TX\_EN signal is used to the control transmit timing. When it goes low, TXN goes low and TXP goes high, so that both transistors in the output stage are turned off. The **RX\_EN** turn off M8\_HV in the pulser when receiving, so that the output of the pulser is high impedance.



Fig 4.1-2: (a) Level shifter for HV\_PMOS and (b) Level shifter for HV\_NMOS.



Fig 4.1-3 Signal generation, T/R timing circuit.

#### **4.1.3 Pulser Simulation results**

The schematic simulation result is shown in Fig 4.1-4. The output of the Pulser is loaded with the electrical model of the ATL P4-1 transducer, which has a 260 pF shunt capacitor. The rising edge is about 100 ns, and falling edge is about 50 ns. This slaw rate ensure that the pulse can goes up to 30 V and drop back to 0 V at 2.5 MHz. Observing the wave carefully, we can notice that for the rising edge, the voltage does not go directly to 30 V, but hesitates at about 29 V and then goes to 30 V gradually. The same behavior happens at the falling edge, where it needs some time to goes from 0.5V to 0 V. This is because there is a RLC branch in the transducer model.



Fig 4.1-4: Pulser schematic simulation result.

The post-layout simulation result is shown in Fig 4.1-5. Compared to schematic output (blue), the rise and fall times of post-layout output (red) are slightly longer. This is due to the parasitic capacitors and resistors in level shifters circuits. The power consumption of the pulser consists of two parts: level-shifters and output stage. The current of the level-shifters is 260  $\mu$ A when the pulser is transmitting, and 10 uA when it is not transmitting. The current of the output stage is depends on the load capacitor and how many pulse cycles do we need, it charges the load capacitor (260 pF) from 0 V to 30 V in 100 ns. If we send 1 pulse every 200  $\mu$ s, the average current would be 39  $\mu$ A. When it is not transmitting, the static current is only 50 nA.



Fig 4.1-5: Post-layout simulation result (red) vs schematic simulation result (blue).

#### 4.1.4 References

[4.1.1] Tang, Hao-Yen. "High Voltage Level-Shifter Circuit Design for Efficiently High Voltage Transducer Driving." (2014).

[4.1.2] I. O. Wygant *et al.*, "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 55, no. 2, pp. 327-342, February 2008.

[4.1.3] D. Zhao *et al.*, "High-voltage pulser for ultrasound medical imaging applications," *2011 International Symposium on Integrated Circuits*, Singapore, 2011, pp. 408-411.

[4.1.4] *TSMC 0.18 UM CMOS HIGH VOLTAGE MIXED SIGNAL BASED GENERATION II BCD 1P6M SALICIDE AL\_FSG 1.8/5/6/7/8/12/16/20/24/36/45/55/65/70V/VG1.8/5V AND 5/6/7/8/12/16/20/24/29/36/45/55/65/70V.VG5V DESIGN RULE*, 1st ed. TSMC.

### 4.2 LNA and T/R switch design

In chapter 3, the signal process scheme has been discussed. In the receive path, a low-noise amplifier (LNA) is responsible for the preliminary amplification of the signal. In this chapter, we will discuss the design of the LNA and the T/R switch, which is used to protect the low-voltage circuits from high-voltage pulses. Design requirements and circuit implementation will be discussed below.

#### 4.2.1 Design requirements and choices

The duty of LNA is to boost the signal to a higher level while introducing noise lower than that of the transducer. In other words, after the signal is boosted by the LNA, the transducer noise will still be dominant at the output. Before we give a certain number for the LNA noise, we need to know the noise of the transducer. Fig 4.2-1 shows the electrical model of the ATL P4-1 transducer and its parameters values. The only noise source of this circuit is  $R_s$ , so the spot noise  $V_n$  is:

$$V_n = \sqrt{4kTR_s} \cong 3.3 \ nV/\sqrt{Hz}$$

This noise is the thermal noise generated by R<sub>s</sub>, but only part of it transferred to V<sub>n</sub>':

$$V_n' = \frac{Z_{Cp}}{R_s + Z_{Ls} + Z_{Cs} + Z_{Cp}} V_n \cong 0.9 \ nV / \sqrt{Hz}$$

The impedance Z of capacitors and inductor are calculated at 2.4 MHz. The noise requirement of LNA is that the output noise should be dominated by  $V_n$ '. The closed-loop gain of LNA is decided to be 20 dB. And the power consumption should be minimized.



Fig 4.2-1 Electrical model of ATL P4-1 transducer.

At the resonance frequency, the source impedance of the signal is  $R_s$ . Since the source impedance is relatively small, a voltage amplifier is desired as shown in Fig 4.2-2. The feedback network is chosen to be capacitive for the noise

concern. The LNA is expected to be the most power-consuming block of the front-end circuit. Since we need to minimize the power consumption, a differential amplifier or multi-stage amplifier are not preferred because they consume more power than the single-stage single-ended amplifier. If the closed-loop gain of the LNA is 20 dB, it means to achieve a 20 dB loop-gain the open-loop gain should be at least 40 dB at the signal frequency range, which is  $2\sim2.5$  MHz. In the meanwhile, a larger input transconductance is preferred because it lowers the thermal noise of the input transistors, which is usually the main contributor of noise. In summary, we need a single-ended single-stage structure which can provide high gain and high transconductance  $g_m$  with high current efficiency. Finally, a cascoded inverter-based single-ended structure is chosen as the operational trans-conductance amplifier (OTA) [4.2.1]. The specifications and requirements are listed in table 4.2-1.



Fig 4.2-2 LNA architecture

T 11 / A 1	TATA			1	•
$\Gamma_{0}$ h $(1/2)$ $1 \cdot$		torgat	anontiontiona	and	roguiromonte
1 a D C 4.2-1.	LINA		SUCCIFICATIONS	anu	TEQUITETIENS
1 4010 112 11			opeen en		

Specifications	Requirements
Input-referred noise	$\sim 0.9 \text{ nV} / \sqrt{Hz}$
Power	Minimize
Signal source	Voltage source
Close-loop gain	20 dB
Signal frequency	2~2.5 MHz

#### 4.2.2 LNA and T/R switch Implementation

The circuit of the LNA is shown in Fig 4.2-3. The OTA consists of 4 transistors, M1~M4. M1 and M4 are input transistors, M2 and M3 are cascode transistors. The feedback network consists of C<sub>1</sub>, C<sub>1</sub><sup>'</sup>, C<sub>2</sub>, C<sub>2</sub><sup>'</sup>. The input and

feedback capacitors are split into two equal pairs. In this way, the gate bias voltage for the NMOS and PMOS transistors can be separated [4.2.1]. The closed-loop gain becomes:

$$A_{cl} = \frac{1}{2} \left( \frac{C_1}{C_2} + \frac{C_1'}{C_2'} \right)$$

Where  $C_1 / C_2 = C_1' / C_2'$ ,  $C_1 = C_1' = 5.6$  pF,  $C_2 = C_2' = 560$  fF. To achieve high current efficiency, the input NMOS and PMOS are biased at the subthreshold region. The parasitic capacitor at the gate of the input PMOS is charged to a bias voltage  $V_{refp}$  at auto-zero (AZ) phase, which is also the transmit phase, and holds this voltage when the auto-zero finishes. A1 is a DC-control opamp that set the DC bias voltage of the  $V_{out}$  to  $V_{dd}/2$  during the AZ phase. To avoid noise from this DC-control opamp, the DC-control loop is disconnected after the auto-zero. In the receiving phase, the OTA operates at the "memorized" bias condition stored on the parasitic capacitors at the gate of the NMOS and the PMOS. The bias voltages are periodically renewed every transmitting period. The transmit/receive cycle is about 200 ~ 400  $\mu$ s, the parasitic capacitors at the gate of the NMOS and PMOS are recharged, which guarantees the effectiveness of this technique because the leakage is small enough compared to the recharging period. The DC-control opamp is no more than a differential pair, as shown in Fig 4.2-4. Since the bandwidth and noise requirement are much lower than the OTA, the power consumption of the DC-control opamp is negligible.



Fig 4.2-3 Schematic of the LNA.



Fig 4.2-4 Schematic of the DC-control opamp.

The input of the LNA cannot be connected directly to the transducer because the high-voltage pulses generated by HVpulser will damage the low-voltage circuits if they connected directly. We need a circuit which can separate the transducer and LNA when transmitting, and connect them when receiving. The T/R switch is designed for this purpose. The circuit is shown in Fig 4.2-5. It consists of 3 transistors. HV\_NMOS is a clipping transistor, which makes sure that its source voltage will not exceed 5V. NMOS\_5V is the switch, which is controlled by signal RX\_EN. NMOS\_2V is used to ground the input of the LNA when transmitting. The on-resistance of HV\_NMOS and NMOS\_5V should be small enough so that the noise contribution is negligible compare to the LNA input-referred noise. In this design the total on-resistance of HV\_NMOS and NMOS\_5V is 60 Ω.



Fig 4.2-5 Schematic of the T/R switch

#### 4.2.3 LNA Simulation results

The AC-analysis of the LNA is shown in Fig 4.2-6. The open-loop gain at around 2.4 MHz is 42 dB and the closedloop gain of that is about 18 dB, the load capacitor is 500 fF. To achieve the noise requirement, the current consumed by the LNA is 1.84 mA, of which 1.68 mA is consumed by the input transistors of the OTA. The PSD of the noise is shown in Fig 4.2-7. The spot noise is about  $1 nV/\sqrt{Hz}$ . The integrated input referred noise is about 1.5  $\mu$ V<sub>rms</sub> when the band is chosen from 1 MHz to 3 MHz. This is an acceptable noise level compare to the transducer noise, which is 1.3  $\mu$ V<sub>rms</sub>. As mentioned above the T/R switch also contribute noise. The integrated input-referred noise rises to 1.9  $\mu$ V<sub>rms</sub> if the T/R switch is included. This is still an acceptable result. The 3 dB bandwidth of the LNA is 300 MHz as a result of a large amount of current is consumed for noise suppression. The bandwidth should be limited to avoid noise folding. The performance summary of LNA and T/R switch is listed in Table 4.2-2.



Fig 4.2-6 AC-analysis of the LNA. The green curve is open-loop transfer function and the red curve is closed-loop transfer function.



Fig 4.2-7 Power spectrum density of input-referred noise of LNA

Specifications	Performance
Input-referred noise	1.5 $\mu$ V <sub>rms</sub> (1.9 $\mu$ V <sub>rms</sub> with T/R switch included)
Current consumption	1.84 mA
Close-loop gain	18.5 dB
-3 dB Bandwidth	300 MHz

Table 4 2-2. LNA	and T/R	switch	performance	summary
1 auto 4.2-2. LINA	and 1/K	Switch	performance	Summary

# 4.2.4 References

[4.2.1] Chen, Chao, et al. "A compact 0.135-mW/channel LNA array for piezoelectric ultrasound transducers." European Solid-State Circuits Conference (ESSCIRC), ESSCIRC 2015-41st. IEEE, 2015.

# 4.3 TGC amplifier design

After the signal experiences a 20 dB amplification through the LNA, more gain is still needed. This is achieved by cascading more amplifier stages following the LNA. The time-gain compensation (TGC) amplifiers are designed for this purpose. The TGC amplifiers are not only providing extra gain to the signal but also can provide variable gain. The design of TGC amplifier will be discussed below.

#### 4.3.1 Design requirements and choices

Along with providing more gain, the signal distortion caused by the amplifier and common-mode noise or spikes coupled from digital lines need to be suppressed. Besides, the noise performance of the TGC amplifier is not as critical as the LNA, which means the power consumption of the TGC amplifier would be much smaller than the LNA. The reasons above lead us to use fully-differential OTA as our TGC amplifier structure. Of course, the power consumption still needs to be minimized. Since the signal has already been amplified by the LNA, the noise requirement of TGC amplifier is much relaxed. As long as the input-referred noise of TGC amplifier is less than the output-referred noise of the LNA, it will not make a significant contribution. The bandwidth of the TGC amplifier should be at least larger than signal bandwidth, and the closed-loop gain steps are chosen to be 10 dB, 20 dB. The target specifications of TGC amplifier are listed in Table 4.3-1. Since minimizing the power is still important and we already have some experience with inverter-based OTA, the structure is again chosen for TGC amplifier. However, instead of using a single-ended structure as we did for LNA, here we use a fully-differential structure for our TGC amplifier. Two TGC amplifiers are cascaded to achieve more overall gain and variable gain steps.

Specifications	Requirements
Input-referred noise	$<19 \ \mu V_{rms}$
Power	Minimize
Signal source	Voltage source
Close-loop gain	10/20 dB
Signal frequency	2~2.5 MHz

Table 4 3-1.	TGC amplifie	r target specifi	ications and	requirements
1 able 4.3-1.	10C amplifie	a larget specifi	ications and	requirements

#### **4.3.2 TGC Implementation**

To avoid the extra noise and power consumption caused by resistive feedback, the feedback circuit for TGC amplifier is purely capacitive. As shown in Fig 4.3-1, switches(S) are used for changing the feedback factor to realize variable

gain settings. AZ switches are used to define the common-mode voltage at the input of the OTA during transmit, and "memorize" the voltage during receive. The common-mode voltage for the TGC amplifier is  $V_{dd}/2$ , which is 900 mV. The Ci = Ci'=510 fF, C1 = C1' = 51 fF, C2 = C2' = 102 fF. When S is opened, the closed-loop gain is Ci/C1 = 20 dB. When S is closed, the close-loop gain is Ci/(C1+C2) = 10 dB. The switches are minimum size NMOS switches.



Fig 4.3-1 Feedback implementation of TGC amplifier

The OTA for the TGC amplifier is shown in Fig 4.3-2. M1 and M4 are positive input transistors, M1' and M4' are negative input transistors. M2, M2', M3, M3' are cascode transistors. M0 is the tail current source. The common-mode feedback (CMFB) is realized by resistors and capacitors combined with M5 as shown in the figure. The common-mode voltage depends on the drain current and W/L ratio of M5. Since the feedback network is purely capacitive, the input terminals of the OTA is isolated in terms of DC. To avoid the drifting of the input operating point when receiving, the pseudo-resistors are introduced. The pseudo-resistors are connected between the positive input and negative output, also between the negative input and positive output. The implementation of the pseudo-resistor is shown on the bottom-right of Fig 4.3-2. Given its high impedance, it only effects the transfer function of the TGC amplifier at very low frequency.



Fig 4.3-2 OTA structure for TGC amplifiers



Fig 4.3-3 Amplification stages of front-end circuit.

The complete diagram of amplification stages is shown in Fig 4.3-3. It consists of 3 stages: LNA, TGC1, TGC2. The gain steps of the complete diagram are 40 dB, 50 dB, 60 dB. Each of these stages has a dedicated auto-zero signal. To prevent charge-injection from affecting the DC-point, the AZ signal for LNA finishes first. Also the AZ' finishes before AZ" finishes. This arrangement makes sure that the moment one of the stages finishes the auto-zero, the following stages are still in auto-zero status.

#### 4.3.3 TGC Simulation results

The AC-analysis of the TGC amplifier is shown in Fig 4.3-4. The green curve is open-loop transfer function, in the signal band the gain is about 40 dB. The red and yellow curves are close-loop gains of 10 dB and 20 dB settings, respectively. The load capacitor is 500 fF. The unity-gain frequency of the TGC amplifier is about 350 MHz. The PSD of the input-referred noise of TGC amplifier is shown in Fig 4.3-5. The spot noise at 2.4 MHz is about **6.2**  $nV/\sqrt{Hz}$ . The integrated input-referred noise is about 11  $\mu$ V<sub>rms</sub> when the band is chosen from 1 MHz to 3 MHz. The performance of the TGC amplifier is summarized in Table 4.3-2.



Fig 4.3-4 AC-analysis of the TGC amplifier. The green curve is open-loop transfer function, the red and yellow curves are close-loop transfer functions.



Fig 4.3-5 Power spectrum density of input-referred noise of TGC amplifier.

Specifications	Performance
Input-referred noise	$11 \ \mu V_{rms}$
Current consumption	300 µA
Close-loop gain	9.1 dB / 18.2 dB
-3 dB Bandwidth	173 MHz / 52 MHz

Table 4.3-2: TGC amplifier performance summary

# 4.4 Beamformer design

After the ultrasound signals received by 8 transducers have been properly amplified by the LNA and the TGC amplifiers in the front-end circuits, the output signals of the TGC amplifiers need to be summed up. Due to the fact that the signal will not be received by the transducers at the same time when the steering angle is not 0, a proper delay has to be applied when we sum up the output signals of the TGC amplifiers. The beamformer is designed for this purpose. The design requirements, architecture and operation principles will be discussed below.

#### 4.4.1 Design requirements and choices

Before we dive into the details of the beamformer design, a choice has to be made between digital beamforming and analog beamforming. The implementation of a digital beamformer is shown in Fig 4.4-1. The advantage of a digital beamformer is that it can be very precise. Once the data from each channel have been digitized, they can be delayed and summed flexibly [4.4.1]. This leads to the requirement that there should be a dedicated ADC for each channel. The typical power consumption of a 10-bit ADC running at 10 Ms/s is several milli-Watt [4.4.2][4.4.3]. This inevitably increases the power consumption of the ASIC compare to no dedicated ADC in each channel. On the other hand, analog beamforming is more energy efficient. The implementation of an analog beamformer is shown in Fig 4.4-2.



Fig 4.4-1 Digital beamformer implementation.



Fig 4.4-2 Analog beamformer implementation.

As shown in Fig 4.4-2, the analog beamformer delays the analog outputs of TGC2 and adds them in the analog domain. There is no dedicated ADC for every channel. The analog beamformer is chosen for this project due to the power concern. The analog delay line is just a capacitor bank, which is the so-called "pipelined-sampled delay" principle [4.4.6], or the time-interleaved S/H delay [4.4.4]. An alternative possible approach is based on cascading all-pass filter cells [4.4.7], but there are two limitations for this approach. Firstly, the gain error of these filter cells accumulate and result in different gains for different delay settings. Secondly, it is difficult to modify the group delay of an all-pass filter once it is fixed, so this approach shows poor adaptability. The output could be summed by a charge integrator as illustrated in [4.4.4], or by simply routing the output of all delay lines together as illustrated in [4.4.5]. The later method is chosen for this project since it is simple and power efficient.

The maximum delay of each delay line is calculated based on the maximum steering angle we want to achieve. As listed in Table 1-1, the maximum steering angle is **45°**. The maximum delay of each delay line is calculated as follow:

$$d_{max} = \frac{p \cdot Sin(45^\circ)}{v} \cong 1.4 \ \mu s$$

The pitch p is the distance between adjacent elements, which is assumed to be  $\frac{\lambda}{2} = 0.375 \text{ mm}$ , where  $\lambda$  is the wavelength of the ultrasound wave . The speed of sound v in the water is about 1500 m/s. So the maximum delay needed is 1.4 µs, which means 200 ns delay between adjacent channels. The sampling frequency is 10 Ms/s, which means we need 15 capacitors for each channel to achieve 1.4 µs maximum delay. In addition, the summation phase also takes 100 ns, so we need 16 capacitors in every delay line. In this application, a steering angle resolution of **10°** is

enough. When the delay increases in fixed steps (25ns) between adjacent elements, the steering angles are listed in Table 4.4-1. As we can see, the steering angles are not uniformly increased even though the delay steps are. The biggest step for steering angle is 8.7°, which happens between the 175 ns and 200 ns delay steps. The noise of the beamformer should be lower than the output noise of TGC2, which is about 200  $\mu$ V<sub>rms</sub>. The type of noise that the beamformer introduces is kT/C noise. The capacitor size in the capacitor bank is chosen to be 250 fF, which results in a noise voltage of 130  $\mu$ V<sub>rms</sub>. The target specifications are listed in Table 4.4-2.

Delay steps	Steering angles
25 ns	5.7°
50 ns	11.5°
75 ns	17.5°
100 ns	23.6°
125 ns	30°
150 ns	36.9°
175 ns	44.4°
200 ns	53.1°

Table 4.4-1 Delay steps vs steering angles

Table 4.4-2 Target specifications and requirements of beamformer

Specifications	Requirements
Input referred noise	~200 µV <sub>rms</sub>
Power	Minimize
Sampling frequency	10 Ms/s
Fixed delay step size	25 ns
Programmable delay range	0 ~ 200 ns

#### 4.4.2 Beamformer architecture and operation principles

The circuit diagram and the clock pattern of the pipelined-sampled delay line is shown in Fig 4.4-3. The circuits of the delay line for each element are completely the same. It consists of 16 sampling capacitors, 16 sampling switches and 16 summation switches. The signals are sampled and summed at 10 Ms/s. The capacitors sample the signal one by one with a time interval of 100 ns. After all the capacitors have sampled, the first capacitor samples again. The time interval for renewing the same capacitor is 1.6 us. Similar to the sampling scheme, the summation time interval is also 100 ns, and the time interval before the same capacitor sums is also  $1.6 \,\mu$ s. The pulse width of the sampling signal is set to 50 ns, which is long enough for TGC amplifier to settle the output on the sampling capacitor.



Fig 4.4-3 Pipelined-sampled delay line circuit and its clock pattern.

To understand the operation scheme better, we explain the procedure from another perspective. For instance, we select the first capacitor in every delay line to form a memory group, so in total 8 capacitors in the group. These capacitors all belong to different elements. In the summation phase, they all connect to the output at the same time. There are 16 of this kind of memory groups. We depict one of those groups in Fig 4.4-4. The inputs of these capacitors connected to the outputs of TGC2 of the different elements. The clock pattern for applying a 25 ns delay and 50 ns delay are shown on the right. The capacitors sample the signal of each channel according to the delay setting, and connect to the output

all together in the summation phase after all the capacitors have finished their sample for this round. The delay step can be increased up to 200 ns, with 25 ns resolution.



Fig 4.4-4 Capacitors from the same memory group and their clock pattern.



Fig 4.4-5 Beamformer block diagram.

The block diagram of the complete beamformer is shown in Fig 4.4-5. Each memory group has a dedicated sample & sum clock generator to control the sample and sum switches. The output of the 6-bit counter is feed into the sample & sum clock generator. The block diagram of the sample & sum clock generator is shown in Fig 4.4-6. It consists of 9 digital comparators, which generate a pulse when the inputs are equal. The delay for each channel is set by a delay code register. The sum signal also generated by a digital comparator and a code register. There are 16 sample & sum clock generators in the beamformer and they share the same shift register. The higher 4-bit of the 6-bit counter are added from 0 to 15 for memory group 1 to 16 respectively before send into the sample & sum clock generator, this makes sure the sampling interval for one element is 100 ns. The final design has a fully-differential structure, so there are two delay lines for every channel.



Fig 4.4-6 Sample & sum clock generator block diagram.

#### 4.4.3 Beamformer simulation results

The simulation result of the beamformer is shown in Fig 4.4-7. The delay step is set to 25 ns. The upper strip shows the waveforms of the 8 inputs, and the bottom strip shows the waveform of the beamformer output. The inputs waveforms have a frequency of 2 MHz and amplitude of 1.2  $V_{ppd}$  (peak-to-peak differential), and 25 ns delay between adjacent channels. The amplitude of the output waveform is about 1.05  $V_{ppd}$  due to the sampling frequency is only 5 times higher than the signal frequency. Another simulation result is shown in Fig 4.4-8. The delay step is set to 175 ns, and the delay between adjacent channels are set to 175 ns as well. The output waves of the two figures are identical, which is reasonable because only the delay settings and input timings are changed. The power consumption of the beamformer is 4.7 mW. The power is consumed mainly in the 6-bit counter and the digital comparators.

Fig 4.4-9 shows an unconstructive summation. The delay is set to 175 ns for the beamformer while the delay of the input signal is 25 ns. The highest amplitude of unconstructive output is only about 75 mV, while the constructive output is about 500 mV. The amplitude of the middle part of the output is lower because in that period the signals sign of the elements are different, which results in a smaller output after averaging.







Fig 4.4-8 Simulation result of 175 ns delay setting.



Fig 4.4-9 Simulation result of 175 ns delay setting, but the input signals have 25 ns delay.

#### 4.4.4 References

[4.4.1] Z.YU, *Low-Power Receive-Electronics for a Miniature 3D Ultrasound Probe*. TU Delft, Delft University of Technology, 2012.

[4.4.2] Shen, Junhua, and Peter R. Kinget. "A 0.5-V 8-bit 10-Ms/s pipelined ADC in 90-nm CMOS." *IEEE Journal of Solid-State Circuits* 43.4 (2008): 787-795.

[4.4.3] Kang, Joshua J., and Michael P. Flynn. "A 12b 11MS/s successive approximation ADC with two comparators in 0.13µm CMOS." *2009 Symposium on VLSI Circuits*. 2009.

[4.4.4] Kim, Jae-Hwan, et al. "Time-interleaved sample clock generator for ultrasound beamformer application." SoC Design Conference (ISOCC), 2011 International. IEEE, 2011.

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[4.4.6] Stefanelli, Bruno, et al. "An analog beam-forming circuit for ultrasound imaging using switched-current delay lines." *IEEE Journal of Solid-State Circuits* 35.2 (2000): 202-211.

[4.4.7] Gurun, Gokce, et al. "A tunable analog delay element for high-frequency dynamic beamforming." 2009 IEEE International Ultrasonics Symposium. IEEE, 2009.

# 4.5 Analog to digital conversion

After the received signal has been amplified and sampled and added together properly, it still needs to be digitized. Unfortunately, due to the time issue, the ADC cannot be implemented on the chip in the time frame of this project. It means the output of the chip would be analog only, but the choice of the ADC type will be discussed below.

#### 4.5.1 ADC architecture choice

At the output of the beamformer, the analog signals are converted to digital signals by an ADC. The ADC should have a 10-bit resolution and 10 Ms/s sampling frequency, and the power consumption should be minimized. In this project, a successive approximation register ADC (SAR ADC) is chosen because it is suitable for moderate speed, moderate resolution, and low-power application. Moreover, a charge-sharing SAR ADC is selected because its structure inherently cooperates well with the beamformer. A basic charge-sharing SAR ADC architecture is shown in Fig 4.5-1[4.5.1]. The capacitors  $C_{sp}$  and  $C_{sn}$  are sampling capacitors. In this project, the beamformer combines 8 capacitors to the output in the summation phase, these capacitors automatically become the sampling capacitors of the ADC, so that the dedicated sampling capacitors for ADC can be eliminated. This is the main advantage of using a charge-sharing SAR ADC in this project, its decreases the power consumption because there is no need for buffering amplifiers which are used to drive the sampling capacitors. All the capacitors in the beamformer have a value of 250 fF, which means the equivalent sampling capacitors for the ADC is 2 pF. Though the effectiveness of this value of sampling capacitors still needs to be verified in the future design.



Fig 4.5-1 Basic charge-sharing SAR ADC architecture.

#### 4.5.2 References

[4.5.1] Craninckx, Jan, and Geert Van der Plas. "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90nm digital CMOS." *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*. IEEE, 2007.

# 4.6 Chip layout

The layout of the front-end circuit is shown in Fig 4.6-1. It consists of HV\_Pulser, T/R Switch, T/R Timing, LNA, TGC1 and TGC2. The layout of the completed chip is shown in Fig 4.6-2. It consists of 8 front-end circuits, beamformer, shift register, output buffer and the current mirror. Fig 4.6-3 shows the die photo of the chip.



Fig 4.6-1 Layout of the front-end circuit.



Fig 4.6-2 Layout of the completed chip.



Fig 4.6-3 Die photo of the ASIC.

# 5. Measurements

After the schematic design and layout, the chip has been taped-out and measured. In this chapter we will discuss the measurement methods and results.

# **5.1 Electrical measurements**

To measure the ASIC, a PCB is designed, which is shown in fig 5.1-1. The functions of the connectors are indicated on the picture. The HV supply and LV supply connectors are connected to 30 V and 7 V supply respectively. A FPGA board is connected to the PCB to generate the clock and the control signals for the ASIC. The FPGA board we are using is Altera DE2-115.



Fig 5.1-1 PCB for measurement.

#### 5.1.1 Transmit measurement

To test the transmit functionality, the FPGA is programmed to generate the TX\_HIGH signals (Fig 4.1-3) for the ASIC. A single high-voltage pulse that generated by the ASIC is shown in Fig 5.1-2. The pulse has a 200 ns pulse-width and the amplitude is 30 V. Fig 5.1-3 and Fig 5.1-4 shows the 8 pulses generated by 8 different front-end circuits,

with 25 ns delay and 200 ns delay respectively. All the measurements are loaded with ATL P4-1 probe. The measurement results are very close to the simulation result (Fig 4.1-4). The voltage goes up to 30 V in 100 ns, keep that level for about 150 ns, then goes back to 0 V in 100 ns. The results show that the pulser can send out 2.5 MHz pulses properly.



Fig 5.1-2 A High-voltage pulse generated by the pulser, which is loaded by ATL P4-1 probe.



Fig 5.1-3 8 High-voltage pulse with 25 ns delay generated by the pulsers, which are loaded by ATL P4-1 probe.



Fig 5.1-4 8 High-voltage pulse with 200 ns delay generated by the pulsers, which are loaded by ATL P4-1 probe.

#### 5.1.2 Receive measurement

To test the receive path of the ASIC, we give a single-period sine wave to the ASIC. The input signal frequency is 2 MHz with peak-to-peak amplitude of 10 mV. The ASIC is set in test-mode, in which all the 8 inputs connected together, the steering angle is set to 0°, and the overall gain is set to 40 dB. The output of the ASIC is shown in Fig 5.1-5. The peak-to-peak amplitude of the measurement result is 480 mV, but there is no guarantee that the maximum and minimum level of the sinewave had been sampled, so the gain calculation cannot be based on this value.

The measured transfer functions for different gain settings are shown in Fig 5.1-6. At the ASIC input, a continuous sinewave is applied and the output waveform is transferred to the frequency domain by means of FFT. The gain is calculated by comparing the highest components of the input FFT result and the output FFT result. Because of the sinc filter caused by sample and hold behavior, the transfer functions have a notch at the sampling frequency fs, which is 10 MHz. Due to the folding around the first component of the sampling frequency, there is also a pit at around 5 MHz, which is fs/2. The 60 dB transfer function is not shown here. Since the LNA defines its operating dc point when the auto-zero phase finish, the continuous signal will exceed the output range because the dc point is not in the middle of the supply, and the distortion will make the result looks horrible. Instead, the gain of 60 dB setting is tested using a single-period sine wave. The measured result is 48 dB at 2.3 MHz. The measured gain of different settings are lower than the simulation results, the sinc function contributes 2 dB at 2.3 MHz, but it only explained part of the gain loss, it needs to be further investigated.



Fig 5.1-5 ASIC output when the input is a single-period sine wave.



Fig 5.1-6 Measured transfer function for 40 and 50 dB gain setting.



Fig 5.1-7 Two single-period sine wave applied to ch1~4 and ch5~ch8 with 725 ns delay, (a) the beamformer not applying any delay between ch1~4 and ch5~ch8, and (b) the beamformer applying 725 ns delay between ch1~4 and ch5~ch8.



Fig 5.1-8 Output noise PSD

To test the functionality of the beamformer, two input signals are used. One of the signals is applied to ch1~ch4, while the other one is applied to ch5~ch8 with 725 ns delay. Both of them are a single-period sine wave. Fig 5.1-7(a) shows the output of the ASIC when the beamformer does not apply delay between the channels. The output waveform clearly shows 2 single-period sine waves with 725 ns delay. After we set the delay to 725 ns between ch1~ch4 and ch5~ch8, the 2 waves merged to 1 wave with doubled amplitude as shown in Fig 5.1-7(b).

The noise of the receive path is tested by connecting the inputs of the ASIC to ground, the output PSD is shown in Fig 5.1-8. The noise is integrated from 1 MHz to 3 MHz and calculated input-referred noise is  $18 \,\mu V_{rms}$ . This number is much higher than the simulated noise of the receive path, which is only 2.6  $\mu V_{rms}$ . The reason for this is that the bandwidth of the TGC amplifier (173 MHz) is much higher than the sampling frequencies (10 MHz) and the noise at higher frequency folded back to the signal band. The total power consumption of the ASIC is about 36 mW.

The performance summary is listed in Table 5.1-1. The total power consumption is 36 mW, in which 31 mW is consumed by the front-end circuits. The overall gain at 2.3 MHz is 32/40/48 dB. The -3 dB bandwidth is limited by sinc function for both case.

The Simulated power consumption of every part of the circuit is shown in Fig 5.1-2. The power of pulser, LNA, and TGC amplifier are the power consumption for one front-end circuit, since we have 8 of them, the numbers need to be timed by 8 if we want to calculate the total power. The main contributor to the total power consumption is the LNA, the power is consumed for good noise performance.

Specifications	Measured performance	Simulated performance
Input-referred noise (1 MHz to 3 MHz)	$18 \ \mu V_{rms}$	2.6 μV <sub>rms</sub>
total power consumption(one pulse every 200µs)	36 mW	36 mW
Power consumption per channel	4.5 mW	4.5 mW
Overall gain	32/40/48 dB	37/46/54 dB
-3 dB Bandwidth	~2.3 MHz	~3 MHz

Table 5.1-1 performance summary of the ASIC

Circuit	Power consumption
Pulser (one pulse every 200 µs)	0.09 mW
LNA	3.3 mW
TGC amplifier	0.5 mW
Beamformer	4.7 mW

# Table 5.1-2: Simulated power consumption of every part of the ASIC.

# **5.2 Acoustic measurements**

The setup for acoustic measurements is shown in Fig 5.2-1. A plastic box is filled with water. A hole is opened on the side wall of the box and sealed by a membrane. The ATL P4-1 probe is placed inside the hole. The target is a copper cylinder with 0.4 mm diameter, hanging on a wooden stick. The stick can move in a semicircle which has a center right above the probe, and the target can move alone the stick.



Fig 5.2-1 Acoustic measurement setup.



Fig 5.2-2 ASIC output when the target is placed at -10° and 13 cm in front of the probe, the beamformer is set to 25 ns delay.

Fig 5.2-2 shows the measurement result when the target is placed at  $-10^{\circ}$  and 13 cm in front of the probe, the beamformer is set to 25 ns delay. The echo is received after 170 µs and has an peak-to-peak amplitude of about 2 V.

The directivity plot is measured by fixing the steering angle of the beamformer and changing the angle of the target. The measured results are shown from Fig 5.2-3 to 5.2-10, together with the simulated results. The directivity plot of 0°, 25° and 50° looks normal, but from 75 ns and higher delays, the side lobe becomes more and more significant. The reason for that needs to be further investigated. Since the transducer element pitch is 0.295 mm, which is different from our estimation, the steering angles under certain delay are also different. Table 5.2-1 shows the steering angle based on 0.295 mm element pitch. The maximum amplitude angle of the directivity plots matches with the calculated value. The steering angle of 200 ns is a complex number because the delay distance is bigger than element pitch, so the directivity plot is not shown here.

Delay steps	Steering angles
25 ns	7.3°
50 ns	14.7°
75 ns	22.4°
100 ns	30.6°
125 ns	39.5°
150 ns	49.7°
175 ns	62.8°
200 ns	-

Table 5.2-1 Delay steps vs steering angles (based on 0.295 mm pitch)



Fig 5.2-3 Directivity plot of 0 ns delay setting, measurement result on the left, simulation result on the right.



Fig 5.2-4 Directivity plot of 25 ns delay setting, measurement result on the left, simulation result on the right.



Fig 5.2-5 Directivity plot of 50 ns delay setting, measurement result on the left, simulation result on the right.



Fig 5.2-6 Directivity plot of 75 ns delay setting, measurement result on the left, simulation result on the right.



Fig 5.2-7 Directivity plot of 100 ns delay setting, measurement result on the left, simulation result on the right.



Fig 5.2-8 Directivity plot of 125 ns delay setting, measurement result on the left, simulation result on the right.



Fig 5.2-9 Directivity plot of 150 ns delay setting, measurement result on the left, simulation result on the right.



Fig 5.2-10 Directivity plot of 175 ns delay setting, measurement result on the left, simulation result on the right.

### **5.3 Human test**

We also did some measurements on the human body. I drink some water, wait for 40 min, then use the probe to find my bladder. The ASIC is set to 40 dB gain and 25 ns delay. Fig 5.2-11 shows the measurement result of  $\frac{1}{2}$  cup of water after 40 min. The first echo happened at 25  $\mu$ s and the second echo happened at 80  $\mu$ s. They are very likely the front wall and the back wall of the bladder. The distance between the two objects are calculated as follow:

$$d = \frac{v * t}{2}$$

"v" is the speed of sound in the water which is 1500 m/s, t is time difference which is 55 µs in this case. The result is divided by 2 because of the return path. The distance is 4.1 cm according to the data. Fig 5.2-12 shows the measurement result of 2 cups of water after 40 min. The calculated distance is 7.5 cm. Fig 5.2-13 shows the result after urinate, but the second echo is not very obvious. The bladder is hard to find when it becomes smaller, this is the best result I can get.



Fig 5.2-11 Measurement result of <sup>1</sup>/<sub>2</sub> cup of water after 40 min.



Fig 5.2-12 Measurement result of 2 cup of water after 40 min.



Fig 5.2-13 Measurement result after urinate.

# 6. Conclusions

This thesis shows the design of a readout IC for an ultrasonic bladder scanner. In this chapter, we will discuss the conclusions and future works for this project.

# **6.1 General Conclusions**

For this project, the operating principle is to transmit an ultrasound wave into the bladder, and estimate the bladder volume by measuring the time interval between the first echo (front wall of the bladder) and the second echo (back wall of the bladder). An ASIC is designed to drive the ultrasound transducer to generate ultrasound pulses, and process the signal (reflected echo) received by the transducer. The ASIC includes 8 transmit/receive front-end circuit, a beamformer, and cable drivers. Each front-end circuit consists of a high-voltage pulser, transmit/receive switch, low-noise amplifier and time-gain compensation amplifier. After layout and tape-out (TSMC 0.18 µm), the ASIC has been measured and verified.

The transducer we are using is not a PMUT array, but a commercial probe ATL P4-1. We select 8 out of 96 elements for this project. They seem to work properly in the measurements.

The pulser is designed to drive the big capacitance of the transducer. The PMUT transducers are expected to have an even larger capacitance (~900 pF). It means the pulser may need to be redesigned if the ASIC is connected to PMUT transducers.

The LNAs in the front-end circuits consume more than 70 % of the total power for good noise performance. But since the bandwidth of the TGC amplifier is not limited, the noise of the ASIC is much higher than we expected.

For the TGC amplifiers, we applied a three-step discrete-gain scheme instead of using a continuous time-gain compensation scheme. This highly simplified the TGC amplifier design. But the bandwidth is too high (173 MHz), which is a big drawback for noise performance.

The beamformer is designed so that the beam angle can be steered. It is important for the device to find the position of the bladder. The beamformer is initially designed to have a  $\pm 45^{\circ}$  steering angle, but because of the a difference between the element pitch assumed during the design phase and that of the ATL probe used, the steering angle coverage is larger. However this is not necessarily a drawback, and it can be fixed by changing the clock frequency.

The ADC is currently not included on the ASIC due to time constraints. However, the beamformer topology have chosen is well suited to be combined with a charge-sharing SAR ADC.

The simulated power consumption is 0.09 mW for the pulser (one pulse every 200  $\mu$ s), 3.3 mW for the low-noise amplifier, 0.5 mW for the time-gain compensation amplifier, 4.7 mW for the beamformer.

# 6.2 Future work

When the PMUT is ready, the pulser and the LNA may need to be redesigned, since the parameters of the electrical model can be changed a lot.

The bandwidth of the TGC amplifiers needs to be limited, otherwise, the aliasing of the noise at higher frequency will located in signal band, hence increase the noise level.

A charge-sharing SAR ADC can be introduced to this ASIC, and it will inherently cooperate well with the beamformer.

The directivity plots looks strange when the delay is higher than 75 ns. This needs to be further investigated.