Digital Twin Technology for Microelectronics Reliability

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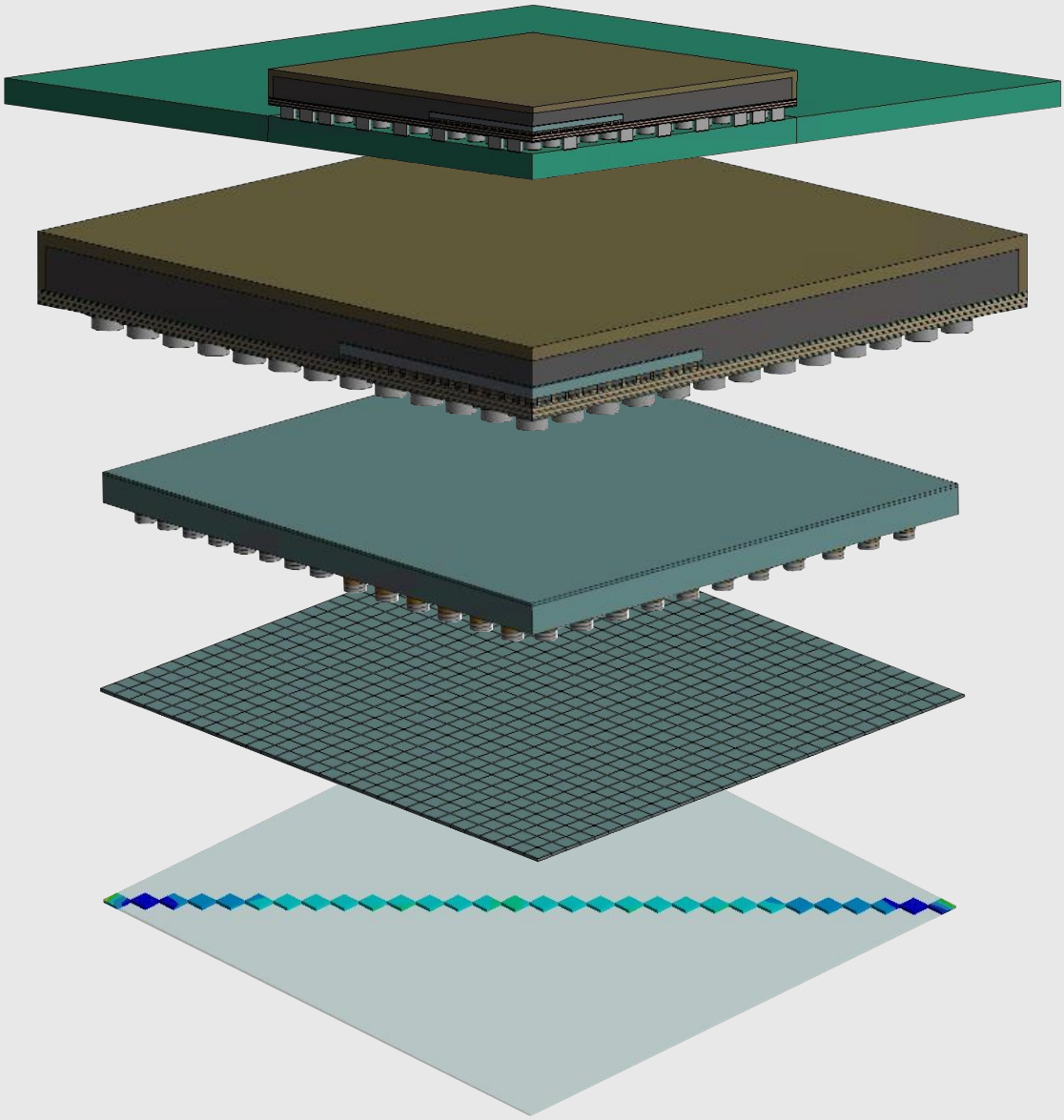
DIGITAL TWIN TECHNOLOGY

FOR MICROELECTRONICS RELIABILITY



ADWAIT INAMDAR

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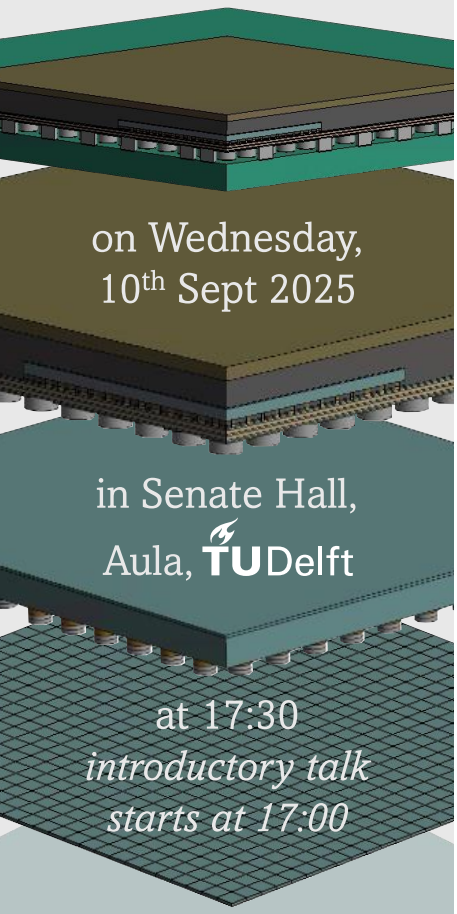
Digital Twin Technology for Microelectronics Reliability



on Wednesday,
10th Sept 2025

in Senate Hall,
Aula, TU Delft

at 17:30
introductory talk
starts at 17:00

by
Adwait Inamdar

Digital Twin Technology for Microelectronics Reliability

Digital Twin Technology for Microelectronics Reliability

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology,

by the authority of the Rector Magnificus
prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates,

to be defended publicly on
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Keywords: Digital Twin, Microelectronics Reliability, Physics of Degradation, Epoxy Moulding Compounds, Thermomechanical Ageing, Finite Element Analysis, In-situ Monitoring, Piezoresistive Sensor, Design of Experiments, Reduced-order Models, Multi-point Constraints.

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Dedicated to my parents,
teachers, friends & family

मला घडवणाऱ्या आणि सदैव पाठीशी असणाऱ्या
आई, बाबा, दादा, आणि संपूर्ण कुटुंबाला,
शिक्षक आणि मित्रपरिवाराला समर्पित!

Contents

List of Abbreviations

Summary

Electronic components are getting increasingly integrated into a diversity of applications, products, and industries and are becoming an essential part of them. In some cases, they are responsible for handling critical tasks (*e.g.*, the perception system in autonomous driving) and, in some, are exposed to harsh environmental conditions (*e.g.*, elevated temperatures). Thus, the reliable functioning of electronics has more significance than ever before. Traditional reliability qualification methods rely on the tests in specification manuals and handbooks. Although still commonly cited, they hold little significance in today's day and age.

New methods of reliability estimation have emerged and evolved quite a lot over the past six decades. Yet, they face the limitation of getting only a collective overview of failures from batch-based experimental tests. In reality, it is often the case that identical electronic components experience non-identical operating conditions and environmental loads and, thus, have a variation in their lifetimes. Thus, obtaining individual, component-specific insights is crucial when moving from a physics-of-failure to a physics-of-degradation approach for reliability. Implementing Prognostics and Health Management (PHM) for electronic components is a promising way to address this challenge. Demonstrating this approach using a Digital Twin-based framework is the primary goal of this dissertation.

First, a generalised framework for PHM is laid out (Chapter 1), and its building blocks are discussed. Then a systematic review of the term 'Digital Twin' and its state of the art is presented (Chapter 2). A new, more comprehensive, and yet generalised definition of a Digital Twin (DT) is prepared. Existing DT architectural models are analysed, and a novel two-branched model is introduced, which incorporates two key techniques, *viz.*, physics-based and data-driven modelling. In a complete DT implementation including both modelling approaches, both a cloud-based (external) computing and an edge-based (localised) computing infrastructure can be utilised to varying capacities. There are three phases of implementing Digital Twins within a product's lifecycle — Digital Twin Prototype (DTP), Digital Twin Instance (DTI), and Digital Twin Aggregate (DTA) — which gradually shift from a cloud-dominant to edge-dominant implementation.

Next, the groundwork for the physics-based branch is laid (Chapter 3) by delving into electronics packaging materials and associated ageing effects and degradation mechanisms due to the three dominant stress-factors — temperature, humidity, and mechanical vibration. Two commonly observed package-associated mechanical failure mechanisms, *viz.*, delamination and solder fatigue are identified. Furthermore, specialised hardware requirements for an edge-based, data-driven DT implementation (*i.e.* a DTA) are explored. Each chapter after this is dedicated to demonstrating one or more puzzle pieces of the two-branched DT framework for PHM.

Starting with the physics-of-degradation, the thermo-oxidative ageing of Epoxy Moulding Compounds (EMC) is modelled to study its effects on the thermomechanical behaviour of an electronic package (Chapter 4). A combination of experimental characterisation and analytical methods is utilised to record the changes in linear elastic temperature-dependent mechanical properties of the oxidised EMC at different stages of thermal ageing. A six-parameter material model (*viz.*, α_1^{ox}, α_2^{ox}, T_{g}^{ox}, T_{e}^{ox}, E_{g}^{ox}, E_{r}^{ox}) is constructed to reflect the changes in between the known ageing stages, and a continuously updated Digital Twin Instance (DTI) of a Flipchip BGA package is prepared. The prepared DTI is utilised to predict mechanical stresses along the top surface of the silicon die, which showed up to 40% increase in the maximum principal stress (σ_1) after 3000 h of ageing. The effect of thermomechanical degradation on the acceleration of EMC-die interface delamination is also discussed.

The in-situ monitoring aspect within the data-driven branch of the DT framework is demonstrated using a solder joint degradation monitoring setup (Chapter 5). A Wafer-Level Chip-Scale Package (WLCSP) housing a piezoresistive sensor with a high spatial resolution (70×30 cells of size 10 µm×10 µm each) is surface-mounted on a PCB. An efficient algorithm is developed to achieve a much faster full-readout under 5 min. A design of experiments involving static mechanical load with a four-point bending setup (maximum bending displacement of up to 1.1 mm) coupled with temperature variation (from −40 °C to 125 °C) is carried out to record piezoresistive data due to the deformation of the package-on-PCB assembly. The measured change in resistance is able to capture the concentrated stress patterns in the regions around the solder joints (*i.e.*, the potential location of failure). Moreover, the sensor is able to detect a crack (*i.e.*, the failure mode) resulting from the static mechanical load.

Another important aspect of the DT framework is hybrid modelling, which combines the physics-based and data-driven approaches. This is demonstrated by preparing thermomechanical Reduced-Order Models (ROM) using the physics-based Full-order Models (FOM) to be utilised in a data-driven approach (Chapter 6). A superelement (SE)-based ROM of a simpler test package (with 4 solder joints) is prepared and is used to study the effect of several combinations of the definitions and locations

of the ROM-FOM interface. A benchmarking against the Finite Element-based FOM shows more than one optimal combination for the accuracy and computational efforts, as well as the dependency on the thermomechanical properties of the materials involved in the ROM-FOM interface. The SE-based approach is then utilised on the thermomechanically aged (3000 h) Flipchip BGA package with a much more complex geometry and a larger 27×27 solder joint array, and its implications on the accuracy and efficiency of the ROM-integrated FOM are studied.

In the end, conclusions are drawn based on the obtained results from the aforementioned demonstrators (Chapter 7). An outlook of the feasibility and complexity of implementing a fully functional Digital Twin framework for PHM of microelectronic components and systems is also discussed. Finally, recommendations are provided for further work in the future.

Samenvatting

Elektronische componenten worden steeds meer geïntegreerd in een verscheidenheid aan toepassingen, producten en industrieën en worden er een essentieel onderdeel van. In sommige gevallen zijn ze verantwoordelijk voor het afhandelen van kritieke taken (*e.g.*, het perceptiesysteem bij autonoom rijden) en in sommige worden ze blootgesteld aan moeilijke omgevingen (*e.g.*, verhoogde temperaturen). Het betrouwbaar functioneren van elektronica is dus belangrijker dan ooit tevoren. Traditionele betrouwbaarheidskwalificatiemethoden zijn gebaseerd op de testen in specificatiehandleidingen en handboeken. Hoewel ze nog steeds vaak naar wordt verwezen, hebben ze weinig betekenis in deze tijd.

Nieuwe methoden voor betrouwbaarheidsschatting zijn ontstaan en zijn de afgelopen zes decennia behoorlijk geëvolueerd. Toch worden ze geconfronteerd met de beperking om alleen een collectief overzicht te krijgen van storingen van batchgebaseerde experimentele testen. In werkelijkheid is het vaak zo dat identieke elektronische componenten niet-identieke operatie-omstandigheden en omgevingsbelastingen ervaren en dus een variatie in hun levensduur hebben. Het verkrijgen van individuele, componentspecifieke inzichten is dus cruciaal bij de overgang van een fysica-van-falen (*physics-of-failure*) naar een fysica-van-degradatie (*physics-of-degradation*)-benadering voor betrouwbaarheid. Het implementeren van Prognostics and Health Management (PHM) voor elektronische componenten is een veelbelovende manier om deze uitdaging aan te gaan. Het aantonen van deze aanpak met behulp van een op Digital Twin gebaseerd werkwijze is het primaire doel van dit proefschrift.

Eerst wordt een algemeen kader voor PHM opgesteld (Chapter 1) en worden de bouwstenen daarvan besproken. Vervolgens wordt een systematisch overzicht gemaakt van de term 'Digital Twin' en de stand van de techniek ervan gepresenteerd (Chapter 2). Er wordt een nieuwe, uitgebreidere en toch algemenere definitie van een Digital Twin (DT) voorbereid. Bestaande DT-architectuurmodellen worden geanalyseerd en een nieuw model met twee takken wordt geïntroduceerd, dat twee belangrijke technieken bevat, *viz.*, op fysica gebaseerde en datagestuurde modellering. In een volledige DT-implementatie die beide modelleringsbenaderingen omvat, kunnen zowel een *cloud*-gebaseerde (externe) computer als een *edge*-gebaseerde

(gelokaliseerde) computerinfrastructuur met verschillende capaciteiten worden gebruikt. Er zijn drie fasen van het implementeren van Digital Twins binnen de levenscyclus van een product — Digital Twin Prototype (DTP), Digital Twin Instance (DTI) en Digital Twin Aggregate (DTA) — die geleidelijk verschuift van een *cloud*-dominante naar *edge*-dominante implementatie.

Vervolgens wordt de basis gelegd voor de op fysica gebaseerde tak (Chapter 3) door zich te verdiepen in verpakkingsmaterialen voor elektronica en bijbehorende verouderingseffecten en afbraakmechanismen als gevolg van de drie dominante stressfactoren — temperatuur, vochtigheid en mechanische trillingen. Twee veelgebruikte verpakkingsgeassocieerde mechanische faalmechanismen, *viz.*, delaminering en soldeervermoeidheid, worden geïdentificeerd. Verder worden gespecialiseerde hardwarevereisten voor een *edge*-gebaseerde, datagestuurde (*i.e.*, een DTA) DT-implementatie onderzocht. Elk hoofdstuk hierna is gewijd aan het demonstreren van een of meer puzzelstukjes van de twee vertakte DT-werkwijze voor PHM.

Beginnend met de *physics-of-degradation*, wordt de thermooxidatieve veroudering van Epoxy Moulding Compounds (EMC) gemodelleerd om de effecten ervan op het thermomechanische gedrag van een elektronisch pakket te bestuderen (Chapter 4). Een combinatie van experimentele karakterisering en analytische methoden wordt gebruikt om de veranderingen in lineaire elastische temperatuurafhankelijke mechanische eigenschappen van de geoxideerde EMC in verschillende stadia van thermische veroudering vast te leggen. Een materiaalmodel met zes parameters (*viz.*, α_1^{ox}, α_2^{ox}, $T_{\mathrm{g}}^{\mathrm{ox}}$, $T_{\mathrm{e}}^{\mathrm{ox}}$, $E_{\mathrm{g}}^{\mathrm{ox}}$, $E_{\mathrm{r}}^{\mathrm{ox}}$) is geconstrueerd om de veranderingen tussen de bekende verouderde stadia weer te geven, en een continu bijgewerkte Digital Twin Instance (DTI) van het Flipchip BGA-pakket wordt voorbereid. De voorbereide DTI wordt gebruikt om de mechanische spanningen langs het bovenoppervlak van de siliciumlaag (*silicon die*) te voorspellen, die tot 40% toename van σ_1 vertoonde na 3000 h veroudering. Het effect van thermomechanische afbraak op de versnelling van de EMC-die raakvlak-delaminering wordt ook besproken.

Het in-situ monitoren aspect binnen de datagestuurde tak van het DT-werkwijze wordt gedemonstreerd met behulp van een opstelling voor het monitoren van de degradatie van soldeerverbindingen (Chapter 5). Een Wafer-level Chip-scale Package (WLCSP) met een piëzoresistieve sensor met een hoge ruimtelijke resolutie (70×30 cellen van grootte 10 µm×10 µm elk) is gemonteerd op het oppervlak van een PCB. Een efficiënt algoritme is ontwikkeld om een veel snellere volledige uitlezing te bereiken binnen 5 min. Een ontwerp van experimenten met statische mechanische belasting met een vierpunts buigopstelling (maximale verplaatsing tot 1.1 mm) gekoppeld aan temperatuurvariatie (van −40 °C tot 125 °C) wordt uitgevoerd om piëzoresistieve gegevens op te nemen als gevolg van de vervorming van de

verpakking-op-PCB assemblage. De gemeten verandering in weerstand is in staat om de geconcentreerde spanningspatronen in het gebied rond de soldeerverbindingen (*i.e.*, de potentiële storingslocatie) vast te leggen. Bovendien kan de sensor een scheur (*i.e.*, de storingsmodus) detecteren als gevolg van de zuivere statische mechanische belasting.

Een ander belangrijk aspect van de DT-werkwijze is hybride modellering, die de op fysica gebaseerde en datagestuurde benaderingen combineert. Dit wordt aangetoond door het voorbereiden van thermomechanische Reduced-Order Models (ROM) met behulp van de op fysica gebaseerde Full-order Models (FOM) die worden gebruikt in een datagestuurde aanpak (Chapter 6). Een op superelement (SE) gebaseerde ROM van een eenvoudiger testpakket (met 4 soldeerverbindingen) wordt voorbereid en gebruikt om het effect van verschillende combinaties van de definities en locaties van de ROM-FOM-interface te bestuderen. Een vergelijking met de op Finite Element gebaseerde FOM toont meer dan één optimale combinatie voor de nauwkeurigheid en computationele inspanningen, evenals de afhankelijkheid van de thermomechanische eigenschappen van de materialen die betrokken zijn bij de ROM-FOM interface. De SE-gebaseerde aanpak wordt vervolgens gebruikt op het thermomechanisch verouderde (3000 h) Flipchip BGA-pakket met een veel complexere geometrie en een grotere 27×27 soldeerverbindingsreeks De implicaties van een complexere geometrie voor de nauwkeurigheid en efficiëntie van de ROM-geïntegreerde FOM worden ook bestudeerd.

Uiteindelijk worden conclusies getrokken op basis van de verkregen resultaten van de bovengenoemde demonstratoren (Chapter 7). Een vooruitblik op de haalbaarheid en complexiteit van het implementeren van een volledige functionele Digital Twin-werkwijze voor PHM van micro-elektronische componenten en systemen wordt ook besproken. Ten slotte worden aanbevelingen voor toekomstig werk verstrekt.

1

Introduction

Parts of this chapter have been published in *Frontiers in Electronics* (2025) [1], in *MDPI Electronics* (2024) [2], in the proceedings of *ESREL Conference* (2023) [3], and submitted to *IEEE Transactions on Intelligent Vehicles* [4].

1

1.1. ELECTRONIFICATION OF INDUSTRIES

Electronics play a vital role in most modern devices and systems. During the second decade of the 21st century, the number of electronic devices used in various applications has seen tremendous growth. Figure 1.1 shows the number of chips made just based on the *ARM* architecture, which is a widely-used Instruction Set Architecture (ISA) for consumer electronic products [5]. By the year 2021, about 200 billion *ARM*-based chips in total were shipped, from which the first 1 billion during 1991-2002, about 100 billion cumulative by 2017, and an additional 100 billion in just the following five years [6–8].

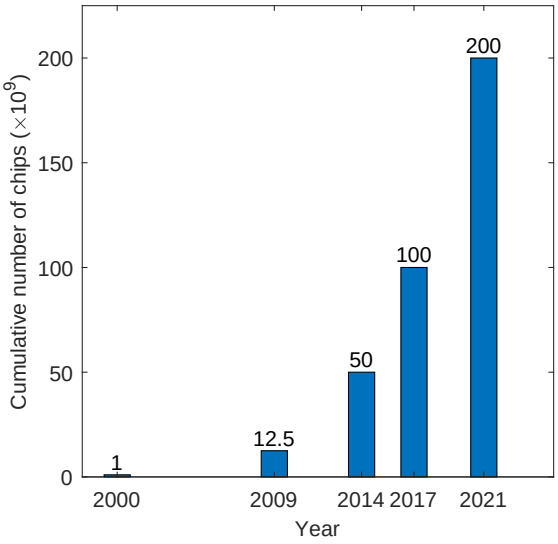


Figure 1.1: Number of semiconductor devices (cumulative) shipped over the last 20 years [6–8]. The chart only includes *ARM*-based chips, which are primarily used in low-power consumer electronic applications. The exponential growth in the last few years indicates the trend of rapid electronification.

At the core of this phenomenon is the 'digitalisation' or 'electronification' of industries over the last few decades. This has been accelerated by newly emerging Information Technology (IT), the incorporation of more and more electronics (*e.g.*, sensors) into conventional products/systems, and the integration of computer-aided, software-based technologies into traditional industries. Internet of Things (IoT)-enabled smart-home products such as Artificial Intelligence (AI)-powered smart speakers, thermostats and home appliances, *etc.*, are classic examples of the latter. Other well-known examples are the daily-use gadgets such as laptop/tablet computers, smartphones, and smartwatches, which consist mostly of electronic components. In addition to consumer electronics, such growth is also reflected in several other industries, such as manufacturing, automotive, and healthcare [9, 10].

USE CASE: AUTOMOTIVE ELECTRONICS

An automobile is no exception to the rapid adoption of electronics. According to a 2019 report by *Deloitte* [10], electronic systems in a modern car constitute about 35 % of its total cost, and it is expected to have close to 50 % share by the year 2030. Automotive electronics are responsible for primary functions such as engine control, transmission control, and suspension control, as well as advanced functions such as telematics (for location tracking and navigation) and cloud connectivity. Figure 1.2 gives an overview of the cost of automotive electronics and the technology deployment over time.

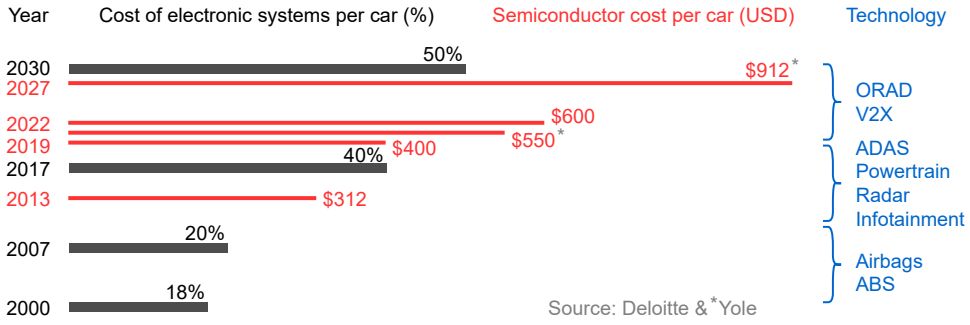


Figure 1.2: Overview of the cost of automotive electronics and the technology deployment over time. The grey bars represent the cost of electronic systems as a percentage (%) of total car cost. The red bars indicate the semiconductor cost per car in United States Dollars ($). Values beyond the year 2022 are predictions. The recorded data and estimated values are sourced from [10] and [11]. The blue text lists the technology deployed in the past and on the roadmap of Society of Automobile Engineers (SAE) [12]. The abbreviations stand for On-Road Automated Driving (ORAD); Vehicle to 'X' (V2X) connectivity including Vehicle to Vehicle (V2V); Advanced Driver Assistance Systems (ADAS); Anti-lock Braking System (ABS).

The automotive industry is progressing towards developing a framework for Electric Connected and Automated (ECA) vehicles, and the development of necessary automotive Electronic Components and Systems (ECS) is driven by three major trends – electrification, connectivity, and automation [13]. The SAE defines six levels of autonomous driving vehicles (*i.e.*, SAE L0–L5), starting with 'level 0' with no automation capabilities and going up to 'level 5' with full automation [14]. The development of a homologation framework for levels 3 to 5 (*i.e.*, SAE L3–L5) is in progress, with a forecast for the number of SAE L3 and L4 vehicles to grow from 0.2 million newly-registered units in the year 2020 to 24 million in the year 2030 [15].

Every step towards a higher level of automation requires additional electronics (*e.g.*, sensors and control units) and their integration into various functions of a car. From the year 2016–2022, a sizeable growth is observed in the revenue of 2 sub-categories of the automotive semiconductor revenue – Advanced Driver Assistance Systems (ADAS) and In-Vehicle Infotainment (IVI) system – aimed primarily at

providing safety and comforts. In terms of revenue, infotainment showed a jump from ~$6 billion to ~$9 billion, while ADAS from ~$3 billion to ~$12 billion [10]. According to *Yole Group* [11], the semiconductor cost per car is predicted to go from $550 today to about $912 by the year 2027. These trends are quite significant in terms of user safety, technological development, and economics.

Thus, automotive electronic systems are, and will remain, a crucial component of an automobile concerning its functionality, cost, and overall safety. To address this, many projects are created under multinational joint undertakings such as European Union (EU)-level funding programs for research and development. The project 'ArchitectECA2030' envisions providing "a harmonized pan European validation framework enabling mission oriented validation of ECS for ECA vehicles from SAE L3 to L5 to improve reliability, robustness, safety and traceability" [16].

Overall, the adoption of electronics is growing at a fast pace across industries. Application fields like autonomous driving, intelligent manufacturing, smart city, and smart services are built around sensing, connectivity, and AI-like software solutions, which require Mission Critical Electronics (MCE) on a large scale. Therefore, the reliable functioning of electronic products and subsystems becomes crucial. Multiple factors can affect the reliability of electronics, such as the choice of materials, sub-optimal design, insufficient quality control, and manufacturing defects, most of which are associated with the beginning phase of a product's life cycle. Another key factor that influences reliability and performance over time is the degradation of materials used in electronic components.

1.2. Degradation of Electronic Components

Electronic components are complex systems made up of a combination of several different materials. Under the influence of environmental and operating conditions (loads), these materials undergo degenerative changes over time following the second law of thermodynamics [17, ch.3]. It causes loss of their quality or functionality, reflected in the degradation of electronic components, which can lead to failure during their operational lifetime. Thus, the reliability of an electronic component is closely linked with the ageing of its constituent materials.

There are several microelectronics-based technologies where material degradation and reliability are actively associated with each other to different extents. Some examples are electrical power systems, ferroelectric (a subset of piezoelectric) technologies, polymer electronics, bioelectronics, Micro-Electro-Mechanical Systems (MEMS), wearable electronics, and electromechanical machines [17, ch.1]. Electronics in some applications (*e.g.*, automotive electronics) need to withstand

harsher environments than others (*e.g.*, consumer electronics). Degradation of materials within electronic components can lead to many failure modes. This demands deep knowledge of failure mechanisms (*i.e.*, *physics-of-failure*), understanding their connection with the ageing process, and their link to the operating conditions and changes in material properties.

Different material degradation mechanisms can be categorised by the domains they belong to. Figure 1.3 indicates the five domains, *viz.*, mechanical, thermal, chemical, electrical, and biological degradation. It also includes annotations of some select degradation and failure mechanisms (relevant to this thesis) associated with one or more of the aforementioned domains. The study of the ageing phenomenon occurring because of a combination of natural processes in single or multiple degradation domains is collectively referred to as *physics-of-degradation*.

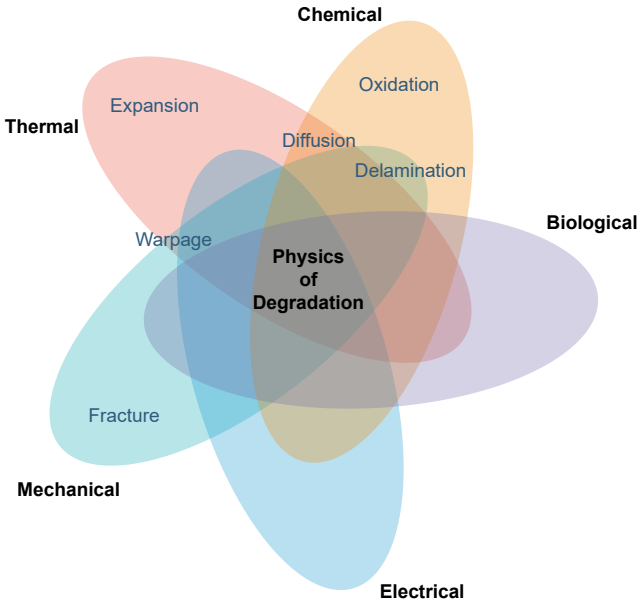


Figure 1.3: Five domains of physics-of-degradation and a few examples of degradation mechanisms associated with one or more of these domains. For example, 'warpage' is the out-of-plane deformation under thermal load (*i.e.*, a thermo-mechanical effect) caused by the mismatch of thermal expansion of different layers in an electronic package and, thus, falls under both mechanical and thermal domains.

The industries are expected to move from an 'application-based' to a 'degradation-based' wave in reliability in the near future [18], which means the focus would transition from a *physics-of-failure* to a *physics-of-degradation* approach to estimate a product's service lifetime, also referred to as the Remaining Useful Life (RUL). Thus, the study of relevant degradation mechanisms is critically important for reliability estimation of microelectronic components.

1

1.3. MICROELECTRONICS RELIABILITY

The term 'microelectronics' broadly encompasses electronic devices and components having a micrometre-scale (0.1–100 µm) or smaller feature size. The technical definition of 'reliability' is the probability that a given item will perform its intended function within specified performance limits, without failures, for a given period of time under a given set of conditions [19, 20]. Bringing both together, microelectronics reliability, thus, refers to the aforementioned definition adapted for electronic components and systems.

RELIABILITY CALCULATIONS

Product reliability refers to its future performance or behaviour, which inherently has the uncertainty and randomness involved [21]. Thus, the mathematical formulation of reliability is grounded in statistics and probability theory. Reliability R is a function of the random variable (*i.e.*, variate) t, which can be a suitable time-related parameter indicating product age. The random variable chosen for reliability estimation is Time to Failure (TTF) T, which has the Probability Density Function (PDF) $f(t)$ under the assumption of t being continuous (practically achievable by choosing a 'large' sample size). In this way, $R(t)$ depends on the PDF $f(t)$ as indicated in Equation (1.1).

$$R(t) = \int_{t}^{\infty} f(\tau)\ \mathrm{d}\tau \tag{1.1}$$

The 'bathtub curves' are also famously used to indicate the trend of failures as a function of component age. It is essentially a(n idealised) plot of (component) hazard rate $h(t)$, which depends on reliability as indicated in Equation (1.2). For systems with individually replaceable components, Rate of Occurrence of Failure (ROCOF) λ is plotted against the system age to obtain the (system) bathtub curve [21, 22]. Hazard rate curves are modelled using a wide range of PDFs to fit the data collected in qualification tests. A PDF can be a discrete function (*e.g.*, binomial and Poisson distribution) or a continuous function (*e.g.*, exponential, normal, log-normal, gamma, and Weibull distribution). Weibull distribution is widely used in the industry because of its versatility in modelling a variety of hazard rate curves. Lastly, reliability calculations can also provide an estimate of the expected life of a component. It is referred to as Mean Time to Failure (MTTF), also as Mean Time Between Failures (MTBF) when the hazard rate $h(t)$ is constant and is evaluated using Equation (1.3).

$$h(t) = \frac{f(t)}{R(t)} = \frac{-1}{R(t)} \frac{\mathrm{d}R(t)}{\mathrm{d}t} \tag{1.2}$$

$$\mathrm{MTTF} = \int_0^\infty t\, f(t)\, \mathrm{d}t = \int_0^\infty R(t)\, \mathrm{d}t \tag{1.3}$$

Note that the described calculations represent the traditional ways (from the 1960s) of calculating the reliability of components. Methods of reliability estimation have evolved quite a lot from the birth of fault-tree analysis in the 1970s, the use of accelerated testing in the 1980s, the adoption of the physics-of-failure approach in the 1990s, to the hybrid approach using physics and statistics together [23, 24]. Thus, the above equations, although they define the technical terms correctly, hold little significance in the current era of reliability engineering.

Reliability Engineering

Reliability engineering is a discipline of its own, established through dedicated efforts from 1952–1957 [25, 26]. It includes applying mathematical and scientific techniques in conjunction with organisational strategies and efforts, where the former is related to the calculation aspect and the latter is related to the management aspect of this interdisciplinary field. Considerable resources are invested by Original Equipment Manufacturers (OEMs) in reliability engineering, as the (electronic) product reliability is crucial and closely tied to their economic aspects (such as production and maintenance costs) and reputation. This can directly influence an OEM's competitive position and market share. Due to the high stakes involved, accurate estimation of a product's reliability becomes of utmost importance.

The reliability assessment procedure is utilised in an iterative way to improve a product/process. Current ways of reliability estimation are based on standard tests documented in specification manuals, such as *Reliability Handbooks* [1] and *International Standards* [2]. The tests are primarily done in a batch during the product qualification phase. This approach provides only a collective overview and broader insights into an entire batch using a statistical approach, which also implies that it lacks the details of sample-specific insights.

Alternatively, an approach of reliability estimation by monitoring a select number of product samples during their real-world usage is utilised. This can help to get sample-specific insights, but it is also restricted to a small number of in-use products

[1] Examples of *Reliability Handbooks* – generic/purely mathematical [27, 28], topic-specific [29, 30]
[2] Examples of *International Standards* – electronics-related [31, 32] and application-specific [12, 33]

from a much bigger batch. Thus, both of these traditional approaches are limiting in terms of either the scale or the details of sample-specific insights.

Moreover, traditional reliability handbooks have also been heavily criticised in the past for being inaccurate and invalid because of being based on insufficient knowledge of component failures [34]. It has also been highly recommended to replace them with newer approaches, *e.g.*, Physics of Failure (PoF). Reliability estimation methodology needs to go to the next generation to match the needs created by the rapid electronification of industries and involvement of MCE. It should provide per-product (sample-specific) health monitoring but at a much larger scale, possibly for *all* the products (not just a smaller sample set) while they are in use. In order to facilitate individual health monitoring on this scale, it is crucial to develop and implement new ways of per-product health monitoring.

1.4. Prognostics and Health Management

Prognostics and Health Management (PHM) is a relatively advanced methodology that allows reliability assessment of a system/component based on its *individual* working conditions. It leverages condition monitoring, which allows for evaluating a system's current state of health based on its load history and keeping track of all its historical health statuses [35, 36]. Prognostics refers to the prediction of the future state, performance, and RUL of a system based on its current state of degradation. Health management is the process of making decisions and planning actions on the basis of the evaluated state of component health. The prognosis can be of a particular failure mode in a critical component, estimating the progression of a fault, or even evaluating the RUL of the whole system, whereas the actions could be issuing a warning, stopping a system function, or even scheduling maintenance (*i.e.*, predictive maintenance) or a component replacement [37].

The current state of degradation depends on the deviation from the nominal operating conditions. Two identical components subjected to different sets of working and environmental conditions after a certain period of time will have different states of health. PHM facilitates capturing that deviation individually for each system. Therefore, this technique gives a major advantage over traditional reliability qualification tests [38]. PHM can be implemented based on a model-based, data-driven, or even a hybrid (fusion) approach [39]. Various publications focused on reviewing and summarising the PHM concept and its implementations present different flowcharts [40–45], which are usually complex and/or application-specific.

Figure 1.4 indicates a rather simplified and generalised framework for the PHM workflow. The workflow of PHM begins with condition monitoring, which requires

the collection of relevant data using appropriate sensors for capturing environmental loads, operating conditions, and additional measurements (*e.g.*, current or voltage). Thus, the first set of steps in the PHM workflow are data sensing, acquisition, and preprocessing. The second phase of the PHM framework is diagnostics. The collected data is processed to provide a preliminary assessment of the component's condition, such as the detection of an anomaly. The state of component health is then evaluated, which requires physics-based validated models for quantifying degradation and fault progression. In the last phase, prognostics and decision-making come into the picture. A prognosis of the component's performance and an estimation of its RUL is made. Based on the prediction, decisive action is chosen, such as scheduling maintenance for repair or replacement.

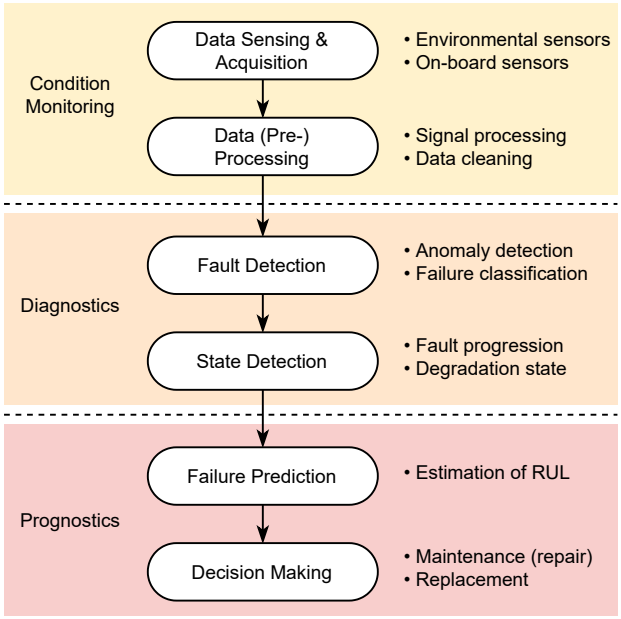


Figure 1.4: Framework of the PHM workflow and its three main phases – condition monitoring, diagnostics, and prognostics. Actions involved in each phase are indicated in the flowchart, and their respective functional descriptions are listed on the right side. This figure has been prepared by combining different elements from several PHM flowcharts in [40–45] to present a more simplified and generalised workflow.

Building Blocks of (Hybrid) PHM

The physics-based models play a key role in the PHM workflow, as the later steps in its framework depend on the health-state evaluation. PoF is a preferred, but not the only, choice for physics-based models. It can be further enhanced when used in conjunction with the Physics of Degradation (PoD)-based models. Some notable examples of PoD-based models due to thermal ageing of different materials and sub-

components of an electronic system are: solder joints [46], moulding compounds [47], and Printed Circuit Boards (PCBs) [48]. A strong foundation of such validated models is a necessity for component-level health monitoring of electronics.

The input to the degradation models is the operating conditions experienced by the electronic system. Ambient conditions such as temperature, moisture, vibrations, shock, pressure, and acoustic levels can affect the component's lifetime. Thus, relevant environmental parameters should be continuously measured. In addition, some additional embedded sensing devices or external measurements, such as electric current, changes in electrical resistance, displacement, and strain, can give even more information about the state of component degradation. Thus, the data-sensing needs should be considered in the hardware design of the component; for example, specialised integrated sensors such as a piezoresistive sensor [49–51] or measurement techniques such as the Direct Current (DC) resistance measurement, Radio Frequency (RF) impedance measurement, Multivariate State Estimation Technique (MSET), and Sequential Probability Ratio Test (SPRT) [52–54].

A robust data processing pipeline needs to be in place to utilise the collected data into data-driven approaches, *e.g.*, lifetime prediction, failure classification, and anomaly detection. The PoF models should identify relevant failure modes associated with the electronic system of interest. The PoD models should be able to translate the loading conditions into an effective aged health state of the component, including the changes in the behaviour of its constituent materials. In addition, PoD should also reflect the effects of all manufacturing steps (semiconductor processing, die-bonding, electronic packaging, moulding, solder reflow, component assembly, *etc.*) until the electronic system is ready to be used in the field. Lastly, the decision-making logic should consider the criticality of an electronic component's function in the entire system, such as an autonomous vehicle or a manufacturing line.

1.5. MONITORING DEVICE

The rapid adoption of electronics across industries has led to a high demand for MCE. More electronics per product put forth the need for a fast ramp-up of new electronic components, resulting in high-volume production in shorter periods of time. Consequently, any issues that emerge from non-reliable electronics affect the functionality of the product and can create serious business problems for the OEMs in different domains. Thus, PHM must be an integral part of the lifecycle management of electronic products.

The increasing importance of electronics and the disadvantage of traditional reliability testing can be overcome by implementing PHM for product-specific monitoring.

It can serve as a product-level Monitoring Device (MonDev), which presents itself as a key enabler for providing performance- and lifetime-on-demand. New IoT options, combined with edge and/or cloud computing possibilities, can run real-time analysis when reliability-specific parameters are measured and recorded at the system level. Such system-level prognostics help avoid failures by detecting them beforehand, thus reducing the residual risk [55].

It is important to note that the MonDev is not necessarily only a physical device but is more of a conceptual term. It includes both physical (dedicated hardware and sensors) and digital (data and software) components. It can take any form of shape depending upon the application (*e.g.*, automotive industry) and the subdomain (*e.g.*, perception, propulsion, connectivity). The project *ArchitectECA2030* [16] explains the implementation of an in-vehicle MonDev for an ECA vehicle [56, 57], which is able to indicate and measure the health status and possible degradation of the functional electronics and electronic systems, enabling predictive diagnosis, maintenance, and re-configuration of embedded software. The framework for risk assessment and safety-level determination is discussed further in [4].

Digital Twin (DT) is one of the implementations of a MonDev. A component-level MonDev can be achieved by integrating the described PHM framework into the Digital Twin architecture. Thus, the work in this thesis aims to develop methods necessary for Digital Twin-based health monitoring for microelectronic components. It addresses the hardware design, sensor selection, step-by-step preparation of PoD models, package-associated failure modes, in-situ monitoring, failure prediction, and reduced-order models, which collectively form various aspects of the MonDev.

1.6. RESEARCH OBJECTIVES

This thesis aims to explore the Digital Twin-based approach for PHM of electronic components. The emphasis is also on developing experimentally validated PoD-based models that reflect a range of states of component degradation. A second goal is to demonstrate in-situ monitoring for the data-driven approach for failure prognosis and design for reliability. The third goal is to explore the effectiveness and practicality of compact models in the Digital Twin workflow.

The following research objectives are defined:

1. To review the concept of a Digital Twin thoroughly by analysing its existing descriptions, including the definitions and architectural models;

2. To formulate a Digital Twin-based framework for condition monitoring, failure prognosis, and health management of microelectronic components;

3. To demonstrate the physics-based aspect of the framework by studying degradation mechanisms responsible for package-associated mechanical failures and preparing an experimentally validated DT to analyse the effects of ageing;
4. To facilitate the data-driven aspect of the framework by developing in-situ sensor-based monitoring techniques for a critical layer of an electronic component and applying it to experimentally detect mechanical failures;
5. To develop and test physics-based reduced-order models aimed at IP protection and interoperability, and analyse their accuracy and efficiency;
6. To draw conclusions on the feasibility of implementing a Digital Twin-based framework for health monitoring of microelectronics in different applications.

1.7. Outline of this Thesis

The key topics of the research were formulated based on the defined research objectives, and the work was disseminated as journal and conference papers. This thesis has been prepared as a combination of multiple publications. This may have resulted in minor overlap of the chapters and repetition of some text. This has been minimised as much as possible, without the individual chapters losing their independence from each other. The chapter-wise outline of this thesis is as follows:

Chapter 2 presents a thorough literature review of the concept of a Digital Twin. It includes the analysis of its various descriptions, including the definitions and architectural models, from the literature. A new decontextualised and yet comprehensive definition and a novel two-branched architectural model are proposed. The extension of the latter for a hybrid PHM approach for electronic components and systems is also discussed.

Chapter 3 delves into the evolution of electronics packaging and the physics-of-degradation of plastic encapsulating materials. The dominating degradation-causing stress-factors are reviewed, and the two most common package-associated failure modes are identified. The hardware requirements, including specialised sensors and measurement techniques, to capture the effects of material degradation are also explored.

Chapter 4 showcases a study of thermo-oxidative degradation of epoxy moulding compounds. A systematic procedure is developed to model the changes in the thermomechanical properties of the encapsulation material due to thermal ageing at 150 °C and reflect it in a continuously updated Finite Element model of a flip-chip ball grid array package to represent any intermediate oxidation stages. The effects of ageing on the package-warpage and die-level stresses are also studied.

Chapter 5 focuses on monitoring the mechanical degradation of package-to-PCB solder interconnects of a wafer-level chip-scale package using a high-resolution piezoresistive sensor. A design of experiments is devised to study the effects of several combinations of mechanical and thermal load using test specimens with embedded piezoresistive sensors in a four-point bending setup. A correlation between the recorded stress pattern and the development of a crack under a purely mechanical load was established.

Chapter 6 explores the role of reduced-order modelling in the Digital Twin framework. A superelement-based Finite Element modelling technique is demonstrated with a virtual (simulation-based) design of experiments. The effect on the accuracy and computational resources is studied for several definitions of the connection between the reduced model and the remaining Finite Element model, and material properties-based dependencies are established. The developed workflow is then utilised on a more complex assembly to achieve optimal accuracy and efficiency.

Chapter 7 concludes this thesis and provides recommendations for further research.

References

[1] A. Inamdar, W. D. Van Driel, and G. Zhang, *Electronics packaging materials and component-level degradation monitoring*, *Frontiers in Electronics*, vol. 6, p. 1 506 112, Jan. 2025, ISSN: 2673-5857 (Cited on p. 1).

[2] A. Inamdar, W. D. van Driel, and G. Zhang, *Digital Twin Technology - A Review and Its Application Model for Prognostics and Health Management of Microelectronics*, *Electronics*, vol. 13, no. 16, p. 3255, Aug. 2024, ISSN: 2079-9292 (Cited on p. 1).

[3] A. Inamdar, W. D. van Driel, and G. Q. Zhang, *Digital Twin-Based Hybrid PHM Framework for Monitoring Package-Level Degradation*, in *European Safety and Reliability Conference (ESREL) 2023*, Southampton, UK, 2023 (Cited on p. 1).

[4] M. van Soestbergen, A. Inamdar, O. Vermesan, J. Niehaus, F. Wotawa, and G. Stettinger, *Driving the Future: A Perspective on Electronic Safety in Autonomous Vehicles, IEEE Transactions on Intelligent Vehicles (submitted)*, 2025 (Cited on pp. 1, 11).

[5] Statista, *Processors (Digital and Trends)*, Tech. Rep., 2024 (Cited on p. 2).

[6] A. L. Shimpi, *ARM Partners Ship 50 Billion Chips Since 1991 - Where Did They Go*, Mar. 2014 (Cited on p. 2).

[7] Edge Impulse, *Jan Jongboom at NVIDIA's GTC21: Arm Your Jetson Nano with Tony Stark Superpowers*, Apr. 2021 (Cited on p. 2).

[8] S. Segars, *Arm Partners Have Shipped 200 Billion Chips*, Oct. 2021 (Cited on p. 2).

[9] Precedence Research, *Medical Electronics Market Size to Hit USD 248.43 Billion*, Dec. 2021 (Cited on p. 2).

[10] W. Chou, J. Shao, R. Chung, L. Chen, A. Chen, and L. Zhou, *Semiconductors - the Next Wave*, Deloitte, Tech. Rep., Apr. 2019 (Cited on pp. 2–4).

[11] Yole Intelligence, *Semiconductor Trends in Automotive 2022*, Oct. 2022 (Cited on pp. 3, 4).

[12] Society of Automotive Engineers, *Automotive Electronic Systems Reliability Standards* (Cited on pp. 3, 7).

[13] P. Gromala, F. Dietz, S. Rzepka, and B. Han, *Concept of the 3rd generation of reliability for electronic smart systems*, *InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM*, vol. 2019-May, pp. 917–922, May 2019 (Cited on p. 3).

[14] P. Warrendale, *SAE International Releases Updated Visual Chart for Its "Levels of Driving Automation" Standard for Self-Driving Vehicles*, Dec. 2018 (Cited on p. 3).

[15] Berg Insight, *The Future of Autonomous Cars*, Feb. 2021 (Cited on p. 3).

[16] ArchitectECA2030, *ArchitectECA2030 - Project Poster*, Nov. 2022 (Cited on pp. 4, 11).

[17] J. Swingler and A. Feinberg, Eds., *The Physics of Degradation in Engineered Materials and Devices: Fundamentals and Principles*. Momentum Press, Dec. 2014, ISBN: 9781606504673 (Cited on p. 4).

[18] W. D. van Driel, M. Y. Mehr, X. J. Fan, and G. Q. Zhang, *Outlook - From Physics of Failure to Physics of Degradation*, in *Reliability of Organic Compounds in Microelectronics and Optoelectronics*, W. D. Van Driel and M. Y. Mehr, Eds., Cham: Springer International Publishing, Jan. 2022, pp. 535–538 (Cited on p. 5).

[19] National Aeronautics and Space Administration (NASA), *Reliability: Definition and Quantitative Illustration* (Cited on p. 6).

[20] American Society for Quality (ASQ), *What is Reliability?* (Cited on p. 6).

[21] K. C. Kapur and M. Pecht, *Reliability Engineering*, 1st ed., A. P. Sage, Ed. Wiley, Apr. 2014, ISBN: 978-1-118-14067-3 (Cited on p. 6).

[22] D. J. Sherwin and A. Bossche, *The Reliability, Availability and Productiveness of Systems*, 1st ed. Springer Netherlands, Oct. 1993 (Cited on p. 6).

[23] M. Azarkhail and M. Modarres, *The Evolution and History of Reliability Engineering: Rise of Mechanistic Reliability Modeling*, *International Journal of Performability Engineering*, vol. 8, no. 1, p. 35, Jan. 2012, ISSN: 0973-1318 (Cited on p. 7).

[24] H. Wang and F. Blaabjerg, *Power Electronics Reliability: State of the Art and Outlook*, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6476–6493, Dec. 2021, ISSN: 2168-6777 (Cited on p. 7).

[25] A. Coppola, *Reliability Engineering of Electronic Equipment - A Historical Perspective*, *IEEE Transactions on Reliability*, vol. R-33, no. 1, pp. 29–35, 1984, ISSN: 00189529 (Cited on p. 7).

[26] Y. Oostendorp, S. Lemkowitz, W. Zwaard, C. van Gulijk, and P. Swuste, *Introduction of the concept of risk within safety science in The Netherlands focussing on the years 1970–1990*, *Safety Science*, vol. 85, pp. 205–219, Jun. 2016, ISSN: 0925-7535 (Cited on p. 7).

[27] H. Pham, Ed., *Handbook of Reliability Engineering*, 1st ed. Springer London, Apr. 2003 (Cited on p. 7).

[28] R. F. Stapelberg, *Handbook of Reliability, Availability, Maintainability and Safety in Engineering Design*, 1st ed. Springer London, Mar. 2009 (Cited on p. 7).

[29] Department of Defense (USA), *Military Handbook - Electronic Reliability Design Handbook*. Oct. 1998 (Cited on p. 7).

[30] Renesas Electronics, *Semiconductor Reliability Handbook*. Jan. 2017 (Cited on p. 7).

[31] Joint Electron Device Engineering Council, *JEDEC Standards* (Cited on p. 7).

[32] Institute for Printed Circuits, *IPC Standards* (Cited on p. 7).

[33] Automotive Electronics Council, *AEC Standards* (Cited on p. 7).

[34] M. G. Pecht and M. Kang, Eds., *Prognostics and Health Management of Electronics: Fundamentals, Machine Learning, and the Internet of Things*. Wiley, Aug. 2018, ISBN: 9781119515326 (Cited on p. 8).

[35] Y. Hu, X. Miao, Y. Si, E. Pan, and E. Zio, *Prognostics and health management: A review from the perspectives of design, development and decision*, *Reliability Engineering & System Safety*, vol. 217, p. 108 063, Jan. 2022, ISSN: 0951-8320 (Cited on p. 8).

[36] L. Biggio and I. Kastanis, *Prognostics and Health Management of Industrial Assets: Current Progress and Road Ahead*, *Frontiers in Artificial Intelligence*, vol. 3, p. 578 613, Nov. 2020, ISSN: 26248212 (Cited on p. 8).

[37] E. Zio, *Prognostics and Health Management (PHM): Where are we and where do we (need to) go in theory and practice*, *Reliability Engineering & System Safety*, vol. 218, p. 108 119, Feb. 2022, ISSN: 0951-8320 (Cited on p. 8).

[38] E. Zio, *Some challenges and opportunities in reliability engineering*, *IEEE Transactions on Reliability*, vol. 65, no. 4, pp. 1769–1782, Dec. 2016, ISSN: 00189529 (Cited on p. 8).

[39] M. Compare, P. Baraldi, and E. Zio, *Challenges to IoT-Enabled Predictive Maintenance for Industry 4.0*, *IEEE Internet of Things Journal*, vol. 7, no. 5, pp. 4585–4597, May 2020, ISSN: 23274662 (Cited on p. 8).

[40] A. Prisacaru, P. J. Gromala, M. B. Jeronimo, B. Han, and G. Qi Zhang, *Prognostics and health monitoring of electronic system: A review*, in *2017 18th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2017*, Institute of Electrical and Electronics Engineers Inc., May 2017, ISBN: 9781509043446 (Cited on pp. 8, 9).

[41] M. Ahsan, S. Stoyanov, and C. Bailey, *Prognostics of automotive electronics with data driven approach: A review*, in *Proceedings of the International Spring Seminar on Electronics Technology*, vol. 2016-September, IEEE Computer Society, Sep. 2016, pp. 279–284, ISBN: 9781509013890 (Cited on pp. 8, 9).

[42] S. Khan and T. Yairi, *A review on the application of deep learning in system health management*, *Mechanical Systems and Signal Processing*, vol. 107, pp. 241–265, Jul. 2018, ISSN: 0888-3270 (Cited on pp. 8, 9).

[43] N. Vichare, B. Tuchband, and M. Pecht, *Prognostics and Health Monitoring of Electronics*, in *Handbook of Performability Engineering*, K. B. Misra, Ed., 1st ed., Springer, London, Aug. 2008, ch. 67, pp. 1107–1122 (Cited on pp. 8, 9).

[44] L. Xu and M. Xu, *PHM-Based Fault Identification for Electronics-Rich Systems Under Uncertainty*, in *Lecture Notes in Electrical Engineering*, J. Xu, M. Yasinzai, and B. Lev, Eds., vol. 185, Springer, London, 2013, ch. 17, pp. 209–218, ISBN: 9781447145998 (Cited on pp. 8, 9).

[45] M. Pecht and R. Jaai, *A prognostics and health management roadmap for information and electronics-rich systems*, *Microelectronics Reliability*, vol. 50, no. 3, pp. 317–323, Mar. 2010, ISSN: 0026-2714 (Cited on pp. 8, 9).

[46] H. Ma, J. C. Suhling, Y. Zhang, P. Lall, and M. J. Bozack, *The influence of elevated temperature aging on reliability of lead free solder joints*, in *Proceedings - Electronic Components and Technology Conference*, 2007, pp. 653–663, ISBN: 1424409853 (Cited on p. 10).

[47] A. Inamdar, Y.-H. Yang, A. Prisacaru, P. Gromala, and B. Han, *High temperature aging of epoxy-based molding compound and its effect on mechanical behavior of molded electronic package*, *Polymer Degradation and Stability*, vol. 188, 2021, ISSN: 01413910 (Cited on p. 10).

[48] M. van Dijk, O. Wittler, S. Wagner, and M. Schneider-Ramelow, *Numerical simulation approach for consideration of ageing effects in PCB substrates by modifying viscoelastic materials properties*, *Microelectronics Reliability*, vol. 157, p. 115 403, Jun. 2024, ISSN: 0026-2714 (Cited on p. 10).

[49] A. Inamdar *et al.*, *Characterization of a Piezoresistive Sensor for In-Situ Health Monitoring of Solder Bumps*, in *IEEE 74th Electronic Components and Technology Conference (ECTC) 2024*, 2024 (Cited on p. 10).

[50] A. Prisacaru, A. Palczynska, A. Theissler, P. Gromala, B. Han, and G. Q. Zhang, *In Situ Failure Detection of Electronic Control Units Using Piezoresistive Stress Sensor*, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 5, pp. 750–763, May 2018, ISSN: 21563950 (Cited on p. 10).

[51] A. Palczynska, A. Prisacaru, P. J. Gromala, B. Han, D. Mayer, and T. Melz, *Towards prognostics and health monitoring: The potential of fault detection by piezoresistive silicon stress sensor*, *Microelectronics Reliability*, vol. 74, pp. 165–172, Jul. 2017, ISSN: 0026-2714 (Cited on p. 10).

[52] R. Jaai, M. Pecht, and J. Cook, *Detecting failure precursors in BGA solder joints*, in *Proceedings of 2009 Annual Reliability and Maintainability Symposium*, 2009, pp. 100–105, ISBN: 9781424425099 (Cited on p. 10).

[53] B. Yao, Y. Lu, and M. Wan, *A study of solder joint degradation and detection using RF impedance analysis*, in *Proceedings of International Symposium on Advanced Packaging Materials*, 2011, pp. 117–121, ISBN: 9781467301473 (Cited on p. 10).

[54] Y. D. Lu, M. Wan, and B. Yao, *Degradation detecting of solder joints by time domain reflectometry technology*, in *Proceedings of 13th International Conference on Electronic Packaging Technology and High Density Packaging ICEPT-HDP 2012*, 2012, pp. 1344–1347, ISBN: 9781467316804 (Cited on p. 10).

[55] S. Solmaz, G. Stettinger, and F. Wotawa, *Residual Risk Management Strategies at System Level presented for ACC/LKA Behavioural Competencies*, in *IEEE International Automated Vehicle Validation Conference, IAVVC 2023*, Institute of Electrical and Electronics Engineers Inc., 2023, ISBN: 9798350322538 (Cited on p. 11).

[56] F. Wotawa and H. Lewitschnig, *Monitoring Hierarchical Systems for Safety Assurance*, in *International Symposium on Intelligent and Distributed Computing, in the book Studies in Computational Intelligence*, vol. 1026, Springer, Cham, May 2022, pp. 331–340, ISBN: 978-3-030-96627-0 (Cited on p. 11).

[57] G. Stettinger and F. Wotawa, *Smart Monitoring for Safety-Assurance in Autonomous Driving*, in *International Conference on Software Engineering and Knowledge Engineering, SEKE 2023*, vol. 2023-July, Knowledge Systems Institute Graduate School, Jul. 2023, pp. 542–547 (Cited on p. 11).

2

Digital Twins for Health Monitoring of Electronics

Digital Twins (DT) play a key role in Industry 4.0 applications, and the technology is in the process of becoming mature. Since its conceptualisation, it has been embraced by several industries, including manufacturing, automotive, and electronics. It has been heavily contextualised and often misinterpreted as being merely a virtual model. There are several contextualised definitions and application-specific interpretations of DT that don't necessarily clarify the reach of the concept. Thus, it is crucial to define it clearly and have a deeper understanding of its architecture, workflow, and implementation scales. This chapter reviews the notion of a Digital Twin represented in the literature, analyses different kinds of descriptions, and proposes a new generalised definition. In addition, the existing models of DT architecture are analysed, and a new simplified two-branched model of DT is introduced. It is then extended for condition monitoring of electronic components and systems, and a new approach to hybrid Prognostics and Health Management (PHM) is further elaborated on. The proposed framework, enabled by the two-branched Digital Twin model, combines the physics-of-degradation and data-driven approaches and empowers the next generation of reliability assessment methods. Finally, the advantages, associated challenges, and future scope of the proposed approach are also discussed.

Parts of this chapter have been published in *MDPI Electronics* (2024) [1], in *Future Generation Computer Systems* (2024) [2], in a book chapter in *Recent Advances in Microelectronics Reliability*, Springer (2024) [3], in IEEE EPS Newsletters (Jul-2022 and Nov-2023) [4, 5], and in the proceedings of *ESREL Conference* (2023) [6] and of *IEEE SWC Conference* (2024) [7].

2.1. Introduction

Digital Twinning is one of the key technologies in Industry 4.0, *i.e.*, the fourth industrial revolution. It plays a crucial role in transforming the industry, and many major companies already use Digital Twins for solving problems and improving efficiency [8, 9]. The idea of a Digital Twin (DT) is relatively new. It was conceptualised during the very beginning of the 21st century and has gained traction mainly during the last decade [10]. The primary reason behind it is the digitalisation of the industry, which has been accelerated by the newly emerging Information Technology (IT) and its infrastructure. Gartner had listed DT as one of the key emerging technologies in 2017 [11], and it was also positioned at the peak of the hype-cycle curve in 2018 [12]. Figure 2.1 indicates a few well-known technologies and the evolution of their position on the hype-curve, over the last few years [13–15].

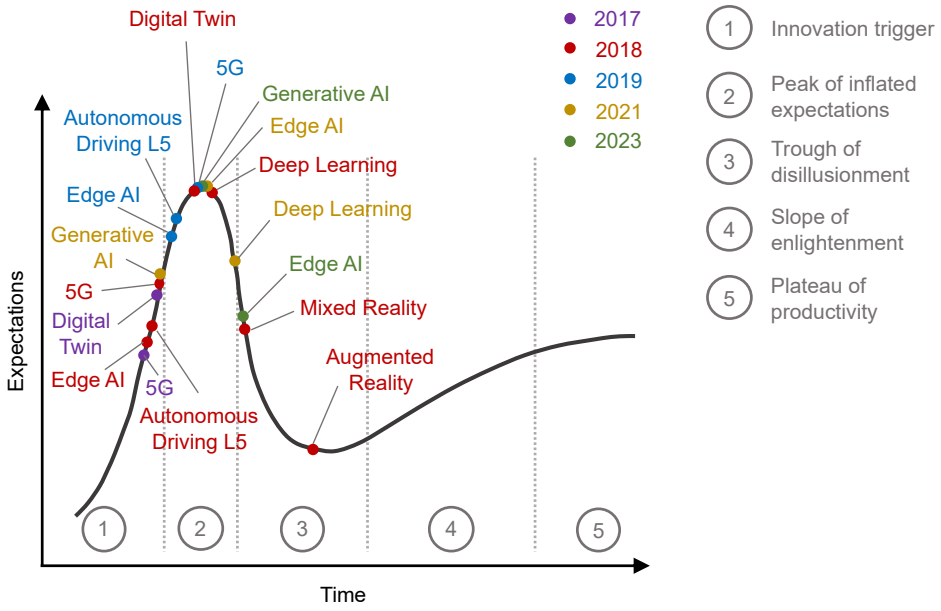


Figure 2.1: The evolution of Digital Twin technology on Gartner's hype-cycle curve, including some additional emerging technologies. The data is sourced from Gartner's reports and press releases [11–15].

The five stages of this evolution are (1) innovation trigger, (2) peak of inflated expectations, (3) trough of disillusionment, (4) slope of enlightenment, and (5) plateau of productivity. The hype cycle lasts for 2-5 or 5-10 years for most cases (and less than 2 or more than 10 years for some). Digital Twin technology has been marked with 5-10 years, and thus, is expected to be in between stage 4 and 5, where the technology starts to mature and shapes up to be incorporated in different applications.

Thus, the concept of Digital Twin is still not fully mature and keeps evolving and becoming more elaborate. It originally emerged in the aerospace industry, developed in the manufacturing domain, and was further adopted by several other sectors such as healthcare, telecommunication, construction, agriculture, energy, environment, *etc.* Through its evolution, the concept of Digital Twins has varied depending on the context, application field, and one's expertise or experience. As a result, there has been large fragmentation in its definitions and models. A Digital Twin can be described as a continuously updated virtual representation of an object, system, or process which replicates all phases in the lifecycle of its physical counterpart. Although this underlying idea remains the same, many applications and publications define it as too context-specific.

As a key technology in the ongoing Industry 4.0 (and the upcoming Industry 5.0), there is a clear need for more clarity on the concept of a Digital Twin and to provide generalised descriptions in the form of a definition, an architectural model, and its working principle. A Digital Twin is also often misinterpreted as being the same as any model in the virtual space. Whereas, DT is actually much more than that, and its representation in the virtual space is just one facet of it [5]. Thus, it is critical to define clear boundaries, features, and capabilities, as well as the criteria to classify a digital model of a system as its Digital Twin.

This chapter aims to review the notion of Digital Twins in the context of Industry 4.0, to comment on existing definitions and architecture models of DT, and to propose improved versions of those with a focus on microelectronics as a product for the latter. The Sections 2.2 and 2.3 describe the development and adoption of DT by different industries, including the evolution of the underlying IT technologies. Various existing definitions of DT are examined, and then a more generalised but detailed definition of a Digital Twin is formulated.

The Sections 2.4 and 2.5 describe the basic architecture of a Digital Twin-based system and review a few existing and well-known workflow models. Furthermore, a new simplified model is proposed, and an implementation of Digital Twins for the Prognostics and Health Management (PHM) of microelectronics is outlined. In addition, a holistic approach for hybrid-PHM of electronic components and electronics-enabled systems is also presented with the help of the new two-branched DT model. Lastly, the key advantages, challenges, and future roadmap are highlighted.

2.2. Digital Twin — Development

The idea of a Digital Twin was first introduced by Dr Michael Grieves in 2003 in a university course on Product Lifecycle Management (PLM), while the term was

used much later in his 2011 book [16] and more elaborated on in his 2014 white paper [17]. The latter also attributes to Vickers, and thus, the mentions of the formation of the concept by Grieves and Vickers together can also be found in the literature [18]. The first mentions of Digital Twin can be found in the technology roadmap of National Aeronautics and Space Administration (NASA) in 2012 (draft in 2010) [19, 20]. The NASA roadmap was referred to by aerospace engineers as the seminal work to define the Digital Twin. The 2012 publication by Glaessgen and Stargel [21] lists Digital Twin as a key technology and, thus, is also cited by a plethora of recent publications as the origin of the Digital Twin concept. It was later adopted by different industries, and thus, several contextualised adaptations of a Digital Twin can be found in the literature.

Thus, the first two decades of the 21st century were the two key periods, respectively, for the formulation and early adoption of the Digital Twin technology. Its roots, however, go much further back in time. Digital Twins are enabled by the underlying foundational technologies developed during the 3rd industrial revolution, also known as the Computer Revolution, during the last 30 years of the 20th century. Therefore, in order to understand the concept more comprehensively, it is important to have an overview of the technological development and milestones in the context of digitalisation over the past 50 years.

2.2.1. History of Digitalisation

The evolution of digitalisation has gone through four progressive stages: digital enablement, digitalisation assistance, digital control and link, and cyber-physical integration [10]. The first stage refers to the process of converting paper documents into digital forms. In this phase, around the year 1950, only the most essential information was digitised for storage, processing, and transfer.

In the late 1970s, computers became small and inexpensive enough to be purchased by individuals, when a large-scale integration made it possible to construct a sufficiently powerful microprocessor on a single semiconductor chip [22]. Computers further evolved in the 1980s to have a Graphical User Interface (GUI) and with the extensive applications of Computer-Aided 'X' (CAX) technologies, *e.g.*, Computer-Aided Drawing (CAD), Computer-Aided Engineering (CAE), and Computer-Aided Machining (CAM), the paradigm of digitalisation shifted towards assisting engineers to work with computers effectively.

The digitalisation of entire businesses was possible in the 1990s with the development of the internet and advanced control technologies [23]. With the increasing spread of workstations and personal computers, the number of simulation users grew rapidly, and the simulation technology further evolved. Today, simulation is

the basis for design decisions, validation and testing not only for components but also for complete systems in nearly all application fields [24].

Electronic components became more and more compact during the first decade of the 21st century, which resulted in the evolution of consumer electronics such as compact, lightweight laptops, smartphones, and later smart devices along with the services associated with them, *e.g.*, cloud storage. As a result, a new generation of information technologies such as the Internet of Things (IoT), cloud computing, big data analytics, and Artificial Intelligence (AI) emerged. They enabled the convergence of physical and virtual worlds, which is also referred to as the cyber-physical integration [25], and therefore, digitalisation is now becoming one of the main drivers of innovation in all sectors [26].

Table 2.1 summarises the highlights of the four key stages of digitalisation. The progress in the latter half of the digitalisation era has dramatically improved the capabilities of computers. As a result, simulation technology also evolved. Digital Twins are the next wave in the simulation technology [24, 27] and are rooted in existing technologies, such as Three-Dimensional (3D) modelling, system simulation, and digital prototyping (incl. geometric, functional, and behavioural prototyping). Thus, the Digital Twin technology stands on the foundations of the technologies developed during the Computer Revolution, also known as the Information Age.

2.2.2. Review of Digital Twin Definitions

Digital Twin has been defined in the literature in a variety of ways. They range from a very high-level abstract and simplistic definition to a highly contextualised and rooted formulation. Highly contextual and application-specific definitions mostly contain technical jargon and, thus, don't necessarily translate well to other applications. Some high-level definitions are too generic and lack the necessary detail. It's rare to find a fit-for-all definition, primarily due to the fact that the concept of DT continues to evolve. Thus, it is crucial to analyse some of the existing key definitions. The 2012 publication by Glaessgen and Stargel [21] is cited by a plethora of publications as the origin of the Digital Twin definition [10, 24, 28–30], which is:

> "*an integrated multi-physics, multiscale, probabilistic simulation of an as-built vehicle or system that uses the best available physical models, sensor updates, fleet history, etc., to mirror the life of its corresponding flying twin*".

Since it originated in the aerospace application, it includes the term 'flying twin' and its 'fleet history' in the definition. It is also the most commonly used 'base' definition, which is then adopted and heavily contextualised for other applications. Other examples of contextual adaptations of this definition can be found in the literature [31–33], which are not generalised and, thus, non-transferable.

Table 2.1: The stages and highlights of the digitalisation era leading to the Digital Twin technology.

Stage	Description	Year	Highlights
1.	Digital Enablement	1950's	→ Paper documents to digital
		1970's	→ Sufficiently powerful microprocessor on a single semiconductor chip → Computers became small and inexpensive, thus, purchased by individuals
2.	Digitalisation Assistance	1980's	→ GUI, applications of CAX technologies (CAD, CAE, CAM)
3.	Digital Control and Link	1990's	→ Digitalisation of entire businesses → Development of the Internet and advanced control technologies → Simulation technology further evolved, and users grew rapidly
4.	Cyber-Physical Integration	2000's	→ Electronic components became more and more compact → Consumer electronics: lightweight laptops, smartphones
		2010's	→ New generation of IT emerged: IoT, cloud computing, big data analytics, AI → It enabled the convergence of physical and virtual worlds
		2020's	→ Digital Twinning is the next wave in the simulation technology → Rooted in existing technologies (3D modelling, digital prototyping)

Digital Twinning was later adopted by many different industries, predominantly by the manufacturing industry. As more and more research was dedicated towards this technology [10], the number of relevant publications began to grow exponentially [30]. As a result, several different definitions of a Digital Twin appeared in the literature. The multi-scale simulation capability facilitated by the structure of a Digital Twin, which is discussed later in detail in Sections 2.4 and 2.5, allows visualisation of a product or process at different levels of granularity. Hence, the definitions vary based on the context and application.

For example, a Digital Twin is defined in the context of production machines and related procedures (installation, commissioning, training, and optimisation) in [34], while it is defined for a manufacturing process in [35], as well as with reference to a service or business in [36]. Various definitions of a Digital Twin published during the years 2012–2016, the period after Industry 4.0 was defined, were analysed in [33] by Negri et al. to trace their evolution from the initial conceptualisation in the aerospace field to the most recent interpretations in the smart manufacturing domain. It is quite common to find definitions and models of DT in the context of manufacturing, as it was the next predominant industry to adopt DT.

One such example of that and another one in the Structural Engineering field are as follows: "*a coupled model of the real machine that operates in the cloud platform and simulates the health condition with an integrated knowledge from both data-driven analytical algorithms as well as other available physical knowledge*" [37]; and "*a high-fidelity structural model that incorporates fatigue damage and presents a fairly complete digital counterpart of the actual structural system of interest*" [38]. The former mentions a 'machine' while the latter mentions a 'structural system' and its 'fatigue damage'. Both are good examples of a DT definition being too context-specific.

In order to explain the concept of a Digital Twin in a more comprehensive and understandable manner, it is crucial to form a detailed and yet precise definition of a Digital Twin. Table 2.2 lists some of the more generalised definitions found in the literature. Important keywords within these selected definitions are also highlighted in grey to underline the unique qualities of a Digital Twin.

The generalised definition by the Digital Twin consortium [39] is a concise description of the Digital Twin concept, but lacks technological details. On the other hand, the definition by Heterogeneous Integration Roadmap (HIR) [40] is a detailed one; however, it is often perceived as too lengthy. The definition in the 2022 newsletter by *IEEE* Electronics Packaging Society (EPS) [4] strikes a reasonably good balance of being concise and detailed. Yet, there is a clear need to define a concise, fit-for-all definition of a Digital Twin that also includes its key features.

Table 2.2: Generalised Digital Twin definitions from the literature with important keywords highlighted.

Src.	Definition
[18]	*a comprehensive digital representation of a product that includes the properties, condition, and behaviour of the real-life object through a set of realistic models and data, which can simulate its actual behavior in the deployed environment.*
[24]	*a comprehensive physical and functional description of a component, product or system, which includes more or less all information which could be useful in all the (current and subsequent) lifecycle phases.*
[26]	*a collection of model-based simulations and data analytics, necessitated by requirements of the modern competitive industrial environment at all stages of design and production, to predict the outcome, optimize, correct and evaluate.*
[28]	*an integrated multiphysics, multiscale, probabilistic, and ultra-realistic simulation of systems or products which can mirror the life of its corresponding twin using available physical models, history data, and real-time data.*
[31]	*a multiphysics and multiscale simulation model that mirrors the corresponding physical twin, allowing the simulation of all life cycle phases of the system.*
[32]	*an organic whole of a physical asset and its digitized representation, which mutually communicate, promote, and co-evolve with bidirectional interactions.*
[34]	*an operational replica used for testing, commissioning, and training.*
[35]	*a replication of real physical production system, that enables bidirectional control with the physical process and is used for system optimization, monitoring, diagnostics and prognostics using the integration of AI, machine learning, and software analytics with a large volume of data from physical systems.*
[36]	*a virtual equivalent of an actual physical product or service.*
[41]	*a technology enabling the replication of the development and manufacturing of a product or production system over the course of its entire lifecycle, and to thereby predict behaviour, optimize operational utilization and apply knowledge gained in the context of earlier design and production efforts.*
[39]	*a virtual representation of real-world entities and processes, synchronized at a specified frequency and fidelity.*
[40]	*an instantiated model (numerical, analytical, hybrid) of an asset or device, which is deployed (in the cloud or on an edge device) and connected to the physical device, where the connection may be established through sensors installed at the device or other sources collecting information, delivering a continuous data stream fed into the model or as a boundary condition or a reference value.*

2.2.3. Formal Definition of a Digital Twin

After carefully reviewing these definitions (and their sources), a common thread can be drawn to understand the underlying concept on a deeper level. Thus, an even more generalised description can be formulated and is proposed as follows:

> Digital Twin is a continuously updated, multi-physics, multiscale, probabilistic simulation model of a physical entity (an object, a system, or a process) utilising big data, bilateral connectivity, and advanced software analytics to provide monitoring, diagnostics, prognostics, and optimisation services.

This definition also summarises the function of a Digital Twin and highlights its nuances and the involved technology. Therefore, it is an example of a concise definition that is also suitable for all types of applications of the Digital Twin technology.

2.3. Digital Twin — Adoption

The term 'Digital Twin' has become a commonly used phrase in the context of products, processes, businesses, and more. Originating in the aerospace industry, the concept evolved in the manufacturing sector and was later embraced by many other industries such as healthcare [42, 43], telecommunication [44–46], fashion [47–49], consumer electronics [50, 51], construction [52], environment [53, 54], agriculture [55], energy [56, 57], privacy and cyber-security services [58, 59], internet-based services and advertisement [60, 61] and several other applications [62].

2.3.1. Industry 4.0 and Smart Manufacturing

The adoption of Digital Twin technology by the manufacturing industry is linked with Industry 4.0, which represents the digital transformation of manufacturing/production and related industries and value creation processes [63]. This ongoing transformation of the traditional manufacturing industry was first defined as Industry 4.0 at Hannover Messe, Germany, in 2011 [64].

The introduction of next-generation information technologies, such as IoT, facilitated the evolution of traditional systems into cyber-physical systems. IoT enables embedding electronics, software, sensors, and connectivity into devices, to allow data collection and exchange through the internet [65]. Thus, cyber-physical systems get networked and can communicate with each other, enabling new ways of production, value creation, and real-time optimisation, creating the capabilities needed for smart factories [63]. Software and network connectivity extend the functionality of mechatronic systems, allowing traditional mechatronic disciplines – mechanics, electric, and electronics – to be realised in a more integrated way [24].

The evolution of IoT and cyber-physical systems, along with the development of simulation technology, has enabled the implementation of Digital Twins in the manufacturing industry. A Digital Twin implementation contains a physical entity as well as its digitised representation of the manufacturing entities (machines, equipment, environment, and even products). Both components mutually communicate, promote, and co-evolve with each other through bidirectional interactions [32], which are facilitated by Industry 4.0. The Digital Twin was first applied to Industry 4.0 by Siemens in 2016 [10].

Additionally, the introduction of commercial software tools for the creation of a Digital Twin, such as Predix (*GE digital*), Simcenter 3D (*Siemens*), Twin Builder (*ANSYS*), and Digital Twin Application Builder (*COMSOL Multiphysics*), demonstrates its importance for the industry as a whole. Moreover, the integration of two or more software tools, such as Creo 3D (*PTC*) with ANSYS Live Discovery and Maximo Manage (*IBM*) with Digital Twin Exchange (*IBM*), further facilitates building exchangeable and interoperable Digital Twins.

The review by Negri et al. [33] suggests that the scientific literature that describes the contextualisation of the Digital Twin concept in the manufacturing domain is still in its infancy. There is a need for future research on relevant industrial applications to investigate and demonstrate a wide range of applications and benefits to realise the full potential of Digital Twinning. An article by Aheleroff et al. [66] describes a holistic reference architecture model of DT for several other Industry 4.0 applications beyond the manufacturing domain.

2.3.2. Health, Telecom, and Other Industries

Health 4.0, analogous to Industry 4.0, is a commonly used term in the healthcare industry. It refers to the progressive virtualisation for enabling personalised and next-to-real-time health and care solutions for patients, professionals, and formal and informal carers [67]. Digital Twin technology holds the promise to deliver Health 4.0 [68]. In personalised healthcare, Digital Twin can be defined as a life-long, rich data record of a person combined with AI-powered models [69], which can provide proactive and preventive care in real-time without being in close proximity [68].

For example, the 'HeartModel' – a clinical application launched by Philips in 2015 – can assess several cardiac functions and provide insights into a possible heart failure [70]. A health-focused Digital Twin can provide assistance in determining the right therapy options for a specific patient, and can also be used to predict the outcome of specific procedures. On a larger scale, if behavioural data and contextual social factors are also integrated, Digital Twins can also help to better manage chronic diseases and the overall population health [69].

In telecommunication, the fifth generation standard for broadband cellular networks, *i.e.*, 5G, has been rolling out worldwide since 2019. A simulation-based approach is being extensively used to evaluate network coverage in cities by visualising wave propagation from several transmitter-receiver pairs located at different locations. An example presented in [71] illustrates a Digital Twin of an entire city, which by its definition is continuously updated over time to monitor changes in the city topology and, therefore, can provide suggestions for modification and maintenance of networking equipment.

In the construction industry, Digital Twins can enable design and energy-performance optimisation, real-time structural health monitoring, predictive and proactive maintenance, and efficient supply chain management. This is enabled by a combination of 3D modelling (such as a Building Information Model (BIM)) and data collection and analysis using an IoT sensor network [72, 73]. DTs are a great tool in environmental sciences to enable a more data-driven investigation to address challenges such as climate change, loss of biodiversity, flooding, and water and subsurface management and facilitate risk-based decision-making [74, 75].

The agriculture industry (Agriculture 4.0) benefits from the adoption of the DT technology, which can be applied to several subdomains of it, *viz.*, farming, processing, consumption, supply and value chain. It enables crop monitoring, resource optimisation and cultivation, livestock management, soil quality management, and identification of bottlenecks and waste [76, 77]. In the energy sector, DTs are applied to a variety of aspects such as energy management, conservation systems, transmission (grids), storage, and consumption for both traditional and renewable energy applications.

The fashion and retail industry has been adopting the Digital Twin technology in two ways. First, for creating personalised products such as smart textiles, shoes, and wearables. The Digital Twin of a customer can be used for analysing personal style, fit, and other parameters such as the financial capability to design as well as recommend products. Similar to the healthcare industry, this approach can also be implemented for a larger demography. The second approach is by using Digital Twin for products, such as footwear and shoes, for monitoring their degradation over time and detecting different ways of failure, and later to use this information for improving the design as well as the fabrication process [78].

Internet-based advertisement businesses run by companies such as *Google*, *YouTube*, and *Meta* (formerly *Facebook*), as well as online retail services such as *Amazon* have been using the Digital Twin approach, which is also referred to as surveillance capitalism, to create and maintain updated models of their users' interests to provide relevant advertisements and buying recommendations [79].

2.3.3. Reliability of Electronic Systems

The adoption of Digital Twin technology was enabled by the incorporation of more and more electronics, such as sensors, into conventional products and systems, as well as the integration of computer-aided and software-based technologies into traditional industries. IoT-enabled smart-home products such as AI-powered smart speakers, smart coffee machines, smart thermostats, *etc.*, are classic examples of this. Similarly, consumer electronics such as computers, laptops, and smartphones consist mostly of electronic components. Even the growth in automotive electronics, described in Chapter 1, indicates a big increase in electronics in terms of their cost and the importance of the (mission-critical) tasks they handle. Therefore, the reliability of these products as a whole, as well as of their electronic subsystems, has become highly critical.

Digital Twinning enables the ability of system optimisation, monitoring, diagnostics, and prognostics using the integration of AI, Machine Learning (ML), and big data analytics. It can be used for predicting failures and estimating the lifetime of electronic components, which then allows for scheduling preventive maintenance. As an example, *Apple Inc.* announced a replacement program for display control modules of certain iPhones manufactured between November 2019 and May 2020, foreseeing a display issue, where the displays are expected to stop responding to touch due to the faulty display module [80, 81]. Launching a preventive maintenance program like this allows the company to save time and costs and avoid customer dissatisfaction as well as unwanted lawsuits. This is facilitated by implementing the Digital Twin technology, which allows continuous monitoring of electronic components for their degradation over their entire lifespan. Thus, prognostics and health management are facilitated by a Digital Twin-based implementation.

2.4. Digital Twin — Architecture

The industry-wide adoption of the Digital Twin technology makes it ever so crucial to study its architecture, alongside its definition, in order to understand its workflow and functions. Similar to the definition of a Digital Twin, its architecture has also seen some transformations and contextual adaptations, which are built on the same conceptual base.

2.4.1. Basic Structure

The basic structure of a Digital Twin system consists of a physical entity, its virtual representation, and an active connection between the real and virtual space for information flow. Figure 2.2 shows the baseline architecture of a Digital Twin system. The physical entity can be any object, system, or process. It can also be implemented

at different scales of an ecosystem. For instance, a manufacturing facility can have DTs of the product, machines and tools, processes, a control volume, or even the entire business. In the context of microelectronic systems, a product-specific implementation is the most relevant one when reliability and lifetime prediction are the main focus.

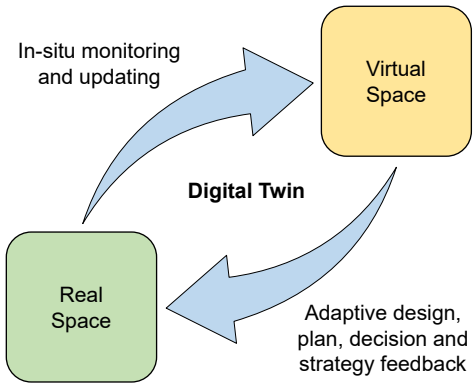


Figure 2.2: The basic architecture of a Digital Twin system, consisting of a physical entity, its virtual representation, and an active connection between the real and virtual space for information flow.

The connectivity between the physical entity and its virtual representation is what sets a Digital Twin system apart from just a nominal model. The connections facilitate data exchange, which enables a continuous update of the model rather than it remaining static. Similarly, the results generated from the updated model can be used as feedback for improving the physical product. Thus, bilateral connectivity is the key to building an effective Digital Twin system.

2.4.2. TYPES OF CONNECTIONS

The continuous update of the digital model in a DT system is achieved by the information exchange through its connection to the physical entity. These connections can have different levels of complexity and can be roughly categorised into three types: weak, cloud-based, and embedded. Figure 2.3 schematically illustrates the key differences in these three kinds of connections to a Digital Twin. Each of these approaches is suitable for different kinds of applications and use cases.

(a) Weak Connection: This configuration utilises a unidirectional flow of information, *i.e.*, from the product to its model. There is no closed loop, and thus, the continuously updated model serves as a supporting tool and has limited functionality. This configuration is sometimes referred to as a 'Digital Shadow' [82]. It can mainly be used for virtual prototyping and product/process design.

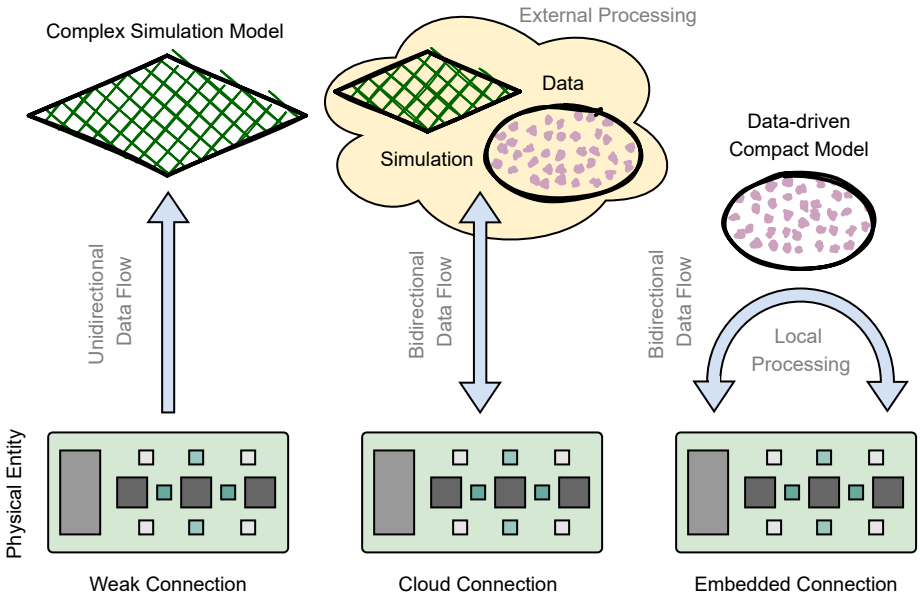


Figure 2.3: Three types of connections in a Digital Twin system, *viz.*, weak, cloud-based, and embedded, each of which differs in the direction of the information flow and the complexity of the digital models.

(b) Cloud-based Connection: This setup explicitly utilises a powerful computing infrastructure external to (and in most cases, distant from) the physical entity. This connection allows for real-time monitoring of a product, data filtering, and transmission. A cloud-based platform facilitates processing and producing large amounts of collected data. This data can then be utilised for product or process improvement with the closed-loop connectivity. Another advantage of this is the capability to run bigger and more complex simulation models on an external computational node. A caveat of this implementation is the higher latency and energy consumption due to the involved data transmission.

(c) Embedded Connection: An embedded connection moves the computation to the edge, which allows models to run locally. It also incorporates real-time monitoring and data collection, but processes the data on an edge-computing infrastructure. This saves the cost and energy of transmitting the data to an external server and, thus, is more efficient. In this way, an integrated closed-loop control and decision-making can be achieved. The shortcoming of this approach is the limited computational power available at the edge, *e.g.*, a Micro-controller Unit (MCU). Therefore, only simpler and computationally lighter (compact) models, such as response surfaces or meta-models, can be utilised in this approach.

2.4.3. Digital Twinning Approach

Digital Twins can be built based primarily on two approaches – physics-based and data-driven. A physics-based twin relies on the knowledge of physics-of-failure or physics-of-degradation models to represent the accurate thermal, electrical, chemical, and mechanical behaviour of materials. This approach is good for accurately representing (only) known physical phenomena using mathematical relations. At the same time, they may not capture all aspects of the physical reality.

A data-driven approach generally relies on the sensor data from the physical product, *i.e.,* real in-situ measurements, and input-to-output correlation techniques that generally have an inherent black-box structure and cannot necessarily always describe the physical mapping between the input data and the prediction.

A hybrid approach combines the workflows of both the physics-based and data-driven approaches. Physics-Informed Neural Networks (PINNs) with aided data are a good example of a hybrid approach. Another example is when a physics-based validated model (such as a Finite Element simulation) is used as a source of data that serves as an input for the data-driven approach. The hybrid approach has the potential to overcome the individual limitations of the physics-based and data-driven approaches.

2.4.4. What is *NOT* a Digital Twin?

The term Digital Twin is often used freely and interchangeably with different digital representations of a physical entity. This, however, misrepresents the actual concept. Thus, to avoid confusion and maintain consistency, it is crucial to understand and clearly define what a Digital Twin is not.

A multi-physics multiscale model is commonly referred to as a Digital Twin. Although such a model accurately represents its physical counterpart (*e.g.,* with a high-fidelity Finite Element model), it cannot always be classified as a Digital Twin. Only when it can be continuously updated through the information exchange with its physical counterpart to represent its current (aged) state, can it qualify as a DT. Bilateral communication is the key to differentiating a model (*i.e.,* essentially just a time-based instance of a DT) from a Digital Twin.

A physical entity can also be represented in the form of a control system flow diagram. Such a representation also cannot be called a Digital Twin unless it can be updated based on the current state of the physical entity. Even when it satisfies the criterion of a continuous update, a control diagram by itself does not suffice to entirely represent the physical entity. Thus, at most, it can be classified as one aspect of the (data-driven) Digital Twin.

2.4.5. Digital Twins and Product-Lifecycle

One of the crucial aspects of any product is its expected lifespan. For electronic components that are involved in mission-critical tasks (*e.g.*, steering functionality in an autonomous vehicle), the estimation of RUL is critical. Implementation of a Digital Twin system can significantly aid this task. However, this only covers the phase of 'product in use'. Digital Twins can be utilised at the different phases of a product's lifecycle, from an early design and prototyping phase to the later manufacturing, qualification, and in-use phases. However, the implementation varies as the product progresses through these phases.

Figure 2.4 indicates six different stages of a product lifecycle, *viz.*, product design, material selection and characterisation, production, usage and service, maintenance and repair, and recycling. A Digital Twinning approach can be applied individually to each one of these stages, which would have unique aspects associated with the real and virtual space (as indicated in Figure 2.4). This makes the Digital Twin multi-layered and multi-scale in nature, as it can be implemented individually for all of the stages within a product lifecycle.

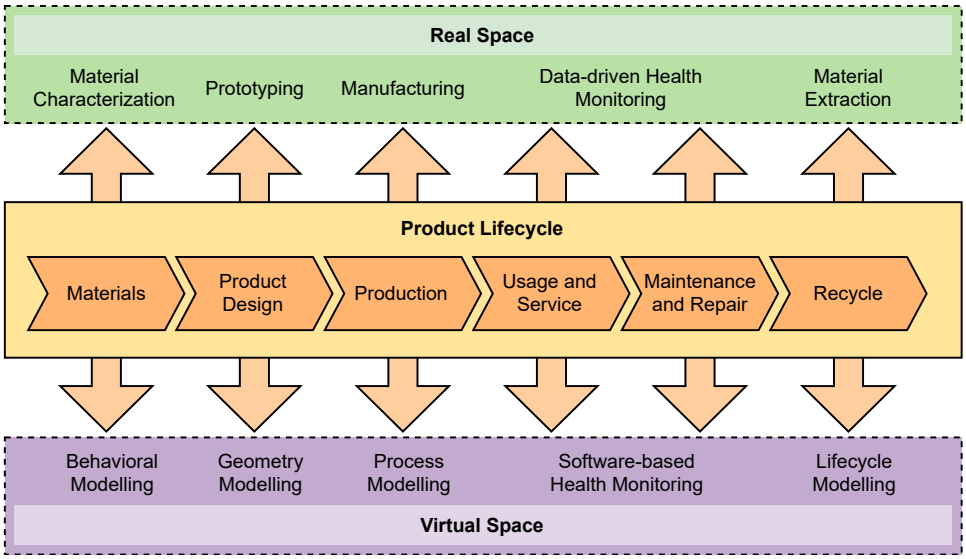


Figure 2.4: Different phases within a product's lifecycle and its corresponding aspects in the real and virtual space of a Digital Twin system.

At different stages, several different 'types' of Digital Twins are possible. Grieves [83] suggests three different kinds of implementations: a Digital Twin Prototype (DTP) in early design stages, a Digital Twin Instance (DTI) of a designed product that is being manufactured, and a Digital Twin Aggregate (DTA) for products manufactured

and deployed. Note that the classifications DTP, DTI, and DTA would apply to the cases where the physical entity is a 'product' and is not restricted to only the manufacturing domain. Figure 2.5 indicates the gradual transformation of these DT implementations through different stages of the product lifecycle.

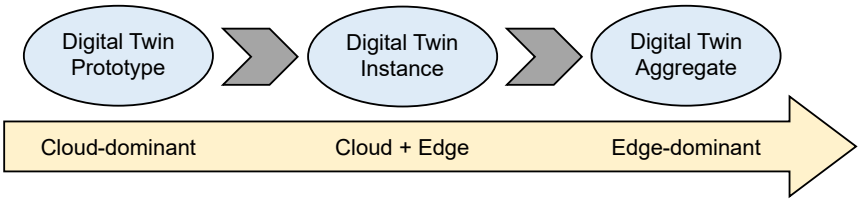


Figure 2.5: Different types of Digital Twins (*viz.*, DTP, DTI, DTA) for a product, as it progresses through its lifecycle stages (arrow), and the suitable computational infrastructure for these DT implementations.

The DTP primarily utilises a physics-based approach and complex simulation models. It can rely on a 'weak' connection setup in the initial phases and move to a closed-loop cloud infrastructure as the product moves from the concept to the manufacturing stage. The DTI is utilised when the products are manufactured and undergo qualification tests. It uses both physics-based and data-driven approaches, yet heavily relies on the former. The DTA is relevant when the product is in use in the field. A data-driven approach and an embedded connection with edge computation are most suitable for this phase. Thus, the three types of DT implementations also gradually progress from being primarily physics-based to a predominantly data-driven approach. Both cloud-based (computationally expensive) and edge-based (local processing) implementations can be combined to varying capacities depending on the needs of a specific application.

2.4.6. IMPLEMENTATION SCALES

Digital Twins are also not limited to just the product itself. As the presented definition (Section 2.2.3) states, the physical entity can also be a 'process' or even a 'business'. Thus, the manufacturing process of semiconductor devices and Integrated Circuits (IC) packaging can be modelled, monitored, and optimised using a Digital Twin. The fabrication and assembly process of electronic components is a multi-step complex affair and can be split up into multiple sub-processes, and therefore, individual Digital Twins can be prepared. Similarly, it applies to different scales of businesses associated with the semiconductor industry, *e.g.*, a wafer fab or foundry, Outsourced Semiconductor Assembly and Test (OSAT), Electronics System Design and Manufacturing (ESDM), Assembly, Testing, Marking, and Packaging (ATMP).

Therefore, there can be several Digital Twins at different phases, scales, and functions of electronics-enabled products, processes and businesses. They can be fo-

cused on different aspects such as PHM, PLM, supply chain, and manufacturing. Individual DTs, like their physical counterparts, need to be interlinked, and thus, integration of their databases also becomes important for developing DTs for a large system, such as a packaging assembly line.

2.5. Digital Twin — Models

The contextual interpretations of a Digital Twin in various fields reveal several interaction models of its architecture. All of them essentially emerge from the basic architecture shown in Figure 2.2. Notably, two main 'generalised' models (*viz.*, a three- and a five-dimensional model) are utilised as the baseline for various applications, and different adoptions of both can be seen widely in the literature. Figure 2.6 (a) and (b) show the three- and five-dimensional models, respectively.

2.5.1. Three and Five-dimensional Models

Initially, a three-dimensional 'information mirroring' model of a Digital Twin was published by Grieves in 2014 [17], which consists of a physical object, its model in the virtual space, and the connection enabling data exchange. Later in 2018, Tao et al. [84] introduced an updated five-dimensional version of that model. This version denotes four aspects of a DT by 'nodes'. It creates a separate node for 'data' and includes a new node called 'services'. The 'connections' stay as an independent dimension connecting each node to every other node.

The three-dimensional model is a bit too similar to the basic architecture (Figure 2.2). Numerous adaptations of this model in the literature often seem to add and define more components, especially the 'data', within the primary three dimensions. Thus, the model itself comes across as too generic and needs some modifications for more clarity. The five-dimensional model adds some value to the basic architecture (and the three-dimensional model) by defining 'data' as a separate entity. In addition, the outputs that the digital models and data processing can produce are collected together in the 'services' node. Moreover, every node can receive input and provide some feedback to every other node.

Figure 2.7 indicates the expanded version of the five-dimensional DT model that is contextualised for the microelectronics domain. It considers an electronic 'product' as the physical entity and thus includes some details specific to Electronic Components and Systems (ECS). Each of the five 'dimensions' serves a certain set of unique functions, and they are interdependent on each other.

The 'physical entity' can be a product, process, or business. It should be equipped with data collection capabilities and device control protocols. For example, an

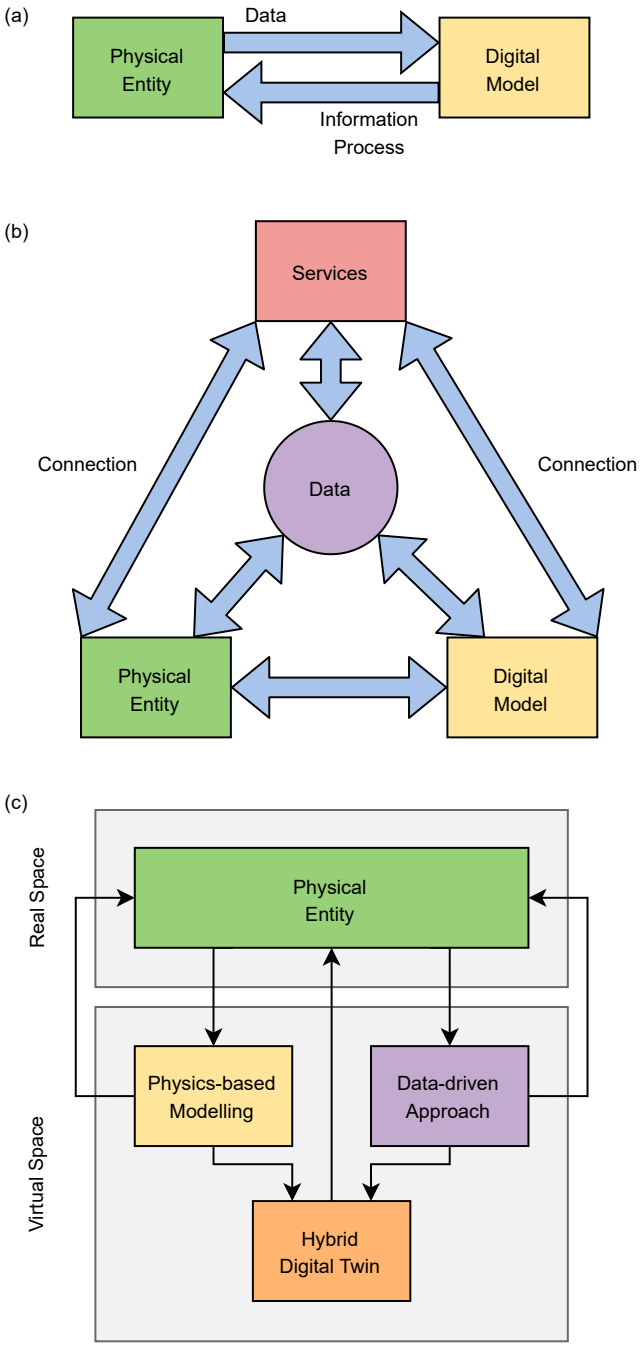


Figure 2.6: The comparison of three different generalised models of the Digital Twin architecture: (a) Three-dimensional model by Grieves [17], (b) Five-dimensional model by Tao et al. [84], (c) the new two-branched model. The newly proposed 'generalised two-branched model' has a simplified approach to structuring a Digital Twin system for PHM with a clear separation between the real and virtual spaces. The two main modelling approaches (*viz.*, physics-based and data-driven) form the two branches of the digital models, which can be combined to a different capacity for hybrid PHM.

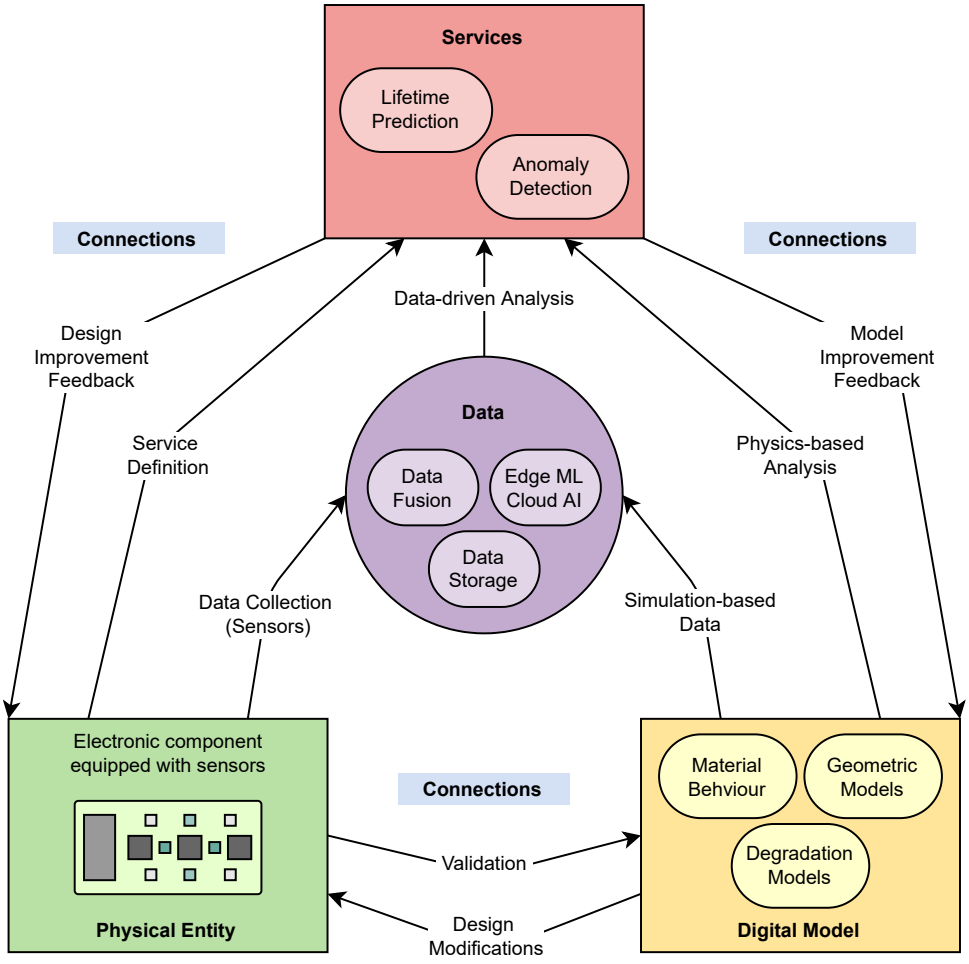


Figure 2.7: Five-dimensional Digital Twin architecture contextualised for the domain of microelectronics. An electronic product is considered the physical entity, and accordingly, the rest of the four dimensions are populated with the relevant details of their corresponding functions.

electronic product should be equipped with sensors to collect, process, and transmit data for its condition monitoring. The 'digital model' is a comprehensive model of the physical entity capable of multiscale multi-physics simulations. The digital model is continuously updated to replicate the current (degraded) state of the physical product based on the collected sensor data and inputs from the 'data' node. The digital model can provide additional data using simulation-based virtual sensors, especially where it's not practical or possible to have a physical sensor placed and record measurements.

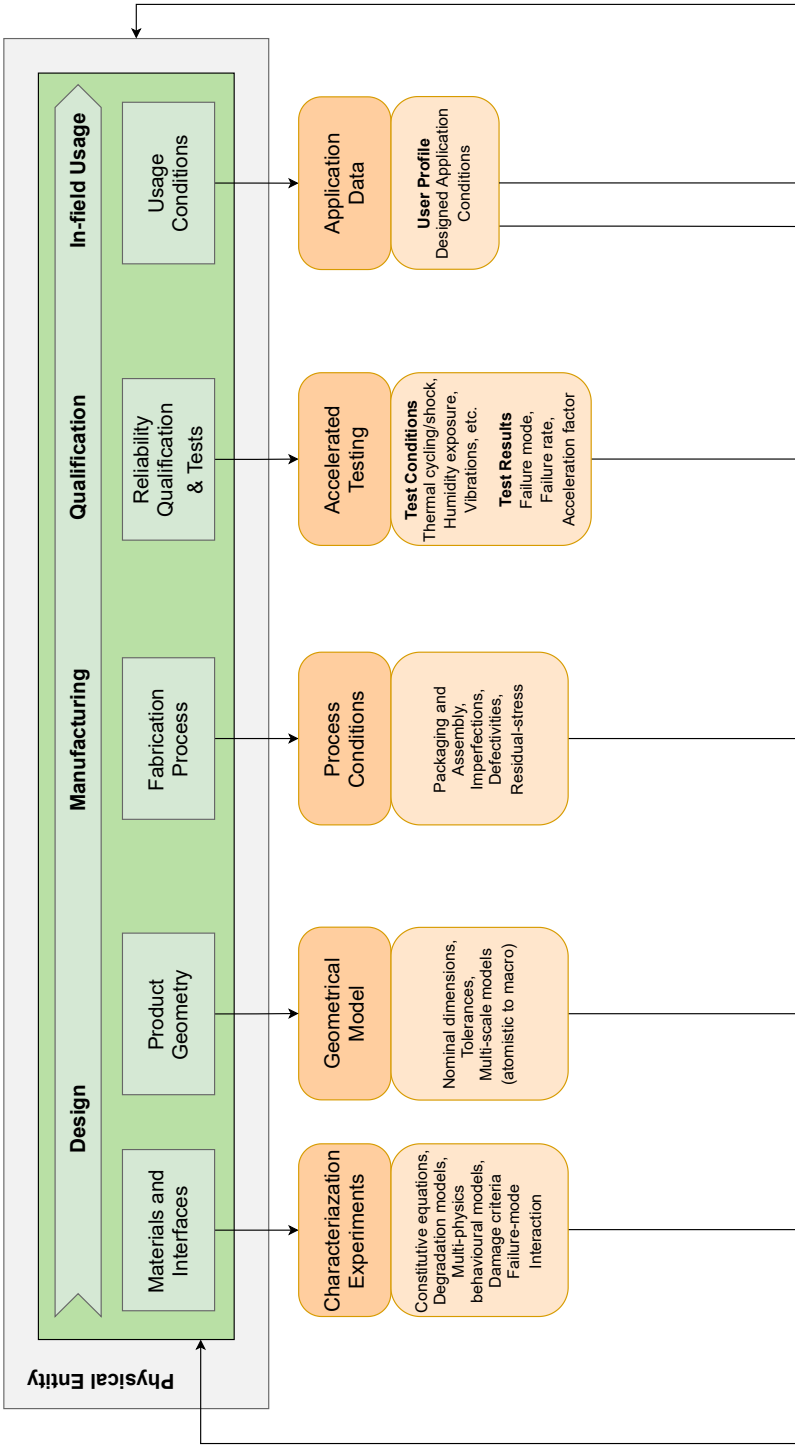
The 'data' node collects, stores, and processes the data coming from real and virtual sensors. It handles the data-driven aspect of a Digital Twin and can run algorithms (on the cloud, at the edge, or as a combination of both) for failure classification, RUL estimation, and optimisation problems. Based on the results generated by the 'data' and 'digital model' nodes (data-driven and physics-based approach, respectively), services such as anomaly detection and reliability prediction can be built. The prediction 'services' serve as an input for making design modifications to the physical product and for improving the other two nodes. Lastly, the 'connection' node ties the other four nodes together. It serves the same role as in the three-dimensional DT architecture, but a distinct definition underlines the importance of efficient communication and interoperability of the exchanged information between the rest of the nodes.

The shortcoming of this model is, however, the lack of a clear separation between the physical and virtual spaces. The representation may indicate an equal weight to all four nodes. In reality, that depends on the application. One of the nodes can be significantly bigger (*i.e.*, more important and/or resource-intensive) than the other. Another challenge it poses is in expanding this representation for different phases in a product's lifecycle. Thus, we identified a need for a more simplified model that can address these challenges and represent a DT architecture even more clearly.

2.5.2. Two-branched Model and PHM

The generalised two-branch model, indicated in Figure 2.6 (c), builds on the basic architecture while adopting some of the elements from the aforementioned models. It has a simplified approach to structuring a Digital Twin system, especially for product-specific PHM, with a clear separation between the real and virtual spaces. The two branches of the digital models are based on the two main modelling approaches: physics-based and data-driven modelling. Either one of these two branches can be the digital model on its own, which can provide 'services', and form a closed feedback loop with the physical product.

Furthermore, the two modelling approaches can be combined to a varied capacity to get a hybrid Digital Twin. This becomes more relevant when the DT implementation takes the forms DTI and DTA (described in Section 2.4). The digital models can draw inputs from one or more phases in the product lifecycle. Thus, three key aspects of building Digital Twins are (i) characterisation of material behaviour (with ageing effects), (ii) modelling loading conditions from several steps of the manufacturing process and qualification tests, and (iii) building infrastructure for in-situ data monitoring and processing while the product is in use. Figure 2.8 elaborates on this with an expanded version of the two-branched model. It is prepared considering microelectronic components and systems (*i.e.*, a product) as the physical entity.


Physical Entity
Design
Manufacturing
Qualification
In-field Usage
Materials and Interfaces
Product Geometry
Fabrication Process
Reliability Qualification & Tests
Usage Conditions
Characterization Experiments
Constitutive equations, Degradation models, Multi-physics behavioural models, Damage criteria Failure-mode Interaction
Geometrical Model
Nominal dimensions, Tolerances, Multi-scale models (atomistic to macro)
Process Conditions
Packaging and Assembly, Imperfections, Defectivities, Residual-stress
Accelerated Testing
Test Conditions
Thermal cycling/shock, Humidity exposure, Vibrations, etc.
Test Results
Failure mode, Failure rate, Acceleration factor
Application Data
User Profile
Designed Application Conditions

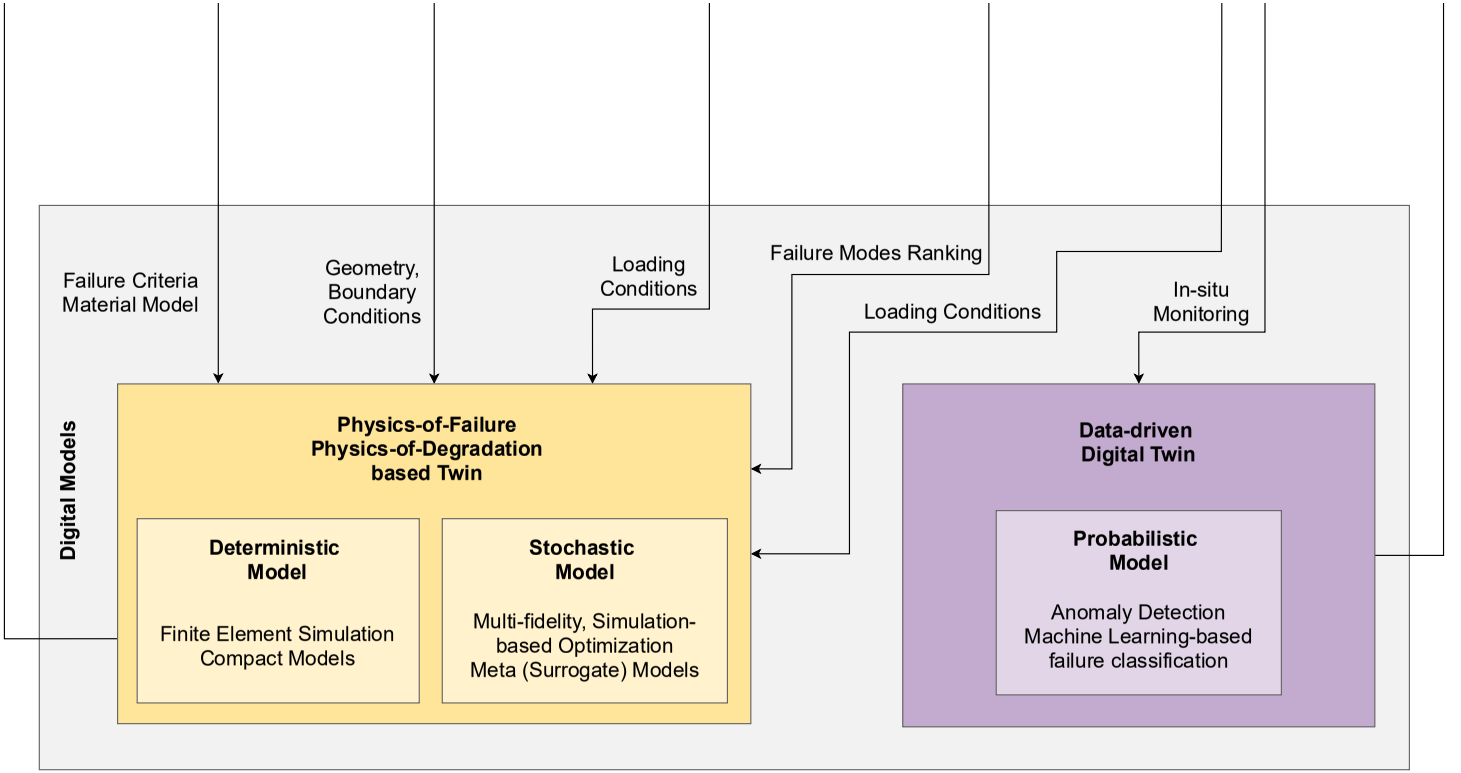


Figure 2.8: The expanded version of the 'generalised two-branched' Digital Twin model. In this description, the physical entity is a product (*e.g.*, a microelectronic system) and its PHM is the key purpose. Along with the different phases within the product lifecycle, a select number of specific inputs that the digital models can draw from different aspects of the product are also indicated.

The digital space can utilise inputs from several lifecycle phases of the product. The text in the 'physical entity' box indicates the features that the Digital Twin can extract from its physical counterpart. A similar approach is utilised in the Reference Architecture Model in Industry 4.0 (RAMI 4.0) for DT [66]. The key differentiation is that RAMI 4.0 includes different terms for the digital replica based on their level of integrity (*i.e.*, the connection type), while the two-branched model keeps a consistent naming scheme for 'Digital Twin' and classifies them based on the connection type (Figure 2.3). In the two-branched model, the number of features and their combinations included in a digital model can vary depending on their availability and the type of Digital Twin implementation (*i.e.*, DTP, DTI, DTA). For instance, a physics-based Digital Twin can consider loading conditions from the manufacturing stage or the in-use stage. Thus, the two-branched model provides a generalised framework for preparing (product) Digital Twins of different complexities and modelling approaches.

Product-specific health monitoring (Section 1.5) can be achieved using a Digital Twin approach. The PHM workflow described in Figure 1.4 utilises a combination of physics-based and data-driven approaches. Thus, it fits perfectly well with the proposed two-branched DT architecture, as it also requires developing both Physics of Degradation (PoD) and data-driven models. An example of a PoD-based Digital Twin (a DTI) that models thermomechanical degradation of electronic packages due to the thermo-oxidative ageing of moulding compounds has been presented in Chapter 4 (and in the article [85]). Another example of in-situ monitoring has been investigated in Chapter 5 (and in the paper [86]), which shows a specialised degradation-monitoring sensor that can serve as an input to the data-driven models as well as for validation for physics-based simulation models. Moreover, Reduced-Order Models (ROMs) are key in edge-computing (for an 'embedded connection' of a DT). Integration of thermomechanical ROMs with full-order physics-based models has been explored in Chapter 6 (and in the publication [87]).

Such examples plug into the DT framework as various aspects of the virtual space and form the building blocks for the two-branched architecture (Figure 2.8). The developed models are then utilised for fault detection, diagnosis, prognosis, and quantification of RUL based on the current state of component degradation. Digital Twin-based hybrid PHM of electronics-enabled systems works as follows. A product is monitored continuously when in use, *i.e.*, in-situ monitoring, using a variety of advanced sensors. The data collected by the sensors is used for anomaly detection on the edge. Anomalies are reported, and otherwise, data is utilised for a data-driven algorithm for the prediction of RUL. This can either be on the cloud (bigger and complex models) or on the edge (ROMs or meta-models).

Simultaneously, the sensor data is utilised to identify the total exposure to 'harsh' environmental conditions, and an equivalent degradation of the material is quantified based on the ageing models. The current state of degradation is then utilised to update the physics-of-failure-based (such as a Finite Element) model of the product. Possible failure modes and resulting RUL are estimated based on the multi-scale multi-physics simulations, historic database, and standards. The simulations run mostly on an external cloud-based computational unit. In this way, a combination of edge and cloud connectivity, as well as computing, can be utilised for a Digital Twin implementation for health monitoring and reliability assessment of an electronic product, on a per-product basis. Based on the estimation, condition-based maintenance can be suggested, which forms a closed loop of connectivity between the physical and virtual worlds.

2.5.3. Advantages, Challenges, and Roadmap

A Digital Twin-based approach facilitates next-generation reliability assessment (*i.e.*, the third and fourth 'wave' in reliability engineering [88]) and PHM of microelectronics. At the same time, there are some important challenges to be addressed. To enable DT implementation in different aspects of a complex ecosystem (*e.g.*, a manufacturing facility), industry-wide standards need to be established and adopted; for example, for the data exchange formats, interoperable IoT connectivity, and cyber-security. Moreover, it is crucial to have more advanced, low-cost, and reliable sensors and different measurement techniques for in-situ monitoring and to integrate them into products to make the system capable of self-monitoring.

Characterisation and modelling of different materials used in an electronic component is a *multi-scale* challenge. For example, a Cu/SiO_2 interface is characterised and modelled on different scales (from molecular-level to macro-scale) using first-principle simulations, Molecular Dynamics (MD) simulations, and finite element simulations. Different phenomena such as electromigration, sulphidation, and oxidation, which are associated with the Copper Nanoparticle (NanoCu) material, are modelled using MD simulations. Similarly, different kinds of simulations and modelling approaches are utilised for deducing a model of the behaviour of different materials and interfaces such as phosphors, phosphor-silicone interface (in Light-Emitting Diode (LED) packaging), Carbon Nanotube (CNT) pillars, *etc.* Another aspect of modelling, crucial for a Digital Twin implementation, is the characterisation of material degradation and the change in behaviour of aged materials.

Modelling of processes involved in manufacturing an electronic component is a *multi-physics* challenge. For example, modelling of the sold reflow process involves a moisture-thermal-mechanical coupling. This involves hygroscopic swelling due to moisture diffusion, moisture-induced stresses due to vapour pressure, and me-

chanical stresses due to a mismatch of thermal expansion properties of different materials in an IC package. Similarly, different coupled approaches are involved in other processes such as sintering, moulding, etc. Design of a process (*e.g.*, flipchip packaging, chip-package-system co-design, and optimisation of thermal stresses) can be assisted by simulations utilising the material models.

The approach to model the standard tests used for reliability qualification and product testing is similar to the aforementioned process modelling. These tests include functional (electrical, optical, *etc.*) performance tests, thermal tests (thermal resistance and junction temperature testing), and accelerated reliability qualification testing (thermal cycling, thermal shocks, moisture cycling, *etc.*). Verification, validation, and correction of the material behaviour model can be achieved using the experimental results of these tests. Thus, the cloud-based digital models need to be multi-scale, multi-physics, and consider complex non-linear and ageing effects.

On the other hand, more efficient compact models (ROMs, meta-models, response surfaces, *etc.*), and AI-based techniques (unsupervised learning, ML-based classification, *etc.*) need to be developed for edge-deployment and local data processing. A purely physics-based approach is challenging to model, whereas a purely data-driven approach is confined to a black box. Thus, both of these approaches for RUL estimation are limiting. Therefore, a hybrid Digital Twinning approach can utilise the best of both approaches.

The key milestones in the context of failure criteria are the definition of accurate failure-threshold levels and the know-how of multi-failure-mode interactions. A push towards simulation-driven design and optimisation, and a transition from a deterministic to a probabilistic/stochastic simulation methodology is crucial. A more robust collection, storage, filtering, and processing of big data, a closed-loop control algorithm, and increased edge-computing capabilities are also essential.

The overall roadmap for the next 5-10 years for addressing the challenges associated with the Digital Twin technology can be summarised as the following six points: (1) smart in-situ sensing and data transmission, (2) edge computing capable hardware, (3) accurate compact/meta-models integrated into products, (4) robust multi-scale multi-physics (nonlinear, dynamic, probabilistic) simulation models, (5) robust data-driven models, and (6) lifetime prediction on demand. Working towards these six goals would push forward the state-of-the-art of Digital Twins.

Finally, Digital Twins are also instrumental in realising the next phase of the industrial revolution (Industry 5.0), which would be an extension of Industry 4.0 and focused on human-centric development, sustainability, and resilience [89, 90]. It has been identified by the *European Commission* as one of the six key technology

pillars of Industry 5.0 [91]. DTs enable health monitoring and preventive maintenance of products and systems, which can help extend their lifetime, taking a step towards a more sustainable and circular economy.

Conclusion

Digital Twinning is a key technology in Industry 4.0. It has evolved from its conceptualisation in the aerospace application to its adoption in manufacturing, automotive, healthcare, and several other industries. The literature shows a big fragmentation in the definitions and architectural models of a Digital Twin. This is largely due to the deep contextualisation of DT and application-specific publications. This chapter addresses three main aspects of the Digital Twin technology – the definition, the architecture, and the framework for (electronic) product-specific DTs.

Along with a detailed review of different kinds of DT definitions, a generalised, information-rich, and yet concise definition is presented. Furthermore, the existing three-dimensional and five-dimensional models of the DT architecture are analysed. To overcome their identified disadvantages, a new two-branched model is proposed along with its expanded version for a product-specific monitoring device. The integration of the simplified PHM workflow into the proposed two-branched DT model is described. Three different categories of classifying Digital Twins are defined based on the (i) type of connection (*viz.*, weak, cloud-based, embedded), (ii) computational infrastructure (*viz.*, cloud and edge), and (iii) modelling approaches (*viz.*, physics-based, data-driven, and hybrid). A combination of aspects within these categories gives three main scales of DT implementation in a product lifecycle: DT 'prototype', 'instance', and 'aggregate' (DTP, DTI, and DTA).

Digital Twins can also be implemented on multiple scales of an ecosystem. Thus, they are not only relevant for electronic 'products', but also for the 'processes' and 'business models' associated with the semiconductor industry. It is important to consider certain criteria to classify a digital representation of a physical entity as a DT. The term Digital Twin should not be used interchangeably with a virtual instance or a model. The bilateral connectivity and active information exchange between the virtual and real spaces are what set a DT apart from them. Finally, the challenges associated with the DT technology can be addressed by more powerful computing infrastructure, energy-efficient edge-computing, advanced AI/ML-based models, standardised IoT connectivity, and cross-industry collaboration.

REFERENCES

[1] A. Inamdar, W. D. van Driel, and G. Zhang, *Digital Twin Technology - A Review and Its Application Model for Prognostics and Health Management of Microelectronics*, *Electronics*, vol. 13, no. 16, p. 3255, Aug. 2024, ISSN: 2079-9292 (Cited on p. 19).

[2] V. Guerra, B. Hamon, B. Bataillou, A. Inamdar, and W. D. van Driel, *Towards a digital twin architecture for the lighting industry*, *Future Generation Computer Systems*, vol. 155, pp. 80–95, Jun. 2024, ISSN: 0167-739X (Cited on p. 19).

[3] H. Moeller *et al.*, *Digital Twin Technology in Electronics*, in *Recent Advances in Microelectronics Reliability*, Springer, Cham, 2024, pp. 283–321, ISBN: 978-3-031-59361-1 (Cited on p. 19).

[4] A. Inamdar, P. Gromala, W. D. van Driel, and G. Q. Zhang, *Making the Digital Twin Work for Mission Critical Electronics*, *IEEE EPS Newsletter July 2022*, Jul. 2022 (Cited on pp. 19, 25).

[5] P. Gromala *et al.*, *Digital Twins for Electronics Packaging and Systems*, *IEEE EPS Newsletter November 2023*, Nov. 2023 (Cited on pp. 19, 21).

[6] A. Inamdar, W. D. van Driel, and G. Q. Zhang, *Digital Twin-Based Hybrid PHM Framework for Monitoring Package-Level Degradation*, in *European Safety and Reliability Conference (ESREL) 2023*, Southampton, UK, 2023 (Cited on p. 19).

[7] A. Inamdar *et al.*, *Digital Twins for IC Packages and Electronics-enabled Systems*, in *IEEE Smart World Congress (SWC) 2024*, Denarau Island, Fiji: IEEE, Dec. 2024, pp. 2125–2132, ISBN: 979-8-3315-2086-1 (Cited on p. 19).

[8] F. Tao and Q. Qi, *Make more digital twins*, *Nature 2021 573:7775*, vol. 573, no. 7775, pp. 490–491, Sep. 2019, ISSN: 14764687 (Cited on p. 20).

[9] F. Tao, M. Zhang, and A. Y. Nee, *Digital Twin Driven Smart Manufacturing*. Elsevier, Jan. 2019, pp. 1–269, ISBN: 9780128176306 (Cited on p. 20).

[10] Q. Qi *et al.*, *Enabling technologies and tools for digital twin*, *Journal of Manufacturing Systems*, vol. 58, pp. 3–21, Jan. 2021, ISSN: 02786125 (Cited on pp. 20, 22, 23, 25, 28).

[11] Gartner Inc., *Gartner Identifies Three Megatrends That Will Drive Digital Business Into the Next Decade*, 2017 (Cited on p. 20).

[12] Gartner Inc., *Gartner identifies five emerging technology trends that will blur the lines between human and machine*, 2018 (Cited on p. 20).

[13] Gartner Inc., *Gartner Identifies Five Emerging Technology Trends With Transformational Impact*, 2019 (Cited on p. 20).

[14] Gartner Inc., *The 4 Trends That Prevail on the Gartner Hype Cycle for AI, 2021*, 2021 (Cited on p. 20).

[15] Gartner Inc., *What's New in Artificial Intelligence From the 2023 Gartner Hype Cycle*, 2023 (Cited on p. 20).

[16] M. Grieves, *Virtually Perfect : Driving innovative and lean products through product lifecycle management*. Space Coast Press, 2011, ISBN: 9780982138007 (Cited on p. 22).

[17] M. Grieves, *Digital Twin: Manufacturing Excellence through Virtual Factory Replication*, Florida Institute of Technology, Tech. Rep., 2014, pp. 1–7 (Cited on pp. 22, 36, 37).

[18] S. Haag and R. Anderl, *Digital twin – Proof of concept*, *Manufacturing Letters*, vol. 15, pp. 64–66, Jan. 2018, ISSN: 22138463 (Cited on pp. 22, 26).

[19] National Aeronautics and Space Administration (NASA), *DRAFT Modeling, Simulation, Information Technology and Processing Roadmap*, NASA, Tech. Rep., 2010, p. 32 (Cited on p. 22).

[20] National Aeronautics and Space Administration (NASA), *FINAL Modeling, Simulation, Information Technology and Processing Roadmap*, NASA, Tech. Rep., 2012, p. 38 (Cited on p. 22).

[21] E. H. Glaessgen and D. S. Stargel, *The Digital Twin Paradigm for Future NASA and U.S. Air Force Vehicles*, in *53rd Structures, Structural Dynamics, and Materials Conference*, Apr. 2012 (Cited on pp. 22, 23).

[22] E. Gregersen, *Personal Computer*, *Britannica Online Encyclopedia - Technology*, May 2020 (Cited on p. 22).

[23] C. Legner *et al.*, *Digitalization: Opportunity and Challenge for the Business and Information Systems Engineering Community*, *Business and Information Systems Engineering*, vol. 59, no. 4, pp. 301–308, Aug. 2017, ISSN: 18670202 (Cited on p. 22).

[24] S. Boschert and R. Rosen, *Digital Twin—The Simulation Aspect*, in *Mechatronic Futures: Challenges and Solutions for Mechatronic Systems and Their Designers*, P. Hehenberger and D. Bradley, Eds., Springer, Cham, Jan. 2016, ch. 5, pp. 59–74 (Cited on pp. 23, 26, 27).

[25] F. Tao, Q. Qi, L. Wang, and A. Y. Nee, *Digital Twins and Cyber–Physical Systems toward Smart Manufacturing and Industry 4.0: Correlation and Comparison*, *Engineering*, vol. 5, no. 4, pp. 653–661, Aug. 2019, ISSN: 20958099 (Cited on p. 23).

[26] D. Botkina, M. Hedlind, B. Olsson, J. Henser, and T. Lundholm, *Digital Twin of a Cutting Tool*, in *Procedia CIRP*, vol. 72, Elsevier B.V., 2018, pp. 215–218 (Cited on pp. 23, 26).

[27] R. Rosen, G. Von Wichert, G. Lo, and K. D. Bettenhausen, *About The Importance of Autonomy and Digital Twins for the Future of Manufacturing*, *IFAC-PapersOnLine*, vol. 48, no. 3, pp. 567–572, Jan. 2015, ISSN: 2405-8963 (Cited on p. 23).

[28] F. Tao *et al.*, *Digital twin-driven product design framework*, *International Journal of Production Research*, vol. 57, no. 12, pp. 3935–3953, Jun. 2019, ISSN: 1366588X (Cited on pp. 23, 26).

[29] Y. Wang, X. Wang, and A. Liu, *Digital twin-driven supply chain planning*, in *Procedia CIRP*, vol. 93, Elsevier B.V., 2020, pp. 198–203 (Cited on p. 23).

[30] F. Tao, H. Zhang, A. Liu, and A. Y. Nee, *Digital Twin in Industry: State-of-the-Art*, *IEEE Transactions on Industrial Informatics*, vol. 15, no. 4, pp. 2405–2415, Apr. 2019, ISSN: 15513203 (Cited on pp. 23, 25).

[31] M. Ayani, M. Ganebäck, and A. H. Ng, *Digital Twin: Applying emulation for machine reconditioning*, in *Procedia CIRP*, vol. 72, Elsevier B.V., 2018, pp. 243–248 (Cited on pp. 23, 26).

[32] F. Tao, J. Cheng, Q. Qi, M. Zhang, H. Zhang, and F. Sui, *Digital twin-driven product design, manufacturing and service with big data*, *International Journal of Advanced Manufacturing Technology*, vol. 94, no. 9-12, pp. 3563–3576, Feb. 2018, ISSN: 14333015 (Cited on pp. 23, 26, 28).

[33] E. Negri, L. Fumagalli, and M. Macchi, *A Review of the Roles of Digital Twin in CPS-based Production Systems*, *Procedia Manufacturing*, vol. 11, pp. 939–948, 2017, ISSN: 23519789 (Cited on pp. 23, 25, 28).

[34] B. Vavra, *Digital Twin Becoming a Singular Tool*, Rockwell Automation Inc., Cleveland, Tech. Rep., 2019 (Cited on pp. 25, 26).

[35] Y. Liau, H. Lee, and K. Ryu, *Digital Twin concept for smart injection molding*, *IOP Conference Series: Materials Science and Engineering*, vol. 324, no. 1, Mar. 2018, ISSN: 1757-8981 (Cited on pp. 25, 26).

[36] G. Kube, *The Digital Twin for Business*, SAP (Systems Applications and Products in Data Processing) Community - Technology, Cleveland, Tech. Rep., 2016 (Cited on pp. 25, 26).

[37] J. Lee, E. Lapira, B. Bagheri, and H. a. Kao, *Recent advances and trends in predictive manufacturing systems in big data environment*, *Manufacturing Letters*, vol. 1, no. 1, pp. 38–41, Oct. 2013, ISSN: 2213-8463 (Cited on p. 25).

[38] Y. Bazilevs, X. Deng, A. Korobenko, F. Lanza di Scalea, M. D. Todd, and S. G. Taylor, *Isogeometric Fatigue Damage Prediction in Large-Scale Composite Structures Driven by Dynamic Sensor Data*, *Journal of Applied Mechanics*, vol. 82, no. 9, Sep. 2015, ISSN: 0021-8936 (Cited on p. 25).

[39] Digital Twin Consortium, *Definition of a Digital Twin*, 2020 (Cited on pp. 25, 26).

[40] IEEE EPS, *Modeling and Simulation*, in *Heterogeneous Integration Roadmap*, IEEE Electronics Packaging Society, 2021, ch. 14 (Cited on pp. 25, 26).

[41] U. August, *Digital Twin Technology for More Efficiency*, *ATZproduction worldwide*, Mar. 2019 (Cited on p. 26).

[42] E. Katsoulakis *et al.*, *Digital twins for health - a scoping review*, *Nature npj Digital Medicine*, vol. 7, no. 1, pp. 1–11, Mar. 2024, ISSN: 2398-6352 (Cited on p. 27).

[43] A. Vallée, *Digital twin for healthcare systems*, *Frontiers in Digital Health*, vol. 5, p. 1 253 050, Sep. 2023, ISSN: 2673253X (Cited on p. 27).

[44] A. Harper, *Top Examples of Digital Twins that Can Impress Telecom Providers*, Aug. 2022 (Cited on p. 27).

[45] Digital Twin Consortium, *Leveraging Digital Twins for Virtual-First Planning That Will Connect the Entire Planet*, 2024 (Cited on p. 27).

[46] Nokia, *How digital twins are driving the future of engineering*, 2024 (Cited on p. 27).

[47] A. Macit, *How Digital Twins Transforming Fashion Industry*, Dec. 2023 (Cited on p. 27).

[48] Geniemode, *Revolutionizing the Fashion Industry - The Rise of Digital Twins*, Jul. 2023 (Cited on p. 27).

[49] S. Gibbons, *How digital twins are shaping the fashion industry*, *Just Style magazine*, Mar. 2023 (Cited on p. 27).

[50] S. Sai, A. Rastogi, and V. Chamola, *Digital Twins for Consumer Electronics*, *IEEE Consumer Electronics Magazine*, pp. 1–6, Oct. 2023, ISSN: 21622256 (Cited on p. 27).

[51] P. Oliveira, *Unlocking the Potential of Digital Twin in Electronics Manufacturing*, May 2023 (Cited on p. 27).

[52] H. Omrany, K. M. Al-Obaidi, A. Husain, and A. Ghaffarianhoseini, *Digital Twins in the Construction Industry: A Comprehensive Review of Current Implementations, Enabling Technologies, and Future Directions*, *Sustainability 2023, Vol. 15, Page 10908*, vol. 15, no. 14, p. 10 908, Jul. 2023, ISSN: 2071-1050 (Cited on p. 27).

[53] G. S. Blair, *Digital twins of the natural environment*, *Patterns*, vol. 2, no. 10, p. 100 359, Oct. 2021, ISSN: 2666-3899 (Cited on p. 27).

[54] X. Li *et al.*, *Big Data in Earth system science and progress towards a digital twin*, *Nature Reviews Earth & Environment 2023 4:5*, vol. 4, no. 5, pp. 319–332, May 2023, ISSN: 2662-138X (Cited on p. 27).

[55] W. Purcell and T. Neubauer, *Digital Twins in Agriculture: A State-of-the-art review*, *Smart Agricultural Technology*, vol. 3, p. 100 094, Feb. 2023, ISSN: 2772-3755 (Cited on p. 27).

[56] J. V. do Amaral, C. H. dos Santos, J. A. Montevechi, and A. R. de Queiroz, *Energy Digital Twin applications: A review*, *Renewable and Sustainable Energy Reviews*, vol. 188, p. 113 891, Dec. 2023, ISSN: 1364-0321 (Cited on p. 27).

[57] V. Solovyova, *Digital Twins for Renewable Energy*, 2023 (Cited on p. 27).

[58] E. C. Balta, M. Pease, J. Moyne, K. Barton, and D. M. Tilbury, *Digital Twin-Based Cyber-Attack Detection Framework for Cyber-Physical Manufacturing Systems*, *IEEE Transactions on Automation Science and Engineering*, vol. 21, no. 2, pp. 1695–1712, Apr. 2024, ISSN: 15583783 (Cited on p. 27).

[59] E. Canorea, *Digital Twins and Cybersecurity - Making the most of their power*, Nov. 2023 (Cited on p. 27).

[60] C. Stöcker, M. Rüther, N. Reinhold, and M. Goebel, *Object Marketing using Digital Twins*, 2017 (Cited on p. 27).

[61] K. McCoy, *WTF is Digital Twinning?* 2023 (Cited on p. 27).

[62] Forbes Technology Council, *15 Workplace And Consumer Functions Transformed By Digital Twin Technology*, Oct. 2022 (Cited on p. 27).

[63] i-SCOOP, *Industry 4.0 and the fourth industrial revolution explained*, 2021 (Cited on p. 27).

[64] J. Jasperneite, *Was hinter Begriffen wie Industrie 4.0 steckt - Steuern und Regeln*, 2012 (Cited on p. 27).

[65] S. Sarma, D. L. Brock, and K. Ashton, *The Networked Physical World - Proposals for Engineering the Next Generation of Computing, Commerce & Automatic-Identification*, Massachusetts Institute of Technology (MIT), Cambridge, Tech. Rep., 2000 (Cited on p. 27).

[66] S. Aheleroff, X. Xu, R. Y. Zhong, and Y. Lu, *Digital Twin as a Service (DTaaS) in Industry 4.0: An Architecture Reference Model*, *Advanced Engineering Informatics*, vol. 47, p. 101 225, Jan. 2021, ISSN: 1474-0346 (Cited on pp. 28, 42).

[67] C. Thuemmler and C. Bai, *Health 4.0: How Virtualization and Big Data are Revolutionizing Healthcare*, C. Thuemmler and C. Bai, Eds. Cham: Springer International, Jan. 2017, pp. 1–254, ISBN: 978-3-319-47616-2 (Cited on p. 28).

[68] A. El Saddik, M. Shamim Hossain, and B. Kantarci, *Connected Health in Smart Cities*, A. El Saddik, M. S. Hossain, and B. Kantarci, Eds. Cham: Springer International Publishing, Jan. 2020, pp. 1–254, ISBN: 978-3-030-27843-4 (Cited on p. 28).

[69] G. Trotabas, *The Digital Twin in healthcare: What it is and why it matters*, 2019 (Cited on p. 28).

[70] H. van Houten, *How a virtual heart could save your real one*, 2018 (Cited on p. 28).

[71] ANSYS, *5G Design Innovation Through Simulation*, 2021 (Cited on p. 29).

[72] D. Nazarevich, *Digital Twin in Construction: Benefits, Challenges and Real-World Examples*, 2024 (Cited on p. 29).

[73] V. V. Tuhaise, J. H. M. Tah, and F. H. Abanda, *Technologies for digital twin applications in construction*, *Automation in Construction*, vol. 152, p. 104 931, Aug. 2023, ISSN: 0926-5805 (Cited on p. 29).

[74] K. I. Dale, E. C. D. Pope, A. R. Hopkinson, T. McCaie, and J. A. Lowe, *Environment-Aware Digital Twins: Incorporating Weather and Climate Information to Support Risk-Based Decision-Making*, *Artificial Intelligence for the Earth Systems*, vol. 2, no. 4, Oct. 2023, ISSN: 2769-7525 (Cited on p. 29).

[75] F. Baart, B. Backerberg, and C. Bremmer, *Digital Twins - Promising tools for water and subsurface management*, *Deltares*, 2024 (Cited on p. 29).

[76] C. Verdouw, B. Tekinerdogan, A. Beulens, and S. Wolfert, *Digital twins in smart farming*, *Agricultural Systems*, vol. 189, p. 103 046, Apr. 2021, ISSN: 0308-521X (Cited on p. 29).

[77] M. Escribà-Gelonch, S. Liang, P. van Schalkwyk, I. Fisk, N. V. D. Long, and V. Hessel, *Digital Twins in Agriculture: Orchestration and Applications*, *Journal of Agricultural and Food Chemistry*, vol. 72, no. 19, pp. 10 737–10 752, May 2024, ISSN: 0021-8561 (Cited on p. 29).

[78] T. R. Nachtigall, *Materializing data: craftsmanship and technology for ultra-personalization*, Ph.D. dissertation, Eindhoven University of Technology (TU Delft), Dec. 2019 (Cited on p. 29).

[79] M. Jongeling, *Digital Twin - Privacy and Security*, Nov. 2020 (Cited on p. 29).

[80] J. Clover, *Apple Launches iPhone 11 Display Module Replacement Program*, Dec. 2020 (Cited on p. 30).

[81] L. Tung, *Apple offers free iPhone 11 repair for touch display module problem*, Dec. 2020 (Cited on p. 30).

[82] W. Kritzinger, M. Karner, G. Traar, J. Henjes, and W. Sihn, *Digital Twin in manufacturing: A categorical literature review and classification*, pp. 1016–1022, 2018 (Cited on p. 31).

[83] M. Grieves, *Digital Twins: Past, Present, and Future*, in *The Digital Twin*, N. Crespi, A. T. Drobot, and R. Minerva, Eds., vol. 1, Springer International Publishing, 2023, pp. 97–121, ISBN: 9783031213434 (Cited on p. 34).

[84] F. Tao, M. Zhang, Y. Liu, and A. Y. Nee, *Digital twin driven prognostics and health management for complex equipment*, *CIRP Annals*, vol. 67, no. 1, pp. 169–172, Jan. 2018, ISSN: 17260604 (Cited on pp. 36, 37).

[85] A. Inamdar, M. van Soestbergen, A. Mavinkurve, W. D. van Driel, and G. Q. Zhang, *Modelling thermomechanical degradation of moulded electronic packages using physics-based digital twin*, *Microelectronics Reliability*, vol. 157, p. 115 416, Jun. 2024, ISSN: 00262714 (Cited on p. 42).

[86] A. Inamdar *et al.*, *Characterization of a Piezoresistive Sensor for In-Situ Health Monitoring of Solder Bumps*, in *IEEE 74th Electronic Components and Technology Conference (ECTC) 2024*, 2024 (Cited on p. 42).

[87] A. Inamdar, T. Hauck, M. van Soestbergen, W. D. Driel, and G. Zhang, *ROM-FOM Interface Optimization for Efficient Thermomechanical Simulations of Electronic Components*, in *2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2024*, Institute of Electrical and Electronics Engineers Inc., Apr. 2024, ISBN: 9798350393637 (Cited on p. 42).

[88] W. D. van Driel, M. Y. Mehr, X. J. Fan, and G. Q. Zhang, *Outlook - From Physics of Failure to Physics of Degradation*, in *Reliability of Organic Compounds in Microelectronics and Optoelectronics*, W. D. Van Driel and M. Y. Mehr, Eds., Cham: Springer International Publishing, Jan. 2022, pp. 535–538 (Cited on p. 43).

[89] X. Xu, Y. Lu, B. Vogel-Heuser, and L. Wang, *Industry 4.0 and Industry 5.0 - Inception, conception and perception*, *Journal of Manufacturing Systems*, vol. 61, pp. 530–535, Oct. 2021, ISSN: 0278-6125 (Cited on p. 44).

[90] S. Aheleroff, H. Huang, X. Xu, and R. Y. Zhong, *Toward sustainability and resilience with Industry 4.0 and Industry 5.0*, *Frontiers in Manufacturing Technology*, vol. 2, p. 951 643, Oct. 2022, ISSN: 2813-0359 (Cited on p. 44).

[91] J. Müller, *Enabling Technologies for Industry 5.0*, European Commission, Tech. Rep., Nov. 2020 (Cited on p. 45).

3

Electronics Packaging and Physics-of-Degradation

Electronic components are complex systems consisting of a combination of different materials, which undergo degenerative changes over time following the second law of thermodynamics. The loss of their quality or functionality is reflected in degraded performance or behaviour of electronic components, which can lead to failures during their operational lifetime. Thus, it is crucial to understand the physics of material degradation and the factors causing it to ensure component reliability. This chapter focuses on the physics-of-degradation of packaging materials, which are typically exposed the most to the environmental and operating loads. The content of this chapter is organised into three parts. First, an overview of the packaging technology and encapsulating materials is presented. Then, the most common degradation-causing factors and package-associated failure modes are reviewed. Lastly, the hardware requirements are discussed, including specialised sensors and measurement techniques, in the context of data-driven, compact Digital Twins, for capturing the degradation effects and facilitating component-level health monitoring for microelectronics.

Parts of this chapter have been published in *Frontiers in Electronics* (2025) [1].

3.1. Packaging Technology

Electronic packages have evolved dramatically over the last 50 years, starting from the Dual In-line Package (DIP), Quad Flat Package (QFP), and Small Outline Package (SOP) in the early 1970s; then, the more efficient Lead-less Chip Carrier (LCC), Pin Grid Array (PGA), and Ball Grid Array (BGA) packages in the 1980s to early 1990s; next, the smaller scale packages such as Quad Flat No-leads (QFN) and Chip-Scale Package (CSP) in the late 1990s; later, the multi-die packaging with System in Package (SiP) and Package on Package (PoP) in the 2000s; Wafer-Level Package (WLP) in the late 2000s; and finally, 2.XD (*i.e.*, 2.1D, 2.3D, and 2.5D) and 3D integration in the 2010s and later [2, 3]. In these different electronic components, electronic circuits and sub-components are encapsulated with different materials, such as ceramics, metals, and plastics, to form electronic packages.

The primary function of an electronic package is to protect the internal circuitry from external environmental and operating conditions that can potentially damage it or obstruct its proper functioning. Advanced packaging techniques provide high interconnect density and facilitate multi-layered, multi-functional heterogeneous integration. Thus, modern electronic packages are designed to also support additional functions such as signal transmission via interconnects, shielding electromagnetic interference (*e.g.*, radio frequency applications), electric power distribution, thermal management, and heat dissipation [4, 5].

Several factors govern the performance and characteristics of an electronic package. For instance, the electrical performance is affected by the packaging delay, which depends on the type, complexity, and arrangement of interconnects [6, 7]. Moreover, the thermomechanical behaviour of an electronic package is also highly influenced by the thermal and mechanical properties of the encapsulating material, as it contributes to a large volume-share in a package [8, 9]. Electronics packaging plays an important role in the functionality and lifetime of an electronic assembly. Thus, the selection of an appropriate packaging material is crucial.

3.1.1. Encapsulating Materials

An encapsulating material is required to have chemical stability, hydrophobic nature, thermomechanical properties in a certain suitable range, electrical insulation, thermal stability, and specific dielectric properties [10]. Historically, hermetic packaging with glass, ceramic, or metals (primarily the latter two) was commonly used for housing electronic circuits, making it up to 80% of worldwide microcircuit production in the 1960s. Emerging as an inexpensive alternative in the 1970s, plastic packaging took over virtually all high-volume packaging products, acquiring 97% of the total market share in 1993 and more than 99% by the year 2000. Due to this

large-scale adoption, polymer-based compounds have dominated the packaging market in the last 2 decades [11, ch.1]. Figure 3.1 summarises the timeline of the two competing packaging technologies, with all hermetic packaging materials classified as a single category.

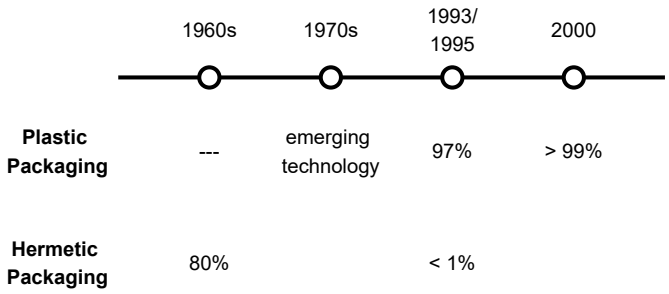


Figure 3.1: The evolution of the per cent (%) market share of packaging materials in the commercial microelectronic devices. Plastic-based packaging became the default for most applications (>99% share) due to its superior electrical performance, achievable thermomechanical behaviour, and lower costs.

Thermosetting polymers such as epoxy, polyimide, bismaleimide-triazine, *etc.* are widely used in packaging materials because of their low dielectric permittivity [12]. Owing to their ability to be moulded, they are also referred to as 'moulding compounds'. Their relatively low cost compared to traditional ceramic packages and also comparable reliability make them a more practical choice for packaging. There is a wide variety of resins suitable for Plastic-Encapsulated Microelectronicss (PEMs) [11, ch.2] [13]. Considering the superior electrical performance, achievable thermal and mechanical behaviour, and economical aspects, the use of epoxy-based plastics is widespread for commercial electronic devices [14].

3.1.2. EPOXY MOULDING COMPOUNDS

A typical Epoxy Moulding Compound (EMC) is a composite material, utilising epoxy resin as a matrix along with a silica-based filler material and other additives. A wide range of thermomechanical properties can be achieved by varying the quantities of the fillers and additives [15, 16]. For example, the glass transition temperature T_g of moulding compounds can be varied from less than 20 °C to greater than 200 °C, whereas the modulus of elasticity E can be changed from 2 GPa for the neat resin to over 100 GPa with continuous fibre reinforcement [17]. Moulding compounds are generally required to have the glass transition temperature greater than the product's service temperature ($T_g > T_s$) for them to remain in the 'glassy' region in order to maintain stable dimensions while the product is in-use [18].

The constitutive materials of an EMC help it attain the desired thermomechanical properties. The epoxy resin contributes to excellent chemical resistance, weight

reduction due to its lower density, as well as high adhesion strength due to the formation of hydroxyl groups during the curing [10, 17]. Typically, an EMC has a very high filler content (up to 90%), which helps reduce the Coefficient of Thermal Expansion (CTE) and increase the thermal conductivity of the moulding compound [11, ch.2]. It also improves dimensional stability with the resulting low shrinkage and high T_g values. Figure 3.2 shows a cross-section of an EMC specimen observed under a Scanning Electron Microscope (SEM), where a very high content of silica filler can be clearly observed.

The silica-based filler (primarily SiO_2) also ensures the reduction of moisture absorption [19] and of the large CTE-mismatch between silicon die (2–3 ppm/°C) and epoxy resin (above 80 ppm/°C), ensuring less warpage [20]. The SiO_2 content and the particle size of the silica-based filler material control the viscosity, and therefore, the flowability of the moulding compound can be adjusted. Hardeners improve the heat resistance and storage stability; cure-promoter increases the cross-linking reaction time; and flame-retardants lower the risk of flammability [21].

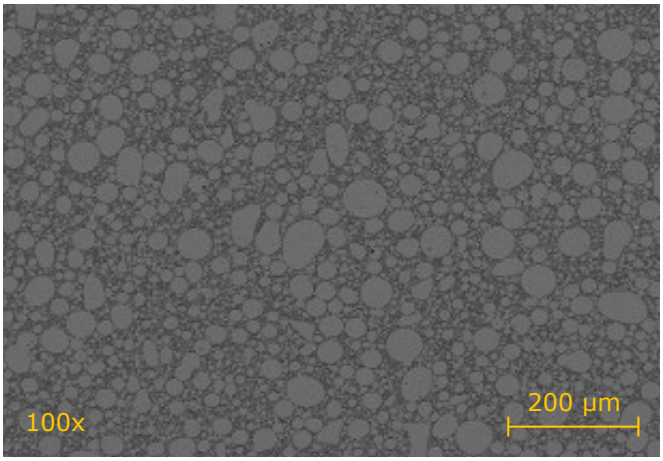


Figure 3.2: A cross section of an EMC specimen observed under a SEM. The light grey region indicates the SiO_2 filler (up to 90% of the total volume) and the surrounding black region is the polymer matrix.

3.2. Package-Associated Degradation

The encapsulating material occupies a large volume within a package (as high as 75% [22]) and, thus, is the most dominant in governing the overall thermomechanical behaviour of a package. It is not only true for simple single-chip packages but also for complex multi-chip packages such as PoP, SiP, and 3D integration. Figure 3.3 illustrates several options for modern electronics packaging. In all of the examples, a high volume-share of the encapsulating material is observed.

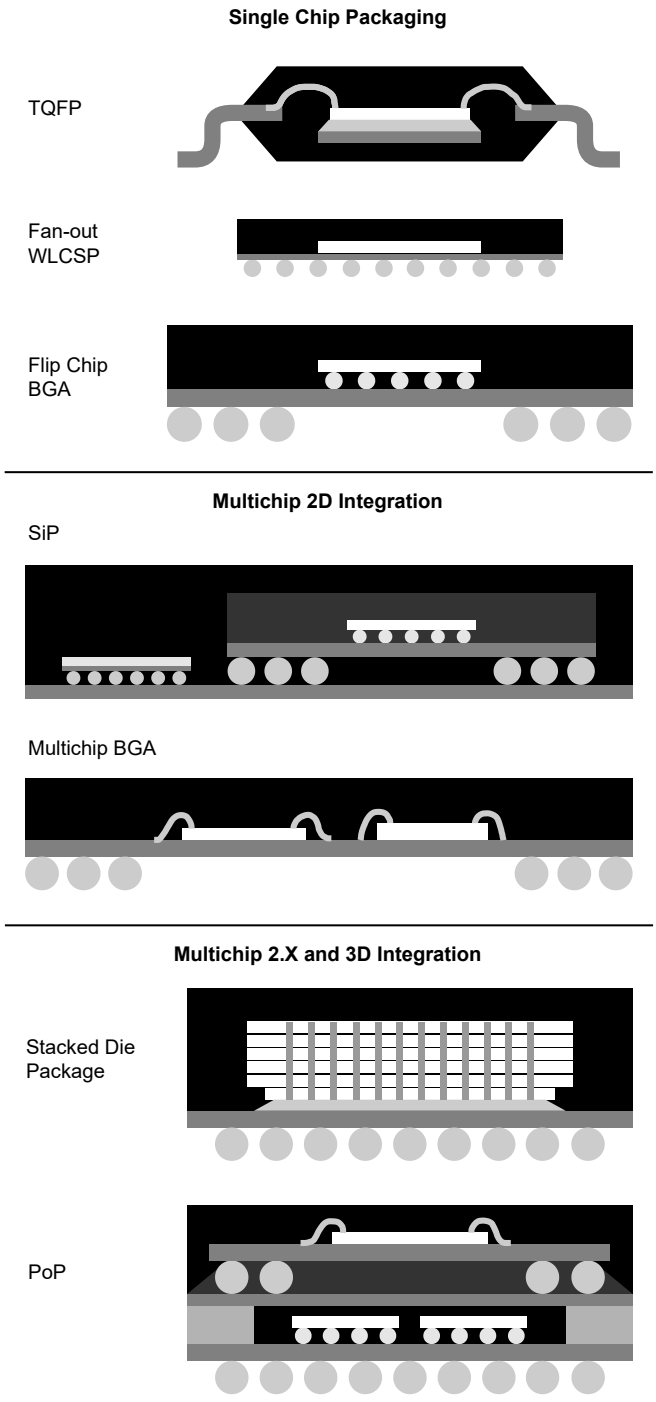


Figure 3.3: A schematic representation of different options for electronic packages, classified into three categories – single-chip packages, multi-chip 2D integration, and advanced 2.X and 3D integration. All options indicate the encapsulating material in black colour, which also has a dominant volume-share.

This trend is seen throughout the history of electronics packaging (1970s–2000s) and also the advancements in the recent past, reviewed in numerous publications [2, 3, 5, 11, 22–25]. Although most Wafer-Level Chip-Scale Packages (WLCSPs) do not have a plastic encapsulation [26, 27], such WLCSPs get encapsulated after being integrated into a larger system (*e.g.*, a SiP). This is illustrated in Figure 3.3 with a Fan-in WLCSP on the left-hand side portion of the indicated SiP. Thus, the encapsulation material is a dominant part of an electronic package. It is exposed the most to the surrounding environment and, thus, is prone to degradation and ageing.

3.2.1. Degradation Factors

The factors responsible for component degradation can either be 'environmental' or 'functional' loads. The former depends on aspects such as the geographic location, season, and time of the day, while the latter on the application field and operating conditions such as the power requirement, runtime, *etc.* These factors can be categorised into eight types – thermal, electrical, mechanical, chemical, electromagnetic, radiation, humidity, and dust [28]. Among these, harsh conditions such as high temperature, moisture, and mechanical vibrations have the most relevance for electronic components in a broad variety of applications. Exposure to these 'stress-factors' alters the thermal, mechanical, electrical, and chemical behaviour of the constituting materials, which influences the performance, behaviour, and lifetime of an electronic component. Figure 3.4 indicates the distribution of the share of four major 'stress-factors' in causing failures in electronic components [1].

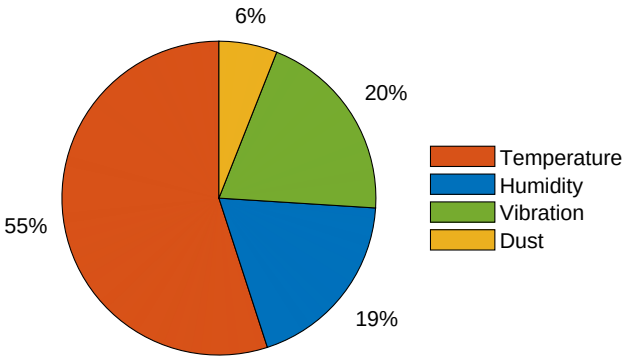


Figure 3.4: Four key 'stress-factors' responsible for causing failures in electronic components – temperature, humidity, vibration, and dust. The pie chart indicates the percentage share of each factor [29–32].

[1] The data originates from a 1990 study by the US Air Force Avionics Integrity Program, which has later been reported on in handbooks such as [29] and a variety of publications on the studies of different failure modes in electronics packages [30–32].

Temperature is the most significant stress-factor (accounting for more than 50%) to facilitate failure mechanisms in electronic components, while humidity and mechanical vibrations are the next two dominant ones. Failure mechanisms are also often accelerated by these factors, and thus, the knowledge of the exposure of an electronic component to the dominant stress-factors is crucial in determining its current state of degradation and predicting a potential failure mode.

3.2.2. FAILURE MODES

Package-level degradation mechanisms can lead to both package-level failures as well as board-level failures. Figure 3.5 shows the distribution of different types of package-level and board-level failure modes associated with power electronic systems [2]. The package-associated failure modes — semiconductors (die), connectors (interconnects), and solder joints — together account for a significant share of 37%. In general, there can be a large number of failure modes for an electronic component or system [11, ch.5]. Thus, a selection is necessary to focus the efforts on modelling the physics-of-degradation and building a Digital Twin. The following three criteria were considered to determine the failure modes and degradation mechanisms of interest: (1) the three dominating stress-factors (*viz.*, temperature, humidity, and vibration); (2) the large volume-share of the encapsulation material with a dominant role in the thermomechanical behaviour of a package; and (3) the trend of commonly observed categories of package-associated failures.

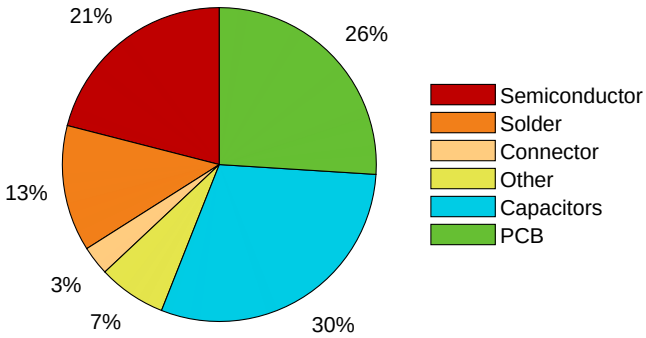
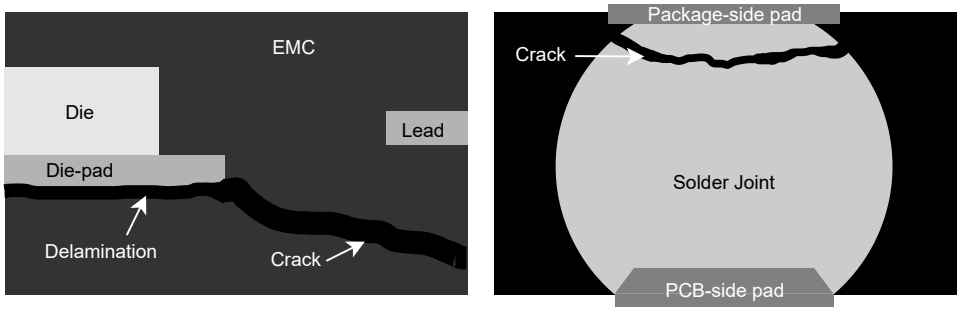


Figure 3.5: The distribution of failure modes associated with different sub-components of power electronic systems based on the data presented in [33–35]. The failures related to the semiconductor (die), connector (interconnects), and solder joints together account for over a third of total failure modes.

Delamination (*i.e.*, the separation of two heterogeneous surfaces) and fracture (*i.e.*, cracking) of materials are two of the most common mechanical failure mechanisms.

[2]The original source [33] is not accessible, but the data were later reproduced in [34, 35])

Delamination is often observed at the interfaces between the moulding compound and other materials, such as EMC-leadframe, EMC-die, *etc.* Delamination can also lead to crack propagation in the bulk of EMC. Figure 3.6(a) shows the schematics of these failure modes, which are mainly caused by the difference between the thermomechanical properties (*e.g.*, CTE-mismatch) and temperature gradient between different layers. A cyclic thermal load during the component's operation causes stress cycling, which leads to crack initiation and propagation. Delamination can affect not only the electrical performance but also the thermal performance by altering the heat distribution and flow within the package [36].



(a) EMC–Die-pad delamination and bulk-EMC crack propogation

(b) Bulk-solder crack propogation (Mode-II)

Figure 3.6: Examples of package-associated failure modes – (a) delamination of EMC-leadframe interface and cracking of bulk-EMC and (b) crack propagation in the bulk of a solder joint. Both failure modes are initiated by fatigue load and accelerated by thermomechanical degradation of EMC.

A cyclic thermal or mechanical load is also a primary cause of crack initiation and propagation within solder joints. Figure 3.6(b) depicts a crack in the bulk of solder material, which is also referred to as a Mode-II failure. Solder cracks can also develop within the intermetallic layer formed up to a certain depth from its contact with the metallisation (commonly copper) layer. This is called a Mode-I failure. The former is a predominantly ductile failure due to plastic deformation (*i.e.*, the accumulated plastic strain), while the latter is a brittle failure. A mixed-mode failure can also be observed in solder joints. Both of the described failure modes (illustrated in Figure 3.6 [3]) have one common factor, which is that they occur during product operation, *i.e.*, the in-use phase of an electronic component. Moreover, they can be accelerated by the changed thermomechanical behaviour of a package due to the ageing of the encapsulating EMC. Thus, the changes in material properties of the encapsulating material are of great significance when considering the effects of package-level degradation on the component-level failure modes.

[3]The schematics are recreated based on figures presented in [37] and [38].

3.3. Hardware for Degradation Monitoring

Product-specific health monitoring and reliability prediction can be achieved when its exposure to the dominant stress-factors is known, which can be used to determine the current state of degradation. This requires incorporating embedded sensors and component-level measurement techniques in an electronic system. Thus, certain hardware considerations are necessary to realise the data-driven branch of the Digital Twin architecture (Figure 2.8), especially the edge-processing aspect, and to establish the data flow between the physical product and its digital models in the virtual space. This is important for the 'instance' (DTI) and crucial for the 'aggregate' (DTA) phase of the Digital Twin. The hardware requirements are categorised into sensing and processing units.

3.3.1. Sensors and Measurements

A set of sensors to measure temperature at various locations of a component, moisture content in the surroundings, and certain aspects of mechanical vibrations is the basic necessity. Multiple locations to measure the temperature are recommended. A measurement outside a package records the environmental (*i.e.,* external temperature), while the ones within a component can measure the effects of joule heating due to the active power cycling. Moreover, a failure mode such as delamination could also be monitored as it affects the heat distribution. An example of temperature sensor-based prediction of the EMC-die delamination has been presented in the *COMPAS* project [39]. A temperature sensor also helps in estimating the stresses when it is linked with a physics-based model, such as a Finite Element model. Additional analogue sensors and external thermocouples can also serve to monitor the temperature at a specific location.

Moisture diffusion into EMC affects the mechanical behaviour of the encapsulation layer and, in turn, of the whole package [40]. Relative humidity (%RH) measurements aided by an atmospheric pressure sensor can help quantify these effects. Humidity and temperature both affect the thermomechanical properties of EMC. Thermal ageing produces permanent oxidative changes, whereas the effects of moisture diffusion are reversible to a certain extent [41]. Thus, real-time and accurate humidity measurements are crucial to accumulate the effects of moisture-induced changes in the mechanical behaviour of an electronic package.

Mechanical vibrations impose a dynamic operating load on electronics in the automotive and manufacturing fields. It causes stress cycling, leading to fatigue failures such as delamination and cracking due to cumulative damage of the EMC-die interface (package-level) and solder fatigue due to accumulated plastic strains (board-level). Linear motion is sensed by a 3-axis accelerometer, while the angular

motion is captured by a 3-axis gyroscope. A standard 6-axis Inertial Measurement Unit (IMU) (or 9-axis IMU, which includes a 3-axis magnetometer for the orientation in space) should be integrated at one or more strategic locations to record the vibrational load at the component- or board-level.

Apart from the individual effects of the stress-factors, it is also crucial to see the effect of coupled loading because such loads represent a more realistic scenario and generally have a greater influence on the acceleration of failure modes. Several publications indicate this by studying the effect of coupling temperature-humidity [42–44] and temperature-vibrations [38, 45]. Some ageing and degradation processes can have much longer characteristic times than the operation times of the device [46, ch.3]. Thus, the frequency of measurements should be tweaked according to the target failure mechanisms and the involved physics-of-degradation.

In addition to capturing the effects of the dominant stress-factors, specialised sensors and measurement methods can be implemented to get additional information about the state of degradation. For instance, electrical resistance measurements can identify a failed solder joint and also a few degraded stages before failure [47, ch.4], as well as the effects such as electromigration. Measurements from a piezoresistive sensor can represent the changes in stresses and indicate the progress of degradation or damage [48–50].

3.3.2. Processing and Communication

Data collection through sensors requires an on-board control unit, which a Microcontroller Unit (MCU) along with a multiplexer (or 'mux') can fulfil. The MCU needs to be selected so that some data processing can be done on the edge. The advantages of this are twofold – (1) high-quality data can be directly processed without it leaving the device, and only the inference can be stored or transmitted. This is also a more secure option with respect to data privacy; and (2) it simplifies the workflow while saving a lot of energy by avoiding at least a part of the data stream transmissions, which inherently has high energy consumption [51, 52].

ARM-based architecture for processors is known for its energy efficiency, and it also provides a wide variety of high and low-power compute cores. Their 'M' series of designs has limited compute power compared to the 'A' series, but are energy efficient, making them suitable for the DTA application. *ARM* recommends several tiers of processing units (xPUs) for data processing across different use cases [53]. A DTA implementation requires making sense of the data coming from different sensors or multiple of the same kind (*i.e.*, sensor fusion) and having embedded-ML capabilities such as feature extraction, failure classification, and anomaly detection. Thus, at the least, *Cortex* M7 or equivalent compute architecture should be selected.

Since the computational power available at the edge MCU has its limitations, some sorts of data analysis (*e.g.*, federated learning) can only be done on an external system, *i.e.*, on the cloud. This can be achieved by wireless communication interfaces such as WiFi and Bluetooth Low Energy (BLE). Wireless connectivity is also paramount for maintaining a continuous feed of sensor data to continuously update the physics-based model in the cloud. For transmitting data to a locally available but external computation infrastructure (*e.g.*, within a car), connections for wired communication channels such as the Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I2C) should be available on the board-level. A Universal Serial Bus (USB) interface or a dedicated port might also be necessary for standardised data transfer as well as software or firmware updates. Finally, flash memory solutions can be considered for the local storage of processed data and inferences.

Predicting failures directly from the collected sensor data is not possible without a robust (purely) data-driven model, which typically requires huge amounts of training data gathered from experiments or in-field use of the product. The hybrid Digital Twin approach can address this challenge, and thus, linking the sensor data to the physics-based models is necessary. Experimentally validated models can then also serve as a source for training data that is convenient and not as resource-intensive as a purely experimental approach. Moreover, these models can extract results from intricate places of an electronic component, serving as 'virtual sensors', where placing a physical sensor or performing actual measurements is either not possible or isn't practical. Therefore, in conjunction with the hardware requirements, Digital Twins with compact degradation models should be utilised.

3.3.3. Test-Board Reference Design

A reference design for a test-board was created considering the requirements stated in the previous subsections. Sensors and other peripheral electronic components were selected according to the recommendations in automotive electronics standards, such as AEC Q100 (by Automotive Electronics Council) and ISO 16750-4 (by International Organisation for Standardisation) [54, 55], to ensure compatibility with experiments representing harsh environments. The preferred rated operating temperature range for all sensors was kept at −40 °C to 125 °C. However, some of the components (such as the USB connector and MCU) are rated for a slightly shorter range, *i.e.*, −40 °C to 105 °C and thus cannot be used for high-temperature accelerated tests. Therefore, for these conditions, the board includes additional capability for power supply and data transfer using compatible wired connectors.

Figure 3.7 indicates the reference design of the test-board for DTA application. A footprint in the centre of the test-board is reserved for test-packages, as indicated in the layout. Some of the test-packages are active, which means each of them would

include a piezoresistive sensor. The board is designed to accommodate both QFN and WLCSP packages. To utilise the board for mechanical vibrations and shock (drop) testing, its size is set to 132 mm × 77 mm following the JEDEC standard by Joint Electron Device Engineering Council [56].

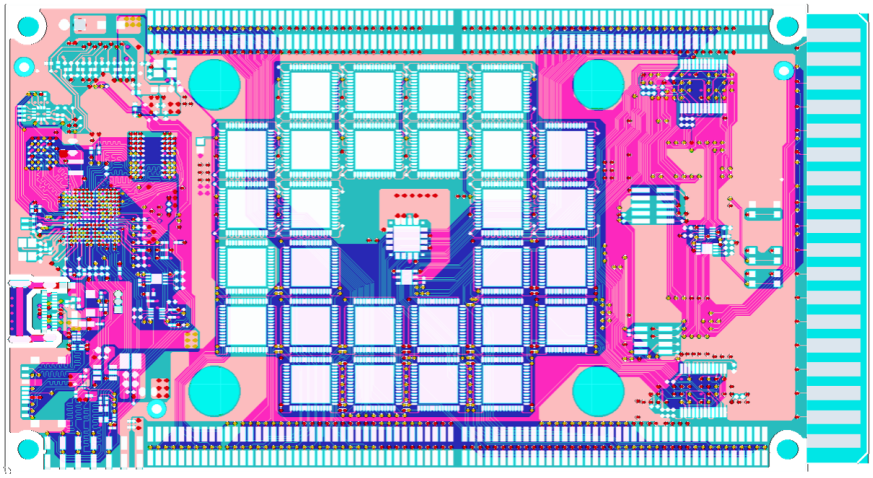


Figure 3.7: A reference design of a Digital Twin test-board, which includes sensors to capture the exposure of dominant stress-factors (*viz.*, temperature, humidity, mechanical vibrations) as well as additional measurement techniques such as resistance measurement and embedded piezoresistive sensors.

The reference design was prepared with the help of circuit-design standards and norms. It is based on an existing commercially available sensor-board, which comes with components on both sides. The new design was simplified to accommodate all sensors and test-packages on one side of the board. All unnecessary components were removed, and some of the existing sensors were replaced with the ones qualifying the temperature range of −40 °C to 125 °C mentioned in the aforementioned automotive standards. Replacement sensors were carefully chosen to meet this criterion and, simultaneously, to have the required accuracy and range. The list of sensors and components, along with their specifications, is included in Appendix A.

Conclusion

This chapter reviews the state of the art of electronics packaging and materials used for encapsulation. It shows that electronic packages have become more and more complex, and over 99% of commercial electronics utilise plastic encapsulation with epoxy-based moulding compounds being a popular choice. The encapsulation layer retains a dominant volume-share in several types of conventional or advanced packages and, thus, is a critical layer when package-level degradation and associated

mechanical failure modes are concerned. Exposure to temperature, moisture, and mechanical vibrations influences the package-associated failure mechanisms. Thus, delamination and solder fatigue are identified as the two failure modes of interest.

Dominant stress-factors have their individual effects on material degradation that lead to the acceleration of failure modes. However, it is also crucial to study the coupled effects, as they represent more realistic loading conditions. Thus, multi-physics superposition is necessary when preparing a physics-based Digital Twin model (*i.e.*, a DTI). In addition, a set of sensors and measurement techniques should be in place to achieve component-level continuous and in-situ condition monitoring. The advantages are twofold – (1) it can be utilised to update the physics-based model in the cloud to represent the current state of degradation, and (2) the data can be processed in-situ using sensor fusion and ML for quantification of degradation parameters, failure detection, and classification of failure modes.

The additional hardware required to realise a DTA for in-situ component-level health monitoring can be categorised into sensing and processing units. The selection of suitable computing hardware, such as an MCU, depends on the required computational power and the necessary energy efficiency at the edge. Apart from the sensors for measuring the basic environmental loads, the inclusion of additional specialised sensors, such as a piezoresistive sensor, provides more insights into the progressive degradation of electronic components. In addition to the hardware sensors, Digital Twin-based 'virtual sensors' serve as a more practical solution for gathering data. Thus, experimentally validated physics-based degradation models are a crucial aspect in realising a hybrid approach to component-level PHM of electronics.

References

[1] A. Inamdar, W. D. Van Driel, and G. Zhang, *Electronics packaging materials and component-level degradation monitoring*, *Frontiers in Electronics*, vol. 6, p. 1 506 112, Jan. 2025, ISSN: 2673-5857 (Cited on p. 53).

[2] J. H. Lau, *Semiconductor Advanced Packaging*. Singapore: Springer Singapore, 2021, ISBN: 978-981-16-1375-3 (Cited on pp. 54, 58).

[3] AnySilicon, *Semiconductor Packaging History and Trends*, 2011 (Cited on pp. 54, 58).

[4] National Research Council (US), *Materials for high-density electronic packaging and interconnection*. National Academy Press, 1990, p. 139, ISBN: 9780309042338 (Cited on p. 54).

[5] A. Lancaster and M. Keswani, *Integrated circuit packaging review with an emphasis on 3D packaging*, *Integration*, vol. 60, pp. 204–212, Jan. 2018, ISSN: 0167-9260 (Cited on pp. 54, 58).

[6] D. Edwards, *Package Interconnects Can Make Or Break Performance*, *Electronic Design*, Sep. 2012 (Cited on p. 54).

[7] M. Lapedus, *Interconnect Challenges Rising*, *Semiconductor Engineering*, Jun. 2016 (Cited on p. 54).

[8] S. P. Phansalkar, C. Kim, and B. Han, *Effect of critical properties of epoxy molding compound on warpage prediction: A critical review*, *Microelectronics Reliability*, vol. 130, p. 114 480, Mar. 2022, ISSN: 0026-2714 (Cited on p. 54).

[9] T. Wei, Z. Fang, C. Xingming, D. Dong, and W. Juan, *The warpage control method in epoxy molding compound*, in *2009 International Conference on Electronic Packaging Technology and High Density Packaging, ICEPT-HDP 2009*, 2009, pp. 722–724, ISBN: 9781424446599 (Cited on p. 54).

[10] T. Na, H. Jiang, X. Liu, and C. Zhao, *Preparation and properties of novel fluorinated epoxy resins cured with 4-trifluoromethyl phenylbenzimidazole for application in electronic materials*, *European Polymer Journal*, vol. 100, pp. 96–102, Mar. 2018, ISSN: 0014-3057 (Cited on pp. 54, 56).

[11] H. Ardebili, Jiawei Zhang, and M. G. Pecht, *Encapsulation Technologies for Electronic Applications*, Second. Elsevier, 2018, pp. 1–498, ISBN: 9780128119785 (Cited on pp. 55, 56, 58, 59).

[12] R. Li *et al.*, *Review on polymer composites with high thermal conductivity and low dielectric properties for electronic packaging*, *Materials Today Physics*, vol. 22, p. 100 594, Jan. 2022, ISSN: 2542-5293 (Cited on p. 55).

[13] H. K. Charles, *Materials in Electronic Packaging at APL*, *Johns Hopkins APL Technical Digest*, vol. 14, no. 1, 1993 (Cited on p. 55).

[14] M. G. Pecht, R. Agarwal, P. McCluskey, T. Dishongh, S. Javadpour, and R. Mahajan, *Electronic Packaging Materials and Their Properties*, 1st ed. CRC Press LLC, 1999, ISBN: 0-8493-9625-5 (Cited on p. 55).

[15] D. Carolan, A. Ivankovic, A. J. Kinloch, S. Sprenger, and A. C. Taylor, *Toughening of epoxy-based hybrid nanocomposites*, *Polymer*, vol. 97, pp. 179–190, Aug. 2016, ISSN: 0032-3861 (Cited on p. 55).

[16] B. K. Kandola, B. Biswas, D. Price, and A. R. Horrocks, *Studies on the effect of different levels of toughener and flame retardants on thermal stability of epoxy resin*, *Polymer Degradation and Stability*, vol. 95, no. 2, pp. 144–152, Feb. 2010, ISSN: 0141-3910 (Cited on p. 55).

[17] M. J. Mullins, D. Liu, and H. J. Sue, *Mechanical Properties of Thermosets*, in *Thermosets: Structure, Properties and Applications*, Q. Guo, Ed., Woodhead Publishing, 2012, ch. 2, pp. 28–61, ISBN: 9780857090867 (Cited on pp. 55, 56).

[18] D. Ratna, *Thermal Properties of Thermosets*, in *Thermosets: Structure, Properties and Applications*, Q. Guo, Ed., Woodhead Publishing, 2012, ch. 3, pp. 62–91, ISBN: 9780857090867 (Cited on p. 55).

[19] H. Sasajima *et al.*, *New development trend of epoxy molding compound for encapsulating semiconductor chips*, in *Materials for Advanced Packaging, Second Edition*, D. Lu and C. Wong, Eds., Springer International Publishing, 2016, pp. 373–419, ISBN: 9783319450988 (Cited on p. 56).

[20] P. L. Teh, M. Mariatti, H. M. Akil, K. N. Seetharamu, A. N. Wagiman, and K. S. Beh, *High filled epoxy composites for electronic packaging application*, in *Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium*, 2006, pp. 275–281, ISBN: 142440729X (Cited on p. 56).

[21] M. Linec and B. Mušič, *The Effects of Silica-Based Fillers on the Properties of Epoxy Molding Compounds*, *Materials 2019, Vol. 12, Page 1811*, vol. 12, no. 11, p. 1811, Jun. 2019, ISSN: 1996-1944 (Cited on p. 56).

[22] Y. Liu, *Power Electronic Packaging*. Springer New York, 2012 (Cited on pp. 56, 58).

[23] W. J. Greig, *Integrated Circuit Packaging, Assembly and Interconnections*. Boston, MA: Springer US, 2007, pp. 1–296, ISBN: 978-0-387-28153-7 (Cited on p. 58).

[24] D. Zhang and J. J. Lu, *3D integration technologies: An overview*, in *Materials for Advanced Packaging, Second Edition*, D. Lu and C. P. Wong, Eds., Springer International Publishing, 2016, pp. 1–26, ISBN: 9783319450988 (Cited on p. 58).

[25] E. Perfecto and K. Srivastava, *Technology trends: Past, present, and future*, in *Advanced Flip Chip Packaging*, H.-M. Tong, Y.-S. Lai, and C. Wong, Eds., 1st ed., vol. 9781441957, Springer US, 2013, ch. 2, pp. 23–52, ISBN: 9781441957689 (Cited on p. 58).

[26] NXP Semiconductor, *Wafer Level Chip Scale Package (WLCSP) - Application Note*, NXP Semiconductor, Tech. Rep., Aug. 2015 (Cited on p. 58).

[27] S. Qu and Y. Liu, *Wafer-Level Chip-Scale Packaging*. New York, NY: Springer New York, 2015, pp. 1–322, ISBN: 978-1-4939-1555-2 (Cited on p. 58).

[28] ZVEI, *Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications*, ZVEI German Electro and Digital Industry Association, Tech. Rep., 2015 (Cited on p. 58).

[29] M. Pecht, *Handbook of Electronic Package Design*. 1991 (Cited on p. 58).

[30] R. C. Chu, R. E. Simons, M. Iyengar, and L.-T. Yeh, *Thermal Management of Flip Chip Packages*, in *Advanced Flip Chip Packaging*, Tong Ho-Ming, Lai Yi-Shao, and Wong C.P., Eds., vol. 9781441957, Springer, Boston, MA, Aug. 2013, ch. 9, pp. 413–469 (Cited on p. 58).

[31] Y. Xu, H. Chen, Z. Hu, and D. Li, *Influence of Relative Humidity on the Temperature Increase of a Power Converter*, *Journal of Power Electronics*, vol. 15, no. 3, pp. 841–848, Jan. 2015, ISSN: 1598-2092 (Cited on p. 58).

[32] B. Qiu *et al.*, *Survey on Fatigue Life Prediction of BGA Solder Joints*, *Electronics*, vol. 11, no. 4, p. 542, Feb. 2022, ISSN: 2079-9292 (Cited on p. 58).

[33] E. Wolfgang, *Examples for failures in power electronics systems*, in *ECPE Tutorial on Reliability of Power Electronic Systems*, European Center for Power Electronics (ECPE), 2007, pp. - (Cited on p. 59).

[34] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, *Condition monitoring for device reliability in power electronic converters: A review*, *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734–2752, 2010, ISSN: 08858993 (Cited on p. 59).

[35] H. Wang, K. Ma, and F. Blaabjerg, *Design for reliability of power electronic systems*, in *IECON Proceedings (Industrial Electronics Conference)*, 2012, pp. 33–44, ISBN: 9781467324212 (Cited on p. 59).

[36] J. Nieuwenkamp and A. Bosco, *Selection of failure mode and mechanism for Digital Twin (Deliverable 1.4 of COMPAS project)*, Tech. Rep., 2021 (Cited on p. 60).

[37] Y. Ju, M. Saka, and H. Abé, *Detection of delamination in IC packages using the phase of microwaves*, *NDT & E International*, vol. 34, no. 1, pp. 49–56, Jan. 2001, ISSN: 0963-8695 (Cited on p. 60).

[38] T. An, C. Fang, F. Qin, H. Li, T. Tang, and P. Chen, *Failure study of Sn37Pb PBGA solder joints using temperature cycling, random vibration and combined temperature cycling and random vibration tests*, *Microelectronics Reliability*, vol. 91, pp. 213–226, Dec. 2018, ISSN: 0026-2714 (Cited on pp. 60, 62).

[39] J. Nieuwenkamp, K. Reinders, H. Wisselink, M. Niessner, M. van Soestbergen, and J. Mendez, *Digital Twin-driven prognostics of lifetime accuracy (Deliverable 3.3 of COMPAS project)*, Tech. Rep., 2023 (Cited on p. 61).

[40] S. Sugiman, I. K. P. Putra, and P. D. Setyawan, *Effects of the media and ageing condition on the tensile properties and fracture toughness of epoxy resin*, *Polymer Degradation and Stability*, vol. 134, pp. 311–321, Dec. 2016, ISSN: 0141-3910 (Cited on p. 61).

[41] K. Netting, *Thermosets for electrical applications*, in *Thermosets: Structure, Properties and Applications*, Q. Guo, Ed., Woodhead Publishing, 2012, pp. 289–303, ISBN: 9780857090867 (Cited on p. 61).

[42] C. K. Wang and M. L. Wu, *Simulation and Analysis of Quad Flat No-lead Package (QFN) under Moisture, and Thermal Stress*, *InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM*, vol. 2020-July, pp. 1165–1169, Jul. 2020, ISSN: 19363958 (Cited on p. 62).

[43] K. M. Jansen, M. F. Zhang, L. J. Ernst, D. K. Vu, and L. Weiss, *Effect of temperature and humidity on moisture diffusion in an epoxy moulding compound material*, *Microelectronics Reliability*, vol. 107, p. 113 596, Apr. 2020, ISSN: 0026-2714 (Cited on p. 62).

[44] K. Zulueta, A. Burgoa, and I. Martínez, *Effects of hygrothermal aging on the thermomechanical properties of a carbon fiber reinforced epoxy sheet molding compound: An experimental research*, *Journal of Applied Polymer Science*, vol. 138, no. 11, Mar. 2021, ISSN: 10974628 (Cited on p. 62).

[45] F. Arabi, A. Gracia, J. Y. Delétage, and H. Frémont, *Effect of thermal and vibrational combined ageing on QFN terminal pads solder reliability*, *Microelectronics Reliability*, vol. 114, p. 113 883, Nov. 2020, ISSN: 0026-2714 (Cited on p. 62).

[46] J. Swingler and A. Feinberg, Eds., *The Physics of Degradation in Engineered Materials and Devices: Fundamentals and Principles*. Momentum Press, Dec. 2014, ISBN: 9781606504673 (Cited on p. 62).

[47] L. Zhang, *Characterization of Solder Joint Degradation under Board-level Reliability Tests for Vibration and Thermal Cycling*, Delft University of Technology, Tech. Rep., 2023 (Cited on p. 62).

[48] A. Prisacaru, P. J. Gromala, B. Han, and G. Q. Zhang, *Degradation Estimation and Prediction of Electronic Packages using Data Driven Approach*, *IEEE Transactions on Industrial Electronics*, 2021, ISSN: 15579948 (Cited on p. 62).

[49] A. Prisacaru and P. J. Gromala, *Aging of the Molding Compound Identification using Piezoresistive Silicon Based Stress Sensor*, in *2021 22nd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2021*, Institute of Electrical and Electronics Engineers Inc., Apr. 2021, ISBN: 9781665413732 (Cited on p. 62).

[50] A. Inamdar *et al.*, *Characterization of a Piezoresistive Sensor for In-Situ Health Monitoring of Solder Bumps*, in *IEEE 74th Electronic Components and Technology Conference (ECTC) 2024*, 2024 (Cited on p. 62).

[51] P. Warden and D. Situnayake, *TinyML: Machine Learning with TensorFlow Lite on Arduino and ultra-low-power microcontrollers*. O'Reilly, 2019, ISBN: 9781492052043 (Cited on p. 62).

[52] Edge Impulse, *Imagine 2021: Innovation Keynotes (Conference by Edge Impulse)*, Sep. 2021 (Cited on p. 62).

[53] D. Vachani, *AI for IoT: Opening up the Last Frontier*, Feb. 2020 (Cited on p. 62).

[54] Automotive Electronics Council, *AEC-Q100-Rev-H Failure Mechanism based Stress Test Qualification for Integrated Circuits*, 2014 (Cited on p. 63).

[55] International Organization for Standardization, *ISO 16750-4:2010(en) Road vehicles — Environmental conditions and testing for electrical and electronic equipment — Part 4: Climatic loads*, 2010 (Cited on p. 63).

[56] Joint Electron Device Engineering Council, *JEDEC JESD22-B111A Board level Drop Test Method of Components for Handheld Electronic Products*, 2016 (Cited on p. 64).

4

Digital Twin Instance for Thermomechanical Ageing

*Semiconductor devices are commonly encapsulated with Epoxy Moulding Compounds (EMC) to form an electronic package. EMC typically occupies a large volume-share within a package and, thus, governs its overall thermomechanical behaviour. When exposed to high temperatures (*150 °C *and above), electronic packages predominantly show oxidation of the outer layer of EMC. Oxidised EMC exhibits notably different material properties, resulting in a modified pattern of mechanical deformation for a thermally aged package under varying thermal loads. As the oxidation layer grows in thickness, its mechanical properties also evolve, indicating distinct phases of the oxidised material at different stages of thermal ageing. Reflecting these changes (i.e., the current state of degradation) into a Finite Element (FE) model-based analysis can provide better insights into failure prediction and component reliability. It requires updating the geometry and material behaviour as a function of ageing. This chapter presents a systematic procedure to build a continuously updated physics-based Digital Twin Instance (DTI) of a thermally aged flip-chip package that can represent intermediate oxidation stages. The developed Digital Twin is utilised for an FE analysis to study the change in the trend of out-of-plane package deformations and die-level stresses as a function of several stages of EMC oxidation.*

Parts of this chapter have been published in *Microelectronics Reliability* (2024) [1], in *Frontiers in Electronics* (2025) [2], and in the proceedings of *IEEE EuroSimE Conference* (2023) [3].

4.1. Introduction

Electronic devices and components are being utilised in an increasing number of application fields such as manufacturing, automotive, and healthcare [4–6]. In some applications, electronic components are exposed to harsh environments such as elevated temperatures. To cover these application environments, the Automotive Electronic Council (AEC) defines standard qualification tests involving temperature variation between −40 °C and 125 °C, mechanical vibrations with a peak acceleration of 50 g, and humid environments up to 85% RH [7]. Under the operating loads, the constituent materials of an electronic component undergo degenerative changes over time, which are typically accelerated under harsh environmental conditions. The term *physics-of-degradation* encompasses the study of degradation mechanisms. It is closely linked with *physics-of-failure* since degradation can eventually lead to component failure. Thus, the reliability of an electronic device is directly linked to the degenerative changes in its constituent materials.

Material degradation can be associated with one or more of the following five key domains: mechanical, thermal, chemical, electrical, and biological degradation. Among the dominant environmental loads (*viz.*, temperature, vibrations, humidity, and dust), exposure to high temperatures is one of the biggest contributing factors for failures in electronic components [8]. To protect the electronic circuits from their environment, they are commonly encapsulated with thermosetting materials using a moulding process. Epoxy-based Moulding Compounds (EMC) are widely chosen for this purpose due to their desirable mechanical and chemical properties while being cost-effective [9–11]. Serving as a protective layer for the internal circuitry, the encapsulation material is, thus, most exposed to the environment. Therefore, the ageing of EMC is one of the most important aspects of the ageing of electronic packages. Figure 1.3 indicates the aforementioned five domains of physics-of-degradation along with a select number of degradation and failure mechanisms that are relevant for the scope of this chapter.

Thermal ageing of EMC results in the oxidation of its outer layer through its contact with atmospheric oxygen. It has been established with Fourier Transform Infrared (FT-IR) spectroscopy measurements that the ageing process changes the material chemically [12, 13]. Moreover, the changes in thermomechanical properties of thermally aged EMC specimens have also been reported in [14, ch.7], [15, ch.5], and [16]. Owing to its volume-share as high as 75% [17] within a typical electronic package, encapsulation tends to govern the overall thermomechanical behaviour of the electronic component [18]. Thus, the degenerative changes in moulding compounds can significantly affect a component's operational lifetime.

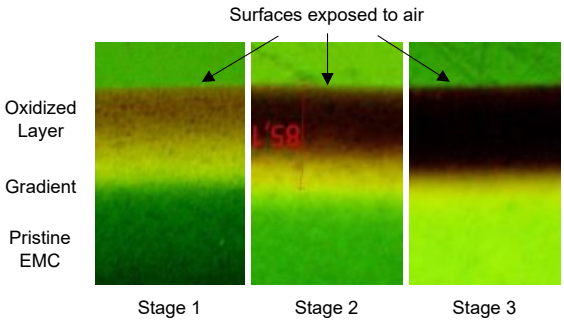


Figure 4.1: Cross sections of EMC specimens, oxidised at three different temperatures of 175 °C, 200 °C, and 225 °C for over 165 h, observed under a fluorescence microscope. Each image represents a different 'stage' of ageing, while the distinct colours within each specimen indicate two different 'phases' of EMC – pristine and oxidised.

Figure 4.1 shows the cross sections of three thermally aged EMC specimens, oxidised at three different temperatures of 175 °C, 200 °C, and 225 °C for over 165 h, observed under a fluorescence microscope. Within a single specimen, the two different colours indicate two distinct 'phases' of EMC – pristine and oxidised. The colour gradient in *Stage 1* shows a gradual transformation from an oxidised to a pristine phase, whereas *Stage 3* indicates a clear distinction between these two phases. The difference in the colour composition of the oxidised layers across three different specimens highlights different 'stages' of EMC oxidation. It is crucial to identify the distinction in these stages while modelling the degradation phenomenon. As thermal ageing progresses, the oxidation layer grows in thickness, and the outer layer of EMC becomes more and more oxidised [19, pp.68-74].

In general, the growth of the oxidation layer thickness is both time- and temperature-dependent [20]. At higher temperatures, the oxidation layer grows faster, resulting in a darker layer that is easier to distinguish. At lower temperatures, the oxidation layer grows more slowly, and a prominent gradient from pristine to oxidised state is observed. The temperature dependency of the ageing process is presented in references [15, pp.73-76], [21, 22], where the cross sections of thermally aged EMC specimens indicate that the same storage time at different ageing temperatures results in different stages of EMC oxidation.

In the current work, we focus on the time dependency of the ageing process carried out at a constant temperature of 150 °C. Therefore, different ageing stages correlate to different storage times. Figure 4.2 illustrates three different stages of EMC oxidation obtained by isothermal ageing of bar-shaped EMC specimens with rectangular cross sections. Note the increased thickness and changed colour of the oxidised layer from left to right. The latter also indicates changes in material properties. In the case of ageing of an encapsulated electronic package, the outer layer of EMC is oxidised to form an outer shell. It exhibits modified thermomechanical properties and modifies the mechanical behaviour of the entire package. This can accelerate certain failure modes, such as delamination along the EMC-die interface, cracks

Figure 4.2: A schematic representation of the rectangular cross sections of (partially oxidised) bar-shaped EMC specimens which are isothermally aged at 150 °C. The oxidation layer not only grows in thickness as a function of ageing time but also changes its colour from pale green to dark brown.

in the bulk of EMC [12], and fatigue failure of solder joints [23]. Thus, a virtual model of a microelectronic package that can capture these failure modes needs to incorporate and to be able to reflect the effect of ageing.

A Digital Twin-based modelling approach can be utilised to address this. This approach requires an active connection between the physical entity and its virtual representation for data and information exchange. This facilitates a continuous update of the digital model to reflect the current state of the physical entity. In a physics-based approach, degenerative changes in a material are modelled using the physics-of-degradation. A physics-based Digital Twin can provide more insights on the effects of material degradation on different failure mechanisms, can facilitate the prediction of component failure, and therefore, plays a key role in the PHM of electronics. Thus, a dedicated physics-based DTI of an electronic component should reflect the changes in material composition (the extent of degradation) and material behaviour (the changes in the aged part of the component).

Here, the focus is on quantifying gradual degenerative changes within EMC, which can be achieved by representing the two aspects at any stage of thermal ageing – (a) the thickness of the oxidised layer and (b) its thermomechanical properties at the current stage. The first aspect has been addressed in some previous studies, which present the models for the growth of oxidation thickness using either physics-based laws or empirical relations based on activation energies [14, p.133], [15, p.74], [19, p.72], [23]. The second aspect, however, is not well addressed in the literature.

Thermomechanical properties of the oxidised EMC are, in most cases, determined at only one particular stage of EMC oxidation (*e.g.*, 150 °C for 2000 h) [21]. This approach is insufficient as it does not provide any information about the intermediate stages of ageing. Moreover, the FT-IR study [13] reports gradual chemical changes as a function of storage time for ageing up to 5000 h at 200 °C and 250 °C. Thus, the thermomechanical properties of just one configuration of the oxidised EMC cannot simply be assumed to be the same and utilised throughout to represent any intermediate stage of thermal ageing. The current work aims to address this gap.

This chapter is organised into two main parts. The initial part focuses on preparing an experimentally validated physics-based Digital Twin Instance (DTI), and the

latter on using that for a simulation-based study. First, a systematic methodology is presented to prepare an experimentally validated physics-based Digital Twin, which can reflect the progress of EMC oxidation in an electronic package due to High-Temperature Storage (HTS). It consists of three steps – (i) quantifying the extent of degradation, (ii) preparing a parametric geometry of the Device Under Test (DUT), and (iii) obtaining an ageing-stage-dependent material behavioural model. These steps are described in Section 4.2, Section 4.3, and Section 4.4.

Next, the prepared continuously updated package-degradation model is utilised to study the effect of EMC oxidation (using Finite Element (FE) simulations) on the warpage of the DUT, *i.e.*, an electronic package. It focuses on two aspects – (1) the change in the maximum warpage of a thermally aged package (several ageing stages) at room temperature and (2) the change in the shape of the warpage curve under a thermal cycle in Section 4.5 and Section 4.6, respectively. Finally, the simulation results are analysed in the context of failure prediction (solder fatigue and EMC-die delamination), underlining the contribution of a continuously updated Digital Twin in the PHM of electronics packaging and electronics-enabled systems.

4.2. Quantification of Oxidation Layer Thickness

EMC oxidation is a combination of two simultaneous processes – (1) the diffusion of oxygen (from the surrounding air) into the free volume of the polymer network and (2) the chemical reaction of oxygen with the resin. Thus, it depends on the oxygen permeability of the material and the intrinsic rate of oxidation [20]. It results in a heterogeneous oxidised layer only up to a certain depth from the exposed surface because epoxies are fairly reactive but have low oxygen permeability [24]. Elevated temperatures facilitate a higher oxidation rate because of the higher activation energies [25]. The rate also slows down as the oxide thickness grows, because it acts as a barrier for further diffusion due to its increased density [15, pp.73-76]. Thermo-oxidation of EMC is dominated by the diffusion of oxygen through the polymer [26] and is referred to as Diffusion-Limited Oxidation (DLO).

In the case of thermal ageing at a constant temperature, the thickness of the resulting oxidation layer defines a particular 'ageing stage'. To prepare a degradation model, the Thickness of Oxidation Layer (TOL) was experimentally measured as a function of storage time (t). Bar-shaped EMC specimens (80 mm × 10 mm × 4 mm) were thermally aged for up to 3000 hours at 150 °C, which is above the glass transition temperature (T_g) of the selected EMC. The aged (partially-oxidised) specimens were cross-sectioned and observed under a fluorescence microscope equipped with Ultraviolet (UV) illumination that reveals more details due to a smaller wavelength.

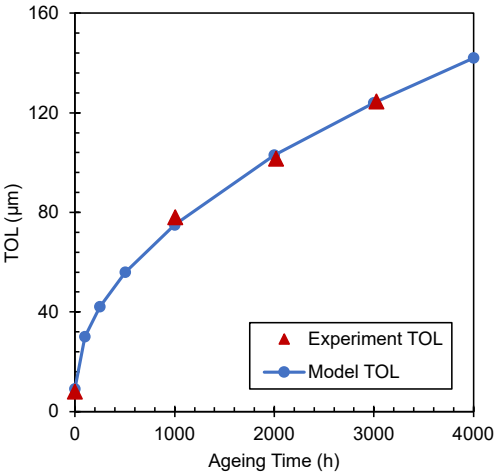


Figure 4.3: Experimentally measured TOL data (red) for thermal ageing at 150 °C fitted to the 'EMC Oxidation Model', which follows the mathematical relation $d = d_0 + d_1\, t^n$, where d is the oxidation layer thickness, t is the ageing time, and the rest are fitting parameters with values $n = 0.5$, $d_0 = 8.7\,\mu m$, and $d_1 = 2.1\,\mu m/h^n$. TOL values generated using the model are indicated in blue.

The minimum and maximum values of the TOL were measured at multiple locations within each specimen by defining two boundaries – the first between the dark-brown and the yellow region and the second between the yellow and the green region (refer to 'Stage 1' in Figure 4.1). The mean value was utilised as the recorded TOL at different ageing times. Figure 4.3 shows the measured data in red.

The oxidation process, being diffusion-limited (*i.e.*, DLO), is often modelled as a diffusion-dominant process with a direct proportionality to the square root of time [19, pp.68-74], *i.e.*, $d \propto \sqrt{t}$, where d is the TOL. The above relation was considered as the basis for the oxidation growth model. The proposed degradation model takes the form of Equation (4.1), where d_0, d_1, and n are fitting parameters. Instead of directly using the square root of time, a slightly more flexible version with $n \in (0, 1)$ was used as a starting point.

$$d = d_0 + d_1\, t^n \tag{4.1}$$

A standard curve fitting procedure was followed to determine the parameter values ($d_0 = 8.7\,\mu m$, $d_1 = 2.1\,\mu m/h^n$, and $n = 0.5$). A non-zero value of the parameter d_0 reflects the oxidation thickness ($\approx 9\,\mu m$) at $t = 0$ due to the processes such as the Post Mould Cure (PMC) prior to the ageing experiment. Interestingly, the value deduced for the parameter n is exactly equal to 0.5. The oxidation growth model fitted to the experimental data is indicated in Figure 4.3, along with some additional TOL values (marked blue) calculated using the finalised model. These values and associated material behaviour are utilised later in Section 4.5 and Section 4.6.

4.3. Parametric Geometry of Test Package

The second step is to create a geometric model of a test device such that it can be updated to reflect the current degradation state. A Ball Grid Array (BGA) package with a flip-chip construction (*i.e.*, the die-to-substrate interconnects consist of copper pillars with solder caps) was chosen as the DUT. Initially, a CAD geometry of the non-aged package was constructed, and then, some simplifications were incorporated to optimise for the required computational efforts.

The substrate has a total of five layers (three copper-dominant metallisation layers and two intermediate layers containing only copper vias surrounded by a polymer resin), each of which was modelled individually as a homogenised layer. Layer-wise equivalent material properties were calculated by volume-based weighted averaging of the (linear elastic temperature-dependent) mechanical properties of copper and the utilised polymer. Moreover, the copper pillars and solder caps in the flip-chip construction were modelled in detail as cylindrical structures. For the chosen DUT, the EMC encapsulates only the die and die-to-substrate interconnects (including the underfill) and rests on the substrate (*i.e.*, does not encapsulate the substrate).

To reflect the growth of the oxidation layer within EMC, a single parameter 'd' was defined to represent the current value of the TOL. It was assumed that the oxidation layer grows uniformly in directions perpendicular to all exposed surfaces of the EMC, which is also a good representation of reality. This results in a core-shell structure representing two distinct layers of the EMC – oxidised and pristine. Figure 4.4 indicates the core-shell style geometry of the thermally aged package. Considering symmetry, the required computational effort was reduced by using a quarter-geometry of the DUT.

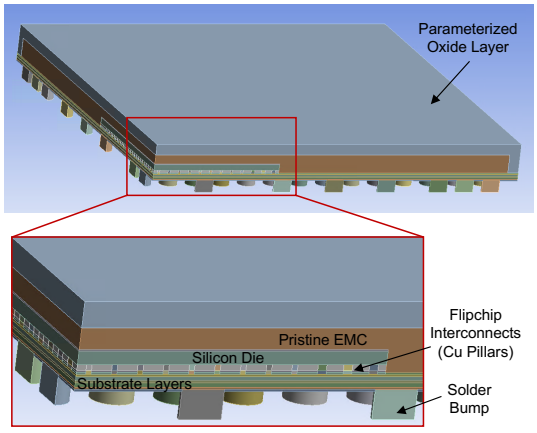


Figure 4.4: The prepared quarter geometry of the thermally aged DUT (a flip-chip BGA package) with annotations for its sub-layers, including a parameterised outer layer for representing the oxidised EMC.

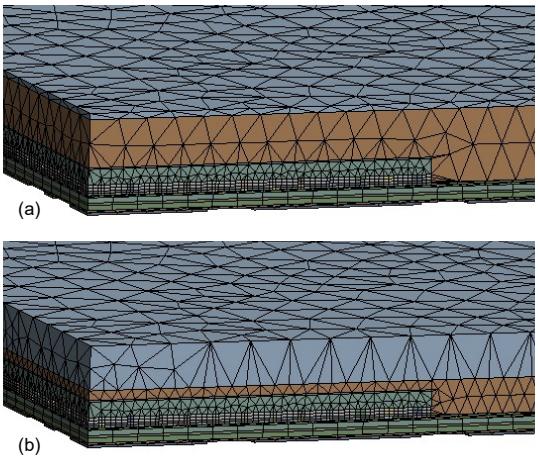


Figure 4.5: The meshed package geometry of the two near-extreme cases within the range of EMC oxidation – (a) very thin (250 h, 42 µm) and (b) very thick (19 145 h, 300 µm) oxidised EMC layer. 3D Finite Elements with quadratic shape functions are used to ensure good quality results for all considered cases.

A parametric setting was utilised along with an automation routine to update the prepared geometric model using a variable TOL value representing any stages of EMC oxidation (isothermal ageing at 150 °C) for up to 28 640 h (≈ 3 years). The TOL growth beyond 3000 h is extrapolated using the fitted model. Appropriate settings were applied to maintain the mesh quality for all intermediate stages of ageing. This setting assumes there would be no cracking in the EMC, which could affect O_2 diffusion into the bulk. Figure 4.5 indicates the meshed geometry of two near-extreme cases within the range of oxidation – (a) with a very thin (250 h, 42 µm) and (b) with a very thick (19 145 h, 300 µm) layer of oxidised EMC.

Higher-order finite elements (quadratic shape functions) with a mix of tetrahedral and hexahedral shapes and about 400 000 in number were utilised to ensure good quality results for all the considered cases. At any given ageing stage, the 'core' EMC would be assigned the 'pristine' material properties while the 'shell' (oxidised layer) gets the corresponding material properties of the oxidised EMC at the current degradation stage. A detailed procedure to derive these material properties at any intermediate stage is discussed in the following section.

4.4. Material Behaviour of Oxidised EMC

The third and most crucial aspect of a physics-based Digital Twin model is reflecting the changes in material behaviour at different ageing stages. To determine the change in thermomechanical properties as a function of the EMC oxidation state, partially-oxidised EMC specimens were utilised in experimental characterisation. Then, an analytical approach was pursued to calculate the effective properties of only the oxidised layer of EMC.

4.4.1. Experimental Characterisation

Two different sets of bar-shaped EMC specimens with rectangular cross sections were thermally aged at 150 °C for 0 h, 500 h, 1000 h, 1500 h, 2000 h, 2500 h, and 3000 h. For each ageing stage, the modulus of elasticity (E) was characterised using a single-frequency Dynamic Mechanical Analysis (DMA) at 1 Hz on the first set of aged specimens (80 mm × 10 mm × 4 mm); whereas the Coefficient of Thermal Expansion (CTE) and the shift in the glass transition temperature (T_g) were characterised using Thermal-Mechanical Analysis (TMA) on the second set of thermally aged specimens (15 mm × 4 mm × 3 mm). In this way, the data of the linear elastic temperature-dependent material properties for the pristine (0 h aged specimens) and different partially-oxidised EMC specimens were gathered experimentally.

Note that this data is derived from partially oxidised specimens and does not indicate the behaviour of only the oxidised EMC but that of an effective beam (E_{eff}), which is a composite beam-like structure consisting of pristine EMC (core) and oxidised EMC (shell). Therefore, the gathered data cannot directly be used for preparing the material model of the oxidised layer. Thus, additional analytical calculations were utilised for extracting experimentally evaluated values for the oxidised EMC (E_{ox}).

4.4.2. Evaluation of Elastic Modulus

The elastic properties of the oxidised layer at each ageing configuration were derived from the experimental data using the flexural equation extended for multi-material composite beams [12]. In this case, the cross-section of a partially-oxidised beam specimen consists of a 'core' pristine layer (thickness h_{pr}) sandwiched between two 'shell' oxidised layers (thickness h_{ox} each). Figure 4.6 illustrates the three-layer composite beam. Considering a wide beam, the analytical calculation considers the oxidation layer only on the top and bottom of the pristine layer. Thus, the total beam thickness h can be expressed as $h = h_{\text{pr}} + 2\,h_{\text{ox}}$.

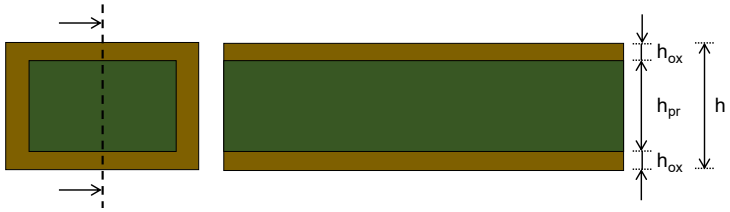


Figure 4.6: The illustration of a partially oxidised bar-shaped EMC specimen with a rectangular cross-section as a three-layered composite beam with a total thickness 'h'. h_{pr} is the thickness of the pristine EMC (core) while h_{ox} is that of the oxidised EMC layer (shell); and thus, follow the relation $h = h_{\text{pr}} + 2\,h_{\text{ox}}$.

Following the bending equation, the bending moment M at a cross-section of an equivalent homogeneous beam can be equated with that of a composite beam. More-

over, strain-continuity (and discontinuous stress) can be applied across different layers within a cross-section. This is indicated in Equation (4.2); where σ is the axial stress (horizontal) on a differential cross-sectional area $\mathrm{d}A$ at a (vertical) distance y from the neutral axis of the beam, E is the elastic modulus, and ρ is the density.

$$M = \int_A \sigma \, y \, \mathrm{d}A = \int_A \frac{E}{\rho} \, y^2 \, \mathrm{d}A \tag{4.2}$$

Due to the different elastic properties of the pristine and oxidised layers, the stress σ is discontinuous, which splits the integral into two parts as shown in Equation (4.3). The density is cancelled out from the integral because it remains practically unchanged, based on the internal tests for measuring the oxidation-induced shrinkage ($< 0.2\,\%$). Thus, the relation between the effective elastic properties and that of the individual layers boils down to Equation (4.4), where E_{eff}, E_{pr}, E_{ox} are the moduli of elasticity, and I_{eff}, I_{pr}, I_{ox} are the corresponding area moment of inertia, for the effective beam (partially-oxidised specimen), 'core' of the composite beam (pristine EMC), and 'shell' of the composite beam (oxidised EMC), respectively.

$$\int_{\mathrm{eff}} \frac{E_{\mathrm{eff}}}{\rho} \, y^2 \, \mathrm{d}A = \int_{\mathrm{pr}} \frac{E_{\mathrm{pr}}}{\rho} \, y^2 \, \mathrm{d}A + \int_{\mathrm{ox}} \frac{E_{\mathrm{ox}}}{\rho} \, y^2 \, \mathrm{d}A \tag{4.3}$$

$$\implies E_{\mathrm{eff}} \, I_{\mathrm{eff}} = E_{\mathrm{pr}} \, I_{\mathrm{pr}} + E_{\mathrm{ox}} \, I_{\mathrm{ox}} \tag{4.4}$$

$$\implies E_{\mathrm{eff}} \, h^3 = E_{\mathrm{pr}} \, {h_{\mathrm{pr}}}^3 + E_{\mathrm{ox}} \, (h^3 - {h_{\mathrm{pr}}}^3) \tag{4.5}$$

The principle of summing and subtracting the area moments of inertia to calculate values for composite cross-sections gives the expression $I_{\mathrm{eff}} = I_{\mathrm{pr}} + I_{\mathrm{ox}}$. Utilizing the expressions $I_{\mathrm{eff}} = bh^3/12$, $I_{\mathrm{pr}} = b{h_{\mathrm{pr}}}^3/12$ and the common width b, the equation gets further simplified to Equation (4.5). Based on this, the values for E_{ox} at different ageing stages were evaluated using the linear elasticity data of E_{pr} and E_{eff}. Figure 4.7 indicates the experimentally evaluated (ExpEval) values of E_{ox} from 20–300 °C at three different stages of oxidation (blue, grey, and red dots).

4.4.3. Mathematical Model for Elasticity

A mathematical model was fitted to the calculated elasticity data to obtain a smooth curve with an inverted S-shape. A few kernel functions were carefully considered to represent the temperature (T)-based relaxation of the modulus [27, ch.1]. Based on the comparison of their features, such as being bounded and the point of 'symmetry' on a logarithmic scale (abscissa), the Kohlrausch–Williams–Watts (KWW) function

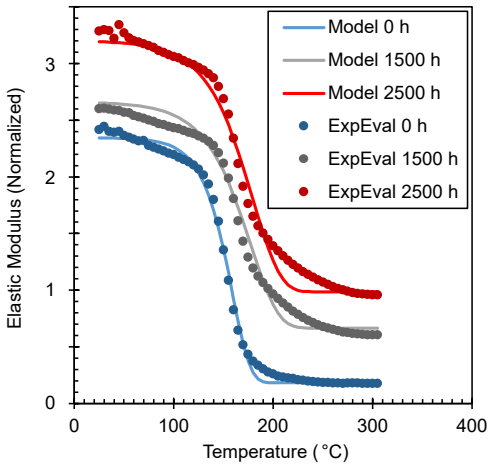


Figure 4.7: Linear elastic temperature-dependent material model (Equation (4.8)) fitted to the experimentally evaluated data of elasticity E_{ox} (Section 4.4.2) of the oxidised EMC layer at three different stages (0 h, 1500 h, and 2500 h) of thermal ageing carried out at the temperature of 150 °C.

was determined to be the most suitable empirical relation to represent the collected data. It is also referred to as the stretched exponential function and has a basic form given in Equation (4.6), where a and b are scaling parameters. The KWW function is also widely used for representing relaxation phenomena of various kinds, in particular, for amorphous materials such as polymers [28]. When resolved onto a linear scale (substituting $T = \log(x)$), it takes the form of Equation (4.7). Note that the common logarithm (base 10) is chosen here instead of the natural logarithm for a better fit to the experimentally obtained data.

$$f(x) = a \exp(-x^b) \tag{4.6}$$

$$\implies f(T) = a \exp(-10^{bT}) \tag{4.7}$$

The function was formulated such that it includes the material parameters (*viz.*, E_g^{ox}, E_r^{ox}, T_g) and incorporates temperature dependency. The final form of the adopted mathematical relation is given in Equation (4.8). It essentially defines E_{ox} as a function of the temperature (T); where $f \in (0, 1)$, r, and s are fitting parameters; T_g^{ox} is the glass transition temperature; E_g^{ox} is the glassy modulus; E_r^{ox} is the rubbery modulus of the oxidised EMC at a particular ageing-stage.

$$E_{ox}(T) = E_r^{ox} + E_g^{ox} f \exp\left[-10^{(T - T_g^{ox} - s)/r}\right] \tag{4.8}$$

Standard curve fitting techniques were utilised to obtain the values of the fitting parameters f, r, and s at different ageing stages. For the pristine EMC, their values

are $f = 0.938$, $r = 41.847$, and $s = 16.044$; whereas for all oxidised stages, they are $f = 0.725$, $r = 63.354$, and $s = 11.803$. Figure 4.7 shows the fit of the finalised material model (blue, grey, and red curves) to the experimentally evaluated E_{ox} data.

The proposed model allows obtaining elasticity curves for the oxidised EMC at any intermediate oxidation stage by determining just the values of three material-model parameters – T_g^{ox}, E_g^{ox}, and E_r^{ox}. Thus, the parameterisation of the material model is an important step in establishing continuity among different oxidation stages, more of which is described later in Section 4.4.6.

4.4.4. Evaluation of CTE and T_g

A similar procedure was followed to evaluate the CTE and glass transition of the oxidised EMC. First, the experimental data of partially oxidised specimens were used to determine the α_{eff} and T_g^{eff}. For each ageing stage, two straight lines were fit to the strain versus temperature data (TMA) using the standard curve fitting procedure. The slopes of these two lines were calculated for the α_1^{eff} and α_2^{eff} values; whereas the point of intersection of the two lines was used to obtain T_g^{eff}. Figure 4.8 indicates an example of the described procedure for the 1000 h aged specimen.

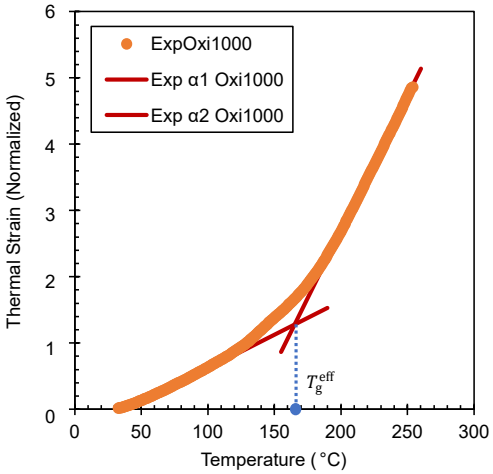


Figure 4.8: Evaluation of the CTEs values (*viz.*, α_1^{eff} and α_2^{eff}) and the glass transition temperature (T_g^{eff}) of the partially-oxidised EMC specimen (aged at 150 °C for 1000 h) using the thermal strain vs. temperature data sourced from the TMA experiments.

Evaluating the CTE values of the oxidised EMC (α_{ox}) from α_{eff} is not straightforward. The TMA test generally focuses on measuring only the change in the (dimension along the) length, whereas a bonded bi-material strip also shows a bending deformation due to a CTE mismatch between layers. Thus, the CTE calculation for a multi-material composite system requires more complex equations, including the moduli of elasticity of the involved layers. The relation between the thermal expansion-induced curvature of a bi-material strip and the properties (E and α) of its constituting materials is derived in the reference [29].

However, the partially oxidised EMC specimens used here are symmetric due to being oxidised from both the upper and lower surfaces of the composite beam. They are, therefore, expected to show negligible bending deformation due to the CTE mismatch. Thus, available values of α_{pr} and α_{eff} from the TMA test results were utilised to calculate α_{ox} at different ageing stages using volume-based weighted averaging, as indicated in Equation (4.9). A similar approach has also been utilised in a previous publication [12]; however, this section provides much more context by elaborating on the reasoning behind implementing this method.

$$h\,\alpha_{eff} = h_{pr}\,\alpha_{pr} + (h - h_{pr})\,\alpha_{ox} \tag{4.9}$$

The T_g is typically determined from the thermal strain versus temperature curves obtained from a TMA test. However, in this case, the T_g obtained from the TMA test would correspond to the partially-oxidised EMC specimen (T_g^{eff}) and not to the oxidised layer (T_g^{ox}). Thus, an additional ballpark value for T_g^{ox} of each oxidised stage was derived from the evaluated elastic modulus values (E_{ox} vs T) based on the DMA results (Figure 4.7). Both values were treated as tentative T_g^{ox} values, which need further fine-tuning and verification steps.

In this way, the linear elastic thermomechanical behavioural model was obtained for the oxidised EMC at different stages of thermal ageing. The elasticity model relies on three parameters: T_g^{ox}, E_g^{ox}, and E_r^{ox}; whereas the tentative values of α_{ox} and T_g^{ox} were also evaluated. Note that the above procedure provides only the initial estimates of the latter two. Thus, an experimental validation was carried out using the DUT to finalise the material model parameters.

4.4.5. Experimental Validation of Material Model

Experiments were designed around thermally aged DUT specimens to validate the material behavioural model. A few package specimens were stored at 150 °C for several ageing intervals of up to 3000 h. Then, the warpage of aged DUTs was measured at various temperatures between 25 °C (room temperature) and 260 °C. The specimens were exposed to high temperature at a rate of 60 °C/min in a controlled environment. In this context, the warpage indicates the out-of-plane deformation (along the Z-direction) measured on the top surface (XY plane) of the package.

A finite element simulation was set up on the parametric geometry of the DUT (Section 4.3) to reflect the experimental load conditions. A diagonal path was defined along the top surface of the package, and the warpage along that path was extracted from the FE results. Figure 4.9 shows the warpage evaluation path in the simulation and the experimental setting. The largest value (in magnitude) of the

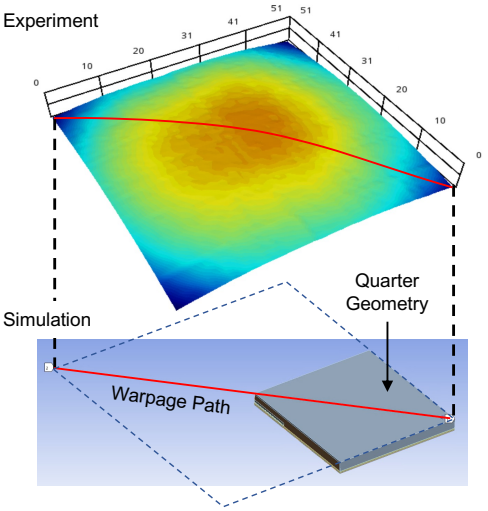


Figure 4.9: Experimental validation of the material model (FE simulations) using warpage measurements along a diagonal path on the top surface of a thermally aged package. The spatial plot in the figure corresponds to the out-of-plane deformation at 100 °C of a package at 1000 h of ageing.

out-of-plane deformation along the diagonal path was recorded as the maximum warpage (Deformation Z) at several temperature values for comparison against the experimental data. Figure 4.10 shows this comparison for the final validated model at three different ageing stages corresponding to 0 h, 1000 h, and 2000 h.

The warpage during a temperature variation primarily originates from the CTE-mismatch (α) among different layers of the package, which is further affected by the glass transition of EMC. Since the first utilised values of α_{ox} and T_g^{ox} were just initial estimates (as described in Section 4.4.4), the initial simulation-based results showed a noticeable mismatch with the experimental trends. This *Reason #1* was addressed by revising the values of the two parameters α_{ox} and T_g^{ox} in an iterative fashion (within an acceptable range) while using them in FE simulations.

The *Reason #2* behind this mismatch is the existence of an initial warpage and residual stresses due to the manufacturing process of a package, especially due to the moulding process. Residual stresses depend on several moulding conditions such as the packing/holding pressure, mould temperature, melt temperature, and injection velocity. A systematic experimental study of the effect of these parameters on the warpage of the moulded product has been presented in [30]. Several publications present characterisation of warpage of the final product utilising an analytical approach [31, 32] or a Finite Element-based numerical approach [33–37] along with the experimental validation.

Some studies describe the calculation of residual stresses after the moulding process (*i.e.*, the state of 'initial warpage') using a viscoelastic temperature-dependent model. This initial warpage occurs due to two things – (i) the 'cold shrinkage' of all materials

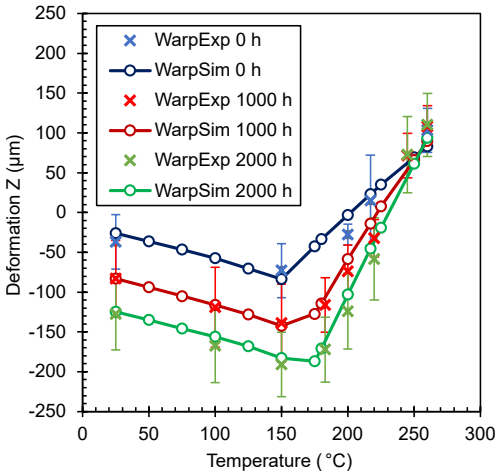


Figure 4.10: The comparison of the experimental data and the FE-simulation results of the maximum warpage along the diagonal path (shown in Figure 4.9) at different temperatures under a thermal load ramping up from 25 °C (room temperature) to 260 °C at 60 °C/min. The negative warpage values indicate the direction of the deformation along the $-z$ axis. The results show a good agreement between the simulation-based results (denoted by 'o') obtained using the finalised material model and the experimental data (denoted by '×') from the package specimens at three different stages of thermal ageing – 0 h, 1000 h, and 2000 h.

with a CTE mismatch among them, and (ii) the curing shrinkage of EMC during the moulding process. Both of these effects need to be coupled together for the FE simulation-based results to be closer to reality. Later, this 'initial' curing shrinkage is applied in finite element models using an initial-strain approach, in which the geometry is predefined with some initial strain values.

Moreover, the viscoelastic properties of EMC are not only time and temperature-dependent but also vary based on the Degree of Cure (DOC) [34]. For composites such as moulding compounds, it has also been observed that lower filler content gives higher values of cure shrinkage [38, p.40]. The shrinkage may or may not be linear with the DOC. A trend of the non-linear change of thickness of epoxy resin specimens with respect to the DOC has been observed and modelled in an earlier publication [39]. The current study, however, assumes linear elastic (temperature-dependent) models for all materials, including the EMC. Thus, consideration of viscoelastic effects is out of the scope of this chapter.

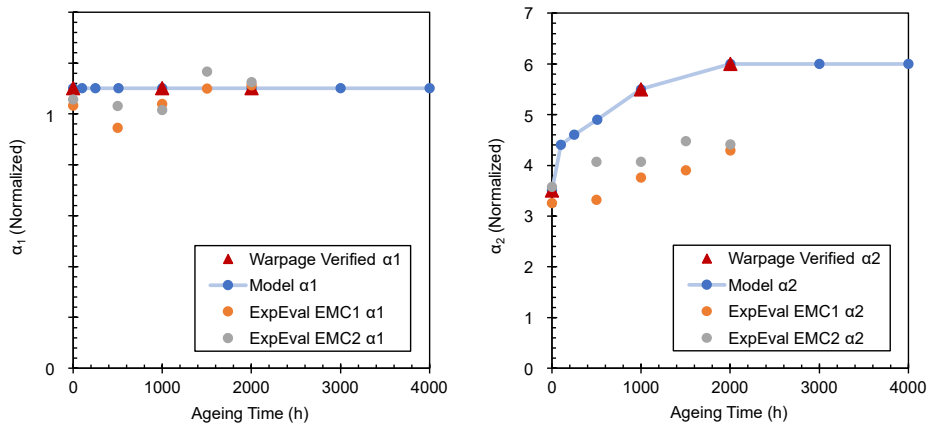
The *Reason #3* for the mismatch of experimental and simulation-based warpage results is the further curing shrinkage of EMC occurring after the moulding process (during PMC and later), which contributes to some additional warpage of the package. In general, during the curing process, the dimensional change occurs due to a combination of two processes – thermal expansion/contraction due to associated CTE ('thermal shrinkage') and chemical reaction ('chemical shrinkage'). Thus, a coupling of thermo-chemical-mechanical modelling would be necessary to represent this, which is also out of the scope of the current study.

However, there exists another simpler way to address the aforementioned points in *Reason #2* and *Reason #3* and keep using the linear elastic temperature-dependent

material models. Both the initial warpage and the curing shrinkage of EMC during moulding can be accounted for by adjusting its stress-free reference temperature (T_e). Setting the T_e of a layer higher than the T_{ref} of the entire geometry, when using linear elastic models, allows having the effect of initial strain and resulting additional deformation. Therefore, this technique was followed in this study to reflect the shrinkage in the FE simulation. The stress-free reference temperature of just the EMC material (T_e) was assigned a value higher than the rest of the package. As a starting point, the stress-free reference temperature (T_{ref}) of 180 °C was assigned to all components of the geometry, including the EMC. This was then updated by setting the T_e for pristine EMC to 190 °C.

It has also been reported that during thermo-oxidative changes, EMC undergoes additional shrinkage [40]. This was taken into account by setting the T_e of the oxidised EMC layer to an even higher value (> 190 °C) than that of the pristine EMC. This was independently done for each 'known' oxidised stage of EMC. In this way, the material model parameters T_e^{ox}, T_g^{ox}, and α_2^{ox} (CTE after the glass transition) were updated over multiple iterations of FE simulations until a good match was found with the experimental results (Figure 4.10).

Figure 4.11 highlights the difference between the initial estimates (denoted by the legend 'ExpEval') based on the procedure in Section 4.4.4 and the updated final values (denoted by 'Warpage Verified') of both CTE, before and after the glass transition. The final values of α_1^{ox} remain nearly the same for all ageing stages, while the α_2^{ox} values are significantly changed from their initial estimates.



(a) CTE before glass transition (α_1^{ox})

(b) CTE after glass transition (α_2^{ox})

Figure 4.11: The comparison of initial estimates ('ExpEval') of α_i^{ox}, where $i \in \{1,2\}$, with its values from the finalised material model ('Warpage Verified'). Additional trend-based data points (blue) for interpolating the material-model parameter α_i^{ox} are also indicated along with a trend line only indicative of continuity.

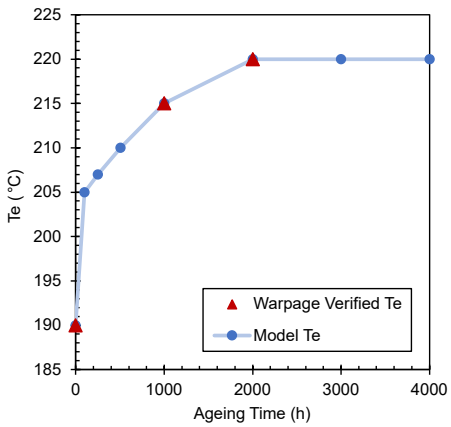
4.4.6. A Continuous Material Model

With the prepared material model, the thermomechanical behaviour of the aged package can be simulated only at a select number of ageing stages. For obtaining the material behaviour of any other intermediate stage, the entire exercise of experimental data collection, analytical calculations, and simulation-driven validation-based parameter tuning must be carried out. However, there are practical limitations to the number of such ageing stages for which the entire cycle can be repeated. Therefore, it makes sense to interpolate the material behaviour for the intermediate 'unknown' stages based on the (validated material models at the) 'known' stages of ageing. This would essentially formulate a continuous material model that can represent the thermomechanical behaviour of all stages of the oxidised EMC.

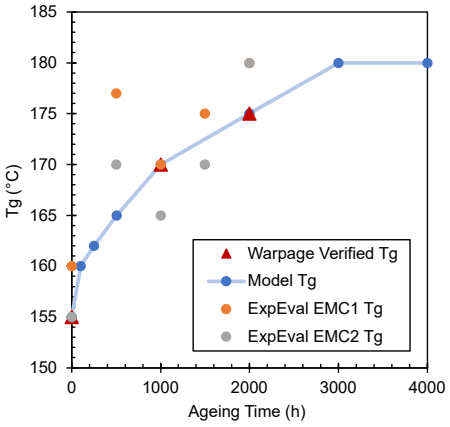
For this study, the continuity within EMC-oxidation stages was established by defining values for the material-model parameters (*viz.*, α_1^{ox}, α_2^{ox}, T_g^{ox}, T_e^{ox}, E_g^{ox}, E_r^{ox}) at additional intermediate ageing stages (here, ageing time t). However, they cannot simply be linearly interpolated between two known stages. Each parameter shows a unique trend, especially in the early stages (0 h to 1000 h) of ageing. This was carefully considered for each of the material model parameters.

Overall, thermomechanical changes in the oxidised EMC tend to saturate beyond 2500–3000 h of ageing. Most material model parameters show a trend in three phases: (a) a rapid initial growth, (b) a slow increase, and (c) saturation. However, these three phases do not necessarily appear at the same ageing time (t) for each material parameter. Thus, additional information on the trends in the glass transition, shrinkage, and other aspects was sourced from the literature, and the intermediate values of the model parameters were defined accordingly at a select number of additional ageing stages (*viz.*, 100 h, 250 h, 505 h, and >3000 h).

For example, the experimental trends of EMC shrinkage during oxidation in references [22, 41] indicate a very sharp initial growth within about 100 h of ageing, followed by a near-constant saturation value. To reflect this shrinkage trend, additional data points for T_e^{ox} were created with a steep jump between 0 h and 100 h, and a more or less a linear trend following the slope between the 1000 h and 2000 h stages. Figure 4.12a shows the development of T_e^{ox} as a function of ageing time. Red markers indicate values from the validated material models, while the trend-based intermediate values are marked in blue. A slightly modified trend was observed for the glass transition temperature T_g^{ox} [42] with the linear relation extending up to 3000 h. Figure 4.12b shows the known (red) and additional (blue) intermediate T_g^{ox} values. In addition, it also highlights the disparity between the initial estimates (denoted by 'ExpEval') and the warpage verified values from the finalised model.



(a) Shrinkage parameter T_e^{ox}



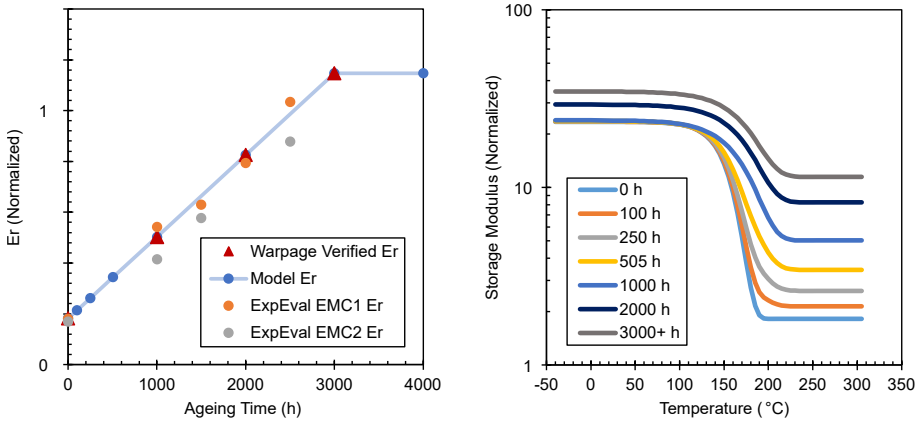
(b) Glass transition temperature T_g^{ox}

Figure 4.12: Values of the material-model parameters T_e^{ox} and T_g^{ox} at different ageing stages. Experimentally verified values are marked in red, while the additional trend-based interpolated values are marked in blue, joined by a trend line to indicate continuity. Subfigure (a): T_e^{ox} is the reference temperature (FE-simulations) of the oxidised EMC to account for the oxidation-induced shrinkage. Subfigure (b): The initial estimates ('ExpEval') of the glass transition temperature of the oxidised EMC T_g^{ox} show a nominal scatter around the experimentally verified values.

The CTE before glass transition (α_1^{ox}) stays nearly constant throughout the ageing time-domain (also observed in reference [15, pp.86-90]), and thus, is represented with a constant function. It also remained unchanged from the initial estimates. The aforementioned generic trend was implemented for the additional data points of the CTE after glass transition (α_2^{ox}) by introducing an initial jump within the first 100 hours of ageing and then a linear trend (Figure 4.11b).

Elasticity-related material parameters (E_g^{ox} and E_r^{ox}) showed distinct trends. The glassy modulus stays nearly the same up to 1000 h of ageing but later shows a linear growth up to 3000 h. On the other hand, the rubbery modulus shows a more or less linear trend until 3000 h. A linear growth of E_r is also recorded in studies [42, 43]. Figure 4.13a shows E_r^{ox} as a function of ageing time, including the results evaluated from the experimental characterisation at different ageing stages.

The vertical shift in the elasticity curves for partially-oxidised EMC specimens (experimental data) tends to slow down and eventually saturate after a particular ageing time (also seen in the literature [44]). Since this change is essentially due to the changes in the oxidised layer, the elasticity curves of the oxidised EMC were assumed to be constant above 3000 h of ageing. This is also the reason behind keeping the rest of the parameters constant beyond the 3000 h stage. Figure 4.13b shows the linear elastic temperature-dependent elasticity model (storage modulus) for the oxidised EMC, including several intermediate stages between 0 h and 1000 h.



(a) Rubbery modulus E_r^{ox}

(b) Elastic modulus E_{ox}

Figure 4.13: The rubbery modulus of the oxidised EMC (E_r^{ox}) and the temperature-dependent elasticity curves (E_{ox}) as a function of ageing time. Subfigure (a): The experimentally evaluated values ('ExpEval') of E_r^{ox} and the values from the elasticity model (Equation (4.8)) show a close agreement, and a linear growth trend up to 3000 h of ageing is observed. Subfigure(b): The elastic (storage) modulus E_{ox} curves include a few 'known' ageing stages, *viz.*, 0 h, 1000 h, 2000 h, and 3000 h. Elasticity curves for some additional ageing stages between 0 h and 1000 h and beyond 3000 h are also indicated based on the continuity of the material-model parameters – E_g^{ox}, E_r^{ox}, and T_g^{ox}.

In this way, the additional values of material-model parameters at intermediate stages of EMC oxidation were introduced to form the basis of a continuous material model. All the graphs of these parameters (Figures 4.11b, 4.12a, 4.12b, 4.13a and 4.13b) show the data points joined with a trend line, which is only indicative of continuity. Each trend line is intentionally kept piecewise linear. A mathematical model is ideally required for each parameter – α_1^{ox}, α_2^{ox}, T_g^{ox}, T_e^{ox}, E_g^{ox}, E_r^{ox} – to define a smooth curve indicating their dependency on ageing time (t). However, this was deliberately not carried out owing to the fact that some of these points, although backed by the trends in the literature, are artificially interpolated. To create an even more robust continuous model, additional experimentally validated data points (*i.e.*, more of the red triangles in the graphs) are required, especially in the first 1000 h of ageing.

The continuous material model (Section 4.4) reflects gradual changes in the thermo-mechanical behaviour of the oxidised EMC. Combining this with the degradation model (described in Section 4.2) and the package geometry (described in Section 4.3), a complete, continuously updated, physics-based Digital Twin is formed. This model also qualifies as a cloud-based component of a Digital Twin Instance (DTI), which is applicable for the intermediate stages in a product lifecycle (refer Section 2.4.5), *i.e.*, when the product is already manufactured. The prepared physics-based DTI is capable of reflecting package-level thermomechanical degradation.

4.5. Package-Warpage at Room Temperature

Electronic packages, when exposed to a varying thermal load, exhibit warpage, *i.e.*, a nonuniform out-of-plane deformation. Such a mechanical deformation results in additional stresses within several layers of a package and their interfaces. When applied in a cyclic fashion, it can lead to fatigue-based failure modes such as cracks in solder joints and EMC and the separation (delamination) at the interfaces of die-EMC, die-adhesive, adhesive-substrate, *etc.* Thus, warpage can serve as a good baseline indication to define the severity of failure modes.

Warpage due to a thermal load originates from the difference in thermal expansion properties (CTE-mismatch) among the constitutive materials of a package. The glass transition of EMC is particularly crucial as it exhibits two different CTE values (α_1^{pr}, α_2^{pr}) leading to a sudden change in the deformation pattern in a short temperature range. A thermally aged package needs even more attention due to the presence of an additional layer of the oxidised EMC, which also exhibits a glass transition and two different CTE values (α_1^{ox}, α_2^{ox}). In addition, the relative difference in the elasticity of multiple layers also contributes to the resulting deformation pattern. Thus, the continuous material model of the prepared Digital Twin comes in particularly handy in determining the package warpage at any intermediate stage of thermal ageing.

This section analyses the effect of oxidation layer thickness on room temperature warpage. As described in Section 4.4.5, there exists inherent warpage at room temperature due to the manufacturing process (including moulding and solder reflow), which introduces a different 'stress-free temperature' (much higher than room temperature) for different materials. A finite element simulation was set up using the test-package geometry and prepared material model to evaluate the package warpage at room temperature under a uniform thermal load from 180 °C to 25 °C. In addition to the warpage-validated 'known' ageing stages – 0 h, 1000 h, 2000 h, 3000 h, three intermediate stages of 100 h, 250 h, and 505 h were utilised. The TOL and material-model parameters for these intermediate stages are indicated in Figure 4.3 and Figures 4.11b, 4.12a, 4.12b, 4.13a and 4.13b, respectively. The TOL values beyond 3000 h were extrapolated using the same growth model, assuming it continues to follow the same trend. For the material properties at ageing stages beyond 3000 h, appropriate assumptions described in Section 4.4.6 were followed.

It is important to note that the automated geometry update could be implemented up to 365 µm of TOL (corresponding to 28 640 h) since that is also the thickness of the EMC layer above the die. Beyond that, the geometry was manually updated by further expanding the EMC oxidation layer (from the top) only in the region around the die and also uniformly from the sides of the package. Finally, a theoretically

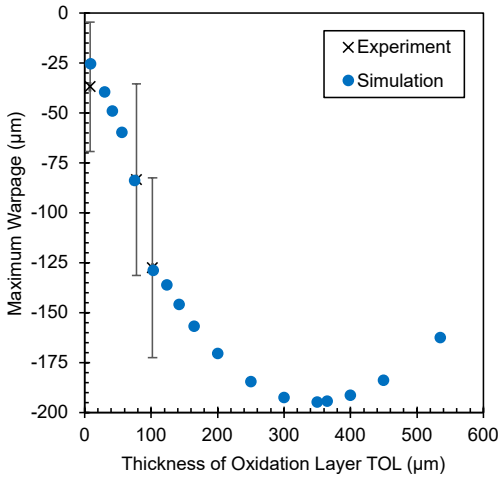


Figure 4.14: Maximum warpage of the test package evaluated along the diagonal path (as indicated in Figure 4.9) as a function of oxidation layer thickness (TOL). The error bars of the experimental data correspond to $\pm 3\sigma$, where σ is the standard deviation.

plausible stage with a fully oxidised EMC layer corresponding to 62 500 h (about 7 years) of isothermal ageing was also considered for the sake of comparison. The maximum value (by magnitude) of the out-of-plane deformation along the diagonal path (Figure 4.9) was recorded at each considered aged state. Figure 4.14 shows the simulation-based values as a function of TOL. For additional context, previously recorded experimental values are also indicated with error bars corresponding to $\pm 3\sigma$, where σ is the standard deviation. The experimental values of TOL correspond to the 0 h, 1000 h, and 2000 h stages of ageing. Negative values of warpage only indicate the direction of the deformation along the $-z$ axis.

A rapid increase in the magnitude of the maximum warpage is observed within the first 2000 h of ageing (TOL ~100 µm). Then, the rate slows down drastically with respect to the ageing time (t) until the TOL reaches 250 µm (13 135 h ≈ 1.5 years). Later, a saturation is seen near the TOL of 350 µm, and the curve reverses its trend after the TOL of 365 µm, showing lower values (magnitude) of maximum warpage for all stages until the fully-oxidised stage is reached.

This interesting change can be explained by a combination of factors. The TOL value and intermaterial interactions are the key contributing factors here because the material-model parameters are kept unchanged after the 3000 h stage (TOL 365 µm). Note that the 'point of reversal' is the instance where the EMC right above the die is completely oxidised (refer Figure 4.5 for more context), which means, from this point onwards, the fully oxidised EMC (*stiff*) interacts directly with the silicon die (*even stiffer*) without any pristine EMC (*softer*) sandwiched between them. This pivotal point also marks about 75% of the total EMC volume being oxidised (*i.e.*, around ~7 mm^3 of pristine and ~18 mm^3 of oxidised EMC).

The CTE does not seem to play a significant role in this phenomenon for three reasons – (1) α_1^{ox} remains unchanged from α_1^{pr}, (2) α_2^{ox} does not play any role for the considered temperature range, *i.e.*, for the defined thermal load, and (3) α^{Si} remains nearly constant within a small range of 2.5–3.5 ppm/°C for the given thermal load. Therefore, it is concluded that the observed 'reversal' phenomenon is initiated and dominated by the direct interaction of two stiff materials (oxidised EMC and silicon die) in combination with a significantly high volume percentage (≥ 75%) of the oxidised layer within the encapsulating EMC.

4.6. Warpage Curvature under Thermal Cycling

This section focuses on studying the changes in the package warpage induced by a thermal cyclic load as a function of EMC oxidation. A finite element simulation was set up with a thermal load including a single cycle from 25 °C to 260 °C with a 1 °C/sec heating and cooling ramp and an intermediate dwell time of 30 min at the highest temperature. The exercise was repeated for the same 17 distinct ageing stages mentioned in Section 4.5 (from pristine to fully oxidised), and the prepared and validated continuous material model was also utilised.

The warpage was evaluated along the half of the path shown in Figure 4.9, *i.e.*, from one corner to the centre of the package. For the comparison at various temperature steps, the plots for relative deformation were created by setting the displacement at the 'package corner' end of the warpage path to zero. Figure 4.15 and Figure 4.17 show a few results. The numbers on the x–axis only indicate the relative position of the points along the warpage evaluation path, where the position '0' is the corner of the test package and the position '10' is its centre.

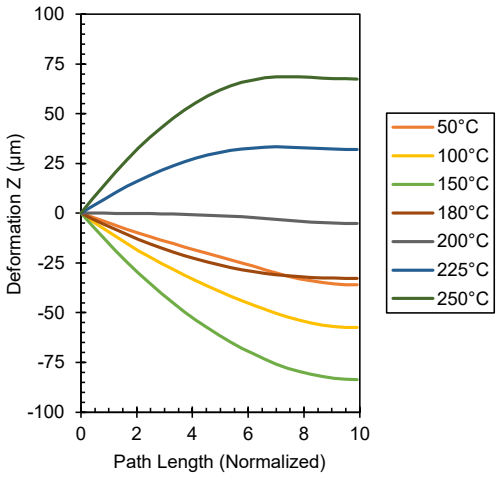
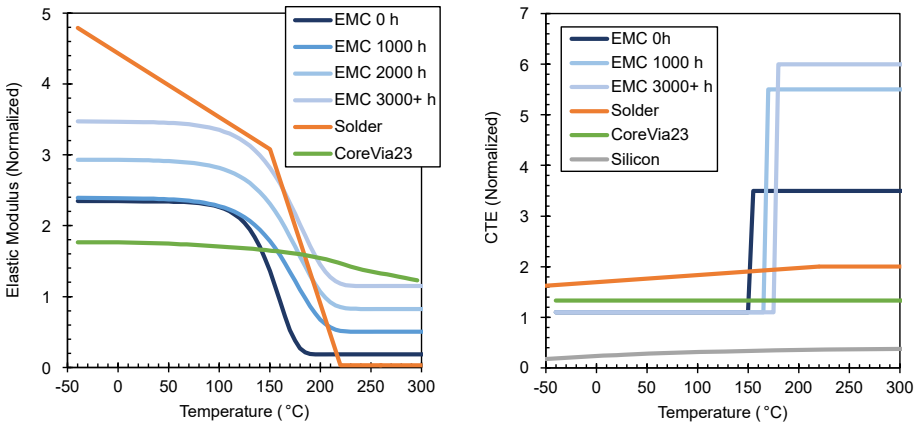


Figure 4.15: Warpage curves of a pristine package (0 h of ageing) under a thermal cyclic load from 25 °C to 260 °C. The values on the x–axis indicate the relative position of the points along the warpage evaluation path, '0' being the package corner and '10' the centre. The shape of the curve begins to change the trend at around 150 °C, and it completely reverses from 'smiling' (⌣) to 'frowning' (⌢) above 200 °C.

The results at all ageing stages (refer Figure 4.17) indicate one common trend: the reversal of the shape of the warpage curve from 'smiling' (⌣) to 'frowning' (⌢). There are two key aspects of this change – (i) the point (temperature step) at which the curvature reversal begins, and (ii) the actual point where the shape changes. Both of these aspects are primarily governed by the increasing volume share and evolving material properties of the oxidised EMC layer.

Figure 4.15 shows the warpage graphs for the package without ageing. The beginning of the curvature change is observed at around 150 °C. This 'pivot temperature' shifts to higher temperature values as the oxidation stages progress. This can be seen in Figure 4.17, where the plots in subfigures (a), (b), and (c) show the warpage curve at 180 °C higher than that of 150 °C (indicating the beginning of reversal), while the plot in subfigure (d) indicates the opposite. This means the pivot temperature moves from around 150 °C for the non-aged stage to above 180 °C for 3000 h of ageing.

This can be explained by the relative differences in the thermomechanical properties of various materials at a particular temperature. Figure 4.16a and Figure 4.16b show the elastic modulus and CTE of a few materials constituting various layers of the test package. The glass transition of EMC (pristine and oxidised) and the softening of solder material (due to the approaching melting point) occurs around the 150 °C mark. The softened layers allow the relaxation of inter-layer stresses and thus produce a less severely deformed shape of the warpage curve.



(a) Elasticity compared

(b) CTE compared

Figure 4.16: The comparison of the modulus of elasticity (E) and the coefficient of thermal expansion (α) of several materials constituting the test package, including a few stages of oxidised EMC. Subfigure (a): The softening of the solder material beyond 150 °C and the glass transition of EMC in the 150–200 °C range contribute to the shape-change of warpage curves. Subfigure (b): In addition to the gradual shift of T_g^{ox}, the α_2^{ox} attains much higher values as a function of ageing, increasing the CTE mismatch with other materials even further in the rubbery phase of the oxidised EMC.

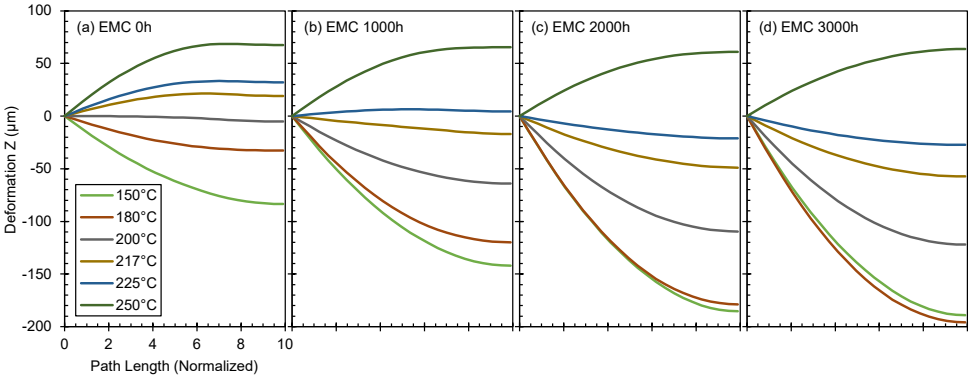


Figure 4.17: The comparison of the warpage curves of the test package (under a thermal cycle from 25 °C to 260 °C) at its four different stages of thermal ageing. The 'pivot temperature', where the shape of the warpage curve reverses the trend of change, shifts from around 150 °C (0 h) to around 180 °C (3000 h). Similarly, the 'shape reversal temperature' also attains higher values from between 200–217 °C (0 h) to between 225–250 °C (2000 h and 3000 h) as a function of thermal ageing.

This is further facilitated by a small CTE difference between the EMC and most other materials (only a select few are shown in Figure 4.16b) in the glass transition region. The gradual shift of the pivot temperature can be explained by the gradual increase in the T_g^{ox} values for the higher stages of oxidation and the increasing volume share of the oxidised EMC. A polymer-dominant layer of the package substrate (named 'CoreVia23') was also considered for the comparison. The transition of that layer into the softer 'rubbery' phase is relatively subtle and does not seem to affect the warpage change as much as the pristine and oxidised EMC does.

Figure 4.17 shows the gradual shift of the actual 'shape reversal temperature' as a function of ageing. This value is between 200–217 °C for the non-aged stage (subfigure (a)), between 217–225 °C for the 1000 h stage (subfigure (b)), and between 225–250 °C for the 2000 h and 3000 h stages (subfigures (c) and (d)). Such a shift to higher values (temperature-delay) is expected to be caused by a combination of three things – (i) the increase in the volume percentage of the oxidised EMC, (ii) the increase in the value of T_e^{ox} (the stress-free temperature of the oxidised layer accounting for shrinkage), and (iii) the gradual shift of the glass transition region.

4.7. Effect on Die-level Stresses

The last two sections show that EMC oxidation affects the package warpage at room temperature as well as its deformation behaviour under a varying thermal load. Larger deformations induce higher local stresses, potentially increasing the risk of the occurrence of a failure mode or even accelerating it. For instance, the EMC-die

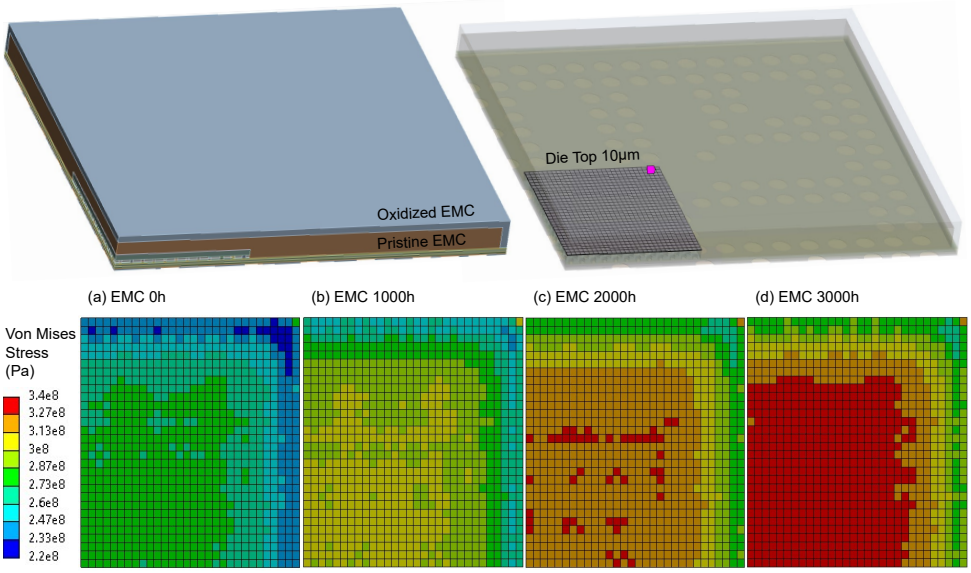


Figure 4.18: The comparison of von Mises equivalent stress (σ_{eq}) at the EMC-die interface (DieTop10 µm) as a function of thermal ageing of EMC. The subfigures indicate the results evaluated at room temperature (25 °C) for four different stages of EMC oxidation – (a) 0 h, (b) 1000 h, (c) 2000 h, and (d) 3000 h.

interface is prone to delamination. Thus, the effects on local stress levels were investigated utilising the prepared, validated model.

A 10 µm thin layer of the silicon die was selected as the domain of interest. This layer was meshed with a single element along its depth and a 30×30 grid of rectangles (91.03 µm×80 µm) along the top surface of the die. Several relevant stress fields, *viz.*, von Mises equivalent stress (σ_{eq}), maximum principal stress (σ_1), out-of-plane normal stress (σ_{zz}), maximum shear stress (τ_{max}), and in-plane shear stress (τ_{xy}), were defined as results and evaluated at multiple temperatures between 25–260 °C.

For all selected stress fields, the 'elemental mean' values were selected as the desired value to display. This means all stress components are represented as single values across an element. The elemental mean values are computed by first calculating the stress components at a select number of integration points (or Gauss points) and then averaging these values. The integration points are used for solving an integral numerically. In this context, it translates to solving the integral equation for the vector containing all components of the stress tensor.

Figure 4.18 shows the von Mises equivalent stress (σ_{eq}) at the EMC-die interface as a function of thermal ageing of EMC. All subfigures indicate the results evaluated at room temperature (25 °C), which showed the most severe stress pattern in

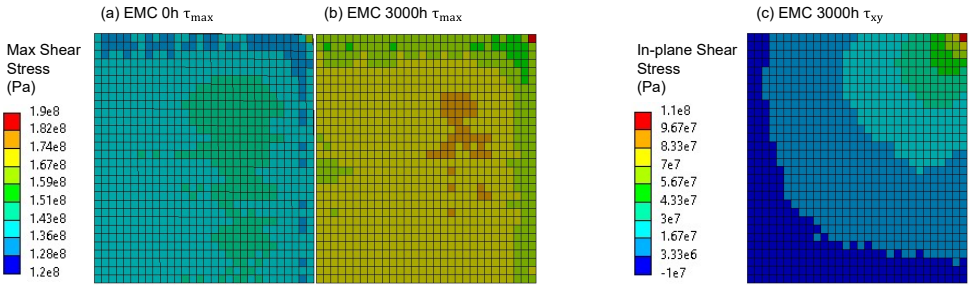


Figure 4.19: The comparison of shear stress at the EMC-die interface at room temperature (25 °C), evaluated at different stages of EMC oxidation. The subfigures (a) and (b) indicate the substantial increase in the maximum shear stress (τ_{max}) from 0 h to 3000 h of ageing. The subfigure (c) shows the in-plane shear stress (τ_{xy}) at 3000 h of ageing, which stays more or less consistent for all ageing stages.

the considered temperature range. Due to the selected 'elemental mean' option, a checkerboard-like pattern is obtained, which serves as a virtual stress sensor with a 30×30 grid at the EMC-die interface. The lower left corner of the rectangle lies on both axes of symmetry of the whole package, while the upper and right edges represent the outer boundary of the EMC-die interface. The results show significantly increased stresses as the oxidation of EMC progresses.

There is also a clear trend of increase in both maximum and minimum values of σ_{eq}, which goes from 286.02 MPa to 338.73 MPa (*i.e.*, an 18.42% increase) and from 223.76 MPa to 266.13 MPa (*i.e.*, an 18.93% increase), respectively, when comparing the 0 h and 3000 h oxidation stages. Figure 4.21(a) shows the values of σ_{eq} of the finite elements along the diagonal from the lower-left corner (*i.e.*, the die centre) to the upper-right corner (*i.e.*, the die corners) of the 10 µm top layer of the die. Along the diagonal path, the maximum and minimum σ_{eq} values showed an increase of 16.96% and 17.85%, respectively, for the 3000 h ageing stage compared to the non-aged stage. EMC oxidation shifts σ_{eq} to higher values with a nearly consistent difference (median ~ 56 MPa), keeping the shape of the graph in Figure 4.21(a) nearly unchanged. High stress-concentration in the central region and the corners of the EMC-die interface makes them the potential sites for the initiation of delamination, and thermal oxidation of EMC clearly makes these locations more susceptible to failure due to the increased stress values.

Another relevant stress field for delamination is the in-plane shear stress (τ_{xy}), which also showed the most severe stress pattern at room temperature. Figure 4.19(c) indicates the τ_{xy} pattern for 3000 h of ageing. A monotonic increase in values is observed along the diagonal sketched on the top surface of the die from its lower-left corner to the upper-right corner. At room temperature, there is a sudden increase in τ_{xy} towards the end of this path. This also aligns with the τ_{xy} trend presented

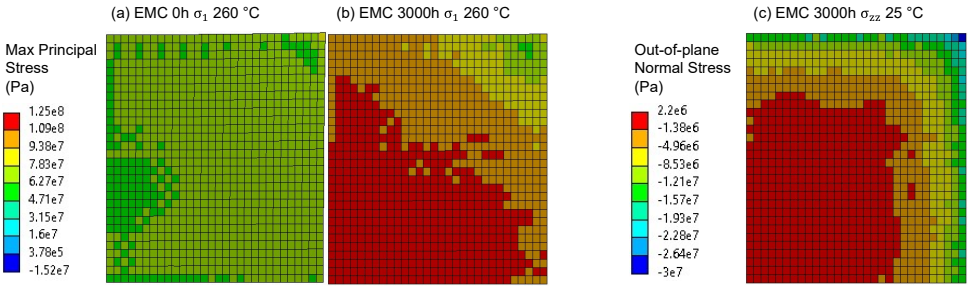


Figure 4.20: The comparison of normal stress at the EMC-die interface evaluated at different stages of EMC oxidation. The subfigures (a) and (b) indicate a substantial increase (~40%) in the maximum principal stress (σ_1) at 260 °C from 0 h to 3000 h of ageing. The subfigure (c) shows the out-of-plane normal stress (σ_{zz}) at room temperature (25 °C) at 3000 h of ageing, which shows a marginal increase as a function of thermal ageing but a pattern consistent with the von Mises stress (σ_{eq}) in Figure 4.18.

in the reference [45]. The current results show that this point of sudden increase retains its position, but the slope increases ever so slightly as a function of EMC oxidation. This brings more die area under higher in-plane shear stresses while increasing the maximum value of τ_{xy} by ~8.5% (from 100.40 MPa to 108.97 MPa) for the finite elements along the aforementioned diagonal path.

The maximum shear stress (τ_{max}) also showed an increasing trend for its maximum and minimum values at room temperature. Respectively, they show a 14.37% increase (from 162.00 MPa to 185.29 MPa) and a 18.60% increase (from 128.89 MPa to 152.87 MPa) when going from 0 h to 3000 h of EMC ageing. Figure 4.19(a) and (b) indicate the comparison of the stress pattern of τ_{max} for 0 h and 3000 h of ageing. For the finite elements along the diagonal path, a trend similar to the σ_{eq} values was observed, as indicated in Figure 4.21(b), where the element number '0' indicates the lower-left and '30' the upper-right corner of the die top layer. The graph shifts to higher values with a median difference of 28.35 MPa from 0 h to 3000 h of ageing.

Thermal ageing showed a marginal variation in the values of σ_{zz} at room temperature. However, σ_{zz} showed a pattern consistent with σ_{eq}, with high stresses at the package centre. Figure 4.20(c) shows the room temperature σ_{zz} pattern for 3000 h of ageing. Although the rest of the elements stay more or less consistent as a function of EMC oxidation, the corner elements showed a very high jump in (compressive) stress, especially going from the 2000 h to 3000 h ageing stage.

The maximum principal stress (σ_1) showed the most variation in the values not at room temperature but at 260 °C. Figure 4.20(a) and (b) show the great difference between σ_1 values for 0 h and 3000 h of ageing. A staggering 39.21% increase in the maximum values (from 87.04 MPa to 121.17 MPa) was observed, while the minimum values showed a marginal (< 5%) increase. Figure 4.21(c) shows the σ_1 values along

the diagonal finite elements. EMC oxidation for 3000 h results in over 85% increase in the maximum σ_1 value, which is close to the die centre (*i.e.*, Element '0'). Overall, the room temperature (25 °C) results of the stress fields σ_{eq}, σ_{zz}, τ_{xy}, and τ_{max} show one common trend, which is the high stress-concentration at the corner element of the EMC-die interface, induced by thermal ageing. Thus, the corner of the EMC-die interface becomes a potential site for failure, which is accelerated by EMC oxidation.

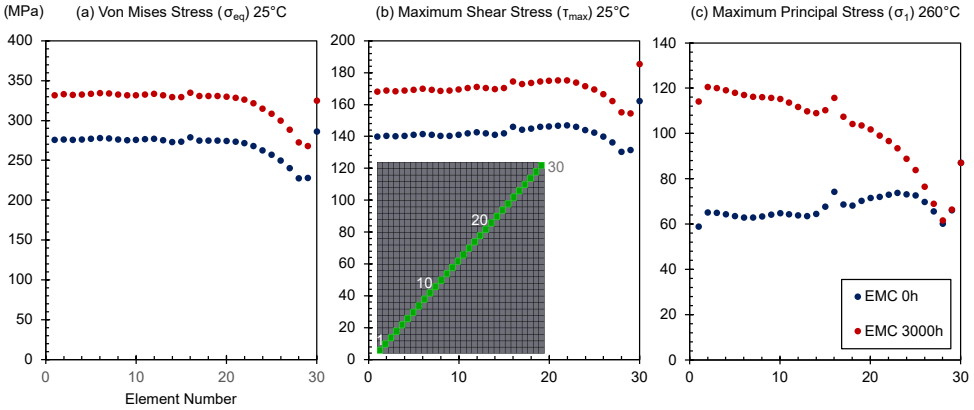


Figure 4.21: The comparison of stress values – (a) σ_{eq}, (b) τ_{max}, and (c) σ_1 – of the finite elements along the diagonal from lower-left corner to the upper-right corner of the 10 µm thick die top layer. The element number '0' indicates the centre, while '30', the corners of the entire EMC-die interface. The σ_{eq} and τ_{max} values show a uniform increase with a median of ~56 MPa and 28.35 MPa, respectively. On the other hand, σ_1 values show a steep increase (~ 40%) at the die centre and marginal change (< 5%) at the corners.

The results in Sections 4.5 to 4.7 describe the changes in the thermomechanical behaviour of an electronic package due to EMC oxidation. These changes are dominated by both the increase in the EMC oxidation thickness and the evolution of its material properties. The 'current' stage of the oxidised layer influences the warpage variation of a package under a thermal cyclic load. This, in turn, changes the accumulated damage in solder joints and affects the time to failure. Similarly, a differently warped package induces different stresses on the relatively stiff silicon die, facilitating delamination of the die-EMC interface. In this way, an experimentally validated physics-based Digital Twin was utilised to reflect the package-level degradation and to visualise and predict the package behaviour and its impact on the associated failure modes, therefore gaining deeper insights into its reliability.

Conclusion

Thermo-oxidative changes in epoxy moulding compounds modify the mechanical behaviour of an encapsulated electronic package. Reliability prediction can be significantly enhanced by reflecting these changes into the finite element models.

A physics-based Digital Twin, which is a continuously updated model, can reflect any state of component degradation by updating the component geometry to reflect the extent of degradation (*i.e.*, the quantified TOL) and also the material behaviour of the aged part of the component (*i.e.*, the oxidised EMC layer).

In particular, characterising the material behaviour of only the oxidised part of the EMC at different ageing stages is tricky. Thus, a hybrid approach was designed and implemented using experimental data, analytical calculations, and numerical validation to obtain six material model parameters, *viz.*, α_1^{ox}, α_2^{ox}, T_g^{ox}, T_e^{ox}, E_g^{ox}, E_r^{ox}. This exercise also helps in highlighting the scope for further improvement by identifying where the need for additional data collection is. Including more stages in the first 1000 h of ageing to establish continuity in the material-model parameters can make the existing model even more robust.

The finite element simulations (Sections 4.5 and 4.6) show the changes in the package warpage as a function of ageing stages and indicate a heavy influence of the oxidised layer on the mechanical behaviour of the package. Thermal ageing increases the magnitude of the maximum warpage at room temperature up to the point when the EMC on top of the silicon die is completely oxidised, and later decreases until the point of full oxidation. In addition, thermally aged stages exhibit a change in shape of the package warpage from 'smiling' (⌣) to 'frowning' (⌢) with a 'temperature-delay', *i.e.*, at a higher temperature compared to that of the pristine stage.

The equivalent (von Mises) stresses along the EMC-die interface are also heavily influenced by the state of oxidation (Section 4.7) with a slightly above 18% increase in the maximum and minimum values at room temperature. Similarly, the maximum principal stress (σ_1) showed a substantial increase (~40%) in its maximum values at 260 °C with 3000 h of ageing compared to the non-aged configuration. This clearly indicates that failure predictions based on the FE models would vary depending on the 'current' state of oxidation. It also underlines the key role of incorporating a Digital Twin for the PHM of electronic components and systems.

The workflow established in this chapter (Sections 4.2 to 4.4) can form the basis for the next step in modelling the thermomechanical degradation of EMC. A more complex viscoelastic material model could be prepared, which would require additional model parameters, a much larger design of experiments, and more intricate numerical simulations that can reflect viscoelastic effects. The current study represents the oxidation layer by a single value, *i.e.*, TOL. The oxidised EMC layer can be represented with multiple sub-layers, each with a varying degree of oxidation from 100% oxidised to 0% (pristine) and the intermediate layers accounting for the 'diffused but unreacted O_2'. This approach would require a more complex design of experiments and extensive FT-IR spectroscopy measurements.

Finally, the prepared physics-based Digital Twin Instance (DTI) can be used to study additional aspects and extract even more data, such as solder fatigue, to study the effect on different package- and board-level mechanical failure modes and to develop a data-driven approach for failure prediction.

REFERENCES

[1] A. Inamdar, M. van Soestbergen, A. Mavinkurve, W. D. van Driel, and G. Q. Zhang, *Modelling thermomechanical degradation of moulded electronic packages using physics-based digital twin*, *Microelectronics Reliability*, vol. 157, p. 115 416, Jun. 2024, ISSN: 00262714 (Cited on p. 71).

[2] A. Inamdar, W. D. Van Driel, and G. Zhang, *Electronics packaging materials and component-level degradation monitoring*, *Frontiers in Electronics*, vol. 6, p. 1 506 112, Jan. 2025, ISSN: 2673-5857 (Cited on p. 71).

[3] A. Inamdar, M. van Soestbergen, A. Mavinkurve, W. D. van Driel, and G. Q. Zhang, *A Continuously Updated Package-Degradation Model reflecting Thermomechanical Changes at Different Thermo-Oxidative Stages of Moulding Compound*, in *24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2023*, Institute of Electrical and Electronics Engineers Inc., Apr. 2023, ISBN: 9798350345971 (Cited on p. 71).

[4] S. Segars, *Arm Partners Have Shipped 200 Billion Chips*, Oct. 2021 (Cited on p. 72).

[5] Yole Intelligence, *Semiconductor Trends in Automotive 2022*, Oct. 2022 (Cited on p. 72).

[6] Precedence Research, *Medical Electronics Market Size to Hit USD 248.43 Billion*, Dec. 2021 (Cited on p. 72).

[7] Automotive Electronics Council, *AEC-Q100-Rev-H Failure Mechanism based Stress Test Qualification for Integrated Circuits*, 2014 (Cited on p. 72).

[8] R. C. Chu, R. E. Simons, M. Iyengar, and L.-T. Yeh, *Thermal Management of Flip Chip Packages*, in *Advanced Flip Chip Packaging*, Tong Ho-Ming, Lai Yi-Shao, and Wong C.P., Eds., vol. 9781441957, Springer, Boston, MA, Aug. 2013, ch. 9, pp. 413–469 (Cited on p. 72).

[9] M. J. Mullins, D. Liu, and H. J. Sue, *Mechanical Properties of Thermosets*, in *Thermosets: Structure, Properties and Applications*, Q. Guo, Ed., Woodhead Publishing, 2012, ch. 2, pp. 28–61, ISBN: 9780857090867 (Cited on p. 72).

[10] D. Carolan, A. Ivankovic, A. J. Kinloch, S. Sprenger, and A. C. Taylor, *Toughening of epoxy-based hybrid nanocomposites*, *Polymer*, vol. 97, pp. 179–190, Aug. 2016, ISSN: 0032-3861 (Cited on p. 72).

[11] H. Ardebili, Jiawei Zhang, and M. G. Pecht, *Encapsulation Technologies for Electronic Applications*, Second. Elsevier, 2018, pp. 1–498, ISBN: 9780128119785 (Cited on p. 72).

[12] A. Mavinkurve, L. Goumans, and J. Martens, *Epoxy molding compounds for high temperature applications*, in *2013 Eurpoean Microelectronics Packaging Conference (EMPC)*, 2013, pp. 1–7 (Cited on pp. 72, 74, 79, 83).

[13] P. Lall, S. Deshpande, Y. Luo, M. Bozack, L. Nguyen, and M. Murtuza, *Degradation mechanisms in electronic mold compounds subjected to high temperature in neighborhood of 200°C*, in *Proceedings - Electronic Components and Technology Conference*, Institute of Electrical and Electronics Engineers Inc., Sep. 2014, pp. 242–254, ISBN: 9781479924073 (Cited on pp. 72, 74).

[14] J. De Vreugd, *The effect of aging on molding compound properties*, Ph.D. dissertation, Delft University of Technology, Jun. 2011 (Cited on pp. 72, 74).

[15] B. Zhang, *Material Characterization, Modelling and Simulation of Epoxy Moulding Compounds under High Temperature Storage and Temperature Cycling Thermal Ageing*, Ph.D. dissertation, Universität der Bundeswehr München, Nov. 2020 (Cited on pp. 72–75, 88).

[16] G. M. Odegard and A. Bandyopadhyay, *Physical aging of epoxy polymers and their composites*, *Journal of Polymer Science Part B: Polymer Physics*, vol. 49, no. 24, pp. 1695–1716, Dec. 2011, ISSN: 1099-0488 (Cited on p. 72).

[17] Y. Liu, *Power Electronic Packaging*. Springer New York, 2012 (Cited on p. 72).

[18] S. P. Phansalkar, C. Kim, and B. Han, *Effect of critical properties of epoxy molding compound on warpage prediction: A critical review*, *Microelectronics Reliability*, vol. 130, p. 114 480, Mar. 2022, ISSN: 0026-2714 (Cited on p. 72).

[19] E. Nguegang, *Experimental and Simulation-based Investigations on the Influence of Thermal Aging and Humidity on the Warpage of Molded Plastic Packages*, Ph.D. dissertation, University of Stuttgart, Apr. 2013, ISBN: 9783736943797 (Cited on pp. 73, 74, 76).

[20] A. Quintana and M. C. Celina, *Overview of DLO modeling and approaches to predict heterogeneous oxidative polymer degradation*, *Polymer Degradation and Stability*, vol. 149, pp. 173–191, Mar. 2018, ISSN: 01413910 (Cited on pp. 73, 75).

[21] A. Inamdar, Y.-H. Yang, A. Prisacaru, P. Gromala, and B. Han, *High temperature aging of epoxy-based molding compound and its effect on mechanical behavior of molded electronic package*, *Polymer Degradation and Stability*, vol. 188, 2021, ISSN: 01413910 (Cited on pp. 73, 74).

[22] L. Grandi and M. Rovitto, *Thermal Aging on Molding Compounds: Material Characterization and Modeling*, in *2022 23rd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2022*, Institute of Electrical and Electronics Engineers Inc., 2022, ISBN: 9781665458368 (Cited on pp. 73, 87).

[23] A. Inamdar, P. Gromala, A. Prisacaru, A. Kabakchiev, Y. Yang, and B. Han, *EMC Oxidation Under High-Temperature Aging*, in *Reliability of Organic Compounds in Microelectronics and Optoelectronics: From Physics-of-Failure to Physics-of-Degradation*, W. van Driel and M. Mehr, Eds., Springer, Cham, 2022, pp. 53–80, ISBN: 9783030815769 (Cited on p. 74).

[24] M. C. Celina, A. R. Dayile, and A. Quintana, *A perspective on the inherent oxidation sensitivity of epoxy materials*, *Polymer*, vol. 54, no. 13, pp. 3290–3296, Jun. 2013, ISSN: 0032-3861 (Cited on p. 75).

[25] M. C. Celina and A. Quintana, *Oxygen diffusivity and permeation through polymers at elevated temperature*, *Polymer*, vol. 150, pp. 326–342, Aug. 2018, ISSN: 0032-3861 (Cited on p. 75).

[26] A. V. Cunliffe and A. Davis, *Photo-oxidation of thick polymer samples—Part II: The influence of oxygen diffusion on the natural and artificial weathering of polyolefins*, *Polymer Degradation and Stability*, vol. 4, no. 1, pp. 17–37, Jan. 1982, ISSN: 0141-3910 (Cited on p. 75).

[27] K. Jansen, *Thermomechanical modeling and characterization of polymers*. TU Delft, 2007 (Cited on p. 80).

[28] A. Lukichev, *Physical meaning of the stretched exponential Kohlrausch function*, *Physics Letters A*, vol. 383, no. 24, pp. 2983–2987, Aug. 2019, ISSN: 0375-9601 (Cited on p. 81).

[29] T. W. Clyne, *Residual Stresses in Surface Coatings and Their Effects on Interfacial Debonding*, *Key Engineering Materials*, vol. 116-117, pp. 307–330, Dec. 1995, ISSN: 1662-9795 (Cited on p. 82).

[30] K. M. Jansen, D. J. Van Dijk, and M. H. Husselman, *Effect of processing conditions on shrinkage in injection molding*, *Polymer Engineering & Science*, vol. 38, no. 5, pp. 838–846, May 1998, ISSN: 1548-2634 (Cited on p. 84).

[31] X. Peng, J. Xu, Y. Cheng, L. Zhang, J. Yang, and Y. Li, *An Analytical Model for Cure-Induced Deformation of Composite Laminates*, *Polymers*, vol. 14, no. 14, p. 2903, Jul. 2022, ISSN: 2073-4360 (Cited on p. 84).

[32] M. Y. Lin, Y. J. Zeng, S. J. Hwang, M. H. Wang, H. P. Liu, and C. L. Fang, *Warpage and residual stress analyses of post-mold cure process of IC packages*, *International Journal of Advanced Manufacturing Technology*, vol. 124, no. 3, pp. 1017–1039, Jan. 2022, ISSN: 14333015 (Cited on p. 84).

[33] D. S. Choi and Y. T. Im, *Prediction of shrinkage and warpage in consideration of residual stress in integrated simulation of injection molding*, *Composite Structures*, vol. 47, no. 1-4, pp. 655–665, Dec. 1999, ISSN: 0263-8223 (Cited on p. 84).

[34] C. C. Lee, C. C. Lee, and C. P. Chang, *Simulation methodology development of warpage estimation for epoxy molding compound under considerations of stress relaxation characteristics and curing conditions applied in semiconductor packaging*, *Materials Science in Semiconductor Processing*, vol. 145, p. 106 637, Jul. 2022, ISSN: 1369-8001 (Cited on pp. 84, 85).

[35] H. C. Cheng and Y. C. Liu, *Warpage characterization of molded wafer for fan-out wafer-level packaging*, *Journal of Electronic Packaging, Transactions of the ASME*, vol. 142, no. 1, Mar. 2020, ISSN: 15289044 (Cited on p. 84).

[36] H. C. Cheng, Z. D. Wu, and Y. C. Liu, *Viscoelastic Warpage Modeling of Fan-Out Wafer-Level Packaging during Wafer-Level Mold Cure Process*, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 7, pp. 1240–1250, Jul. 2020, ISSN: 21563985 (Cited on p. 84).

[37] A. R. Adli and K. M. Jansen, *Numerical investigation and experimental validation of residual stresses building up in microelectronics packaging*, *Microelectronics Reliability*, vol. 62, pp. 26–38, Jul. 2016, ISSN: 0026-2714 (Cited on p. 84).

[38] A. Rezaie Adli, *Numerical Analysis and Experimental Verification of Stresses Building up in Microelectronics Packaging*, Ph.D. dissertation, Delft University of Technology, Jan. 2017, ISBN: 9789461867773 (Cited on p. 85).

[39] Y. Nawab, X. Tardif, N. Boyard, V. Sobotka, P. Casari, and F. Jacquemin, *Determination and modelling of the cure shrinkage of epoxy vinylester resin and associated composites by considering thermal gradients*, *Composites Science and Technology*, vol. 73, no. 1, pp. 81–87, Nov. 2012, ISSN: 02663538 (Cited on p. 85).

[40] L. Olivier, C. Baudet, D. Bertheau, J. C. Grandidier, and M. C. Lafarie-Frenot, *Development of experimental, theoretical and numerical tools for studying thermo-oxidation of CFRP composites*, *Composites Part A: Applied Science and Manufacturing*, vol. 40, no. 8, pp. 1008–1016, Aug. 2009, ISSN: 1359-835X (Cited on p. 86).

[41] L. Ernst, *Refreshing Fracture Mechanics and High Temperature Aging of EMC*, in *Internal presentation (NXP Semiconductors)*, 2016 (Cited on p. 87).

[42] J. De Vreugd, K. M. Jansen, L. J. Ernst, C. Bohm, and R. Pufall, *High temperature storage influence on molding compound properties*, in *2010 11th International Conference on Thermal, Mechanical and Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems, EuroSimE 2010*, 2010, ISBN: 9781424470266 (Cited on pp. 87, 88).

[43] J. De Vreugd *et al.*, *Effect of postcure and thermal aging on molding compound properties*, in *Proceedings of the Electronic Packaging Technology Conference, EPTC*, 2009, pp. 342–347, ISBN: 9781424451005 (Cited on p. 88).

[44] B. Zhang *et al.*, *Modelling of thermal aging of moulding compound by using an equivalent layer assumption*, in *2017 18th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2017*, Institute of Electrical and Electronics Engineers Inc., May 2017, ISBN: 9781509043446 (Cited on p. 88).

[45] W. D. Van Driel, J. H. Janssen, G. Q. Zhang, D. G. Yang, and L. J. Ernst, *Packaging Induced Die Stresses - Effect of Chip Anisotropy and Time-Dependent Behavior of a Molding Compound*, *Journal of Electronic Packaging*, vol. 125, no. 4, pp. 520–526, Dec. 2003, ISSN: 1043-7398 (Cited on p. 97).

5

In-situ Monitoring for Data-driven Digital Twins

Mechanical failure of solder joints is one of the most common board-level failure modes in electronic components. It is crucial for a next-generation reliability assessment method to have an in-situ health monitoring system in place to evaluate the current state of component degradation. This is achieved by specialised embedded sensors and data processing on the edge. This chapter focuses on monitoring the mechanical degradation of the package-to-PCB board-level solder interconnects of a Wafer-Level Chip-Scale Package (WLCSP) using a high-resolution piezoresistive sensor. First, a measurement workflow was set up to optimise and significantly improve the readout time of the sensor containing a 70×30 matrix of piezoresistive cells. Then, utilising a design of experiments, the test specimens were subjected to certain combinations of mechanical and thermal loads in a four-point bending setup. Temperature-coupled mechanical loading showed a greater impact on the resulting stress pattern compared to that of a superposition of the corresponding individual purely thermal and mechanical load configurations. Finally, the specimens were tested under a purely mechanical load until failure, and a correlation between the recorded stress pattern and the initiation and propagation of a crack was established.

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5.1. Introduction

Electronic components undergo degradation under the environmental and operating loads, which leads to package-level and board-level failures. These failures occur either due to an event of a sudden change in loads (such as excess temperature, excess current or voltage, mechanical shock, stress or impact) or a prolonged exposure to nominal operating conditions. About 70% of the failures in electronic components occur during the packaging process, and the predominant failure mode is associated with the solder joints [3]. Temperature, humidity, mechanical vibrations, and dust are the four key environmental factors that are responsible for component degradation, in which the temperature factor is the most dominant one [4] and is responsible for about 55% of the failures; whereas mechanical vibrations contribute to about 20% of the failures [5]. Failures related to semiconductors, connectors, and solder joints together account for over one-third of the share for power electronics [6]. A solder joint failure is primarily governed by the variation of temperature and mechanical loads [7, 8]. Thus, it is one of the key aspects of reliability engineering for IC packages and electronics-enabled systems.

For mission-critical electronics, it is crucial to predict a failure before it occurs. Therefore, it has become increasingly important to have a continuous health monitoring system in place to evaluate the current state of component degradation during its operational lifetime. The two-branched Digital Twin-based approach to PHM (as indicated in Figure 2.8) can realise this. Its second, data-driven, aspect is more prominent in the 'aggregate' phase (*i.e.*, DTA) and relies primarily on the data input from the operating phase of electronic components. This can be achieved by in-situ measurements using embedded sensors and processing the data on the edge. Thus, there is a need to develop and utilise specialised sensors and data processing workflows for in-situ data-driven condition monitoring.

There are a few established ways for condition-monitoring of solder joints, such as DC resistance measurement, Radio Frequency (RF) impedance measurement, Multivariate State Estimation Technique (MSET), and Sequential Probability Ratio Test (SPRT) [9–11]. Electrical resistance measurement along a path formed by a daisy chain of solder joints is one of the most common ones. This method can detect a mechanical failure (and also monitor several stages of degradation [12]). However, it fails to get precise, localised information of the failed solder joint. Another drawback is that the fractured interconnect may remain undetected for a longer time due to maintained spring contact [13]. On the other hand, active devices based on the piezoresistive effect can provide more localised details [14–16]. Yet, such an implementation generally has to make a tradeoff between more piezoresistive cells and faster data collection, since a single measurement can typically be a lot slower.

This chapter addresses this challenge by utilising a piezoresistive sensor with a much higher spatial resolution (2100 piezoresistive cells, arranged in a 70×30 matrix) than others reported in the literature [17–23] for monitoring the mechanical degradation of package-to-PCB solder interconnects. First, an efficient software workflow was specifically designed to optimise the sensor readout time and achieve recording a set of data from all the cells under five minutes. Then, a Design of Experiments (DoE) with a four-point bending setup was utilised to study the effect of a combination of mechanical and thermal loads on the sensitivity of the sensor readouts. Finally, the test specimens were subjected to a purely mechanical loading condition until a failure was observed. Based on the experimental data, a correlation between the stress pattern at the die, which sits right above the two solder bumps, and the corresponding state of solder crack initiation and propagation was established.

5.2. STRESS SENSING

The selected piezoresistive sensor consists of an N-type mono-doping resistance piezoresistive module with 2100 cells that are arranged in a 70×30 matrix. Each cell has a size of 10 µm×10 µm, and thus, the whole sensor collectively provides a high spatial resolution. This sensor module (*i.e.*, the semiconductor die) is packaged in a test component and then assembled on a PCB using the Surface Mount Technology (SMT) process. For this study, the sensor was packaged in a Wafer-Level Chip-Scale Package (WLCSP), where the die and the solder bumps are very close to each other, with only a few Back-End of Line (BEOL) layers between them. This assembly allows the sensor to record mechanical deformations adjacent to the top surface of the solder joints. Figure 5.1 shows the schematics of the piezoresistive sensor module. Its 2100 cells are indicated by the rectangular grid, and the footprint of solder bumps (circular and dashed lines) and the BEOL layers (light grey lines) are also indicated.

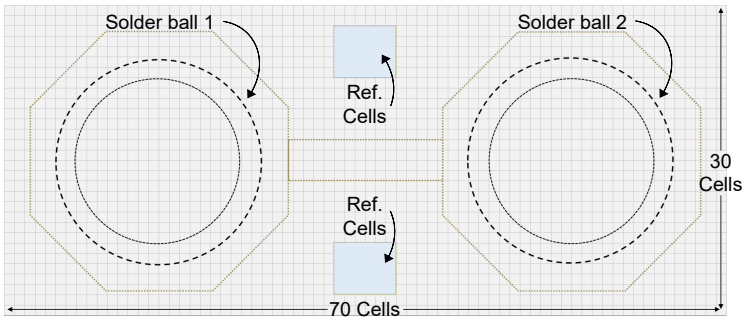


Figure 5.1: The distribution of 2100 piezoresistive cells above the two solder bumps of the WLCSP test specimen. The two light-blue regions, located not too close to either of the solder joints, the metal pad, and the package edge, are considered as 'reference' cells to calculate the relative change in resistance.

When the test specimen is subjected to thermal loads, it deforms due to a mismatch in the Coefficient of Thermal Expansion (CTE) of different sub-layers. Similarly, a mechanical load, static or dynamic, leads to (plastic) deformation and damage accumulation. The deformation causes a change in the length of the piezoresistive path, and hence, changes its resistance. This change can be measured by correlating it to the change in current or voltage. Moreover, the relative change in the resistivity ($\Delta\rho/\rho$), or for crystalline semiconductors, the resistance ($\Delta R/R$), and the normal stress components (σ_{xx}, σ_{yy}, σ_{zz}) can be expressed as a linear combination of each other, scaled using a set of piezoresistive coefficients [16, 24–26]. One such possible form is indicated in Equation (5.1), where π_L denotes the longitudinal, π_T the transverse, and π_{out} the out-of-plane piezoresistive coefficient, respectively.

$$\frac{\Delta R}{R} = \pi_L \, \sigma_{xx} + \pi_T \, \sigma_{yy} + \pi_{out} \, \sigma_{zz} \tag{5.1}$$

In this way, the data recorded by the piezoresistive cells arranged in a matrix can provide a correlation to the map of stress distribution across the surface of the die. The two blocks of 30 cells marked as 'reference cells' in Figure 5.1 are used later to process the recorded data and visualise the changes in stress distribution corresponding to only the post-SMT loading conditions. A previous version of this sensor was utilised in [15], which reports that a single measurement (from all 2100 cells) takes up to 50 minutes. This duration is extremely lengthy for degradation monitoring during Board-Level Reliability (BLR) tests and needs to be optimised.

5.2.1. Sensor Readout Optimisation

To obtain the stress distribution across the entire surface of the die, all 2100 piezoresistive cells need to be accessed one by one by address selection, followed by data processing. Due to the large number of cells, the individual cell-readout becomes the bottleneck in the measurement workflow. To address this, an intermediate 'adapter PCB' was designed and utilised to connect the piezoresistive sensor with a microprocessor unit, which sends data to a computer that controls, collects, processes, and stores the data. The setup also utilises a Source Measurement Unit (SMU) to control the input current and voltage. Figure 5.2 indicates the measurement setup and workflow, including the annotations for different ports on the adapter PCB.

A unique addressing technique was engineered to use a 100-bit address signal to access all 2100 cells. Only when both the row and the column switches are active (set to '1'), the 'force' and 'sense' ports are connected to the desired piezoresistive cell. A Python program was utilised to handle the address allocation. A stable power supply of 3.3 V was managed and maintained by enabling one DC voltage value with the Python program, which communicates with SMU using *PyVISA* library [27].

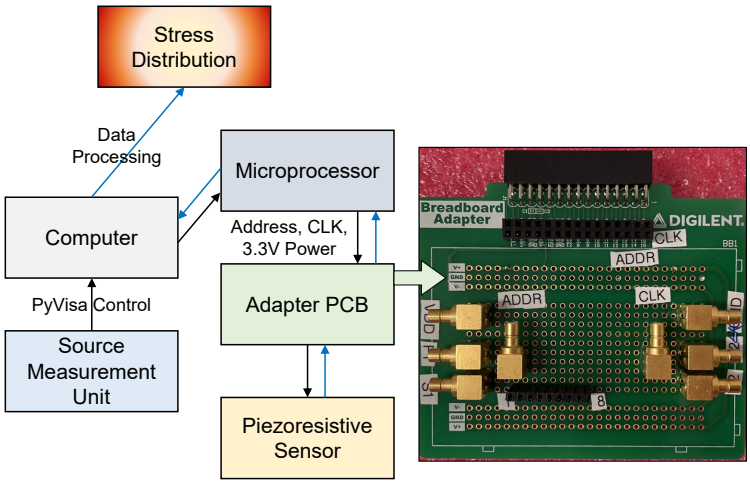


Figure 5.2: The flowchart for recording measurements from the piezoresistive sensor. The adapter PCB has several ports for governing certain signals that are an essential part of the measurement workflow.

5

Sending the Standard Commands for Programmable Instruments (SCPI) commands initialises the SMU, setting it to source current while measuring voltage [28]. The finalised measurement algorithm first selects a cell to measure and acquire its column number m and row number n. Next, it gives the DC voltage supply between *VDD* and *GND* and feeds the *CLK* port (corresponding to the clock) with a 100-cycle square signal. Then, it feeds the address signal simultaneously with the clock signal from *ADDR* port, with only the numbers m and $(70 + n)$ of the address signal set to '1' and the rest to '0'. It then sends a current of 50 µA and measures the voltage between the two sense ports. Finally, it calculates the current value of resistance based on the measured voltage and known input current and stores the result. This entire process is repeated until all 2100 cells are accessed.

The measurement workflow was further improved by implementing a waveform correction to optimise the clock signal frequency. To ensure the accuracy and reliability of the measurements, a repeatability test was also included in the Python code. With these optimisation steps, a single measurement from all 2100 cells takes less than five minutes, achieving a significant reduction in the measurement time.

5.2.2. SENSOR DATA PROCESSING

The optimised measurement workflow generates data when the test specimens with piezoresistive sensors are subjected to thermal or mechanical load. However, the sensor still shows non-zero default values under no load, due to the pre-stress resulting from packaging and SMT processes. To record the changes corresponding to the applied load (*i.e.*, a relative change), a data processing step must be in place.

To achieve this, two blocks of 30 cells (indicated in Figure 5.1) are selected as reference cells. The conductance values are calculated using the reciprocal values of the measured resistance. Then, the reference conductance value is obtained from the reference cells. The choice of these cell-blocks is made such that they are not too close to either of the solder joints. The average value of the selected 60 cells is used as the reference value for calculating the relative change under the applied load. Thus, at any loaded stage, the algorithm first calculates and plots all 2100 values relative to the average reference value. Each cell is then assigned a colour based on the relative conductance value to form a gradient, in which red signifies a positive value, yellow the zero, and green a negative value. This results in a spatial plot with a clear gradient and the noise eliminated. Figure 5.3 shows an example of the difference between a spatial plot of absolute values and that of relative values. The plots correspond to a state after 50 thermal cycles relative to the first cycle.

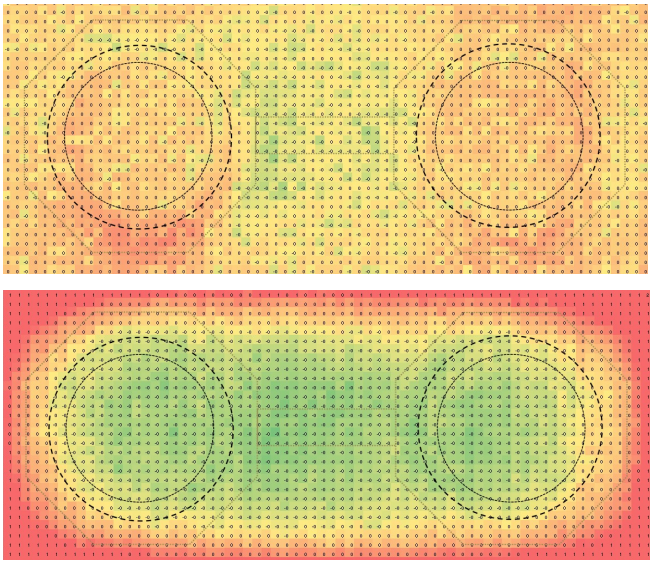


Figure 5.3: The qualitative comparison of the conductance data recorded at the 50^{th} cycle of a thermal cyclic load. The plot above represents absolute values, while the one below represents relative values. The plot with relative values provides a much better insight into the changes in the stress distribution.

The plots with relative values provide a much better insight into the changes due to the applied load. Using the $\Delta R/R$ values from each cell and the literature-reported values of the piezoresistive coefficients [18, 26, 29, 30], a correlation between the linear combination of normal stress components and the measurement data can be established (Equation (5.1)). To evaluate individual stress components, a simulation-assisted verification approach can be employed [31]. Thus, the spatial plots obtained using relative values can also give a much clearer idea of the stress distribution.

5.3. Temperature-Coupled Bend Test

The piezoresistive sensor with the optimised measurement algorithm was first tested in a temperature-coupled mechanical bend test environment. This is an important intermediate step to characterise and test the component against a static thermal and mechanical load before utilising it in BLR tests, which typically consider dynamic loads such as thermal cycling and mechanical vibrations. In this test, the state of solder joint degradation was monitored under a combination of isothermal conditions and static mechanical loads.

5.3.1. Experimental Setup

A four-point bending setup equipped with a temperature chamber was utilised to characterise the piezoresistive sensor under a combination of thermal and mechanical loads. Figure 5.4 shows the schematics of the four-point bending setup annotated with the dimensions (*viz.*, d_1, d_2, b, h) and point force F, relevant for designing the experiments. A load span of 30 mm (*i.e.*, $d_1 = 15$ mm) and a support span of 66 mm (*i.e.*, $d_2 = 33$ mm) were utilised. A PCB with a WLCSP equipped with piezoresistive sensors was utilised as the test specimen, such that the package is facing downwards. Due to this orientation, the recorded piezoresistive data matrix needs to be flipped horizontally, *i.e.*, along the shorter edge, before further analysis.

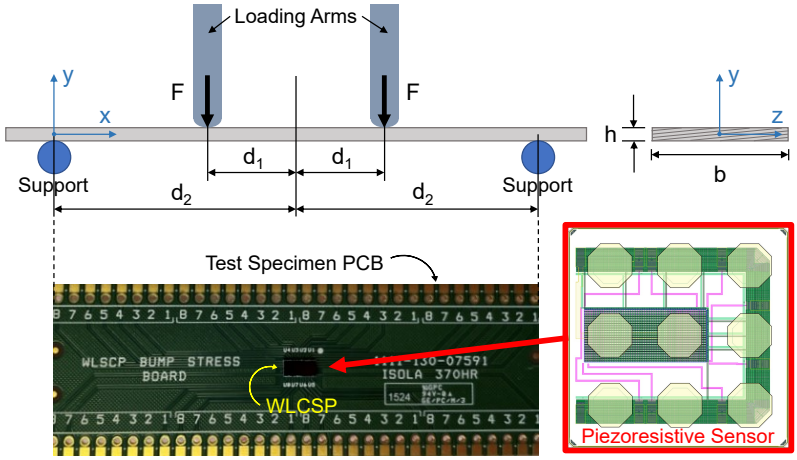


Figure 5.4: The schematics of the experimental setup for four-point bending with temperature variation. The test specimen PCB has a WLCSP placed centrally and equipped with the piezoresistive sensor.

According to the bending equations and beam theory, the bending moment remains constant between the two loading arms at a constant applied static force F. The Euler-Bernoulli beam equations (suitable for thin beams) lead to the expression in Equation (5.2) for the maximum bending stress, which occurs at the top-most and

bottom-most layer of the beam. The shear force is non-zero (and constant) only in the two regions between a support and a loading arm, and the maximum shear stress (at the neutral axis of the beam) is given by Equation (5.3). The maximum bending displacement (v_{max}) at the centre of the beam-span is given by Equation (5.4), where E_x is the modulus of elasticity along the x-direction. The displacement v_{max} was considered as a control parameter for applying different mechanical load-steps.

$$(\sigma_{xx})_{max} = \frac{6}{bh^2} F\,(d_2 - d_1) \tag{5.2}$$

$$(\tau_{xy})_{max} = \frac{3F}{2bh} \tag{5.3}$$

$$v_{max} = \frac{2F}{E_x bh^3}\,(d_2 - d_1)\,(2{d_2}^2 + 2d_1 d_2 - {d_1}^2) \tag{5.4}$$

5

5.3.2. Test Specimen

A PCB of the size 84 mm×29 mm was utilised as the test specimen for the four-point bending experiment. For this study, a single wafer-level chip-scale package containing multiple piezoresistive sensor modules was utilised and assembled on the test specimen PCB. Figure 5.5 shows the layout of the die in the WLCSP test package that contains 8 piezoresistive sensor modules arranged in a 4×2 grid fashion. Each unit consists of a total of 9 solder joints. The piezoresistive sensor sits above 2 of those solder joints, while the rest are dedicated to circuit connections.

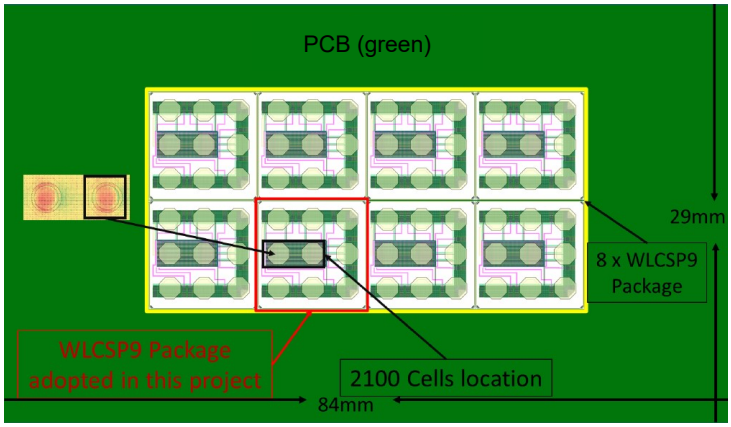


Figure 5.5: The layout of the die in the WLCSP test package that contains 8 piezoresistive sensor modules (with different doping) arranged in a 4×2 grid. The module utilised for recording the measurements in this study is indicated with a red square along with the position of the stress sensor within.

Seven of the 8 units on the die feature different piezoresistive modules, providing diverse types of methods for evaluating stress distribution (such as resistance, current factor for Metal Oxide Semiconductor (MOS), and saturation collector current for bipolar transistors). Figure 5.5 highlights the location of the single unit that was utilised for the data collection and characterisation experiments in this study.

5.3.3. Loading Conditions

A design of experiments was prepared to expose the test specimen to various combinations of thermal and mechanical loads. The DoE considers 11 different temperature steps and 4 distinct mechanical displacements (including the zero displacement). The specimen was exposed to a static mechanical load equivalent of a 0 mm, 0.5 mm, 0.75 mm, and 1.1 mm of bending displacement (v_{max}), along with an isothermal load of different ambient temperature values between −40 °C to 125 °C (*viz.*, -40, -20, 0, 10, 25, 30, 45, 65, 85, 105, and 125 °C). The change in resistance was recorded by the piezoresistive sensor embedded in the WLCSP at various load conditions, and the previously described data processing workflow was followed.

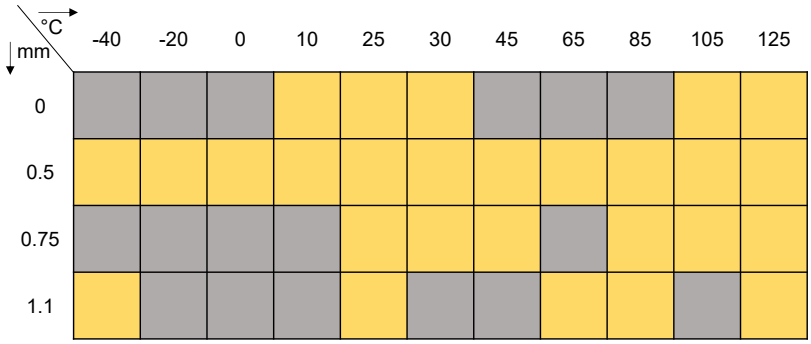


Figure 5.6: The design space considered for the temperature-coupled bend test. The rows indicate maximum displacement v_{max} (mm), while the columns indicate the temperature (°C). The yellow squares indicate the final combinations for which the data were recorded within this design of experiments.

Figure 5.6 summarises the DoE and highlights in yellow all the combinations for which data were recorded. A select number of combinations could be covered due to practical limitations. During the test, the PCB was first bent, and then the chamber temperature was adjusted in order to minimise the amount of repeated bending. After each temperature cycle at a certain displacement, the motor was reset to the zero displacement position before commencing the next cycle. A complete spectrum of displacements at 25 °C (room temperature) and 125 °C was captured. Similarly, data for all temperature steps at 0.5 mm displacement were collected.

5.3.4. Data Processing and Analysis

The recorded data was processed utilising the blocks of 'reference cells' for each reading, as discussed in previous sections. Furthermore, the conductance change was plotted relative to the reference state of room temperature (25 °C) and zero displacement, *i.e.*, the (25 °C, 0 mm) combination. The resulting plots of all yellow squares in Figure 5.6 (except the reference state) were analysed, and the following two key observations were recorded.

(1) Patterns of thermal expansion mismatch:

Initially, only the effect of temperature variation was studied. Figure 5.7 shows the evolution of the recorded pattern over the considered temperature range (all subplots are rotated 90° counterclockwise) with a bending displacement of 0.5 mm.

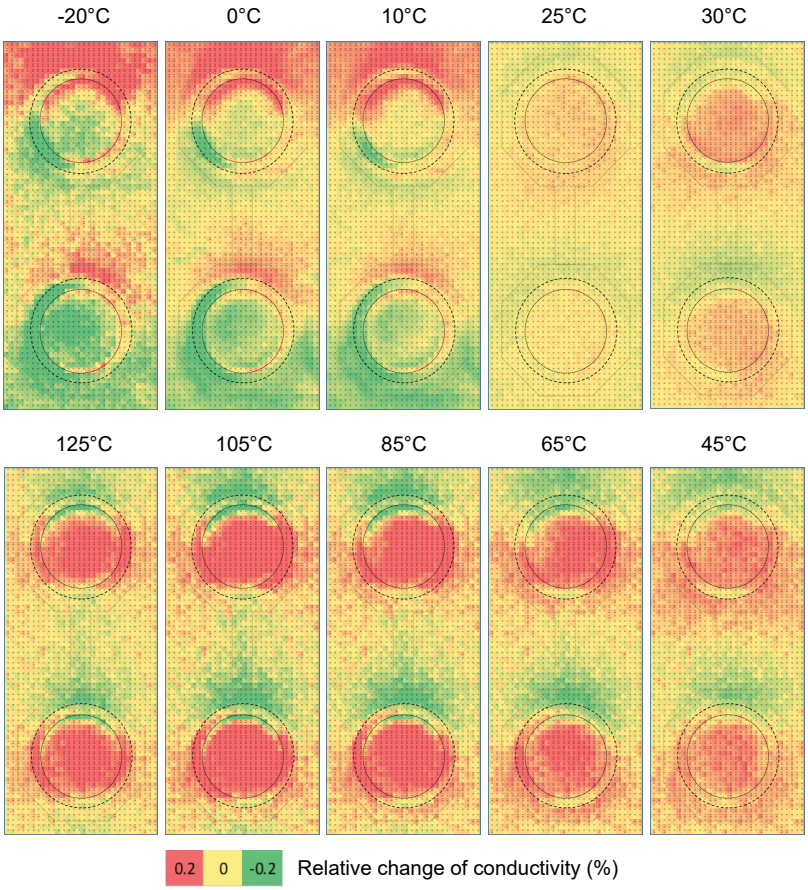


Figure 5.7: The evolution of the piezoresistive sensor measurements (*i.e.*, the relative change of conductance) over the considered temperature range and with a maintained bending displacement of 0.5 mm.

A significant change in the stress pattern is observed from low to high temperature values. The region under the left bump (bottom in the figure) first recovers from the green shade with the increasing temperature and then turns red. This sign change of conductance signifies the change in direction of the mechanical stress components, predominantly the bending stress in axial direction (*i.e.*, σ_{xx}).

It is evident that this occurs due to out-of-plane deformation caused by the mismatch in thermal expansion (CTE-mismatch) of the different involved materials. At low temperatures, the solder joint can stretch the die towards the centre of the die; whereas at high temperatures, the stretch is in the other direction. In addition to showing the changes in the effective stress pattern, this enables visualising the warpage behaviour of the die/package under the influence of temperature variation.

(2) Higher sensitivity towards a combined loading:

The effect of purely mechanical load was also studied using the configurations corresponding to the columns corresponding to 25 °C and 125 °C in Figure 5.6. Neither of the two cases showed a significant change in the recorded pattern. For the four cases corresponding to 25 °C, the change from 0 mm to 1.1 mm displacement was nearly linear, whereas all non-zero displacement configurations corresponding to 125 °C showed nearly the same pattern. This indicates a non-linear relationship at higher temperatures, where the recorded pattern first shows significant changes at smaller displacements but then remains nearly unchanged.

The effect of a combined thermal and mechanical load was also studied by comparing it with their individual effects. Figure 5.8 shows this comparison for the configuration for 125 °C and 1.1 mm bending displacement. The top subfigure refers to the aforementioned combined loading. An artificial superposition of the two configurations (125 °C, 0 mm) and (25 °C, 1.1 mm) was created using the sum of the values in each corresponding cell of their recorded patterns. This is depicted in the bottom subfigure of Figure 5.8. A pattern with values slightly more towards both extremes was observed for the combined load. This can be visually confirmed from the marginally darker shades of red and green in the first pattern (top) in Figure 5.8.

Out of the total of 290 full cells within the footprint of the right solder ball (*i.e.*, the outer dashed circle on the right), close to 50% of the cells show an increase in the relative conductance change (measured in percentage) by 0.1 (where the total range is from -0.5 to +0.5). It indicates that a coupled thermal and mechanical load results in a more severe stressed state than the superposition of the individual effects. As electronic components are often subjected to multiple simultaneous environmental and operating loads [32], an in-situ measurement provides much more accurate and valuable information about the thermomechanical stresses within the component.

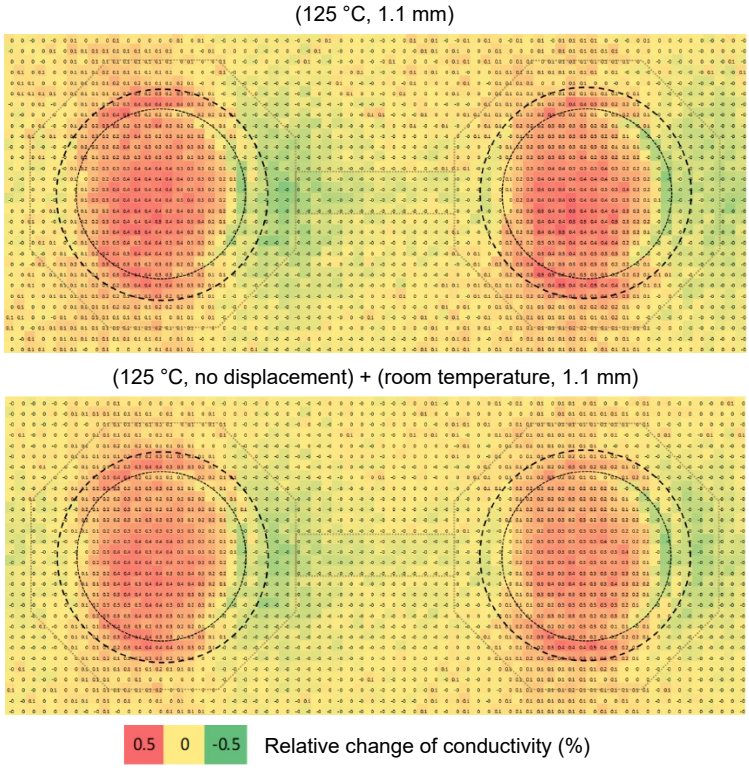


Figure 5.8: The comparison of the spatial plots obtained from a temperature-coupled bend test configuration (top) with that of a superposition of corresponding individual purely thermal and mechanical load configurations (bottom). The combined load configuration shows a slightly more stressed state.

5.4. Mechanical Bend-Test until Failure

The temperature-coupled bend test included mechanical loads equivalent to up to 1.1 mm of bending displacement, which did not show a significant change in the recorded pattern. Thus, a purely mechanical bend test at room temperature (25 °C) was carried out until a failure in solder joints was observed. The same four-point bending setup and measurement workflow were utilised. The considered $v_{\max}$ values range from 0.5 mm to 10 mm. After reaching each selected displacement, the fixture maintained that position until two measurements were conducted. Collected data was processed and analysed relative to the 0 mm displacement configuration.

In order to have an effective comparison, a path formed by a single row (number 15 from the top) of cells was selected, which coincides with the horizontal diameters of both solder bumps. The change in conductance was plotted for all cells along this path, and this was repeated for all the considered displacement values.

Figure 5.9 shows the comparison of the obtained plots. The plots gradually move down until $\nu_{max} = 3\,mm$, and then a trend reversal is observed, which is indicated by yellow arrows in Figure 5.9. Moreover, a peculiar fluctuation in values was also observed between column numbers 45 and 50 (highlighted with a red rectangle in Figure 5.9) in the plots corresponding to displacements larger than 3.5 mm. This location is the inner edge of the right solder joint.

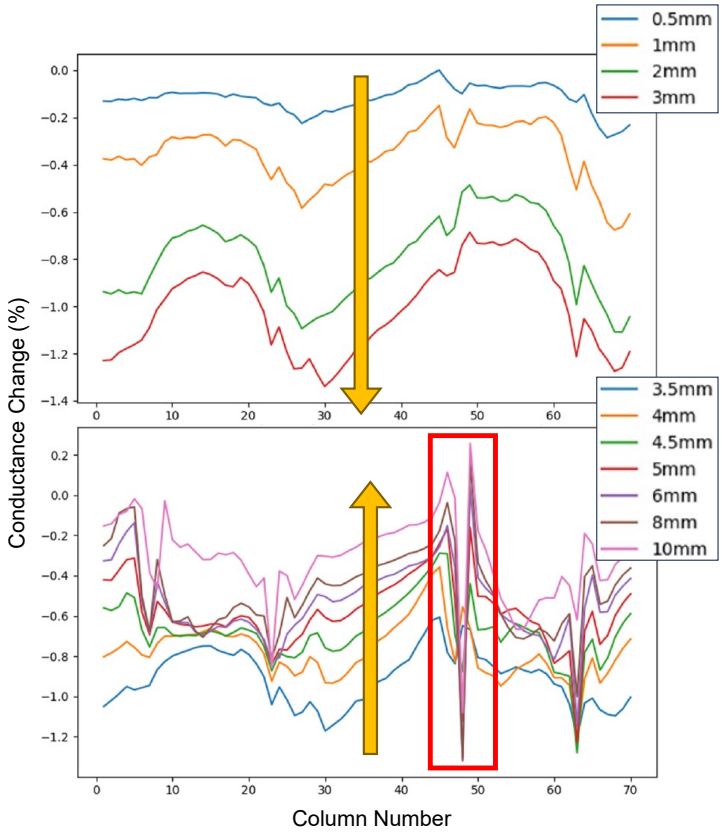


Figure 5.9: Plots of the conductance change along a path formed by a single row (number 15 from the top) of the piezoresistive cell matrix that coincides with the diameters of both solder bumps. A trend reversal (yellow arrows) is observed after 3 mm of bending displacement (ν_{max}), and a high fluctuation in readings (red rectangle) between column numbers 45 and 50 indicates the existence of a crack.

To investigate further, cross sections of the test specimen were studied under a SEM. A crack propagated in the region of the PCB-solder interface was observed. Thus, it was concluded that the sudden change in the trend of conductance data and the localised fluctuation of values correspond to the mechanical crack. The piezoresistive patterns, corresponding to mechanical stresses, change due to the release of surface energy during crack initiation and propagation.

Figure 5.10 shows the cross-section image observed under a SEM, and the location of the crack. The corresponding change in the recorded pattern before and after the crack initiation (v_{max} = 2 mm and 4 mm, respectively) are also indicated. It shows that a failure can be detected using the patterns generated by a piezoresistive sensor.

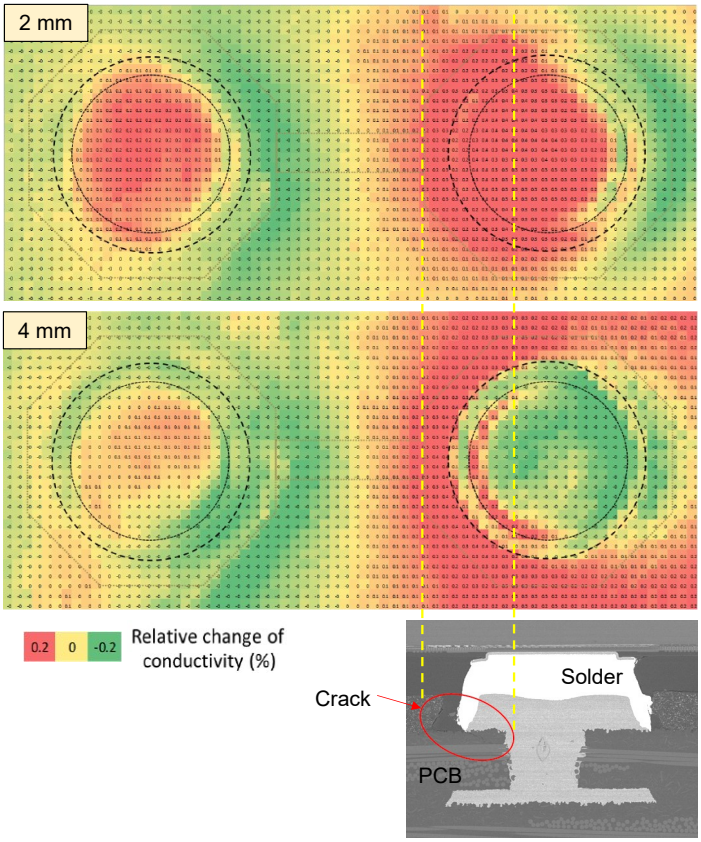


Figure 5.10: Spatial plots recorded by the piezoresistive sensor before and after the crack initiation (corresponding to the bending displacement of 2 mm and 4 mm, respectively). The cross section observed under a SEM indicates the crack position in the region next to the inner edge of the right solder bump.

Moreover, the patterns captured by the sensor at the stages before the crack was initiated were also further studied. They showed a concentration of extreme conductance values (hinting at stress concentration) around the inner edge of the right bump. This shows that the evolution of 'stress' patterns can serve as an indication of failure before it occurs.

Conclusion

This study utilises a piezoresistive sensor with a high spatial resolution of 70×30 cells. Due to the large number of cells, the sensor readout time can become the bottleneck in recording data during the BLR tests. Thus, an optimised workflow was developed to bring the complete readout time under five minutes. With the developed time-optimised measurement workflow, this sensor can be practically used for real-time health monitoring of microelectronics. Moreover, depending on the choice of packaging, it can enable monitoring of different layers of an electronic component, in the same way the unique construction of a WLCSP enabled in-situ monitoring of solder bumps in this work.

The spatial plots of conductance change provide more detailed and localised information compared to other condition monitoring techniques for solder joints. The spatial plots reflect the changes caused by applied loading conditions. A coupled thermal and mechanical load appears to have a greater impact on resulting stresses compared to an artificial superposition of the individual effects. This aspect underlines the importance of considering combined loading conditions in reliability testing and their significance in the calculation of component lifetime. This aspect can be further investigated by using additional combinations of coupled loads and by including additional loading factors, such as exposure to humidity.

The design of experiments involving a combined thermal and mechanical loading indicates that the mechanical stresses show more sensitivity towards temperature changes in the considered range than the mechanical loads (*i.e.*, bending displacements). Based on the recorded data, the mechanical stress components can be evaluated and visualised by processing the spatial plots of conductance change and utilising the literature-reported values of the piezoresistive coefficients. However, these coefficients should be validated for the chosen test specimen/device. This can be done in a simulation-assisted manner using a Finite Element-based model of the test specimen and correlating the stress values to the experimentally gathered data. This step is crucial while transitioning from the 'instance' to the 'aggregate' (*i.e.*, from DTP to DTA) phase of a Digital Twin.

The spatial plots obtained during the purely mechanical bend test with larger displacements not only helped in detecting a failure (*i.e.*, the crack initiation) but also in determining the location of the defect. This unique functionality of the piezoresistive sensor has great potential in applying an edge-based data-driven in-situ monitoring effectively for failure detection and prediction in the DTA phase of the two-branched Digital Twin-based PHM workflow.

REFERENCES

[1] A. Inamdar *et al.*, *Characterization of a Piezoresistive Sensor for In-Situ Health Monitoring of Solder Bumps*, in *IEEE 74th Electronic Components and Technology Conference (ECTC) 2024*, 2024 (Cited on p. 105).

[2] L. Zhang, *Characterization of Solder Joint Degradation under Board-level Reliability Tests for Vibration and Thermal Cycling*, Delft University of Technology, Tech. Rep., 2023 (Cited on p. 105).

[3] R. Tilgner, *Physics of failure for interconnect structures: an essay*, *Microsystem Technologies*, vol. 15, no. 1, Jan. 2009 (Cited on p. 106).

[4] X. Li, R. Sun, and Y. Wang, *A review of typical thermal fatigue failure models for solder joints of electronic components*, in *IOP Conference Series: Materials Science and Engineering*, vol. 242, IOP Publishing, Sep. 2017, p. 012 103 (Cited on p. 106).

[5] M. Pecht, *Handbook of Electronic Package Design*. 1991 (Cited on p. 106).

[6] E. Wolfgang, *Examples for failures in power electronics systems*, in *ECPE Tutorial on Reliability of Power Electronic Systems*, European Center for Power Electronics (ECPE), 2007, pp. - (Cited on p. 106).

[7] O. O. Ogbomo, E. H. Amalu, N. N. Ekere, and P. O. Olagbegi, *Effect of operating temperature on degradation of solder joints in crystalline silicon photovoltaic modules for improved reliability in hot climates*, *Solar Energy*, vol. 170, pp. 682–693, Aug. 2018, ISSN: 0038-092X (Cited on p. 106).

[8] F. Arabi, A. Gracia, J. Y. Delétage, and H. Frémont, *Effect of thermal and vibrational combined ageing on QFN terminal pads solder reliability*, *Microelectronics Reliability*, vol. 114, p. 113 883, Nov. 2020, ISSN: 0026-2714 (Cited on p. 106).

[9] Y. D. Lu, M. Wan, and B. Yao, *Degradation detecting of solder joints by time domain reflectometry technology*, in *Proceedings of 13th International Conference on Electronic Packaging Technology and High Density Packaging ICEPT-HDP 2012*, 2012, pp. 1344–1347, ISBN: 9781467316804 (Cited on p. 106).

[10] B. Yao, Y. Lu, and M. Wan, *A study of solder joint degradation and detection using RF impedance analysis*, in *Proceedings of International Symposium on Advanced Packaging Materials*, 2011, pp. 117–121, ISBN: 9781467301473 (Cited on p. 106).

[11] R. Jaai, M. Pecht, and J. Cook, *Detecting failure precursors in BGA solder joints*, in *Proceedings of 2009 Annual Reliability and Maintainability Symposium*, 2009, pp. 100–105, ISBN: 9781424425099 (Cited on p. 106).

[12] V. Thukral *et al.*, *AI-Enabled Board Level Vibration Testing: Unveiling The Physics of Degradation*, in *2024 IEEE International Test Conference (ITC)*, Institute of Electrical and Electronics Engineers Inc., 2024, pp. 436–444, ISBN: 9798331520137 (Cited on p. 106).

[13] A. Batra, L. Fang, and J. H. Constable, *Implementation of low-cost failure detection system using resistance spectroscopy*, in *Proceedings - Electronic Components and Technology Conference*, IEEE, Aug. 2003, pp. 933–939 (Cited on p. 106).

[14] M. Usui, M. Kuwahara, and T. Satoh, *A feasibility study on potential of stress sensors to detect solder joint defects toward prognostics of power modules*, *Microelectronics Reliability*, vol. 137, p. 114 785, Oct. 2022, ISSN: 0026-2714 (Cited on p. 106).

[15] H. Tuinhout and R. Van Dalen, *Design and use of an array-based test structure to characterize mechanical stress effects caused by WLCSP solder bumps*, *IEEE International Conference on Microelectronic Test Structures*, vol. 2016-May, pp. 62–67, May 2016 (Cited on pp. 106, 108).

[16] R. Van Dalen *et al.*, *A methodology to predict the impact of wafer level chip scale package stress on high-precision circuits*, *International Electron Devices Meeting, IEDM*, pp. 1–7, Feb. 2015, ISSN: 01631918 (Cited on pp. 106, 108).

[17] T. Schreier-Alt, G. Chmiel, F. Ansorge, and K. D. Lang, *Piezoresistive stress sensor for inline monitoring during assembly and packaging of QFN*, in *Proceedings - Electronic Components and Technology Conference*, 2013, pp. 2126–2131, ISBN: 9781479902330 (Cited on p. 107).

[18] J. Sun *et al.*, *Evaluation of Chip-Package Interaction by Means of Stress Sensors*, *IEEE Sensors Journal*, pp. 1–1, May 2022, ISSN: 1530-437X (Cited on pp. 107, 110).

[19] A. Prisacaru and P. J. Gromala, *Aging of the Molding Compound Identification using Piezoresistive Silicon Based Stress Sensor*, in *2021 22nd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2021*, Institute of Electrical and Electronics Engineers Inc., Apr. 2021, ISBN: 9781665413732 (Cited on p. 107).

[20] Y. H. Yang, B. Han, A. Prisacaru, P. Gromala, S. Jiang, and A. Sarwar, *In-situ service load monitoring of automotive electronic systems using silicon-based piezoresistive stress sensor*, *Microelectronics Reliability*, vol. 110, p. 113 650, Jul. 2020, ISSN: 0026-2714 (Cited on p. 107).

[21] A. Palczynska, A. Prisacaru, P. J. Gromala, B. Han, D. Mayer, and T. Melz, *Towards prognostics and health monitoring: The potential of fault detection by piezoresistive silicon stress sensor*, *Microelectronics Reliability*, vol. 74, pp. 165–172, Jul. 2017, ISSN: 0026-2714 (Cited on p. 107).

[22] A. Prisacaru, A. Palczynska, A. Theissler, P. Gromala, B. Han, and G. Q. Zhang, *In Situ Failure Detection of Electronic Control Units Using Piezoresistive Stress Sensor*, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 5, pp. 750–763, May 2018, ISSN: 21563950 (Cited on p. 107).

[23] H. Kittel, S. Endler, and F. Schindler-Saefkow, *Novel Stress Measurement System for Evaluation of Package Induced Stress*, in *2nd European Conference & Exhibition on Integration Issues of Miniaturized Systems - MOMS, MOEMS, ICS and Electronic Components*, Barcelona, Spain, 2008 (Cited on p. 107).

[24] Y. Sun, S. E. Thompson, and T. Nishida, *Strain effect in semiconductors: Theory and device applications*, 1st ed. Springer US, 2010, pp. 1–350, ISBN: 9781441905512 (Cited on p. 108).

[25] N. Matsuzuka and T. Toriyama, *Analysis for piezoresistive property of heavily-doped polysilicon with upper and lower bounds*, *Journal of Applied Physics*, vol. 108, no. 6, p. 59, Sep. 2010, ISSN: 00218979 (Cited on p. 108).

[26] R. C. Jaeger, J. C. Suhling, R. Ramani, A. T. Bradley, and J. Xu, *CMOS Stress Sensors on (100) Silicon*, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 35, no. 1, 2000 (Cited on pp. 108, 110).

[27] M. Dartiailh, *Control your instruments with Python*, 2019 (Cited on p. 108).

[28] Keithley Instruments, *Reference Manual Model 2450 SourceMeter Instrument*. Sep. 2019 (Cited on p. 109).

[29] P. French and A. Evans, *Piezoresistance in polysilicon and its applications to strain gauges*, *Solid-State Electronics*, vol. 32, no. 1, pp. 1–10, Jan. 1989, ISSN: 00381101 (Cited on p. 110).

[30] J. C. Suhling and R. C. Jaeger, *Silicon Piezoresistive Stress Sensors and Their Application in Electronic Packaging*, Tech. Rep. 1, 2001 (Cited on p. 110).

[31] F. Schindler-Saefkow *et al.*, *Material parameter identification by combination of stress chip measurements and FE simulation in MERGE Material parameter identification by combination of stress chip measurements and FE-simulation in MERGE*, Tech. Rep. (Cited on p. 110).

[32] ZVEI, *Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications*, ZVEI German Electro and Digital Industry Association, Tech. Rep., 2015 (Cited on p. 115).

6

Reduced-Order Modelling for Compact Digital Twins

Model order reduction techniques are developed and utilised to make numerical simulations more efficient. The use of Reduced-Order Models (ROMs) also enables data exchange with external parties without disclosing the sensitive information present in a Full-Order Model (FOM). It is crucial to optimise for both the efficiency and accuracy of a ROM to keep a minimal deviation from the FOM. The complexity of a ROM-based simulation depends on the definition of the ROM as well as its connection with the remaining FOM. This chapter investigates the effect of different ROM-FOM interface definitions for a test case consisting of an electronic package-on-PCB assembly. A virtual Design of Experiments (DoE) was carried out with a total of 41 cases, considering three different locations and up to four different constraint equations for the ROM-FOM interface. The effect on the accuracy and time-efficiency of the ROM-based thermomechanical simulations is compared to that of the full Finite Element (FE) model. The 'deformable' configuration for the interface generally showed the most accurate results, while the 'rigid' configuration was the most efficient across the board. The 'beam' configuration did not always follow an expected trend based on the order of elasticity values of the assigned materials. Based on the deformation results and the time associated with ROM generation and use-pass, multiple optimal solutions from the DoE are discussed. Finally, the effect of increasing the complexity of the ROM-FOM assembly, with 129 interface nodes (instead of 4) along with a more complex package geometry, on the simulation accuracy and efficiency is studied, and the practicality of ROM-integrated FOM simulations is discussed.

Parts of this chapter have been published in the proceedings of *IEEE EuroSimE Conference* (2024) [1].

6.1. Introduction

Digital Twinning for PHM requires preparing a range of models at different scales. They vary from high-fidelity, large models that require more computational resources to run and can provide more accurate results and better predictions, to low-fidelity, compact, and efficient models that can run on edge-computing hardware and provide faster results. This applies to both the physics-based and data-driven approaches within the two-branched Digital Twin architecture (refer Figure 2.8). Compact models are particularly handy for mass deployment in the form of a Digital Twin Aggregate (DTA) and can be created from high-fidelity, more accurate models and data. This is realised using different Model Order Reduction (MOR) techniques.

Compact models can be of several kinds, and there are several mathematical workflows to obtain them [2, 3]. They can be prepared from a larger set of data or existing larger models and, therefore, are their lower-dimensional versions. They can be categorised in different ways. Based on the utilised method for MOR, they can be classified as projection-based, multi-fidelity (adjusting fidelity on the fly), response surface-based meta models, multi-scale sub-models, and equivalent lumped models (*e.g.*, Lumped Parameter Model (LPM), Simulation Program with Integrated Circuit Emphasis (SPICE) models) [4–6]. In terms of the two branches of DT modelling, compact models can also be either data-driven or physics-based.

Reduced-Order Models (ROMs) can take the following forms:

- Data-driven compact models from larger purely data-driven models (*e.g.*, Artificial Neural Network (ANN)-based/other response surfaces)
- Data-driven models trained on physics-based models (*e.g.*, physics-informed ML or PINNs-based models)
- Empirical analytical models based on experimental data (*i.e.*, empirical analytical regression/meta models)
- Physics-based models created from experimental data (*i.e.*, physics-based analytical regression/meta models)
- Physics-based compact models from larger physics-based models (*e.g.*, LPMs, SPICE models, and reduced FE models)

For microelectronic systems, physics-based compact modelling is relevant in the electrical, thermal, and mechanical domains. However, existing MOR techniques and commercially available tools are mostly limited to the electrical [7, 8] and thermal domains [9–11]. It becomes tricky when such models are expected to capture the effects of these domains interacting (*e.g.*, thermomechanical properties). The

domain of thermomechanical compact models is relatively new, and there is limited research and tools available for such models [12–16]. The thermomechanical behaviour of an electronic system can affect its functional lifetime and, thus, is crucial to be included in the prepared ROMs aimed at reliability assessment and PHM. This chapter delves into physics-based ROMs in the thermomechanical domain.

Among various physics-based computational methods, Finite Element Method (FEM) is widely used for modelling and analysing thermal, mechanical, and electrical behaviour of electronic packaged components and associated electronics-enabled systems. The computational resources and simulation time required by a complex Finite Element Analysis (FEA) can be cut down by using a reduced FE model of a certain (sub)component or (sub)system within an electronic assembly. Such ROMs tend to have lower accuracy compared to the Full-Order Models (FOMs) and are primarily considered for improving the model efficiency [17–21]. Counter-intuitively, FE-based ROMs in the thermomechanical domain can be more computationally expensive in practice with the existing infrastructure of the available methodologies and developed software. The efficiency and the accuracy of such a ROM often compete with each other and cannot be achieved at the same time [22]. Therefore, it is important to choose a ROM which strikes a balance between running efficiently and attaining acceptable accuracy. Another important and yet commonly overlooked advantage of a ROM is Intellectual Property (IP) protection. They are particularly handy for exchanging data with external parties without the need to share detailed models [23]. Thus, when protecting sensitive information is a priority, the use of compact models is not just a matter of choice, convenience, or resource availability but becomes a necessity. Thus, optimising for the model efficiency is an essential aspect of using physics-based (FEM-derived) ROMs.

The computational complexity of a ROM primarily depends on the definition of its subspace and the utilised model order reduction technique. There are several MOR techniques, such as Krylov Subspace [12, 24–29], Component Mode Synthesis [29, 30], Proper Orthogonal Decomposition [31–33], Static Condensation [34, 35], *etc.* Moreover, for a certain reduction technique, the complexity varies based on the choice of the ROM-FOM interface, which defines *where* and *how* the ROM (subcomponent) is connected to the rest of the FOM (component). This chapter focuses on this particular aspect and addresses it by investigating the effect of the ROM-FOM interface definition on the accuracy of the results compared to that of a full Finite Element (FE)-based model while optimising for the efficiency of the computation.

First, a workflow of creating a Super Element (SE)-based ROM of an electronic package is presented. Then, the ROM-FOM interface, *i.e.*, the connection between the package ROM and the remaining FOM (solder + PCB) was defined using different

definitions of the constraint equations and at three different layers within the package. A Virtual Design of Experiments (VDoE) was carried out for a total of 41 cases of ROMs, and the results are compared with those of the original FOM of the complete package-PCB assembly. The accuracy of the thermomechanical deformation and the time-efficiency of the simulations were compared, and the possible optimal cases are discussed. Finally, the established workflow is implemented for a more complex package-on-PCB assembly with a significantly higher number of interface nodes along the ROM-FOM interface, and the effect on the result accuracy and simulation efficiency is studied.

6.2. Finite Element-based FOM

Initially, a test case of a package-on-PCB assembly was prepared using FE modelling. Figure 6.1 indicates the model geometry, which considers a single Quad Flat No-leads (QFN) package with a centrally placed silicon die attached to copper Lead-Frame (LF) using die-attach adhesive. In addition, there are copper pads at each corner of the package, and this sub-assembly is encapsulated by Epoxy Moulding Compound (EMC). The package is connected to the PCB using four solder interconnects at its corners. The PCB is modelled as a homogenised equivalent layer.

The main objective of the prepared FE-model is to simulate the thermomechanical behaviour of the considered electronic system and utilise the workflow to evaluate thermal stresses in solder joints for the estimation of fatigue lifetime. Considering this goal, the four landing pads (copper) embedded into the PCB were modelled separately to make the region surrounding the solder joints more detailed for better accuracy. Moreover, the package geometry is prepared such that a ROM-FOM interface can be defined at different layers within the package, keeping the solder joints and PCB always a part of the remaining FOM.

A cyclic thermal load induces the accumulation of damage in solder material due to plastic strains and eventually leads to fatigue failure. This is governed by warpage

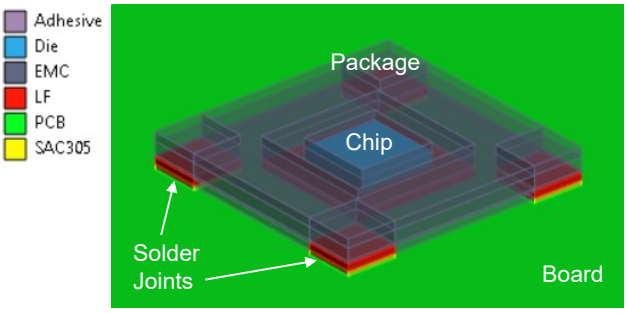


Figure 6.1: The geometry of the package-on-PCB assembly test case. The QFN package contains a centrally placed silicon die attached to the copper leadframe (LF) with the die-attach (adhesive) and encapsulated with EMC. Four solder joints connect the copper pads of the package and PCB.

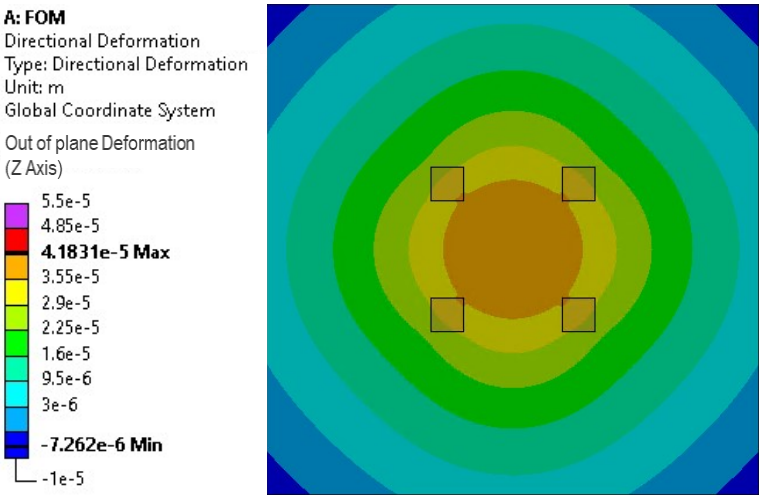


Figure 6.2: The out-of-plane deformation (*i.e.*, warpage) of the solder-PCB subassembly in the original Full-Order Model (FOM) under a temperature variation from 125 °C to −40 °C. This spatial plot is used as the reference for benchmarking the accuracy of different cases of ROM-based simulations.

(*i.e.*, the out-of-plane deformation) due to the CTE mismatch between different materials in the assembly. It is crucial to get the failure prediction from a ROM-based simulation, the same as or as close to the FOM. Therefore, the warpage plot of the solder-PCB sub-assembly was utilised for benchmarking the accuracy of ROM-based models. Figure 6.2 shows the spatial plot of the out-of-plane deformation for the FOM under a temperature variation from 125 °C to −40 °C. This plot is used as the reference for comparing the results of different ROM-based simulation cases.

6.3. SUBSTRUCTURE-BASED FEA (ROM)

A substructure-based approach was utilised to create an equivalent compact model of the package, considering it as the target IP to be protected. This method generates a superelement of the package subassembly. Figure 6.3 shows the cross-sectioned geometry of the package-on-PCB test case with annotations for all material layers and the three considered locations for the ROM-FOM interface.

6.3.1. SUBSTRUCTURE GENERATION

First, the entire system assembly was partitioned by defining the ROM-FOM interface at one of the three different locations – (1) between package-leadframe and solder joint, (2) within the package-leadframe, and (3) between package-leadframe and moulding compound, as indicated in Figure 6.3.

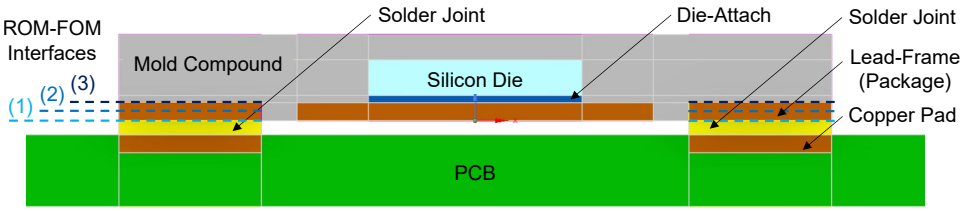
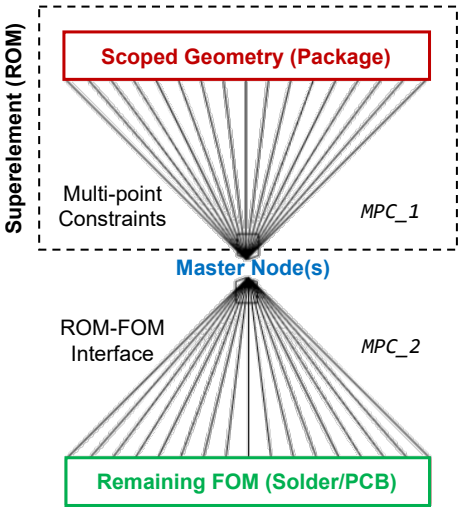


Figure 6.3: The cross section of the test case assembly indicating different layers of materials and the three considered locations of the ROM-FOM interface (*viz.*, *Interface 1*, *Interface 2*, and *Interface 3*).

Next, the steps for substructure generation were carried out on the package side of the geometry. Four surfaces were defined as the scope geometry for creating master nodes of the resulting superelement. For example, the lower surface of each copper pad of the package became the scoped geometry for the *Interface 1*. For simplicity and efficient simulations, each scoped geometry was assigned only one master node with six Degrees of Freedom (DoF). This step connects each node on the scoped geometry's FE mesh to the respective master node using Multi-Point Constraint (MPC) equations. MPCs are the set of additional equations that map the DoF of the scoped nodes to those of the respective master nodes.

Figure 6.4 shows the schematic representation of how a scoped geometry is connected to a master node using a set of equations (`MPC_1`), which forms the SE-based ROM of the package subassembly. For this study, three main types of MPCs were considered – *deformable*, *rigid*, and *beam*. A *deformable* relation makes the DoF of master nodes dependent, with only 6 MPCs, while a *rigid* relation makes the DoF of 81 scoped nodes dependent, with 486 (6×81) MPCs.

Figure 6.4: A schematic representation of two sets of multi-point constraints (MPC) for the ROM-FOM interface. `MPC_1` connects the scoped geometry to master nodes to form a superelement-based ROM, and `MPC_2` connects the ROM substructure to the remaining FOM.



A *beam* relation acts as a beam (finite) element with a defined circular cross section and assigned material properties. For every beam definition, the cross-sectional diameter was kept the same as the side of the square copper pad, and one of the interface materials was assigned. For example, a *beam* MPC for the *Interface 3* could have EMC and LF (copper), while only LF could be assigned to the *Interface 2* MPC.

Then, a matrix reduction step was defined, which removes the dependent DoF applicable for the chosen MPC relation using static condensation. The goal of the SE generation step is to obtain the effective load vector to be applied to the remaining FOM. A thermal load vector corresponding to a unit temperature difference (*i.e.*, $\Delta T = 1\,^{\circ}\mathrm{C}$) was obtained from this step by exporting the resulting substructure file.

6.3.2. ROM Integration and Load Vector

A new simulation project was created from the original FOM for utilising the prepared ROM. Based on the location of the interface for each case, the package geometry was excluded. The thermal load conditions were kept identical for the remaining FOM. Then, the generated ROM substructure of the package was imported and tied to the rest of the FOM geometry, *i.e.*, the PCB, solder joints, and the remaining package subcomponents (if applicable), using another choice of MPC relation (`MPC_2`). Figure 6.5 shows the integrated ROM, represented by only the geometric outer boundary (wireframe) of the package, keeping the inner layers completely hidden.

At the same time, an effective load is applied at the master nodes, which now scope the corresponding surfaces on the other side of the ROM-FOM interface. The same set of MPC definitions (*deformable*, *rigid*, and one or more *beam* configurations) was utilised. The default thermomechanical load (force and moment) exerted by the imported ROM corresponds to the package deformations due to a unit temperature increase (*i.e.*, $\Delta T = 1\,^{\circ}\mathrm{C}$). Thus, a custom subroutine (refer Appendix B) was utilised to scale the thermal load vector as a function of temperature at different time steps [36], matching the temperature profile applied to the FOM subassembly.

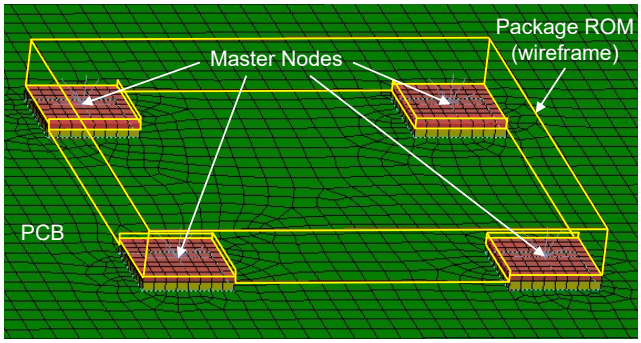


Figure 6.5: An example of the integrated ROM substructure of the package (for *Interface 3*), which hides the inner layers completely. The effective thermomechanical load vector is applied at the master node connections between the ROM and the remaining FOM.

The mathematical representation of the effective thermomechanical load scaling is given in Equation (6.1), where $\boldsymbol{K}$ is the global stiffness matrix of the remaining FOM, $\boldsymbol{u}$ is the displacement vector, $\boldsymbol{f}^{\text{th}}$ is the load vector due to applied thermal load conditions, $\boldsymbol{f}^{\text{th}}_{\text{ROM}}$ is the default load vector from ROM due to the $\Delta T = 1\,^{\circ}\text{C}$, and $w(T)$ is the temperature (T)-dependent scaling parameter. Note that the temperature-dependent properties for the materials in the remaining FOM (*e.g.*, solder) also scale the $\boldsymbol{K}$ matrix as per the applied thermal condition.

$$\boldsymbol{K} \cdot \boldsymbol{u} = \boldsymbol{f}^{\text{th}} + w(T) \cdot \boldsymbol{f}^{\text{th}}_{\text{ROM}} \tag{6.1}$$

6.4. Virtual Design of Experiments

A virtual design of experiments was created based on all possible combinations of the location of the system partition and the two sets of MPC definitions applicable for the chosen ROM-FOM interface. The simulation results are compared with those of the original FOM (indicated in Figure 6.2) to find the most accurate cases, and the required computational time was also compared. The DoE results data are summarised in Table 6.1 and Table 6.2, where B-Sol, B-LF, and B-MC indicate a *beam* MPC definition utilising the material properties of solder, leadframe (copper), and moulding compound (EMC), respectively.

Table 6.1 shows the variation of the accuracy of ROM-based simulations by comparing the percentage deviation of the maximum warpage value with respect to 0.041 83 mm of the original FOM. Table 6.2 shows the comparison of model efficiency by comparing the surplus computation time in seconds of the ROM-based simulation with respect to 14.797 seconds for the original FOM. Note that this particular comparison only considers the time required for the SE use-pass, *i.e.*, the substructure generation time is excluded. Substructure generation time for all definitions of `MPC_1` remains close to the 30-second mark for the *Interface 1* and *Interface 3*, whereas it is around 40 seconds for the *Interface 2*. Figure 6.6 shows the comparison of spatial plots of warpage of the remaining FOM for all combinations of the MPC definitions for the *Interface 1*. Similar plots for *Interface 2* and *Interface 3* were also obtained and are indicated in Figure B.1 and Figure B.2, respectively, in Appendix B.

VDoE Results and Discussion

The results obtained from the VDoE are compared for the quality and efficiency of the ROM-based simulations. The data in Table 6.1 and Table 6.2 are classified into several zones (denoted by colours) to highlight the observed trends. The reasoning behind a few MPC combinations is discussed, and the possibilities of an overall optimal solution are explored.

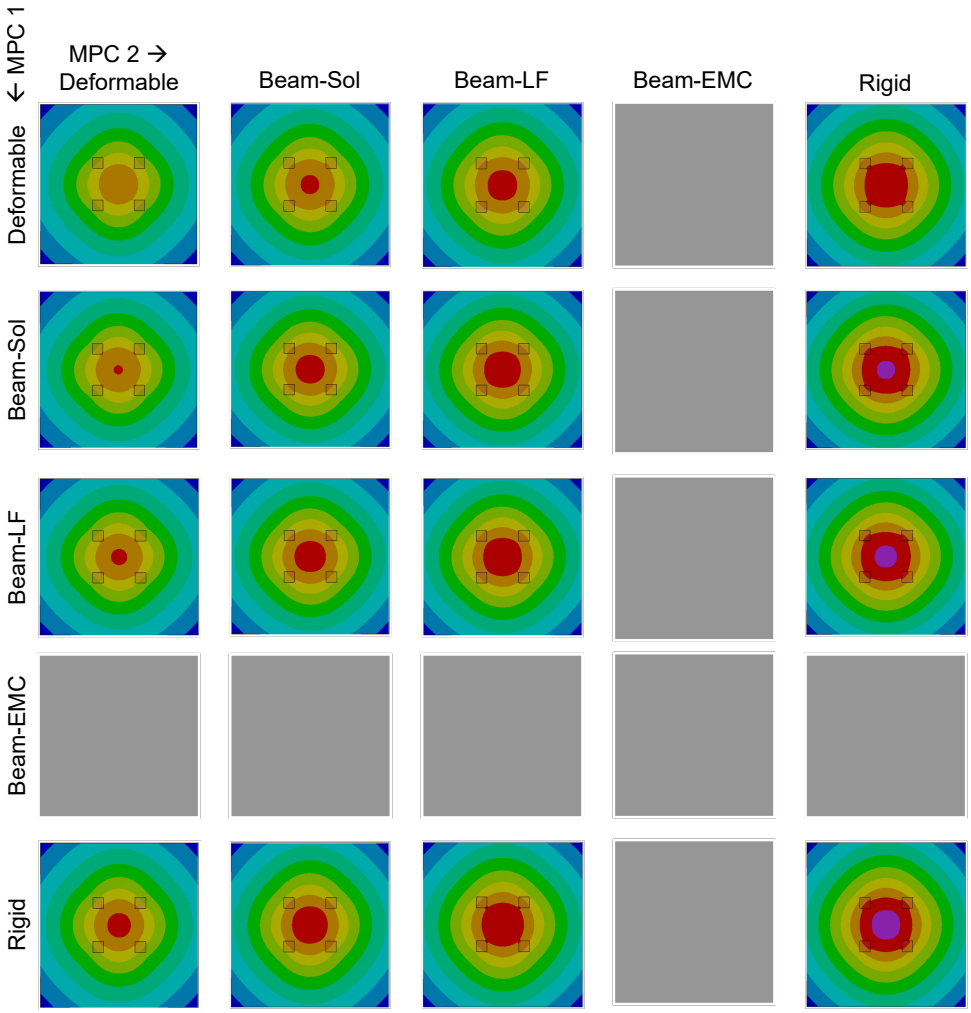


Figure 6.6: The comparison of spatial plots of warpage (identical scale as Figure 6.2 for all subplots) of the solder-PCB subassembly (remaining FOM) for all combinations of the MPC definitions for *Interface 1*.

The trends in Table 6.1 show that for all three interfaces, the inclusion of a *rigid* configuration in any of the `MPC_1` and `MPC_2` definitions gives the least accurate results. This is because a *rigid* configuration retains the original shape of the scoped geometry [36], which restricts thermal expansion in some ways and produces unrealistically high thermal stresses. Thus, a *rigid* configuration is not the most suited for thermomechanical problems. On the other hand, it significantly increases the time-efficiency of the SE use-pass, as indicated in Table 6.2. This also holds true for the time required for SE generation (not included in Table 6.2) for all three

Table 6.1: The percentage deviation of the maximum warpage value of the ROM-based simulation with respect to 0.041 83 mm of the original FOM.

Legend:

< 5%	5-10%	10-15%	15-20%	> 20%

(a) Interface 1: between Package-LF and Solder Joint

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	-2.93	2.94	6.79		14.46
B-Sol	1.13	6.97	10.79		18.41
B-LF	2.48	8.31	12.13		19.74
B-MC					
Rigid	4.92	10.74	14.55		22.17

(b) Interface 2: within Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	-0.82		5.10		10.39
B-Sol					
B-LF	6.50		12.42		17.67
B-MC					
Rigid	12.67		18.65		23.88

(c) Interface 3: between EMC and Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	1.33		3.48	5.55	9.19
B-Sol					
B-LF	6.71		8.78	10.88	14.52
B-MC	10.19		12.29	14.39	18.02
Rigid	16.06		18.20	20.31	23.93

interfaces. It can be explained by the fact that a *rigid* definition treats all the scoped nodes as dependent, which eliminates a large number of DoF and greatly reduces the size of the stiffness matrix, requiring fewer computational resources.

The inclusion of the *deformable* configuration generally keeps the accuracy high. With a *deformable* definition, FEM solver keeps the DoF of the scoped nodes independent, making it the same in number as in the original FOM. Thus, it does not gain much of an advantage in efficiency over the *rigid* configuration, which is evident from the data in Table 6.2. Among various MPC combinations of the considered cases, the *deformable-deformable* configuration shows one of the most accurate results (see Table 6.1). But this consistency doesn't translate to its time-efficiency, as shown by quite inconsistent trends in Table 6.2 across the three interfaces. Therefore, the suitability of the *deformable* configuration seems to be material dependent.

Table 6.2: The surplus computation time in seconds of the ROM-based simulation (use-pass only) with respect to 14.797 seconds for the original FOM.

Legend:

< 40%	40-50%	50-60%	60-65%	> 65%

(a) Interface 1: between Package-LF and Solder Joint

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	5.00	10.28	8.39		4.45
B-Sol	6.44	8.80	8.70		6.41
B-LF	5.81	8.34	9.30		6.17
B-MC					
Rigid	5.02	7.31	7.20		4.73

(b) Interface 2: within Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	7.25		7.06		5.50
B-Sol					
B-LF	7.56		9.58		7.14
B-MC					
Rigid	7.61		7.95		8.14

(c) Interface 3: between EMC and Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	10.03		10.20	10.20	8.64
B-Sol					
B-LF	8.78		8.70	9.30	8.36
B-MC	8.59		9.69	8.66	6.92
Rigid	5.89		7.16	9.38	5.25

The results in Table 6.1 collectively indicate that it is important to consider the configuration of the interfacing layers while choosing an optimal MPC relation pair. The suitability of an MPC definition also depends on the material properties of the respective scoped geometries. For instance, consider all the combinations of the *deformable* and *rigid* definitions for the *Interface 1*. It involves copper and solder, the former of which is much stiffer than the latter, with a ratio of the elasticity moduli ($E_{\mathrm{LF}}/E_{\mathrm{sol}}$) ranging from 4:1 to 2.25:1.

The *rigid-deformable* configuration pair works well with a less than 5% deviation of warpage with respect to FOM. Similarly, when the location of interface is moved to between the EMC and LF (*Interface 3*), the stiffness ratio of the scope geometry 1 and 2 ($E_{\mathrm{EMC}}/E_{\mathrm{LF}}$) is 1:6, much lower compared to that of the *Interface 1*. The *rigid-deformable* configuration for this is one of the worst combinations for the accuracy.

The same logic justifies the case where these MPC relations are swapped (the *deformable-rigid* configuration pair) being much worse for *Interface 1* (nearly 15% deviation) and slightly better for the *Interface 3*. This proves that the *rigid* configuration could be considered when a relatively stiff material is involved and should only be assigned to that scoped geometry. It can be paired with a *deformable* configuration if the other scoped layer has a relatively much lower stiffness.

A *beam* configuration sits in between the *rigid* and *deformable* configurations in terms of accuracy of results. However, the trend does not always follow an expected trend based on the increasing order of material stiffness values (which is EMC, solder, and copper). For the *Interface 1* (Table 6.1(a)), the colour trend clearly shows that the result accuracy of the *beamSol* and *beamLF* configurations fits perfectly between the *deformable* and *rigid* configurations in the order of their relative stiffness values. This can be observed in the spatial plots shown in Figure 6.6, where a gradual increase in the out-of-plane deformation is observed as a function of increasing the column and row number.

For the *Interface 3* results (Table 6.1(c)), the order of decreasing result accuracy is followed only if *beamEMC* is placed after *beamLF*, which is the opposite of the order of relative stiffness. One of the reasons is that the EMC has a slightly lower CTE than LF, which allows less thermal expansion for the *beamEMC* configuration. In addition, EMC occupies a large volume in the package compared to any other material. These two aspects combined put *beamEMC* closer to the *rigid* configuration than *beamLF* in terms of accuracy. In other words, a much higher volume fraction of EMC and a slightly lower CTE compensate for its lower stiffness. Thus, the quality of results also depends on a combination of material properties (stiffness and CTE) and the relative share of the chosen interfacing material in the ROM geometry.

The *beam* configuration, by its definition, serves as a 'spot weld' joint and is more effective for geometries with a smaller width-to-thickness ratio [36]. The solder joints and leadframe copper pads utilised in this test case have a much larger width-to-thickness (height) ratio of 10:1. Thus, a *beam* configuration would be more effective for a geometry containing, *e.g.*, a solder joint with smaller dimensions and higher standoff height, which is used in a new test case described in the following section.

Multiple cases in the DoE could be chosen as the overall optimal solution based on the deformation results and the time associated with the ROM use-pass. For example, all four cases with `MPC_2` set to *deformable* for the *Interface 1* show the least deviation from FOM for the results and the surplus time. The *deformable-deformable* pair for the *Interface 2* is the global optimum for accuracy and also gives an acceptable time-efficiency. The *beamLF-deformable* and *beamLF-beamLF* are the only combinations for the *Interface 3* with a good balance of accuracy and efficiency.

6.5. ROM-FOM Interface for Complex Test Cases

The presented VDoE considers a rather simpler package-on-PCB assembly. While it was necessary to obtain an overview of the ROM-FOM interface selection, it does not necessarily fully comment on the effectiveness of the FE-based compact models for more complex electronic assemblies and the accuracy and efficiency of their ROM-integrated FOM simulations. Thus, the established workflow was implemented on a new, more complex test case.

The new test case also comprises a package-on-PCB assembly, which includes the same package corresponding to the 3000 h of thermal ageing stage, previously developed in Chapter 3. The CAD geometry includes a flipchip BGA package (including the detailed models of copper pillars, solder interconnects, and a multi-layered substrate within the package) with a total footprint of 14 mm × 14 mm, assembled centrally on a PCB (with four times the area of the top surface) using cylindrically shaped solder joints. The solder joints have a much smaller width-to-thickness (*i.e.*, diameter to height) aspect ratio of ≈ 1.43 than that of the previous test case. Due to symmetry, a quarter model is utilised for this analysis. Figure 6.7(a) and (b) show the model of the package-on-PCB assembly (quarter geometry) and the detailed package geometry with several aforementioned layers within.

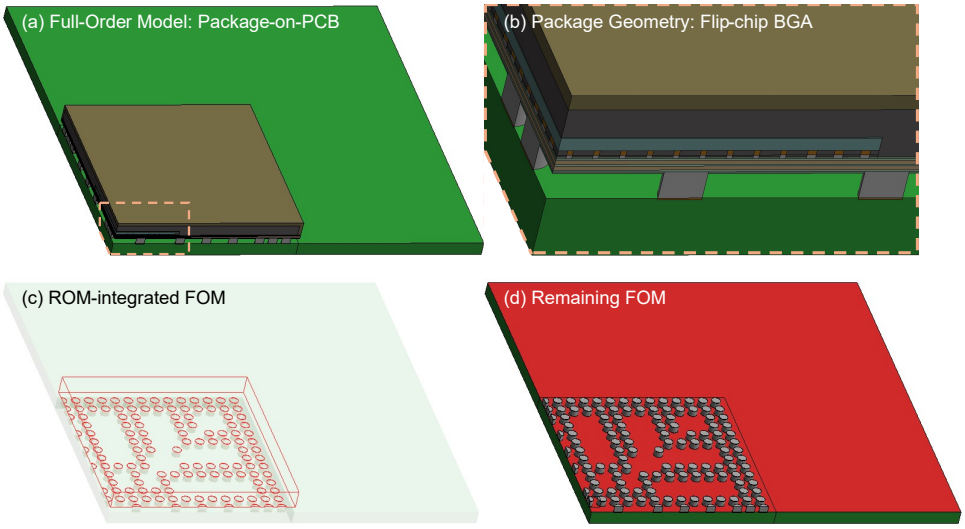


Figure 6.7: The second test case for the ROM-FOM interface – (a) the quarter geometry of the full-order model of the package-on-PCB assembly, (b) detailed model of the flipchip BGA package (representing 3000 h of thermal ageing of EMC) with copper pillars, solder caps, and a multi-layered substrate within the package, (c) ROM-integrated FOM with 129 interface nodes located on top surfaces of the cylindrically shaped board-level solder interconnects, and (d) the solder-PCB subassembly, *i.e.*, the remaining FOM, with the PCB top surface indicated in red and used for warpage calculation.

The ROM-FOM interface was defined between the package metallisation layer and the board-level solder joints (similar to the *Interface 1* indicated in Figure 6.3), using the same principle of multi-point constraints (previously described in Figure 6.4). A total of 129 master nodes were defined connecting the corresponding scoped geometries on either sides, *i.e.*, the bottom surface of the bottom-most metallisation layer within the package (*Core M3*) and the top surface of each solder joint, to define the MPCs, `MPC1` and `MPC2`, respectively. Note that on each side, the total of 129 scoped geometries includes 15 semicircular faces due to the fact that the model geometry is sectioned along the planes of symmetry. Figure 6.7(c) and (d) show the ROM-integrated FOM and the solder-PCB subassembly (*i.e.*, the remaining FOM).

The outcomes of the VDoE on the previous test case indicate that the results corresponding to `MPC1` with the *deformable* configuration are overall better than the rest, in terms of both accuracy and efficiency. Thus, only the *deformable* configuration for the SE generation pass (*i.e.*, for `MPC1`) was considered for the new test case. Whereas, all four possible options – *deformable*, *rigid*, *BeamSol*, *BeamCoreM3* – for the SE use-pass (*i.e.*, for `MPC2`) were taken into consideration. A thermal load from 180 °C to −40 °C was applied with several steps in between with a maximum interval of 25 °C. For the SE use-pass, the script for scaling the load vector was implemented after adapting it for the new thermal load. The top surface of the PCB (marked in red in Figure 6.7(d)) was utilised for the calculation of out-of-plane deformation.

6.5.1. Accuracy Comparison

Figure 6.8 shows the warpage comparison of all considered cases at −40 °C. All of the ROM-integrated FOM configurations depict a similar warpage trend to that of the full-order model without any large discrepancies. The *deformable-deformable* configuration manages to produce results with ≈ 10% deviation for the maximum deformation values while keeping the diagonal symmetry of results consistent across all temperature steps. Both *beam* configurations show an even smaller, ≈ 5%, deviation, but lose the diagonal symmetry of the results. The *rigid* configuration, as expected from the previous DoE, shows the most, ≈ 20%, deviation from the FOM.

A similar trend is observed for temperature values up to 75 °C. Above this, in the glass transition region of the pristine and oxidised EMC, the gap between the deformation of any ROM-integrated FOM configuration and that of the FOM widens, with ROM-FOM showing more deformation than that of the FOM. As the temperature descends from 180 °C, the deformation of FOM scales non-linearly, starting with no deformation at 180 °C, increasing in magnitude with a smaller rate up to 125 °C, and then continuing the increase with a much larger slope. This artefact can be explained by the temperature-dependent and non-linear material properties of the involved materials, primarily the EMC.

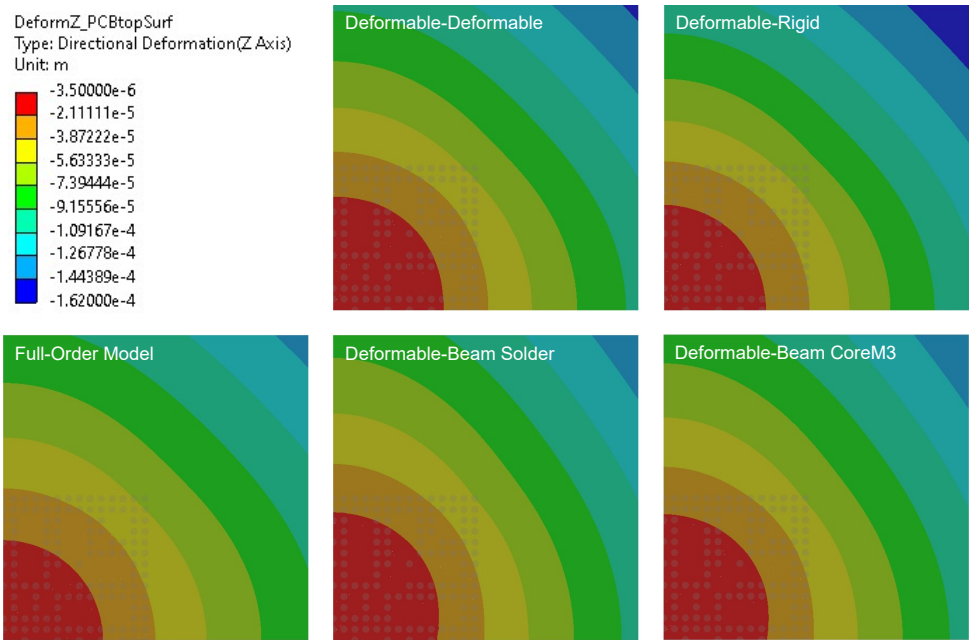


Figure 6.8: The comparison of spatial plots of warpage of the solder-PCB subassembly (remaining FOM) at −40 °C for all combinations of the MPC definitions for the new test case with a flipchip BGA package. Compared to FOM, the *deformable-deformable* configuration has ≈ 10%, and the *deformable-rigid* configuration has ≈ 20% deviation for the maximum deformation values, while retaining the diagonal symmetry. Both *deformable-beam* configurations show ≈ 5% deviation but lose the diagonal symmetry of the results.

On the other hand, the deformation in ROM-integrated FOM scales linearly, because of the linear material properties of the remaining FOM and linear scaling of the superelement load vector. Another reason for an acceptable match of results in the range −40 °C to 50 °C is that the SE is prepared around 0 °C (*i.e.*, the reference temperature for the SE generation pass is set to 0 °C), with a thermal load $\Delta T = 1$ °C. This setting assumes the values of material properties at the reference temperature, and the load vector is linearly scaled, without considering any temperature dependency. This is an expected side-effect of using a ROM with a single, linear SE.

This limitation regarding the non-linear effects can be overcome by three different ways – (i) non-linear scaling of the load vector, (ii) using a superposition of multiple linear SEs that are generated at several different reference temperature values within the range of the intended thermal load, and (iii) generating a temperature-dependent SE which would involve directly scaling the stiffness matrix of the SE (package ROM) instead of linearly scaling the resulting load vector. The effect on accuracy can be further analysed by defining multiple master nodes per interface (*i.e.*, scoped geometry) and exploring other shapes and aspect ratios of solder joints.

6.5.2. Efficiency Comparison

In terms of simulation efficiency, the new test case is particularly important because the package that is being reduced to a superelement is in itself a complex, intricate geometry requiring a fine FE mesh. In this case, the full package-on-PCB assembly (FOM) consist of 3D finite elements with 2 576 562 DoF, while the package (*i.e.*, the target geometry for SE generation) comprises 1 638 750 DoF. Therefore, the package itself consists of more than 60% of the total FE model. This has an effect on the efficiency of the ROM-integrated FOM simulation.

Since the full model in the new test case is much more complex than the first test case, it takes more time to compute, which is expected to reduce the time gap between the original FOM and the ROM-integrated FOM simulations. In fact, the SE generation pass takes nearly the same (≈ 500 s) as that of the entire FOM while running on a High-Performance Computer (HPC), while all SE use-pass cases take less than 60% of the time that of the FOM. Thus, the time taken for the SE use-pass determines the overall model efficiency.

Considering the time taken for the SE generation and use-pass together (unlike the use-pass only time for the previous test case, as presented in Table 6.2), the *deformable-deformable* configuration takes about 43%, both *deformable-beam* configurations take 45–50%, and the *deformable-rigid* configuration takes about 64% surplus computational time over the FOM. The *deformable-deformable* configuration, along with more consistent and accurate results, happens to be the most efficient one for this test case. Therefore, it can be concluded that this configuration is generally a better overall choice for the MPC definitions in a ROM-integrated FOM simulation.

Conclusion

Reduced-order models can be of different forms – projection-based, multi-fidelity, response surface-based meta models, equivalent lumped models, *etc.* They can be prepared based on experimental data or larger data-driven / physics-based models. Finite Element-based ROMs in the thermomechanical domain can be computationally more expensive as opposed to the common belief of them being always more efficient than FOMs. However, such ROMs facilitate IP protection, and thus, can be a great way of information exchange with external parties. The accuracy and efficiency of ROMs often compete with each other and need to be optimised.

The VDoE shows that there could be more than one optimal solution when it comes to finding the most suitable location and MPC definition for a ROM-FOM interface. The inclusion of the *deformable* configuration generally results in higher accuracy. However, the optimal MPC choice depends on the thermomechanical properties

of the involved materials and also on their volume fraction in the ROM geometry, especially when EMC is one of the interfacing layers. When a heterogeneous interface is involved, the ratio of stiffness and the disparity in CTE values should be taken into consideration when making a choice for a suitable MPC configuration.

The current work utilises a linear superelement that generates a thermomechanical load vector corresponding to $\Delta T = 1\,^{\circ}\mathrm{C}$, which is then scaled according to the applied thermal load to get an effective load vector from the package-ROM. This approach worked well for the first test case across the considered temperature range, since only linear material properties were involved. The second test case, involving a more complex FE model, fared well on the grounds of efficiency. It also showed a reasonably good match of results for a certain temperature range around $0\,^{\circ}\mathrm{C}$ but showed deviation in the glass transition region of EMC, where its thermomechanical elastic properties change in a non-linear fashion. Thus, a ROM based on a single linear SE can be used if the temperature-dependent material properties do not drastically change in the given temperature range.

The analyses presented in this chapter prove the point that the right implementation of the MOR technique and the right choice of the ROM-FOM interface and MPC configuration can make the SE-based reduced-order modelling a more practical approach, while achieving a crucial goal of IP protection. When made compatible with a data exchange standard like Functional Mock-up Interface (FMI), such physics-based ROMs can also serve as Functional Mock-up Units (FMUs). This ties well with the Digital Twin framework for PHM (refer Figure 2.8) where a series of models can interact with each other, as these models can be integrated into larger physics-based FE models or even into Digital Twins of other larger systems. Well-optimised FE-based reduced models that require fewer computational resources can serve as a good alternative to purely data-driven reduced models and can facilitate the implementation of the Digital Twin Aggregate (DTA) phase.

References

[1] A. Inamdar, T. Hauck, M. van Soestbergen, W. D. Driel, and G. Zhang, *ROM-FOM Interface Optimization for Efficient Thermomechanical Simulations of Electronic Components*, in *2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2024*, Institute of Electrical and Electronics Engineers Inc., Apr. 2024, ISBN: 9798350393637 (Cited on p. 123).

[2] G. Gildenblat, Ed., *Compact modeling: Principles, techniques and applications*, 1st ed. Springer Netherlands, Sep. 2010, pp. 1–527, ISBN: 9789048186136 (Cited on p. 124).

[3] W. Keiper, A. Milde, and S. Volkwein, Eds., *Reduced-order modeling (ROM) for simulation and optimization: Powerful algorithms as key enablers for scientific computing*. Springer International Publishing, Apr. 2018, pp. 1–179, ISBN: 9783319753195 (Cited on p. 124).

[4] T. Bechtold, G. Schrag, and L. Feng, Eds., *System-level modeling of MEMS*. Wiley-VCH Verlag, Feb. 2013, vol. 10, pp. 1–530, ISBN: 9783527647132 (Cited on p. 124).

[5] K. Fukami, K. Hasegawa, T. Nakamura, M. Morimoto, and K. Fukagata, *Model Order Reduction with Neural Networks: Application to Laminar and Turbulent Flows*, *SN Computer Science*, vol. 2, no. 6, pp. 1–16, Nov. 2021, ISSN: 26618907 (Cited on p. 124).

[6] M. Hinze, J. N. Kutz, O. Mula, and K. Urban, *Model Order Reduction and Applications* (Lecture Notes in Mathematics), M. Falcone and G. Rozza, Eds. Cham: Springer Nature Switzerland, 2023, vol. 2328, ISBN: 978-3-031-29562-1 (Cited on p. 124).

[7] R. Ionutiu, *Model order reduction for multi-terminals systems : with applications to circuit simulation*, Ph.D. dissertation, Technische Universiteit Eindhoven, Eindhoven, The Netherlands, 2011, ISBN: 9789038625805 (Cited on p. 124).

[8] B. Nouri, E. Gad, M. Nakhla, and R. Achar, *Model order reduction in microelectronics*, in *Model Order Reduction: Applications*, vol. 3, De Gruyter, Dec. 2020, pp. 111–144, ISBN: 9783110499001 (Cited on p. 124).

[9] M. Galicia, P. Zajac, C. Maj, M. Szermer, and A. Napieralski, *Modelling modern processors using FEM and compact model - A comparative study*, *Proceedings of the 21st International Conference on Mixed Design of Integrated Circuits and Systems, MIXDES 2014*, pp. 293–297, 2014 (Cited on p. 124).

[10] L. Codecasa, V. D'Alessandro, and R. Bornoff, *Galerkin's Projection Framework for BCI CTMs - Part I: Extended FANTASTIC Approach*, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 11, pp. 1792–1803, Nov. 2021, ISSN: 21563985 (Cited on p. 124).

[11] B. Rogié *et al.*, *Multi-port dynamic compact thermal models of dual-chip package using model order reduction and metaheuristic optimization*, *Microelectronics Reliability*, vol. 87, pp. 222–231, Aug. 2018, ISSN: 0026-2714 (Cited on p. 124).

[12] C. B. Umunnakwe, I. Zawra, M. Niessner, E. B. Rudnyi, D. Hohlfeld, and T. Bechtold, *Compact modelling of a thermo-mechanical finite element model of a microelectronic package*, *Microelectronics Reliability*, vol. 151, p. 115 238, Dec. 2023, ISSN: 0026-2714 (Cited on p. 125).

[13] E. Zukowski, J. Wilde, E. Rudnyi, and J. G. Korvink, *Model reduction for thermo-mechanical simulation of packages*, in *International Workshop on Thermal Investigation of ICs and Systems*, Belgirate. Italy, Sep. 2005, pp. 134–138 (Cited on p. 125).

[14] M. Van Soestbergen, *Thermo-Mechanical Compact Model to Simulate Solder Fatigue of QFN packages*, in *2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2024*, Catania, Italy: Institute of Electrical and Electronics Engineers Inc., Apr. 2024, ISBN: 9798350393637 (Cited on p. 125).

[15] C. B. Umunnakwe *et al.*, *Model Order Reduction of a Thermo-Mechanical Packaged Chip Model for automotive MOSFET applications*, in *2022 23rd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2022*, Malta: Institute of Electrical and Electronics Engineers Inc., Apr. 2022, ISBN: 9781665458368 (Cited on p. 125).

[16] S. Hassan, S. Stoyanov, P. Rajaguru, and C. Bailey, *Reduced-Order Modelling for Coupled Thermal-Mechanical Analysis and Reliability Assessment of Power Electronic Modules with Nonlinear Material Behaviours*, in *2024 IEEE 10th Electronics System-Integration Technology Conference, ESTC 2024 - Proceedings*, Berlin, Germany: Institute of Electrical and Electronics Engineers Inc., 2024, ISBN: 9798350390360 (Cited on p. 125).

[17] D. Hartmann, M. Herz, and U. Wever, *Model order reduction a key technology for digital twins*, in *Reduced-Order Modeling (ROM) for Simulation and Optimization: Powerful Algorithms as Key Enablers for Scientific Computing*, Springer International Publishing, Apr. 2018, ch. 8, pp. 167–179, ISBN: 9783319753195 (Cited on p. 125).

[18] I. Zawra, J. Zaal, M. v. Soestbergen, T. Hauck, E. Rudnyi, and T. Bechtold, *Compact Modelling of Wafer Level Chip-Scale Package via Parametric Model Order Reduction*, in *Scientific Computing in Electrical Engineering (SCEE) 2022*, M. van Beurden, N. V. Budko, G. Ciuprina, W. Schilders, H. Bansal, and R. Barbulescu, Eds., vol. 43, Amsterdam: Springer Medizin, Mar. 2024, pp. 217–228 (Cited on p. 125).

[19] M. Niessner, A. Gyarmati, and H. Guettler, *Impact of mechanical material modeling on the solder joint fatigue analysis of a leadless package mounted at different positions inside a generic aluminum ECU*, in *2023 24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2023*, Institute of Electrical and Electronics Engineers Inc., 2023, ISBN: 9798350345971 (Cited on p. 125).

[20] T. Zhu, Q. Wang, Y. Lin, R. Wang, and R. Huang, *MORE-Stress: Model Order Reduction based Efficient Numerical Algorithm for Thermal Stress Simulation of TSV Arrays in 2.5D/3D IC*, *Arxiv - Computer Science - Computational Engineering*, Nov. 2024 (Cited on p. 125).

[21] A. Schütz, M. Olbrich, A. Taghdiri, C. Ament, and T. Bechtold, *Towards Automated Model Order Reduction and Feedback Control for Nonlinear Finite Element Models*, in *International Federation of Automatic Control (IFAC) PapersOnLine*, vol. 59, Elsevier, Jan. 2025, pp. 139–144 (Cited on p. 125).

[22] MathWorks Corporation, *Reduced Order Modeling*, 2023 (Cited on p. 125).

[23] B. Lecointre and C. M. Mathieu, *Reduce model complexity with Simcenter Reduced Order Modeling*, Nov. 2023 (Cited on p. 125).

[24] R. W. Freund, *Krylov-subspace methods for reduced-order modeling in circuit simulation*, *Journal of Computational and Applied Mathematics*, vol. 123, no. 1-2, pp. 395–421, Nov. 2000, ISSN: 0377-0427 (Cited on p. 125).

[25] A. Schütz, M. Farny, M. Olbrich, M. Hoffmann, C. Ament, and T. Bechtold, *Model Order Reduction of a Nonlinear Electromechanical Beam Actuator by Clustering Nonlinearities*, in *Proceedings of ACTUATOR 2022 International Conference and Exhibition on New Actuator Systems and Applications*, Mannheim, Germany: VDE, 2022, ISBN: 978-3-8007-5894-4 (Cited on p. 125).

[26] C. Yuan, S. Maeter, Y. Maniar, and T. Bechtold, *Re-Integrating a Reduced-Order Model into Finite Element Environment for Thermo-Mechanical Reliability Analysis in Microelectronics*, in *Proceedings of 2024 IEEE 10th Electronics System-Integration Technology Conference, ESTC 2024*, Berlin, Germany: Institute of Electrical and Electronics Engineers Inc., 2024, ISBN: 9798350390360 (Cited on p. 125).

[27] C. Yuan, S. Maeter, A. Schutz, I. Zawra, M. V. Soestbergen, and T. Bechtold, *Efficient Simulation of Nonlinear Plastic Models in Microelectronics: A Trajectory Piecewise Linear-Based Model Order Reduction*, in *2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2024*, Catania, Italy: Institute of Electrical and Electronics Engineers Inc., 2024, ISBN: 9798350393637 (Cited on p. 125).

[28] C. Yuan, M. Niessner, and T. Bechtold, *Model Order Reduction of a Microelectronic Package Subjected to Temperature Cycling and Vibration Test*, in *2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2024*, Catania, Italy: Institute of Electrical and Electronics Engineers Inc., 2024, ISBN: 9798350393637 (Cited on p. 125).

[29] C. Yuan, S. Maeter, S. Kuttler, O. Wittler, and T. Bechtold, *Reduced-Order Modelling for Efficient Chip-Package-Board Design*, in *2025 26th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, IEEE, Apr. 2025, pp. 1–6, ISBN: 979-8-3503-9300-2 (Cited on p. 125).

[30] Y. Aoyama and G. Yagawa, *Component mode synthesis for large-scale structural eigenanalysis*, *Computers & Structures*, vol. 79, no. 6, pp. 605–615, Feb. 2001, ISSN: 0045-7949 (Cited on p. 125).

[31] A. Schütz, S. Maeter, and T. Bechtold, *Nonlinear Model Order Reduction of a MEMS Actuator by a Trajectory Piecewise-Linear Approximation*, in *MikroSystemTechnik Kongress 2023*, Dresden, Germany: VDE Verlag, 2023, ISBN: 978-3-8007-6203-3 (Cited on p. 125).

[32] C. Yuan, A. Schutz, D. Hohlfeld, and T. Bechtold, *Matrix Interpolation-Based Parametric Model Order Reduction of a Miniaturized Electromagnetic Energy Harvester Model*, in *PowerMEMS 2023 - 2023 IEEE 22nd International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications*, Institute of Electrical and Electronics Engineers Inc., 2023, pp. 52–55, ISBN: 9798350344219 (Cited on p. 125).

[33] G. Kerschen, J. C. Golinval, A. F. Vakakis, and L. A. Bergman, *The method of proper orthogonal decomposition for dynamical characterization and order reduction of mechanical systems: An overview*, *Nonlinear Dynamics*, vol. 41, no. 1-3, pp. 147–169, Aug. 2005, ISSN: 0924090X (Cited on p. 125).

[34] R. J. Guyan, *Reduction of stiffness and mass matrices*, *AIAA Journal*, vol. 3, no. 2, p. 380, May 1965, ISSN: 00011452 (Cited on p. 125).

[35] R. Kumar, S. F. Ali, and S. Gupta, *Static condensation based reduced order modelling of stochastically parametered large ordered systems*, *Probabilistic Engineering Mechanics*, vol. 66, p. 103 166, Oct. 2021, ISSN: 0266-8920 (Cited on p. 125).

[36] ANSYS Incorporation, *Multipoint Constraints and Assemblies*, 2023 (Cited on pp. 129, 131, 134).

7

Conclusion and Future Outlook

This chapter summarises the main conclusions of the work presented in this thesis while considering the research objectives postulated in Section 1.6 and provides recommendations for future steps of research in this field.

7.1. Concluding Remarks

This dissertation aims to demonstrate a new-generation approach to reliability estimation using a Digital Twin-based framework for Prognostics and Health Management (PHM) of electronic components and systems. The newly proposed framework with two branches — physics-based and data-driven modelling — highlights the technological requirements, which are explored in the last three chapters of this thesis. Below are the topic-wise conclusions drawn from the performed research.

Digital Twin Framework for PHM

The term Digital Twin (DT) has been used widely in the last 5–7 years. However, it faces big fragmentation in its definitions and the models due to its application-specific, deep contextualisation. It is essential to have a new, standardised, comprehensive, and yet generalised definition of a Digital Twin. This has been addressed in Chapter 2 to achieve the first research objective (*Objective 1*) of this dissertation.

It is important to note that the different types of DT implementations (viz., DTP, DTI, and DTA) apply to different phases of a product's lifecycle. It is, thus, crucial to specify the type when reporting on a work because it helps clarify the complexity and the technological backbone of that implementation. A hybrid approach is

feasible by combining the aforementioned two modelling approaches to a varying capacity and in a number of ways. This pertains to the *Objective 2*, which is also addressed in Chapter 2 by the introduction of a Digital Twin-based framework for PHM with a two-branched modelling approach that facilitates hybrid modelling.

Move to Physics-of-Degradation

Identical electronic components can have non-identical environmental and operational load profiles, which leads to a variation in their lifetimes. The three dominant stress factors — temperature, humidity, and mechanical vibrations — have their individual as well as combined effects on material ageing and acceleration of mechanical failure modes. It is crucial to identify the most critical stress-factor(s), degradation mechanism(s), and failure mode(s) for an electronic component for a certain application. Chapter 3 delves into this by exploring modern electronic packages, encapsulation materials, degradation mechanisms, and mechanical failures.

Developing detailed physics-based models replicating the quantified gradual degenerative changes in materials is of high significance. New types of experimental, analysis, and equivalent-modelling techniques are necessary to achieve good-quality physics-of-degradation models. Chapter 4 demonstrates a detailed (geometry and material) modelling procedure to create a continuously updated thermomechanical model of an encapsulated electronic package undergoing thermal ageing. Thus, the Chapters 3 and 4 meet the *Objective 3* concerning the topic of physics-of-degradation.

In-situ Monitoring

In-situ, continuous condition monitoring is a key building block of the PHM framework and an essential element in continuously updated Digital Twin models. New types of sensors and measurement techniques need to be developed and integrated into electronic systems. In-situ monitoring can detect several states of degradation, which can be used to determine the remaining useful life of the component before the actual failure. To facilitate this, appropriate edge-computing hardware and Reduced-Order Models (ROMs) are necessary. Chapter 3 describes the hardware requirements, including specialised sensors and edge-computing application processors, to realise in-situ degradation monitoring; whereas Chapter 6 delves into the software aspect by discussing different techniques for reduced-order modelling.

To achieve in-situ monitoring, certain packaging types can be cleverly utilised for extracting additional data at a certain material layer. This is demonstrated in Chapter 5 by utilising a WLCSP to monitor changes in mechanical stresses and to detect failure in solder joints. Thus, the setup developed and experiments conducted in Chapter 5 and parts of Chapters 3 and 6 collectively achieve the target described in the *Objective 4* of this thesis.

COMPACT MODELS

Compact models can be prepared by different model order reduction techniques. Some are key in facilitating edge-based DT services, while others help protect the intellectual property of a Full-Order Model (FOM). While thermal and electrical ROMs are an industry norm, thermomechanical ROMs are not. They need new standards for model order reduction techniques, file formats, and data exchange. Chapter 6 demonstrates a superelement-based thermomechanical ROM generation technique which utilises 'mechanical ports', *i.e.*, master nodes that connect to the geometry using multi-point constraint equations.

ROMs are not necessarily always computationally more efficient. The overhead for ROM generation and its integration into FOM can overpower the actual computational run. The location, definition, and the involved materials of the ROM-FOM interface play a crucial role in the resulting accuracy and efficiency of a ROM-integrated FOM. This is exhibited in the virtual design of experiments devised around the first test case presented in Chapter 6.

A complex FOM can benefit from the efficiency gains of ROM-based simulations when the original full model is complex and the ROM-FOM interfaces are well optimised. At the same time, the temperature-dependency of the materials involved in the reduced geometry could be a limitation of linear superelements and may require advanced techniques to capture the non-linear effects. The second test case in Chapter 6 demonstrates this, while achieving the crucial goal of IP protection. In this way, the *Objective 5* and *6* of this dissertation are addressed.

7.2. RECOMMENDATIONS

This dissertation sets a baseline for implementing the Digital Twin technology for microelectronics reliability. The Digital Twin-based PHM framework needs several technological advancements and new modelling techniques. The last three chapters of this thesis touch upon a few key aspects of the two-branched DT model, primarily in the 'prototype' and 'instance' phases of the Digital Twin (*i.e.*, DTP and DTI). The natural evolution of this work is a move towards a Digital Twin Aggregate (DTA).

The DTA phase relies heavily on the data-driven modelling approach. It requires different kinds of reduced-order models that are computationally inexpensive and run on edge-computing hardware. In addition, there is room for more work in preparing other physics-based degradation models. Further research can be conducted by expanding on the key pillars of this dissertation.

Considering this, the following recommendations are made for future work:

- **Physics-based models:** This thesis explores different stress-factors and their effects on material degradation and mechanical failures, and then dives deep into modelling the physics-of-degradation of one mechanism — thermal ageing of moulding compounds. Similar continuously updated models that consider the effects of other dominant stress-factors (*i.e.*, humidity and mechanical vibrations) should also be built. It has also been deduced that the impact of a coupled load with multiple stress-factors has a greater impact on resulting mechanical stresses compared to the sum of the individual ones. Thus, models for these interactions should also be prepared for integrating competing failure modes into the DT models.
- **Data-driven models:** In order to realise the DTA phase, preparing efficient data-driven models is essential. These models can be prepared using techniques such as response surface-based metamodels, Artificial Neural Network (ANN)-based Deep Learning models, and other Machine Learning-based regression models. The data on which these models would be trained could be generated using additional experiments, the prepared physics-based models (the DTI), or even a combination of both.
- **The hardware:** The compact models could be run on the edge-computing hardware built with the help of the requirements and the part list included in this thesis. The models could be tested starting with a slightly more powerful system, such as a Single-Board Computer (SBC), and then moving towards a more power-efficient microcontroller (MCU)-based system.
- **ROM-integrated FOMs:** The biggest challenge with these types of compact models in the thermomechanical domain is to balance efficiency and accuracy. This could be addressed by looking into ways to improve the mathematical formulation of the ROM and the computer science (code) behind the data exchange. Moreover, additional, yet-to-be-established features such as temperature dependency and nonlinearity for such ROMs could also be explored.
- **Beyond deterministic modelling:** The inclusion of stochastic modelling in the physics-based approach could be used to study the effects of the dimensional uncertainty and variation in material properties. The modelling can also benefit from the use of Generative AI, which could on-demand generate (*i.e.*, prepare, change, and refine) CAD geometries and discretised domain meshes.

A

Appendix A: Supplemental Information to Chapter 3

Specifications of Sensors and Components

A set of sensors and components were selected for the test-board reference design presented in Chapter 3. The specifications are listed in the tables below.

Type	Humidity and Temperature
Sensor	Relative Humidity + Temperature
Description	SHT4x is a digital sensor platform for measuring relative humidity and temperature at different accuracy classes. Its I2C interface provides several preconfigured I2C addresses while maintaining an ultra-low power budget (0.4 µW).
Manufacturer	Sensirion
Part Number	SHT40
Accuracy	±1.0 % RH, ±0.1 °C
Range	0 to 100 %RH, −40 °C to 125 °C
Temperature Range	−40 °C to 125 °C
Link / Datasheet	https://sensirion.com/media/documents/33FD6951/662A593A/HT_DS_Datasheet_SHT4x.pdf

Type	IMU
Sensor	Accelerometer (high range)

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Description	The analog output ADXL356 and the digital output ADXL357 are low noise density, low 0 *g* offset drift, low power, 3-axis accelerometers with selectable measurement ranges. The ADXL356/ADXL357 offer industry leading noise, minimal offset drift over temperature, and long-term stability, enabling precision applications with minimal calibration.
Manufacturer	Analogue Devices
Part Number	ADXL356 ADXL357
Range	±10 *g*, ±20 *g*, and ±40 *g*
Sensitivity	51200 LSB/*g*, 25600 LSB/*g*, 12800 LSB/*g* for x, y, and z-axis
Temperature Range	−40 °C to 125 °C
Link / Datasheet	https://www.analog.com/media/en/technical-documentation/data-sheets/adxl356-357.pdf

Type	IMU
Sensor	Accelerometer (low range)
Description	The SCA3300-D01 is a high performance accelerometer sensor component. It is a three-axis accelerometer sensor based on Murata's proven capacitive 3D-MEMS technology.
Manufacturer	MURATA
Part Number	SCA3300-D01-1
Range	±1.5 *g*, ±3 *g*, ±6 *g*
Sensitivity	5400 LSB/*g*, 2700 LSB/*g*, 1350 LSB/*g*
Temperature Range	−40 °C to 125 °C
Link / Datasheet	https://eu.mouser.com/datasheet/2/281/Murata_datasheet_sca3300_d01-1890566.pdf

Type	IMU
Sensor	Gyroscope + Accelerometer
Description	The IIM-42652 is a 6-axis SmartIndustrial MotionTracking device that supports an extended operating temperature range. It consists of a 3-axis accelerometer and a 3-axis gyroscope.
Manufacturer	TDK InvenSense

Part Number	IIM-42652
Range	±2 *g*, ±4 *g*, ±8 *g*, ±16 *g*; ±2000 dps, ±1000 dps, ±500 dps, ±250 dps, ±125 dps, ±62.5 dps, ±31.25 dps, ±15.625 dps
Sensitivity	16384 LSB/*g*, 8192 LSB/*g*, 4096 LSB/*g*, 2048 LSB/*g*; 60.97 mdps/LSB, 30.48 mdps/LSB, 15.26 mdps/LSB, 7.63 mdps/LSB, 3.81 mdps/LSB, 1.90 mdps/LSB, 0.95 mdps/LSB, 0.47 mdps/LSB
Temperature Range	−40 °C to 105 °C
Link / Datasheet	https://invensense.tdk.com/products/smartindustrial/iim-42652/

Type	IMU
Sensor	Magnetometer
Description	The 3D magnetic sensor TLV493D-A1B6 offers accurate three-dimensional sensing with extremely low power consumption in a small 6-pin package. With its magnetic field detection in x, y, and z-direction the sensor reliably measures three-dimensional, linear and rotational movements.
Manufacturer	Infineon
Part Number	TLV493DA1B6HTSA2
Accuracy	±0.2 mT
Range	±130 mT
Sensitivity	10.2 LSB/mT
Temperature Range	−40 °C to 125 °C
Link / Datasheet	https://eu.mouser.com/datasheet/2/196/Infineon_TLV493D_A1B6_DataSheet_v01_10_EN-3363980.pdf

Type	Pressure
Sensor	Barometric Pressure
Description	The FXPS7115D4 is a high-performance, high-precision barometric absolute pressure (BAP) sensor consisting of a compact capacitive micro-electro-mechanical systems (MEMS) device coupled with a digital integrated circuit (IC) producing a fully calibrated digital output.
Manufacturer	NXP

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Part Number	FXPS7115DI4
Accuracy	±1.25 kPa, ±1.75 kPa, ±2.0 kPa
Range	40 to 115 kPa
Sensitivity	46.67 LSB/kPa (12-bit), 93.34 LSB/kPa (16-bit)
Temperature Range	−40 °C to 130 °C
Link / Datasheet	https://eu.mouser.com/datasheet/2/302/FXPS7115D4-1544418.pdf

Type	Deformation
Sensor	Strain Gauge
Description	The HBM strain gauge range consists of the Y, C, M, G series and special strain gauges. RF9 strain gauge rosette is suitable for PCB testing and small surfaces. Strain gauge matching all requirements is a RF91 (120 Ohm) tri-axial module with 5mm radius circular footprint.
Manufacturer	HBM
Part Number	RF91
Accuracy	±0.3 %, ±0.35 %, ±0.5 %
Range	120, 350, 700, 1000 Ω resistance
Sensitivity	Gauge factor $k = 2 \pm 1\%$
Temperature Range	−200 °C to 250 °C
Link / Datasheet	https://www.hbm.com/en/6367/rf9-miniature-rosette-for-mechanical-tests-on-printed-circuit-boards/

Type	Processing Unit
Sensor	Microprocessor including MCU
Description	The i.MX 7Dual family of processors features speeds of up to 1 GHz and 1.2 GHz. It provides up to 32-bit DDR3/DDR3L/LPDDR2/LPDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, and GPS. The i.MX7D uses heterogeneous processing with dual Arm Cortex-A7 cores and one Cortex-M4 core.
Manufacturer	NXP
Part Number	IMX7DCEC

Temperature Range	−20 °C to 105 °C (industrial version)
Link / Datasheet	https://www.nxp.com/docs/en/data-sheet/IMX7DCEC.pdf

Type	Connectivity and Data
Sensor	WiFi Chip
Description	The ESP8266 is a low-cost WiFi microchip, with a full TCP/IP stack and microcontroller capability. Used in ESP-01 module, made by a third-party manufacturer Ai-Thinker.
Manufacturer	Espressif Systems
Part Number	ESP8266
Range	WiFi: 802.11 b/g/n, clock speed: 80 MHz, 160 MHz
Temperature Range	−40 °C to 125 °C
Link / Datasheet	https://www.microchip.ua/wireless/esp01.pdf

Type	Indicator
Sensor	LED (RGB)
Description	WS2812, more commonly known as “neopixel"
Manufacturer	Worldsemi
Part Number	WS2812
Temperature Range	−25 °C to 80 °C
Link / Datasheet	https://cdn-shop.adafruit.com/datasheets/WS2812.pdf

B

Appendix B: Supplemental Information to Chapter 6

Additional Results of ROM-based Simulations

The DoE devised around the first test case for ROM-integrated FOM (Chapter 6) considers three different locations for the ROM-FOM interface, and the spatial plots of warpage are compared with that of the FOM (indicated in Figure 6.2). While Figure 6.6 indicates the simulation results for *Interface 1*, the comparison of spatial plots of warpage of the remaining FOM for all combinations of the MPC definitions for *Interface 2* and *Interface 3* is indicated in Figure B.1 and Figure B.2, respectively.

Script for Scaling Superelement Load Vector

In the ROM-integrated FOM setup, an effective thermomechanical load is applied at the master nodes of the imported superelement. This load vector is calculated at each temperature step in the defined thermal load. The SE generation step calculates the default thermomechanical load (force and moment) corresponding to the package deformations due to a unit temperature increase (*i.e.*, $\Delta T = 1\,^{\circ}\mathrm{C}$). A custom subroutine is utilised to scale the load vector as a function of temperature at different time steps, matching the temperature profile applied to the FOM subassembly. The script with *ANSYS APDL* commands was initially developed for the first test case and was later adopted for the second test case (refer to Section 6.5). The subroutine *APDL* script utilised for the second test case is indicated as follows.

```
! Active UNIT system:  Metric (m, kg, N, s, V, A)
!
TR=125
mydim = 5
*dim,mytable,table,mydim,,,time
mytable(1,0) = 0
mytable(1,1) = 180.0-TR
mytable(2,0) = 1
mytable(2,1) = 180.0-TR
mytable(3,0) = 60
mytable(3,1) = 175.0-TR
mytable(4,0) = 360
mytable(4,1) = 150.0-TR
mytable(5,0) = 660
mytable(5,1) = 125.0-TR
mytable(6,0) = 960
mytable(6,1) = 100.0-TR
mytable(7,0) = 1260
mytable(7,1) = 75.0-TR
mytable(8,0) = 1560
mytable(8,1) = 50.0-TR
mytable(9,0) = 1860
mytable(9,1) = 25.0-TR
mytable(10,0) = 2160
mytable(10,1) = 0.0-TR
mytable(11,0) = 2460
mytable(11,1) = -25.0-TR
mytable(12,0) = 2640
mytable(12,1) = -40.0-TR
!*vplot,mytable(1,0),mytable(1,1)
!
esel,s,enam,,50
*GET,num_elem,ELEM,,COUNT
eid=0
*DO,i,1,num_elem
  eid = elnext(eid)
  sfe,eid,1,selv,0,%mytable%
*ENDDO
alls
```

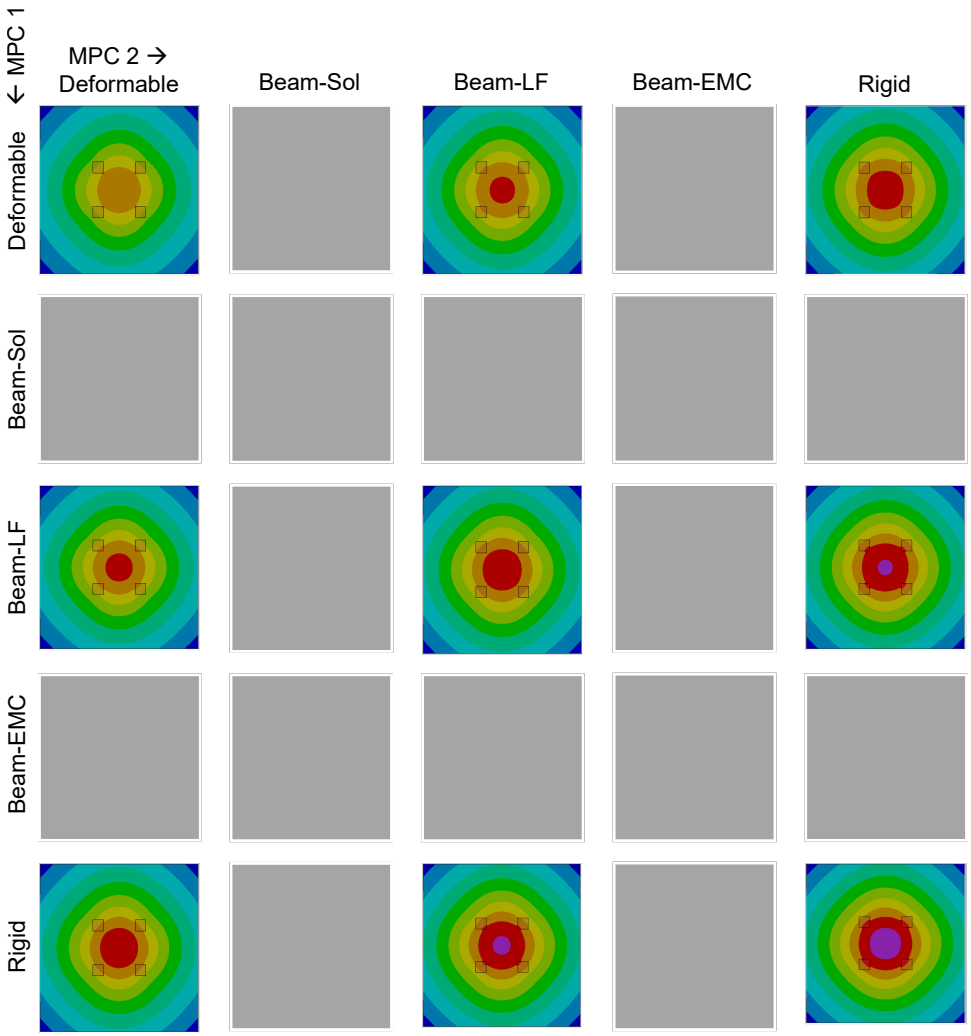

Figure B.1: The comparison of spatial plots of warpage (identical scale as Figure 6.2 for all subplots) of the solder-PCB subassembly (remaining FOM) for all combinations of the MPC definitions for *Interface 2*.

B

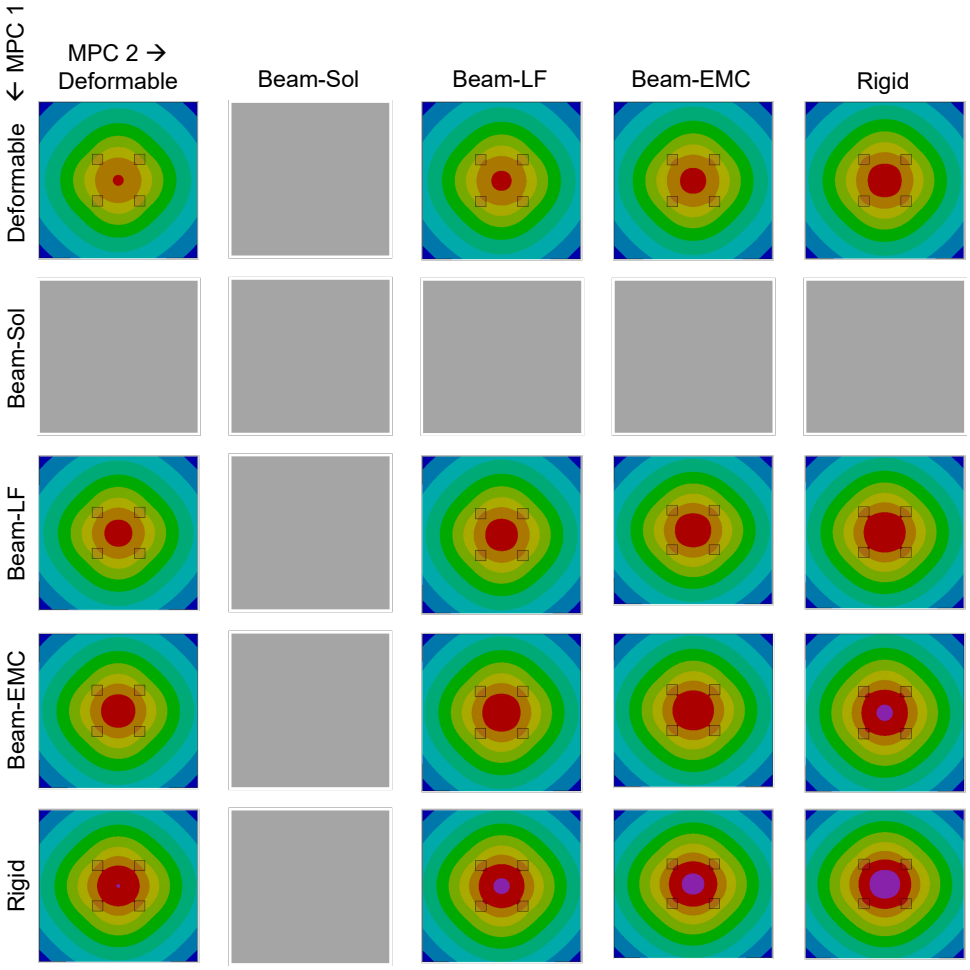

Figure B.2: The comparison of spatial plots of warpage (identical scale as Figure 6.2 for all subplots) of the solder-PCB subassembly (remaining FOM) for all combinations of the MPC definitions for *Interface 3*.

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Writing a PhD thesis is an exercise of going back in time, reading through the notes made and documents collected over the past few years, and making sense of every piece of work done and seeing how (dis)similar the overall story is now compared to the initial plans. It is also an opportunity to recall the challenges faced and realise what could be learned from this journey. No journey is truly solitary, and it's the people around one who actually help shape it through their efforts, support, and sometimes, mere presence. Thus, I would like to take this opportunity to thank everyone who supported me and contributed to my work and personal life.

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I got to work and collaborate with colleagues at NXP Semiconductors, Nijmegen.

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Adwait
Delft, September 2025

Curriculum Vitæ

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02-02-1993 Born in Thane, Maharashtra, India

Education

2011-2015 **Bachelor of Technology (B.Tech.) in Mechanical Engineering**
Visvesvaraya National Institute of Technology, Nagpur, India
Thesis: "Design and Development of Low Cost Silicone Implant for Augmentation Rhinoplasty"

2016-2020 **Master of Science (M.Sc.) in Computational Engineering**
Ruhr-University Bochum, Germany
Thesis: "Modelling and Validation of In-Situ Stress Measurement ASIC Module using Finite Element and Experimental Methods"

2020-2025 **Doctor of Philosophy (Ph.D.) in Microelectronics Reliability**
Delft University of Technology, The Netherlands
Thesis: "Digital Twin Technology for Microelectonics Reliability"
Promoters: Prof. dr. G.Q. Zhang and Prof. dr. ir. W.D. van Driel

Achievements

2017 **German National Scholarship** (*Deutschlandstipendium*)
Federal Ministry of Research, Technology and Space (*BMBF*), Ruhr-University Bochum, and Evonik Stiftung

2025 **Certificate of Achievement**
IEEE Electronics Packaging Society

Experience

2014-2016	**TATA Motors, Pune, India** Internship (May 2014 – Jul 2014) Graduate Engineering Trainee (Aug 2015 – Jan 2016)
2017-2018	**Ruhr-University Bochum, Germany** Research Assistant (*HiWi*) (Apr 2017 – Apr 2018)
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Certificates

2015	**Computational Fluid Dynamics (CFD) with OpenFOAM** Visvesvaraya National Institute of Technology Nagpur
2021	**Machine Learning** Stanford University
2021	**Introduction to Embedded Machine Learning** Edge Impulse (a Qualcomm Company)
2023	**Semiconductor Process Integration Training** Else Kooi Laboratory, Delft University of Technology
2024	**Introduction to Device and System Packaging** Birla Institute of Technology and Science Pilani

List of Publications

Journal Papers

1. **A. Inamdar**, W.D. van Driel, and G.Q. Zhang, *Electronics Packaging Materials and Component-level Degradation Monitoring*, Frontiers in Electronics, **6**, 1506112 (2025).

2. M. van Soestbergen, **A. Inamdar**, O. Vermesan, J. Niehaus, F. Wotawa, and G. Stettinger, *Driving the Future: A Perspective on Electronic Safety in Autonomous Vehicles*, IEEE Transactions on Intelligent Vehicles, (*submitted*).

3. L. Guo, **A. Inamdar**, W.D. van Driel, and G.Q. Zhang, *Adaptive Bayesian Data-Driven Design of Reliable Solder Joints for Micro-electronic Devices*, Applied Mathematical Modelling, (*submitted*), preprint available on arXiv.

4. **A. Inamdar**, W.D. van Driel, and G.Q. Zhang, *Digital Twin Technology – A Review and Its Application Model for Prognostics and Health Management of Microelectronics*, Electronics, **13**(16), 3255 (2024).

5. **A. Inamdar**, M. van Soestbergen, A. Mavinkurve, W.D. van Driel, and G.Q. Zhang, *Modelling Thermomechanical Degradation of Moulded Electronic Packages using Physics-based Digital Twin*, Microelectronics Reliability, **157**, 115-416 (2024).

6. V. Guerra, B. Hamon, B. Bataillou, **A. Inamdar**, and W.D. van Driel, *Towards A Digital Twin Architecture for the Lighting Industry*, Future Generation Computer Systems, **155**, 80–95 (2024).

7. **A. Inamdar**, Y.H. Yang, A. Prisacaru, P. Gromala, and B. Han, *High Temperature Aging of Epoxy-based Molding Compound and its Effect on Mechanical Behavior of Molded Electronic Package*, Polymer Degradation and Stability, **188**, 109572 (2021).

8. **A. Inamdar**, N. Adhe, S. Shende, R.V. Uddanwadiker, and S.N. Lulay *Design and Development of Low Cost Silicone Implant Used in Augmentation Rhinoplasty Suitable for the Indian Sub-continental Population*, International Journal of Pharma

Medicine and Biological Sciences, **5**, 81-85 (2016), and in International Conference on Biomedical Engineering (ICBET) 2016.

Conference Papers

1. S.D.M. de Jong, **A. Inamdar**, W.D. van Driel, and G.Q. Zhang, *Prediction of Void-induced Crack Propagation within Underfill using the Meshless Material Point Method*, IEEE 27th Electronics Packaging Technology Conference (EPTC) 2025, Singapore, (*accepted*).

2. **A. Inamdar**, P. Gromala, C. Bailey, L. Nguyen, B. Chan, J.E. Ryu, F. Rezaie, A. Detofsky, W.D. van Driel, and G.Q. Zhang, *Digital Twins for IC Packages and Electronics-enabled Systems*, IEEE Smart World Congress (SWC) 2024, Denarau Island, Fiji.

3. M. Musadiq, **A. Inamdar**, R. Roucou, and W. D. van Driel, *Investigating Competing Failure Modes in Microelectronic Devices Due to Small Temperature Variations*, IEEE 10th Electronics System-Integration Technology Conference (ESTC) 2024, Berlin, Germany.

4. **A. Inamdar**, V. Thukral, L. Zhang, J.J.M. Zaal, M. Van Soestbergen, H. Tuinhout, W.D. van Driel, and G.Q. Zhang *Characterization of a Piezoresistive Sensor for In-Situ Health Monitoring of Solder Bumps*, IEEE 74th Electronic Components and Technology Conference (ECTC) 2024, Denver, USA.

5. **A. Inamdar**, T. Hauck, M. van Soestbergen, W.D. van Driel, and G.Q. Zhang *ROM-FOM Interface Optimization for Efficient Thermomechanical Simulations of Electronic Components*, IEEE 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE) 2024, Catania, Italy.

6. **A. Inamdar**, M. van Soestbergen, A. Mavinkurve, W.D. van Driel, and G.Q. Zhang, *A Continuously Updated Package-Degradation Model reflecting Thermomechanical Changes at Different Thermo-Oxidative Stages of Moulding Compound*, IEEE 24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE) 2023, Graz, Austria.

7. **A. Inamdar**, A. Prisacaru, M. Fleischman, E. Franieck, P. Gromala, A. Veres, C. Nemeth, Y.H. Yang, and B. Han, *Study of Thermal Aging Behavior of Epoxy Molding Compound for Applications in Harsh Environments*, IEEE 69th Electronic Components and Technology Conference (ECTC) 2019, Las Vegas, USA.

Book Chapters

1. H. Moeller, **A. Inamdar**, W.D. van Driel, J. Bredberg, P. Hille, H. Knoll, B. Vandevelde, *Digital Twin Technology in Electronics*, Recent Advances in Microelectronics Reliability, Springer International Publishing, ISBN: 978-3-031-59361-1 (2024).

2. **A. Inamdar**, P. Gromala, A. Prisacaru, A. Kabakchiev, Y.H. Yang, and B. Han, *EMC Oxidation Under High-Temperature Aging*, Reliability of Organic Compounds in Microelectronics and Optoelectronics: From Physics-of-Failure to Physics-of-Degradation, Springer International Publishing, ISBN: 978-3-030-81576-9 (2022).

3. P. Gromala, **A. Inamdar**, A. Prisacaru, M. Dressler, and A. Kabakchiev, *Degradation and Remaining Useful Life Prediction of Automotive Electronics*, Reliability of Organic Compounds in Microelectronics and Optoelectronics: From Physics-of-Failure to Physics-of-Degradation, Springer International Publishing, ISBN: 978-3-030-81576-9 (2022).

IEEE Newsletter Articles

1. P. Gromala, **A. Inamdar**, W.D. van Driel, G.Q. Zhang, C. Bailey, L. Nguyen, B. Chan, J.E. Ryu, F. Rezaie, and A. Detofsky, *Digital Twins for Electronics Packaging and Systems* [Article], IEEE Electronics Packaging Society Newsletter, November 2023.

2. **A. Inamdar**, P. Gromala, W.D. van Driel, and G.Q. Zhang, *Making the Digital Twin Work for Mission Critical Electronics* [Article], IEEE Electronics Packaging Society Newsletter, July 2022.

Talks and Posters

1. **A. Inamdar**, W.D. van Driel, and G.Q. Zhang, *Digital Twin-Based Hybrid PHM Framework for Monitoring Package-Level Degradation* [Talk], 33rd European Safety and Reliability Conference (ESREL) 2023, Southampton, UK.

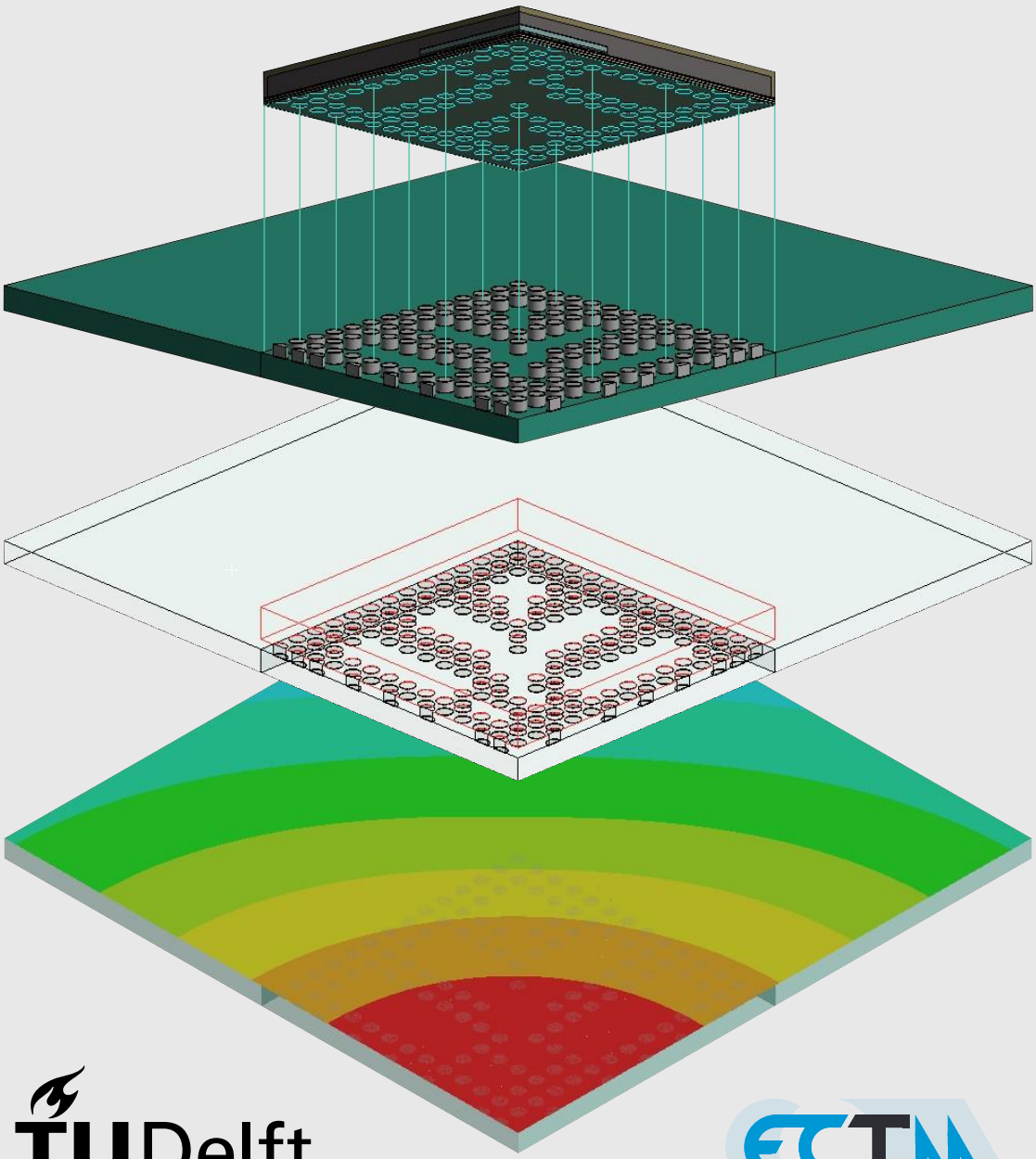
2. **A. Inamdar**, W.D. van Driel, and G.Q. Zhang, *Monitoring Thermomechanical Degradation of Electronic Packages – A Hybrid Digital Twinning Approach* [Poster], ASME International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems (InterPACK) 2023, San Diego, USA.

3. **A. Inamdar**, W.D. van Driel, and G.Q. Zhang, *Digital Twin-based Hybrid PHM Framework for Monitoring Package-level Degradation* [Talk], ASML Reliability Seminar (ARES) 2023, Eindhoven, Netherlands.

PATENT

1. R.V. Uddanwadiker, N. Adhe, **A. Inamdar**, S. Shende, S.N. Lulay, *Indigenously Manufactured Nasal Implants suitable for Indian Demography*, Indian Patent application 2067/MUM/2015 filed on 27-05-2015, Indian Patent Number 392019 granted on 15-03-2022.

A Digital Twin is a continuously updated multi-physics, multiscale, probabilistic simulation model of a physical entity (an object, a system, or a process) utilising big data, bilateral connectivity, and advanced software analytics to provide monitoring, diagnostics, prognostics, and optimisation services.



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