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Fundamentals of Cryo-CMOS Circuits and Systems for Quantum Computing

*Challenges and prospects in interfacing
future quantum computers*

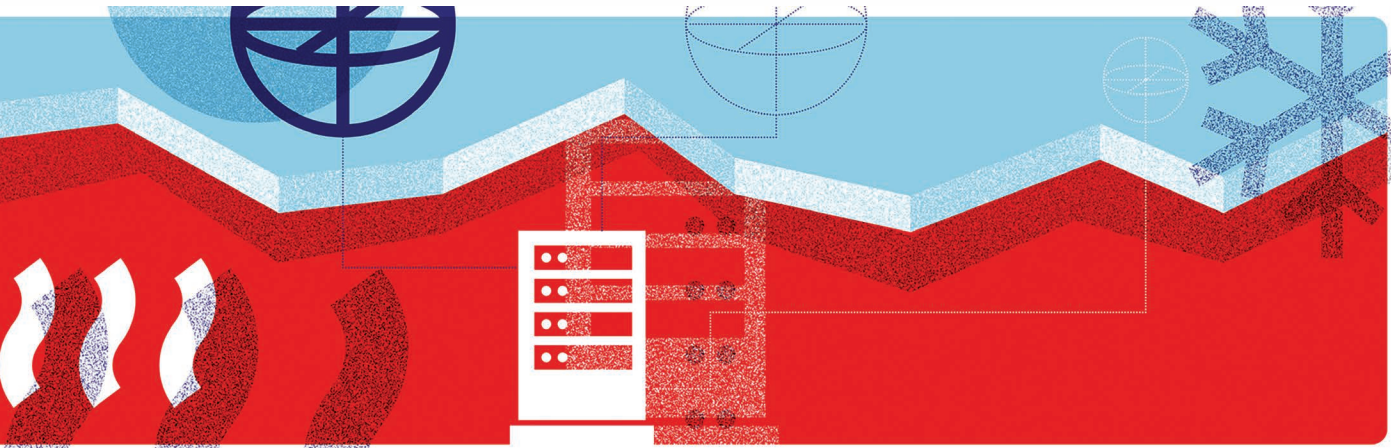
 uantum computing holds the potential to solve problems beyond the capabilities of classical computers. However, realizing practical large-scale quantum computers faces critical challenges, including

the key bottleneck in wiring quantum processors operating at cryogenic temperatures to their room temperature control electronics. This article explores cryo-CMOS ICs as an enabling technology to circumvent such a wiring bottleneck. After reviewing the basics of quantum computing and the behavior of CMOS devices at cryogenic temperatures, the requirements for the interface electronics for

superconducting and semiconductor qubits are discussed, and state-of-the-art cryo-CMOS circuit solutions are briefly described, including a few hints to other qubit platforms. Finally, the article concludes with an overview of future challenges to be addressed to realize the vision of cryo-CMOS technology as an enabler of large-scale quantum computers with practical applications.

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Toward Practical Large-Scale Quantum Computers

Quantum computers promise to solve computational problems that will always be impractical for classical computers, thus potentially unlocking scientific and industrial advancements in several fields,

such as chemistry [1], health, and medicine [1], [2], [3]. As a result, research on quantum computing has attracted increasing scientific interest and investments in the past decade, including growing attention in the solid-state circuit community. After quickly reviewing the

basics of quantum computing, this article illustrates the role of ICs operating at cryogenic temperatures as a key enabling technology for developing application-ready quantum computers.

The fundamental unit of computation in quantum computers is the quantum bit, or qubit, which, unlike classical bits, can assume not only the value of the quantum states $|0\rangle$ or $|1\rangle$ but also a superposition of those two states, as shown in Figure 1(a) and (b). Although superposition may seem a straightforward way to achieve parallelism by simultaneously operating on all possible values of a qubit register, it is not sufficient, as it is impossible to read a quantum superposition deterministically [Figure 1(d)]. However, when coupling superposition with quantum entanglement, some algorithms can be devised that achieve a speedup with respect to their classical nonquantum alternatives [4], [5]. While not every algorithm can be accelerated by a quantum computer, the limited set of quantum algorithms discovered so far is still very relevant for quantum computing target applications and fully motivates their development.

To implement this speedup in practice, several qubit hardware platforms are currently competing, including superconducting qubits, spin qubits in semiconductors, spin qubits in diamonds, ion traps, and many others. The most intuitive metric to benchmark those platforms is the number of available qubits, which directly maps to the available computational power. Since the simplest quantum algorithms with a practical application that can beat a supercomputer ask for only hundreds or thousands of qubits [6], [7], this seems within reach of current quantum processors, which showcase hundreds of qubits. However, due to unwanted coupling with the environment, the qubits show nonideal behavior, which can hamper the correct algorithm execution. Such a behavior can be measured by the qubits' fidelity metric being significantly below

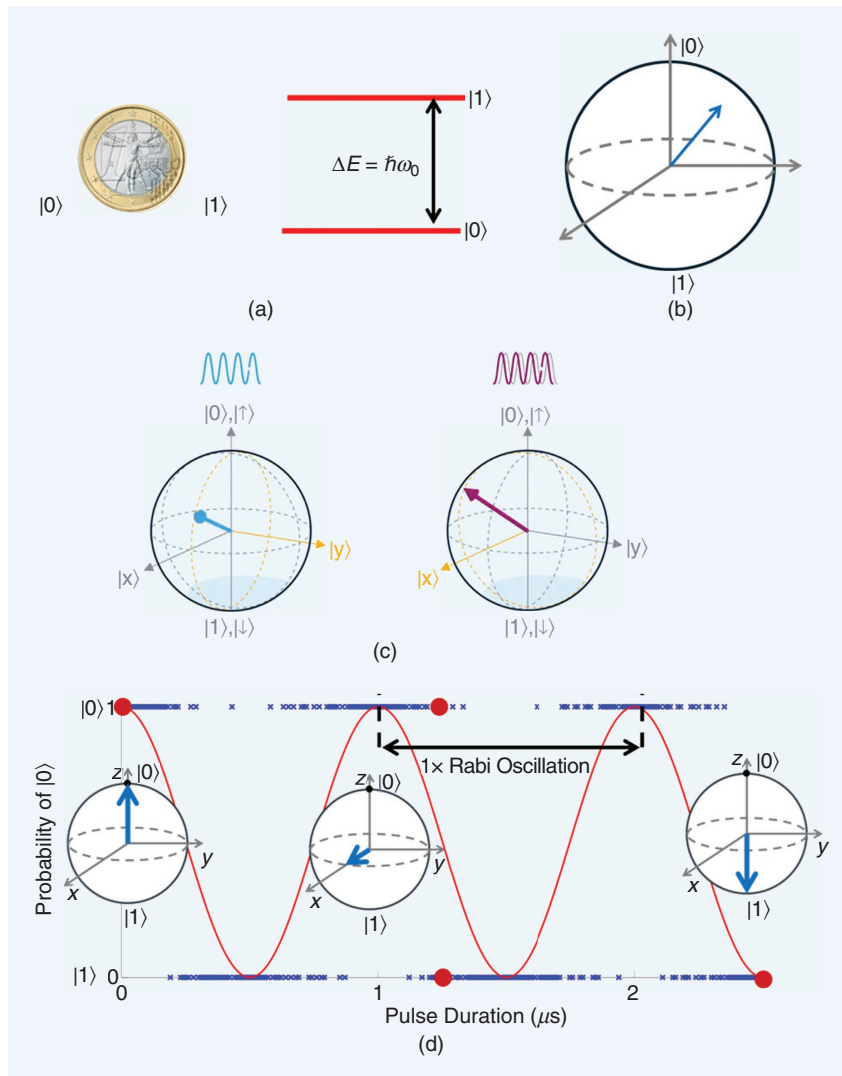


FIGURE 1: Qubit basics. (a) Unlike a conventional bit, a qubit can be in a superposition of two states, e.g., heads or tails, or the quantum states $|0\rangle$ or $|1\rangle$, and can be encoded in a two-level quantum system. (b) The qubit state can be represented as a point on the Bloch sphere, with $|0\rangle$ or $|1\rangle$ at the sphere's north pole and south pole, respectively, and any other point representing a superposition state. (c) An operation on a single qubit is represented by a rotation on the Bloch sphere and can be driven by a signal resonating with the qubit Larmor frequency ω_0 . The signal's phase determines the rotation axis; e.g., a zero phase shift results in a rotation around the y-axis (left), while a 90° phase shift results in a rotation around the x-axis (right). The amplitude and duration of the exciting pulse determine the rotation angle; see also [75]. (d) When applying a pulse with varying duration, the qubit will rotate on the Bloch sphere. After the pulse is applied, measuring the qubit results in reading either $|0\rangle$ or $|1\rangle$. Unless the qubit is exactly on the north pole or the south pole of the Bloch sphere, the measurement results in a random $|0\rangle$ or $|1\rangle$ (blue crosses). When averaging over several experiments, the measurement probability ideally converges to a sinusoid, the so-called Rabi oscillation, since the statistics of such stochastic measurement depend on the qubit state.

100%. Quantum error correction (QEC) has, then, been introduced to compensate with redundancy for the limited qubit fidelity, i.e., using up to thousands of physical qubits to encode a single logical, i.e., perfect, qubit, similar to conventional error correction schemes [7], [8], [9]. As a consequence, although alternative approaches exploiting imperfect qubits are being explored [10], [11], [12], quantum processors should offer millions of qubits to keep the promise of quantum speedup.

Next to the formidable engineering challenge to scale up quantum processors from hundreds to millions of qubits while increasing their fidelity, another bottleneck appears on the horizon. As described in Figure 1(c) and (d), qubits are typically controlled and read out by applying and detecting electrical—and sometimes optical—signals. Today, those signals are typically generated and acquired by electronic equipment operating at room temperature and routed to the qubits, which are cooled down to cryogenic temperatures to show their quantum behavior. While this approach is feasible for the few hundred qubits available today, it is hardly scalable to millions of qubits. Considering that one or two wires are typically required per qubit, as shown later in the article, the room temperature electronic interface must be carefully engineered [11], [13], [14]. Even if such a room temperature interface were developed for millions of qubits, millions of meter-long cables would have to be wired through a cryogenic refrigerator to the qubits. While several not-so-compelling arguments against such an approach have been listed, including cost, propagation delay, and the heat conducted through the wires into the refrigerator, the wires' impractical size and limited reliability impose a stringent wiring bottleneck for quantum processors beyond a few thousand qubits.

To circumvent such a bottleneck, the electronic interface could be operated close to the cryogenic qubits,

Quantum computing has attracted increasing scientific interest and investments in the past decade, including growing attention in the solid-state circuit community.

but that would require electronics that were integrated to fit in the cryostat and operate at cryogenic temperature due to the proximity to the cryogenic qubits. Several challenges must be overcome to develop such an integrated cryogenic electronic interface to support large-scale quantum computers. First, the electronic performance should not limit the qubit fidelity. Defining the electrical specifications accordingly is not trivial, as it requires quantum/classical analysis and cosimulations [16], [17]. Next, the power dissipation of the electronics is limited by the cooling power of the cryostat, which typically offers only a few milliwatts at sub-Kelvin temperatures. For this reason, cryogenic electronics often operate at higher temperatures (1–4 K), where watts of cooling power are available. Finally, a cryogenic technology must be used. Among several alternatives, the adoption of devices fabricated with commercial CMOS technologies and operating at cryogenic temperatures, i.e., cryo-CMOS, has emerged as a preferred solution thanks to the very low operating temperature and the unique capability to integrate the high-complexity SoCs required to drive millions of qubits [11], [19].

Cryo-CMOS Device Performance

Surprisingly, transistors fabricated in commercial CMOS processes still behave as good transistors [Figure 2(a)]. However, the increased threshold voltage at cryogenic temperatures—typically up to 100–200 mV—may cause voltage headroom limitations, although techniques have been proposed to reduce the cryogenic threshold shift, such as aggressive back biasing in FDSOI [20] and cryogenic-aware forward body biasing in bulk CMOS [21]. Despite the higher

threshold, the higher carrier mobility enhances the transistor current driving capability. When looking into weak inversion, the higher subthreshold slope offers an improved transconductance efficiency that can be exploited for low-power design [Figure 2(b)]. However, operation in the deep subthreshold is discouraged by the degraded matching, which is worse for all operating regimes but particularly in weak inversion [Figure 2(c)] [22], [23], [24], [25], [26], [27]. Integrated passive components are still usable at cryogenic temperatures: polysilicon resistors properly operate despite a nonnegligible variation in their resistivity [28]; inductors and capacitors show only minimal variations in their nominal value, while benefiting from a nonnegligible increase in the quality factor thanks to the freeze out-induced higher substrate impedance and higher metallization conductivity [29]. For similar reasons, transistor parasitics have a lower effect at cryogenic temperatures, which, coupled to the increased current, leads to a general increase in speed. As expected, thermal noise decreases at lower temperatures, but the improvement saturates at cryogenic temperatures, possibly due to shot noise or device self-heating [30]. This is corroborated by the significant observed self-heating and thermal crosstalk, which could also hinder cointegration with qubits [31], [32], [33], [34]. No general trend has been observed for low-frequency noise [35], [36], [37].

Although most of the device physics is well understood, some effects, such as the noise behavior, still lack a comprehensive characterization, while others, such as mismatch and the saturation of the subthreshold

slope, still miss a complete physical model. Most affecting circuit designers is the lack of a standard cryogenic device model usable in simulation. Designers can, then, validate their circuits only at the lowest temperature offered by the process design kit (−40 or −55 °C)

and extrapolate the change in performance (and bias point) using the available cryogenic characterization data. To bypass these limitations, tuning and calibration knobs are extensively used, and large design margins are left, although affecting the power efficiency. More de-

tails on cryo-CMOS modeling can be found in [38].

Cryo-CMOS Circuits for Quantum Processors

To identify the functionalities required of cryo-CMOS electronics to control a quantum processor, we can revisit the conditions necessary for quantum computation (as stated in DiVincenzo's criteria [39]) from a circuit designer's perspective. A quantum computer should offer

- **scalable qubits**, which require a qubit platform and qubit **biasing electronics**
- **a long qubit coherence time**, which requires the **electronics for QEC**
- **qubit initialization**, which is neglected here, as qubits can be initialized by measuring them and performing single-qubit operations, thus reusing the electronics dedicated to those operations
- a “universal” set of quantum gates:
 - **single-qubit operations**, which require **single-qubit driving electronics**
 - **two-qubit operations**, which require **two-qubit operation driving electronics**
- **qubit measurement**, which requires **readout electronics**.

In the following, we review the specifics of the above-mentioned electronic blocks for a few mainstream qubit platforms.

Superconducting Qubits

A parallel LC network behaves energetically as a harmonic oscillator with a parabolic energy profile. When cooling the circuit down to cryogenic temperatures, the energy states of the resonator become quantized, allowing the use of the two lowest-energy states to encode the qubit quantum states $|0\rangle$ and $|1\rangle$ [Figure 3(a)]. However, since more energy levels with the same energy spacing coexist in a purely harmonic oscillator, exciting the resonator with a frequency $\omega_{01} = \Delta E_{01}/\hbar$ could excite any of the

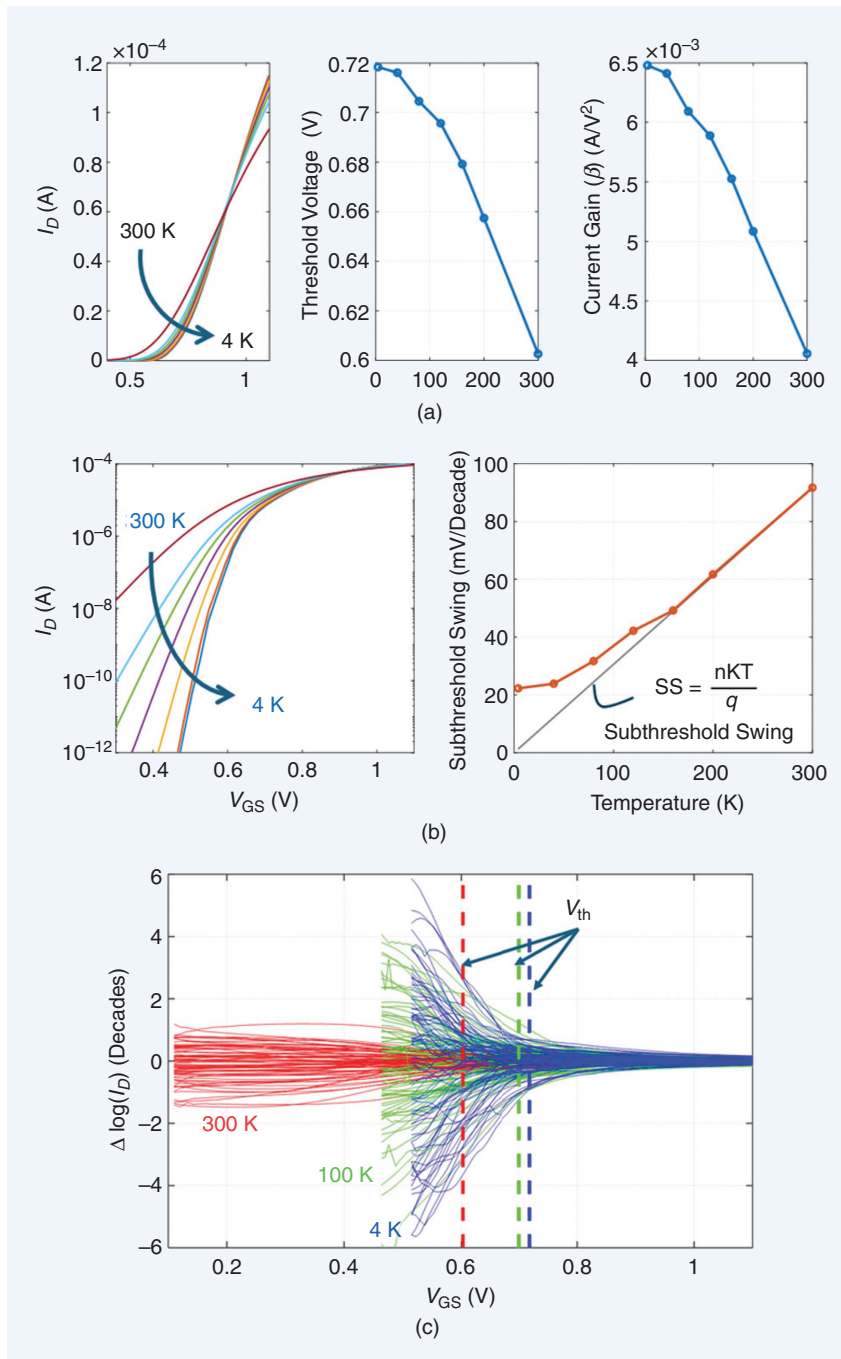


FIGURE 2: Cryo-CMOS device performance. (a) Data from a 40-nm NMOS transistor, highlighting the cryogenic threshold voltage shift and the increase in mobility. (b) Weak inversion behavior [using the data in (a)]. (c) The mismatch of a 40-nm NMOS pair over multiple samples at three different temperatures.

transitions, thus possibly bringing the resonator into a noncomputational state different from the wanted $|0\rangle$ and $|1\rangle$. This is avoided by replacing the inductor with a loop of two superconductor–insulator–superconductor Josephson junctions, which acts as a nonlinear inductor. As the energy profile is no longer parabolic, the uniformity of the energy level spacing is broken, making the transition energy ΔE_{01} unique. By applying a magnetic flux through the Josephson junction loop, the transition energy

Cryo-CMOS is an enabling technology that addresses the wiring bottleneck in large-scale quantum computers.

and, hence, the resonant frequency of the resonator, now implementing our superconducting qubit, can also be tuned. Such so-called flux bias can be set by inductively coupling a cryo-CMOS current generator [Figure 3(b)] that is used to implement several functionalities: **bi-**

resonance frequency, i.e., its Larmor frequency; pulsing the current for a short time to induce a temporary shift of the Larmor frequency to let the qubit rotate around the z-axis of the Bloch sphere, thus implementing a specific **single-qubit operation**; and pulsing the current to bring two coupled qubits

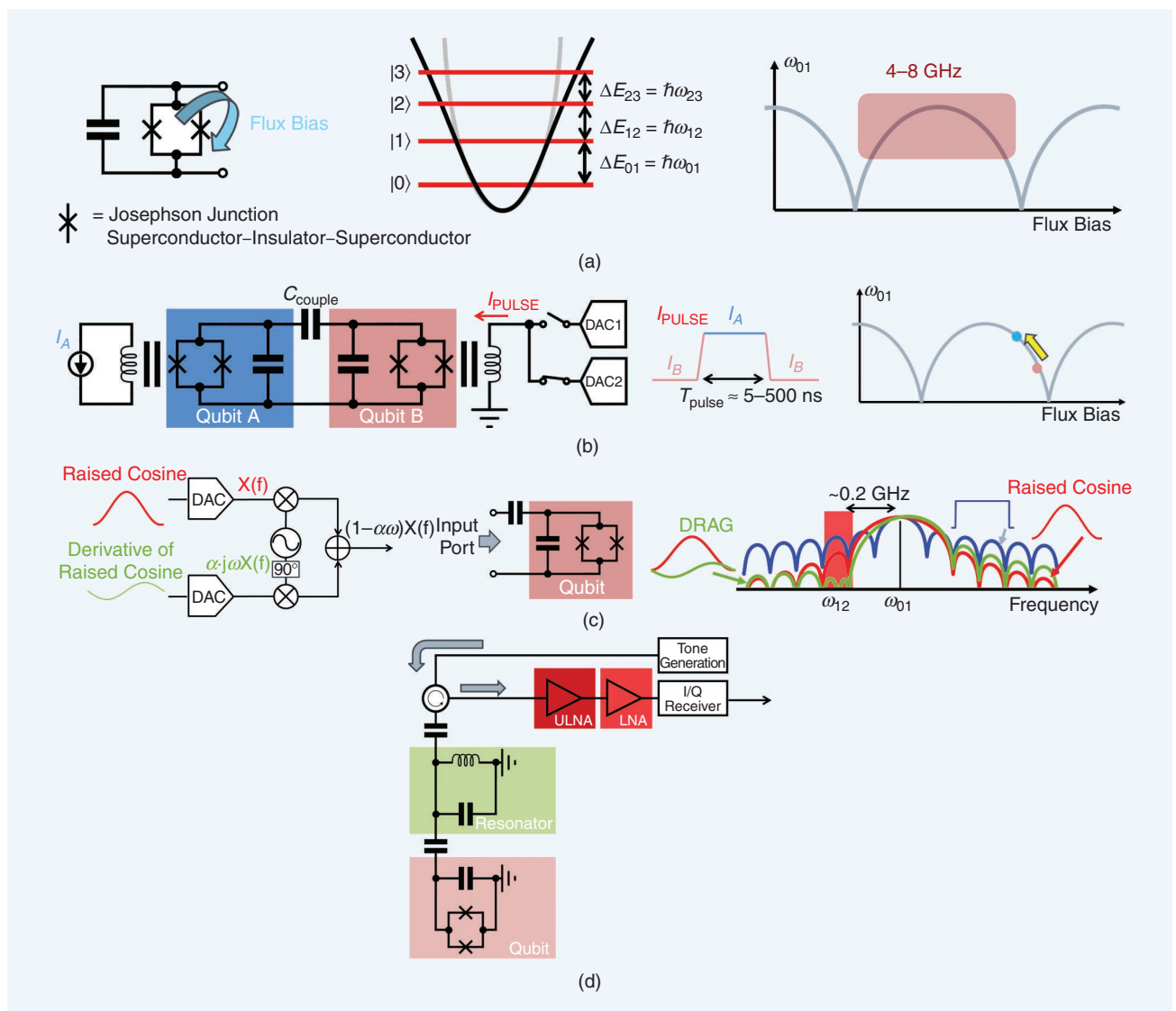


FIGURE 3: Superconducting qubits. (a) The implementation of a superconducting qubit (left); its nonharmonic energy profile (black), which is different from a purely parabolic profile (gray) (center); and the tunability of the Larmor frequency with the flux bias (right). (b) The biasing and pulsing of the flux bias to obtain a two-qubit operation. (c) A single-qubit operation using a Derivative Removal by Adiabatic Gate (DRAG) pulse (left) and comparison of the spectral leakage to noncomputational levels for different waveform envelopes (right). (d) The qubit readout. ULNA: ultra-low-noise amplifier.

Stepping into designing with cryo-CMOS technology is like adopting a new technology node with different device characteristics.

to the same frequency to let them interact, hence implementing a **two-qubit operation**. While a high accuracy in such a current (~ 14 b over a $\sim 500\text{-}\mu\text{A}$ range) is needed to set the qubit frequency, it must also be quickly pulsed on the nanoscale timescale. To meet those contrasting specifications, multiple current steering DACs that are optimized for high resolution and not for speed can be quickly switched [40], [41], as illustrated in Figure 3(b).

For a more generic **single-qubit operation**, the qubit can be excited by a microwave pulse with the right frequency, phase, amplitude, and duration (see Figure 1), which is generated by a microwave modulator [Figure 3(c)]. Although a simple rectangular envelope would suffice, spectral leakage would excite the unwanted higher-energy states in Figure 3(a). More complex pulse envelopes can be used to engineer the spectral shape, e.g., a raised cosine pulse or the commonly adopted Derivative Removal by Adiabatic Gate (DRAG) pulse, which requires an I/Q modulator. As an alternative, instead of using a complex modulator to achieve advanced spectral shaping, a fluxonium superconducting qubit can be employed, which moves the forbidden energy transitions to a frequency far enough away to allow a simple rectangular envelope, hence saving circuit complexity and power dissipation [34]. This is an example of an emerging trend: designing quantum processors to ease the constraint on the electronics, rather than designing the electronics given the qubits. Such an approach is a natural choice when the electronics become a bottleneck for scaling. Several architectures for the microwave modulators have been proposed [40], [42], [43], [44], [45], which borrow known techniques for designing

room-temperature wireless transmitters to achieve power efficiency as low as 4 mW/qubit.

For **qubit readout**, the qubit state modulates the frequency response of a coupled resonator tuned close to the qubit Larmor frequency [Figure 3(d)]. The reflection coefficient (or transmission coefficient in a different configuration) of the resonator is probed by a tone and measured by an I/Q receiver, whose architecture can be inspired by modern wireless receivers [45], [46], [47], similar to the microwave modulator for single-qubit operations. As only very little power (typically < -125 dBm) can be used by the probing tone to avoid ruining the qubit state, the weak readout signal must be amplified by an ultra-low-noise amplifier, typically a superconducting Josephson parametric amplifier (JPA) that achieves the lowest possible noise, the so-called quantum noise limit. Due to the limited JPA gain (< 20 dB), a cascaded LNA is still needed, often implemented as a discrete InP HEMT amplifier, although CMOS or SiGe bipolar LNAs are currently being investigated [48], [49]. An interesting tutorial entirely focusing on superconducting qubits can be found in [50].

In general, superconducting qubits are microwave objects in the 6–8-GHz band that require mainly microwave control with enhanced spectral purity and a low-noise microwave readout, all on 50- Ω matched interfaces, in addition to some limited baseband control, thus making them the perfect application for RF/microwave engineers. Those quantum processors are the most popular target for cryo-CMOS ICs, as they are among the largest quantum processors available today with 1,000+ qubits. However, while the superconducting qubits must oper-

ate at a sub-Kelvin temperature, the specifications for all the cryo-CMOS electronics discussed above lead to a power consumption that is compatible only with cooling power above 4 K. Thus, a wiring bottleneck still exists between 4-K cryo-CMOS electronics and milli-Kelvin qubits that may limit the quantum processor to the size of a few thousand wires and, hence, a few thousands qubits. Furthermore, superconducting qubits occupy a die area larger than $100 \times 100\text{ }\mu\text{m}^2$, making it challenging to monolithically integrate millions of qubits. Future scaling may, then, ask for multicore architectures, eventually spanning over multiple cryostats, as, for instance, road mapped by IBM.

Semiconductor Qubits

As an alternative to superconducting qubits, semiconductor spin qubits offer a very tight pitch (~ 100 nm) when organized in arrays and operation at relatively hot temperatures up to 4 K. Compatibility with advanced semiconductor manufacturing also strengthens the promise of a large-scale spin qubit quantum processor, although only a 12-qubit processor has been demonstrated [51]. In those processors, single charge carriers (holes or electrons) are isolated into quantum dots electrostatically defined by a set of metal electrodes [Figure 4(a)]. By applying an external magnetic field, their spin-up and spin-down states have different energies and can be used to encode the qubit state.

As one or two electrodes are often used per qubit, a scalable **biasing** involves multiplexing a single DAC over many qubits and locally storing the electrode bias on a capacitive sample-and-hold [Figure 4(b)]. Since those bias voltages are refreshed at a very low rate thanks to a low charge leakage, the DAC power dissipation can be reduced to be compatible even with sub-Kelvin cooling power [52], [53], [54], [55], [56], [57]. Instead, the main challenges in the DAC design lie

in ensuring the required low noise and high resolution, sometimes even exceeding 18 b [58].

Single-qubit operations are performed by applying a microwave (1–20-GHz) magnetic field, either by running a current through a nearby wire or by moving the hole/electron in a magnetic field gradient with an ac excitation on a nearby electrode [Figure 4(c)]. In both cases, the cryo-CMOS microwave driver shares

It is unlikely that a CMOS technology will be expressly optimized for cryogenic operation, due to cost constraints.

similar specifications with the ones used for superconducting qubits—and hence, similar architectures are adopted [42], [59]—with the main differences that 1) the requirements for spectral purity are relaxed; 2) an

“open” at the electrode, similar to the gate impedance of a very small MOS, may be driven, rather than $50\ \Omega$; and 3) more recent spin qubits ask for lower (subgigahertz) driving frequencies.

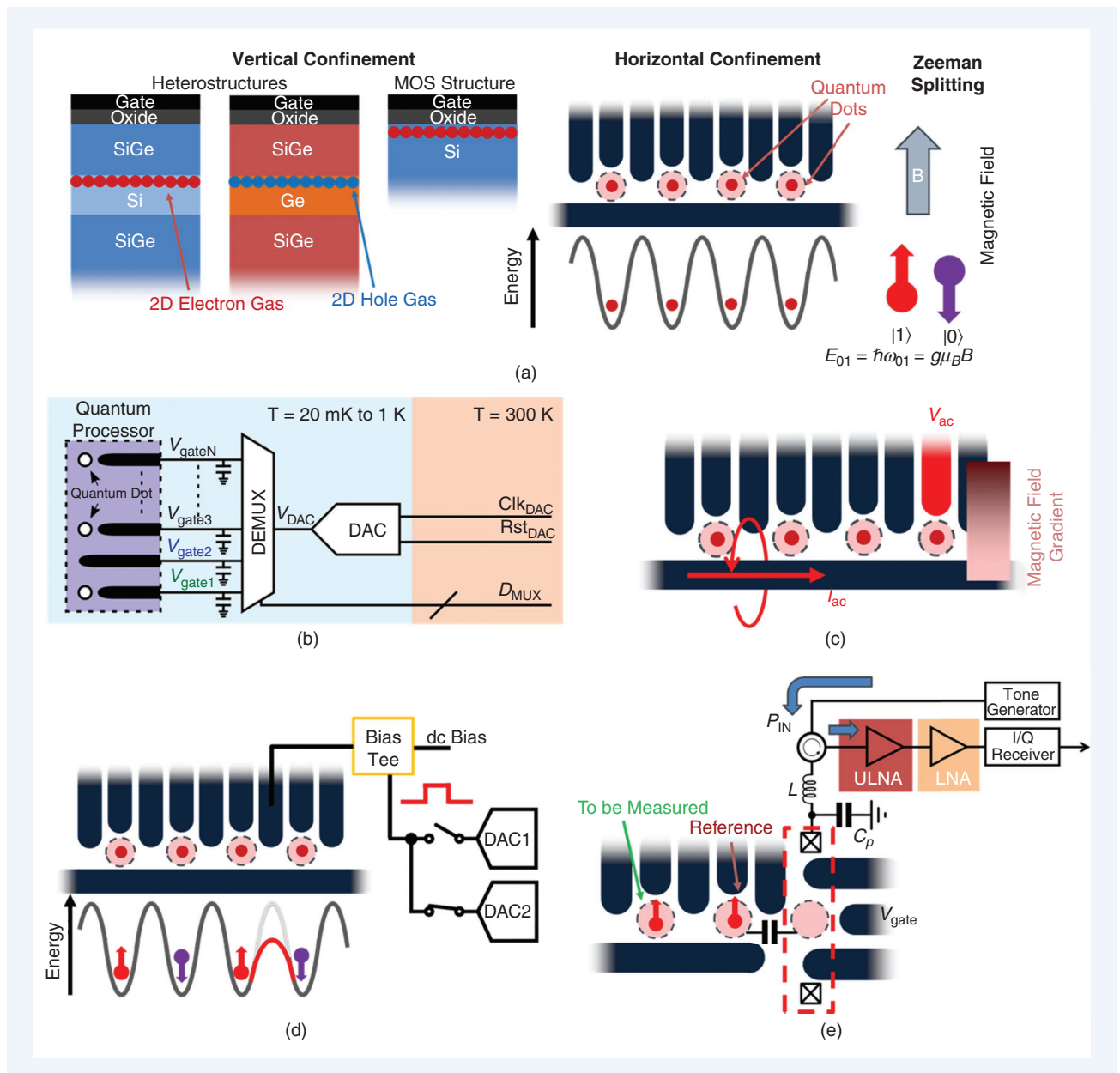


FIGURE 4: Semiconductor qubits. (a) The vertical and horizontal confinement of individual charges and application of an external magnetic field to define the two energy states (spin up and spin down) encoding the qubit state. (b) The biasing of the electrodes. (c) A single-qubit operation either using a current-induced magnetic field or moving the charge in a magnetic gradient. (d) A two-qubit operation by dynamically adapting the barrier potential between two neighboring quantum dots. (e) A qubit measurement via the RF reflectometry readout of a charge sensor.

Looking into the future, we will move from demonstrating individual functionalities to building larger systems.

In **two-qubit operations**, the electrostatic potential defining the quantum dots is temporarily altered to lower the barrier between neighboring dots so that the two qubits can interact [Figure 4(d)]. As pulsing the electrode voltage demands high-resolution amplitudes (>11 b) and fast switching (~ 1 ns), two slow high-accuracy DACs can be quickly switched, similar to pulsing the flux bias in superconducting qubits [59]. Depending on the specific qubit, slower smooth pulses, i.e., adiabatic pulses, may be needed, which would require moderate resolution but high sample rates up to hundreds of megasamples per second.

Since reading out the spin of a single hole/electron is impractical, the spin information is converted into charge displacement by pushing the charge carrier to move to a neighboring quantum dot already hosting a reference charge with a predefined spin [Figure 4(e)]. As two charges with the same spin cannot be hosted on the same quantum dot, we will get either the two charges on the same dot or each charge on a separate dot, depending on the spin state of the charge to be sensed. The charge configuration can then be monitored by a charge sensor, e.g., a single-

electron transistor, whose resistance depends on the qubit state. Such resistance can be remotely monitored by measuring the reflection coefficient at a $50\text{-}\Omega$ line connected to the sensor. However, due to limited sensor sensitivity ($\Delta R/R \sim 1\%$) and because a large probing power can alter the qubit state, the reflected power is extremely weak (<-130 dBm), thus requiring an ultralow-noise readout, which shares challenges similar to those of the superconducting-qubit readout [60]. Although this readout technique can achieve short measurement times and facilitate frequency multiplexing by using multiple matching networks tuned to distinct frequencies, the presence of a charge sensor breaks the uniformity of the qubit array, thus questioning its scalability. In an alternative readout scheme, the charge sensor may be left out by connecting the matching network to the metal electrode closer to the qubit and sensing its state-dependent capacitance [61]. Still, a large inductor remains, whose footprint may be larger than thousands of qubits, again hindering scalability. A promising solution is, then, to skip the matching network and directly read the output current

of the charge sensor [62], [63], [64], [65], [66], [67]. As any parasitic capacitance would limit the speed and/or noise performance of such a readout, this solution is mainly appealing when the cryo-CMOS electronics are close to the qubits, thus strictly constraining the power dissipation due to cooling and thermal crosstalk limitations.

All the cryo-CMOS electronics just mentioned could in principle be cointegrated on the same chip with the spin qubits. However, the progress toward large arrays of spin qubits has been slowed down by the limited qubit uniformity that would require individual qubit addressing. In turn, it is challenging to efficiently fan out individual electrodes to the electronics when the electrode pitch is on the order of 100 nm. Still, viable paths forward are being explored, including adopting spin qubits that do not require any microwave control or readout but only baseband electronics [67], [68]. Avoiding bulky microwave components, such as inductors, and getting rid of high-power high-frequency circuits, and the potential qubit/electronics cointegration, boosts the prospects of this qubit platform.

Other Technologies

The very tight pitch of semiconductor spin qubits makes it difficult to connect to their control electronics efficiently. In contrast, spin qubits in color centers, e.g., fabricated on diamond substrates, can easily operate at high operating temperature (>1 K) while arranged in arrays with a millimeter-size pitch (Figure 5), thanks to their remote entanglement via an optical link, thus giving plenty of space to cointegrate cryogenic electronics. However, optical control requires complex cointegration of cryo-CMOS electronics, integrated photonics, and qubit substrates, which leads to suboptimal coupling between the qubits and the coils driving the qubit operations [68], [70]. Thus, the cryo-CMOS drivers must face the challenge to

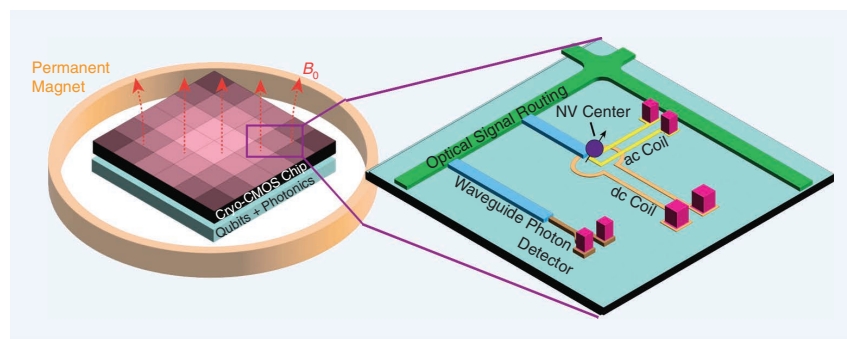


FIGURE 5: The architecture of a 3D-integrated quantum processor based on nitrogen vacancy (NV) color centers, including multiple unit cells at a millimeter-size pitch. The zoom in shows the different non-CMOS components, which also require control by the cryo-CMOS electronics.

generate significant currents (>10 mA) with minimum power dissipation [61], unlike cryo-CMOS for the other qubits mentioned earlier that deal only with extremely low signals. A similar hurdle appears in ion-trap quantum computers, which ask for driving voltages exceeding 10 V [71], in addition to microwave drivers similar to other qubit platforms [70]. Those applications, in addition to the need for high-performance low-power circuits, also add unexplored concerns about the reliability of the cryo-CMOS technology.

Other Cryo-CMOS Circuits

Next to the signal processing blocks, we should not forget the “support” electronics, such as voltage/current references and frequency generators, necessary for the correct operation of the RF transceivers, the data converters, and the other circuits described earlier. Luckily, the solid-state circuit community is extensively addressing the challenges associated with the cryogenic operation of those circuits.

In addition, as we are building a computer, digital functionalities are essential, for instance, for the flow control of the quantum algorithm but also for the DSP in the readout/driving circuits. Furthermore, we have not yet discussed how to address the remaining DiVincenzo criterion: how can cryo-CMOS support long coherence times by enabling QEC? Also, for this, fast and efficient digital circuits are crucial for the real-time processing of the terabits per second of data used to decode the QEC codes and detect/correct any errors [9].

Cryo-CMOS digital circuits can be built using standard room temperature design techniques. In general, digital circuits are faster at lower temperatures, thanks to the higher mobility. However, since they cannot be simulated due to the lack of compact models, extra margins are often introduced to avoid timing violations. Although most digital cells have shown proper functionality, the tradeoffs are different due to

There is ample space (and need!) for the solid-state-circuit community to pursue innovation, research, and industrialization of cryo-CMOS interfaces for quantum computing.

different device performance; e.g., the static power is negligible due to the reduced leakage. For memories, for instance, the reduced leakage allows for lower refresh rates in DRAMs and, hence, lower power, while SRAMs have negligible leakage power that makes the dynamic power dominant even at very low access rates [73].

Future Challenges and Vision

Cryo-CMOS is an enabling technology that addresses the wiring bottleneck in large-scale quantum computers. Cryo-CMOS circuits are tasked to operate the qubits while maintaining high fidelity. This does not necessarily ask for new circuit topologies and architectures but more for careful power and footprint¹ minimization to fit the electronic interface next to the quantum processor. The biggest gain in such an optimization lies in thoroughly understanding the qubits and their requirements, but unfortunately, the qubit specifications are a moving target due to their continuous development. On the bright side, since quantum engineers have started worrying about the limitations in the design of the electronics, they are adapting the qubits to make their control easier for cryo-CMOS, e.g., with superconducting qubits with simpler requirements for the spectral purity or semiconductor qubits without microwave control.

Stepping into designing with cryo-CMOS technology is like adopting a new technology node with different device characteristics, and circuit design can be approached with the same spirit. It is unlikely

that a CMOS technology will be expressly optimized for cryogenic operation, due to cost constraints, while it is possible that a mix of semiconductor technologies (bulk CMOS, FDSOI, and SiGe BiCMOS) will be adopted. For those technologies, the main aid will possibly come from the availability of reliable cryogenic device models.

Looking into the future, we will move from demonstrating individual functionalities to building larger systems. For superconducting qubits, we will still see a two-chip solution: a milli-Kelvin quantum processing unit (eventually including superconducting amplifiers) and a 4-K cryo-CMOS interface. For semiconductor qubits and other platforms, such as color centers, monolithic or 3D integration will take hold. Research topics associated with SoC development, such as power and thermal management, will pick up momentum together with growing attention to qubit/electronics codesign, co-simulation, and cointegration as well as new aspects in device modeling, such as reliability. While significant progress has been made in the past decade toward such a vision, there is ample space (and need!) for the solid-state-circuit community to pursue innovation, research, and industrialization of cryo-CMOS interfaces for quantum computing.

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¹See, e.g., the push for area minimization in [74] and [75].

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