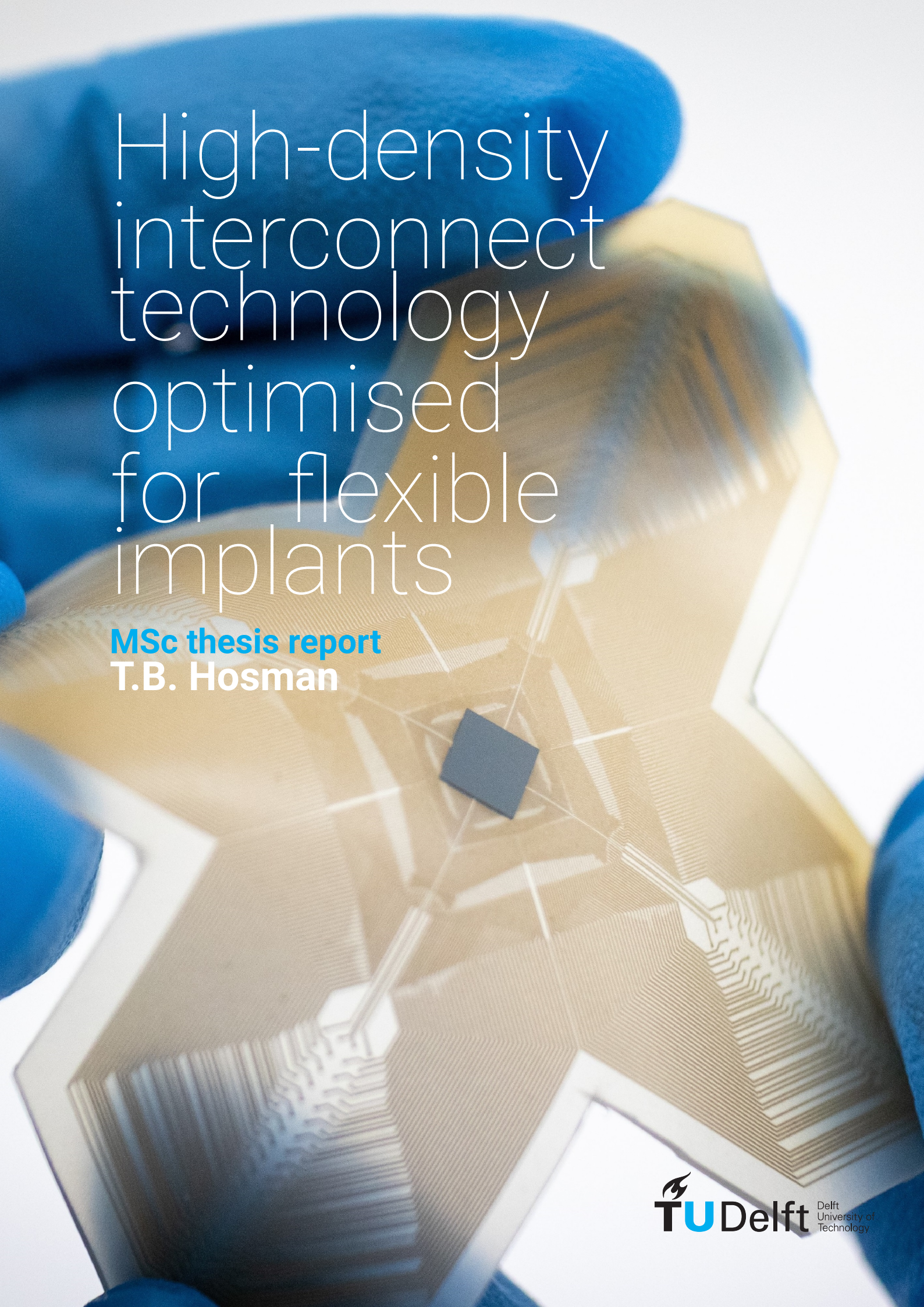

High-density interconnect technology optimised for flexible implants

MSc thesis report

T.B. Hosman

TU Delft Delft University of Technology

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by

T.B. Hosman

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An electronic version of this thesis is available at `https://repository.tudelft.nl/`.

TU Delft

Abstract

Electronic implants are becoming a valuable tool to explore as well as regulate neural activity, potentially overcoming neural disabilities that are not yet curable. On the one hand, neural recording can provide tremendous insight in the behaviour of the neural system and the sometimes accompanied neural diseases. On the other hand, neural stimulation is necessary to control or adjust neural activity related to neural diseases. Detail of neural recording and stimulation is achieved with highly dense and often deep implantable electrodes (spatial resolution), while neural patterns are found with larger neural area coverage. In both stimulating and recording, a combination of spatial resolution and area coverage can be key to understanding and curing.

Application-specific integrated circuits (ASICs) are often employed to accommodate the interaction with the electrodes interfacing with neural tissue but ASICs are limited in size, which consequently limits the amount of individual recording or stimulation channels. The de facto solution to circumvent this limitation is to multiplex high numbers of electrodes to a single ASIC channel. However, due to switching and signal latencies only a limited number of electrodes can be multiplexed per channel. Multiple channels on an ASIC are therefore desirable nonetheless to accommodate implants with a high electrode count.

Due to recent miniaturization advances, an ever-increasing number of channels can be made available on a single ASIC and the urgency arises to investigate technological complications of connecting these channels to electrodes and integrating them on a flexible and implantable substrate. In this work we will investigate the technological complications of assembling a fully flexible electrode array substrate to an ASIC with a high number of independent channels. For such assemblies, a routing optimiser methodology was developed especially for flexible implants, optimising for chip size and critical technology parameters such as the number of metallization layers. However, with no established manufacturing methodology for such systems, technology parameters were not fully understood. Therefore, initial efforts were put into fabrication of a custom chip with which 72 chip-to-substrate gold stud contacts can be evaluated by means of 4-point measurements and daisy-chaining. This multifunctional chip allows for experiments at various chip-to-substrate contact diameters and pitches. In addition, different materials, including polycarbonate (PC), polyimide (PI) and thermoplastic polyurethane (TPU) were investigated as candidate substrate materials. A tranfer methodology, using copper and FR-4 as a carrier materials, proved fruitful for these polymeric materials. TPU samples in particular showed most promising results, with contact resistances in the range of 4.5 to $14 m\Omega$. The main advantage of this material is that it can encapsulate the entire implantable system, including chip and metallization, without the formation of any additional material interface between the layers of the process. This has significant advantages for the longevity of an implantable system.

The results were applied for a second design for which the developed optimiser was used. The chip consists of 1008 gold electroplated contacts that can be evaluated with a similar measurement network. The chip measures at $4 \times 4 mm^2$ and contacts were designed to be $36 \times 36 \mu m^2$ in size, pitched at $80 \mu m$ apart. Contact resistances of this chip on TPU substrates were in the range of 5.5 and $73 m\Omega$ but the yield of proper contact dropped from 100% to an estimated 90% compared to experiments with the previous chip. A demonstrator product was made using the same chip that connects 324 peripheral electrodes to the chip on a single Au metallization layer and is fully embedded in TPU.

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My parents, for your unconditional support and love. Thank you for aiding me in the opportunity to study abroad. Thank you friends and family, for staying close even when you are far. Thank you, Renske, for joyously staying by my side and giving space to unwind.

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Contents

List of abbreviations

ACA	Anisotropic conductive adhesive
ACF	Anisotropic conductive film
ADC	Analog-digital converter
AIBM	Active implantable biomedical microsystem
Al	Aluminium
AP	Action potential
ASIC	Application-specific integrated circuit
Au	Gold
AuPd	Gold-palladium
BMI	Brain-machine interface
CNS	Central nervous system
CT	Computed tomography
Cu	Copper
DBS	Deep-brain stimulation
DI	Deionized
ECoG	Electrocorticography
EEG	Electroencephalography
ENIG	Electroless Nickel Immersion Gold
EP	Electroplating
FC	Flip-chip
ICA	Isotropic conductive adhesive
IPA	Isopropyl alcohol
LDI	Laser Direct Imaging
LFP	Local field potential
MEA	Multi electrode array
NCA	Non-conductive adhesive
NCF	Non-conductive film
Ni	Nickel
OL	Open-loop
P	Phosphorus

PC	Polycarbonate
PDMS	Polydimethylsiloxane
PI	Polyimide
PR	Photoresist
PU	Polyurethane
SCI	Spinal cord injury
Si	Silicon
TAB	Tape-automated bonding
TC	Thermocompression
Ti	Titanium
TPU	Thermoplastic polyurethane
TS	Thermosonic
UBM	Under-bump metallization
US	Ultrasound

1 Introduction

Active implantable biomedical microsystems (AIBMs) have proven to be a valuable tool in exploring as well as regulating neural activity, playing an important role in deciphering and curing a wide range of neural disorders such as spinal cord injuries (SCI), epilepsy, Alzheimer's and Parkinson's [1], auto-immune disorders such as Crohn's disease and rheumatoid arthritis [2] [3], and sensory disorders such as vision and hearing impairments. Similar minimally-invasive technology is finding its way into externally wearable health-monitors that could track a wide range of biomarkers found in saliva, sweat, tears and interstitial fluids [4].

One of many general trends in these applications has been to increase the area coverage and spatial density of sensing and stimulation systems. Coverage allows for high-level neural mapping, while density allows for more detailed knowledge and control over a neural site [5]. Existing high-resolution applications for the brain, commonly named brain-machine interfaces (BMIs), aim to closely interweave the electronic system with signals of the central and peripheral nervous system, allowing for neuroprosthetic control such as robotic limbs [6] and speech synthesizers [7]. According to a bioelectronics research roadmap by Birmingham et Al. "The research should be iterative, drilling deeper into the signals as higher-resolution interfacing technology emerges until the functional units of nerve fibres and their signalling patterns are established" [8]. These kind of high-density neural interfaces have tremendous potential to cure a wide range of (neural) diseases that to-date remain (largely) unsolvable, and could give us better insight in the working principles of the brain. For such AIBMs, improvements should ideally include many, if not all, of the following features:

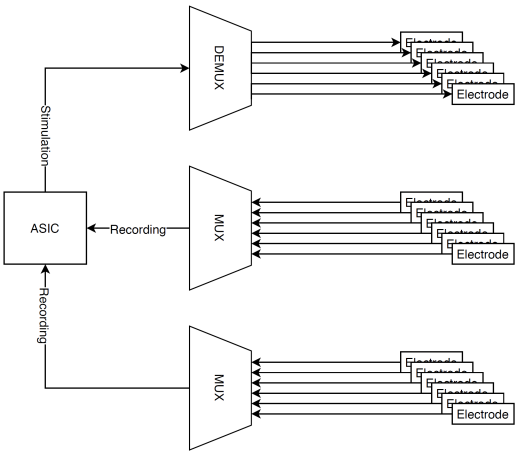
- Flexible
- Biocompatible
- Biostable
- Fully implantable
- Large number of sites for neural interaction (area coverage and/or density)
- Limited number of sites per channel

The meanings of these features will be described in the following 2 sections.

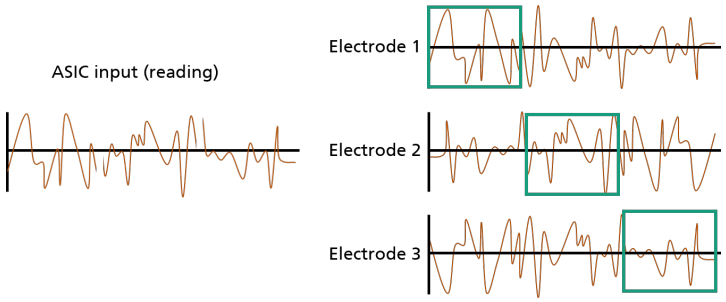
1.1. Recording and stimulation resolution

Depending on the application of an AIBM, two types of coverage are of importance: spatial resolution and area coverage. Both can give an indication of the versatility and effectivity of the device. Spatial resolution indicates the density at which the device is able to stimulate. A higher spatial resolution means that electrodes are smaller and are more tightly placed together, thus allowing for more detailed and local neural recording or stimulation. This comes at the cost of a higher electrode impedance, increasing power consumption as well as noise. Note that neurons are in the order of 5 to 140μm, with the large majority being in the sub-20μm range [9] so electrodes should be in the microns range if recording or stimulation of individual neurons is

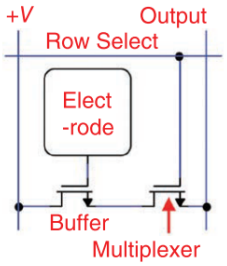
desired. When a bigger stimulation or recording area is required, a bigger area coverage might be in order. Electrodes in such an array will be more spread out and most likely bigger to individually cover a multitude of neurons. Depending on the area that needs to be covered and the spatial resolution, one can estimate how many electrodes need to be managed in order to properly record or stimulate the neural site of interest.



(a) Simplified connection scheme between an ASIC and electrodes. Two intermediate multiplexers reduce the required number of ASIC recording channels to two, while one intermediate demultiplexer allows for multiple stimulation electrodes to be controlled by a single stimulation channel.



(b) An example of electrode readout. The left graph shows a reading output from the multiplexer to the ASIC over time. The graphs to the right show electrode signals over time where the green boxes outline the signals that are being fed to the ASIC. Signals outside of the green boxes are discarded information.



(c) Implementation of multiplexing on a single electrode [10].

Figure 1.1: A simplified example of multiplexing electrodes to an ASIC.

To allow all electrodes in an array to be actively recorded and/or stimulated, an Application Specific Integrated Circuit (ASIC) is usually integrated on the AIBM. Connections are made between the ASIC and the electrode array during assembly. However, bioelectronic research is moving towards higher connectivity to neural tissue [5], meaning more electrodes on a single array. To date, when the number of available connections on an ASIC exceeds the number of electrodes, multiplexing is used to allow multiple electrodes to be connected to a single ASIC channel. An example of such an implementation can be found in figure 1.1. This is possible to some degree, but limited by:

- Switching latencies
- Recording/stimulation time
- Recording/stimulation frequency

The exact values of these limitations depend heavily on the technology and application of the AIBM, but as an order of magnitude the electrode-to-channel ratio is generally between 1:1 to 10:1 in recent flexible implant developments [10][11]. The practical reasons that a higher ratio is not desired are:

- Loss of synchronicity between electrodes

- Loss of data when electrodes are idle
- No continuity in electrode control

1.2. Implantability

Many of the earlier listed features relate to the level of implantability of an AIBM. These are important system properties because they define how well the technology can be applied as a chronic solution for patients. For example, flexibility and elasticity are properties that are - ideally - close to that of the surrounding tissue. If a mismatch exists in these properties between the tissue and implant, it will cause mechanical stress both on the implant and the tissue. This can lead to premature failure in case of the implant, while for the tissue there can be minor to severe tissue damage as well as scar formation.

Biocompatibility and biostability relate to a similar interaction between the implant and the surrounding tissue. Biocompatibility is defined by Dorland's Medical Dictionary as "the quality of not having toxic or injurious effects on biological systems". 'Toxic effects' relate to the chemical interaction of the implant, often referred to as surface biocomptability, while 'injurous effect' relate to mechanical interaction of the implant, often referred to as structural biocompatibility. Structural biocompatibility is tighly related to the flexibility and elasticity of an implant. Depending on the material, non-biocompatible devices could cause scarring, inflammation, infections or even cell death. Biostability tells us something about how well the implant can cope with the environment of the body, including moisture, biochemicals (enzymes, etc.), heat and movement. Both biocompatibility and biostability are vital for a reliable long-term AIBM.

Full implantability tells us if the functionality of the device is implanted in the body. In this case we will consider all devices with no physical connection to the body exterior as "fully implantable". Cochlear implants, for example, have a sound processor on the external ear and an implanted electrode array in the cochlea as well as a subdural receiving coil. We will consider this device "fully implantable" since there are no connections between the implanted and exterior part. Full implantability is a vital aspect of chronic implants because it allows the patient for more freedom of movement and significantly decreases chances of complications and infections since the device does not form any potentially infectious openings to the outside world.

1.3. Limitations of existing work

Numerous research projects are looking into effectively increasing the number of sites and since this is primarily needed in neural interaction, focus is mainly on increasing the number or reducing the size of electrodes. Among applications one can find multi-electrode array (MEA) well systems, silicon probes and electrode arrays. However, no research as of yet has been able to manufacture a fully implantable flexible active electrode array with a large number of electrodes. The challenges for such a device are numerous, including:

- Substrate assembly for long term reliability
- Acquisition of sufficient operating power
- Substrate manufacturing for high-density electrode routing
- Multilayer flexible substrate manufacturing for high-density routing
- Decreasing or integrating the number of off-chip components (e.g. multiplexers and capacitors)
- ASIC bonding, integration and protection
- Thin electronics, flexibility, assembly and handling
- ASIC size and the number of stimulation/recording channels

1.4. Project goal

The aim for this project is to prove that there is an assembly method possible that allows for connecting a high number of electrodes to a single ASIC on a flexible substrate, with the intention of working towards a long-term fully implantable neurostimulator with high-density simultaneous stimulation. The resulting prototype

should be a novel product that can solve some of the challenges listed above that have not been solved by preceding research outcomes. The following requirements are set as the goal of this thesis project:

- Develop an assembly technique that:
  - Can handle up to 10.000 connections
  - Is highly dense ($< 40 \times 40 \mu m^2$ per connection)
  - Is suitable for flexible substrates
- A substrate manufacturing method that enables:
  - Routing for high-density connectivity
  - Compatibility with the assembly technique
  - Flexible substrates
  - Biocompatibility

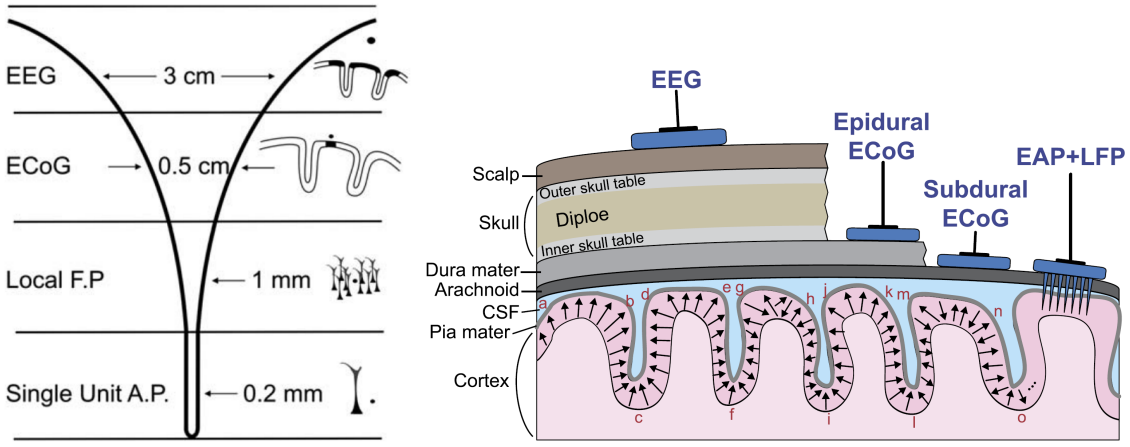
2

State-of-the-art

This chapter will explain the details of relevant state-of-the-art work. It will describe an application-level overview in section 2.1 and gives specific neural interfacing examples in section 2.2. Assembly-specific literature will be discussed in detail in section 2.3 through 2.5. Finally, section 2.6 will elaborate on polymer substrate materials available for biomedical applications.

2.1. High-density neural interfacing

Prototypes for neural interfacing have found their way into implantation sites all over the body. With the exception of retinal implants, high-density neural interfaces are exclusively found around the Central Nervous System (CNS) because this neural tissue has the highest signal density throughout the body. These BMIs are available in a wide variety of applications but can be categorized on their spatial resolution (see figure 2.1a).



(a) Spatial resolution of different BMI techniques [12] (b) Schematic of different types of neural interfaces [13]

Figure 2.1: Schematical overview of common neural interfaces

Electroencephalography (EEG) is a electrophysiological monitoring method used for global brain activity recording. EEG is a non-invasive technology (see figure 2.1b) and is therefore commonly used clinically to diagnose neural disorders such as epilepsy and sleep disorders. Its electrodes are placed on the scalp, therefore spacing them about $2-3cm$ from the cortical surface. Inherent to this spacing, a single action potential (AP) records at only $25pV$ in amplitude at the scalp surface. EEG can therefore only measure a "large neuronal population of synchronously active neurons", requiring nearly $6cm^2$ of synchronized cortical tissue to generate a potential of a few mV on the scalp surface [12]. Other limitations in EEG monitoring include limited bandwidth ($< 100Hz$ due to scalp filtering), electrode contact variations, patient tethering, significant noise

and environmental artifacts [14].

Electrocorticography (ECoG) is similar to EEG but consists of electrodes placed directly on the cortex (see figure 2.1b). They are placed either outside or inside the dura matter (epidural or subdural, respectively) by means of a craniotomy procedure done by a surgeon. The closer positioning to the cortex allows for a spatial resolution in the order of millimeters [15] with conventional ECoG devices measuring up to $200Hz$ [12]. However, in recent work by Khodagholy et al., Neurogrid has succeeded in LFP and AP readings using non-penetrating ECoG [16], indicating that higher spatial resolutions can be accomplished with subdural ECoG systems. In addition, more recent work on BMI systems suggests that subdural reading can benefit from higher sampling frequencies (up to $20kHz$) if the electrodes are positioned on slightly penetrating nanowires [17]. ECoG devices are indeed promising due to their "lower noise signal and higher bandwidth and power, because filtering by the scalp is reduced" compared to EEG [14]. Furthermore, ECoG devices are relatively low-risk compared to (deep) probes and penetrating arrays (see figure 2.1b) and have shown promising results e.g. in 2D and 3D limb movement [18] [19], though as of yet only short-term ECoG interfaces are currently FDA-approved.

Local Field Potential (LFP) recordings are electrophysiological recordings of a sum of neural cells concentrated around a penetrating electrode. The recording radius is generally in the order of a few hundred microns. LPFs are extracted by low-pass filtering the signal (<300Hz), this conveniently makes the recordings less sensitive to geometry and the tissue-electrode interface [12]. Offering more spatial resolution tat ECoG, LFP recordings show promising results in the field of BMIs, though to date it still suffers from reliability and safety issues due to its rigidity [12].

Table 2.1: Design requirements for different readout/stimulation functionality [20]

Function	Application	Spatial Resolution	Signal level	Signal Frequency	Noise & Linearity	Number of channels
AP Readout	Electrical: AP recording	Sub-cellular	Neuronal AP: <$1mV$	Neuronal AP: $300Hz$–$6kHz$	<$5\mu V_{RMS}$	Thousands
LFP Readout	Electrical: LFP recording	Few hundred μm	Neuronal LFP: <$5mV$ Cardiac/ Pancreatic: tens of mV	Neuronal: $\sim 1-300Hz$ Cardiac: $\sim 1-1000Hz$	<$10\mu V_{RMS}$	Few tens
Neurotransmitter Detection	Electrochem: Neurotransmitter detection	Sub-cellular/ cellular	$nA-\mu A$	$\sim 10kHz$ for FSCV	<$0.5nA_{RMS}$	Few tens
Impedance Measurement	Electrical/ Electrochem: Cell-electrode interface characterization	Sub-cellular	$10k\Omega-10G\Omega$	$1Hz-1MHz$	<$1.0pA_{RMS}$	Few tens
Stimulation	Electrical: Apply voltage/ current pulse	Sub-cellular	Voltage:$\pm 1.3V$ Current: $\pm 30\mu A$ in low range, $\pm 300\mu A$ in high range	$10kHz$–$100kHz$ for single electrode	>9 bit linearity	Few tens
Current Readout	Electrical: current recording	Sub-cellular	pA	-	<$100fA_{RMS}$	Few tens

Single Unit Action Potential (AP) recordings are recordings very similar to LFP recordings, utilizing similar penetrating probing devices. They differ mainly in the filtering process. High-frequency neural activity does not carry as far as lower-frequency signals (LFPs) due to capacitive filtering, therefore AP recordings are band-pass filtered in the order of 300Hz-6kHz [20], filtering most lower-frequency signals of surrounding neurons. AP recordings suffer from similar risks and reliability issues as LFP recordings, with only half of the

implanted nanowires being functional recording sites in studies by Schwartz et al [12].

Work by Dragas et al. tries to set some design requirements depending on the desired interaction with the neural tissue. An overview of these requirements can be found in table 2.1.

2.2. Existing high-density electrode array systems

To date, there is already a wide variety of high-density electrode arrays found on the market and academia. Depending on the application, they can have wildly different electrode sizes, be rigid or (partially) flexible, fully implantable or only partly implantable, etc. In this section, current common applications and their respectable features will be discussed. State-of-the-art prototypes are taken as a comparing reference.

One of the most common applications for high-density electrode arrays is in research fields where *in vitro* experiments are executed. In these experiments, cell cultures are grown in petri dishes to test - for example - the effectiveness of medicine, the toxicity of materials or a cell's responsiveness to electronic stimulation. These are valuable experiments for the development of drugs and implants, allowing them to move ahead from lab prototype to first *in vivo* trials. Even more so due to recent developments in the field of *organ-on-chip*, where the aim is to take the growing of cell cultures to the next level by forming them into micro versions of an entire organ, including lungs, livers and kidneys [21]. Recent work has even succeeded in interconnecting and maintaining multiple micro-organs over a 28-day period [22]. This promising new field reports significant advances in more personalized medicine with fewer side-effects because they can be created for *in vitro* testing on a per-patient basis. Furthermore, the development allows for a lower demand in rodent experiments.
High-density electrode arrays are in high demand in the field of *in vitro* experiments because they allow for accurate monitoring of cell culture activity down to the single-cell level. Current state-of-the-art high-density Multi-Electrode Array (HD-MEA) wells in this field include the switch matrix system by Dragas et al., which has 59760 transducers pitched at $13.5\mu m$. The system has 2048 readout channels for APs and 32 more for LFPs, converting at a $20kS/s$ 10 bit ADC resolution [20]. Other modes for the device include impedance measurements, neurotransmitter detection and V- or I/V-controlled stimulation. The device is fully rigid and obviously not designed for implantation in the body. Biocompatibility and stability is not specifically mentioned by the authors.

A more implantable high-density electrode array is commonly dubbed Deep-Brain Stimulation (DBS) probe. These are silicon-based shank structures are able to penetrate deep into the brain tissue. High-density DBS assemblies find their application in *in vivo* studies on rodents where high-density high-performance neural readout is desired without any tethering to an external measurement system. Current state-of-the-art high-density DBS systems are able to facilitate up to 1356 electrodes and sample at a similar rate in the order of $20kS/s$ with 10 bits of ADC resolution [23]. Other DBS systems focus on making a very narrow and thin shank to reduce the impact on surrounding neural tissue, fitting up to 966 electrodes on a $10mm$ long shank with a diameter of $70\times20\mu m^2$ [24]. Downside of these high-density DBS systems is that they are not suited for long-term implantability due to their rigidity, causing electrode migration, tissue damage and scarring [25]. These problems have been partially mitigated in commercially available DBS stimulators for e.g. Alzheimer's and Tourette's [26], albeit at the cost of spatial resolution and area coverage of the electrodes.

One of the few successful forms of a fully implantable electrode array is the one used in cochlear implants. These implants are designed for a specific group of the hearing impaired where a part of the hearing preceding the cochlea are dysfunctional (such as the auditory ossicles or tympanic membrane). A cochlear implant bypasses these parts of the hearing organ by wirelessly transmitting externally recorded sound to a fully implanted neuromodulator that stimulates the cochlea. Cochlear implants have become reasonably reliable over the years because the implantation site is relatively bony, with reliability problems in only $1-2\%$ of successfully implanted systems, although implantation itself is still a high-risk procedure with almost 20% of all patients post-implantation complications. State-of-the-art commercial cochlear implants have not increased the number of electrodes beyond 22 in total because the increased power consumption would require a larger implant for adequate power supply [27].

A similar neuroprosthetic implant - although to-date less successful than the cochlear implant - is the retinal implant. This type of implant aims to restore some degree of vision of the blind, though it is lim-

ited to the blind with outer retinal degradation. On system level, a conventional retinal implant works similar to the cochlear implant: an external camera input is processed externally and wirelessly transfered to a fully implanted system that stimulates the optic nerve. However in state-of-the-art retinal implants such as the Alpha-IMS, a high-density electrode array has been integrated together with a photodiode array, thereby eliminating the need for external camera information. The implant, consisting of 1500 stimulatory electrodes, is still powered and monitored externally with a wireless induction link [11]. With a stimulation frequency between 5-20Hz depending on patient preferences, the implant is able to recover some basic visionary sensing such as light perception, localization, motion and very simple patterns.

The most common of BMI systems is the subdural electrode array. These types of implants generally lie on the cortical surface and are primarily used to interface with brain mapping [13], motor control signals [28] and speech [29]. However, same or similar systems can be positioned on other neural surfaces such as the visual cortex or into the interhemispheric fissure [10]. Compared to penetrating electrodes, subdural electrodes excel in maintaining signal integrity over longer periods of time, with similar results and only minimal irritation and injury complications to surrounding brain tissues [10]. Current state-of-the-art subdural systems include the flexible 360-electrode array of Viventi et al. By locally integrating electrode multiplexing circuits and using $100kS/s$ external ADCs, this research group was able to reduce the amount of electrode connections ninefold while maintaining a sampling rate of $10kS/s$ per electrode. According to the authors, the technology has potential to be scaled to encompass 25600 electrodes with at least $1.2kS/s$ each and could be used in clinical trials on brain dynamics [10]. The neuroelectronics start-up Neuralink, one of many ventures of Elon Musk, has taken a different approach and has ambitions to merge the digital and biological domain. Their most recent prototype is a semi-flexible subdural implant with electrodes integrated on flexible threads that can be inserted in the cortex by means of a robot. The prototype was manufactured with up to 3072 electrodes that are individually connected to a multitude of ASICs. Each of the ASICs is mounted in the rigid part of the implant and each can handle up to 256 electrode inputs. It is currently undergoing initial *in vivo* experiments, however with a power consumption of up to $750mW$ there seems to be no indication of fully implantable capabilities.

Table 2.2: Comparison table on some recent high-density biomedical electrode arrays

	[20]	[10]	[24]	[11]	[23]	[30]	[31]	[17]
Stimulation site	In vitro	Subdural	DBS	Retinal	DBS	Subdural	Cochlear	Subdural
Flexible	No	Yes	No	No	No	Yes	Yes	Yes
Biocompatible	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Biostable	No	No	No	Yes	No	No	Yes	Yes
Fully implantable	No	No	No	Yes	No	No	Yes	No
# electrodes	59760	360	966	1500	1356	31	22	3072
Electrode size [μm^2]	22.5	9.00×10^4	144	N/A	400	3.1×10^4	N/A	336
IC size [mm^2]	N/A	N/A	45.2	9	160.6	N/A	N/A	300
# channels	2048	40	384	1500	678	31	N/A	3072
Array surface [mm^2]	10.9	90	7	9	0.8	200	8.5	~ 600
Sampling rate [kS/s]	20 (r)	100 (r)	30 (r)	<0.02 (s)	20 (r)	N/A	32 (s)	18.6 (r)
Crosstalk [dB]	N/A	-65	-64.4	N/A	-63	N/A	N/A	N/A
ADC resolution	10	N/A	10	N/A	10	N/A	N/A	10
Total power cons. [mW]	86	N/A	47	N/A	61	N/A	~ 8.5	750

Table 2.2 shows an overview of the discussed state-of-the-art systems to date. It has become evident that *high-definition* is a very stretchable term for electrode arrays since the state-of-the-art varies significantly from application to application. However, across the board, most systems still struggle to encompass most, if not all, of the ideal properties of a neural implant. Full implantability is often a problem because it requires the complete decoupling of a system and a provision of both power and information via wireless links. Sticking to wired connections requires less engineering effort while maintaining the essence of the topic of interest, which for state-of-the-art systems is the analysis of neural activity foremost. The practicality and longevity of a fully implantable system (as well as flexibility) is not required in the current state of most research. However, if more of today's neurological, auto-immune and sensory disorders are to be investigated and resolved by means of long-term implantation, it is important that high-density electrode array systems

are taken to the next level.

2.3. Chip bonding technology

Bonding is an assembly method that was developed to merge the advantages of the semiconductor industry with substrate technology. The first offers advantages in terms of manufacturing scalability and allows for high functionality density on a single miniature chip. The second allows for more flexibility in terms of device materials and allows for connections with other components. Many bonding methodologies have been developed over the years, all having their clear advantages and disadvantages. We will consider the following bonding techniques for this project:

- Wire bonding
- Tape-automated bonding
- Flip-chip bonding
- Embedding

2.3.1. Wire bonding

Wire bonding is considered one of the oldest forms of bonding and was first applied during the development of the first transistor in 1947. Over the years, industry has refined and optimised the technique to allow for increased yields, decreased pitch and lower costs [32]. This makes wire bonding a competitive bonding process even today. Generally speaking, two different classes of wire bonding can be applied: wedge bonding and ball bonding. A simplified overview of these forms of bonding can be found in figure 2.2. Both classes are most commonly applied using aluminium or gold wire, but many other metals have been used. The wire varies in thickness depending on the application or can be ribbon-shaped for power applications. Like flip-chip bonding, wire bonding is generally applied with one of three application methods.

Thermocompression (TC) is a method that uses both temperature and pressure, hence the name. The temperature will soften (not melt) the bond metal while the applied pressure deforms the softened wire and attaches it to the substrate below. It is the simplest of three methods requiring only 2 parameters, but is also the least often used mainly due to the required temperatures in the order of $300^{\circ}C$, longer bonding times and susceptibility to surface contaminants [32].

Ultrasonic (US) bonding replaces temperature with ultrasonic movement of the tool. The tip of the bonder will generally vibrate between 60 to 250kHz, with most modern autobonders will operate in the 120 to 140 kHz region [32]. There seems to be no consensus on the exact physical workings behind US bonding, though it is thought that the ultrasonic energy causes local heat that forms microwelds at the bonding interface. US bonding is superior over TC and TS bonding in terms of yield and required bonding temperatures but lacks bonding speed like TC bonding.

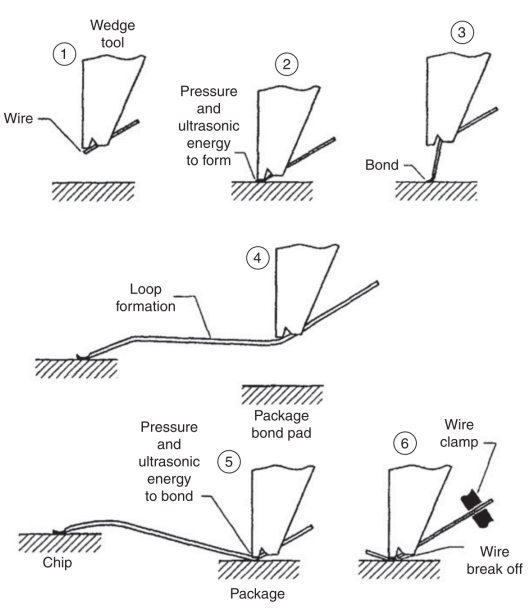
Thermosonic (TS) bonding aims for the best of both worlds by combining temperature, pressure and ultrasound energy during the bonding process. This bonding technique is more complex due to the higher number of parameters but is still the predominant wire bonding technique in industry due to the bonding speed and reliable bonds [32].

2.3.2. Tape-automated bonding

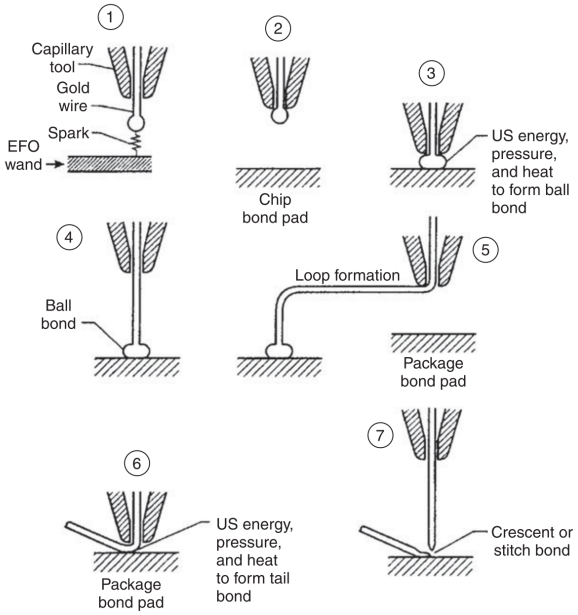
Tape-automated bonding (TAB) was invented in 1960 that utilizes ribbon-like beams held in place by a thin polymer tape [32]. It is a niche technique similar to wire bonding that can offer some advantages for high-frequency applications but is a rather expensive technology. Applications are therefore primarily high-volume productions. Like wire-bonding, TAB is not designed to work with area-array chips.

2.3.3. Flip-chip bonding

Flip-chip (FC) bonding too emerged in the 1960s and has developed as a technology ideal for applications that require high-density area-array bonds. Furthermore, FC bonding technology allows for the highest frequency response, lowest crosstalk and lowest contact resistance due to the very direct and short bonds that are created [32].



(a) Simplified procedure of wedge bonding interconnection [32]



(b) Simplified procedure of ball bonding interconnection [32]

Figure 2.2: Simplified wire bonding process steps.

In FC bonding, a die is flipped with its active face down. After alignment with the substrate, all connections are made simultaneously by applying pressure, temperature and/or ultrasound just like wire bonding. Parameters vary significantly based on the type of bonding and the involved metals, an overview of commonly used flip-chip parameters was made by Klein et al. and can be found in figure 2.3. The different bump types in this figure will be explained in section 2.4. In addition, a wide variety adhesives can be used in flip-chip bonding to improve conductivity, mechanical stability, reliability, etc. Commonly used adhesives include non-conductive adhesives (NCA) and films (NCF), anisotropic conductive adhesives (ACA) and films (ACF) and isotropic conductive adhesive (ICA). The flip-chip bonding process with an adhesive can be found in figure 2.6 but will be explained in more detail in section 2.5.

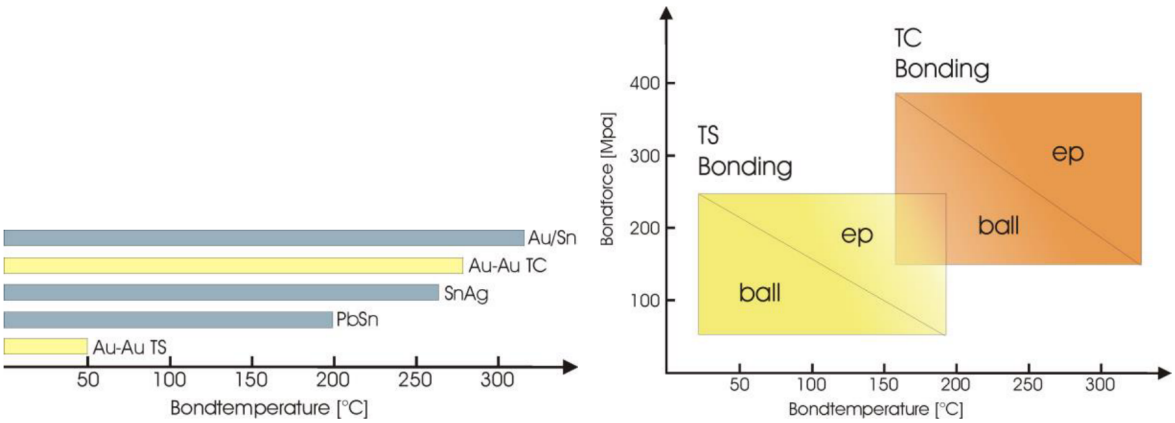


Figure 2.3: Common flip-chip bonding parameters. Left: comparison of maximum temperatures, right: comparing TS and TC bonding (*ball*: stud bumps, *ep*: electroplated bumps) [33]

2.3.4. Embedding

Embedding is a chip bonding technique largely unused in industry because it is still very much experimental. The embedding process allows for a (thinned) silicon chip to be placed during the deposition of substrate

layers, nesting it in the substrate and protecting it from the environment. Figure 2.4 schematically shows a wafer-level embedding technique used at Fraunhofer IZM, where multiple layers of polyimide (PI) are spin coated on a wafer and where metallization is sputtered and patterned in between layers. After chip placement and embedding, the chip contacts are accessed using laser drilling. The technique also allows for multiple metallization layers in a flexible substrate, making it very suitable for wearable and medical applications. Downsides include costs due to lithography processes and required tools, as well as a limited contact size due to the laser resolutions (>60µm).

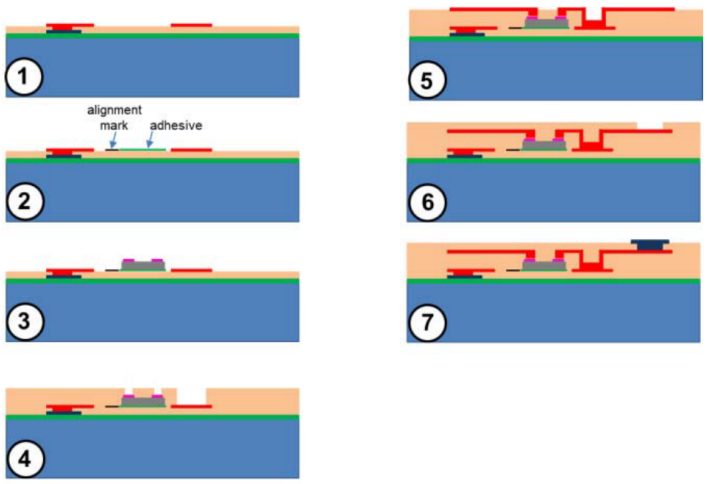


Figure 2.4: Schematic overview of the embedding process [34]

2.4. Flip-chip bumping technology

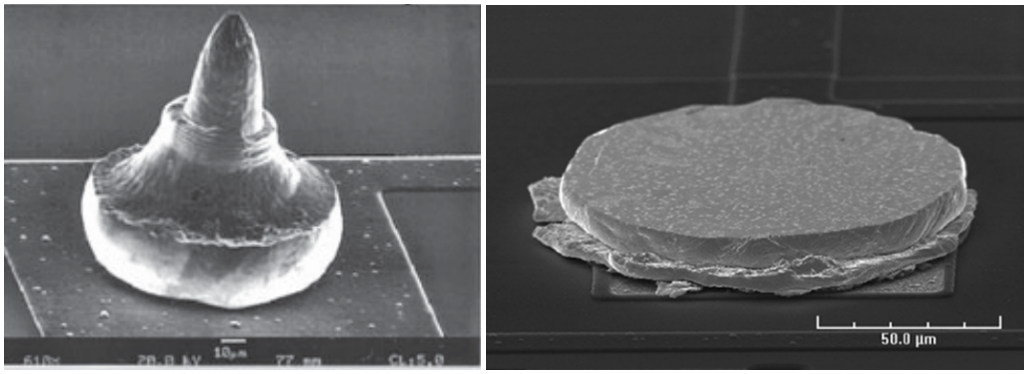
When considering flip-chip bonding as an assembly technique, some aspects regarding the chip bumping should be considered. Chip bumps are the metallization bumps made on the chip that function as an interface between the chip and the substrate. Their function after flip-chip bonding is twofold: 1. provide an electrically conducting connection between the chip pad and the substrate pad and 2. provide - to some degree - a mechanically fastening interface between the chip and substrate. Mechanical stability is enhanced by means of an adhesive, which will be described in further detail in section 2.5. Bumps present on the chip can be of great influence to the overall quality of the electrical and mechanical properties of the bond. For example, the amount of contact surface can greatly alter the contact resistance and mechanical stability of the bond. This is even influenced at the micro-level due to surface roughness [35]. In addition, a bump with too much hardness can damage the bonding surface during flip-chip assembly.

As material, Au is a widely used metal for flip-chip bump formation because of its resistance to corrosion, electrical conductivity and ductility (deformability), though cheaper solutions such as PbSn are available too. Ductility is especially important for bonding directly onto flexible substrates to prevent damage and delamination when pressure is applied in the flip-chip bonding process. Conveniently, Au is well known as a biocompatible material making it a suitable interconnect material for implantable devices. There are three methods for making Au chip bumps: stud bumping, electroplating and electroless nickel immersion gold (ENIG) plating.

2.4.1. Stud bumping

Au stud bumps for flip-chip bonding can be made by using a typical wire bonder. The process is identical to the first 4 steps in figure 2.2, however instead of moving to a second bonding site, the lead is cut off at the root, leaving only a stud with a small tail (see figure 2.5a). Although technically challenging, if 18μm Au wire is used for bump placement, Au stud bumps can be made as small as 36μm in diameter at Fraunhofer IZM.

Processing stud bumps on a chip has its downsides. The placement process is done one-by-one and the cutting of the wire happens with some margin, causing height inconsistencies across the chip. This can cause uneven force distribution that lead to die fractures and open connections. In general, flip-chip bonding re-



(a) An example of a standard stud bump with a tail [32] (b) An example of a stud bump after coining [36]

Figure 2.5: Examples of stud bumping shapes

quires height inconsistencies of less than 5 microns. This can be achieved by post-processing the bump surface to a shape optimal for specific bonding procedures or even certain adhesives [37]. For flip-chip bonding on flexible substrates, a stud bumps can be compressed into coined gold bumps (see figure 2.5b). According to Majeed et al., Deforming the stud bumps into this shape results in excellent failure-resistance for Au-Cu flip-chip bonding on a flexible substrate [36]. This is supported by research of Wu et al., whom state that lower mechanical stresses are to be expected at the bonding interface when bump height is decreased [38].

2.4.2. Electroplating

Electroplated bumps are produced wafer-level and can thus only be processed if the wafer are not yet diced. The first step of electroplating is the patterning of under-bump metallization (UBM) at the contact openings, which is a Ti-W(N) layer that prevents degradation of the chip's Al contact openings due to diffusion. In addition to this step, a temporary electroplating structure (plating base) connects to the UBM contacts so the cathode can be connected during electroplating. The wafer is then plated with Au in a cyanidic gold bath and finally, the plating base is stripped [35].

Compared to stud bumps, electroplating is the technology of choice if high yield and fine contact pitches are desired. Au electroplating limits were already in the order of $10\mu m$ over a decade ago [39], significantly finer compared to stud bump limitations of today. On the other hand, figure 2.3 clearly shows that compared to stud bumps, electroplating requires higher temperatures and/or forces. This is alerting for flexible substrates for which these parameters are especially restricting. However, there are alternatives if these parameters were to cause an impasse for bonding with electroplated bumps. For example, research by Oppermann et al. has provided insight into TC bonding with electroplated nanoporous Au bumps. This technology allows for exceptionally low forces (<10MPa) and low temperatures ($150°C$) [40].

2.4.3. ENIG plating

ENIG plating is a bumping process for bumps similar to that of electroplating. The final bumps in ENIG consist mostly of Ni and are plated with only a thin layer of immersion Au. The process normally starts with a zincation process which removes any oxide on the chip Al contacts and activates the surface by means of zinc displacement plating. With the surface clean and activated, it is placed in a hypophosphase-based Ni bath that allows growth of a nickel-phosphorus alloy on the Al contacts. The process is autocatalytic of which 3 to 15% of the alloy consists of P [41]. Immersion Au is used to cover the Ni with an Au layer up to about $100nm$ in thickness. Thicker Au coatings can be achieved by additionally plating in autocatalytic electroless gold (0.5-1.5μm) [41].

ENIG plating has the considerable advantage of accuracy without the requirement of any lithography, sputtering or evaporation technology. However, due to the hardness of ENIG bumps, they are only suitable for a low number of contacts [42].

2.5. Types of adhesives

Flip-chip bonding is generally accompanied by an adhesive that ensures a more reliable interconnection between the chip and the substrate. It sits between the two interfaces and can act as a mechanical support as

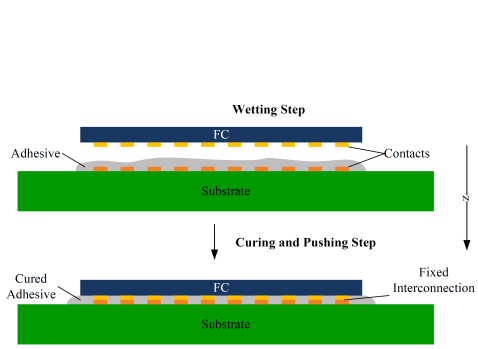
well as aid in electrical conduction.

2.5.1. NCA/NCF

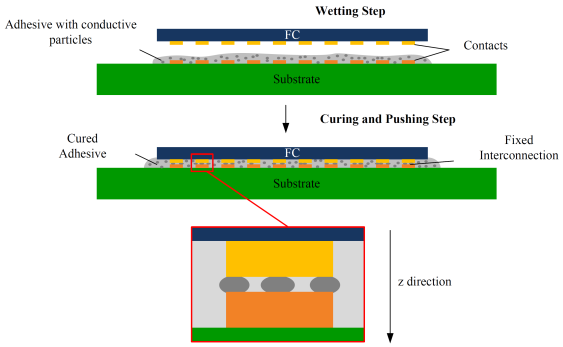
Non-conductive adhesives (NCAs) are adhesives (usually epoxies) applied in liquid form to the substrate before bonding. NCAs act only as mechanical support and are pressed away from the electrical contact interface during the application of pressure. Curing usually happens during the bonding procedure due to the temperature of the bonding procedure. Figure 2.6a shows a schematic overview of NCA bonding a flip-chip. Non-conductive films (NCFs) function similar to NCAs in their functionality but differ in the application of the material. Films are generally easier to apply and are more uniform than manual adhesive deposition. Thermoplastic Polyurethane (TPU) is a polymeric material that can be used as an NCF [43]. Being a thermoplast, it melts and forms during the bonding process after which it solidifies when the bonding process completes. It can be remelted because it does not cure like epoxies.

2.5.2. ACA/ACF

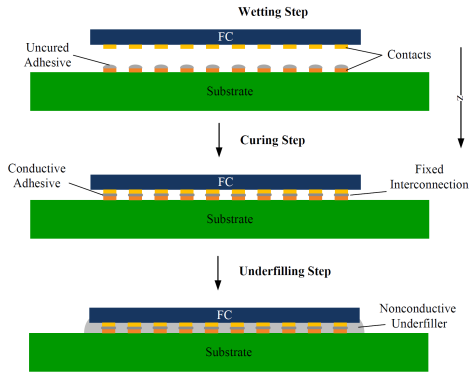
Anisotropic conductive adhesives (ACAs) are similar to NCAs but have some conductive particles added: usually Ag or Ni, sometimes coated by an additional layer such as Au. When bonding with an ACA, particles are caught between the contacts during bonding and therefore allow electrical conductivity only in the z-direction between contacts (anisotropic conductivity). However, one should take care of the size of the particles. If they are too small, bonding might fail, but if they are too big, they might start to form conducting lines in x- and y-directions (between contacts). ACA bonding requires less pressure compared to NCA bonding at the cost of current carrying capabilities [44]. Figure 2.6b shows a schematic overview of ACA bonding a flip-chip. Similar to NCAs, the ACA has a film counterpart called anisotropic conductive film (ACF).



(a) Schematic overview of NCA bonding.



(b) Schematic overview of ACA bonding.



(c) Schematic overview of ICA bonding.

Figure 2.6: Schematic overview of different types of adhesives in FC-bonding [35].

2.5.3. ICA

With isotropic conductive adhesives (ICAs), even more conductive particles are added compared to ACAs. The adhesive therefore becomes fully conductive and is only applied on the contacts to prevent shorts. Because of this, ICAs are generally applied only on larger contact surfaces beyond 127µm [44]. The assembly is

then strengthened with a non-conductive underfiller. Figure 2.6c shows a schematic overview of ICA bonding a flip-chip.

2.6. Biomedical polymer substrates

There is a wide variety of flexible materials that are commonly used in AIBMs, each with their own up- and downsides. Common biocompatible, flexible materials include: polyimide (PI), polyurethane (PU), parylene-C, polydimethylsiloxane (PDMS), SU-8 and liquid-crystal polymer (LCP). Table 2.3 gives an overview of the mechanical and electrical properies of some of these polymers. A polymer property that is often a consern for implantables is the elasticity, plotted also in figure 2.7. Ideally, the elastic modulus of a polymer should be as close as possible to the surrounding tissue, because it will behave mechanically similar to the surrounding tissue, causing less strain on the tissue and therefore less scarring during long-term implantation. Not surprisingly, tissue damage and scarring is one of the primary failure mechanisms in neural probes, starting between weeks to years after implantation [45].

Table 2.3: Overview of mechanical and electrical properties of biocompatible flexible polymers [46].

Properties of Polymers	Polyimide[a]	Parylene C[b]	PDMS[c]	SU–8[d]	LCP[e]
Precursor	BPDA/PPD	DPX–C	N/A	N/A	N/A
Possible thicknesses (μm)	1–15	1–100	10–100 for spin coating	1–300	25–3000
Density (g/cm^3)	1.10–1.11	1.289	1.08	1.075–1.238	1.4
Viscosity (Pa s)	5 $\pm$ 1	–	0.01–400	0.06–15	–
Moisture absorption (%)	0.8–1.4	0.06	$<$1	0.55–0.65	0.03
Melting temperature (°C)	–	290	–	–	280
Thermal decomposition temperature (°C)	$>$ 550	–	$\sim$250	300–315	–
Glass transition temperature (°C)	–	–	–	200–210	–
Thermal conductivity (W/cm K)	0.29	8.2	15–25	0.002–0.003	–
Thermal coefficient of expansion (ppm/K)	12	35	–	52	4–38
Specific heat (10^7 cm^2/s^2 K)	1.13	–	–	–	–
Specific resistivity (Ω cm)	$> 10^{16}$	$> 10^{16}$	10^{15}	7.8×10^{14}	1×10^{13}
Disruptive strength (V/cm)	1.510^s	2.6–10^6	2000	$>$4 10^5	4.7×10^6
Dieletric coefficient ε_r	3.5 (at 1 kHz)	3.1 (at 1 kHz)	2.6–3.8 (at 50 Hz)	3.2 (at 10 MHz)	3 (at 1MHz)
Loss factor tan δ	0.0013 (at 1 kHz)	0.019 (at 1 kHz)	0.002–0.02 (at 50 Hz)	–	0.02 (at 1 MHz)
Tensile strength (MPa)	392	69	6.2	60	182
Tensile module (MPa)	8830	20	0.1–0.5	20	10,600
Elongation (%)	30	200	600	4.8–6.5	3.4
USP class	–	VI	VI	–	VI

[a] UBE U–Varnish–S.[31]
[b] PCS Parylene C.[32]
[c] NuSil MED–1000.[33]
[d] MicroChem SU–8 2000 & 3000 Series.[34,35]
[e] Vectra MT1300.[36]

Out of all of these materials, PI is the most widely used material due to its "thermoxidative stability, high mechanical strength, high modulus, excellent insulating properties, and superior chemical resistance" [46]. Furthermore, PI is generally considered biocompatible and has long-term stability in *in vitro* environments [47], although no official FDA approval has been given. The strength of PI as an implantable material is also its weakness for some applications. One can see in table 2.3 that the elastic modulus of polyimide comes close to that of hard biological tissue, making it an unlikely candidate for long-term implantation in soft tissue such as the CNS.

Due to this very reason, some research has opted for more flexible polymeric materials such as polydimethylsiloxane (PDMS). As a hybrid methodology, PDMS is used as an encapsulant on more rigid substrates [49][50], allowing for softer interaction with surrounding tissue. Research by Guo et al. has also proven that PDMS can be used as a standalone substrate material by patterning Au tracks on PDMS using lift-off [51], structuring even on three interconnect layers [52], though adhesion and long-term stability remains to be

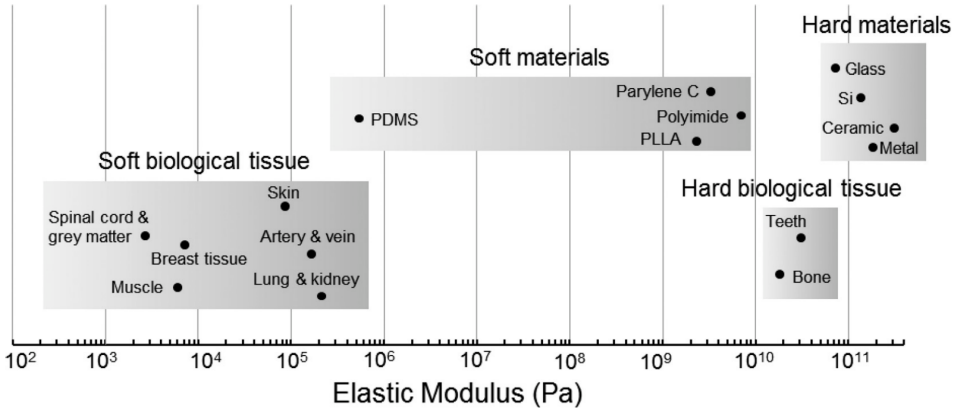


Figure 2.7: Elasticity modulus of different implant materials and biological tissues [48]

proved. PDMS has USP class VI certification and a clear advantage in soft biological tissue compared to other polymers (figure 2.7), but is also more difficult to handle in manufacturing processes due to this very property. Another pitfall of PDMS is its moisture absorption, which can promote implant degradation and can change electrical properties.

In contrast to PDMS and PI, Parylene C [poly(dichloro-p-xylylene)] excels in water barrier capabilities. Electrically, it has excellent electrical properties. Mechanically, it benefits from a slippery surface, has higher elasticity than PI and it can be deposited at room temperature. Medically, it is biocompatible (FDA approved) and it is inert both chemically and biologically. On the other hand, Parylene C sheets are known to be fragile and deposition is done with specialized reactor chambers [46].

TPU is a material that lies between PDMS and PI in terms of its elastic modulus, ranging between 10^7 – $10^9 Pa$ [53]. It is widely considered biocompatible and biostable, finding its way into both neurostimulation and orthopedic applications even though to-date is has not been approved by the FDA. Like PI, manufacturing with TPU is done by means of sheets or as a curable liquid. However, TPU has a significantly lower working temperature (down to $80°C$ [54]). Furthermore, being a thermoplast, TPU can be remelted without changing the material properties. This has tremendous potential for implant longevity because it allows for lamination without an interface [55], which is a well-known cause of long-term implant failure [56]. Additionally, thermoplastic properties allow for better electrical and mechanical properties during annealing processes in flip-chip bonds [35].

3

Summary of the work

The main aim of this work is to provide technology that allows for the routing of thousands of electrodes to a chip on a fully flexible and fully implantable substrate. The prime purpose of such technology is twofold: 1) obtain detailed knowledge on neural functioning and malfunctioning by means of (long-term) mapping of the neural network using a recording electrode network, and 2) provide a technology that can interweave electronic stimulation with neural tissue closely enough to allow for neural and neuroprosthetic control, offering potential solutions for neural malfunction (such as epilepsy and Alzheimer's) and injury (such as spinal-cord injuries and amputation). Flexibility and implantability are important aspects for the longevity, usability and comfort of implantable electronics, though no implant to-date is able to facilitate this for more than a couple of tens of electrodes (see section 2.2). In addition, the large number of sites for neural interaction that this technology potentially allows introduces redundancy options in the array of electrodes. This can prevent the numerous problems following surgery misalignment and scar formation by shifting functionality to neighbouring electrodes and can improve implant longevity.

Based on the described aim, the most likely implantation site for implants based on this technology would be the Central Nervous System (CNS), the retina or the cochlea because of their density of neural signals. The retina and cochlea are more bone-like and allow for implantation of harder flexible materials, such as Polyimide (PI), even for longer-term implantation (see section 2.2). The CNS is a much softer tissue and benefits from a very soft implant material, however such materials are more experimental in terms of fabrication, generally lacking in high-density metallization.

Two polymers were experimented with over the course of this project. PI was initially chosen because it is mechanically and chemically the most stable flexible material, giving little limitations to manufacturing parameters during further processing, such as assembly. In addition, there is an established process flow available for PI substrates with 2 Cu metallization layers within Fraunhofer IZM (see section 4.5.1), and a more advanced wafer-level process flow for up to four integrated Cu metallization layers in PI (see section 2.3.4). The metallization for the first prototypes was Cu which was plated using immersion Au coating (explained in section 4.5.1). Results can be found in section 5.2, showing workable initial results between 1.2 and 4.0$m\Omega$ (see section 5.2.3).

The next step in the process was to move to a manufacturing method where Cu is not present in the final prototype because Cu is not a biocompatible material and therefore not desired in implantable systems. This new process involves Au patterned onto Cu which is transferred to a polymer after which the Cu is etched. This process is explained in section 4.5.2. The results of this process can be found in section 5.3 and were not as fruitful as hoped, showing significant voids in the chip adhesive and damage due to Cu etching (see section 5.4). Most fundamentally however: none of the established processes allowed for pure-Au metallization (only Au-plated Cu) and PI is inherently very non-elastic (see section 2.6) making it an unlikely candidate for implantation in soft neural tissue such as the CNS. In addition, the adhesion strength between material layers, such as PI to NCA, was often unknown and adds complexity and possible points of failure to the technology.

For this reason, polymer substrate materials were re-evaluated and Thermoplastic Polyurethane (TPU) showed most potential. The main reason for TPU is its thermoplastic properties, which allow melting of the material without changing its properties. This enables lamination of multiple polymer layers without forming any interface between the layers, subsequently improving lifetime of the implant. In addition, TPU is a very

elastic material compared to other polymers and manufacturing with TPU is well established within Fraunhofer IZM. The process using TPU is explained in section 4.5.2. Section 5.5 shows significantly improved results in initial prototypes, with no visual void formation and significantly better Au-to-polymer adhesion. One sample in particular showed very good 4-point measurement results between 4.5 and $14m\Omega$ (section 5.5.3), with failures most likely caused by residual Cu etching solution and (height) inconsistencies in chip contacts.

During the infancy of this work, it was unclear what the limitations of the technology available inside the Fraunhofer IZM were. This, alongside the experimental nature of the work, meant that an iterative way of progressing would be beneficial for the final result. At the core of these iterations is the chip, because a chip is the most rigid element in an implant and should therefore be as small as possible to reduce the implant's rigidity (as explained in section 2.6). With respect to the chip, iterations had to be made in two directions: contact size and number of contacts. The contact size is an inevitable parameter when designing an optimally sized chip, this will become clear in section 4.1. For a certain contact size, increasing the number of contacts inevitably requires the chip to become larger. However, in addition to the required area for contacts, they each require area for routing to the periphery below the chip. The exact area required to redistribute each contact to the chip periphery was optimised in this work. The optimisation takes into account technology parameters of the substrate material, such as minimum track width, via size and number of metallization layers. The functionality of this optimisation is described in section 4.1. Optimisation results for the ultimately desired 10.000 connections can be found in section 5.10.

Regarding chip iterations, it was decided to first optimise in contact size and miniaturize connections as far as possible before scaling to a high number of contacts. A multi-functional chip was produced that allows for three different kinds of contact sizes to be investigated, $80\mu m$, $40\mu m$ and $20\mu m$ square contacts. This allows iterative experimentation with contact size without having to produce multiple chip designs. Each set of contacts can be evaluated by means of 4-point measurements and daisy chaining as explained in section 4.2. The chip measures at $\sim 500\mu m$ thickness. Further functional details of the chip can be found in section 5.1.

Successive effort was put in an assembly with a new high-density chip. This chip, named '361008', consists of 1008 contacts in a more dense contact array compared to the previous design. This chip design was based on results of the optimiser, details can be found in section 5.6. It has similar bond evaluation structures as the first chip iteration. The chip was produced at two different thicknesses: $500\mu m$ and $300\mu m$. This chip has an unheard-of connectivity density more than four times higher compared to existing neurostimulating systems (see section 2.2).

In section 4.4 the interconnect options for the chips are evaluated. Flip-chip bonding was considered the most mature process for very high-density interconnect structures and was the most accessible technology available in Fraunhofer IZM. Later work with TPU shifted the process of choice to a hybrid between conventional flip-chip bonding and the embedding process, essentially taking the best-of-both-worlds in terms of criteria discussed in section 4.4.

Based on flip-chip bonding as an interconnection technology, the first chip iteration had AuPd stud bumps that were placed manually using a wire-bonder. This was a quick and cheap way to start flip-chip prototyping in an early stage of the project. These type of interconnects sufficed for initial experiments but were unreliable for a higher number of contacts. The second chip iteration was manufactured with electroplating (EP) rather than stud bumping due to the reliability, miniaturization and scalability potential it has in future research (see secton 5.6). The manufacturing details of both chips is explained in section 4.3. As flip-chip underfill and adhesive, experiments were conducted with an epoxy-based NCA as well as TPU functioning as an NCF.

Towards the end of the thesis, efforts were spent on the assembly with the 361008 chip in an all-TPU substrate assembly. Section 5.7.1 elaborates on the mixed outcomes of this chip in a TPU assembly and concludes with a bonding profile that works well with the Cu carrier and TPU. Measurement results in section 5.7.3 reveal that bond yield was in the order of 90% for the three samples bonded with this bonding profile. Learnings with the 361008 chip were used to manufacture a demonstrator which is able to route 324 of the 1008 chip I/Os to electrodes $200\mu m$ in diameter via Au tracks between 15 and $100\mu m$ thick. The chip in this prototype is $300\mu m$ thick. The prototype is completely embedded in TPU measuring at $600\mu m$ of thickness

over a surface of roughly $16.8cm^2$. Details on this demonstrator can be found in section 5.9. To the best of the authors knowledge, this is the first time that up to 324 connections are made to a chip in a completely embedded and fully flexible substrate.

3.1. Novelty of the work

The novelty of this thesis lies in three main aspects: the optimisation, use of material and the connectivity density. To the best of the author's knowledge, the optimisation technique as presented in section 4.1 offers profound advantage in routing optimisation in flexible implants because implants are particularly limited by technology parameters and chip dimensions. Technology parameters in flexible substrates have shown to be especially constraining in terms of metallization layers, a parameter to which the proposed technique can indeed optimise. If IC design is co-developed with the substrate fabrication limitations in mind, the proposed optimisation technology offers design parameters that allow for minimal chip size for a large number of chip I/Os. The main limitations regarding the IC design are that it has to fit in these reduced chip dimensions and that it should match set electrical specifications such as cross-talk even in high-density configurations.

The second aspect of novelty is the use of material, in particular: the use of TPU. To the best of the author's knowledge, this work is the first to describe a flexible substrate with a routed chip which is completely embedded with only TPU, including the chip underfill material. Due to the thermoplastic properties of TPU, this has significant potential in the longevity of such implants because separate sheets of TPU do not form interfaces, which are known to cause long-term failure.

Thirdly and finally, a comparison with state-of-the-art systems in table 2.2 reveals that this work has initiated a plausible manufacturing technique that allows for the highest connectivity of electrodes to-date in AIBMs. Where other systems fundamentally fail to offer at least one of the criteria (flexibility, biocompatibility, implantability, hundreds of electrodes), this work has the potential to check each criterium. To the best of the author's knowledge, with a chip measuring at $\sim 160mm^2$ for 10.000 connections, this technology surpasses connectivity density of any of the existing state-of-the-art systems more than fourfold.

4

Materials and methods

This chapter will dive into the details of used process workflows and theoretical derivations. Section 4.1 details the theoretical work on optimising the routing to the chip and shows the workings of the optimiser software. Section 4.2 explains how the bonding quality of prototypes can be characterized and informs about naming conventions. Section 4.3 briefly explains the manufacturing steps of the chip and 4.4 elaborates on the advantages and disadvantages of the chip connection processes that were explained in section 2.3. Finally, based on the chip design and chosen chip connection process, section 4.5 will elaborate on the additive build-up and transfer-based substrate manufacturing processes used throughout this work.

4.1. Array routing optimisation

One obvious question regarding the substrate states: how can we optimally route the substrate connections outward? This type of routing is often called "escape routing" in the industry and can quickly become a complex mathematical problem depending on technology limitations and connection properties such as crosstalk, impedance and exit location [57]. For the sake of simplicity we will consider only the escape routing of the required pads and the technological limitations of the substrate process, including:

- Track width
- Track pitch
- Pad dimensions
- Pad pitch
- Number of substrate routing layers

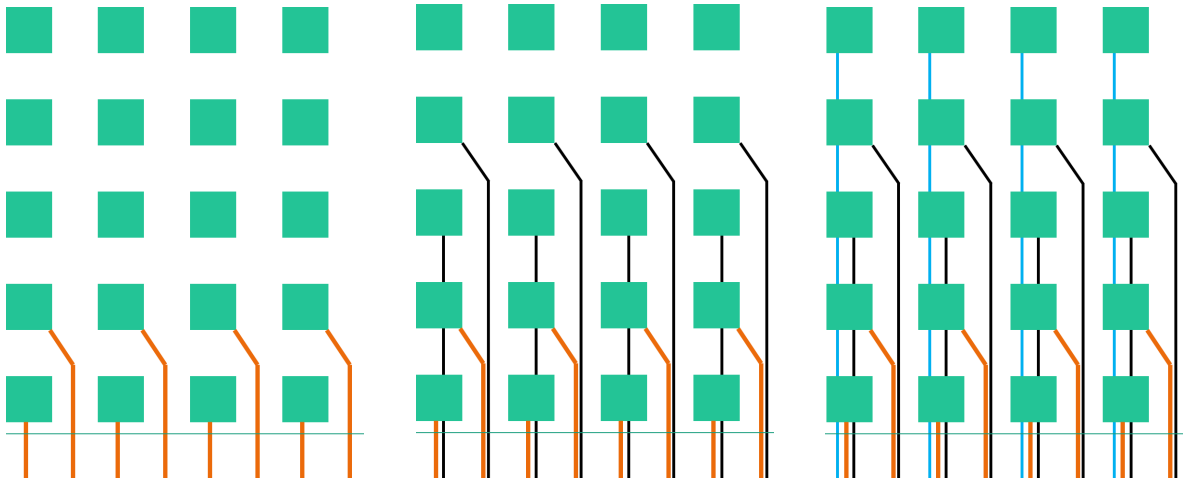
The traditional way of routing arrays in the PCB technology is by means of column routing. This way of routing will route the PCB column-by-column utilizing a new metallization layer when no more tracks fit on a layer. A step-by-step example of this method can be found in figure 4.1.

4.1.1. Calculating chip dimensions

Given a certain routing strategy on our substrate, it would be convenient to know what the chip dimension d would be given the total number of pads (let's name this N) and the pitch p. If we consider a full array of pads on a square chip with evenly distributed pads, this is quite trivial to calculate:

$$d = (\sqrt{N} + 1) * p \tag{4.1}$$

Meaning that an array of 40.000 pads at $40\mu m$ pitch would result in 200 pads on one side, or a chip of roughly $80x80mm^2$. However, it is unlikely that there are enough layers in our flexible substrate to route all these pads. We would need to route 100 columns deep if we would apply the method shown in figure 4.1. If we were to route 2 columns per metallization layer we would need a 50-layer PCB, which is unheard of and



(a) Column routing of the outermost two columns.

(b) Column routing of third and fourth column of the array.

(c) Column routing of fifth column of the array.

Figure 4.1: Steps of column routing a pad array. Orange, black and blue lines all indicate different layers in the substrate. Via routing is done directly under the pads.

most likely not flexible.

We therefore need to distribute the pads in such a way that it becomes routable on a given amount of metallization layers. To ease the calculations, a division in an array can be made for optimisation. This, as well as some parameter indications, can be found in figure 4.2. The sectioning in the figure gives us the option to only optimise a fourth of the array (the yellow sector in the figure) and to just copy this result to the other three sectors (the green, red and purple sectors). Evidently, there are other ways to sector and route an array. For example, triangular routing [58] or hexagonal patterns [59] can improve routing density to some degree. However, since the traditional routing method will route all connections via the shortest way out, it will decrease total track length to a minimum and will consequently avoid the significantly more complex routing patterns and calculations involved in applying these more optimal techniques on large arrays.

If we would like to properly apply the routing technique of figure 4.1, we should include the number of routable rows, R, in our equations and ultimately find a formula with which we can express chip dimension d as a function of N, R and p. Consequently, this will mean that our chip will become bigger than what we previously calculated simply because all the pads that we cannot route in the center of the array will need to be moved to the periphery until we have a value of R that corresponds to a reasonable amount of layers. For flexible polyimide substrates, there will be about 4 available layers [34], but let's stick to variables for now. To clarify, note that:

$$R = \sum_{n=1}^{L} r_n \tag{4.2}$$

Where r equals the number of routable rows in a layer and L equals to the number of layers in the flexible substrate. Values of r are dependant on technology parameters. We can calculate chip dimensions by calculating the number of outer bonding areas on a single side and multiplying this number by the pitch. We can say that:

$$N_{outer} = \frac{l}{p} \tag{4.3}$$

$$l = N_{outer} * p \tag{4.4}$$

Where N_{outer} equals the number of pads on column 1 on a single side and where l corresponds to the total length of this column. Note that:

$$d \approx l + 2p \tag{4.5}$$

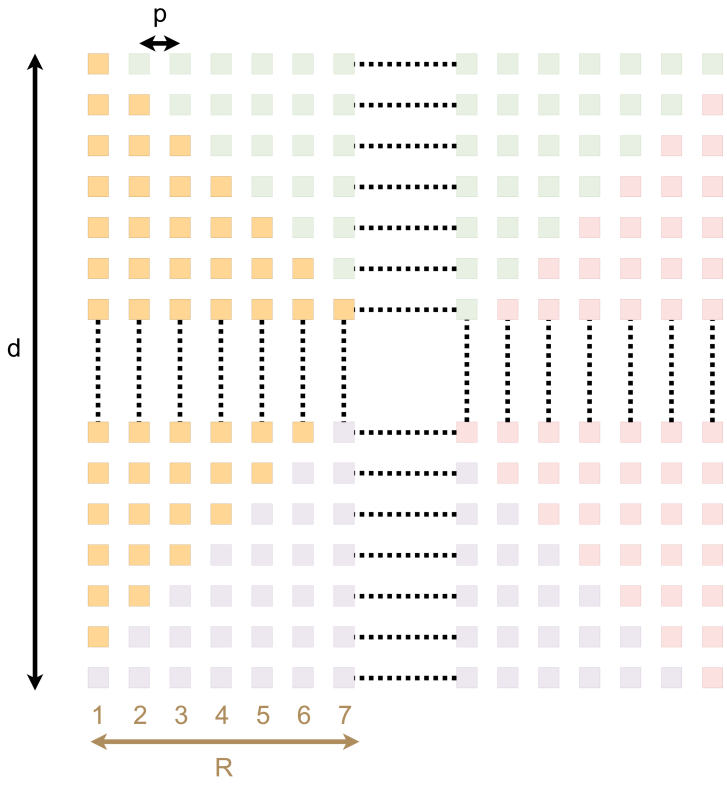


Figure 4.2: Pad array visualization. The highlighted yellow pads resemble a quarter of the array that can be repeated four times to form the entire array. Black dots indicate repetition of pads. d indicates the dimension of the chip, p indicates the pitch, R indicates the number of routable rows in the yellow sector. Note that in this example R can be 7 maximum (leaving the middle area empty), but can be changed depending on the routing possibilities.

We also know that each consecutive inner column loses 2 pads (because of the pyramid shape seen in figure 4.2) and so we can say:

$$N_{inner} = \frac{l}{p} - 2(c-1) \tag{4.6}$$

Where c corresponds to the column number as numbered in figure 4.2 and N_{inner} corresponds to the number of pads in column c. Combined, we can say:

$$N_{inner} + N_{outer} = \sum_{c=1}^{R} \frac{l}{p} - 2(c-1) \tag{4.7}$$

Which we can also simplify to:

$$N_{inner} + N_{outer} = R\frac{l}{p} - \sum_{c=1}^{R} 2(c-1) \tag{4.8}$$

However since c is related to R, we can further simplify to remove the summation:

$$N_{inner} + N_{outer} = R(\frac{l}{p} - R + 1) \tag{4.9}$$

According to equation 4.9 and 4.3 we can now say that:

$$N_{inner} = R(\frac{l}{p} - R + 1) - \frac{l}{p} = (R-1)(\frac{l}{p} - R) \tag{4.10}$$

Giving us the number of outer pads with inclusion of R and N:

$$N_{outer} = \frac{N}{4} - (R-1)(\frac{l}{p} - R) \tag{4.11}$$

Finally, substituting equation 4.11 in equation 4.4, we ultimately arrive to:

$$l = (\frac{N}{4R} + R - 1)p \tag{4.12}$$

And we can approximate using equation 4.5 that:

$$d \approx (\frac{N}{4R} + R + 1)p \tag{4.13}$$

Repeating our earlier example and assuming 8 routable columns (4 layers, 2 columns per layer), we find a chip dimension of approximately $5.0 \times 5.0 cm^2$ instead of a previously estimated $80 \times 80 mm^2$.

4.1.2. Array optimiser and visualizer

A MATLAB script was written to automatically use the earlier calculated formulae and find the optimal distribution of chip connections. This script can be found in appendix A. It assumes a range of reasonable parameters and sweeps through all of them, calculating the dimensions for each configuration (roughly 200 configurations are generally considered). All pad distributions are forced uniform, meaning that if the desired number of pads does not solve into a uniformly distributed ring or array the number will be rounded up until this holds true. The script then verifies some of the equations in chapter 4.1.1 and finally outputs some information to the user, including:

- A print of all parameters relevant for the smallest design, including chip dimensions (d), number of pads (N), pad size, center-center pad pitch (p), number of rows (R), number of pads on one side of the periphery and number of layers.
- An identical print for the smallest full-array design. This design is beneficial if a uniform mechanical bonding pressure during the bonding process is desired.
- A visualization of both designs, plotting them to-scale and showing how the pads are distributed (see figure 4.3a).
- A plot to show the influence of center-center pitch between pads to the overall size of the chip (see figure 4.3e).

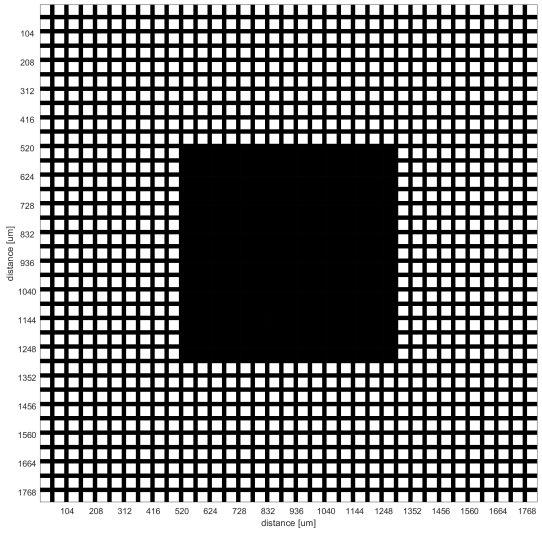
The optimiser works roughly as follows:

1. The script starts with initialization of variables, generating values for all indices. The number of indices - determined by the user - determines how many chip array configurations should be considered. The first index for the calculation will hold the smallest distance possible between pads, whilst each consecutive index will add 1 micron to the previous pitch value.
2. Assuming each of these pitches between pads, the script determines how many rows it can connect to the periphery of the chip for each index. This is done in a way similar to that described in figure 4.1.
3. The script now determines the size of the chip based on the formula found in formula 4.13, as well as the corresponding amount of total pads and outer pads.
4. The script verifies that the theoretical formulae determined in chapter 4.1.1 hold.
5. The script generates a visualization array to scale for the optima that are found. It outputs all prints found in figure 4.3 to the user.

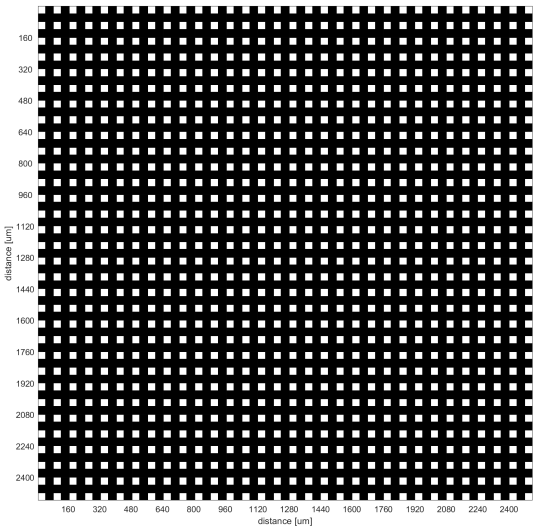
A graphical overview of important variables in the script can be found in figure 4.4. All variables - including the variables in the figure - are explained in detail in appendix A.

4.2. Bond quality testability

Two measurement techniques are implemented in the chip and substrate to evaluate the bond strength between the chip and the substrate. These techniques are merely used for researching different bonding techniques and are not meant to facilitate high-density routing. Once a reliable bonding technique has been established and suits the requirements set in chapter 1.4, the technique will be applied on a high-density multi-layer substrate.



(a) Visualizer script output example for 1000 desired connections distributed optimally for a 4-layer substrate. White squares mark chip connections.



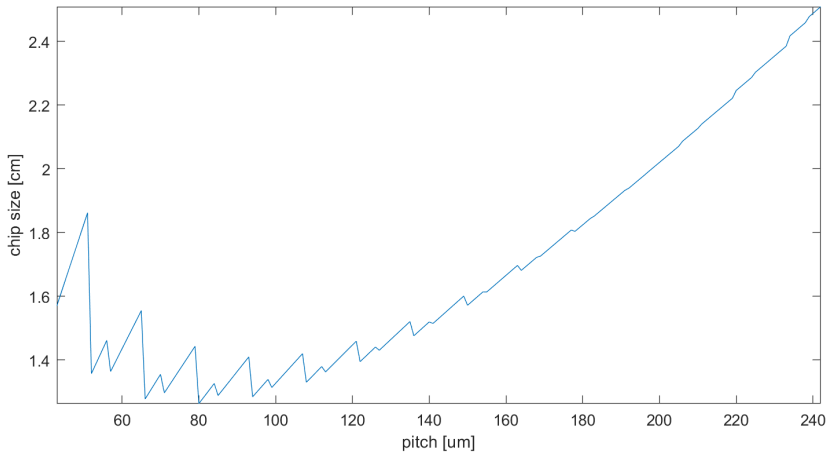
(b) Visualizer script output example for 1000 desired connections distributed optimally for a 4-layer substrate in a full-array manner. White squares mark chip connections.

```
Smallest design will have the following specifications:
Chip size:          0.187 cm
Number of pads:     1000
Pad size:           36 um
c-c pad pitch:      52 um
Rows:               10
Outer pads:         35
Number of layers:   4
```

(c) Visualizer script print output example for 1000 desired connections distributed optimally for a 4-layer substrate. Corresponds to array output found in figure 4.3a.

```
Smallest full-array design will have the following specifications:
Chip size:          0.263 cm
Number of pads:     1024
Pad size:           36 um
c-c pad pitch:      80 um
Rows:               18
Outer pads:         32
Number of layers:   4
```

(d) Visualizer script print output example for 1000 desired connections distributed optimally for a 4-layer substrate in a full-array manner. Corresponds to array output found in figure 4.3b.



(e) Optimiser plot example for 10.000 connections showing the influence of center-center pitch distance to the overall chip size.

Figure 4.3: Graphical output of the optimiser script. Design rules for given example were: $36 \times 36 \mu m$ in size, $7 \mu m$ track width and spacing, $17 \mu m$ via size and 4 metallization layers.

4.2.1. 4-probe measurements

The first technique applies the Kelvin 4-probe measurement technique to accurately measure the resistance of an individual bond [2]. A 4-probe measurement requires two connections to both sides of the resistance that needs to be measured. In the case of this setup, it means that two connections are needed on the substrate side of the bond and two on the chip side. These should be routed out to larger pads that can be probed. Figure 4.5 shows how these connections are made. Note that this technique bypasses one bond to allow for the second connection on the chip side, excluding it from the previously mentioned daisy-chain measurement. As stated in the figure, we can say:

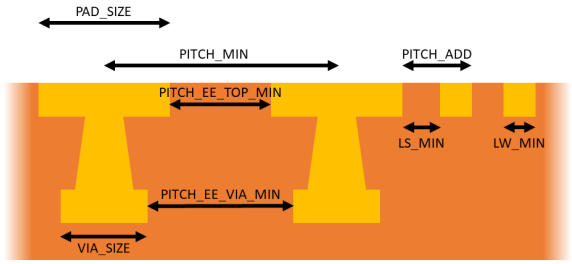


Figure 4.4: A cross-section view of a substrate with design rule names as used in the MATLAB script. Variables are explained in appendix A

$$R_{bond} = \frac{U_{meas}}{I_{in}} \tag{4.14}$$

Prototypes are fitted with at least eight 4-probe measurement sites. Four to measure the resistance of each of the chip's corner connections, and four halfway each of the chip edge. This is also visualized in figure 5.1a. Note that there can be slight variations in the measured value based on the measurement configuration. For example, if the two 'top' connections (the right connection of I_{in} and U_{meas} in figure 4.5) are swapped, it will still be a 4-point measurement of the contact but the current will flow slightly different and the voltage measurement will be slightly different as a result too. A similar truth holds for the 'bottom' connections. Therefore, there are 4 ways to measure the same contact resistance with slightly different results [60].

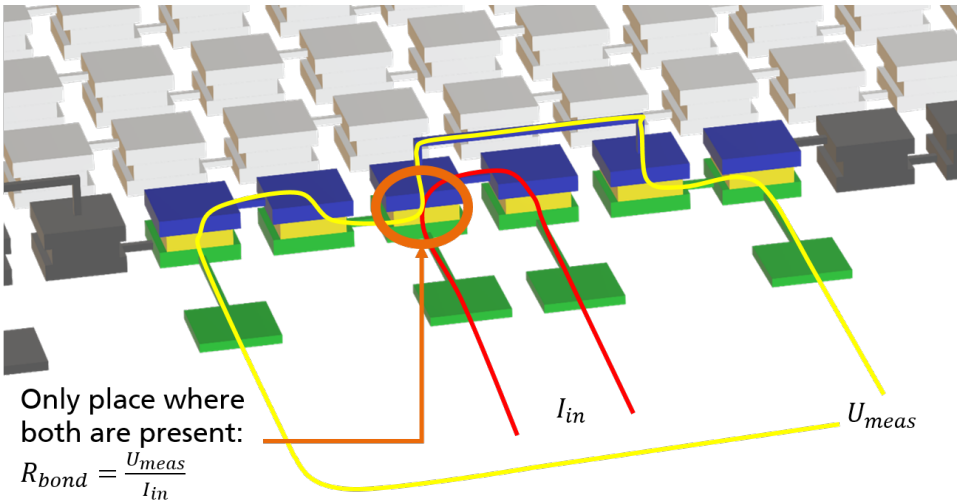


Figure 4.5: A simplified 3D-view of the 4-point measurement principle. Blue indicates chip metallization, yellow indicates the bond and green represents the substrate metallization. The red line indicates how the current flows during an impedance measurement, while the yellow line indicates the voltage path that will be measured. The measured pad is encircled in orange.

4.2.2. Daisy-chaining

The second technique is called daisy-chaining and evaluates all bonds by measuring their resistance in series. It is implemented by connecting metal pads in the chip and substrate to form a chain-like connection through the entire bonding area of the chip (see figure 4.6). The chain has four endings which can be connected to measure the impedance of the full chain with a 4-probe measurement. If all bonds are well, the impedance will be low (in the order of a 10mΩ per bond [61]). Obviously, the total impedance will increase if one more more bonds fail (in the order of 100mΩ for a single bond [61]). Note that the implementation of the previously mentioned technique, by chance, allows also to measure segments of the daisy-chain, allowing for partial daisy-chain measurements as well as options to narrow down a point of failure.

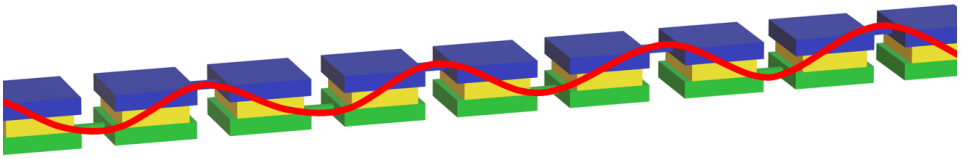


Figure 4.6: A simplified 3D-view of the daisy-chaining measurement principle. Blue indicates chip metallization, yellow indicates the bond and green represents the substrate metallization. The red wave-like line indicates how the current flows during an impedance measurement of the daisy-chain.

4.2.3. Test substrate naming conventions

To avoid any misinterpretation during the measurements of prototypes a naming convention was implemented. Measurement connections are labeled either 'S' (start of 4-point daisy-chain), 'F' (finish of 4-point daisy-chain), 'C' (4-point measurement at chip corner) or 'M' (4-point measurement halfway chip edge). Middle and corner connections are marked with a number to distinguish which side of the chip it corresponds to (between 1 and 4) as well as a letter 't' or 'b' indicating whether the connection reaches to the top or bottom of the corresponding bond. As long as the current runs from top to bottom and voltage is measured from top to bottom (or reverse, both from bottom to top) the measured resistance should be the same. For example, one could measure contact resistance of 'C1' by running a current from pad 'C1t' to 'C1b' and measuring the voltage over the other identically labeled pads. Note that some pads are marked with two labels because they can be used for multiple 4-point measurements.

In addition, all chips and substrates are given a type number consisting of the pad size and followed by the number of contacts. For example, a chip with bumps on 72 pads dimensioned $80\mu m$ is named '8072'. Substrates have a versioning number in addition because multiple versions were made for most iterations, so a fitting substrate would be named '8072 V3' for example.

4.3. Manufacturing dummy chips

To test the manufacturing of a prototype, chips have to be designed and fabricated. Several custom designs are presented in chapter 5. These chips are made at EKL, a cleanroom facility at the Delft University Of Technology, as part of another MSc thesis. An overview of the manufacturing process can be found in figure 4.7, manufacturing details can be found in the work by Velea [62].

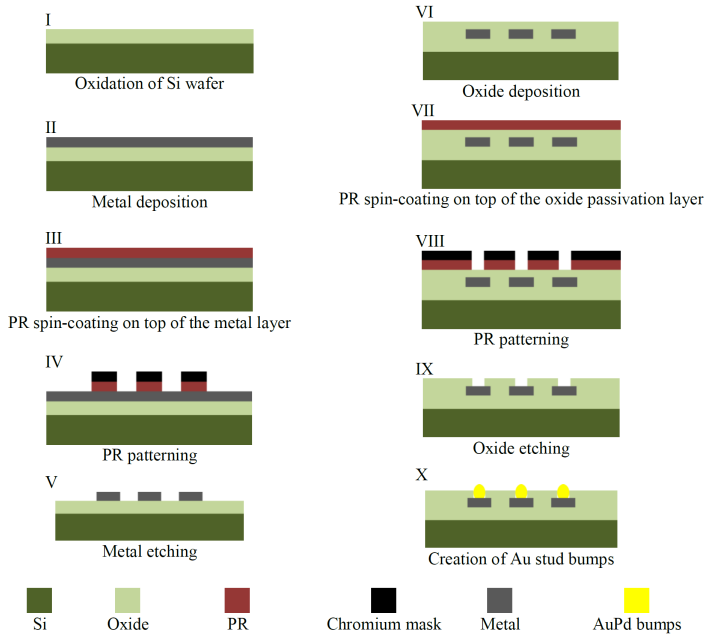
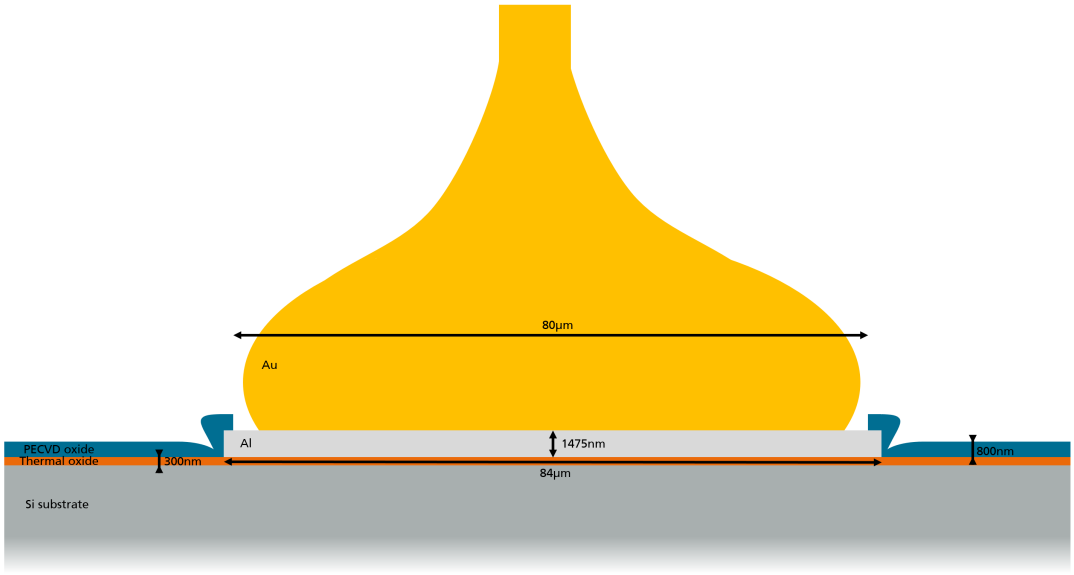
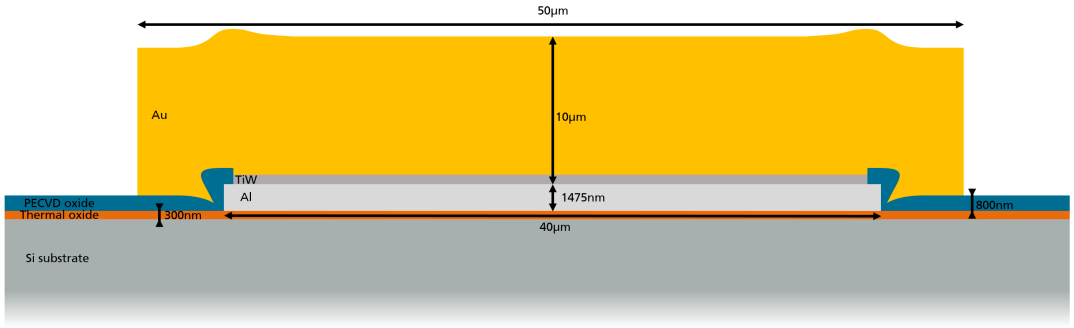


Figure 4.7: Process flow for the development of dummy chips on a Si wafer [62].

Dummy chip contacts were either stud bumped (manually) or electroplated by an external manufacturer (wafer-level process as explained in section 2.4.2). A schematic cross-section of a stud-bumped and an EP chip can be found in figure 4.8. Note that for electroplating, the bump is wider than the contact opening ($50\mu m$ compared to $36\mu m$). This was done for budgetary reasons: a lower electroplating resolution at $50\mu m$ was less expensive compared electroplating on $36\mu m$ sized contacts.



(a) Schematic cross-section of a stud bump on a 8072 dummy chip. Dimensions are not to scale.



(b) Schematic cross-section of an EP bump on a 361008 dummy chip. Dimensions are not to scale.

Figure 4.8: Schematic cross-sections of different bumping types.

4.4. Connecting the chip

Considering the types of bonding available, as explained in section 2.3, an overview was made to evaluate which of the options is most suitable for this application. A simplified overview of this can be found in table 4.1 (for the full overview, please refer to appendix B). Wire bonding and TAB were discarded due to their limited bonding density options as well as their limited mechanical flexibility. Embedding offers distinct advantages in terms of encapsulation since it completely covers the chip inside of the substrate. However, the technology is very new and therefore still expensive and unreliable. In particular, there were no embedding techniques (such as the work by Zoschke et al [63]) available within Fraunhofer IZM that were established enough to prototype with.

This leaves flip-chip bonding as the most likely candidate due to its all-round assembly advantages, wide availability of literature and solid availability within the Fraunhofer IZM. Specifically, thermocompression (TC) flip-chip bonding was chosen due to its availability and knowledge within the facility, though ultrasound (US) bonding can be considered if too much pressure or temperature is required for bonding. The most critical parameter for TC bonding is temperature, which is limited by the temperature that the polymer

substrate and adhesives can handle. The TC pressure parameter is chosen accordingly, as explained in detail in figure 2.3. The prefered candidates in terms of adhesives are the NCA and NCF due to their biocompatibility, although the ACA or ACF can be considered if too much pressure is required in the bonding procedure.

Table 4.1: Simplified overview of considered bonding methods. The full evaluation can be found in appendix B.

	Wire bonding	TAB	flip-chip	Embedding
Density				
Flexibility strength				
Biocompatibility				
Availability				
Maturity				
Encapsulation				

The TC flip-chip bonding process is performed in an *ISO6* cleanroom, meaning that there can be up to 1.000.000 particles $< 0.1\mu m$ in diameter per cubic meter of air. The SET FC150 thermocompression bonder is used in particular, of which a picture can be found in figure 4.9. The main component of this machine is the bonding head, which holds a tool that can pick and place chips with a $\pm 1\mu m$ placing accuracy. The bonding head can heat the chip it holds to up to $450^{\circ}C$ and applies up to $100kg$ of weight during the bonding. The bonding tool that it holds is available with a variety holding tips depending on the size of the chip that is to be bonded. The surface of the tip is usually in the dimensions of the chip (or bigger) and has a vacuum opening so the bonding head can hold the chip. Below the bonding head, one finds the substrate holder which keeps the substrate in place by means of vacuum. It can heat the substrate up to $450^{\circ}C$ and has micromanipulators in x, y, z and θ (angle along z-axis) directions for alignment to the bonding head. A bi-directional microscope can be positioned between the bonding head and substrate holder to simultaneously view chip and substrate for the purpose of manual alignment.

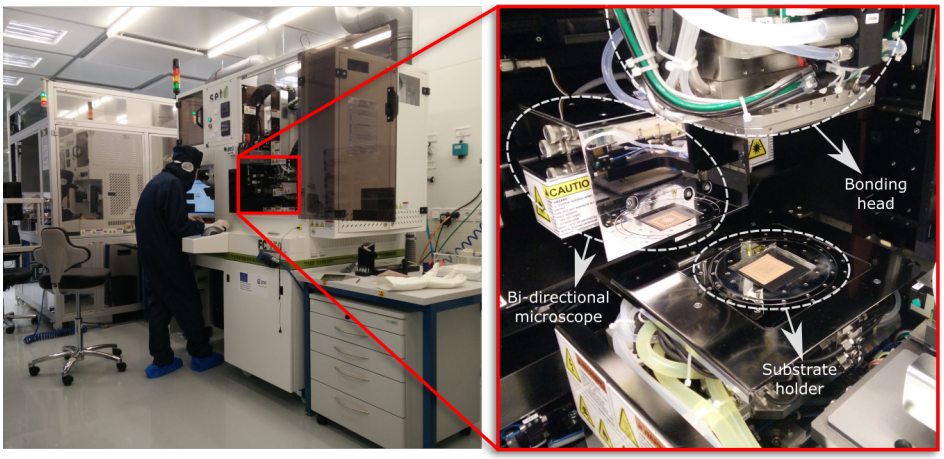


Figure 4.9: The SET FC150 thermosonic flip-chip bonder. The bi-directional microscope is used to align the bonding head (holding the chip) with the substrate holder. The microscope is retracted to the rear in this picture to show the substrate holder.

4.5. Flexible substrate manufacturing

Based on the conclusion that flip-chip bonding is most suitable for the purpose of this thesis (section 4.4, three process flows were used for assembly. The initial additive build-up process flow was already present in Fraunhofer IZM and is explained in section 4.5.1. However, this process is limited to a specific type of PI and introduces the polymer substrate in the first step of processing. Introducing the polymer later in the process is important to prevent damage and contamination of the material and widens the working parameters in

preceding stages (maximum temperatures, for example). A transfer-based process was therefore developed especially for this thesis in which assembly is done on a temporary carrier substrate, of which the structures are transfered to a polymer at a later stage. Section 4.5.2 explains the two transfer-based processes designed for this thesis. The first includes an epoxy-based NCA chip underfill and is suitable for polymers that can be found as curable liquid, such as polycarbonate (PC) and PI. The second process works specifically for TPU, used as NCF underfill as well as substrate material, and takes advantage of the thermoplastic properties of the material. TPU sheets melt and merge during the lamination which removes any interface between the underfill and embedding layers. This improves adhesion and system lifetime [55][56].

4.5.1. Additive build-up process

Initial substrate prototypes were made out of PI with up to two layers of Cu. The manufacturing process is an established process of Fraunhofer IZM and makes use of Espanex S Series by Holders Technology: cured PI sheets ($50\mu m$ thick) pre-laminated with Cu on both sides ($15\mu m$ thick). This is the starting point of the flow-chart described in figure 4.10. During steps II to IV, vias are made in the PI. This is done by means of laser drilling (step II), followed by a Pd plating bath that only attaches this metal to the PI and allowing the vias to be plated (step III). The entire substrate is then electroplated with Cu to cover the deposited Pd layer (step IV). In steps V through X, the copper is patterned on both sides of the PI. An acidic roughening solution (step V) allows for better adhesion between PR and Cu during a roll-lamination process (step VI). The PR is positively illuminated using Laser-Direct Imaging (LDI) lithography (step VII) after which all uncured PR is etched (step VIII). The opened-up Cu is etched in a cupric chloride etching line and finally the cured PR is stripped (step X). To allow for Au-Au bonding, the substrates are plated with a thin layer of immersion Au ($\sim 100nm$). Finally, the sheets are cut into individual samples using laser cutting.

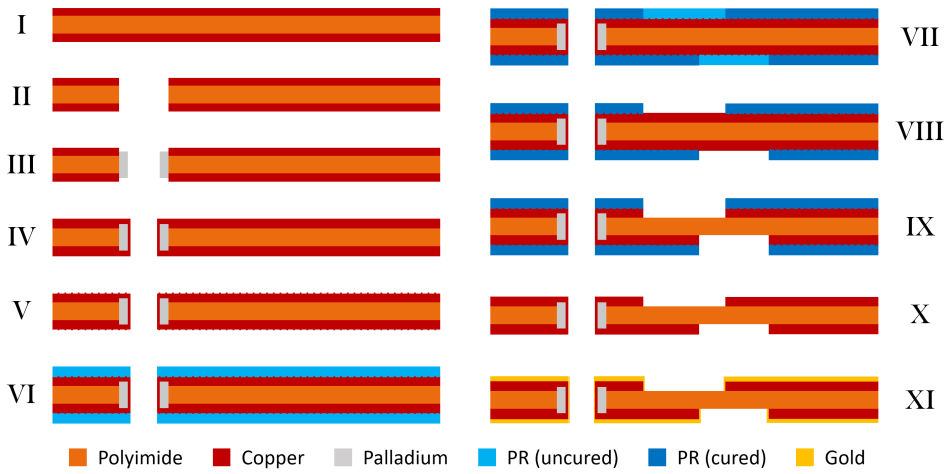


Figure 4.10: Process flow for manufacturing 2-layer PI substrates with Au-plated Cu metallization.

4.5.2. Transfer-based process

For liquid polymers with NCA

Cu is not a biocompatible metal so a substrate as explained in section 4.5.1 is not desirable. A process where Cu is released from the structure was therefore designed, the flow-chart of this process can be found in figure 4.11. The patterning steps I through IV are identical to process steps IV through VIII described in section 4.5.1, though the material initially does not include polyimide (PI) and it negatively illuminated in lithography. These steps were an already existing process-flow in Fraunhofer IZM. In step V, Au is electroplated to the Cu carrier in a cyanidic Au bath (explained below), this Au will form the tracks of the copperless substrate. The PR is stripped (step VI) after which the chip will be flip-chipped onto the patterned Au using an NCA as an adhesive (VII). Next, the structure is coated with a liquid-form polymer (such as PI) that is then cured (step VIII) so that it can be released from the Cu using a $CuCl_2$ etching solution (step IX) in a custom etching setup (explained below). At this point, the prototype is in a state in which it can be electrically characterized. In the final step, the prototype is coated once more on the rear side with liquid-form polymer so that the structure is completely encapsulated in polymer.

The process was initially designed for PI but was only used for transfer to polycarbonate (PC) in this thesis. PC was used because it was available in the institute in liquid form and can have mechanical properties similar to PI.

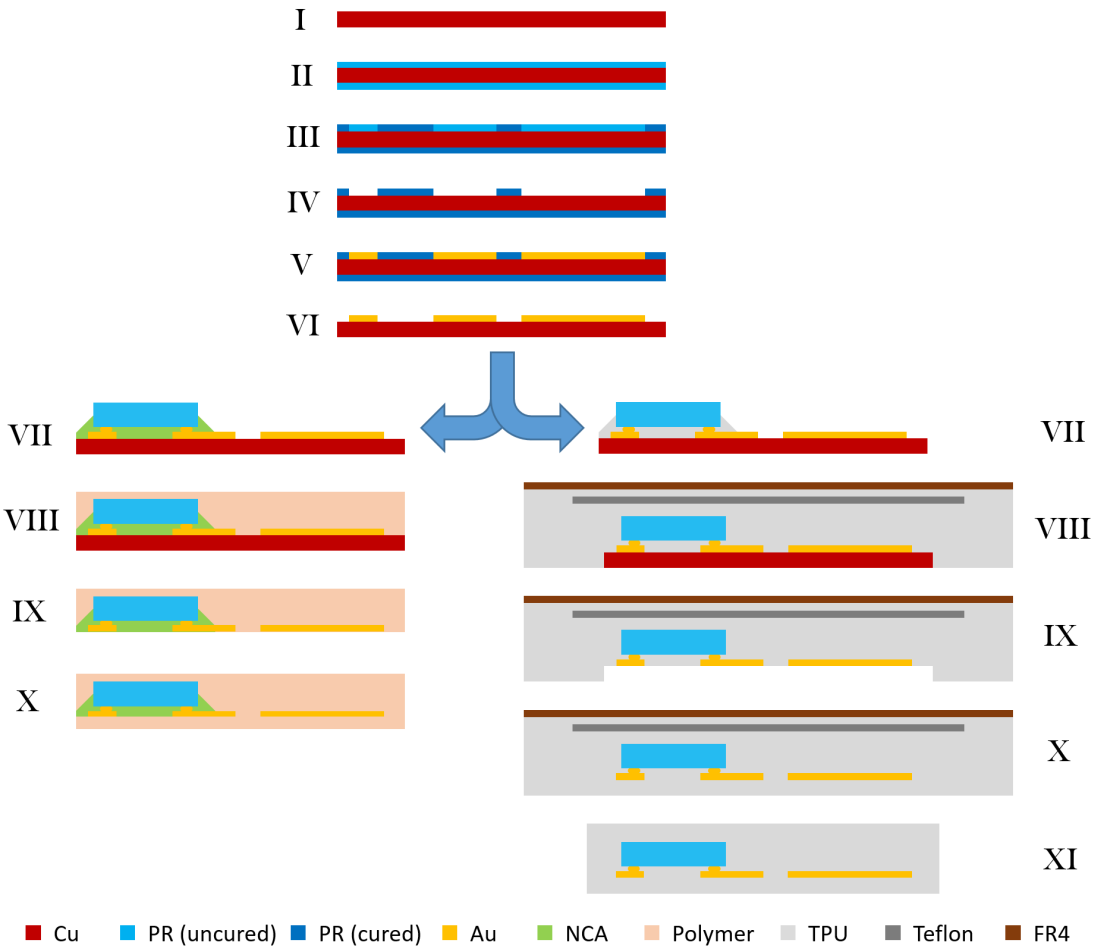


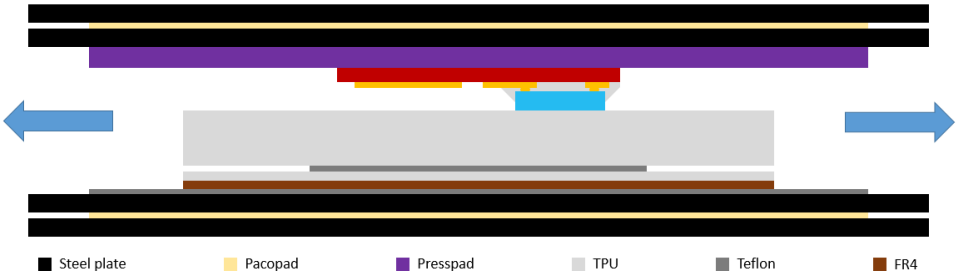
Figure 4.11: Process flow for manufacturing polymer substrates with an embedded flip-chip bonded chip on Au. Steps I through VI are common steps to pattern Au on Cu. From here it branches into two options: a flow for liquid polymers such as PC and PI (left) and a press-lamination flow for TPU (right).

For films of TPU without additional underfill

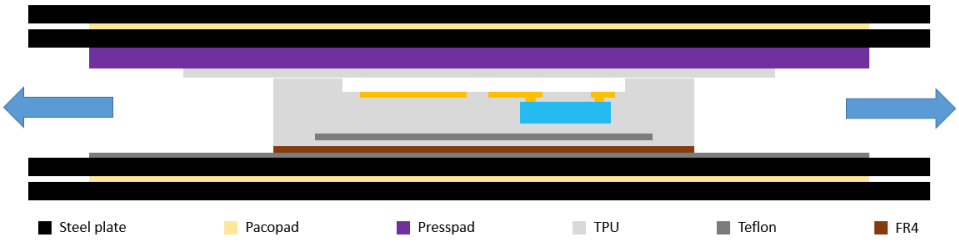
An alternative approach was developed for manufacturing with TPU as a polymer substrate. This approach was adapted from work by Pak et al [55] by including TPU as a chip underfill (improving overall adhesion and increasing implant lifetime by reducing material interfaces) and by including a FR-4 carrier as part of the transfer for rigidity purposes. In this process, steps I through VI are identical (see figure 4.11). By using TPU as an underfill during the flip-chip bonding process (step VII), the substrate can be made without forming an additional material interface (as explained in section 2.6). Due to the thermoplastic properties of TPU, the material can be laminated onto the Au-on-Cu assembly using the MP30-VK-S lamination press at about $180°C$ and $100N/cm^2$ (step VIII). The lamination process is done on a piece of FR-4, which is a glass-fiber reinforced rigid substrate material that subsequently makes the assembly easier to handle. A sheet of teflon is laminated in between the FR-4 and the rest of the assembly, acting as a release layer in the final step. To allow full release of the prototype structure, is important that the teflon sheet is under the complete structure. Teflon and FR-4 are both smooth surfaces, so a single sheet of TPU is added between the teflon and FR-4 to prevent the teflon from moving during lamination. In addition, the lamination process allows the TPU under the chip to remelt and lower mechanical tensions created during bonding, which has shown to reduce contact resistance on flip-chip bonds [35]. More details on the lamination can be found below. Cu is etched using a cupric chloride etching solution (step IX) in a custom etching setup (will be explained later) and

a second lamination step is done on the opened-up side at a slightly lower temperature (about 160°C) to prevent migration of components when the TPU melts (step X). Finally, the boundaries of the prototype are cut, releasing it from the FR-4 due to the teflon release layer (step XI).

Lamination stack and process The stacks for the 1st and 2nd lamination step (step VIII and step X, respectively) are shown in figure 4.12. The steel outer plates are pressed and heated by the lamination press while vacuum removes air to reduce void forming during the procedure. Pacopads by Pacothane Technologies are thin paper-like sheets that improve the alignment of the plates, ensuring a more uniform distribution of force. Presspads by Yamauchi Corporation are thicker, softer mats that smoothen out any non-uniformities in the sample. In this case, the mat mainly ensures that the thickest part, the chip, does not receive all the lamination force. Another teflon sheet ensures, together with the presspad, that the sample can be released from the steel plates after lamination.



(a) Stackup for first step of TPU lamination.



(b) Stackup for second step of TPU lamination.

Figure 4.12: Stackups for lamination of TPU. Vacuum is inicated with blue arrows.

Lamination is done in 6 steps. 1) the chamber is vacuumed to ~ $5mbar$. 2) the chamber is preheated to about 80°C at a rate of $4K/min$ and held at this temperature for 10 minutes, allowing the stack to set and dry. 3) the chamber is heated to the lamination temperature of ~ 180°C for the 1st lamination and ~ 160°C for the 2nd lamination (to prevent shifting of metallization on the already existing TPU layer) at an identical heating rate of $4K/min$. The temperature is held stable for 10 minutes to allow once more for setting and a uniform temperature. 4) When everything is heated up, the plates are pressurised to $100N/cm^2$. 5) After 5 minutes of pressure, the stack is cooled at about $4K/min$ while pressure is maintained to hold everything in place. 6) When everything has cooled down to about 40°C the chamber is re-pressurised and the stackup can be removed from the lamination press.

Common manufacturing topics

The transfer-based processes have two important steps in common that will be explained in more detail below: electroplating (step IV) and wet Cu etching (step IX). These processes will be explained in more detail below.

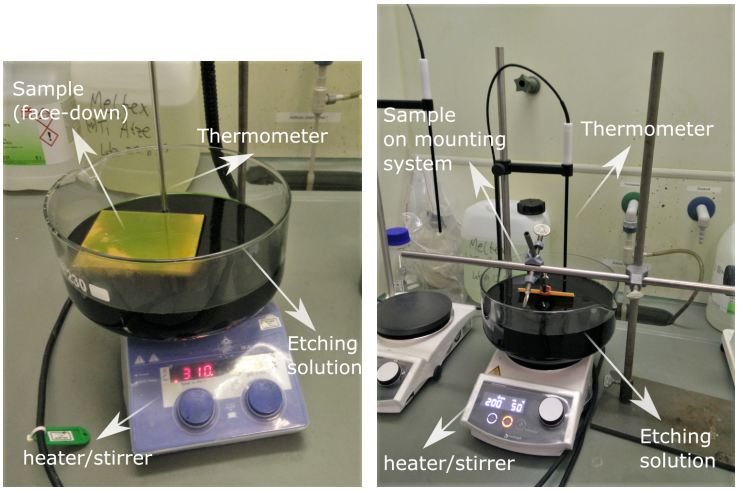
Wet etching of copper A couple of processes throughout this work use a Cu wet-etching solution. The working element in this solution is cupric chloride ($CuCl_2$) which reacts with Cu as follows:

$$CuCl_{2\,(aq)} + 2\,Cu_{(s)} \longrightarrow 2\,CuCl_{(aq)} \tag{4.15}$$

To replenish the lost Cl atom of the etchant, HCl is added to the solution. The remaining H+ atom is neutralized by adding H_2O_2 to the solution. The reaction therefore becomes as follows:

$$2\,CuCl_{(aq)} + 2\,HCl_{(aq)} + H_2O_{2\,(l)} \longrightarrow 2\,CuCl_{2\,(aq)} + 2\,H_2O_{(l)} \tag{4.16}$$

Cu etching is normally done in an automatic etching line where the etching solution is sprayed at roughly $50°C$ onto the substrate. Cu is etched in such an etching line at a rate of about 20 to $30\mu m/min$. However, in some cases this form of etching can be too harsh and a more gentle method is required. A custom setup was therefore devised for this thesis, using a heating plate with magnetic stirrer. This results in etching rates between 2 to $7\mu m/min$ depending on the exact setup. Figure 4.13 shows the two manual setups used throughout the thesis. Figure 4.13a is a setup used in initial prototyping work in which samples are not mounted and either floating or sinking in the etching solution depending on their density. Etching rates are in the order of $2\mu m/min$, requiring up to an hour of etching. Figure 4.13b shows an improved setup devised in a later phase of this work. Samples are fixated perpendicular to the etchant's flow direction, though tilted face-down at about 50° to allow for etchant flow accross the sample surface. This increases the etch rate to 5 to $7\mu m/min$.



(a) Custom manual Cu etching setup used in early prototypes.

(b) Modified manual Cu etching setup used in later prototypes.

Figure 4.13: Manual Cu etching setups.

Au electroplating of a Cu carrier Au electroplating is a manufacturing step commonly used throughout this work. The principle rests on a solution of Au ions, which are kept suspended with cyanidic ions. These positively charged ions can be solidified by injecting electrons in the solution, a process which can chemically be expressed as:

$$Au^{3+} + 3\,e \longrightarrow Au \tag{4.17}$$

A setup that is able to inject such charge can be found in figure 4.14. This setup takes advantage of the fact that the amount of injected electrons can be carefully regulated by controlling current and time following:

$$Q = I \times t \tag{4.18}$$

Where Q equals charge in Coulomb, I equals current in Ampères and t equals time in seconds. During electroplating the sample is connected to the cathode of the setup, attracting the positively charged Au ions that can solidify on the sample's negatively charged surface. The injected current spreads over the surface of the sample so should be corrected accordingly. Internal literature states that for a Puramet 202 cyanidic Au bath deposition rate is roughly $0.25\mu m/min$ when a current density of $3mA/cm^2$ is applied. The Au bath is kept at $60°C$ and a pH-value between 5.5 – 6.5 during plating.

When starting the electroplating of a sample, it is positioned in the cyanidic bath whilst using $\sim 1mA$ of cathodic saving current. This prevents the Cu from oxidising during positioning but does not start the electroplating. The electroplating current (in the order of $50mA$ for samples in this thesis) is applied only when the panel is fully submerged and properly positioned. After electroplating, the sample is rinsed in an acidic spray cleaning bath to neutralize the sample and finally, the sample is rinsed in DI water.

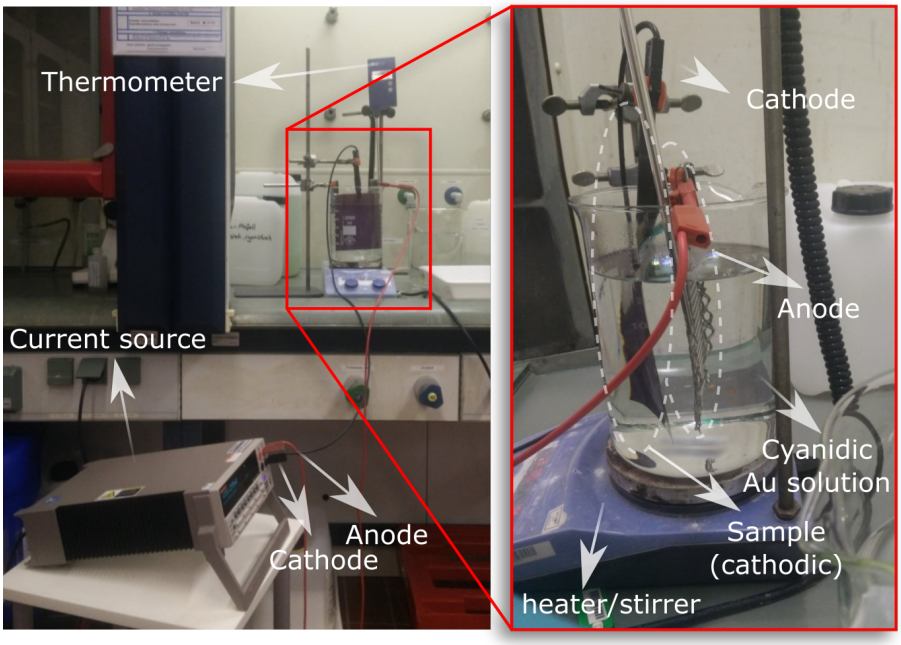


Figure 4.14: The cyanidic Au electroplating setup.

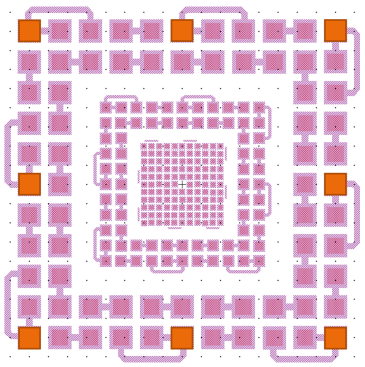
5

Results

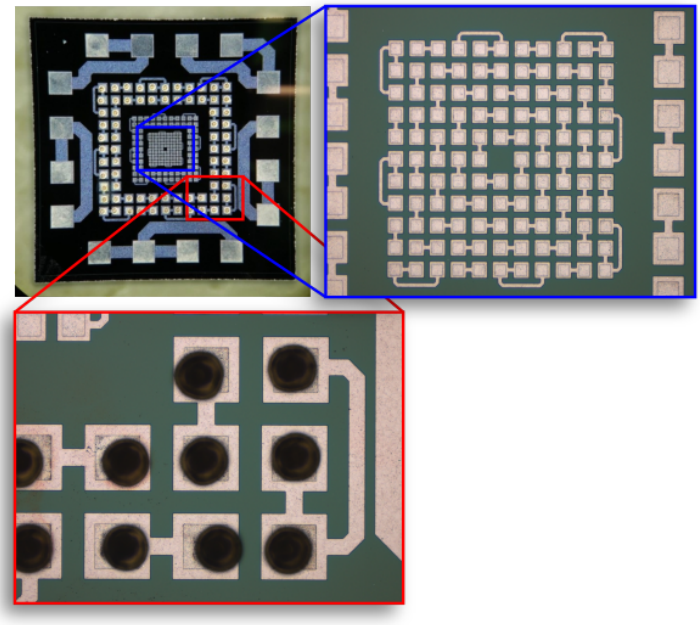
5.1. Iterating contact size

It was decided to work in iterations towards the desired configuration mentioned in introductory section 1.4 so verification could be done in an early stage of development. The first dummy chip was designed with the intent to explore the feasibility of various pad sizes. The chip is a dummy chip meaning that it has only functionality that allows to measure bonding quality in a way described in section 4.2. This, including the distribution of the pads (which is ring-shaped) meant that the middle of the chip remained unused. The middle was therefore filled with two scale-down designs, resulting in three designs on a single die:

- Outer ring: 72 pads, 80μm dimensions
- Middle ring: 72 pads, 40μm dimensions
- Inner grid: 120 pads, 20μm dimensions



(a) Design of the first chip. Light-pink marks internal tracks of the chip, dark-pink marks exposed connections (pads), orange squares mark all pads on the outer ring that can be probed with a 4-point measurement. The middle ring and inner grid have 4-point measurement connections on corresponding locations (not marked).



(b) Diced chip of first iteration with bumps on the outer ring. Note that the outermost 16 pads are part of an unrelated project that was merged in the design due to cost and time. Zoom-in figures show the bumped 8072 ring and the inner 20μm pad array.

Figure 5.1: Figures of the first chip iteration.

The result is a multifunctional dummy chip, where stud bumps can be placed on one of the three designs, effectively deactivating the functionality of the other two designs. Chip naming is according to which chip region is activated, so bumping the outer ring would dub the chip to '8072' as explained in section 4.2.3. The chip was made according to the manufacturing process described in section 4.3, figures of the chip can be found in figure 5.1. The optimiser script described in section 4.1 was not functional at the time of designing the first chip iteration so the center-center distance was chosen to be what is considered the industry standard: double the pad size. Note that the chip has rotational symmetry meaning that the orientation is irrelevant during the bonding process because the connections will be identical.

5.2. Cu-to-PI prototyping

Though not preferred due to compatibility, Cu was used as an initial metallization on PI. The advantage being that the process (as explained in section 4.5.1) is well established in Fraunhofer IZM and therefore an convenient entry-level prototyping platform. Manufacturing, assembly and electrical measurements will be explained in the following subsections.

5.2.1. Cu-to-PI substrate manufacturing

A substrate layout was designed in Altium to match with the outer ring of pads of the first chip iteration. The substrate is named according to naming conventions described in section 4.2.3: '8072 V2'. A render of the substrate can be found in figure 5.2. Note that the design was made on a single metallization layer so that manufacturing of vias was not needed.

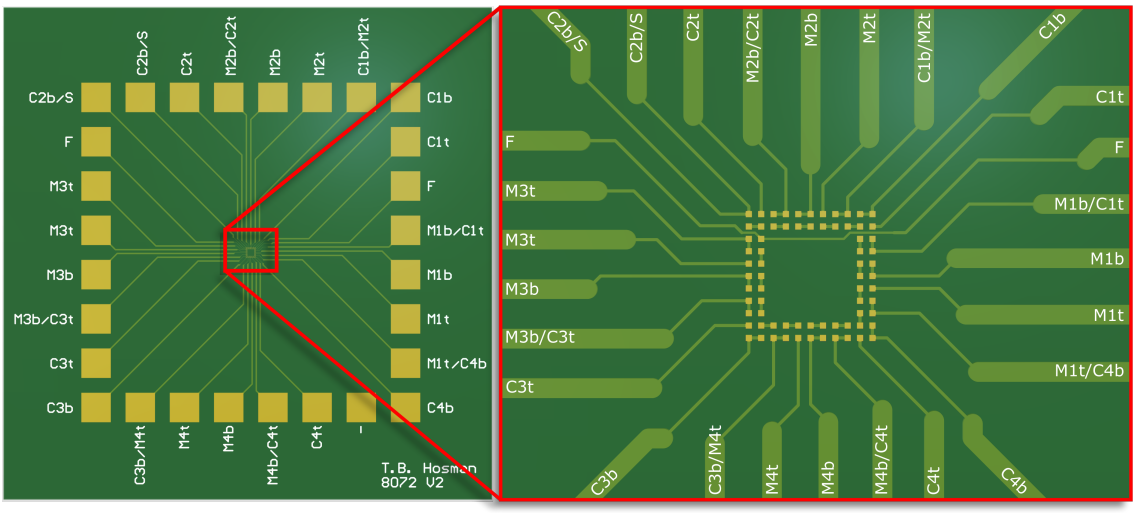


Figure 5.2: 8072 V2 render. On the left the full substrate, on the right a zoom-in of the bonding array. Track labeling is according to naming conventions described in section 4.2.3

As explained in chapter 2.6, the preferred metallization on the PI substrate is Au. However, a more convenient and significantly cheaper option as a first prototype and proof-of-concept was to produce a PI substrate with Cu metallization electroplated with Au. The procedure for such a substrate is explained in section 4.5.1. The copper tracks of four substrates were coated with immersion Au plating. The thickness averaged at $161nm$ over 30 measurements across the four samples, though readings varied between $72nm$ and $369nm$. Actual Cu thickness on the substrates was $15.52\mu m$ on average, deviating anywhere between $14.7\mu m$ and $17.0\mu m$. Full thickness details can be found in appendix C.

5.2.2. Cu-to-PI assembly

For the first assembly iteration, the outer ring of the chip in figure 5.1a was used. This ring of pads was manually bumped using a wire bonder able to place AuPd stud bumps roughly $80\mu m$ in diameter when using $25\mu m$ thick wire.

These bumped chips were then assembled with an NCA (Epotek 301-2FL) onto the polyimide substrate using the SET FC150 flip-chip bonder. The work by Wu et al. [64] was used as a starting point for the flip-chip bonding parameters. The polyimide substrate was fixed in the bonding machine by means of polyimide film tape. An NCA was manually applied to the bonding site after which the PI substrate was pre-cured at 90°C to lower epoxy viscosity, spreading it more evenly over the substrate surface and ideally removing air trapped inside the adhesive.

The chip is held by the bonding head through vacuum. Initially, tiny holes were inserted in a piece of teflon with a pair of sharp tweezers. The sheet was placed between the chip and the bonding head to prevent the NCA from contaminating the bonding head. The punctures allow vacuum to reach the chip behind the teflon sheet. However the non-uniformity caused by the punctures was already enough to break the chip during bonding so this method was omitted in the remaining three Cu-to-PI samples. Instead, extra care had to be taken into the amount of NCA applied to the substrate surface.

The bonder arm holds the chip in contact with the substrate surface during pre-curing to ensure a good contact with the heating element. Pre-heating was followed immediately by the full bonding pressure and temperature for final bonding and curing. The bonding profile can be found in figure 5.3. The temperature was applied via the substrate surface as well as the arm tool that holds the chip when pressure is applied.

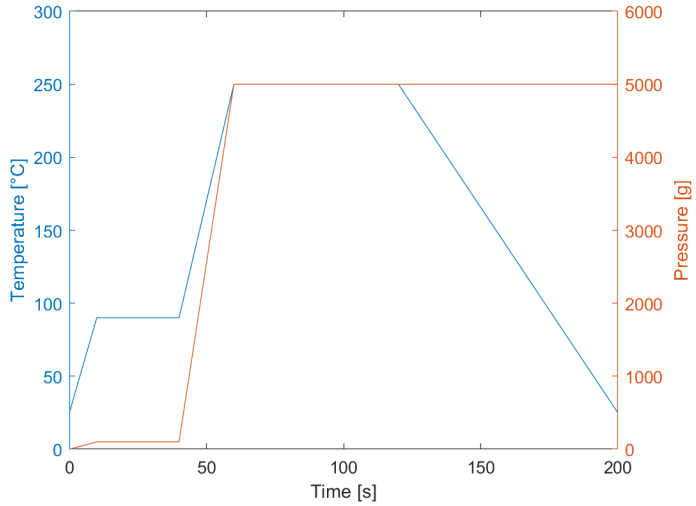


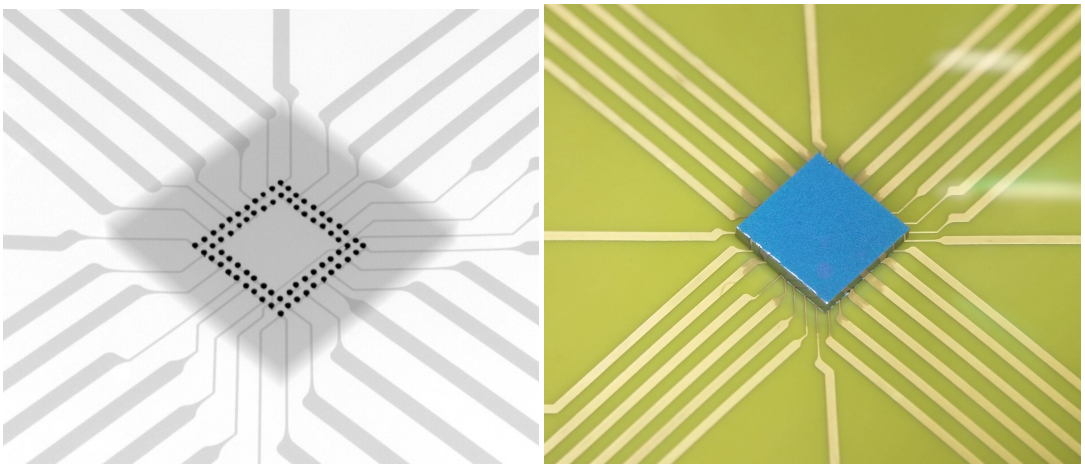
Figure 5.3: Bonding profile used for the chip assembly on the Au-plated Cu-to-PI substrates.

5.2.3. Cu-to-PI 4-point measurements

X-ray imaging and optical inspection of the prototypes (see figure 5.4) showed good alignment and bump shapes indicated that Au-Au bonding was successful. However, this was not reflected in the results of contact resistance measurements, mostly indicating open-loop (OL). Ultimately, it was discovered that the result of a flip-chip operation would also mirror the patterns compared to the face-up design of the chip. The substrate was unintentionally mirrored as a result. Coincidentally, there was a single 4-point measurement per assembly that remained measurable. With one chip broken during assembly (see previous section), this resulted in three 4-point measurements: 1.2$m\Omega$, 4.0$m\Omega$ and 1.9$m\Omega$. This indicates excellent contact (see section 4.2), though no accurate conclusions can be drawn due to the limited number of measurements.

5.3. Au-to-PI prototyping

As explained, Cu is not a biocompatible material and therefore not desired in an AIBM. This section covers an alternative approach with PI where Cu is etched away before completion of the prototype (as explained in section 4.5.2). Section 5.3.1 describes the Cu carrier manufacturing process and design considerations. This is followed by results of the flip-chip bonding and polymer transfer processes in sections 5.3.2 and 5.3.3, respectively.



(a) X-ray photo of 8072 bonding onto PI. Studs are reasonably aligned to the substrate, some studs still show tails of the uncoined studs.

(b) Optical photo of 8072 bonding onto PI. The epoxy has creeped to the surrounding gold tracks during preheating. The microscope shows some unintended glare in the top-right.

Figure 5.4: Pictures of the first 8072 assembly.

5.3.1. Au-to-PI carrier manufacturing

In contrast to the Cu-to-PI process, Au-to-PI process as explained in section 4.5.2 has the option for only a single metallization layer. This meant that the connections at the end of the daisy-chain (as explained in section 4.2) had to be routed between the pads to be able to connect to the outer measurement contacts, the so-called 'passthroughs'. Patterning at this resolution worked for the Cu-to-PI process but it was not known if this resolution could be reached for the Au-to-PI process, though it was likely because the same machines are used in both methodologies. The first steps of the Au-to-PI manufacturing process are the Au patterning steps on Cu. This was done on a Cu sheet of 105μm thickness. Microscope images in figure 5.5 show patterning results of the 8072 V3 design. The finest part of this structure is evidently the passthroughs, measuring at 30μm with 25μm spacing. Microscope images before Au plating showed that the LDI patterning was not a problem at this resolution (see figure 5.5a). The panel of 8072 V3 samples was cut into sets of 9 in a 3×3 grid to be electroplated. However, after Au plating and PR stripping, the passthroughs widened. Figure 5.5c shows a sample where the passthrough is only barely separated from the pads, while figure 5.5d even shows some shorts to the neighbouring contacts. The latter sample was most likely damaged because the polarity was accidentally initially set to negative during electroplating, causing the anode to be electroplated instead of the cathode (the sample) and possibly slightly damaging the photoresist.

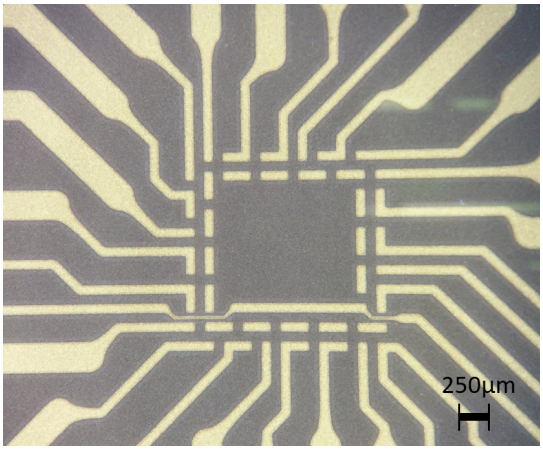
The first set of 9 samples was electroplated for 10 minutes, so the expected thickness of the Au was 2.5μm. In reality, the thickness was about 1.5μm on average. The thickness was measured at the outermost contact pads of the samples because they were the largest and thus easier to evaluate. In addition, it was non-uniform with the thinnest parts at the top of the solution (about 1.35μm) and the thickest at the bottom (about 2μm). Full results of this sample can be found in the left half of table 5.1. The second batch was clocked at roughly 12 minutes and was similarly lacking in thickness. These results can be found in the right half of table 5.1.

Table 5.1: Au plating thickness on 8072 V3 panel samples

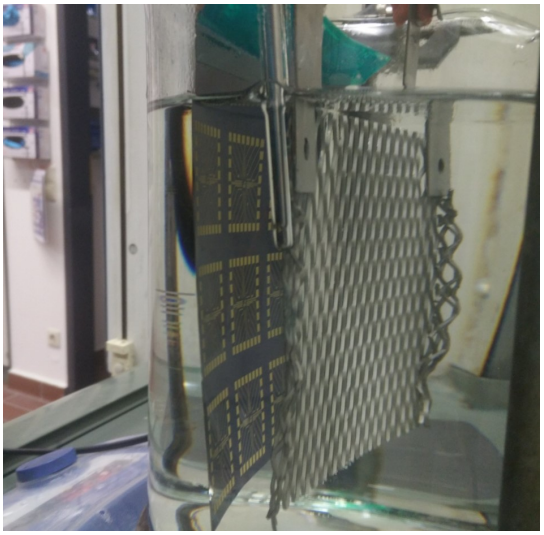
	8072 V3 panel sample 1			8072 V3 panel sample 2		
	Left	Center	Right	Left	Center	Right
Top	1.33μm	•	1.35μm	1.5μm	•	1.5μm
Middle	•	1.5μm	•	•	2.0μm	•
Bottom	2.0μm	•	1.68μm	2.5μm	•	2.0μm

5.3.2. Au-to-PI flip-chip bonding

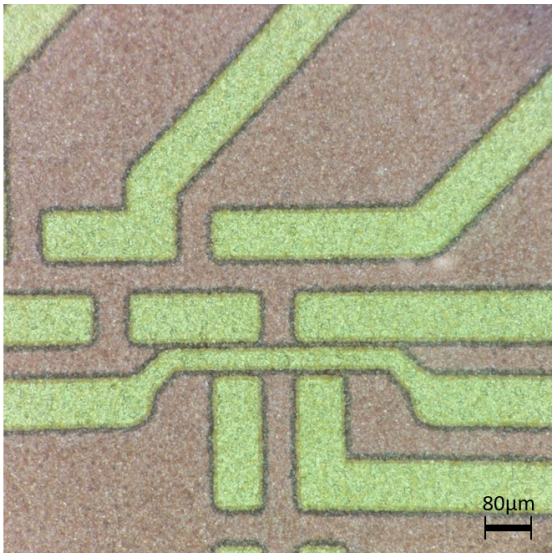
Samples in panel 2 were used in following steps while panel 1 was discarded because of the risk of shorts (see figure 5.5d). The chip bonding was done with a similar albeit different bonding profile than with the Cu-



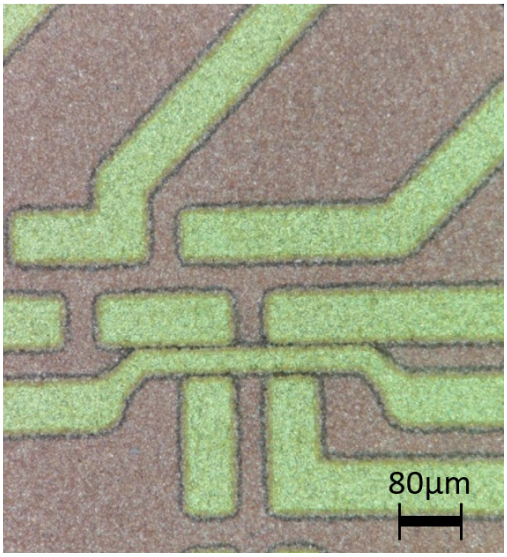
(a) 8072 V3 Cu carrier before Au plating. Passthrough pattern running between the bottom pads of the grid is clearly etched.



(b) Setup for cyanidic Au plating. The samples (left) are connected to the cathode while a grid (right) injects the current as an anode.



(c) Corner of 8072 V3 panel sample 2. The passthrough track is designed to be 30μm with 25μm spacing. Reality shows a barely seperated track.



(d) Corner of 8072 V3 panel sample 1. The passthrough track is designed to be 30μm with 25μm spacing. Reality shows that the tracks did not seperate.

Figure 5.5: Images of 8072 Cu carrier manufacturing.

to-PI prototype because work by Fretz proved to be more similar to the faced bonding problem, using only a different epoxy and substrate material [60]. The used bonding profile can be found in figure 5.6. Like the Cu-to-PI samples, epoxy was applied manually. Bonding data was logged and can be found in appendix D.1. After flip-chip bonding, X-ray imaging showed that there might be some voids inside of the epoxy. This was difficult to see however, since epoxy is hardly visible on X-ray. The epoxy is sandwiched between the Si chip and the Cu-Au carrier, so the only way to visually confirm voids was to transfer the material to a polymer and etch the Cu.

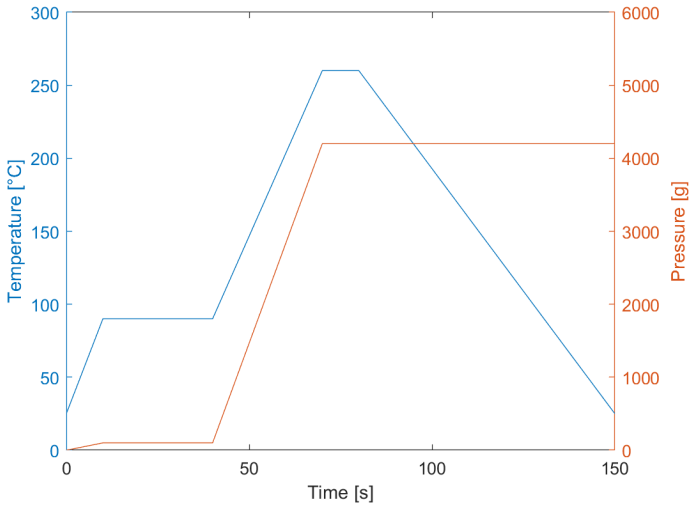


Figure 5.6: Bonding profile used for the 8072 Au-on-Cu assembly iteration.

5.3.3. Au-to-PI polymer transfer

The polymer of choice would have been PI, but for this first run PC was used instead because it was in stock within the institute. The Cu was pretreated with ethanol and plasma from the KINPen®IND from Neoplas GmbH to promote adhesion between PC and Au. A mask was cut by hand after which a liquid PC (unknown consistency) was applied. The PC was cured in approximately 60 minutes at $80°C$.

Three samples were made in total via this methodology. PC sample 1 was etched in the automatic Cu etching line but this was too harsh, delaminating some of the Au in the process. The remainders were etched manually at $50°C$, stirring the solution at $150rpm$ in the 'old' manual method as shown in figure 4.13a.

Figure 5.7 shows microscope images of a PC sample manufactured as described. Tracks remained connected for most of the structures though some parts were close to delamination. Chip alignment was good though connections were measured as OL or high impedance in the connected structure (2-point measurements). In addition, clear voids were present in the epoxy and the PC, though the latter was expected because no care was taken into degassing. Finally, some edges of Au tracks were surrounded by a haze of migrated Au particles.

Priority in the PC samples was to investigate why the chip was not conducting well with the outer ring of measurement contacts. For this purpose, a CT scan was done on PC sample 1. Some images can be found in 5.8. Figure 5.8a and (to a lesser extent) 5.8c shows clear connections between the Au bumps and the underlying tracks and no significant deformations due to flip-chip bonding pressure, indicating that the flip-chip process was not a likely cause for the lack of conductivity. Figure 5.8b showed unusual artifacts in the centermost contact grid (indicated with an arrow) and there seemed to be an aluminium contact in the outermost ring of which the part present in a void was gone (indicated with an arrow). The findings revealed that the voids in the epoxy unintentionally opened up room for the Cu etching chemicals to seep inside and etch away the Al contacts via the following chemical reaction:

$$2\,Al_{(s)} + 6\,HCl_{(aq)} \longrightarrow 2\,AlCl_{3\,(aq)} + 3\,H_{2\,(g)} \tag{5.1}$$

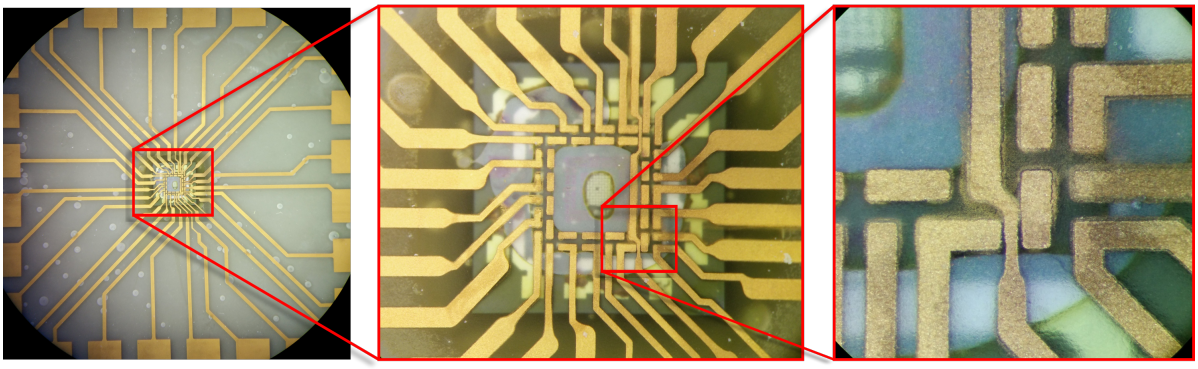
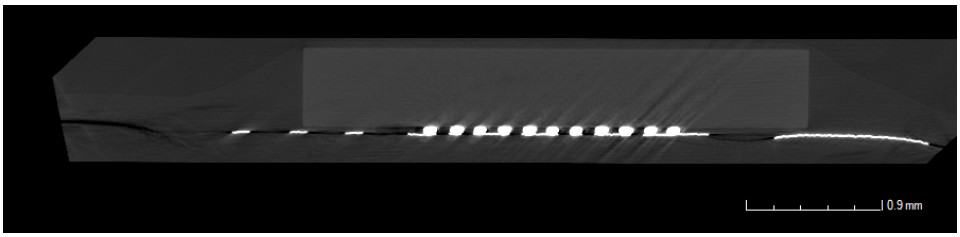
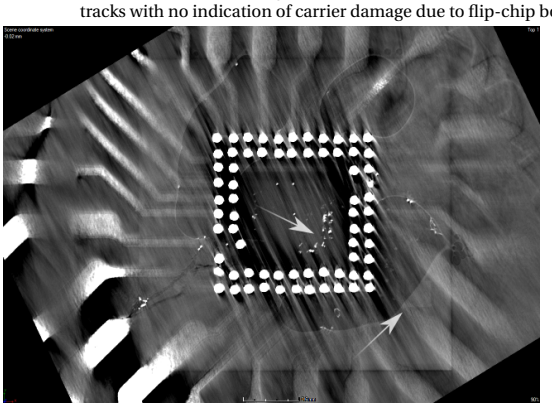


Figure 5.7: Microscope images of PC sample 2 using the Au-to-PI workflow.

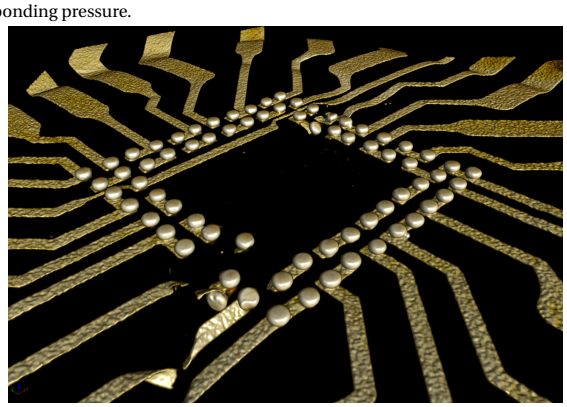
The findings were confirmed under the microscope. Looking at the second image in figure 5.7, one can see that Al contacts in and close to the voids show dark staining, indicating deterioration. It is likely to have caused low conductivity around the chip contacts.



(a) Cross-section CT image of 8072 sample on PC. Proper contact seems to be made between the stud bumps and the Au tracks with no indication of carrier damage due to flip-chip bonding pressure.



(b) Top-view CT image of 8072 sample on PC. White arrows show deterioration artefacts of Al chip contacts.



(c) Rendering of Au in 8072 sample on PC.

Figure 5.8: CT images of 8072 PC sample 1. An accidental diagonal cut damaged the contacts on two sides of this sample. Figure 5.8a and 5.8b show some artifacts due to reflections with Au.

5.4. Summary of findings for liquid polymer processes

This section will summarize findings of the curable liquid polymer processes described in sections 5.2 and 5.3 because following sections take a different approach to the problem whilst taking into account previous findings. The summary is divided in three sections: Cu etching, epoxy-based flip-chip bonding and PI as a substrate material. The first two topics reveal problems related mainly to the use of an NCA, while the last topic reveals problems inherent to PI.

Cu etching Cu etching is part of the Au-to-PI process that proved problematic on the chip surface and on the substrate surface. The Al on the chip surface deteriorates in contact with the etching solution so it is vital

for longevity that the Cu etching solution does not condense at the chip surface during etching. Main causes of etching solution condensation at the chip surface were voids in the NCA, as the chip surface remained seemingly untouched in areas where the NCA properly encapsulated the chip area.

As for the substrate surface, the Cu etching process is harsh and causes significant chances of delaminating Au from the transfer polymer. This is can be reduced by increasing adhesion between the two substrate materials. In addition, the etching rate in the manual Cu etching should be increased so the etching solution does not have time to creep deeper into the substrate material and deteriorate unintended regions. On the other hand, it should remain gentle enough as to not delaminate Au from the polymer.

NCA flip-chip bonding The epoxy-based flip-chip bonding was not quite working as intended, with main problems being voids (causing Al etching of the chip) and dispensing repeatability. The following process improvements were listed to improve bonding with the epoxy:

1. Use an automatic adhesive dispenser to improve repeatability and reduce formation of voids;
2. Purchase a fresh epoxy that has been degassed to reduce formation of voids;
3. Additionally degas epoxy before usage.

A more fundamental word of caution, however: epoxy adhesives cannot form chemical bonds with the surrounding polymer. This forms a material interface of which adhesion is currently unknown and that can cause failure in long-term implantation (as explained in section 2.6).

PI as a substrate PI was a valuable material in early prototypes described in section 5.2. However, the future prospects of PI were not so bright as initially thought. The state-of-the-art embedding technologies within the institute (as described in 2.3.4) turned out to be premature, expensive and highly specialized. Furthermore, and in contrast with what was previously thought, it currently not possible to metallize with Au in this process making it an unsuitable technique for future work. However most importantly: the inherent lack of elasticity for PI is a significant flaw when considering that the most likely implantation site is the Central Nervous System (CNS), consisting solely out of soft tissue. This makes the long-term implantability prospects dim for this work and its successors because the significant mechanical mismatch between CNS tissue and a PI implant can damage (and scar) surrounding tissue as well as damage the implant. This leaves PI with not a lot of advantages over other polymer materials, thus the question therefore arose if the choice for PI was the right choice for this work and the foreseeable future.

5.5. Au-to-TPU prototyping

The following sections step away from PI as a substrate because previous methodology was not as effective as was hoped (as explained in section 5.4) and other polymer materials could prove more valuable. Reflecting on the polymer evaluation described in section 2.6, TPU was considered as the most likely alternative mainly because of the thermoplastic interface merging capabilities, the options as an NCF adhesive and the available expertise/machinery within Fraunhofer IZM. In addition, TPU has a much higher elasticity compared to PI, making it more suitable for implantation in soft tissue such as the CNS. However, TPU is also a risk, because it melts at mild temperatures so high-temperature processes are unavailable once TPU becomes part of an assembly. For the purpose of this substrate material, the transfer process as used in section 5.3 was modified to accommodate for a lamination step as opposed to a polymer curing step. The TPU transfer process is explained in section 4.5.2.

5.5.1. Au-to-TPU flip-chip assembly

For the first trial assemblies of Au-to-TPU, leftover Cu carriers were used that were manufactured in section 5.3.1. TPU pieces - with footprint dimensions slightly bigger compared to the chip - were cut manually from a sheet of Platilon AU4201 by Covestro AG, to be used as a NCF for the flip-chip bonding process. A distance measurement in figure 5.8a revealed that spacing between the chip and the Cu sheet was approximately $40\mu m$ and so the NCF pieces were cut from a $50\mu m$ thick TPU sheet. This thickness should allow for enough material to underfill the chip completely but should also allow for close enough spacing to make successful contact during the flip-chip bonding process. The TPU pieces were cleaned with IPA and then dried for ~ 30 minutes

at 80°C to prevent formation of voids. A flip-chip bonding profile specifically for TPU was used because the material cannot handle temperatures used in previous flip-chip bonding attempts. Work by Foerster gave insight for the bonding profile found in figure 5.9 [35].

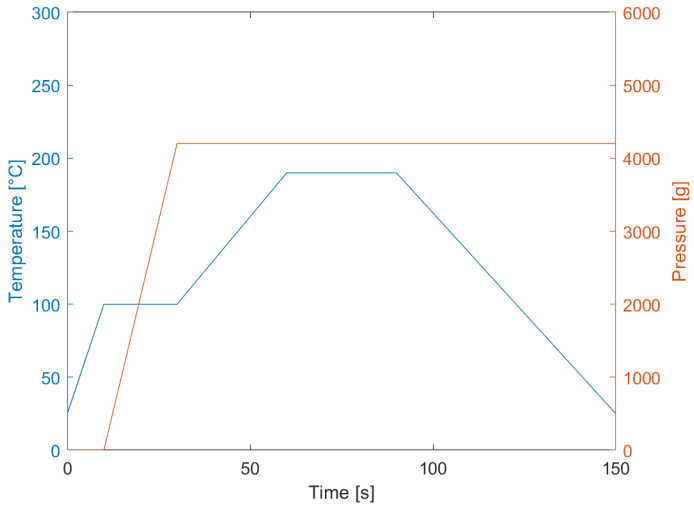
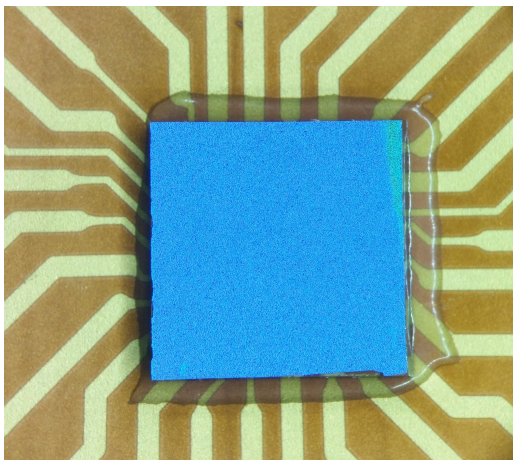
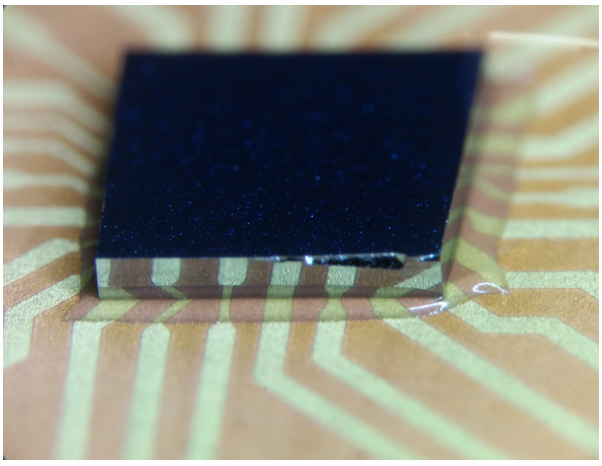


Figure 5.9: Bonding profile used for the Au-to-TPU assembly iteration.

A total of 6 samples were made with this methology. All of them showed results similar to that illustrated in figure 5.10. The TPU sheets seem to have underfilled the chip completely, though the area under the chip remains uncertain until after polymer transfer because X-ray was unable to detect TPU properly.



(a) Top-view microscope image of a flip-chip bonded 8072 chip with TPU as an NCF. The chip is completely surrounded by TPU suggesting that the chip is completely underfilled.



(b) Side-view Top-view microscope image of a flip-chip bonded 8072 chip with TPU as an NCF. The TPU has slightly lifted onto the side of the chip, suggesting that sufficient TPU material was present to underfill the chip.

Figure 5.10: Microscope images of a flip-chip bonded 8072 chip with TPU as an NCF.

5.5.2. Au-to-TPU polymer transfer

The assembly now has to be transferred according to the lamination steps described in figure 4.12a. To ensure that the lamination force is not all focused on the thickest part of the samples (the chip), the surrounding TPU material has to be thicker so it can evenly spread across the sample surface. The transfer stack therefore consisted of 7 TPU layers (each 100μm thick) of which one is placed below the teflon release layer and the rest is placed on top of it. Each sheet of TPU is individually cleaned with pressurised air and ethanol before stacking. Lamination was done with the profile found in figure 5.11.

Two samples were laminated successfully, showing no signs of voids, though some non-uniformity was observed around the chip's TPU surface of about 50μm. Cu was etched using the etching setup as seen in

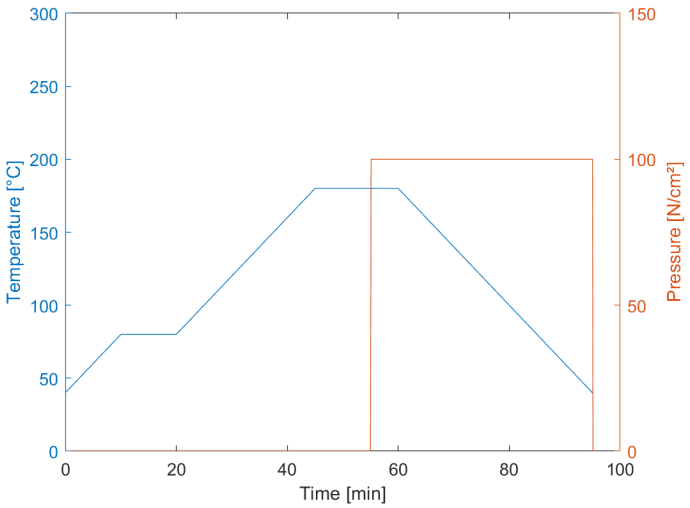


Figure 5.11: Initial lamination profile for transfer layer of TPU.

figure 4.13a for about 50 minutes at $300rpm$. These samples were cleaned for ~ 30 seconds in DI water directly after etching. 2-point measurements showed resistance measurements in the order of 2 to 3Ω through a single contact and about 12Ω for the daisy-chain, which is the expected range for a 2-point measurement. In addition, close-ups in the right part of figure 5.12 showed that the passthroughs had not made contact with the surrounding contacts. Nonetheless, a 4-point measurement was attempted 2 days later and resulted OL and high-impedance contacts. Microscope images seen in figure 5.12 were in fact made on that very day and showed that the Cu etching solution had once again seeped through to the TPU and deteriorated the Al contacts. It became clear that it was not just the large voids that allowed for the Cu etching solution to reach to the chip surface.

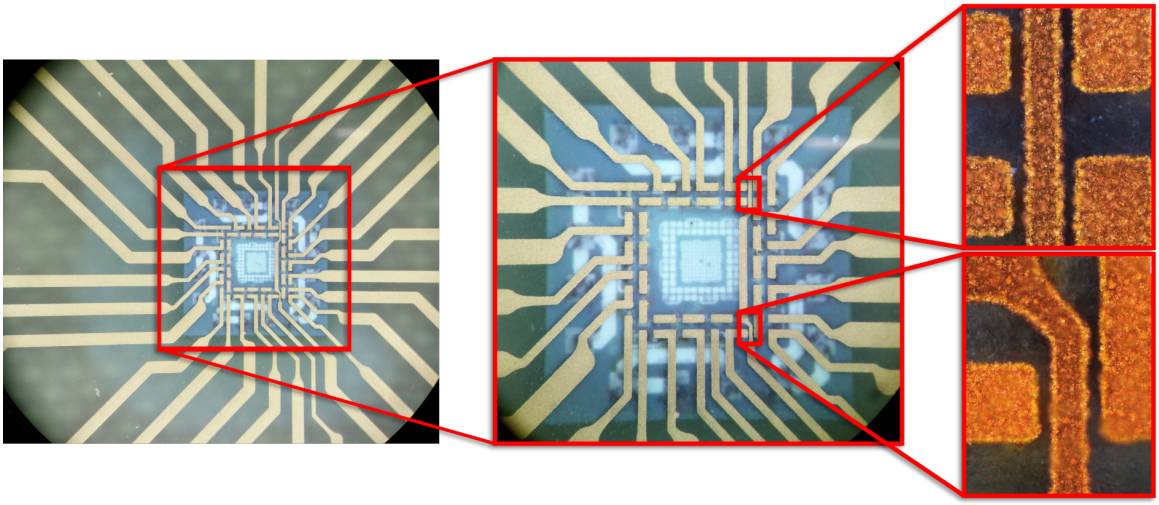


Figure 5.12: Microscope image of a 8072 sample with TPU as NCF & substrate after Cu etching.

The remaining 4 samples were used to conduct further investigation into reducing chip deterioration. One Au-to-TPU sample was etched in the automatic etching line because adhesion between Au and TPU seemed adequate, showing no significant delamination. However, some flakes of Au tracks were washed away, especially the thin tracks in the center of the structure (at the chip bonding site). To improve the etching in the manual etching method instead, a clamping mechanism and higher stirring rates (up to $350rpm$) were used to increase the flow and turbulence of the Cu etching solution around the Cu surface of the samples. This reduced the etching time from 50 minutes to about 15 to 25 minutes without any apparent damage or

delamination to the Au tracks. In addition, samples were cleaned more thoroughly: 1 minute in a bath of IPA followed by 5 minutes of ultrasound cleaning in a 45°C DI bath.

5.5.3. Au-to-TPU resistance measurements

Three remaining samples were etched and cleaned in a similar manner, with etching times of 21, 26 and 18 minutes respectively for the samples labelled 4, 5 and 7. Resistance measurements showed mostly OL and high resistance measurements for sample 5 and 7, with no apparent indication as to why that was the case. However, sample 4 showed good results that can be found in figure 5.13. The first bar in each of the plots shows the resistance measured shortly after Cu etching. The remaining 4 bars were measurements all conducted 72 hours later to measure if any Cu etching solution was still present. The measurement was done 4 times in the slightly different configurations as discussed in 4.2.1 to rule out geometry variations. Interestingly, the corner measurements C1-C4 slightly *increased* or remained the same, while the middle measurements slightly M1-M4 *decreased* or remained the same.

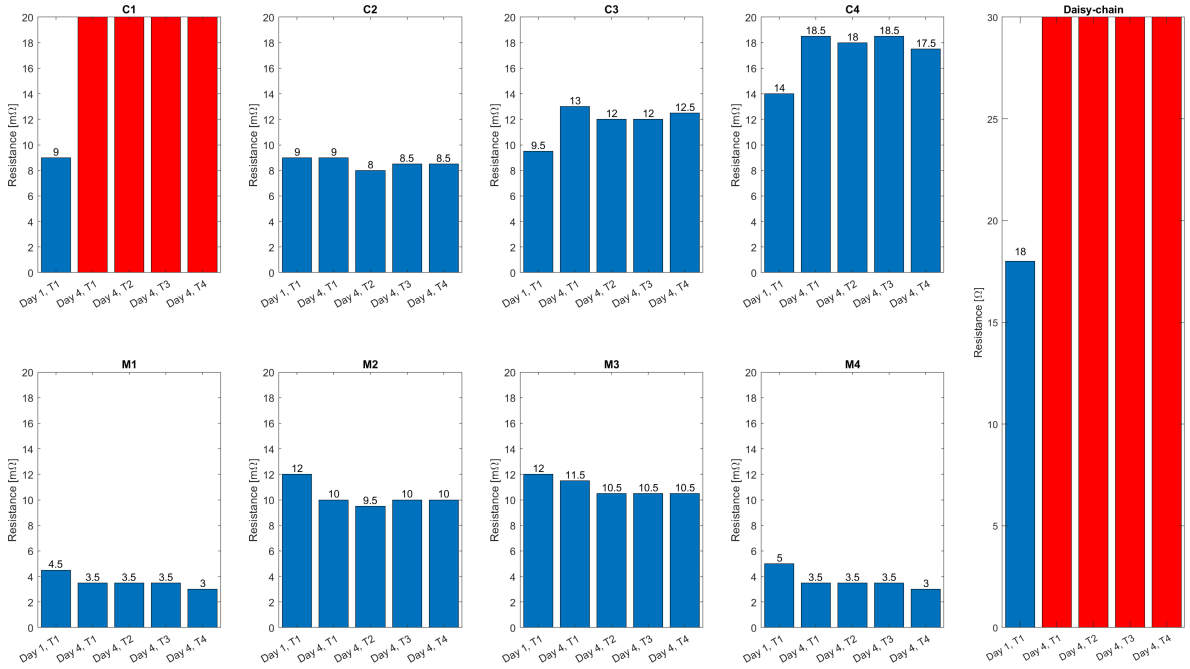


Figure 5.13: 4-point resistance measurement results of TPU sample 4 in 8072 configuration. Measurements were repeated on 2 different days with 3 days in between. Each connection can be measured in 4 slightly different configurations so the day 4 measurement was done 4 times to see its significance. Plots titled 'C' indicate 4-point contact resistance measurements at the corner of the chip, plots titled 'M' indicate 4-point contact resistance measurements of a center-edge contact. Bars in red indicate >100Ω was measured.

Based on the measured daisy-chain value during day 1, one can estimate the average resistance of the bonds. The daisy-chain runs through 64 of 72 flip-chip contacts, but dividing the measured 18Ω over 64 would include all interconnect tracks within the chain. To roughly compensate for that, the resistance of these interconnects was estimated:

$$R_{chip,short} = N \times \rho_{Al} \frac{\ell_{short}}{A_{chip}} \approx 23 \times 26.5[n\Omega/m] \times \frac{60[\mu m]}{1475[nm] \times 40[\mu m]} = 0.62[\Omega] \tag{5.2}$$

$$R_{chip,long} = N \times \rho_{Al} \frac{\ell_{long}}{A_{chip}} \approx 8 \times 26.5[n\Omega/m] \times \frac{240[\mu m]}{1475[nm] \times 40[\mu m]} = 0.86[\Omega] \tag{5.3}$$

$R_{chip,short}$ indicates the resistance of direct connections between chip pads, $R_{chip,short}$ the resistance of the longer bypass chip connections around 4-point measurement sites, ρ_{Al} the electrical resistivity of Al, ℓ the length of the track to calculate and A_{chip} the diameter of said track. Similarly, for Au connections in the substrate, we can calculate:

$$R_{substrate,short} = N \times \rho_{Au} \frac{\ell_{short}}{A_{substrate}} \approx 31 \times 22.14[n\Omega/m] \times \frac{60[\mu m]}{2[\mu m] \times 80[\mu m]} = 0.3[\Omega] \tag{5.4}$$

With parameters being similar to previous calculations. However, especially for Au the actual resistivity is possibly higher because the Au is to some degree porous. To estimate this effect, four Au-plated tracks $\sim 250\mu m$ in width and $2cm$ long were measured for resistance on the same substrate. The average equivalent electrical resistivity for these tracks of Au was:

$$\rho_{Au,eq} = \overline{R_{track}} \times \frac{A_{substrate}}{\ell_{track}} \approx 2.0 \times \frac{2[\mu m] \times 250[\mu m]}{2[cm]} = 50[n\Omega/m] \tag{5.5}$$

Where $\overline{R_{track}}$ indicates the average resistance of the four measured tracks. From this, one can conclude that substrate Au track resistances are roughly double the resistance compared to solid Au. Finally, subtracting estimations (including a correction for the Au porosity) and dividing over the number of contacts reveals:

$$R_{contact,avg} = \frac{R_{daisy} - R_{chip,short} - R_{chip,long} - \frac{\rho_{Au,eq}}{\rho_{Au}} * R_{substrate,short}}{N_{daisy}} \tag{5.6}$$

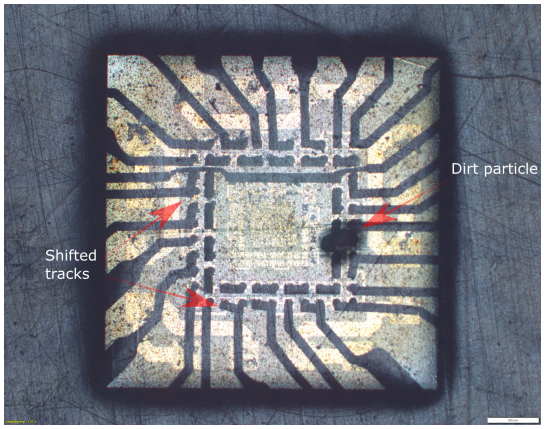
$$= \frac{18[\Omega] - 0.62[\Omega] - 0.86[\Omega] - 2.1 * 0.3[\Omega]}{64} \approx 0.25[\Omega] \tag{5.7}$$

This value is significantly higher than that measured in figure 5.13, indicating that there are inconsistencies in either contacts or substrate tracks.

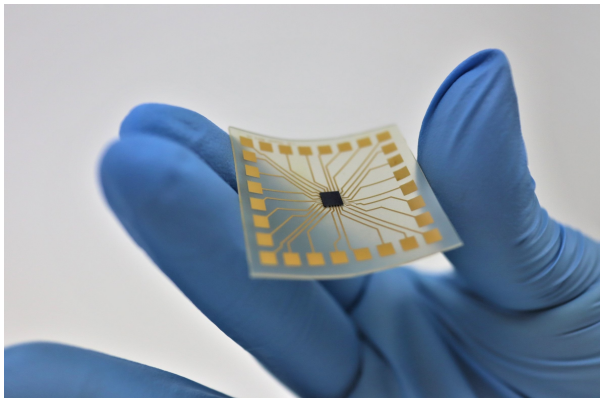
5.5.4. Au-to-TPU embedding

The final step for the Au-to-TPU process with 8072 chips was the embedding process, which involves a second step of TPU lamination as seen in figure 4.12b. The embedding was done with a single layer of $100\mu m$ thick TPU, making the total sample roughly $800\mu m$ thick. Similarly to the first lamination step, the TPU sheet is cleaned with pressurised air and ethanol. In addition, it turned out vital that the sample itself is thoroughly cleaned and was etched sufficiently quick in the Cu etching process (less than ~ 25 minutes). Samples that do not qualify develop a uneven coffee stain-like tinge. After embedding, a high-contrast microscope image was made of the samples, one of which can be seen in figure 5.14a. The figure shows that the contacts connected to the measurement tracks have been pulled towards the edges of the chip. This pulling force is most likely the result of a strain on the tracks caused by the slightly non-uniform surface of the TPU surrounding the chip which is forcing the TPU to shift towards the edges to achieve uniformity during the embedding operation. In addition, the high contrast of the image reveals plenty of contaminative dust and in the case of figure 5.14a: a dirt or sand particle. This is a result of the fact that the lamination process is not performed in a cleanroom.

A second, cleaner sample was embedded in a similar manner. A picture of this sample can be found in figure 5.14b.



(a) High-contrast image of an embedded 8072 TPU sample. The image shows a shift of Au tracks towards the edges of the chip that occurred during the 2nd lamination press. This is most likely due to strain on the tracks caused by the substrate non-uniformity as result of the thickness of the chip. The image also shows plenty of dust contamination and even a particle of what looks like sand (the latter was not observed in other samples).



(b) Picture of a fully embedded 8072 TPU sample.

Figure 5.14: 8072 TPU sample pictures.

5.6. Increasing number of contacts in second chip iteration

Assessing the first chip iteration as described in section 5.1 revealed that it was reaching the end of its purpose. The inner-ring 20μm contacts are simply too small for stud bumping and the middle-ring 40μm contacts need to be bumped with automated tooling that is expensive to operate. Therefore, a new chip iteration with more contacts was imminent. The stud bumps as manufactured in the first iteration were manually placed and come with significant height and placement inconsistencies visible throughout X-ray images of various flip-chipped samples, though exact deviations were never measured. Section 2.4.1 has shown that height inconsistencies reduce lifetime and X-ray images have revealed microcracking in the thin Au tracks most likely formed during the increased mechanical stresses of non-uniform flip-chip bonding (see figure 5.15).

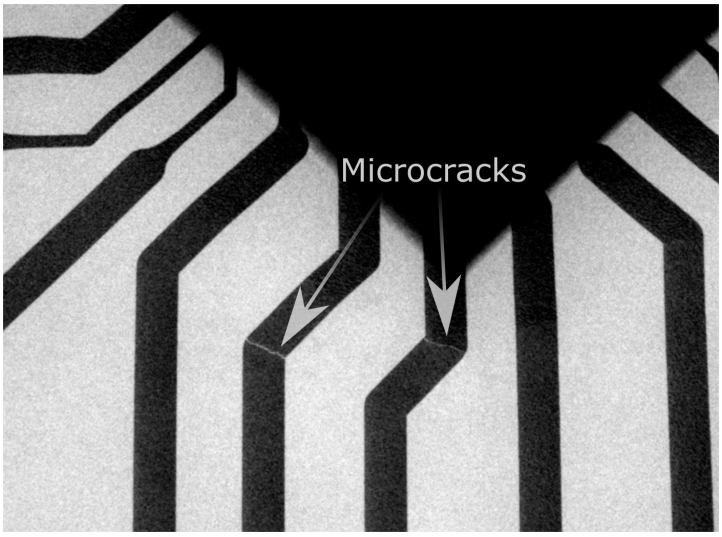


Figure 5.15: X-ray image of microcracks showing after flip-chip bonding.

A more repeatable and more reliable Au bump contact was therefore desired. With Au stud bump diameter limits around 36μm (see 2.4.1) this was decided as a reasonable contact dimension. A total of roughly 1000 contacts was considered a reasonable step-up in the iteration process. The distribution of the contacts was designed based on the results of the optimiser script described in section 4.1. Substrate parameters were taken from the literature described in section 2.3.4 (conclusions from section 5.4 were not yet drawn) and 2 metallization layers were given as a limit. The optimiser output for these parameters is a distribution of 1008 contacts over 7 rows with center-center spacing at 71μm, 3 of which should be routed on the top metallization layer and 4 of which should be routed on the layer below. However, with the aim of 10.000 contacts and 4 metallization layers the optimiser script was also run for this amount (as described in section 5.10), revealing 80μm center-center spacing for that specific configuration. The center-center spacing of the appropriately named '361008' chip was therefore slightly widened to 80μm. Nonetheless, the resulting chip design has a unheard-of connectivity density more than four times higher compared to existing neurostimulating systems (see section 2.2).

Two 4-inch wafers were manufactured according to the method described in section 4.3. The first wafer was 500μm in thickness, making it the same as the wafer used to produce the 8072 chips. The second wafer was thinned down to 300μm with the reason being twofold: 1) allow for potentially thinner assemblies, and 2) reduce height to prevent shifting during lamination (as was observed in section 5.5.4). It was decided that the contacts of this chip are to be electroplated instead of stud bumped, because:

- Electroplating allows for further bump miniaturization in future work;
- Electroplating is more scalable, stud bumping can only be done stud-by-stud;
- Electroplated bumps can be made thin easier than stud bumps.

The only downside being that electroplated flip-chip bonding requires more force and/or temperature because the bumps have an increased hardness, as also seen in figure 2.3. The electroplated bumps were

manufactured according to specifications as found in figure 4.8b. Pictures of the 361008 chip including electroplated bumps can be found in figure 5.16. Note that according to this picture, the electroplated bumps are roughly $60 \times 60 \mu m^2$ which is significantly wider than the $50 \times 50 \mu m^2$ as explained in figure 4.3. The difference was the result of manufacturing margins that were not clearly revealed by the electroplating manufacturer beforehand.

The increased dimensions of the contacts was not accounted for in the optimisation of the contact array. With roughly $20 \mu m$ of spacing between the contacts instead of the designed $44 \mu m$, it leaves room for only 1 passthrough connection instead of the 2 passthrough connections that it was designed for (if the chosen technology parameters remain the same). In this case, the top layer can only route 2 contact rows, netting a total of 6 rows of connections instead of 7. Therefore, the innermost row of contacts, consisting of 120 connections in total, remains initially unroutable.

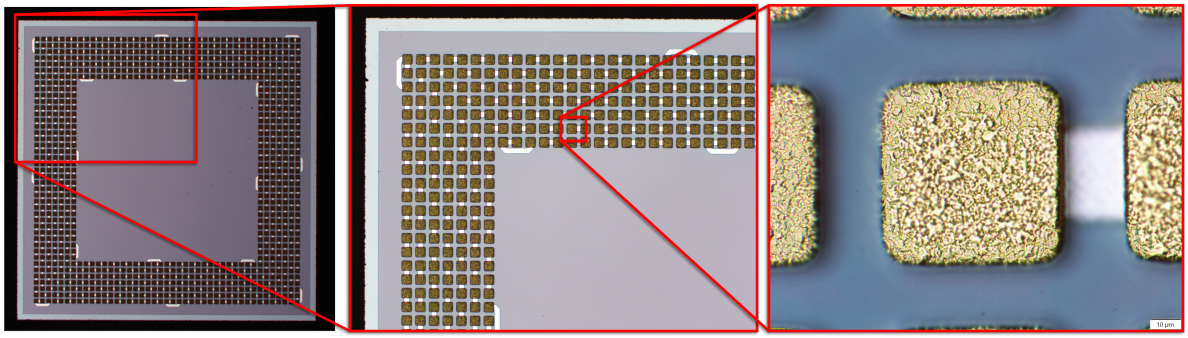


Figure 5.16: 361008 chip with electroplated bumps.

5.7. High-density Au-to-TPU prototyping

This section continues the researched technology as described in section 5.5 and lifts it to a routing technology with higher density using the second chip iteration as described in section 5.1. Section 5.7.1 will describe the design and manufacturing considerations of the Cu carrier. Section 5.7.2 describes the assembly process, including flip-chip bonding, lamination and etching processes. Concluding 5.7.3 will evaluate on the resistance measurements of the manufactured prototype samples.

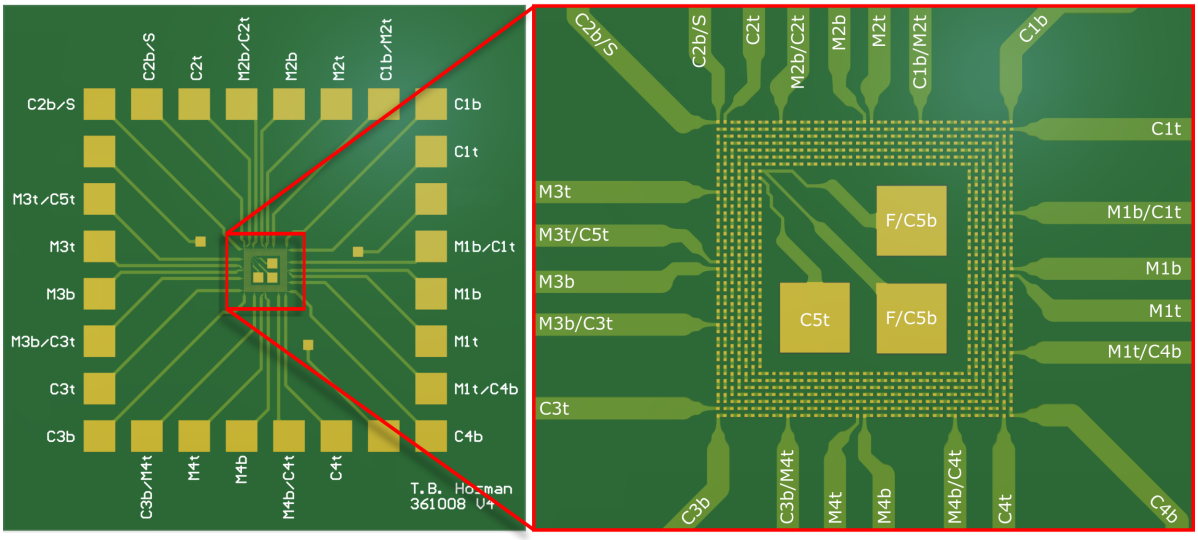


Figure 5.17: 361008 V4 substrate render. On the left the full substrate, on the right a zoom-in of the bonding array. Track labeling is according to naming conventions described in section 4.2.3.

5.7.1. HD Au-to-TPU carrier manufacturing

A measurement circuit similar to the 8072 substrate design as described in section 5.2.1 was developed in Altium to facilitate the 361008 chip. A design render can be found in figure 5.17. The outer ring of measurement pads remains largely identical in terms of layout. However, there was insufficient room to route the 'F' contacts from the innermost part of the chip to the outermost part of the substrate. Therefore, measurement contacts *inside* the unused middle region of the chip were placed. Conveniently, an additional third contact could be added that allows for the measuring of 'C5', which is the last contact in the daisy-chain on the innermost ring of the contact array. In addition, the measurement tracks were widened as much as possible to reduce the risk of cracking during the assembly process.

The design was processed according to the manufacturing steps I through VI as described in section 4.5.2 on a Cu carrier of $105\mu m$ thick. Before electroplating, two panels were cut in pieces containing 9 samples each (distributed 3 by 3). The thickness of Au was measured for both samples on multiple locations to measure Au uniformity across the panels. The results of this can be found in table 5.2. Images of the Cu carrier were made after PR stripping to validate that the desired Au pattern resolution was reached, the results can be found in figure 5.18. Apart from some inconsistencies that should be taken into account during electrical characterization, no significant issues were observed in the Au-to-Cu carrier substrates.

Table 5.2: Au plating thickness on 361008 V4 panel samples

	361008 V4 panel sample 1			361008 V4 panel sample 2		
	Left	Center	Right	Left	Center	Right
Top	$1.8\mu m$	•	$2.5\mu m$	$2.0\mu m$	•	$2.2\mu m$
Middle	$2.5\mu m$	$2.6\mu m$	•	•	$2.6\mu m$	•
Bottom	$3.3\mu m$	•	$2.5\mu m$	$2.9\mu m$	•	$2.8\mu m$

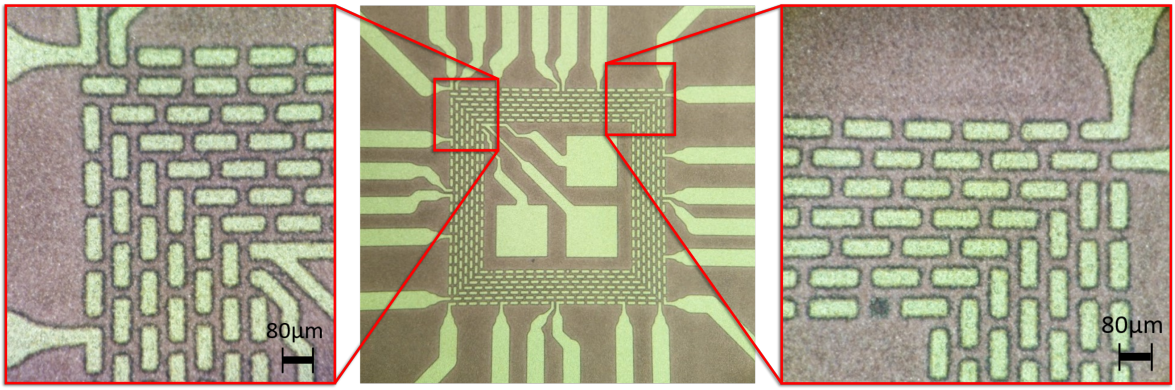


Figure 5.18: 361008 V4 Au-to-Cu carrier images. Patterning resolution is sufficient though incidentally single $36 \times 36\mu m^2$ pads released (right figure). The 'C5t' connection in the bottom right of the left picture is barely separated from the adjacent contact.

5.7.2. HD Au-to-TPU flip-chip assembly

The flip-chip bonding procedure was initially done similarly to what was described in section 5.5.1 for the 8072 chip, scaling only the pressure relative to the contact size and number of contacts. Assuming 1008 contacts each with $36 \times 36\mu m^2$ of surface area and applying $180MPa$ according to Foerster [35] resulted in approximately $180MPa \times (0.036\mu m)^2 \times 1008 \approx 24kg$ of maximum bonding force. Note that the bonding pressure of $180MPa$ is about half of what can be found in figure 2.3 because approximately half of the contact forms a bond [35]. Initial bonding was therefore done according to the profile found in figure 5.19.

The first set of 361008 samples was made with this bonding profile. The first two were made with the $500\mu m$ thick chip and although electrical measurements could not yet be conducted, X-ray images showed that the alignment was good (see figure 5.20a). The samples were transferred via lamination to 7 layers of $100\mu m$ thick TPU, however components had started to shift in this process and the chip was no longer aligned (see figure 5.20b). Luckily, there was still a 2-point measurement connection that could be measured to verify that contact is made between the chip and the tracks: the center lines at the bottom of the chip in figure

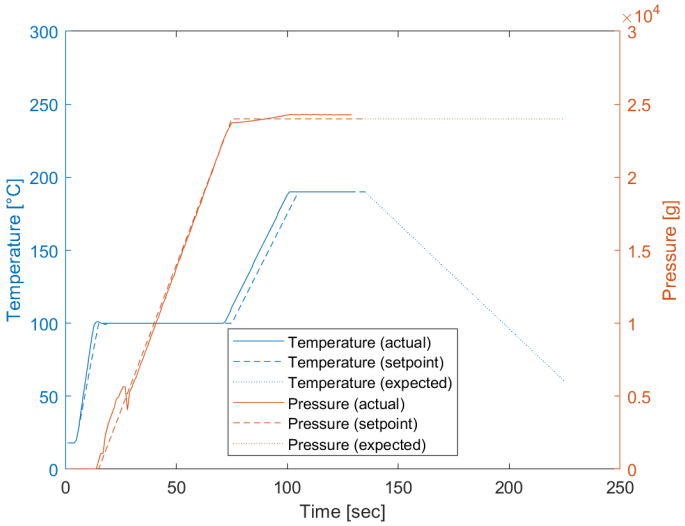
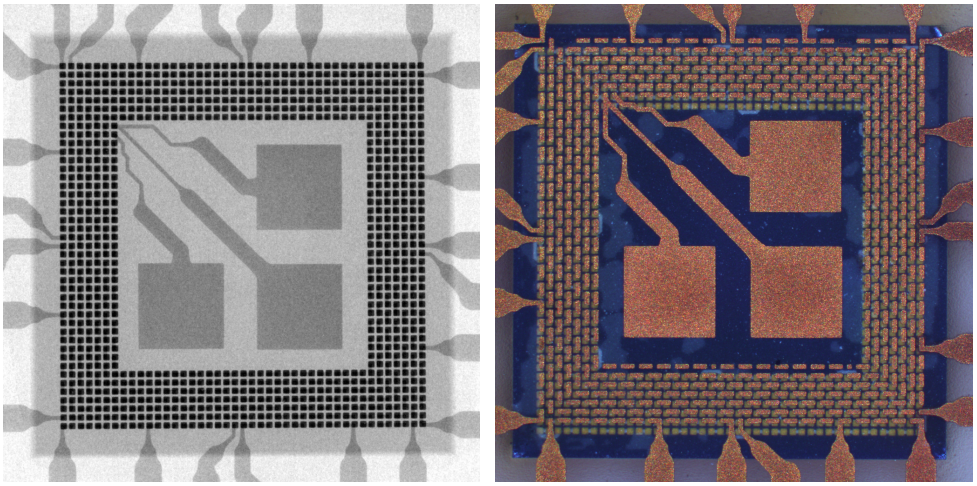


Figure 5.19: Initial bonding profile used for the 361008 Au-to-TPU assembly iteration. Setpoint values indicate all parameters explicitly set in the bonder, expected values indicate how the parameters are expected to hold after bonding has strictly ended and monitoring data stops. Actual data is taken of sample #7 and shows a dip at $5kg$ of force due to a switching error between the low-force ($< 5kg$) and high-force ($5-100kg$) sensor, this happens by default in this model in high-force applications.

5.20b are connected via a single connection within the chip. With this coincidental contact measuring at 1.3Ω, bonding seemed to be successful. Bonding data of these samples can be found in figure D.4 and D.5 in appendix D.2.



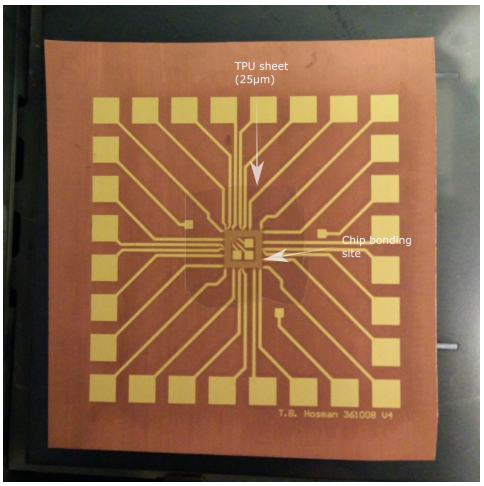
(a) X-ray image of the first 361008 sample. The alignment between the tracks and the chip seem good enough for the first measurements. The 'C5t' contact close to the end of the daisy-chain is possibly shorted to the preceding contact.

(b) Microscope image of the first 361008 sample. The alignment had shifted during the first lamination step to TPU, rendering the electrical measurement structures useless. The chip passivation is showing some delamination to the TPU (multiple spots on chip area).

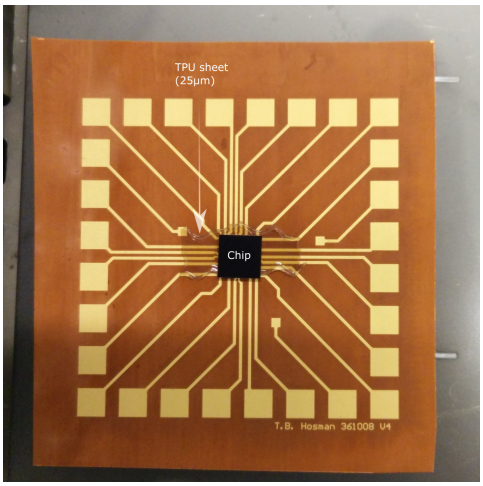
Figure 5.20: Pictures of the first 361008 sample. The chip alignment was initially good but has shifted during the first lamination step.

Unfortunately, successive flip-chip bonding experiments, conducted with thinner $300\mu m$ thick chips, did not turn out as the first two samples. Rather, they all showed significant shrinkage of the TPU sheet in a single direction and most samples did not have the bonding area completely covered with TPU after bonding. The difference before and after bonding can be found in figure 5.21a and 5.21b respectively. Similar behaviour was observed when bonding with the $500\mu m$ chips. Bonding data of these samples (both chip thicknesses) can be found in figure D.6 through D.12 in appendix D.2. Careful inspection of the samples revealed that the TPU had retracted into a thick band underneath most of the chips, as can be seen in figure 5.21c. Furthermore, samples gave the impression that TC bonding had been unsuccessful for each of these samples because the chips were

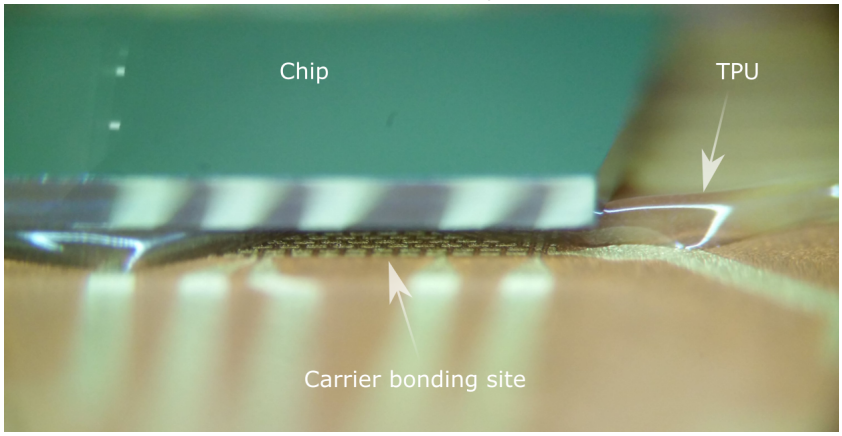
removable and showed no sign of bonding pressure on individual contacts. It indicated that bonding force should be increased to facilitate a proper TC bond. In addition, the hypothesis was that the TPU was most likely still melted when the bonding head released. With hardly anything holding the chip to the carrier (no TC bond and no hardened TPU) the release of the bonding head alone was probably enough to slighly lift the chip, hence its tilted positioning and the TPU retraction underneath the chip. Although only a speculation, it revealed that the bonding head might not hold the chip under pressure until temperature was back below melting temperatures (the region after $\sim 140 sec$ in figure 5.19). The bonding machine by default cools down the structure before release (down to $200°C$), but it turned out the cooling was insufficient to properly cool down the TPU before release (Platilon U4201 melts above $155°C$).



(a) 361008 carrier with $25\mu m$ thick TPU sheet to be used as underfill during flip-chip bonding.



(b) 361008 carrier shortly after flip-chip bonding. TPU is not filling the entire bottom surface of the chip and it has shrunk in a single dimension.

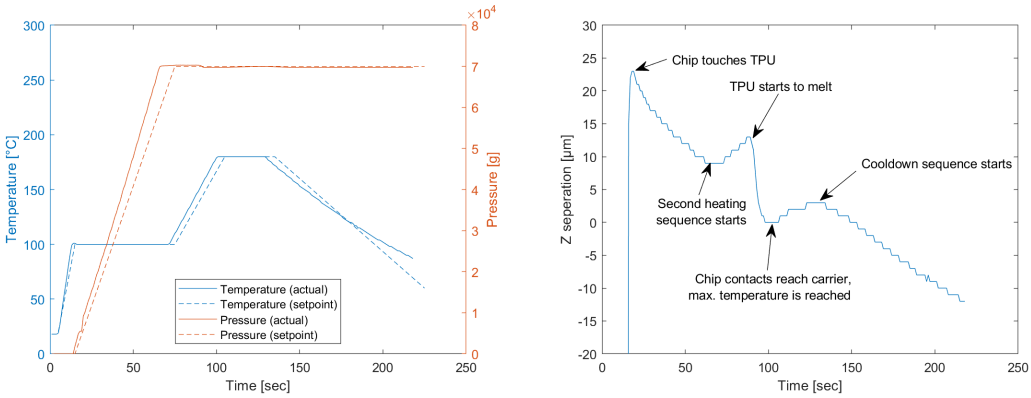


(c) Side-view of the 361008 carrier with bonded chip. excess TPU has manifested underneath the chip. No TC bonding seems to have occurred during bonding.

Figure 5.21: Pictures of TPU 361008 sample 8. The TPU sheet seems to have shrunk in a single direction. Similar results were found in samples 3-9.

At this point, the observation was made that the contacts were in fact $60 \times 60 \mu m^2$, as shown in 5.6, rather than the assumed $36 \times 36 \mu m^2$ contacts. According to previously discussed literature (figure 2.3 and work by Foerster [35]), pressure at $180°C$ should be in the order of 180-200MPa. This is slightly higher than previously applied pressures of $180 MPa$ because of the slightly lower bonding temperature. This amount of pressure translates to a bonding force in the range of 65-73kg. Along with the added cooling-down pattern, this resulted in a new bonding profile found in figure 5.22a.

The first sample bonded with this new bonding profile appeared to be bonded properly. However, successive samples once more showed results similar to those of figure 5.21. Ultimately, it was discovered that the bonding head would often miscalibrate in the Z-direction during bonding, causing it to apply the desired pressure on an internal component instead of the Cu substrate. This occurred only a couple of hundreds of



(a) Updated bonding profile according to initial findings for the 361008 Au-to-TPU assembly iteration.

(b) Height separation between chip contacts and Cu carrier during the bonding procedure. Height measurements are done relative and gives no information about the absolute height separation.

Figure 5.22: Typical bonding data for the final set of 361008 bonding samples. This bonding data originates from sample S20.

microns above the Cu substrate, causing the chip to stick to the TPU but not to bond. The problem was solved by elevating the bonding surface to ensure that force cannot be mistakenly applied to the internal component. The resulting assemblies were now consistent, though a misalignment of approximately 20 to 40μm remained. Bonding data found in figure 5.22 originate from a sample bonded using this final configuration. Bonding data of remainder samples can be found in figure D.13 through D.21 in appendix D.2.

With the flip-chip bonds appearing functional, the TPU transfer was done according to the lamination process described in figure 4.12a. Lamination temperature was reduced to 160°C which, together with the thinner chip (measuring at 300μm thickness), should reduce the track migration as observed in figure 5.14a. The Cu was then etched again according to the setup in figure 4.13b at 50°C.

5.7.3. HD Au-to-TPU resistance measurements

Three samples were assembled according to the final assembly parameters described in the previous section. These samples were numbered S18 through S20. 4-point measurements were conducted on each sample to evaluate the resistance of the contacts in each of the four corners and the four pads halfway these corners. Though values in the order of $m\Omega$ are expected (as measured in figure 5.13), S18 showed values only above 4Ω and while S19 showed one contact of 26$m\Omega$, the remaining contacts all measured above 10Ω. For S20, half of the measurements were in the $m\Omega$-range. Values for S20 can be found in figure 5.23.

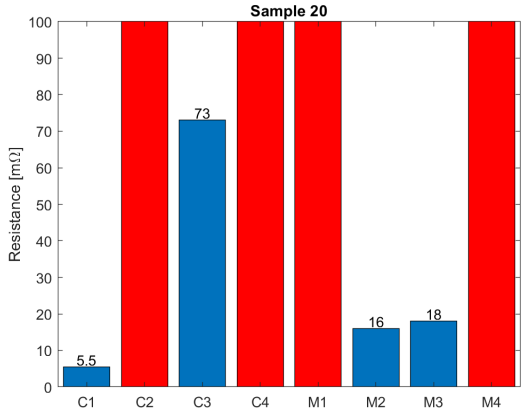


Figure 5.23: Updated bonding profile according to initial findings for the 361008 Au-to-TPU assembly iteration.

Additional 2-point measurements were conducted to map the scale of failures across the samples. This mapping can be found in figure 5.25. Note that the resistance of the measurement tracks in series with the two probes measures in the order of 1.0 to 1.5Ω.

The mapping holds an indication of the yield of proper contacts. If we observe the measurements running through the chip once (indicated with the blue arrows in figure 5.25), we see that out of 24 measurements across all samples, 5 indicated failure. These cases measure through 2 contacts (see figure 5.24) for which we can state the following in terms of failure probability:

$$\mathbb{P}(A \cup B) + \mathbb{P}(A \cap B) = \mathbb{P}(A) + \mathbb{P}(B) \tag{5.8}$$

Where $\mathbb{P}(A)$ and $\mathbb{P}(B)$ indicate the probability of failure for each of these two contacts (see figure 5.24). Assuming these probabilities are equal, and knowing that failure occurs in $\mathbb{P}(A \cup B) + \mathbb{P}(A \cap B) = \frac{5}{24}$ of measurements, we can say:

$$\frac{5}{24 \times 2} = \mathbb{P}(A) \tag{5.9}$$

We can therefore roughly estimate a bond yield of 90% across the three samples for the outer ring of contacts. Nonetheless, between 10 to 27 bonds need to be successful in order for a 4-point measurement to conduct properly (depending on which of the contacts is being measured), diminishing the chances of a successful 4-point measurement and supporting findings presented earlier in this section.

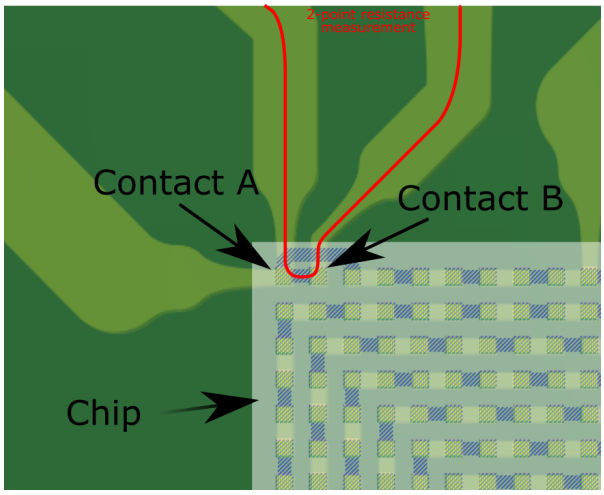


Figure 5.24: Zoom-in of 361008 substrate render including chip (outline in white). The red line shows a conductivity line of a 2-point measurement. 'Contact A' and 'Contact B' indicate the two bonds through which the measurement runs and can be used to estimate bond yield.

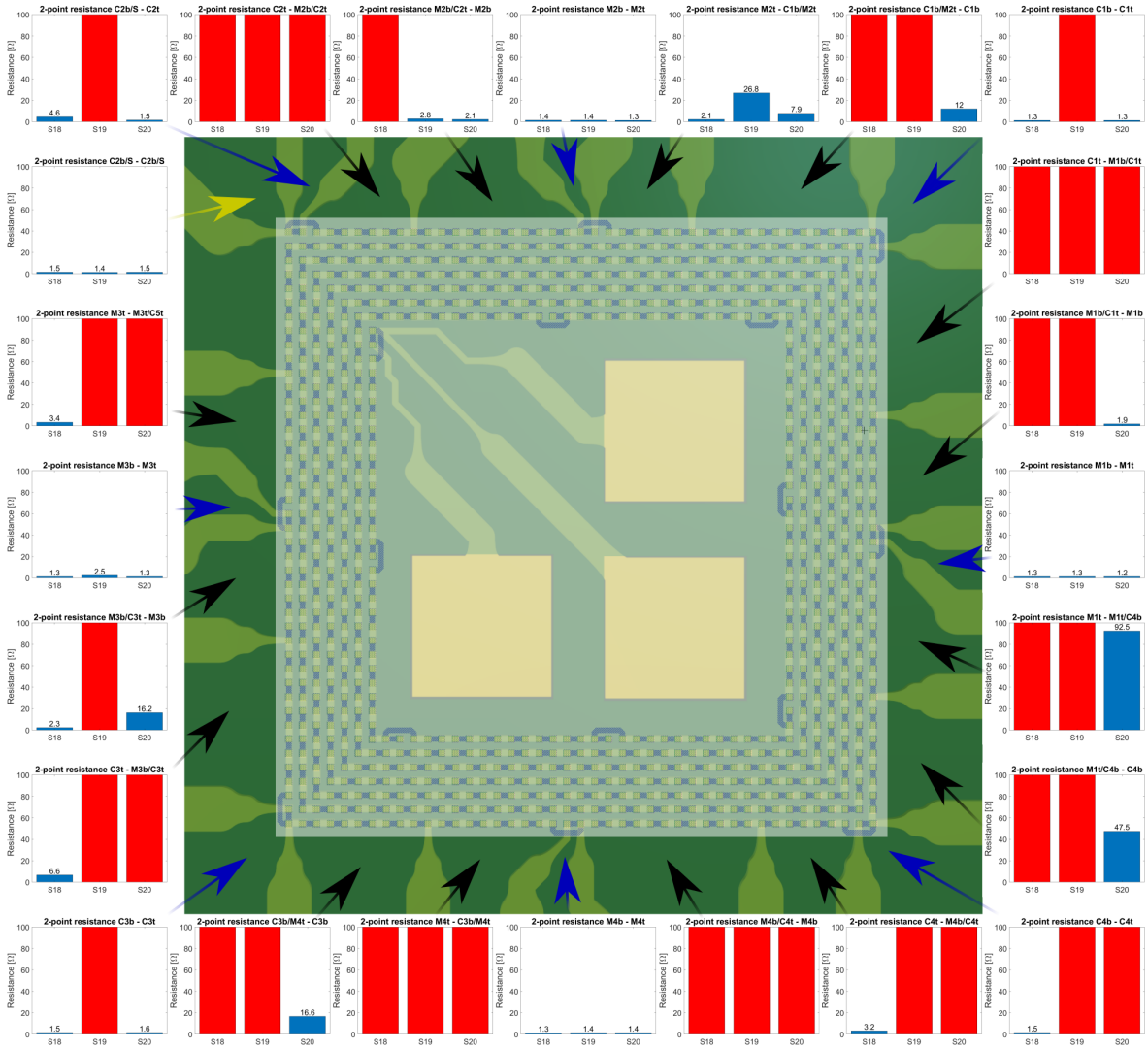


Figure 5.25: '361008' 2-point resistance measurements overview. In the center, a zoom-in of the substrate render (green and yellow colored) is shown with the chip configuration overlapping. The chip outline is shown transparent white, while its connections are shown in dark-blue. The outer picture area holds 2-point resistance measurement data of S18-S20. An arrow, originating from each of the graphs, marks between which two lines the measurement was conducted (the lines left and right of each arrow). Arrows in yellow indicate resistance measurements that *do not* run through the chip. Arrows in blue indicate 2-point measurements that run through the chip *once*. Black arrows indicate 2-point measurements that run through the chip *multiple times* (between 4-6 times). All resistances above 100Ω are considered OL and marked with red bars in the graphs.

5.7.4. HD Au-to-TPU failure analysis

To investigate the points of failure and the room for assembly improvement, a computer tomography (CT) scan was done on one of the final samples. The scan was investigated on void formations and bonding contact quality, however the resolution of this scan was too low to properly analyse these quality features.

In addition, a cross-section was made on a different sample using a water jet cutter, after which the sample was polished along the etching line. This is not the conventional way for a cross-section but was the quickest option given the thesis time constraints. The cutting and polishing process was difficult on a flexible substrate and damaged the sample in the process. Nonetheless, images seen in figure 5.26 showed valuable failure data. Jetting had washed away some of the TPU underfill together with some tracks, revealing some of the bonding patterns on the chip's electroplated contacts. Bonding spots can be seen at the areas that opened up, but they were not of the size that is to be expected when a proper thermocompression bond is made.

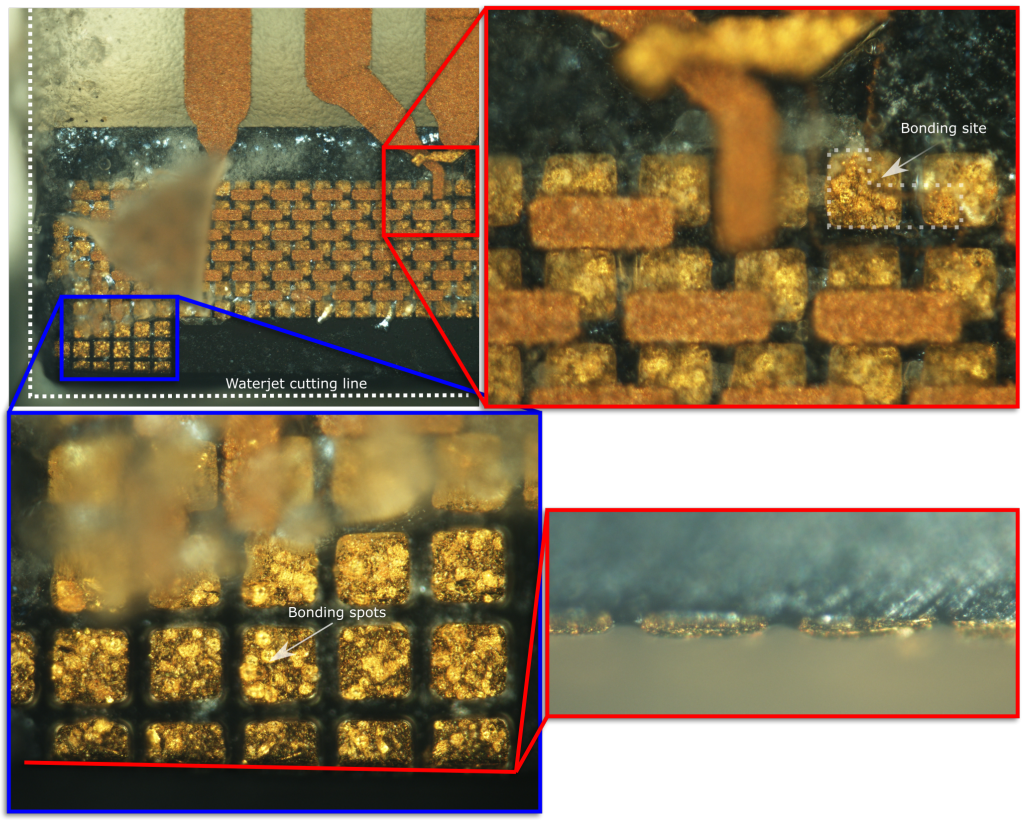


Figure 5.26: Images of TPU 361008 sample 18 cut with a water jet cutter. The top left picture shows a dotted line on which the cutting was done. The picture on the top right zooms in on a contact that was washed away during cutting, revealing that electrical contact was made over the full area of the track (dotted line). The bottom left picture shows a zoom in on a full area of tracks that was washed away, revealing bonding spots on most contacts.

5.8. Summary of findings for TPU processes

Results of 8072 samples and 361008 samples have shown promising results overall with the use of TPU. This chapter will briefly summarize the findings of some steps involved in the TPU substrate processing steps, including flip-chip bonding, lamination and Cu carrier etching.

TPU as a flip-chip bonding underfill TPU has shown significant advantages as an underfill in assemblies throughout this work. The most noticeable advantage is its thermoplasticity, which has proven to merge the underfill seamlessly with TPU sheets laminated on top of the chip (see figure 5.12). In addition, the underfill seems to perform well when it comes to uniformity, showing no optically visible void formation across the

chip surface. However, TPU as an underfill has its limitations in terms of temperature capabilities, allowing for flip-chip bonding only in the order of $< 200°C$. Nonetheless, the temperatures seem to be high enough to perform thermosonic (TC) bonding operations. For high-density 361008 assemblies, roughly 10% of bonds did not conduct. Failure analysis has shown that further experiments need to be done to optimize the bonding parameters.

TPU as a substrate Lamination and embedding steps with TPU sheets showed good results. Even though multiple TPU sheets had to be stacked to reduce stressing the chip, not one of these interfaces showed visible voids and all had merged seamlessly with one-another as well as the chip underfill. However, the lamination material has shown to contain significant amounts of dust particles and it is unknown whether this causes longevity issues for an assembly.

Cu etching The improved manual Cu etching method significantly improved the problems that were encountered after the release step. Samples were cleaner, though it still proved difficult to remove all residues of the etching solution completely. The chip surface no longer showed staining of Al contacts, but some failure was measured across a 3-day time-frame suggesting that etching solution might still be present.

5.9. High-density Au-to-TPU routing demonstrator

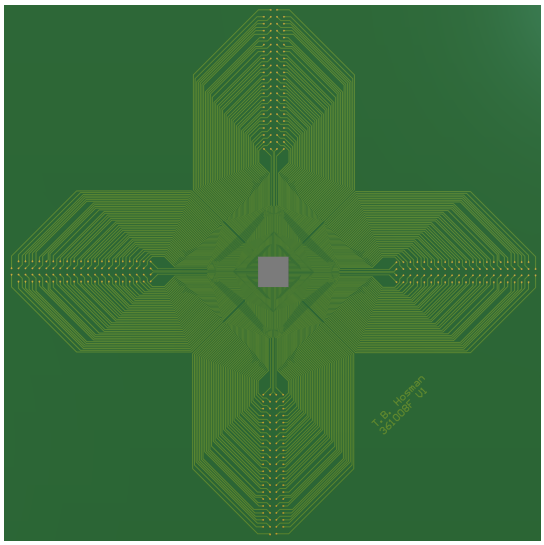
5.9.1. Au-to-TPU demonstrator substrate design

A final prototype was devised to function as a technical demonstrator and to prove that not only escape routing underneath the chip is possible (which is what the optimizer is built for) but also routing between the chip's outer dimensions and peripheral structures (such as electrodes). The substrate dubbed '361008F' (where the 'F' stands for 'full') was designed in Altium and should connect to as many electrodes as possible with the available technique. According to the technology described in section 4.5.2, the demonstrator has to be routed on a single metallization layer. As discussed in section 5.6, the top metallization layer allows for the 2 outer rows of the 361008 chip to be routed. The routing of these two rows, consisting of 328 contacts in total, can be found in figure 5.27. The design has 328 electrodes $200\mu m$ distributed over 4 wings. Each wing has their 82 electrodes distributed over 4 columns where the electrodes are spaced at $800\mu m$. The tracks connecting the electrodes become progressively smaller closer to the chip bonding surface to accommodate for the numerous tracks on this single metallization layer, shrinking in thickness from $100\mu m$ all the way down to $15\mu m$ in steps ($70\mu m$, $40\mu m$ and $30\mu m$).

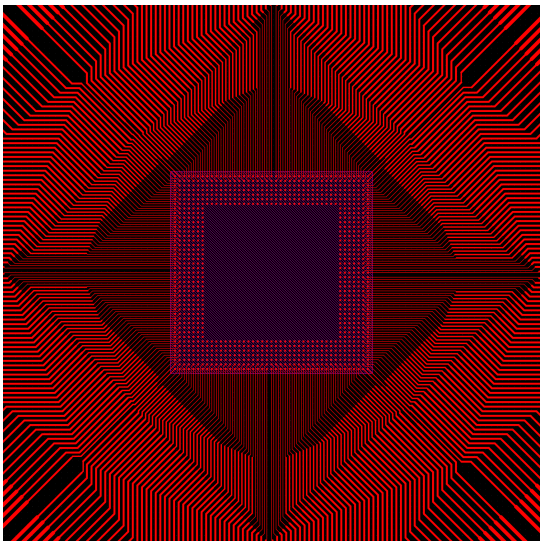
5.9.2. Au-to-TPU demonstrator assembly

In contrast to previous assemblies that apply the Au-to-TPU methodology, the demonstrator assembly is manufactured on a $70\mu m$ Cu carrier instead of $105\mu m$. These thinner pieces of Cu are slightly more difficult to handle and more fragile. However, they require shorter Cu etching times during the transferring steps to TPU, which in turn has shown that it reduces track and contact damage to the samples (section 5.5.2) and staining (section 5.5.4). Au plating of the Cu carriers was done for 20 minutes, giving the samples an estimated Au track thickness of $3\mu m$ when linearly extrapolating the data of section 5.3.1. The thickness of the Au could not be analytically measured for these samples because the features were too small to be properly registered by the analyser. In all other aspects, manufacturing of the Cu carrier was done identical to the 361008 samples as described in section 5.7.1. Pictures of the 361008F Cu carrier patterned with the Au tracks can be found in figure 5.28.

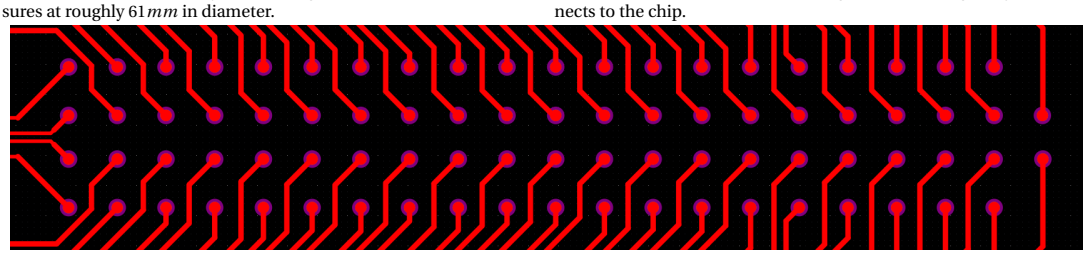
The successing steps were identical to those of the final 361008 samples described in section 5.7.2, using figure 5.22a as a bonding profile for $300\mu m$ thick chips and laminating at at $160°C$, though only 5 TPU layers were used in the first lamination step. Bonding data of demonstrator samples can be found in figure D.22 through D.23 in appendix D.2. Cu was etched in roughly 13 minutes followed by thorough cleaning in DI water, IPA and an ultrasound bath ($45°C$ for 5 minutes). After the embedding lamination step, the 361008F samples were released and manually cut to size with a pair of scissors. A picture of the completed demonstrator can be found in figure 5.29. The demonstrator measures at approximately $16.8cm^2$ of surface and is roughly $600\mu m$ thick.



(a) Render of the full prototype including the chip. The structure measures at roughly 61mm in diameter.



(b) Zoom-in of the tracks connecting to the bonding array that connects to the chip.



(c) Zoom-in of electrodes on one of the 361008F wings. The circular electrodes are 200μm in diameter and connected to 100μm thick tracks.

Figure 5.27: Render images of the 361008F prototype connecting 328 electrodes to the outer two rows of the 361008 chip.

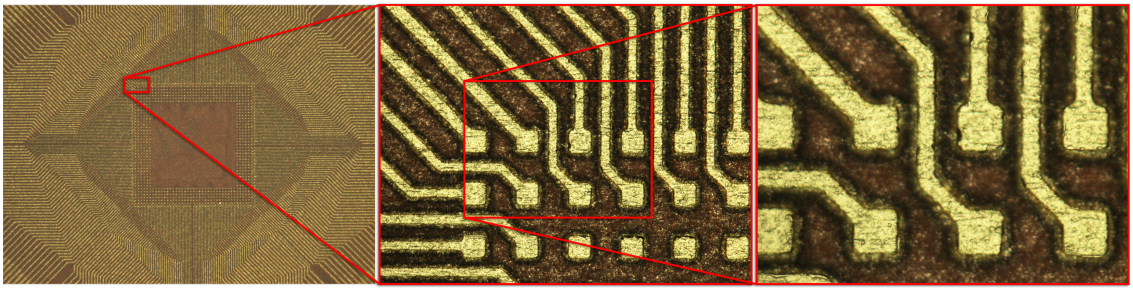


Figure 5.28: Au patterned on Cu for the 361008F demonstrator samples.

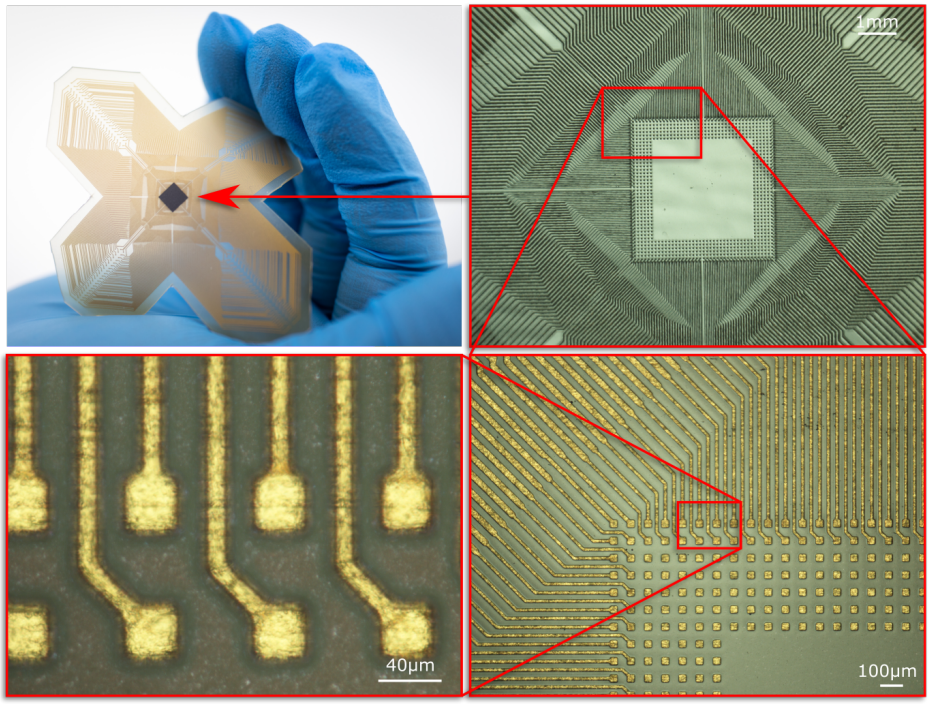


Figure 5.29: Picture of a fully embedded 361008F sample including pre-bonding zoom-in images of the chip bonding site and track structure.

5.10. Optimal array configuration for 10.000 contacts

Due to time constraints and intermediate findings of this thesis, no practical research was conducted to assemblies beyond 1008 contacts. However, the optimisation script as described in chapter 4.1 allows for multiple technology parameters to be defined by the user, giving insight in potential design parameters for a system with 10.000 individual contacts. A novel technology by Zoschke et al. allows for high-density multilayer routing on PI and is taken as a technology reference [63]. A graphical overview of technology limitations as described in the paper can be found in figure 5.30.

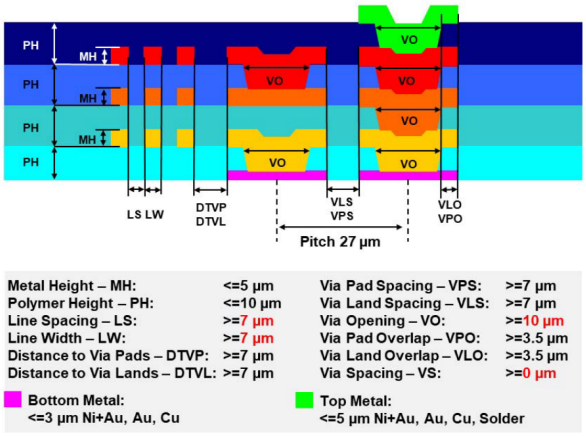


Figure 5.30: A graphical cross-section showing technology limitations of the technology developed by Zoschke et al. [34]

These technology limitations were combined with reasonable bumping technology limitations (stating a bump size of $36 \times 36 \mu m^2$ as described in section 5.6) and the desired number of connections of 10.000. The resulting specifications according to the optimiser script are as follows:

- $1.26 \times 1.26 cm^2$ chip dimensions
- 10.008 connections
- $36 \mu m$ pad size
- $80 \mu m$ center-center pad pitch
- 18 rows
- 157 outer pads
- 4 substrate layers

The plot given by the optimiser can be found in figure 5.31, where one can see that indeed the optimum lies at a $80 \mu m$ center-center pad pitch. However, note that alternative optima can be found in the plot too if other specifications are desired. For example, chip dimensions still remain below $1.3 \times 1.3 cm^2$ for center-center pad pitches of 66, 71, 85 and $94 \mu m$.

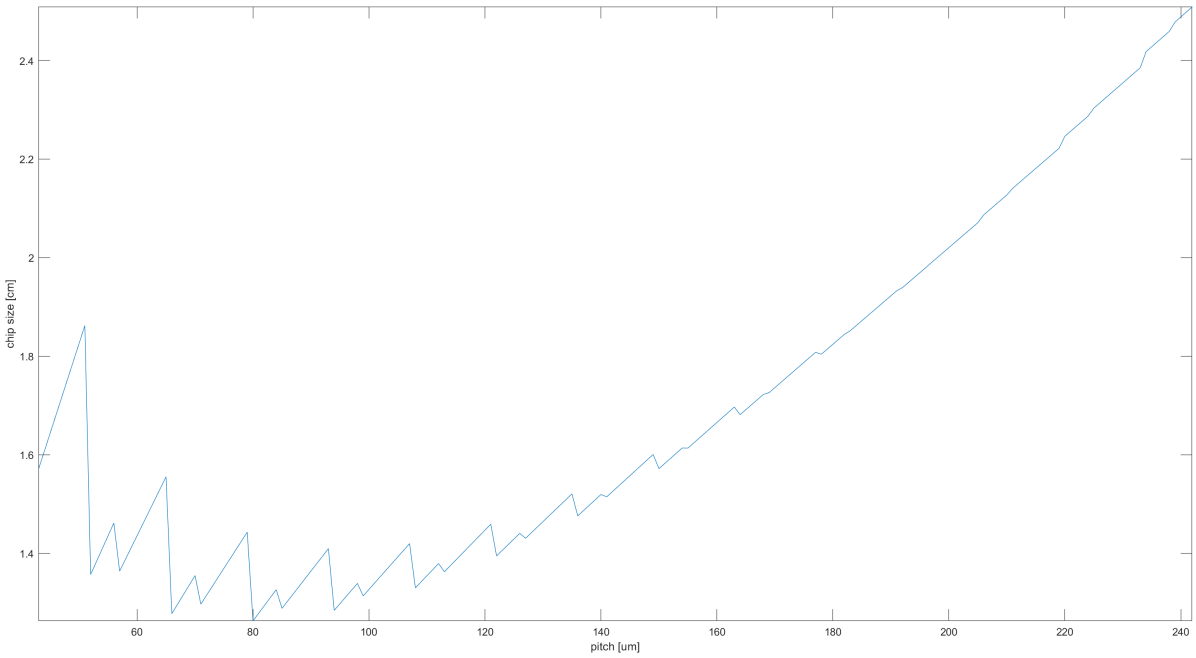


Figure 5.31: Generated optimiser plot for 10000 connections configured for technology parameters found in chapter 5.10.

6
Discussion

6.1. Chip fabrication

A couple of remarks are to be made regarding the chip fabrication. Firstly, it was observed across multiple 361008 samples with TPU that delamination was occuring between the chip and the TPU (seen also in figure 5.20b. This would normally disappear after the second (embedding) lamination process but indicates poor adhesion between TPU and the SiO_2 passivation of the chip nonetheless. This was not observed with any of the 8072 substrates, neither for NCA nor TPU underfill samples. Most likely, the unused patterns for $40\mu m$ and $20\mu m$ contacts provided a rougher surface or more suitable material for the underfill material to adhere to. Adhesion between TPU and the passivation layer should be investigated in more detail for future chip designs.

A second remark on the chip manufacturing lies in the electroplating margins of chip manufacturing. Optimisation assumed contacts of $36\mu m$ but for the 361008 chip they were in fact almost $60\mu m$ after electroplating. Bonding happens on the same Au metallization layer as some of the tracks and so it leaves little room for substrate tracks to run between the contact pads. It should be emphasized that for the optimiser to function properly, the optimiser input should correspond with the contact dimensions after electroplating and *not* the dimensions of the Al chip openings as was done with the 361008 chip.

6.2. Substrate fabrication

In terms of substrate fabrication, the biggest point of discussion is the use of Cu as a carrier. Though Cu is etched in the developed transfer-based processes, it is never completely removed from the Au tracks. The main cause for this is that Cu diffuses into the Au over time, a process that is accelerated with heat (such as a flip-chip bonding step). Wet Cu etching cannot reach to all of these Cu particles, which are left in the tracks. This phenomenon can be seen across all samples, which show a more Cu-coloured track surface on the side that was in contact with the Cu carrier. The Cu residues make the prototypes inherently unsuitable for implantation, though the exact impact this has on cells remain unknown and could be investigated.

Another point of discussion is the absence of options for multiple layers in the developed transfer-based process. The initial hope was to continue on existing multilayer work with PI within Fraunhofer IZM but this process turned out to be unsuitable for Au tracks and PI is inherently not elastic enough for CNS implantation. The currently established transfer-based process does not support multilayer metallization.

6.3. Flip-chip bonding

Regarding the thermocompression (TC) flip-chip bonding with the 361008 chip, contact was made between the chip contacts and the Cu carrier. However, the contact was not perfect and showed failure in about 10% of the connections. There are possibly multiple causes.

Firstly, the assembled work was processed in an *ISO* 6 rated cleanroom. In contrast, high-yield flip-chip processes are generally performed in an *ISO* 2 rated cleanroom or better (10^4 times fewer particles than *ISO* 6). Similar flip-chip work with TPU underfill and the same bonding machine showed more than 30% failure on PCBs after bonding, though no exact failure criterium is given. The author suggests that reason of low yield could be due to the cleanliness of the cleanroom [35]. Scaling these yield results to a high-connectivity chip such as the 361008 chip in this work, a bonding yield like this is likely to result in poor assembly results. A second reason for the observed bond yield in this work could be a lack of bonding pressure. A solid thermocompression (TC) bond often shows bonding contact on the entire edge of the bump surface. However, although figure 5.26 shows some indications of bonding, it does not look like bonding patterns seen in other TC flip-chip bonding work. The reason for this could be twofold. On the one hand, the used TPU sheets are $\sim 25\mu m$ thick and should melt down to roughly $10\mu m$ in thickness for the chip and substrate to touch. This might be just too much material to push away, so thinner TPU underfill sheets could be considered. In addition, higher pressure or a longer bonding time above the TPU melting temperature could give the material more incentive to move, leaving more time for TC flip-chip bonding to occur.

Finally, the observed chip-to-carrier misalignment of 20 to $40\mu m$ decreases the area of contact which consequently reduces the chances of forming a proper bond on a significant area. The cause of the misalignment is not fully understood. The misalignment is not consistent in a certain direction making a misalignment issue within the bonder itself unlikely. Therefore, a non-uniformity of one of the parts between the bonding head and the substrate vacuum is the most likely cause (such as the Cu carrier, chip, bonding tool or substrate tool). Non-uniformity in the chip is very unlikely, being produced in a well-regulated wafer processing line. The Cu carrier substrate was taped to the substrate holder because of its flexibility as a foil. Looking from the bonder's bi-directional microscope this was sufficient to properly align the chip with the Cu substrate making this too an unlikely cause of non-uniformity. This leaves two bonding components to be checked for non-uniformity: the chip underfill and the bonding tool (holding the chip). The latter was a tool with significant use and thus a likely cause, but neither has been tested for confirmation.

It should be noted that the bonding force of $70kg$ used in latest prototypes is at the limit of what the used SET FC150 bonder can apply ($< 100kg$). The applied force for the 361008 is likely to increase according to failure analysis found in section 5.7.4 so linear scaling of pressure for 10.000 connections would require over $700kg$ of bonding force. This kind of force is possible with more advanced bonding machines such as the SET FC300. Temperature during TC bonding could be increased to reduce required bond force, but the underfill material should be able to handle the temperature. For TPU as an underfill, this would require a different kind of TPU that is more resistant to heat. Alternatively, the required bond force could be lowered by switching to thermosonic (TS) bonding, though bonding parameters for this work remain to be investigated.

6.4. TPU lamination

The lamination of TPU samples showed excellent results with no visible voids in the material. However, due to the non-uniformity caused by the chip on the Cu carrier, a significant amount of TPU had to be laminated to give the chip room in which it can level out, ensuring minimal stress on the tracks around the chip. This makes the prototype significantly thicker around the peripheral tracks than what is technically necessary. Regardless of the used lamination layer thickness, the current process of lamination has shown that strain forms on the connecting tracks to some degree. Ideally, lamination should happen in a way that the tracks remain parallel and do not experience any straining forces during the lamination. This remains to be investigated.

Though no visible voids were encountered, small inconsistencies should still be investigated on in the TPU lamination process. In all samples, a significant amount of dust particles were observed even though all lamination components were cleaned thoroughly with compressed air and ethanol. When aiming for implantation, such particles could allow for water vapour to manifest and damage the implant, and could significantly influence the electrical properties of substrate tracks. The effect of these material inconsistencies remains to be investigated.

7

Conclusions and future work

7.1. Conclusions

There is a clear momentum and demand in the world of neuroscience for high-density neural stimulation and recording implants. The investigation and mapping of biological neural networks is essential for understanding and curing of neural disease and malfunction. The aim of this work was to reach a new milestone in the fabrication of the next generation of high-density neurostimulation systems and to provide new technology for this field of neuroscience. The set goal at the beginning of this work was to develop an assembly technique that allows for highly dense contact arrays with up to 10.000 individual chip connections. In addition, the goal was to accompany such an assembly technique with a multi-layered substrate material that is flexible and biocompatible.

Initial results for this goal were produced using a custom designed multi-functional chip consisting of 72 to 120 contacts of either $80\mu m$, $40\mu m$ or $20\mu m$ in dimension. The chip's main function is to evaluate what contact size is reasonable to assemble with. These contacts were bumped using manual stud bumping. For a successive work, a second chip with 1008 contacts $36\mu m$ in diameter was fabricated with electroplated (EP) contact bumps. This chip has an unheard-of connectivity density more than four times higher compared to existing neurostimulating systems.

Different connection techniques were evaluated for these chips and concluded that for these chips thermocompression (TC) flip-chip bonding was most suitable because it best suited the biocompatibility requirements, allowed high-density connectivity and was conveniently available within Fraunhofer IZM. TC flip-chip bonding was done using two different kinds of underfill: an epoxy-based non-conductive adhesive (NCA) and thermoplastic polyurethane (TPU) acting as an non-conductive film (NCF).

The NCA adhesive was first used in an additive build-up assembly with polyimide (PI) as a substrate material because of its mechanical and chemical stability. Tracks were made of Cu coated with a thin layer of immersion Au and showed good flip-chip bonding results with the lower-density chip, measuring between 1.2 and $4.0 m\Omega$. Nonetheless, the process was changed to a transfer-based process because Cu lacks biocompatibility. Cu is only used as a carrier and etched away after transfer to a polymer material. First experiments showed some problems in the chip assembly, such as voids in the NCA and Cu etching damaging to the chip. Though solvable issues, more fundamental problems to the process existed: no assembly method existed that allowed for pure-Au metallization on PI (only Au-plated Cu) and PI is inherently very non-elastic making it an unlikely candidate for implantation in soft neural tissue such as the central nervous system (CNS).

More fruitful results were observed in a similar transfer-based process optimised for the use with TPU, which is significantly more elastic than PI and thus more suitable for implantation in soft neural tissue. Being a thermoplast, this material is able to remelt without changing its chemical consistency during processing. In this work, the material is for the first time used as chip underfill as well as transfer and embedding material and can therefore encapsulate as a completely uniform substrate, forming a material interface only with the tracks and chip. This has significant potential for implant lifetime. Initial produced 72-contact samples

($80\mu m$ pad size) showed clean bonding results with no voids and significantly less etching damage. Contact resistances were good for assemblies with the lower-density chip, measuring between 4.5 and $14m\Omega$. Daisy-chain measurements measured at 18Ω.

Scaling the work with TPU proved partially successful. TC bonding showed successes for an estimated 90% of the 1008 contacts of this chip, with measured resistances in the range of 5.50 and $73m\Omega$. In addition, a misalignment between 20 and $40\mu m$ was observed in the three successfully bonded assemblies. Most likely improvements for bonding yield and misalignment include thinner underfill TPU sheets, higher or longer maximum bonding pressure, cleaner assembly (better than *ISO* 6) and a new bonding tool.

The gathered knowledge was applied in the fabrication of a demonstrator prototype. This prototype is able to connect 324 electrodes ($200\mu m$ in diameter) on a single metallization layer to the chip using tracks as small as $15\mu m$ in width. The entire demonstrator measures at $600\mu m$ in thickness and spans across just $16.8cm^2$.

7.2. Future work

The presented work has shown some successful results in the production of a high-density flexible implant, but there are some aspects that should be further investigated in the described assembly technology.

Improve flip-chip bonding procedure In terms of the bonding process, continuation should optimise the clearly imperfect bonding setup and parameters. Specifically for the high-density work in this thesis, most likely improvements include: thinner underfill TPU sheets, higher or longer maximum bonding pressure, a cleaner bonding environment (better than *ISO* 6) and new bonding tools. These improvement should reduce misalignment and yield issues that were observed in the final work of this thesis. Though electroplated (EP) chip contacts have indeed shown to require higher bonding pressure, future work should keep focus on EP-bumped chips if the carrier material allows. If bonded well, EP contacts have (compared to stud bumps) more potential to offer more in terms of miniaturization, scalability and reliability.

Characterise assembly More mechanical and electrical characterization tests need to be done to assess the reliability of the presented assembly technique. Mechanically, this includes shear testing, bending and torsion testing, temperature cycling, humidity cycling and soak testing. All to evaluate long-term behaviour under mechanical stress and simulate an implant environment. Electrically, characterization could include cross-talk sensitivity measurements and more detailed contact/track impedance measurements. The daisy-chain and 4-point measurement structures of this work can be used to measure bond state during the characterization tests.

Scale to more contacts The work could be expanded for more than the current 1008 chip-to-substrate contacts. However, better tooling would be required to allow for such progress to be made. Since thermocompression (TC) flip-chip bonding is likely to remain as a bonding method for such systems (due to the limited amount of parameters and the available literature) one would need to increase bonding force if the number of contacts is increased (or contact size should be decreased). For 10.000 electroplated contacts $36\times36\mu m^2$ in size, bonding force would be in the order of 200-250kg for TC bonding. The used machine (SET FC150) goes up to $100kg$ in bonding force so one would need to have access to its bigger brother (SET FC300) for such a chip. Alternately, one could decrease contact size to 20 - $25\mu m$, which would require $< 100kg$ of maximum bonding force. However, it is unknown whether such pad sizes are feasible.

Another way of decreasing bonding force for 10.000 contacts would be to experiment with thermosonic (TS) flip-chip bonding. This form of bonding decreases required bonding force to almost half that of TC bonding, however it is also significantly more difficult to set up (due to tooling and additional parameters) and is notorious for more misalignment due to the added ultrasonic forces.

Whatever chosen direction, if a new chip were to be made for further iterations, it should bare in mind the margins involving electroplating.

Improve TPU lamination process The overall thickness of current prototypes ranges between $500\mu m$ and $700\mu m$, most of which is required because of the thickness of the chip. There are two ways to reduce the overall thickness of the prototype. The first would be to thin the chips down further than $300\mu m$, possibly

down to tens of microns. An added benefit to this would be a slight improvement to the flexiblity of the chip. The second option would be to make a cutout in the FR-4 carrier material before the first lamination step, giving the chip some room to press into. Such method could make most of the prototype much thinner ($< 100\mu m$ thick), though the region around the chip would still be thicker due to the chip thickness.

In addition, future work should investigate the options of using a cleaner lamination environment. Current work showed significant dust contamination which can diminish implant longevity significantly.

Expand to multi-layered substrates For the substrate manufacturing technology, further investigation needs to be done to support multilayer metallization and vias while preventing non-biocompatible materials such as Cu to manifest in the final assembly. A radically different wafer-level process was developed during this thesis and can be found in appendix E. However, a cheaper option would most likely be to continue the current path of non-wafer carrier materials. Multilayer tracks should be possible by repeating the manufacturing of a Au-patterned carrier and laminating it to an existing embedded assembly, however the main complication is the formation of vias between these layers. Continuing efforts within Fraunhofer IZM have started to adapt this proposed technology to accommodate multilayer substrates.

Modify the carrier material The current use of Cu as a carrier material was chosen due to the established options within Fraunhofer IZM. However, this work has shown significant flaws for Cu as a carrier material for implants, mentioning three specifically: 1) Cu is not a biocompatible material and is not desired in an implant, though it is unclear if low concentration levels are problematic. 2) Cu migrates into the Au patterns, especially during heated process steps such as flip-chip bonding. It is difficult (if not impossible) to properly etch all Cu manifested in the Au. 3) The Cu etching solution deteriorates TPU and underlying structures.

Future work could benefit from converting the process to a carrier of a different material (such as Ti) to circumvent these issues. This could be used as a barrier material on top of Cu or as a completely standalone carrier material. Such alternative carrier materials and their corresponding etching solutions should be investigated.

Investigate adhesion strength of remaining interfaces TPU has shown with its thermoplasticity to be a valuable material in the reduction of material interfaces, concequently allowing for improved longevity of implantables. However, the final bonding results have shown that adhesion between other materials should be investigated and quantised by means of peel tests.

For one, the adhesion between TPU and SiO_2 is troublesome, showing visible delamination at the material interface. It is currently unknown whether this is due to the material or due to the roughness of the chip passivation. Either way, this material interface remains to be investigated and improved in future work for the sake of implant longevity.

A second interface to be investigated is the adhesion between the Au tracks and the TPU. This was workable for the purpose of this work, but could be better to allow for different assembly methods (e.g. automated Cu etching, which was not possible in this work due to adhesion of this interface).

Add integrated chip functionality Currently, the chip used in this work has only passive characterization tracks. Extensive investigation needs to be done on a functional IC design that can include sufficient functionality in the given dimensions of this work without breaking the given low-power budget and crosstalk limitations that an implant is often given. In addition, the extraordinary amount of generated data coming from these high-density arrays should be intelligently processed and compressed to be transmitted or to be translated to stimulation signals.

Furthermore, IC design could investigate a multi-chip configuration which opens up new possibilities for implant flexibility (because the chips are smaller) and routing optimisation (more details below). In addition, it could improve electrical properties such as track impedance and cross-talk (because the chips can be distributed to be closer to the electrodes).

Improve optimiser functionality Currently, the routing optimisation makes four significant assumptions to application and technology for which it optimises. The first assumption is that all connections from the chip are assumed to be in the correct position to be routed directly outward to the periphery of the chip. This simplifies the grid optimisation because no complex network re-routing has to be done (such as Yan et

al. [57]), something that could be needed when an IC is not specifically designed for a certain electrode layout. Another assumption that was made is the grid structure, which the optimiser assumes to be consisting of square contacts organized in a grid. However, in theory, both circular contacts as well as a non-grid array (such as a hexagonal array) could theoretically further decrease required chip surface [59] [58], and there could be valid IC design reasons to have a non-square chip design. The third assumption made in the optimiser is that for multilayer substrates, vias can be placed directly under the bonding surface. It has been done in other multilayer flexible substrates but it is unknown if this is a reasonable assumption for future applications of this technology. The fourth and final assumption is that the circuitry on the chip is assumed to have no influence on the grid distribution. However, circuitry might restrict the placement of pads on certain locations in the grid. This is not so much a problem for a single contact (removing a single pad hardly influences the optimum), but for larger restricted areas the optimum could shift significantly.

In addition for the optimiser methodology, it should be noted that it is limited to the escape routing of a single chip. There could very well be advantages to splitting the chip functionality into multiple (intercommunicating) chips. 10.000 contacts could be spread over 4 chips with 2.500 connections each, for example. This theoretically reduces the total chip surface required for interconnect: with identical design specifications, a single 10.000-contact chip would measure at $1.26 \times 1.26 cm^2$ while four 2.500-contacts chips would theoretically measure at $0.76 \times 0.76 cm^2$. The reduced number of contacts additionally reduces specifications to the bonding parameters and gives more flexibility to the substrate as a whole. Additionally, such a distributed system would theoretically mean less and shorter interconnecting tracks to peripheral electrodes, reducing chances of failure and reducing crosstalk. One should bare in mind though that intercommunication and synchronization between the chips is not trivial and that chip components have fewer resources to share (e.g. power circuitry).

Appendices

A

Array Optimiser code

A.1. Variables

Important variables in the optimiser script are explained here. Apart from the description, the table includes equivalent variables of the calculations done in chapter 4.1.1 if applicable.

Table A.1: Overview of optimiser variables

Variable name	Formulae equivalent	Description
ARRAY_SIZE		Number of iterations that will be calculated.
PAD_SIZE		Dimensions of a pad in microns.
N_PADS	N	Number of pads required between chip and substrate.
LAYERS	L	Number of metallization layers available on the substrate.
LW_MIN		Minimum track width in microns.
LS_MIN		Minimum spacing between tracks in microns.
VPS_MIN		Minimum spacing between via pads in microns. Generally no restriction because VIA_SIZE<PAD_SIZE.
VO_MIN		Minimum size of via in microns.
PITCH_MIN		Minimum center-center pitch possible between pads in microns.
PITCH_ADD		Additional pitch needed to route additional track.
VIA_SIZE		Minimum width of a via.
PITCH_EE_TOP_MIN		Edge-edge distance between top layer pads.
PITCH_EE_VIA_MIN		Edge-edge distance between vias.
CCPitchArray	p	Array of size ARRAY_SIZE containing center-center pitch values of all iterations. PITCH_MIN is the smallest center-center pitch and is therefore the first value. Consecutive values incrementwith PITCH_ADD.
topEEPitchArray		Array of size ARRAY_SIZE containing edge-edge pad pitch values of all iterations.
viaEEPitchArray		Array of size ARRAY_SIZE containing edge-edge via pitch values of all iterations.
NPadsActual		Array of size ARRAY_SIZE containing number of pads of all iterations after rounding up. This number will be higher than N_PADS whenever there is room left to route on the chip.
topRArray	r_1	Array of size ARRAY_SIZE containing the number of routable rows when routing ONLY the top row.
viaRArray	r_n	Array of size ARRAY_SIZE containing the number of routable rows when routing ONLY a burried row.
totalRArray	R	Array of size ARRAY_SIZE containing the total number of routable rows for each iteration.
dimensionArrayUm	d	Array of size ARRAY_SIZE containing the chip size for each iteration in microns.
sectorLengthArrayUm	l	Array of size ARRAY_SIZE containing the width of a single sector.
outerPadsArray	N_{outer}	Array of size ARRAY_SIZE containing the number of pads present on the outer dimensions of the chip.
visualizerArray		Array representing chip distribution. Pads are represented by a '1' and opens by a '0'.
visualizerArrayScaled		A scaled version of visualizerArray where indices correspond to the chip size in microns. By default, 1 index is equivalent to 1 micron. This can be scaled using the 'scale' parameter of the plotVisual function.

A.2. Main code

```
%-------------------------------------------------------------------------%
% Part of array visualizer for CoF applications as part of my thesis
% project titled 'High-density interconnect technology optimised for
% flexible implants'. This is the main script of the optimizer.
% Full documentation can be found in my thesis report.
%
% Author:    T.B. Hosman
% E-mail:    timhosman@posteo.net
% Version:   1.2
% Created:   01/08/2019
% Modified: 22/08/2019
%-------------------------------------------------------------------------%

close all
clear variables

%% Constants
ARRAY_SIZE = 200; % number of pitch sizes to calculate
PAD_SIZE = 36;    % microns
N_PADS = 10000;   % # of pads
LAYERS = 4;       % number of layers
LW_MIN = 7;       % minimum track width in microns
LS_MIN = 7;       % minimum spacing between tracks in microns
VPS_MIN = 7;      % minimum spacing between via pads in microns
VO_MIN = 10;      % minimum size of via in microns
VLO_MIN = 3.5;    % minimum pad size beyond pad in microns

%% Extracted constants
PITCH_MIN = PAD_SIZE + VPS_MIN;  % minimum pitch between pads in microns
PITCH_ADD = LW_MIN + LS_MIN;     % add. pitch required to route extra line
VIA_SIZE = VO_MIN + 2 * VLO_MIN; % minimum width of a via
PITCH_EE_TOP_MIN = PITCH_MIN - PAD_SIZE;% edge-edge distance top layer pads
PITCH_EE_VIA_MIN = PITCH_MIN - VIA_SIZE;% edge-edge distance between vias

%% Array initialization
CCPitchArray = linspace(PITCH_MIN, PITCH_MIN + ARRAY_SIZE - 1, ...
    ARRAY_SIZE); % generate center-center pitch array
topEEPitchArray = CCPitchArray - PAD_SIZE;% generate distances between pads
viaEEPitchArray = CCPitchArray - VIA_SIZE;% generate distances between vias
NPadsActual = zeros(1,ARRAY_SIZE);

%% Calculate number of routable rows
topRArrayUR = 1 + (topEEPitchArray - VPS_MIN) / PITCH_ADD;
viaRArrayUR = 1 + (viaEEPitchArray - VPS_MIN) / PITCH_ADD;
topRArray = floor(topRArrayUR); % round down
viaRArray = floor(viaRArrayUR); % round down
totalRArray = topRArray + (LAYERS - 1) * viaRArray;

%% Chip size calculations
dimensionArrayUm = (N_PADS / 4 ./ totalRArray + totalRArray + 1) ...
    .* CCPitchArray;
dimensionArrayCm = dimensionArrayUm / 10000;
sectorLengthArrayUm = dimensionArrayUm - 2 * CCPitchArray;
sectorLengthArrayCm = sectorLengthArrayUm / 10000;
```

```
55 outerPadsArrayUR = dimensionArrayUm ./ CCPitchArray - 1;
56 outerPadsArray = ceil(outerPadsArrayUR); % ensures we have at least N_PADS
57
58 %% Calculate actual number of pads
59 smallestFullArrayIndex = 0;
60 for n=1:ARRAY_SIZE
61     [NPadsActual(n), ~, rFull] = ...
62     generate_visual(outerPadsArray(n),totalRArray(n),false);
63     % Check if a full-array configuration was found
64     if (rFull && (smallestFullArrayIndex == 0))
65         smallestFullArrayIndex = n;
66     end
67 end
68
69 %% Verify theoretical calculations
70 syms c;
71 ver3 = zeros(1,ARRAY_SIZE);
72 ver8 = zeros(1,ARRAY_SIZE);
73 ver9 = zeros(1,ARRAY_SIZE);
74 %---------------------- verify formula 3.3 ----------------------%
75 for iArray=1:ARRAY_SIZE
76     ver3(iArray) = sectorLengthArrayUm(iArray) / CCPitchArray(iArray);
77 end
78
79 % give result to user
80 if (round(outerPadsArrayUR, 4) == round(ver3 + 1, 4))
81     fprintf('Formula 3.3 PASS\n')
82 else warning('Formula 3.3 not satisfied')
83 end
84
85 %---------------------- verify formula 3.8 ----------------------%
86 for iArray=1:ARRAY_SIZE
87     ver8(iArray) = totalRArray(iArray) * sectorLengthArrayUm(iArray) / ...
88         CCPitchArray(iArray) - symsum(2*(c-1), c, 1, totalRArray(iArray));
89 end
90 % give result to user
91 if all(ver8 == ver8(1)) fprintf('Formula 3.8 PASS\n')
92 else warning('Formula 3.8 not satisfied')
93 end
94
95 %---------------------- verify formula 3.9 ----------------------%
96 for iArray=1:ARRAY_SIZE
97     tmp = totalRArray(iArray) * (sectorLengthArrayUm(iArray) / ...
98         CCPitchArray(iArray) - totalRArray(iArray) + 1);
99     ver9(iArray) = round(tmp,4); % filter small rounding errors
100 end
101 % give result to user
102 if all(ver9 == ver9(1)) fprintf('Formula 3.9 PASS\n')
103 else warning('Formula 3.9 not satisfied')
104 end
105
106 %---------------------- verify formula 3.10 ----------------------%
107 for iArray=1:ARRAY_SIZE
108     ver10(iArray) = (totalRArray(iArray) - 1) * ...
109         (sectorLengthArrayUm(iArray) / CCPitchArray(iArray) ...
110         - totalRArray(iArray));
```

```
111 end
112 % give result to user
113 ver10 = round(ver10 + outerPadsArrayUR - 1, 4);
114 if all(ver10 == ver10(1)) fprintf('Formula 3.10 PASS\n')
115 else warning('Formula 3.10 not satisfied')
116 end
117
118 %---------------------- verify formula 3.11 ----------------------%
119 for iArray=1:ARRAY_SIZE
120     ver11(iArray) = N_PADS / 4 - ((totalRArray(iArray) - 1) * ...
121         (sectorLengthArrayUm(iArray) / CCPitchArray(iArray) ...
122         - totalRArray(iArray)));
123 end
124 % give result to user
125 if (round(ver11 + 1, 4) == round(outerPadsArrayUR, 4))
126     fprintf('Formula 3.11 PASS\n')
127 else warning('Formula 3.11 not satisfied')
128 end
129
130 %% Output to user
131
132 % Plot chip size over pitch
133 plot(CCPitchArray,dimensionArrayCm);
134 xlabel('pitch [um]');
135 ylabel('chip size [cm]');
136 axis tight;
137
138 % Plot smallest design
139 figure;
140 [minChipDimension, smallestChipIndex] = min(dimensionArrayCm);
141 [NPadsActual(smallestChipIndex), visualizerArray] = ...
142     generate_visual(outerPadsArray(smallestChipIndex), ...
143     totalRArray(smallestChipIndex),false);
144 visualizerArrayScaled  = plot_visual(visualizerArray, PAD_SIZE, ...
145     topEEPitchArray(smallestChipIndex), 1);
146
147 % Print values of smallest design
148 fprintf('\n');
149 fprintf('<strong>Smallest design will have the following');
150 fprintf(' specifications:</strong>\n');
151 fprintf('Chip size:\t\t\t%4.3f cm\n', minChipDimension);
152 fprintf('Number of pads:\t\t%d \n', NPadsActual(smallestChipIndex));
153 fprintf('Pad size:\t\t\t%d um\n', PAD_SIZE);
154 fprintf('c-c pad pitch:\t\t%d um\n', CCPitchArray(smallestChipIndex));
155 fprintf('Rows:\t\t\t\t%d\n', totalRArray(smallestChipIndex));
156 fprintf('Outer pads:\t\t\t%d\n', outerPadsArray(smallestChipIndex));
157 fprintf('Number of layers:\t%d\n', LAYERS);
158 fprintf('\n');
159
160 if (smallestFullArrayIndex ~= 0)
161 % Plot smallest full-array design
162 figure;
163 [NPadsActual(smallestFullArrayIndex), visualizerArray] = ...
164     generate_visual(outerPadsArray(smallestFullArrayIndex), ...
165     totalRArray(smallestFullArrayIndex),false);
166 visualizerArrayScaled  = plot_visual(visualizerArray, PAD_SIZE, ...
```

```
167     topEEPitchArray(smallestFullArrayIndex), 1);
168
169 % Print values of full-array design
170 fprintf('\n');
171 fprintf('<strong>Smallest full-array design will have the following');
172 fprintf(' specifications:</strong>\n');
173 fprintf('Chip size:\t\t\t%4.3f cm\n', ...
174     dimensionArrayCm(smallestFullArrayIndex));
175 fprintf('Number of pads:\t\t%d \n', NPadsActual(smallestFullArrayIndex));
176 fprintf('Pad size:\t\t\t%d um\n', PAD_SIZE);
177 fprintf('c-c pad pitch:\t\t%d um\n', CCPitchArray(smallestFullArrayIndex));
178 fprintf('Rows:\t\t\t\t%d\n', totalRArray(smallestFullArrayIndex));
179 fprintf('Outer pads:\t\t\t%d\n', outerPadsArray(smallestFullArrayIndex));
180 fprintf('Number of layers:\t%d\n', LAYERS);
181 fprintf('\n');
182
183 else
184     fprintf('<strong>No full-array design in range</strong>\n');
185 end
186
187 clear n tmp c iArray;   % clean output workspace
```

A.3. Generate visual

```
1  %-------------------------------------------------------------------------%
2  % Part of array visualizer for CoF applications as part of my thesis
3  % project titled 'High-density interconnect technology optimised for
4  % flexible implants'.
5  % Full documentation can be found in my thesis report.
6  %
7  % Author:    T.B. Hosman
8  % E-mail:    timhosman@posteo.net
9  % Version:   1.2
10 % Created:   01/08/2019
11 % Modified:  22/08/2019
12 %-------------------------------------------------------------------------%
13
14 function [numberOfPads,visualizerArray,rFull] = ...
15     generate_visual(OUTER_PADS,TOTAL_R,showUnscaled)
16 %GENERATEVISUAL This function is used in combination with the optimizer
17 % script, it generates a matrix of pad locations and sums a number of pads
18 % of the array.
19 %   OUTER_PADS  = int number of pads on one side of chip periphery
20 %   TOTAL_R     = int number of routable rows
21 %   showUnscaled = boolean for showing unscaled visualization (true)
22 %                  or not (false)
23 %   numberOfPads = number of pads of the generated array
24 %   visualizerArray = representation of generated visual. '1' represents
25 %                     array connections. '0' represents no connections.
26 %   rFull       = returns if the array is completely filled or not
27
28 % Check if values are realistic
29 rFull = false;
30 if (ceil(OUTER_PADS/2)>=TOTAL_R) fprintf('Valid visualizer input\n')
31 else
32     warning ('Cannot utilize all rows, incorrect calculations likely');
33     rFull = true;
```

```
    % This will likely cause stray values, calculating higher than desired
    % number of pads on a large area. These will be sub-optimal values.
end

%% Generate initial visualizer array
arraySize = (OUTER_PADS * 2) - 1;
visualizerArray = int8(zeros(arraySize));
for n=1:((arraySize-1)/2+1)
    visualizerArray(2*n-1,1:end) = mod(1:arraySize,2);
end

%% Empty unreachable array area
unreachableRows = OUTER_PADS - 2 * TOTAL_R;
if (unreachableRows > 0)
    %fillerArray = zeros(unreachableRows * 2 - 1);
    fillerStartLoc = 2 * TOTAL_R + 1;
    fillerEndLoc = 2 * (OUTER_PADS - TOTAL_R) - 1;
    visualizerArray(fillerStartLoc:fillerEndLoc, ...
        fillerStartLoc:fillerEndLoc) = 0;%fillerArray;
end

%% Plot visuals
% credit to https://stackoverflow.com/questions/3280705/
% how-can-i-display-a-2d-binary-matrix-as-a-black-white-plot
if (showUnscaled)
    TICK_SIZE = 10; % Set axis tick, larger value -> fewer pad markers
    %visualizerArray = ~visualizerArray;        % To inverse b/w color
    [r, c] = size(visualizerArray);             % Get the matrix size
    imagesc((1:c)+0.5, (1:r)+0.5, visualizerArray); % Plot the image
    colormap(gray);                             % Use a gray colormap
    axis equal                                  % Make axes grid sizes equal
    set(gca, 'XTick', 0:2*TICK_SIZE:(c+1),... % Change some axis properties
             'YTick', 0:2*TICK_SIZE:(r+1), ...
             'XTickLabel', 0:TICK_SIZE:(c+1)/2, ...
             'YTickLabel', 0:TICK_SIZE:(r+1)/2, ...
             'XLim', [1 c+1], ...
             'YLim', [1 r+1], ...
             'GridLineStyle', '-', ...
             'XGrid', 'on', ...
             'YGrid', 'on');

end

%% Return total number of pads
numberOfPads = sum(sum(visualizerArray == 1));

end
```

A.4. Plot visual

```
%-------------------------------------------------------------------------%
% Part of array visualizer for CoF applications as part of my thesis
% project titled 'High-density interconnect technology optimised for
% flexible implants'.
% Full documentation can be found in my thesis report.
%
% Author:    T.B. Hosman
```

```
8  % E-mail:    timhosman@posteo.net
9  % Version:   1.1
10 % Created:   07/08/2019
11 % Modified:  22/08/2019
12 %-------------------------------------------------------------------------%
13
14 function [visualizerArrayScaled] = plot_visual(visualizerArray, ...
15     PAD_SIZE, eePitch, scale)
16 %PLOTVISUAL This function is used in combination with the optimizer script,
17 % it plots a visualizerArray generated by the generate_visual function and
18 % scales to save calculation time if necessary (for very large arrays).
19 %   visualizerArray     = Unscaled array containing '1' for connections and
20 %                         '0' for opens.
21 %   PAD_SIZE            = dimensions of a single pad
22 %   eePitch             = edge-edge distance between pads
23 %   scale               = compression factor, used to downsize large arrays
24
25 %% Determine array size and initialize
26 totalOuterPads = sum(visualizerArray(:,1) == 1);
27 totalPadLength = totalOuterPads * PAD_SIZE;
28 totalPitchLength = (totalOuterPads - 1) * eePitch;
29 arraySize = round((totalPadLength + totalPitchLength) * scale,0);
30 visualizerArrayScaled = int8(zeros(arraySize));
31 pitchPadLength = round(scale * (PAD_SIZE + eePitch),0);
32
33 %% Fill array
34 scaledPad = ones(round(scale * PAD_SIZE,0));
35 unscaledSize = size(visualizerArray,1);
36 for i=1:unscaledSize
37     for j=1:unscaledSize
38         if (visualizerArray(i,j) == 1)
39             xLoc = 1 + (i-1) / 2 * pitchPadLength;
40             yLoc = 1 + (j-1) / 2 * pitchPadLength;
41             visualizerArrayScaled( ...
42                 xLoc:xLoc + round(scale * PAD_SIZE - 1,0), ...
43                 yLoc:yLoc + round(scale * PAD_SIZE - 1,0)) ...
44                 = scaledPad;
45         end
46     end
47 end
48
49 %% Plot visuals
50 % credit to https://stackoverflow.com/questions/3280705/
51 % how-can-i-display-a-2d-binary-matrix-as-a-black-white-plot
52
53 TICK_SCALE = 2;
54
55 [r, c] = size(visualizerArrayScaled);            % Get the matrix size
56 imagesc((1:c)+0.5, (1:r)+0.5, visualizerArrayScaled); % Plot the image
57 colormap(gray);                                  % Use a gray colormap
58 axis equal                                       % Make axes grid sizes equal
59 set(gca, 'XTick', 0:TICK_SCALE*pitchPadLength:(c+1),... % Change some axis
       properties
60           'YTick', 0:TICK_SCALE*pitchPadLength:(r+1), ...
61           'XTickLabel', 0:TICK_SCALE*pitchPadLength/scale:(c+1)/scale, ...
62           'YTickLabel', 0:TICK_SCALE*pitchPadLength/scale:(r+1)/scale, ...
```

```
63            'XLim', [1 c+1], ...
64            'YLim', [1 r+1], ...
65            'GridLineStyle', '-', ...
66            'XGrid', 'on', ...
67            'YGrid', 'on');
68   xlabel('distance [um]');
69   ylabel('distance [um]');
70
71 %end
72
73 end
```

B

Bonding evaluation details

B.1. Criteria explanation

Table B.1: Descriptions of criteria used for bonding evaluation

Criterium name	Description
Reliability, humidity	Degree of resistance to humid environment.
Reliability, thermal	Degree of resistance to thermal cycles.
Reliability, biostability	Degree of mechanical stability.
Reliability, bond	How well bonds can cope with mechanical stress.
Characteristics, contact resistance	Typical resistance of a bond as measured in figure 4.5.
Characteristics, crosstalk sensitivity	Degree of sensitivity to crosstalk.
Characteristics, current capacity	Typical maximum continuous current capacity of a bond.
Characteristics, biocompatibility	Whether all materials in the assembly are considered biocompatible.
Process, chip connection	How the chip is connected to the substrate.
Process, fine-pitch bonding	How much spacing individual connections typically require.
Process, curing temperature	Heating temperature required to cure adhesive.
Process, bonding temperature	Heating temperature required to bond.
Process, bonding pressure	Amount of pressure required to bond.
Feasibility, complexity	Effort required for a single assembly (steps, time, machines).
Feasibility, availability FH	Whether the technique can be applied within Fraunhofer IZM.
Feasibility, experience FH	Whether there is experience within the institute to apply a technique.
Feasibility, cost	Costs for manufacturing and assembling.
Feasibility, adhesive application	Degree of difficulty to apply the adhesive.

B.2. Evaluation table

Table B.2 shows a full list of quantative evaluation results assuming a bonding process with gold a polyimide. A plus (+), circle (o) and minus (-) sign represents how well this technology performs in a specific criterium, where a plus is relatively good and a minus is relatively bad. Some boxes are marked with a question mark, where the result is not quite known or could not be found according to the author's best knowledge. If applicable, some boxes have also been filled with a quantitative value.
Colors in boxes represent to what degree the grade can be of concern. Green marks no complications, yellow marks some complications, red marks a definitive deal-breaker and blue marks any unknown data. **Note** that references in the table refer to the seperate reference list for the evaluation.

Table B.2: Full overview of considered bonding methods.

Type	Bonding	Embedding	Flip-chip TS	Flip-chip TC	Flip-chip US	Flip-chip TS	Flip-chip TC	Flip-chip US	Flip-chip TC			Wire bonding	tape-automated
	Adhesive	NCA		NCA			NCF		ACA	ACF	ICA	None	None
Material	Chip pad	Au	Au	Au	Au	Au	Au	Au	Au	Au	Au	Au	Au
	Substrate pad	Au	Au	Au	Au	Au	Au	Au	Au	Au	Au	Au	Au
	Substrate	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide
Reliability	Humidity	?	+ [2]	+ [2]	+ [2]	?	?	?	?	?	?	?	?
	Thermal	?	o [4]	o [4]	o [4]	?	?	?	o [10]	?	+ [5]	?	?
	Biostability	+	o	o	o	o	o	o	o	o	o	-	o
	Bond	?	+ [19]	+ [19]	+ [19]	+ [19]	+ [19]	+ [19]	?	?	+	+	+
Characteristics	Contact resistance	+ [16]	+ [1]	+ [1]	+ [1]	+ [1]	+ [1]	+ [1]	o [1]	o [1]	<5mΩ	0.38mΩ [26]	0.31mΩ [26]
	Crosstalk sensitivity	+	+	+	+	+	+	+	+	+	+	-	o
	Current capacity	+	+ [12]	+ [12]	+ [12]	+ [12]	+ [12]	+ [12]	o [12]	o [12]	o	+	+
	Biocompatibility	+	+	+	+	+ [27]	+ [27]	?	Ball is Ni/Ag on inside		Ag	+	+
Process	Chip connection	Laser + SAS	Stud/EP	Stud/EP	Stud/EP	Stud/EP	Stud/EP	Stud/EP	Stud/EP	Stud/EP	Stud/EP	Wire	TAB
	Fine-pitch bonding	~60µm [16]	+	+	+	+	+	+	<40µm [8]	<40µm [8]	>127µm [6]	-	50µm 1 row [26]
	Curing temperature	+	65-150°C [23]	65-150°C [23]	65-150°C [23]	+ [27]	+ [27]	?	?	<150°C [21]	85°C [7]	+	+
	Bonding temperature	250°C [16]	150°C [19]	<300°C [19]	Room temp.	150°C [19]	<300°C [19]	Room temp.	180°C [11]	180-220 [21] [2	?	+	300-400°C [26]
	Bonding pressure	+	o [12]	o [12]	o [12]	o [12]	o [12]	o [12]	+ [12]	+ [12]	?	+	o [26]
Feasibility	Complexity	-	- [19]	o [19]	o [19]	- [19]	o [19]	o [19]	- [9]	- [9]	-	+	+
	Availability FH	+	-	+ [25]	+ [25]	-	+ [25]	+ [25]	+ [24]	+ [24]	+	+	?
	Experience FH	o	+	+	?	+	+	?	+ [24]	+ [24]	+	+	?
	Cost	-	o	o	o	o	o	o	o	o	o	+	+
	Adhesive application	o	o	o	o	+	+	+	o	+	-	+	+

B.3. Evaluation table references

1. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 294. NCF>ACF, ACF can be improved with a double-layered film.
2. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 285-288.
3. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 309.
4. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 432. Bad without fillers.
5. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 132.
6. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 134.
7. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 183.
8. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 227.
9. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 230.
10. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 265. Best with polymer CTE close to that of chip and board.
11. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 265.
12. Electrical Conductive Adhesives with Nanotechnologies [44]. p. 279.
16. High-Density Flexible Substrate Technology with Thin Chip Embedding and Partial Carrier Release Option for IoT and Sensor Applications [34].
17. NCA flip-chip bonding with thermoplastic elastomer adhesives [35].
19. Wire Bonding in microelectronics [32]. p. 37. CAREFUL: regarding wire bonding.
21. `https://en.wikipedia.org/wiki/Anisotropic_conductive_film`
22. Interconnection of multichannel polyimide electrodes using anisotropic conductive films (ACFs) for biomedical applications [65].
23. `https://www.masterbond.com/certifications/usp-class-vi`
24. According to Barbara Pahl, Fraunhofer IZM
25. According to Thomas Fritzsch, Fraunhofer IZM
26. `http://www.idc-online.com/technical_references/pdfs/electronic_engineering/Tape_Automated_Bonding.pdf`
27. TPU, acrylic, PI, PTFE

C

Immersion gold thickness reports

Fraunhofer IZM Berlin
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Fischerscope® XRAY XDV-SD
Product: 11 / ENEPIG-FR4-Koll2_2016 **Dir.: 00_Hauptverzeichnis Fischer Block: 328**
Application: 152 / ENEPIG-FR4-Koll2

Auftrags-Nr: **PUembedding**
Los-Nr.: **Au511**
Bemerkung1: **30 min K200**
Bemerkung2: **samples 1/2**

n	Au 1[µm]	Pd 2[µm]	Ni 3[µm]	Cu 4[µm]
1	0.190	-0.001	0.005	15.04
2	0.140	0.003	0.002	16.27
3	0.321	0.013	0.013	16.49
4	0.122	-0.012	0.007	16.77
5	0.369	-0.003	-0.001	16.70
6	0.072	0.006	0.004	17.00
7	0.097	-0.004	0.009	16.12
8	0.118	-0.003	0.005	15.55
9	0.118	-0.001	0.004	15.31
10	0.122	-0.003	0.006	15.24
11	0.126	-0.004	0.007	15.31
12	0.107	-0.007	0.004	15.78
13	0.111	-0.002	0.005	15.42
14	0.106	-0.003	0.004	15.77
15	0.143	-0.005	0.002	15.84

	Au 1	Pd 2	Ni 3	Cu 4
Mean	0.151 µm	-0.002 µm	0.005 µm	15.91 µm
Standard deviation	0.084 µm	0.006 µm	0.003 µm	0.622 µm
Range	0.298 µm	0.026 µm	0.013 µm	1.964 µm
Number of readings	15	15	15	15
Min. reading	0.072 µm	-0.012 µm	-0.001 µm	15.04 µm
Max. reading	0.369 µm	0.013 µm	0.013 µm	17.00 µm
Measuring time	15 sec			

Operator: Schmidt
Date: 24.06.19 Time: 10:25:52

Fraunhofer IZM Berlin
Abt. SIIT

Fischerscope® XRAY XDV-SD
Product: 11 / ENEPIG-FR4-Koll2_2016 **Dir.: 00_Hauptverzeichnis Fischer Block: 329**
Application: 152 / ENEPIG-FR4-Koll2

Auftrags-Nr: PUembedding
Los-Nr.: Au511
Bemerkung1: 30 min K100
Bemerkung2: sample 3/4

n	Au 1[µm]	Pd 2[µm]	Ni 3[µm]	Cu 4[µm]
1	0.184	-0.001	0.008	15.34
2	0.117	-0.010	0.006	15.33
3	0.165	0.015	0.008	15.97
4	0.107	-0.003	0.001	15.59
5	0.165	-0.005	0.007	14.72
6	0.107	0.003	0.006	15.18
7	0.156	0.003	0.009	15.05
8	0.300	0.001	0.007	15.30
9	0.186	-0.003	0.008	15.31
10	0.193	-0.008	0.006	14.85
11	0.116	-0.004	0.006	14.79
12	0.243	-0.001	0.006	15.03
13	0.254	-0.002	0.004	15.16
14	0.228	-0.008	0.005	14.97
15	0.116	0.002	0.006	14.84
16	0.094	-0.002	0.006	14.70

	Au 1	Pd 2	Ni 3	Cu 4
Mean	0.171 µm	-0.001 µm	0.006 µm	15.13 µm
Standard deviation	0.061 µm	0.006 µm	0.002 µm	0.340 µm
Range	0.206 µm	0.025 µm	0.007 µm	1.265 µm
Number of readings	16	16	16	16
Min. reading	0.094 µm	-0.010 µm	0.001 µm	14.70 µm
Max. reading	0.300 µm	0.015 µm	0.009 µm	15.97 µm
Measuring time	15 sec			

Operator: Schmidt
Date: 24.06.19 Time: 10:27:44

D

Flip-chip bonding data

D.1. Au-to-PI bonding data

This section contains all relevant flip-chip bonding data of Au-to-PI samples with the 301-2FL epoxy-based underfill by Epotek bonded with the 8072 chip. Note that all data shows a dip at $5kg$ of force due to a switching error between the low-force ($< 5kg$) and high-force ($5 - 100kg$) sensor, this happens by default in the used flip-chip bonder in high-force applications.

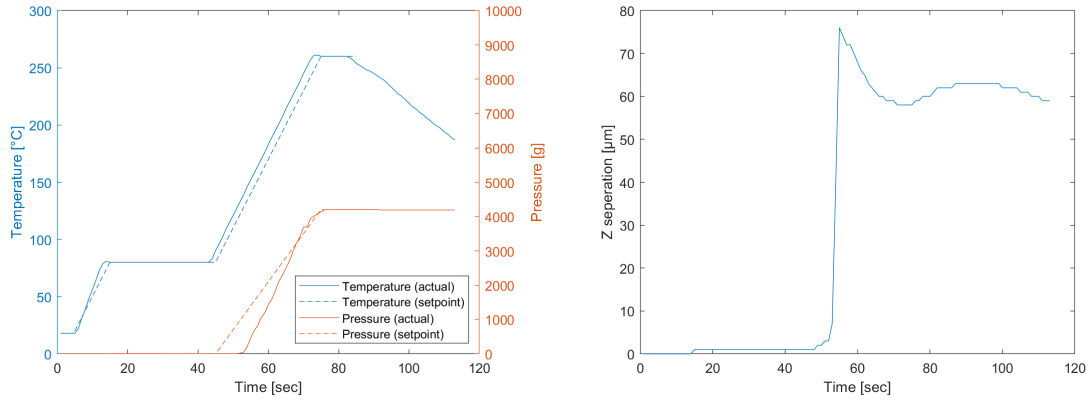

Figure D.1: 8072 NCA sample 1 bonding data

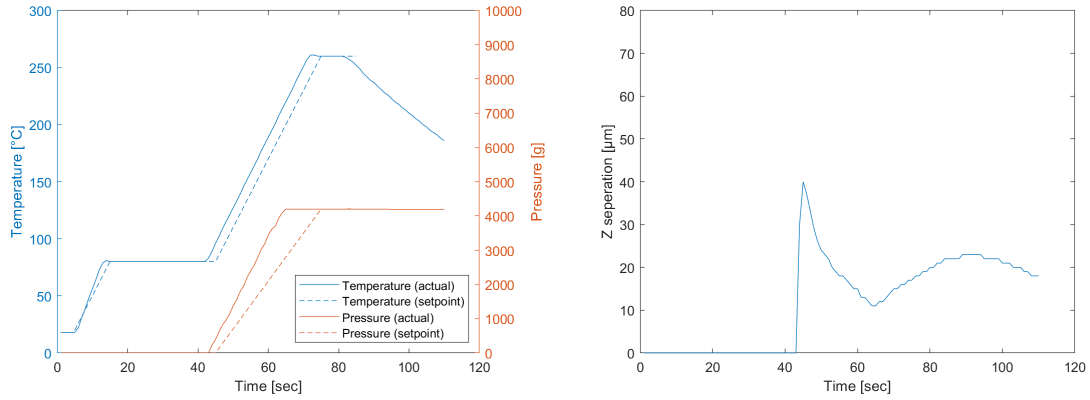

Figure D.2: 8072 NCA sample 2 bonding data

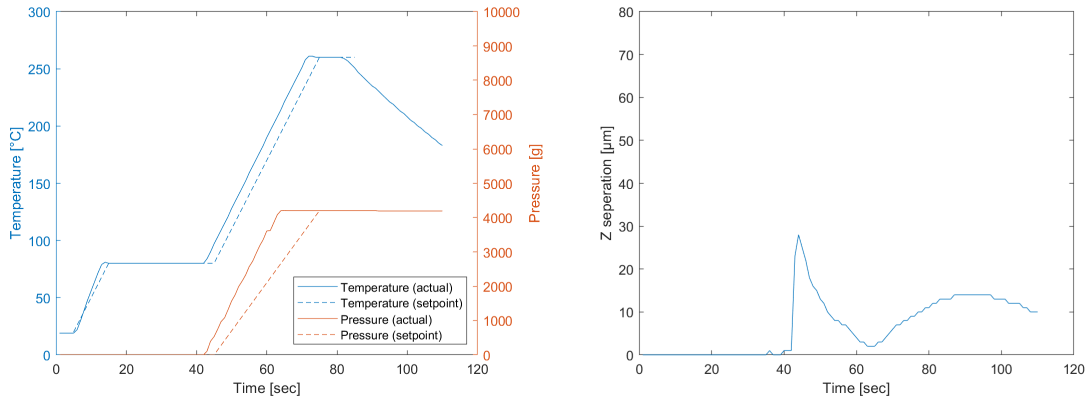

Figure D.3: 8072 NCA sample 3 bonding data

D.2. TPU 361008 bonding data

This section contains all relevant flip-chip bonding data of HD Au-to-TPU samples with TPU underfill bonded with the 361008 chip. Sample 16 and 17 were 361008F samples and can be found in section D.3.

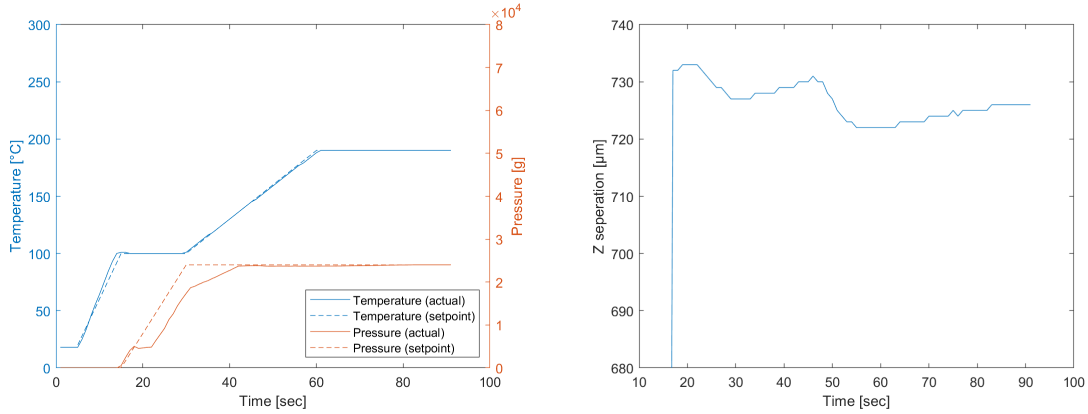

Figure D.4: 361008 TPU sample 1 bonding data

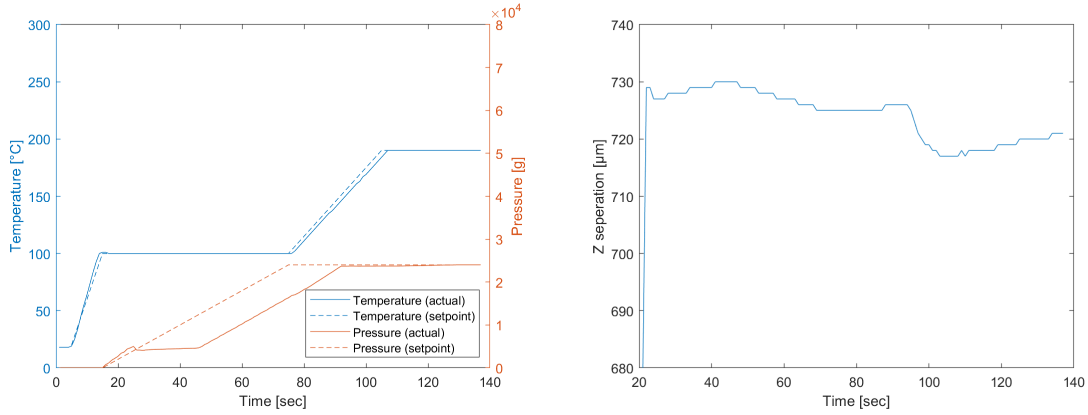

Figure D.5: 361008 TPU sample 2 bonding data

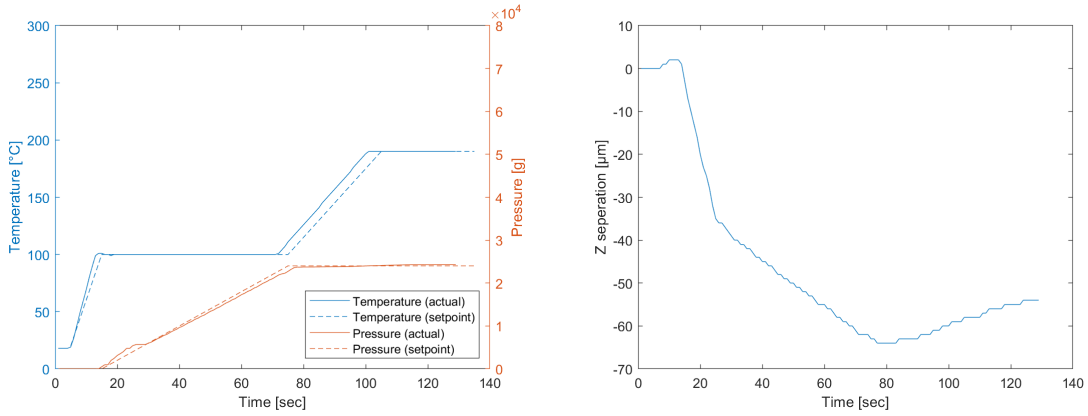

Figure D.6: 361008 TPU sample 3 bonding data (failed to bond)

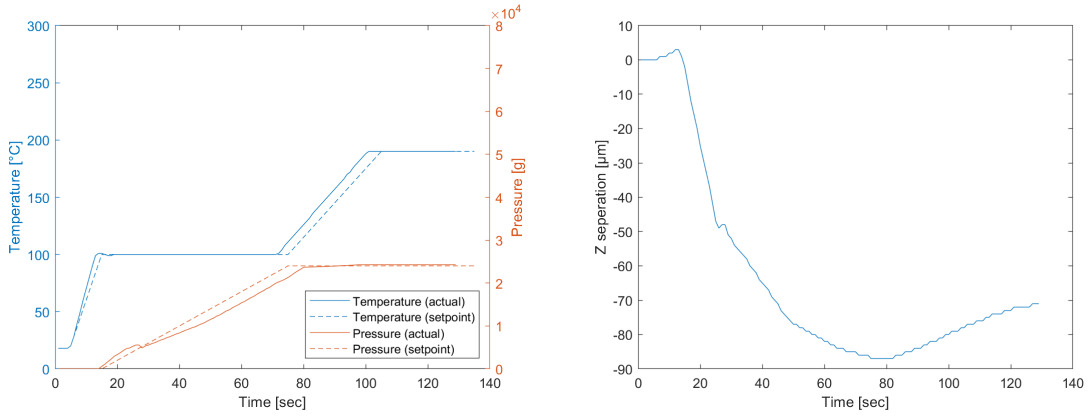

Figure D.7: 361008 TPU sample 4 bonding data (failed to bond)

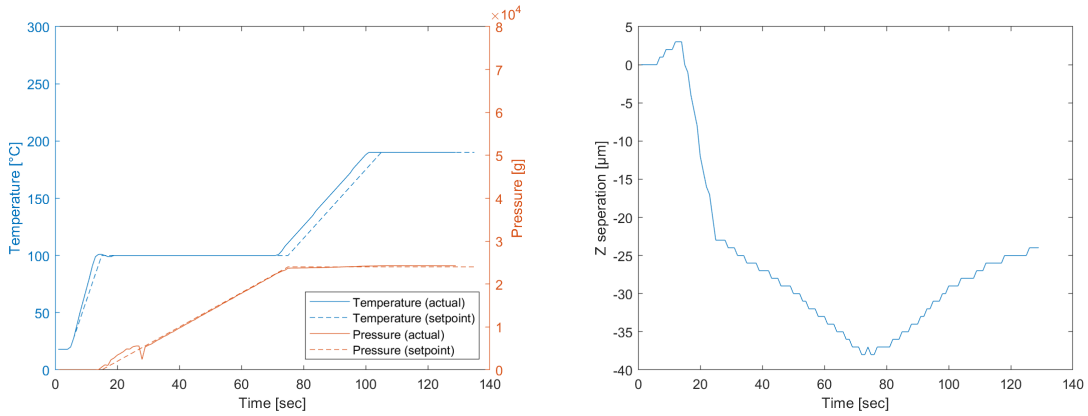

Figure D.8: 361008 TPU sample 5 bonding data (failed to bond)

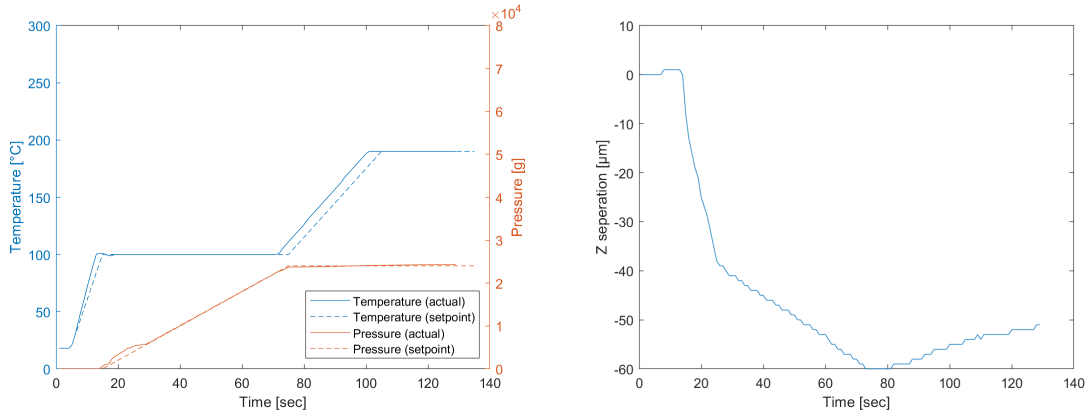

Figure D.9: 361008 TPU sample 6 bonding data (failed to bond)

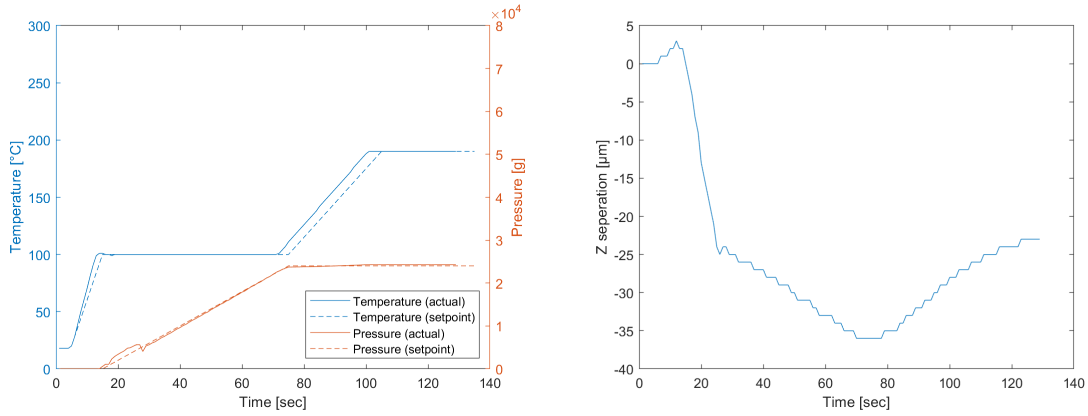

Figure D.10: 361008 TPU sample 7 bonding data (failed to bond)

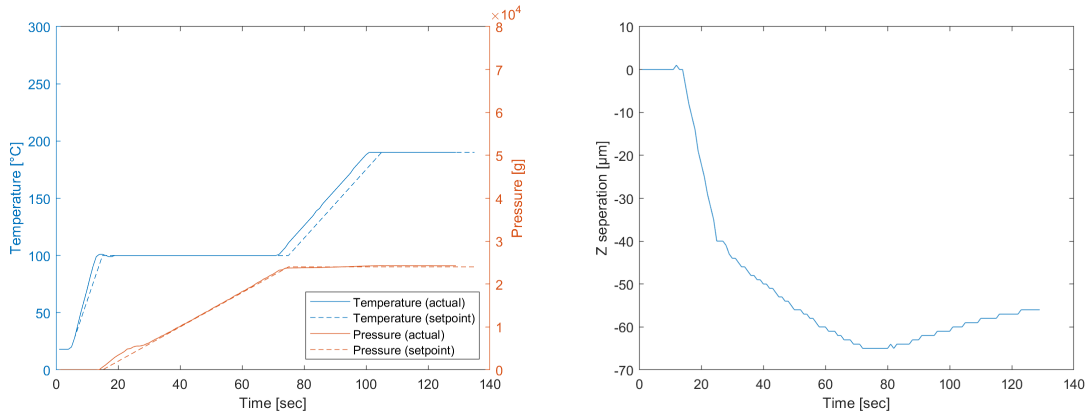

Figure D.11: 361008 TPU sample 8 bonding data (failed to bond)

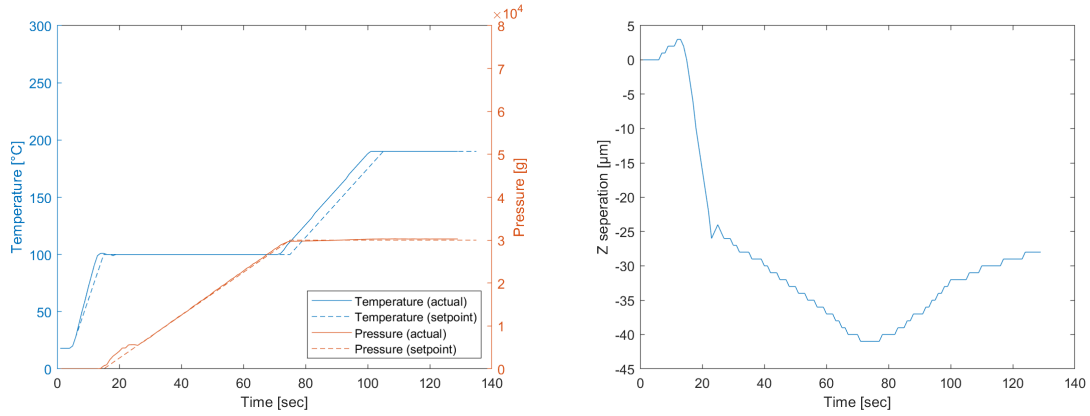

Figure D.12: 361008 TPU sample 9 bonding data (failed to bond)

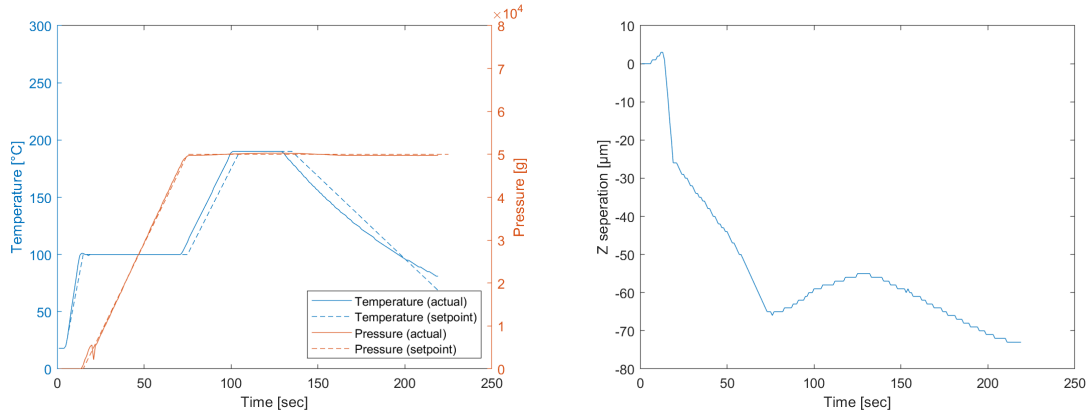

Figure D.13: 361008 TPU sample 10 bonding data (failed to bond)

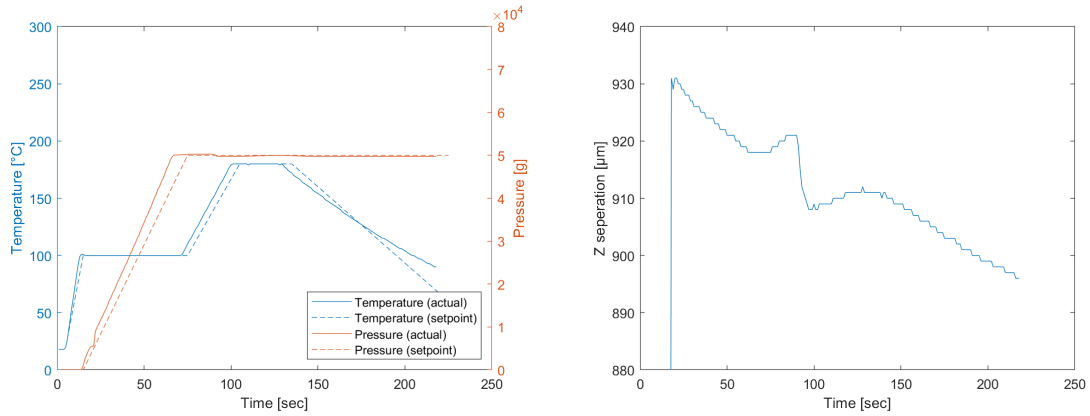

Figure D.14: 361008 TPU sample 11 bonding data

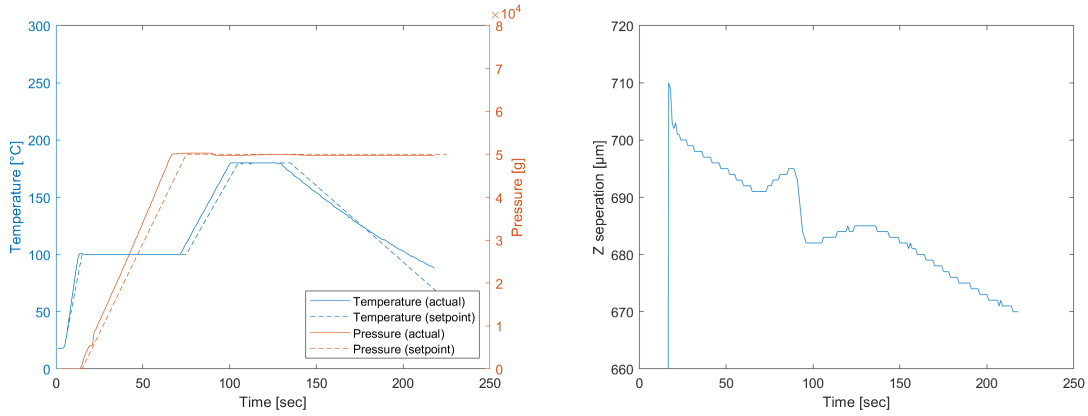

Figure D.15: 361008 TPU sample 12 bonding data

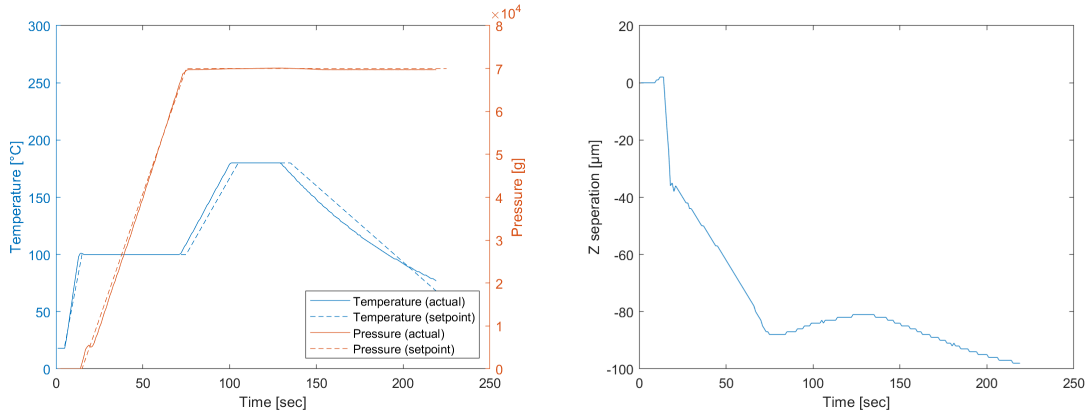

Figure D.16: 361008 TPU sample 13 bonding data (failed to bond)

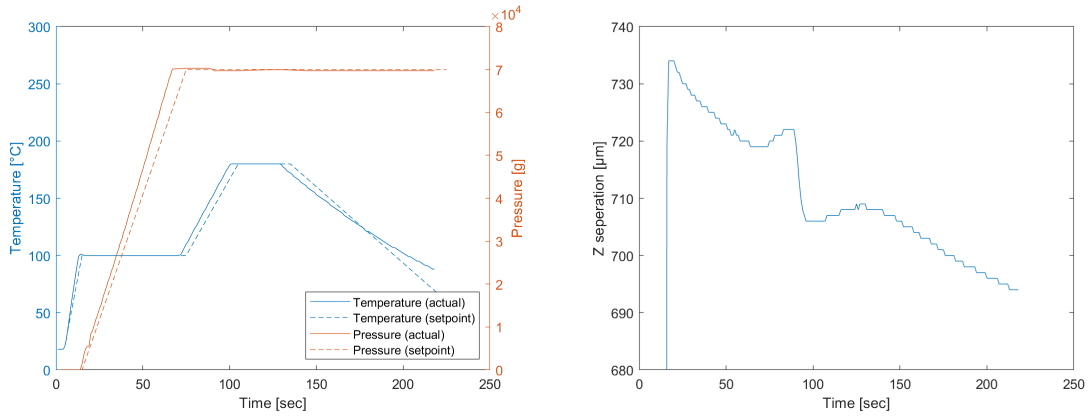

Figure D.17: 361008 TPU sample 14 bonding data

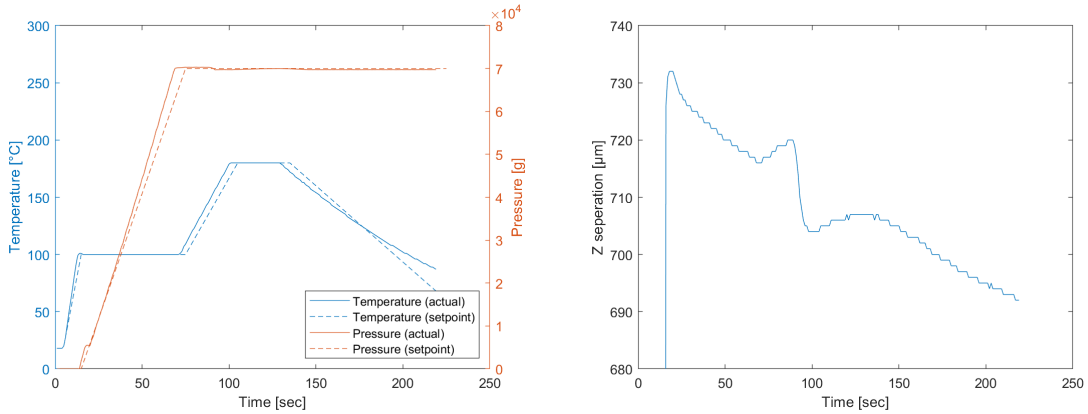

Figure D.18: 361008 TPU sample 15 bonding data

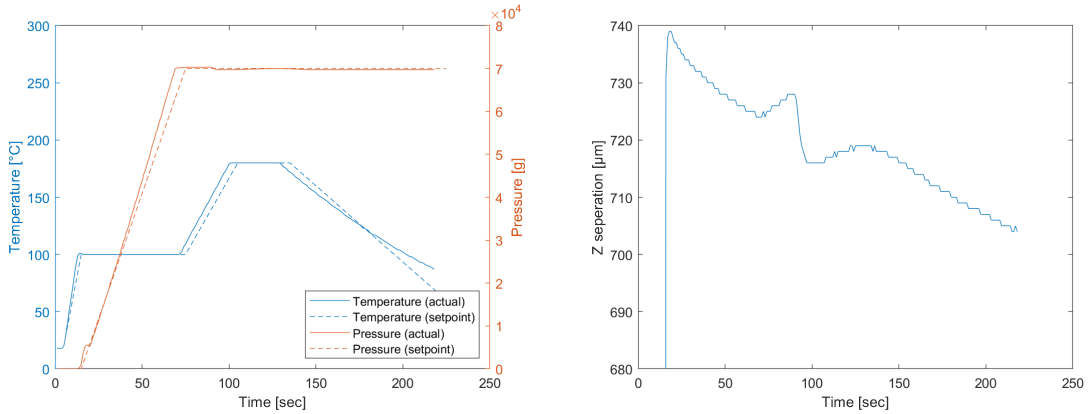

Figure D.19: 361008 TPU sample 18 bonding data

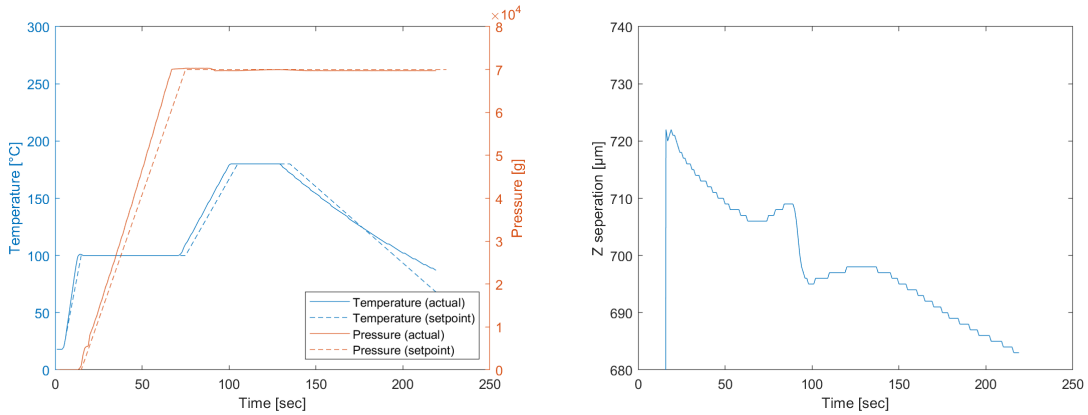

Figure D.20: 361008 TPU sample 19 bonding data

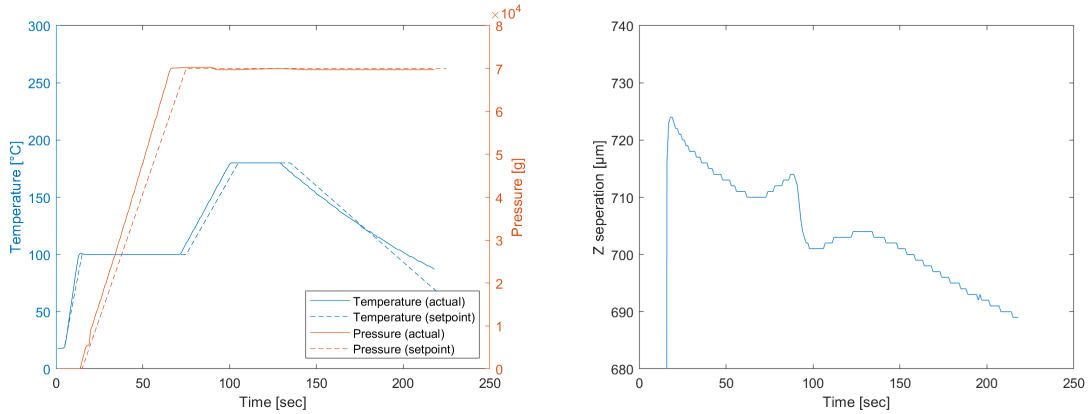

Figure D.21: 361008 TPU sample 20 bonding data

D.3. TPU 361008F bonding data

This section contains all relevant flip-chip bonding data of 324-electrode demonstrator samples with TPU underfill bonded with the 361008 chip. Note that all data shows a dip at $5kg$ of force due to a switching error between the low-force ($<5kg$) and high-force ($5-100kg$) sensor, this happens by default in the used flip-chip bonder in high-force applications.

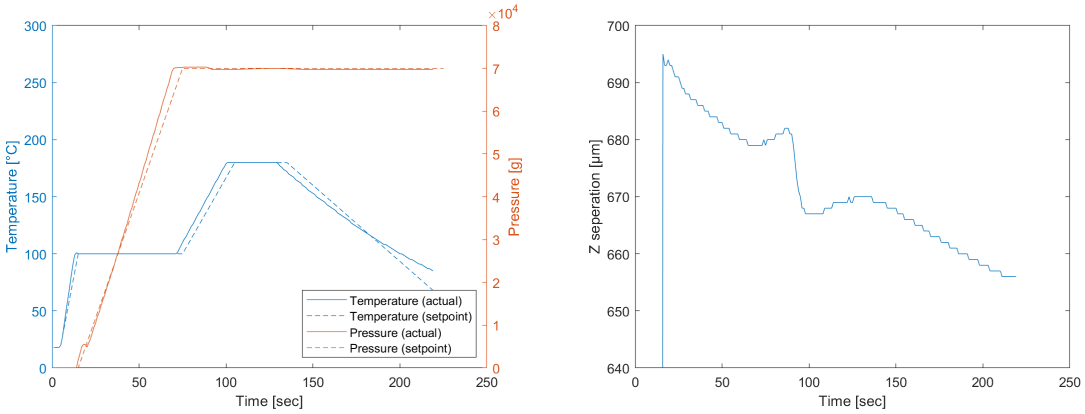

Figure D.22: 361008F TPU sample 1 bonding data

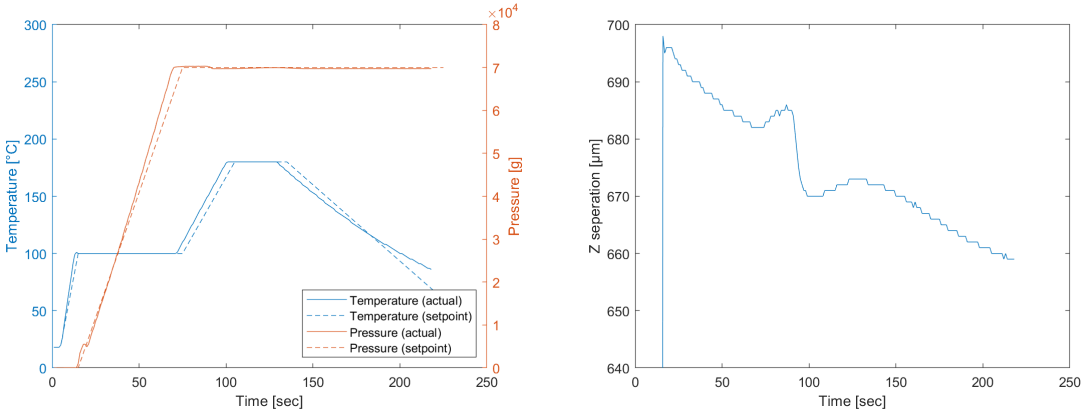

Figure D.23: 361008F TPU sample 2 bonding data

E

Wafer-level multilayer build-up process concept

A concept workflow was developed during this thesis which describes a wafer-level process to manufacture an embedded multilayer polymer substrate with integrated chip. It was discarded due to the pricing of required masks and required wafer surface, but remains a valid concept to investigate. Advantages include the access to clean, highly accurate and regulated processes of wafer-level processing and full flexibility with respect to material options. The process is based on the F2R method developed by Velea [62].

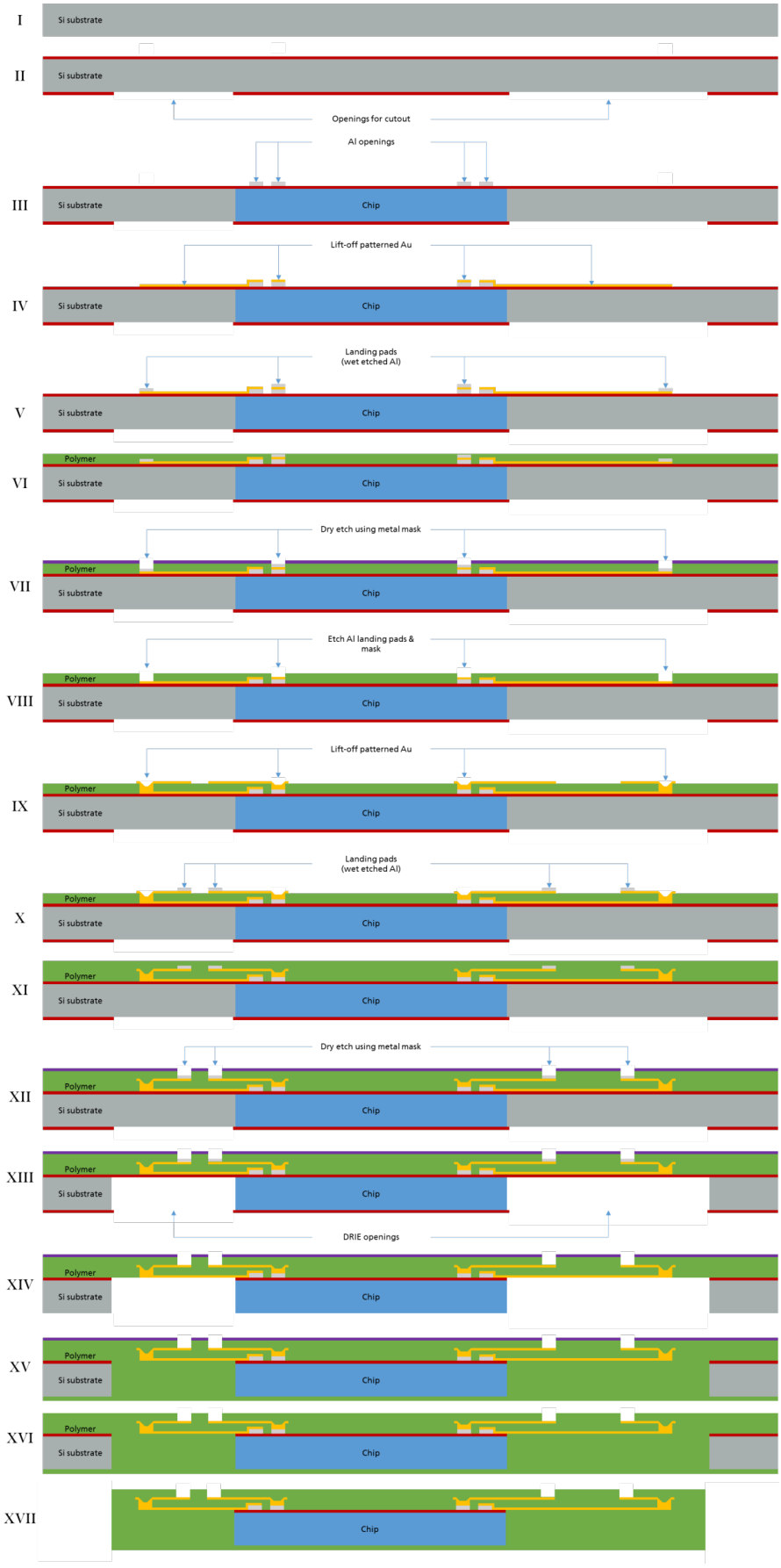

Figure E.1: Wafer-level production concept for an embedded multilayer polymer implant with integrated chip based on the F2R method described by Velea [62].

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