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DOI
10.1109/ARFTG.2019.8739197

Publication date
2019

Document Version
Final published version

Published in
2019 93rd ARFTG Microwave Measurement Conference

A TRL Error-box Split Procedure to Compensate for the Bias Dependency Effects in Device Test-Fixtures

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***Abstract* — In this paper we present a method to alleviate the errors introduced by the bias dependency of the electrostatic discharge or antenna-effect protection diodes when a direct metal-one TRL calibration is employed. The proposed method shows that the two error-boxes produced by the TRL algorithm can be split and combined without introducing mathematical errors as long as the perturbation can be assumed to be a reciprocal network. A mathematical analysis is provided and initially bench marked against a circuit level simulation employing only s-parameter defined error boxes and ideal lumped components and after verified using 3D EM simulations of the test fixtures. The circuit level simulator confirms the mathematical analysis while the 3D EM simulator validates the applicability in a more realistic setting. Finally, the proposed method is used in a real measurement where the test fixture are implemented in a 28nm CMOS technology and characterized at frequencies between 140 GHz to 200 GHz. The measurement using the proposed method clearly shows reduced deviation from known reference when compared to the non-split approach.**

***Index Terms* — mm-wave, ESD, on-wafer, Antenna effect, S-parameters, TRL calibration**

I. Introduction

Recent years have seen a considerable increase of the commercial interest in applications operating in the mm-wave and sub-mm-wave frequency bands. The reason for this is twofold, on one side the technology performance improvement have provided sufficient capabilities also in low-cost (i.e., silicon based) technologies. On the other side the frequency congestion occurring in conventional (i.e., below 6GHz) telecom bands has pushed to look for new available spectrum for broadband applications. Nevertheless, to reduce the design iterations and time to market of mm-wave integrated systems, it is necessary to accurately characterize and model the devices that form the core building blocks of these circuits, i.e., the transistors. The mentioned model accuracy improves predictability and thus reduces the number of iterations needed to reach the targeted performance levels.

Recent years have shown many studies and improvements in the measurement setups and calibration/de-embedding procedures to increase the accuracy and reliability of mm-wave S-parameters measurements [1][2][3]. Nevertheless, when considering state-of-the-art CMOS technologies, the reduced device parasitic highlight potential difficulties when using these approaches that were not evident in larger footprint (i.e., large parasitic components) devices. Part of these limitations are related to the de-embedding/calibration procedure which sets most of the accuracy limitation in the device S-parameters measurements [1][4].

The calibration procedure provides the mean to accurately place the measurement reference planes at a given location, by first measuring the imperfections of the setup and then mathematically removing these, up to that particular reference plane. When aiming for device modelling the above mentioned reference plane should be placed as close as possible to the (intrinsic) device under test (DUT).

Placing the reference plane close to the device has always been a challenging quest, which is even augmented by the frequency increase up to the mm-wave range. This procedure, often defined as second-tier or de-embedding step, has continuously improved in the last thirty years from [5] to [6] (among many contributions) until recent with [7] where a direct "Thru-Reflect-Line" (TRL) calibration/de-embedding procedure was demonstrated building all the standards at metal 1 (M1) in close proximity to the (intrinsic) DUT.

Calibration procedures work by producing a set of error-terms (ETs) that compensate for the imperfections present in the measurement setup. These ETs are usually considered constant during the calibration and the measurement phases and in most cases this is true (a part the inevitable drift). In this contribution we consider the specific case (one among probably others) in which the ETs vary with the bias conditions applied to the DUT. The analyzed case occurs when a direct M1 calibration is employed to measure devices where electrostatic discharge (ESD) [8] or antenna protection diodes are embedded in the fixture. This condition leads to a bias dependent error in the calibration procedure, which becomes more evident with the reduction of the parasitic elements of the intrinsic device, i.e., when the DUT parameters become comparable to the bias induced variation of the ESD/antenna-protection diode.

In this paper we present a calibration procedure, denoted as "split TRL" to remove the bias dependency of the test-fixture when a TRL direct calibration/de-embedding method is employed. The proposed solutions is obtained by combining two different error box T_A (at port 1) and T_B (at port 2) computed from two different bias condition cases. After introducing the mathematical base of the spilt and re-combination of the TRL error boxes we validate its usability employing a circuit level simulation (Keysight ADS) where

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S-parameter defined error boxes are used. Then, a 3D EM-simulation (CST microwave studio) using accurate model of the device fixture and finally measurements on devices realized in a 28nm CMOS technology from 140 GHz to 200 GHz, are employed to validate the approach in a realistic environment.

II. ESD DIODES AND ITS EFFECTS ON THE MEASUREMENTS

In order to survive both the fabrication process as well as machine and human handling during assembly, integrated devices need to be protected by special structures (i.e., diodes). These structures are then capable of routing the electro-static discharge event away from the device areas which would not withstand those sudden high voltage events.

For this reason, it is recommended to insert the ESD protection device in the proximity of the DUT.

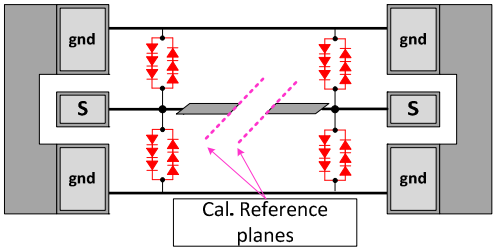
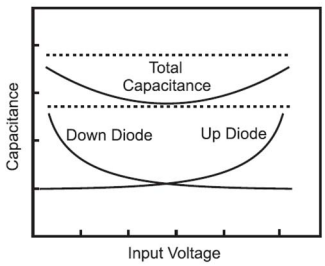


Fig. 1. Simplified representation of the fixture with embedded ESD protection devices (shown in red).

This contribution employs an NMOS fabricated in a 28nm CMOS technology and embedded in a TRL compatible fixture for verification of the proposed approach. The calibration/de-embedding procedure is based on a M1 level Thru, Reflect Line following the method presented in [7]. As shown in Fig. 1, the ESD protection consists of a six-diode antiparallel configuration, with three diodes in series in each branch, placed symmetrically in both sides of the line (at M1) connecting the DUT . It is important to note that although the ESD protection diodes are designed to operate only in case of an electrostatic discharge event, their impedance (capacitance) is bias depend. This dependency comes partly from the junction capacitance variation of the diodes as shown in Fig. 2 [8] where the contribution of the two diode branch of Fig. 1 are summed.



$$C_j(V) = \frac{C_o}{\left[1 - \frac{V}{V_o}\right]^{1/2}}$$

Fig. 2. Expected capacitance variation of the ESD protection diode due to the sum of the two branch Cj variation [8].

The effect of the diode impedance variation can also be observed directly in the measurements. In Fig. 3 the S21 variation over bias of a thru line embedded in the considered fixture is shown. The line response which would be constant without the presence of diodes, changes when the voltage on the fixture is modified. A variation of more than 0.1 dB, see Fig. 4, is observed varying the voltage from 0 V to 2.5 V at 180 GHz.

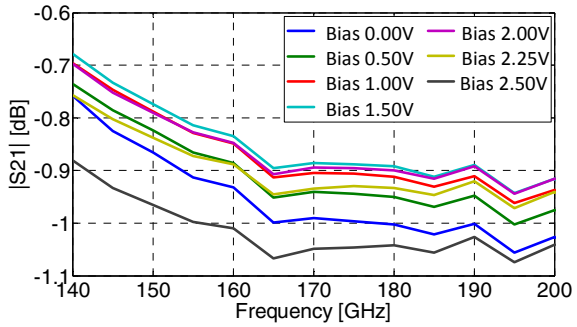


Fig. 3. Measured S21 over a thru line embedded in the fixture at different bias levels.

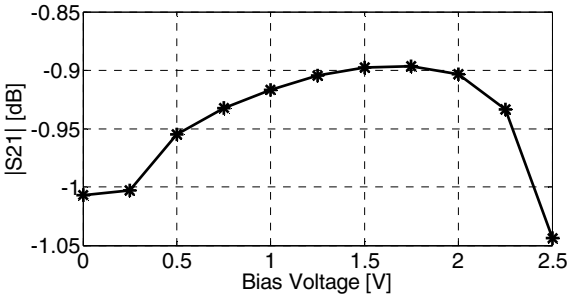


Fig. 4. Variation of |S21| of the thru line embedded in the fixture changing the voltage at 180 GHz.

III. SPLIT TRL

The TRL calibration algorithm allows calculating the error-terms in the form of T-matrixes, T_A and T_B (Fig. 5), by measuring three standards, a thru connection, a symmetric reflect and a line.

When the ESD protection diodes are placed inside of the fixtures its perturbation and its dependency with the applied voltage translates into error boxes that become bias dependent. If the voltage is the same on the two ports the dependence does not influence the measurements. In this case it is indeed possible to perform the calibration directly at those voltage values (port 1 and port 2) using an "open" as reflect and applying the same (bias) conditions used during the calibration in the measurement phase.

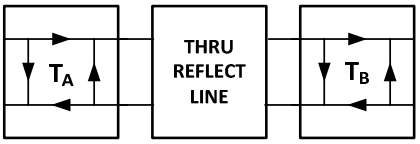


Fig. 5 Graphical representation of the 8-terms error model.

Usually, this condition (symmetric port1 and port2 bias) cannot be met in every case, for example, when measuring an active device it can be required to apply different voltages at the various terminals. In this case a deviation on the original calibration is created which can be mathematically model as an additionally error box that represents the perturbation component. The resulting discrepancy can be removed by combining the two error boxes obtained performing the calibration at two different bias points, this is true provided that the perturbation is caused by a reciprocal network, as can be shown by the following mathematical analysis.

The two T-parameters matrixes of the error-boxes can be written using S-parameters notation, employing the well-known conversion formulas, leading to eq. (1) and eq. (2)

$$T_A = \frac{1}{S_{21}^A}\begin{bmatrix} -\Delta & S_{11}^A \\ -S_{22}^A & 1 \end{bmatrix} = K^A R_n^A \tag{1}$$

$$T_B = \frac{1}{S_{21}^B}\begin{bmatrix} -\Delta & S_{11}^B \\ -S_{22}^B & 1 \end{bmatrix} = K^B R_n^B \tag{2}$$

Where R_n^A and R_n^B are the two normalized T-matrixes and K^A and K^B are two coefficients that are equal to $1/S_{21}^A$ and $1/S_{21}^B$, respectively, in case the error-boxes are reciprocal. The TRL algorithm provides the matrixes R_n^A and R_n^B and the product $K^A \cdot K^B$ [9]. As such, after some mathematical manipulation of eq. (1) and eq. (2) one can isolate K^A and K^B individually, resulting in eq. (3)and eq. (4), respectively.

$$K^A = \frac{1}{\sqrt{S_{12}^A \cdot S_{21}^A}} \tag{3}$$

$$K^B = \frac{\sqrt{S_{12}^A \cdot S_{12}^A}}{S_{21}^A \cdot S_{21}^B} \tag{4}$$

Considering the calibration scenario with a perturbation added on port1 (T_P) as given in Fig. 6,Where

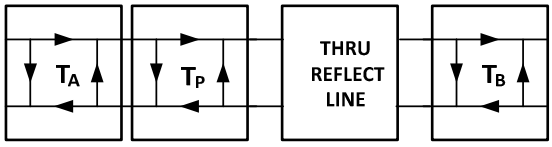


Fig. 6 Calibration scenario with perturbation box

the transmission matrix T_P of the perturbation can be described in terms of its S-parameters as eq. (5).

$$T_P = \frac{1}{S_{21}^P}\begin{bmatrix} -\Delta & S_{11}^P \\ -S_{22}^P & 1 \end{bmatrix} \tag{5}$$

In this new scenario eq. (3) and eq. (4) can be written as eq. (6) and eq. (7).

$$K^A = \frac{(S_{12}^A \cdot S_{21}^A - 1)}{\sqrt{S_{12}^A \cdot S_{21}^A \cdot S_{12}^P \cdot S_{21}^P}} \tag{6}$$

$$K^B = \frac{\sqrt{S_{12}^A \cdot S_{21}^A \cdot S_{12}^P \cdot S_{21}^P}}{S_{21}^A \cdot S_{21}^B \cdot S_{21}^P} \tag{7}$$

From eq. (7) it is possible to observe that if the component that represent the perturbation is reciprocal ($S_{12}^P = S_{21}^P$) K^B is equal to the one in the eq. (4), i.e., no perturbation.

In order to finally conclude that T_B is equal in both of the two previous cases, it is still required to demonstrate that R_n^A and R_n^B are independent. However given that T_A(eq.(1)), T_B(eq.(2)), and T_P (eq.(5)), and using the TRL equations (eq. 40, 41 and 46 from [9]) the independency of the two renormalized matrixes from the perturbation immediately come out.

Therefore it is possible to conclude that when T_P is reciprocal the matrix T_B calculated with and without perturbation are the same and thus independent from what is present at port 1. This mathematical demonstration shows that performing two different calibrations at the respective device operating voltage values (Fig. 7), it is allowed to combine their two error boxes (Fig. 8) without introducing an error in the measurement.

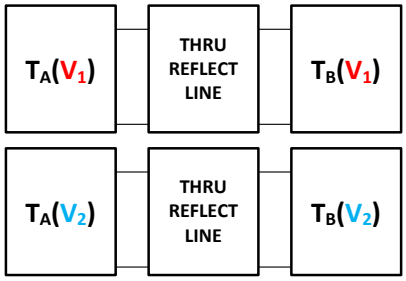


Fig. 7 Calibration scenario at two different bias voltages (V_1 and V_2).

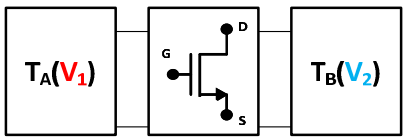


Fig. 8 Measurement scenario employing the split TRL. The error-boxes coming from two different calibrations performed at different bias points are combining

IV. Simulation Setups and Results

To validate the proposed split TRL technique a set of simulations have been performed. First an ADS simulation has been carried out. This simulation consists of two sources, two error boxes with a set of given S-parameters that would represent the measurement setup without any ESD protection diode effect. Two capacitances are then added to the schematic to include also the ESD diode (bias dependent) perturbation (Fig. 9).

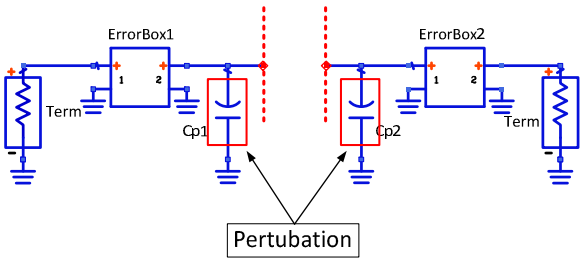


Fig. 9 ADS simulation using as perturbation in the fixture two capacitances that would represent the bias dependent ESD protection diode effect.

The verification consists of the 3 steps:

- A first TRL calibration using the same value (Cp1=Cp2=C_1) of capacitance for both components is performed. This would be representing the two ESD protection diodes at the same voltage value (V_1).
- A second TRL calibration using the same value (Cp1=Cp2=C_2) of capacitance for both components is then carried out. This would be representing the two ESD protection diodes at the same voltage value (V_2).
- The two calibrations are then combined to correct a simulation on the known S-parameters block where the first value of capacitance is used for port 1 and the second one for port 2 (Cp1=C_1 and Cp2=C_2).

For this simulation two different capacitance values have been used: C_1=1 fF and C_2=5 fF. Those values of capacitance are assumed to represent realistic values for the parasitic capacitance of the ESD or antenna protection diode in a fixture for the WR5 frequency band. The results of this simulation is that the proposed approach does not introduce any error, as expected.

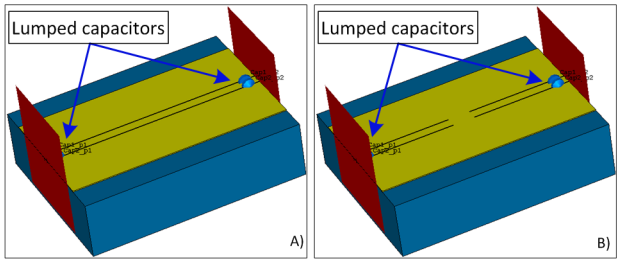


Fig. 10 3D design of the standard loads in CST: A) Thru/Line/Dut; B) Short.

To validate the technique in a more realistic environment and to check if some parasitic effect can influence the results, 3D EM simulations are performed using CST microwave studio (Fig. 10) in the frequency range 75-325GHz. To simplify the structures a CPW in vacuum ($\varepsilon_{r=1}$) is considered to build the standards necessary for the TRL algorithm. The ESD protection diodes is included in the simulation by placing two lumped capacitors (through the usage of lumped ports), with the same value, symmetrically to the line for each port, as shown in Fig. 10. In order to be consistent the same procedure and the same capacitance values considered for the ADS analysis are used.

The result, shown in Fig. 11 as the maximum deviation of all the two-port S-parameters from the reference (Worst Case Error Bound), shows clearly that in case of a non-accounted (standard TRL) perturbation (i.e., ESD protection diode capacitance variation) an error arises in the fixture removal performed by the calibration. Moreover, it shows that, in case a split TRL is used, an error comparable with the one achievable using the TRL calibration in the mm-wave frequency range is expected.

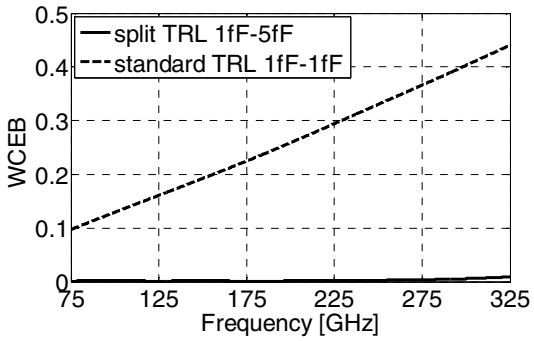


Fig. 11. WCEB obtained using a TRL split technique (solid line) and using a standard TRL calibration (dashed line).

V. Experimental Results

In order to experimentally validate the proposed (split TRL) procedure first a reference measurement needs to be defined. A direct TRL, i.e., with the desired bias value (V_1 at port 1 and V_2 at port 2) at the M1 calibration (M1 Cal) planes (see Fig. 12) is not possible. This is due to the requirement of using a thru and line connection, which impose to have the same port voltages, during the calibration. Moreover note, that using the zero bias value of the open standard as a constant reference device, is also not possible since the substrate cross talk varies versus bias. For the above mentioned reasons the Pads calibration (Pad Cal) planes was used to obtain the reference measurement to validate the procedure using as bias condition V_1=1.5 V and V_2=0 V. The following steps describe the experimental validation procedure:

1. Perform a Pad Cal at zero bias. Note that this calibration does not contain any ESD protection device and its accuracy is independent on the applied bias.
2. Perform two M1 Cal at V_1= V_2=1.5 V (split TRL) and V_1= V_2=0 V (standard TRL).
3. Use the Pad Cal and M1 Cal to calculate the two T-matrixes (Fix_A and Fix_B) for the condition V_1=1.5 V and V_2=0 V (Fig. 12a.) and for the V_1= V_2=0 V.
4. Obtain the S-parameters of the open at the pads using the Pad Cal with V_1=1.5 V and V_2=0 V (Fig. 12b.), i.e., reference data
5. Obtain the S-parameters of the open at M1 using the split TRL technique with the same voltage settings of step 4 (Fig. 12c).

6. De-embed the fixtures by using the relative T-matrixes ($Fix_A(V_1)$ and $Fix_B(V_2)$), calculated in step 3, from the S-parameters obtained in step 5 to find the S-parameters of the open at the pads (Fig. 12d).
7. Finally, calculate the S-parameters at the pads using the same procedure in the step 6 but with the T-matrixes at 0V (standard TRL).

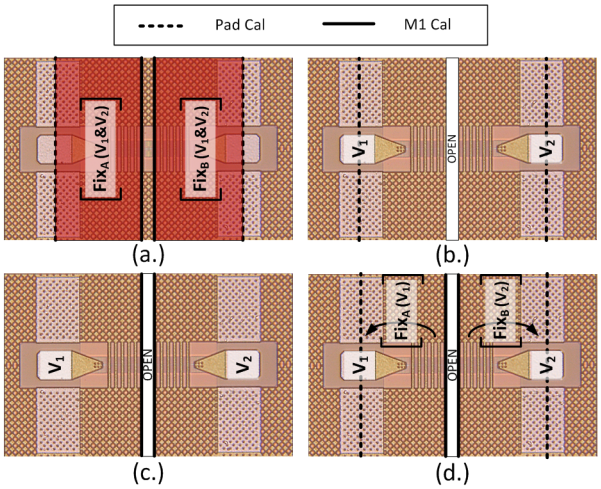


Fig. 12. Measurement verification steps. (a.) M1 Cal and Pad Cal are used to calculate the fixtures at two different bias voltage. (b.) Pad Cal is used to get the reference. (c.) M1 Cal is used to obtain the measurements of an open at different bias voltages directly to M1; (d.) The fixtures are de-embedded from the measurements at M1.

Fig. 13 shows the S11 and the S22 for the case computed from step 6 (split TRL) and step 7 (standard TRL) compared with the reference measurement at the pads computed from step 4.

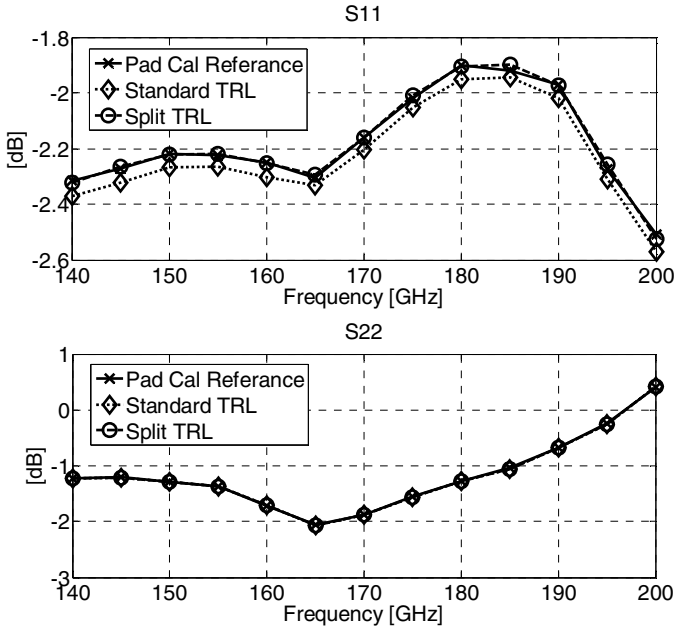


Fig. 13 Reflection parameters at the pads obtained using the TRL split and the standard 0-bias calibration compared with the reference measurement at the pads.

As it can be seen from the figure the S11 obtained using the split TRL approach is basically on top of the reference (step 1) showing only a small error due to the fact that two different calibration are employing. Instead, the S11 computed from the standard TRL performed at zero bias shows an evident deviation from the reference. Since the bias at port 2 doesn't change in both case the S22 doesn't show an error as was expected.

VI. Conclusion

In this paper we presented a strategy to remove the error that the ESD protection diode can causes during device characterization. This error is due to dependency of the ESD protection diode parameters from the different bias voltages applied on the fixtures, when a direct M1 calibration is used. The strategy consists of combing the error-terms boxes calculated performing a TRL algorithm at different voltages in one set of the error-terms. After a mathematical demonstration the technique has been validated with a circuit level simulation that shown no errors and then using a 3D EM simulation that shown an error comparable with the one achievable using the TRL calibration in the mm-wave frequency range. Finally measurements on an passive structure (i.e. Open) are presented to experimentally validate the proposed method. The split TRL technique enables to employ direct calibration/de-embedding techniques also in the characterization of extremely low parasitic devices, as state-of-the-art CMOS and future nano-devices.

Acknowledgement

This research is supported by the Dutch Technology Foundation STW (project 13325), which is part of the Netherlands Organization for Scientific Research (NWO), and which is partly funded by the Ministry of Economic Affairs. The authors would like to thank NXP semiconductors for providing technology access.

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