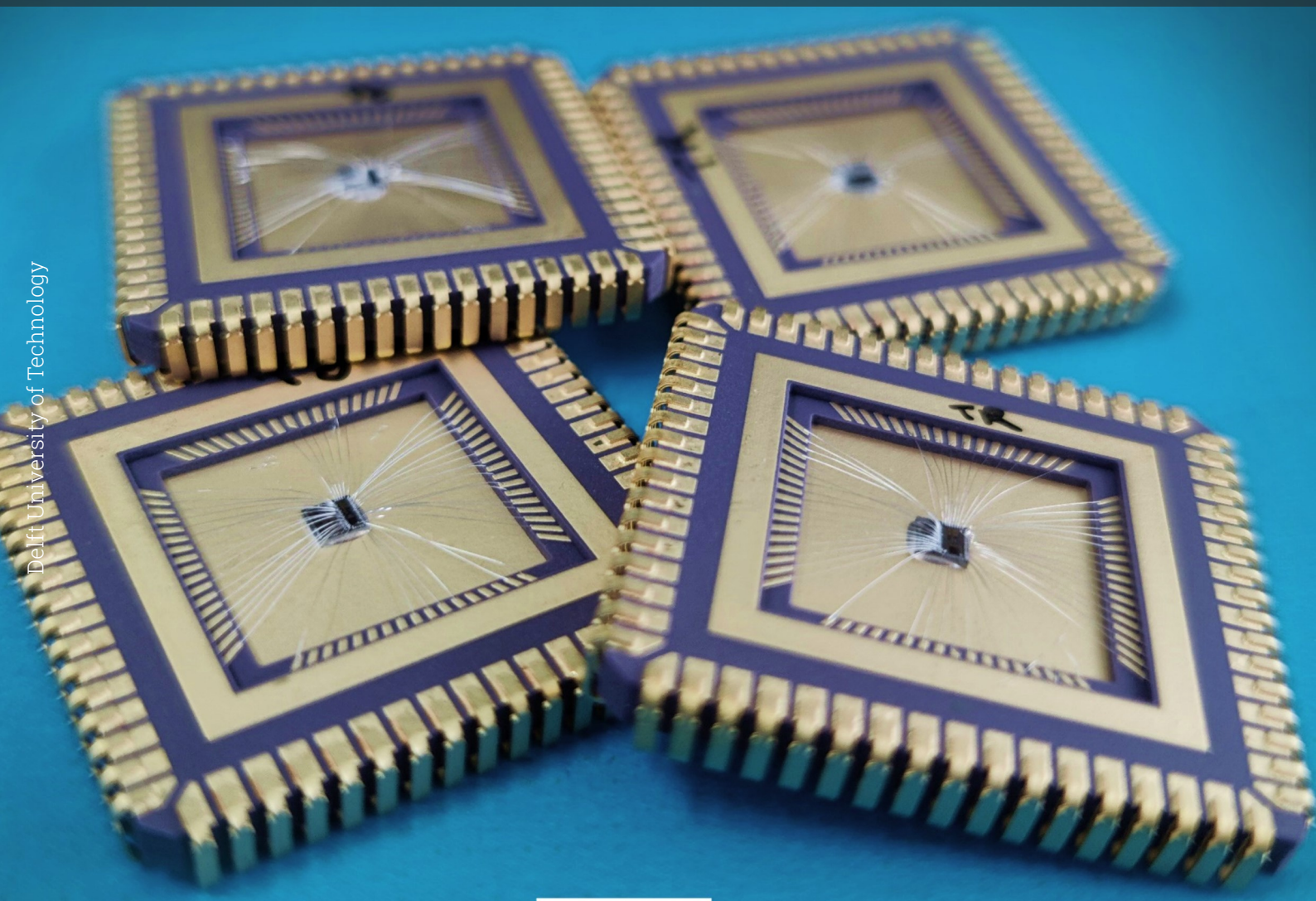
A Programmable Energy Recycling Resonant Pulser for Miniature Wearable Ultrasound Applications

Towards portable ultrasound diagnostics

Imad Bellouki



Delft University of Technology

TU Delft

A Programmable Energy Recycling Resonant Pulser for Miniature Wearable Ultrasound Applications

Towards portable ultrasound diagnostics

by

Imad Bellouki

To obtain the degree of Master of Science in Microelectronics
at the Delft University of Technology,
to be defended publicly on Wednesday December 6th, 2023

Student number:	4920376	
Project duration:	August 15, 2022 - December 6, 2023	
Thesis committee:	dr. ir. M.A.P. Pertijs,	TU Delft, supervisor
	dr. T. Costa,	TU Delft
	N. Rozsa,	TU Delft

TU Delft

Note of publication

The work described in this thesis has at the time of writing been accepted for publication as a conference paper for the ISSCC 2024 conference. The paper titled:

"A Resonant High-Voltage Pulser for Battery-Powered Ultrasound Devices"
Authors: Imad Bellouki[1], Nuriel Rozsa[1], Zu-yao Chang[1], Zhao Chen[1],
Mingliang Tan[1,2], Michiel Pertijs[1]

[1]Delft University of Technology, Delft, The Netherlands, [2]SonoSilicon, Hangzhou, China

was part of the session titled "Imagers and Ultrasound". The published work presents the same measurement results of the ASIC provided in this thesis.

Abstract

This work presents an ASIC designed for portable (wearable) ultrasound (US) imaging systems. The ASIC presents a new type of energy-efficient high-voltage (HV) transmit pulser able to generate up to $30V$ pulses directly from a low-voltage battery supply to excite an US transducer.

HV operation is a necessity in US imaging transceiver design in order to generate sufficiently large pressure waves inside of the body and hence obtain high roundtrip SNR and to increase the imaging depth. Traditionally, external HV supplies are used to supply the transmit pulser with tens of volts. Currently, for portable designs, on-chip HV DC-DC converters are employed to generate the HV supply, and large off-chip decoupling capacitors are required to regulate the HV supply. The goal of this work is to circumvent these additional (very large) conversion losses and increase the end-to-end efficiency of portable US imaging systems significantly.

The pulser uses only a single off-chip component, that being an inductor, to produce HV half-sine wave pulses to excite a US transducer. It uses the resonance energy transfer from the energy stored on the magnetic field of an inductor to create a pulse with the capacitance associated with the US transducer, hence the design being named the ”resonant pulser”. The resulting system architecture leads to a small area-efficient design, considering the omission of the HV supply. The resonant operation of the pulser makes it possible to recycle residual reactive energy left on the transducer back to the source resulting in an energy-efficient design.

Due to the transmit voltage being a function of time, an automatic calibration technique is used to quickly calibrate the transmit voltage to 5 different programmable levels between $10V$ and $30V$. Allowing the pulser to be used for apodization techniques to improve the imaging performance or to adapt the imaging depth for different imaging scenarios.

By means of automatically calibrating the timing of the recycling operation of the pulser an power efficient solution is implemented that optimizes the efficiency of the pulser.

Two prototype chips have been taped out in TSMC $0.18\mu m$ BCD Gen2 technology. One of the ASICs implements a single pulser design which has been optimized for power efficiency, while the second ASIC implements 2 transmit channels and the ability to receive echoes. The two-channel ASIC has been measured both electrically and acoustically with CMUT transducers. The resonant pulser has been demonstrated to generate the different programmable pulse amplitudes correctly with a $1V$ accuracy. And furthermore, both transducer trimming and energy recycling calibration have been tested successfully. The ASIC measured a peak efficiency of $0.37fCV^2$.

The prototype ASIC has been designed to handle variations of $\pm 20\%$ on both the inductance of the inductor and the transducer capacitance by means of performing a trim operation to set the resulting resonance frequency equal to the transducer’s center frequency. Resulting in an efficient synchronous operation of the pulser.

This work shows the first ASIC that is able to directly create an HV pulse from a low voltage supply, and the first reported portable design to use only a single off-chip component. Besides the pulser being 63% more efficient compared to a Class-D pulser it saves a considerable amount of power considering the omission of a HV supply.

Keywords: Ultrasound imaging, Pulser, Resonant pulser, Energy recycling, Portable ultrasound, High voltage CMOS.

Acknowledgements

Writing this work could not have been done without the support and help of my friends, family, and colleagues.

First and foremost, I want to thank and express my appreciation to my supervisor Michiel Pertijs for all the opportunities, the discussions, and the support over the last year. During my MSc thesis, I have learned a lot and gained much valuable experience in circuit design and project management. Thanks to our many discussions and (often long) meetings I always gained inspiration to try out or consider new ideas. The results reached in this thesis wouldn't have been possible to be reached without all his help and ideas. He always tried his best to help me solve the issues, improve my knowledge and increase my writing and presentation skills, and was always willing to give feedback on my work.

I would also like to thank Nuriel Rozsa for helping and advising me during the layout and measurement process of the project. His experience and willingness to help me during the stressful tape-out deadline and ISSCC deadline played an important role in the completion of this work and couldn't have been done without him. The many talks we had about his own work and other related work from our group have led me to appreciate the work that is being done in our research group a lot more.

In general, I want to thank all my colleagues in the Electronic Instrumentation group. A special mention goes to the technicians Zu-Yao, Lukasz and Ron for their kind help in solving all the technical issues I had and showing me the ways around the measurement and assembly facilities. I would also like to thank my fellow MSc students Jie, Tianyi, and Lai whom I have shared an office space the last year.

A special thanks go to all my good friends who have supported me and made me laugh the last 5 years here in Delft. Ronald, Lars and Charlene you made the last 2 years of my studies during the master's a wonderful time. There wasn't a single moment we didn't have a laugh together and let us not forget our many (sometimes getting out of hand) coffee breaks during the thesis. Where we often come up with new ideas to help each other out besides having a good laugh. Also, my other good friends that I've known since my bachelor Paul, Luuk, Melle, Sven, Wessel, Marten, Mark, Thijmen, and Niels who have stood beside me during the difficult times we had in our studies and who were there to help me out and make me laugh. I appreciate all the fun time we have spent together since we all met during the first days we started in Delft, you guys gave me the courage and motivation to keep on going.

Lastly, I want to thank my caring parents for supporting me during my studies at TU Delft and always trusting me in my decision making and leaving me the freedom to choose my own direction.

Imad Bellouki
Delft, December 2023

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Acronyms

AR - Aspect ratio
ASIC - Application specific integrated circuit
AWG - arbitrary waveform generator
BCD - Bipolar-CMOS-DMOS
BGR - Bandgap reference
BPF - Band pass filter
BVD - Butterworth-Van Dyke
CM - Common-mode
CDAC - Capacitive digital to analog converter
CMUT - Capacitive Micromachined Ultrasound Transducers
CL - Capacitor-less
CT - Continous time
DM - Differential-mode
DMOS - Double diffused MOS
DNL - Differential non-linearity
DT - Descrete time
DTI - Deep trench isolation
ESD - Electrostatic discharge
ESR - Equivalent series resistance
FPGA - Field-programmable gate array
FSM - Finite state machine
HV - High-voltage
ICE - Intercardiac echocardiography
INL - Integral non-linearity
IVUS - Intravasculair Ultra Sound
LDO - Low-dropout regulator
LHP - Left half plane
LSB - Least significant bit
LV - Low-voltage
MSB - Most significant bit
NBL - N-burried layer
NF - Noise figure
OTA - Operational transconductance amplifier
PMUT - Piezoelectric Micromachined Ultrasonic Transducers
PTAT - Proportional to absolute temperature
RX - Receive
PZT - Piezoelectric (Lead zirconate titanate)
RTL - Register-transfer level
SAR - Successive-approximation register
S/H - Sample and hold
SNR - Signal to noise ratio
SOI - Silicon on insulator
SRF - Self resoannce frequency
STI - Shallow trench isolation
TC - Temperature coefficient
TR - Transmit/receive
TX - Transmit
US - Ultrasound
ZCD - Zero crossing detection

1 Introduction

1.1. Application and Background

In recent years many technological advancements have paved the way for new innovative medical devices that are able to make patient diagnostics simpler and cheaper. One of these medical fields is ultrasound (US) imaging, Traditional US is known for being characterized by bulky devices connected to large imaging systems in a doctor's office. In recent years, more effort has been taken into miniaturizing these US systems and integrating them into a single application-specific integrated circuit (ASIC). Many challenges arise by trying to fit all the required electronics into a small chip footprint while maintaining good imaging performance. The most basic form of US imaging relies on simple pulse-echo measurements. Where the propagation time of a pressure wave, produced and received by an electromechanical transducer(s), is directly correlated to the distance between that transducer(s) and the object to be imaged. The intensity of the received echo is ideally only determined by the impedance difference between the medium (tissue) and the object causing the reflection. However, US waves decimate exponentially as they propagate through the body, causing signal attenuation as a function of distance. For soft tissue the attenuation is given by [1]:

$$\alpha = 0.5 \cdot \frac{dB}{MHz \cdot cm} \tag{1.1}$$

In order to obtain sufficient imaging depth for a targeted roundtrip signal-to-noise ratio (SNR) for the receive chain a large excitation voltage on the transducer's of tens of volts is required. In order to sustain such high voltages on-chip, special high voltage (HV) devices are often used in the design of these pulser's, contributing to a large part of the chip area [2].

During a single transmit period often only a single pulse or a short train of pulses is used in order to excite the transducer element. The transducer elements are characterized by their center frequency of a few MHz (or even $\geq$ 10MHz if high resolution is required) from which one would readily see that the receive period is much longer in order to obtain echoes from inside the body (see Figure 1.1). This leads to the receive chain operation taking much longer and often dominating the total power dissipation of the system [3]. In some specific situations where one would perform continuous pulsing for imaging purposes (in this case the system would operate in a full duplex manner), the energy consumption of the pulser could dominate the total power efficiency of the system. Often not only a single transducer element but multiple on an array are pulsed, these could be either 1-dimensional (1D) or 2-dimensional (2D) arrays enabling 2D or 3D imaging from inside of the patient [3]. More advanced techniques are then required to obtain a steered plane of the focused US wave by means of beamforming as an alternative for mechanically moving the array as is done in traditional US imaging [3].

During the acquisition of the image, the image is often created by scanning a single 'line' and moving the transducer or transducer array in order to take the follow-up line scan. These lines are then combined in a process to create the image. The speed at which each new scan line is acquired is often referred to as the pulse repetition frequency (PRF). The required PRF depends on the application, e.g. in applications where the to-be-imaged object moves fast like in cardiology, it requires high PRF rates around 10kHz while abdominal imaging is often done at only 3 or 4 kHz [1]. This thesis will focus

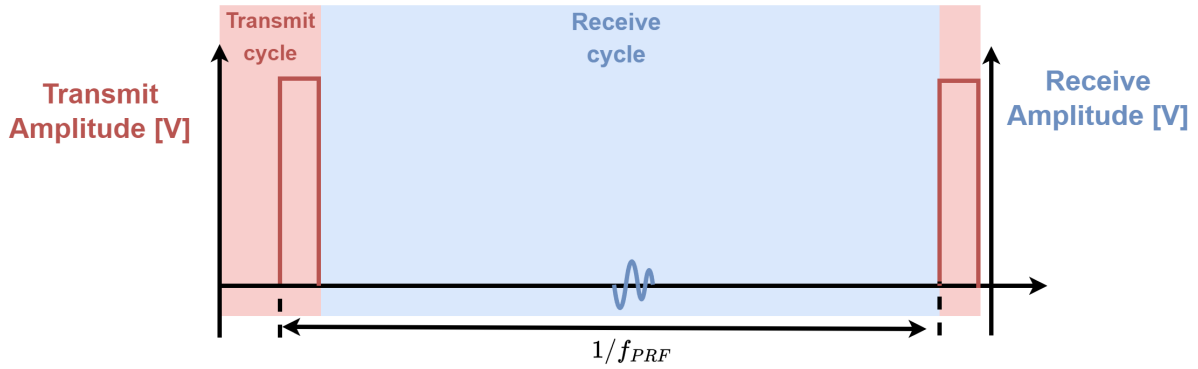

Figure 1.1: Example of a single transmit/receive cycle for a US imaging system seen from the transducer voltage.

specifically on a new type of HV transmit circuit capable of generating the required HV transmit pulses for a US ASIC in an energy efficient manner for future portable US ASICs. This implies that the whole system will be run off a small battery, leading to a strict requirement on the energy efficiency of the entire system.

1.1.1. US patches

Compared to other medical imaging methods miniaturized US can offer a cheap non-evasive solution to diagnose/monitor patients or be used in medical intervention. Examples of cases where on-chip US imaging is used are for bladder monitoring or for imaging within the body, i.e. intracardiac echocardiography (ICE) using a probe or catheter. The common denominator in all prior miniaturized US imaging systems is that they are still connected to a large external imaging system that processes all the ASIC data and acts as the power supply for the ASIC. Nowadays integrated US systems find their way into many non-evasive US and point-of-care US scenarios. Some of these require rapid high-resolution imaging techniques such as Doppler imaging, while others require less extensive imaging techniques. A pivotal new development is the shift towards compact portable US imaging systems, one of the popular forms where this has taken the form of are US patches (see Figure 1.2). These patches promise to offer a cheap method to perform diagnostics or monitoring on a patient for long time periods without the constant intervention of a medical professional.

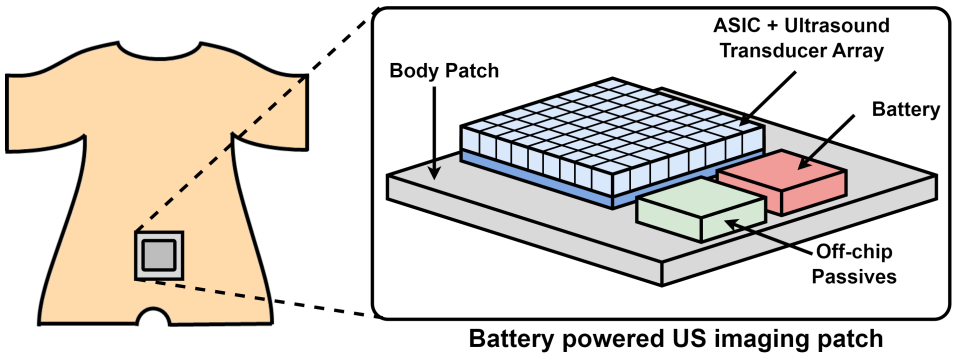

Figure 1.2: Artistic impression of the envisioned battery-powered US patch.

The development of these devices face a few large roadblocks that need to be addressed. One of these roadblocks is the lack of an available HV supply in order to generate HV pulses. A conventional solution would require an on-chip HV DC-DC converter (either a charge pump-like structure or even an HV boost converter) in order to generate the required HV, and large off-chip capacitors to regulate the supply [4],[5]. Besides the additional conversion losses (which can be very large [4]) leakage from the off-chip decoupling capacitors can pose an even larger source of energy loss. The ASIC would operate on a low duty cycle, where the measurement intervals could be in the order of tens of minutes. Considering these time intervals the charge on these capacitors would leak away requiring them to

be charged again at startup. Since the size of these capacitors could be orders of magnitude larger than the total transducer array capacitance, the power consumption of the ASIC could get significantly higher.

In this thesis, a new method for generating HV pulses for US imaging is proposed based on a boost-converter-like architecture, which targets energy-efficient design for portable US imaging applications that run off a low-voltage battery input supply. Here a circuit using only one off-chip component, an inductor, is used in order to generate AC pulses instead of a constant DC voltage. This will allow efficient direct generation of HV pulses without the need to generate and regulate an HV supply on the chip at all. The pulser utilizes resonant energy transfer from the energy stored in the magnetic field in the inductor to directly transfer the energy to a US transducer hence creating an HV pulse. The residual energy left on the transducer can in the same way be recycled back to the battery. For this thesis, the 'resonant pulser' will be designed around its application in a US patch, where the aim is to show the increased energy efficiency compared to CV^2 from the conventional HV square pulser without the need to generate and regulate an HV supply. Figure 1.3 shows a simple comparison between the two.

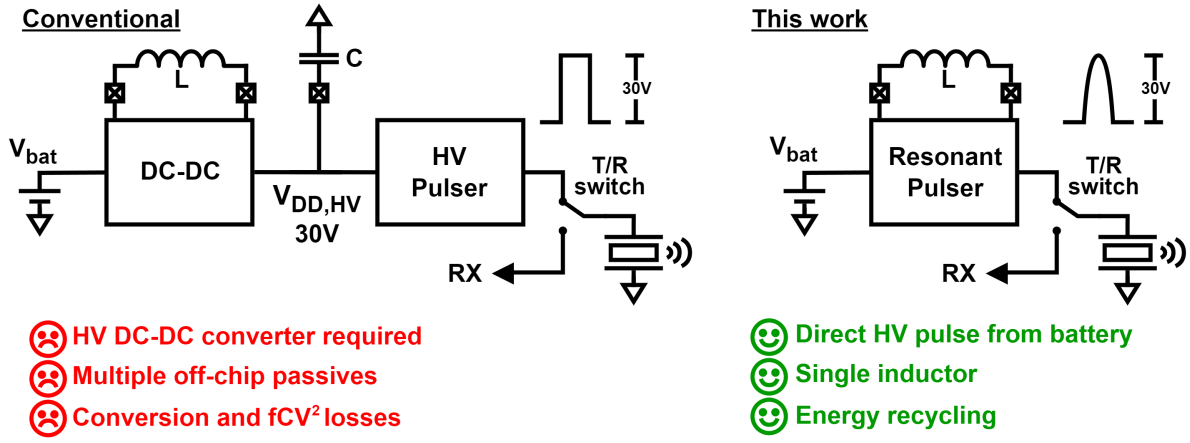

Figure 1.3: Comparison between a conventional US system targeting portable applications and the proposed resonant pulser.

1.2. Prior art

1.2.1. Traditional US tranceivers

A US transceiver consists mainly of two parts, the transmit and the receive chain. The transmit chain (TX) is responsible for producing the US pressure waves with the use of transducer elements. The receive chain (RX) is responsible for conditioning and digitizing the received echo signals [3]. Here circuits like a low noise amplifier (with often additional time gain compensation) and optionally an ADC for on-chip digitization are often present. Figure 1.4 shows a simple example of how a traditional US transceiver architecture looks like.

The transmitters in US ASICs are responsible for generating the HV pulses needed to generate the US pressure waves by exciting a transducer. These transducer's, such as bulk PZT or micromachined CMUT devices, are characterized by a sensitivity in the order of kPa/V [3]. Due to significant signal attenuation from the reflected signal through human tissue which is both proportional to the signal frequency and the measurement distance (in dB). A large signal amplitude is required from the transmitter to achieve sufficient SNR for the echo signal. The circuit topologies used for these HV transmit circuits are in most cases either a class-D (push-pull) like pulser or a linear amplifier.

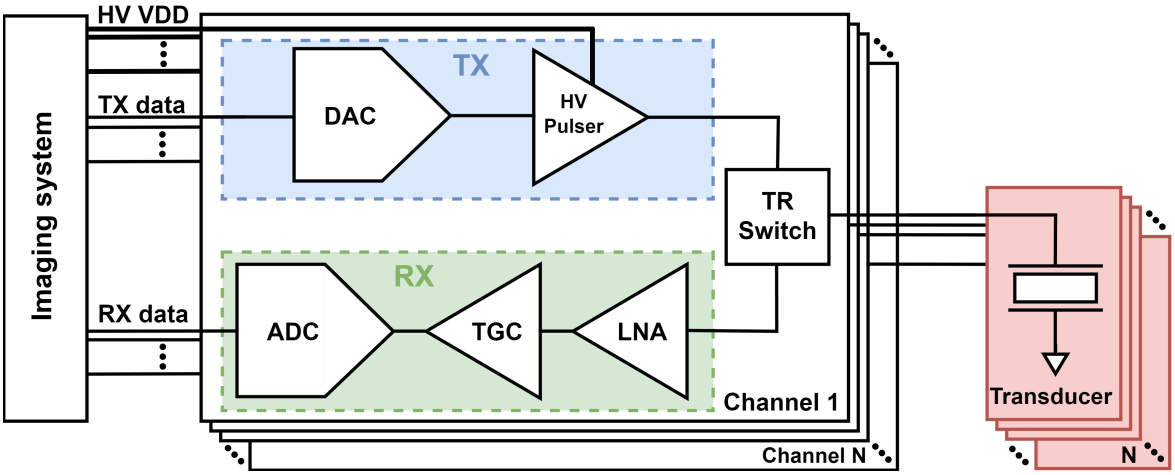

Figure 1.4: Example of a traditional US transceiver system architecture.

Conventional HV pulser design

Pulser's often employ either unipolar or bipolar pulsing. Unipolar pulsing is widely adopted due to its simplicity in operation and small footprint. However, for high-frequency applications such as B-mode imaging, bipolar pulsing is often preferred due to its higher SNR and sensitivity [6]. Bipolar pulsing also offers higher transmit efficiency due to the omission of the unwanted DC components unipolar pulses [3]. Figure 1.5 shows three common typologies used for creating HV unipolar pulses.

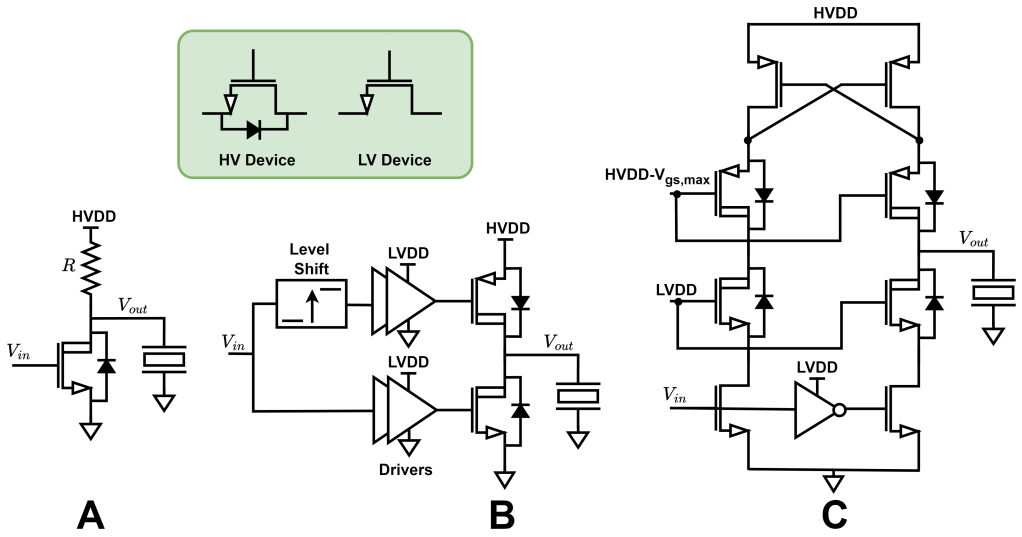

Figure 1.5: Conventional (unipolar) HV pulser topologies,(A) single HV NMOS pull-down transistor [7],(B) HV push-pull [4] ,(C) HV cross-coupled level shifter [8].

The smallest and simplest implementation uses only a single HV transistor by implementing a simple pull-down transistor, this obviously comes with large static power consumption. The HV push-pull pulser is a popular choice due to its relatively compact size and low power consumption (dissipating only dynamic power) [3]. These circuits require besides the HV NMOS and PMOS devices at the output an additional level shifter in order to sustain the limited $V_{GS} = 5V$ of the HV devices in most technologies [3]. These level shifters also require additional HV devices. Finally, a cross-coupled HV level shifter could be used, as presented in [8]. This or a similar structure uses positive feedback in order to create sharper rising and falling transitions of the HV pulse which are required in high-speed imaging. The downside of implementing such a pulser is the large amount of HV transistors required per transmit channel.

1.2.2. Energy efficient HV pulser's

For the pulser design in this thesis, one of the most important goals is to achieve high energy efficiency. In prior art, several approaches have already been reported that try to reduce the energy loss associated with the charging and discharging of the US transducer. This subsection will present a short overview of the current prior-art techniques used to reduce energy loss in HV pulser design.

Multi-level pulsing

When a transducer is pulsed with a unipolar rectangular pulse, the electrical losses consist of 2 parts. The first is the 'useful' energy consumed by the transducer in order to generate the acoustic pressure wave. The second is the wasted energy that is associated with charging and discharging the capacitance C_p of the transducer. The energy required then simply equals $C_p V_{TX}^2$, with V_{TX} being the transmit voltage (in case the transducer is purely capacitive). The losses can be significantly reduced by charging and discharging the transducer in multiple steps. This could be achieved by switching the transducer to a number of intermediate supply levels. For an N-level pulser the switching is done for $N-1$ steps, and the associated energy consumption from charging and discharging C_p is reduced by a factor of $N-1$ [9]. In a simple case where 1 additional voltage level is added between the HV supply and ground, this could be generated using a simple switch capacitor DC-DC converter and be shared across multiple pulser's (see Figure 1.6) [10]. The addition of the DC-DC converters does lead to additional (significant) conversion losses and multiple off-chip capacitors. A similar three-level pulser that could save $0.5CV^2$ presented in [6] utilized a bipolar pulser design pulsing the transducer at $\pm V_{TX}/2$. This however does come at a cost of requiring a symmetric HV supply. Figure 1.7 shows a more advanced implementation for a 7-level pulser that does not generate the 5 intermediate voltage level explicitly [11]. In case the pulser is pulsed continuously or with a very high PRF it could be already sufficient to use large reservoir capacitors which would reach a steady state corresponding to the desired voltage level. However, this requires multiple large off-chip capacitors and won't be a viable method to be used in most US imaging applications.

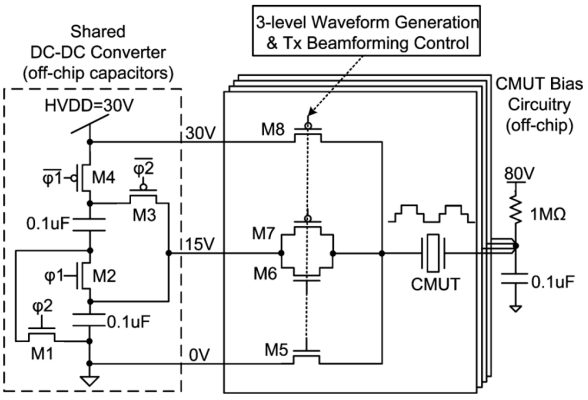

Figure 1.6: Schematic of a three-level pulser with mid voltage generation using a 2:1 parallel-series switched-capacitor dc-dc converter [10].

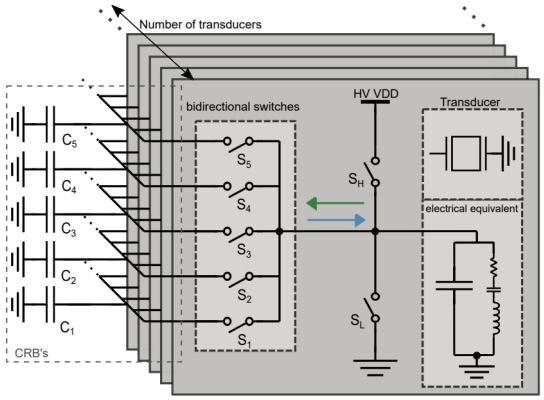

Figure 1.7: A 7-level pulser implementing large reservoir capacitors instead of generating intermediate voltage levels explicitly [11].

Capacitive charge redistribution/recycling

In some particular cases, the transducer does not require to be driven in a single-ended fashion, transducer's like piezoelectric micromachined US transducer's (PMUTs) can have both terminals accessed independently. This opens the possibility that instead of keeping one of the terminals always connected to AC ground, the transducer could be driven differentially or in an H-bridge configuration. The works presented in [12] show implementations using this 'charge redistribution' on PMUT transducer's, this is also shown in Figure 1.8. In this case, energy used to charge the transducer is saved by shorting both terminals of the transducer in a second phase before reversing the polarity of transducer voltage across the PMUT. By looking into this method further one would find that in effect a three-level pulser had been realized. In cases as presented in [13] the energy that can be saved is not equal to a factor of 2 as presented in the paper. Some of the energy can be saved by means of shorting the terminals

of the transducer since the losses associated with the parasitic capacitances (the parasitics referred to ground) are reduced.

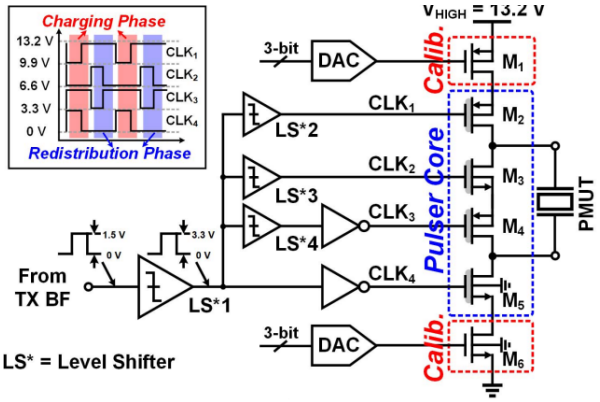

Figure 1.8: Schematic of a charge redistribution HV pulser using a PMUT transducer in a standard CMOS process [12].

Inductive energy recycling

The final method that reduces energy losses in an HV pulser design leverages a series inductor to avoid CV^2 losses. The work presented in [14] shows a US HV pulser design targeted at portable US applications (capsule endoscopy) which charges and discharges the transducer C_p through a series inductor (see Figure 1.9). This minimizes the energy dissipation in the switches and the energy stored on C_p can be recycled back to the supply via the inductor. This approach, however, still requires a dedicated HV supply. Generating this supply will inevitably again lead to multiple large off-chip capacitors and losses associated with generating and regulating an HV supply. Besides this, the design utilizes conduction through the body diodes of the HV transistors during the energy recycling phase while being fabricated in a BCD technology, which could lead to latch-up related problems in the circuit (this will be elaborated upon in Chapter 2). From the measured results it also becomes clear that this system requires many 100's of transmit pulses before reaching a steady state. This work achieves a 73.1% reduction of dynamic power consumption on a large 820pF capacitive load pulsing at an extremely low frequency of 5kHz.

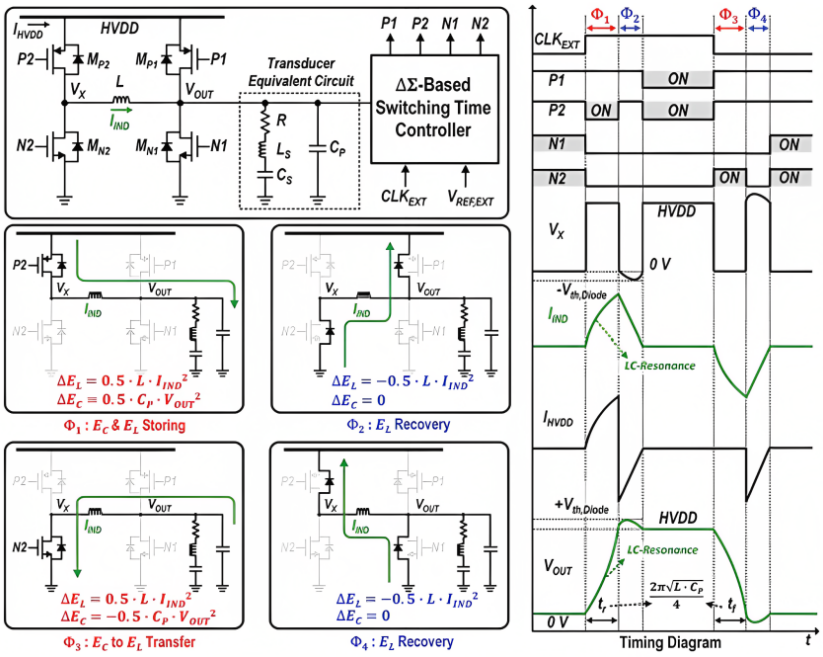

Figure 1.9: Schematic of the inductive energy-replenishing US pulser core presented in [14].

1.2.3. Low voltage powered HV pulser's

Besides obtaining a high efficient pulser design a second problem that this thesis needs to tackle is the issue revolving around driving an HV pulser from a low-voltage battery supply. This subsection will present a short overview of the current prior-art techniques used to create HV waveforms or pulses from a low voltage input supply. This will serve as a basis for the proposed HV pulser design for portable US imaging applications presented in the subsequent subsection.

Charge-pump-based waveform generation

One method to generate HV pulses from a low voltage supply is to use a capacitive charge-pump type circuit (or voltage multiplier). The work presented in [15] achieved a peak power efficiency of 64% at minimum load current and highest pumping frequency (see Figure 1.10). In [16] the energy left on the transducer is recycled in order to increase the total efficiency of the pulser. By leveraging multilevel pulsing the work presented in [17] achieves a peak power reduction of 75.4% relative to CV^2f by implementing 7 intermediate voltage levels to which a PMUT transducer is pulsed (see Figure 1.11). This approach however requires multiple large pumping capacitors which are orders of magnitude larger than the target load and have to be placed off-chip. Also, the end-to-end efficiency of these systems is not very high due to the losses associated with the generation of the HV supply. Also, some time would be required before a steady state is reached leading to even lower total efficiency in case the system would be only turned on for a short time interval.

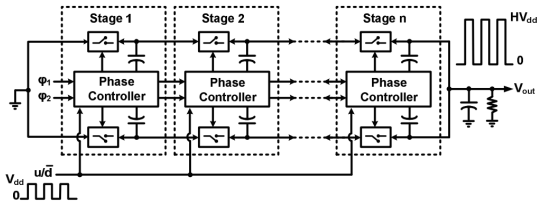

Figure 1.10: Charge pump-based square wave pulser achieving 64% peak efficiency [15].

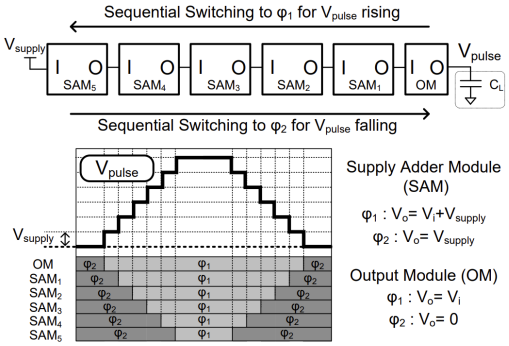

Figure 1.11: Charge pump-based multilevel pulser achieving 75.4% peak power reduction compared to CV^2f [17].

Buck-Boost-converter based waveform generation

An alternative method to drive transducer's is using an inductive boost converter [18], possibly combined with reverse-buck functionality[19], in order to generate HV waveforms that can drive a PZT transducer in an energy-efficient manner. Figure 1.12 shows the architecture of a bidirectional buck-boost driver that generates a continuous $100V$ peak-to-peak sinusoidal excitation waveform on a PZT transducer [18]. Such an approach has the benefit of generating HV excitation waveform on a transducer directly from a low-voltage battery input supply. However, still, an off-chip inductor, filter capacitor, and sense resistor are still required. Furthermore, the most important drawback of using such a converter is that the converter itself runs at a frequency much higher than that of the generated waveform. In [18] the converter runs at 100s of Hz while the generated waveform frequency is 150Hz, likewise in [19] the converter runs at several MHz while the generated waveform frequency equals 30kHz. In US imaging where pulses in the MHz range are required this method becomes unfeasible to implement.

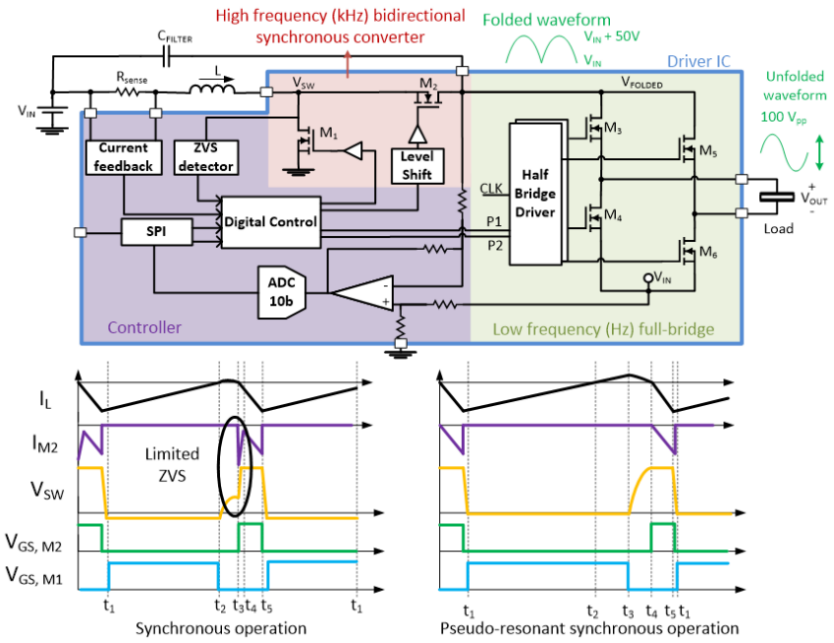

Figure 1.12: Architecture of a bidirectional synchronous buck-boost converter to drive a piezoelectric element at 100V peak-to-peak [18].

Fly-back converter based drivers

Another interesting variation on the previously described buck-boost converter-based driver is using a fly-back converter-based driver. The work presented in [20] proposes a dual-stage piezoelectric driver achieving 100V excitation on two piezoelectric transducer's used to drive microrobots. The circuit implements a high step-up ratio fly-back converter cascaded with a bidirectional half-bridge (see Figure 1.13). The first stage steps up the low battery voltage $(3.7V)$ to the required HV, whereas the second stage transforms the DC voltage into a time-varying drive signal. The structure reuses the residual reactive energy on one of the PZT elements to charge a second PZT element together with the charged energy on the inductor. This charging and recycling method could be increased to more than 2 elements by increasing the number of HV transistors. The obvious downside of this driving circuit is the number of off-chip components that are required for a CMOS implementation of such a circuit. it requires a (relatively bulky) fly-back transformer and (off-chip) freewheeling diodes that need to be placed in parallel to the HV transistors to create a proper condition path and avoid triggering the body-diodes of the HV transistors in case of an HV BCD CMOS integration of the design. And an off-chip inductor.

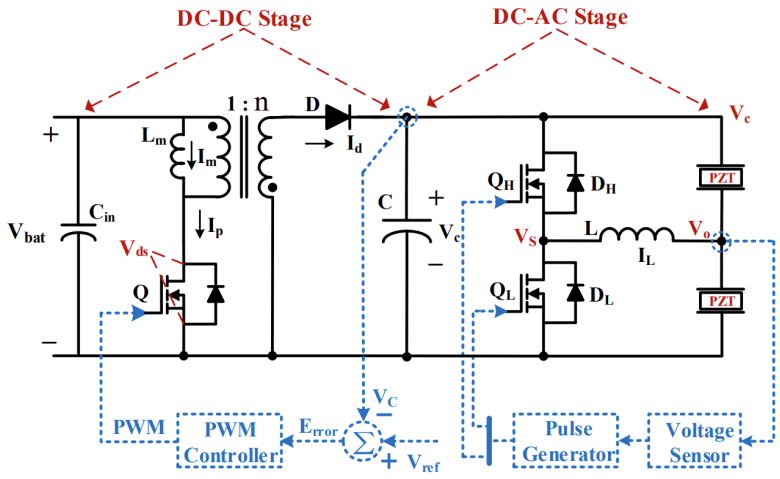

Figure 1.13: Bidirectional fly-back converter based piezoelectric driver [20].

1.3. Resonant pulser system proposal

1.3.1. operation principle

Figure 1.14 shows a simplified circuit of the resonant pulser core with the different operational phases of the system. In the first phase ϕ_1 the inductor is charged to its peak current I_{pk}, in the second phase ϕ_2 the energy that has been built up in the magnetic field of the inductor is supplied to the transducer in resonance. This series LC connection would generate an oscillation that is stopped at the peak output voltage amplitude. During ϕ_{hold} the transducer is left floating generating a square wave-like pulse (similar to a conventional square wave HV pulser) while the residual energy in the inductor is dissipated. In ϕ_3 the energy that is left on the transducer is cycled back to the inductor and in the final phase ϕ_4 this energy is recycled back to the battery.

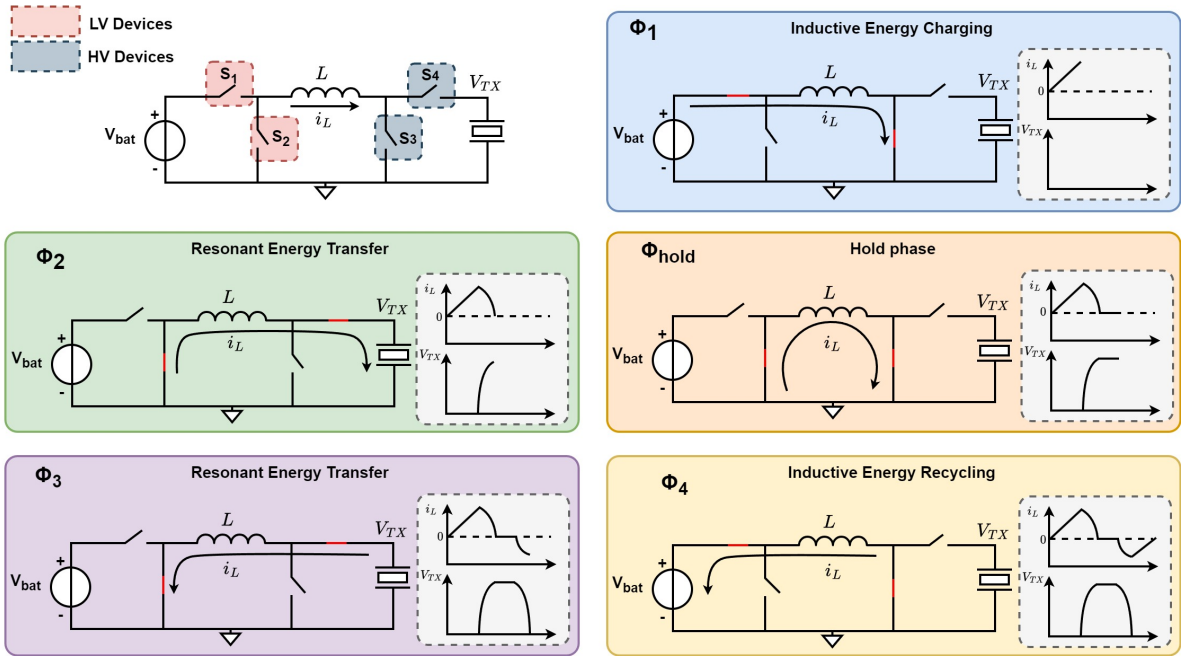

Figure 1.14: Simplified diagram showing the basic operation of the proposed resonant pulser.

1.3.2. Limitations

The requirement of an off-chip inductor does impose limitations on the application of the resonant pulser. First, this design would not be suited for highly integrated US applications due to the required off-chip inductor. The size of these commercially available inductors could be large compared to the ASIC. Secondly, the architecture of the proposed pulser could fundamentally impose limitations on the types of imaging that could be used for this system. The resonant pulser is still capable of imaging through a 2D array of transducer's, however pulsing multiple transducer's simultaneously could prove to be more difficult. As an example, for more advanced imaging techniques one would like to transmit multiple transducer elements on the array in order to perform transmit beamforming. If one would transmit different combinations of transducer elements using the resonant pulser the larger capacitance C_p that the battery has to drive would result in a different time constant τ. This could however be solved by changing the inductor charging time to build up a larger peak current through the inductor since the amount of transducer's to be pulsed is known to the system. This would unfortunately lead to a less power-efficient system since in that case the inductance is not optimized for the load it has to drive in order to generate the pulse during its series resonance cycle.

This drawback does not make the resonant pulser a bad contender for US imaging applications. The resonant pulser can make use of synthetic aperture imaging to get around some of the imaging limitations. In this imaging technique, a single transducer (or a single row of elements) is pulsed on a transducer array while in the receive phase, all transducer's receive the reflected echo [21]. Synthetic aperture imaging can still lead to high-resolution images in case the measured object does not move too

much in the time window needed to pulse the entire array. One obvious drawback is still the resulting poor SNR because of the weak transmission from a single element.

1.3.3. Advantages

The proposed resonant pulser offers some important benefits compared to conventional class-D or linear amplifier-based HV pulser's. The resonant pulser can prove to be more area efficient since no HV supply needs to be regulated on the chip or has to be generated locally on-chip by means of a charge pump or DC-DC converter as is done in the prior art. Also, this design would only require one off-chip inductor and no additional bulky off-chip capacitors resulting in possibly a smaller total footprint of the system. The resonant pulser can potentially offer much higher power efficiency compared to the dynamic power dissipated which equals $fC_pV_{TX}^2$. This energy saving would stem from the fact that the resonant pulser is able to efficiently supply energy during resonance to the transducer and recycle back reactive energy left on the transducer to the battery through the inductor. Ideally, there could be zero $C_pV_{TX}^2$ energy loss. If we now also consider the fact that the resonant pulser operates without additional conversion losses the total end-to-end efficiency of the system can prove to be very high.

1.3.4. Application scenarios

The main application targeted in this thesis for the resonant pulser are US patches, as introduced earlier in this chapter. Besides imaging patches other emerging battery-powered US applications could benefit from the resonant pulser. US capsule endoscopy is another example where energy efficiency, and minimizing off-chip passives are important in order to both reduce the size of the total device and reduce cost [17]. Another interesting field where the resonant pulser could prove useful is in wearable US stimulation. The work presented in [22] targets a wearable US neurostimulator. It utilizes a hybrid (inductive and capacitive) programmable boost-converter, and an additional voltage multiplier (off-chip IC). Measurements show that the power management system is responsible for 46.5% of the total average power consumption (the ASIC only consumes 5.4%). Demonstrating that possibly a lot can be won on the end-to-end efficiency of such a system if the required power management system could be omitted.

1.4. Objectives

Now that the concept of the resonant pulser has been shown together with its target application. This section will present the different thesis objectives that need to be reached in the design for the prototype chip of the pulser. The goal is to achieve a prototype chip that utilizes only a single off-chip component, that being the inductor, and a low voltage input supply to realize a portable US HV pulser. The inductor should be a small SMD component that together with the chip would only require a small battery to operate. The battery voltage imposes a limitation on the maximum achievable efficiency and charge time given an inductance L and transducer with capacitance C_p. For this prototype, a $3.6V$ Li-ion battery is assumed. Due to the varying voltage that a battery has depending on its depth of charge a range between $3.3V - 3.9V$ is assumed. In order to achieve sufficient SNR for the receive chain, a maximum transmit amplitude of $30V$ is targeted. The transmit amplitude itself should be programmable in order to adapt the penetration depth of the pulser. With the addition of a programmable transmit amplitude, one could implement apodization on a transducer array to optimize the profile of the transmitted beam. Apodization in effect applies a spacial window (weighting of the individual pulsed elements) across the transmitted beam in order to reduce the side lobe levels. This could be easily implemented using the resonant pulser since the controlled quantity that will set the transmit amplitude level is time. The maximum deviation from the targeted amplitude levels is set to $300mV$ which corresponds to 1% of $V_{TX,max}$.

For the sizing requirements, this prototype does not target a pitch-matched design or a full array integration. Unlike US ASICs targeting high-density integration like an ICE or IVUS catheter, a US patch comes with more relaxed requirements in regards to die area. Of course, during the design, some realistic considerations need to be made in the sizing of the HV devices to obtain a scalable pulser for a large multi-element array. The energy efficiency should be optimized. The resonant operation during the energy transfer and the inductive energy recycling promises to reduce energy dissipation compared to CV^2. However, the required system overhead could add considerable power consumption which has to be minimized. The ASIC should work with a commercially-available SMD inductor,

which means that the system should handle the large tolerances these off-chip components have. Here an inductance deviation of $\pm 20\%$ is assumed. Likewise, the capacitance that characterizes the transducer spreads across an array and even between neighboring elements, therefore the system should be able to handle variations up to $\pm 20\%$ (around $\pm 1dB$) on the transducer capacitance C_p. Since the prototype targets on-body US patches, the temperature requirements can be relaxed for the ASIC. For this work, an operation temperature range between $0°C$ and $40°C$ is assumed. For the timing of the circuit, an external clock of $50MHz$ is assumed to be available from an FPGA.

Table 1.1 presents a summary of all the objectives set for the prototype resonant pulser ASIC.

Table 1.1: Summary of the requirements for the resonant pulser prototype ASIC.

ASIC requirements
Only a single off-chip inductor should be used.
Maximum transmit amplitude $V_{TX} = 30V$.
Maximum deviation of the target amplitude should not exceed $300mV$ (1% of $V_{TX,max}$).
Programmable transmit amplitude.
Target silicon area: no specific requirements are set since no pitch-match design is required, however, the design should be small in order to be implemented with a transducer array.
Energy efficiency should be lower than CV^2.
The input supply should be limited to low voltage battery levels, e.g. $3.6V$ for Li-ion batteries.
The ASIC should be able to handle $\pm 20\%$ variation on the SMD inductor L .
The ASIC should be able to handle the variation on the transducer capacitance C_p depending on the specific transducer used, a range of $\pm 20\%$ (around $\pm 1dB$) is assumed.
The ASIC should be able to handle variations in the battery voltage levels which will vary depending on the depth of charge, a range between $3.3V - 3.9V$ is assumed for $3.6V$ rated Li-ion battery.
Since the patch is used outside of the body a working temperature range between $0°C$ and $40°C$ is assumed.
The system clock frequency equals $f_{CLK} = 50MHz$

1.5. Thesis organization

This Thesis presents the steps taken in the design of a prototype resonant pulser targeted for wearable US patches. The chapters are organized in chronological order, starting in Chapter 2 with a feasibility analysis and architecture-level design and ending in Chapter 5 with the measurements from the prototype chip.

Chapter 2 will discuss the feasibility analysis of the resonant pulser and will present two architecture topologies with their advantages and disadvantages. Also, technology limitations will be discussed.

Chapter 3 presents the circuit-level implementation of the resonant pulser and the full implementation of the prototype ASIC.

Chapter 4 discusses the layout and floor-planning of the ASIC, methods to reduce layout parasitics, and post-layout simulations will be shown and compared.

Chapter 5 will show the measurement setup and both electrical and acoustic measurements of the resonant pulser ASIC.

Chapter 6 will conclude the thesis with the conclusions and suggestions for future work.

2

Architecture level analysis and design

In this chapter, the architecture design of the proposed resonant pulser will be discussed. Different parameters that influence the energy efficiency and functionality of the pulser are analyzed in a feasibility study. Also, different transducer types and their model are presented to finally lead to a simple energy-efficient topology for the entire system.

2.1. HV operation in silicon technologies

As presented in the introduction chapter the US transducer's that are targeted to be driven by the pulser require high transmit voltages (V_{TX}) in order to obtain sufficient mechanical pressure. Typically voltages between 10 and $100V$ are used in current state-of-the-art designs [3], [23]. In order to sustain such high voltages on-chip, either a special high voltage technology is used, or different techniques within standard CMOS technologies can be leveraged in order to produce high voltages.

The works presented in [24] and [25] show HV pulser designs targeted at US transducer's implemented in standard CMOS. Here techniques using dynamic gate biasing or using staggered well potentials are presented in order to disperse the electric field stress across the transistors terminals. The advantages of using a standard CMOS process are that the pulser can occupy less area and is cheaper to manufacture. Also, using a standard CMOS process gives the opportunity to use a more advanced CMOS process node which will be more beneficial to the receive path of the ASIC and for all the required digital logic. There are however drawbacks to using a standard CMOS process in the design of these HV pulser's and that lies mainly in the reliability concerns in applying the aforementioned techniques. Especially in this design where an inductive load is driven and no HV supply will be generated implementing the design in a standard CMOS process will not be realistic. Also, generating HV pulses much larger than $15V$ can be proven to be difficult using standard CMOS.

2.2. HV BCD technology

One of the options for an HV-capable technology is a BCD technology (Bipolar-CMOS-DMOS), which is a junction isolation-based technology. ASIC design in BCD technology is often employed for the design of US systems. The works presented in [10], [11], [6], [17] and [14] are a few examples where HV devices are used in the design of the pulser's. The BCD technology combines standard low-voltage CMOS together with both bipolar and DMOS (double diffused MOS) devices in one process enabling the integration of HV operation together with LV CMOS design. These HV devices come at the expected cost of silicon area in order to distribute the large electrical fields over large distances to prevent reaching critical values. This leads to larger distances across device terminals and more spacing for isolation barriers between the devices for example. A good understanding of how the technology works and where the limitations lie is important for designing the resonant pulser. A brief introduction of these HV devices in BCD technology is presented in this section together with the resulting parasitic devices and non-idealities. Figure 2.1 shows a schematic cross-section of a standard CMOS NMOS and PMOS transistor where its parasitic junction diodes and bipolar devices are shown. By means of proper biasing of the implanted regions, the p-n junctions won't be set in forward bias. The parasitic PNP and NPN devices can cause an effect known as latch-up. Here the bipolar devices can cause

each other to turn on and get stuck in a positive feedback loop causing a current to flow from supply to ground. This can be prevented by making the resistances in the silicon low by adding sufficient contacts to the wells.

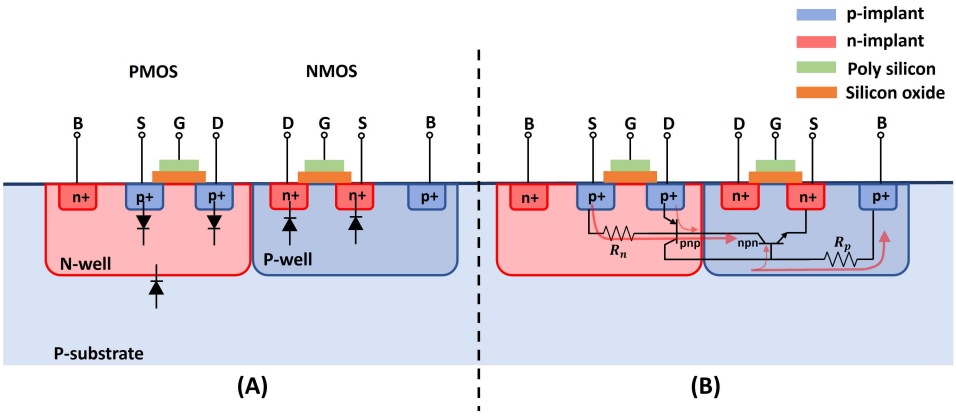

Figure 2.1: Parasitic devices in a standard CMOS process, (A) shorted and reversed biased p-n junctions, (B) parasitic bipolar devices triggering latch-up [26].

Figure 2.2 shows a simple implementation of an HV DMOS (double diffused MOS) device in a BCD technology. The double diffusion referred to in DMOS is due to the n+ source and p-body diffusion regions. This structure presents a strong resemblance to a BJT device with a MOS gate added on top. In DMOS devices the source and bulk are almost always connected together and are aligned with the gate. This creates a channel region underneath the gate that has a length determined by the difference in lateral diffusion between the p-body and the n+ source. The length of the resulting channel does not depend on the dimensions of the gate thus often only the width of these devices can be scaled.

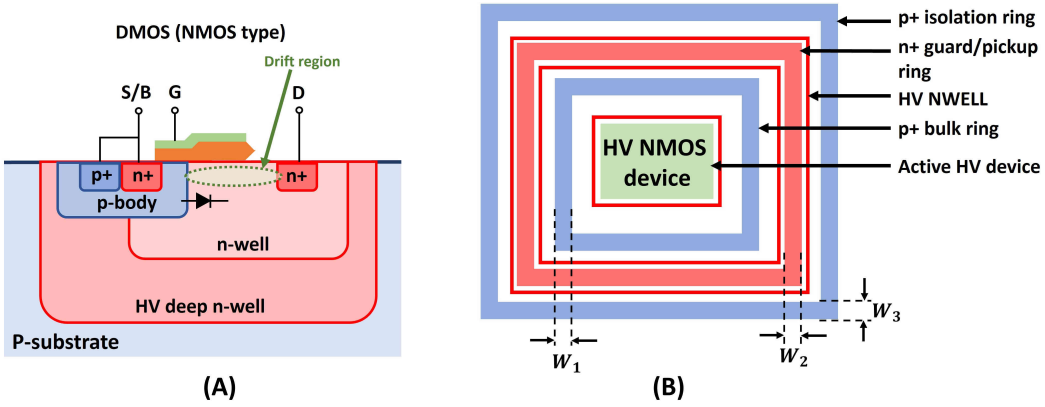

Figure 2.2: (A) General cross-section of a DMOS device (NMOS type) [26], (B) simplified top view of a general NMOS type DMOS in the TSMC BCD technology (obtained from technology PDK).

The more lightly doped n-well region acts as a buffer region between the drain and the channel, this buffer region is referred to as the drift region. Since this drift region is placed in series with the channel and the drain it effectively determines the on-resistance (R_{on}) of the device. From this structure, it becomes clear that these DMOS devices can only handle a large voltage on their drain terminal. Furthermore, unlike standard CMOS transistors, the DMOS devices are asymmetrical. The overdrive of DMOS devices is thus still limited by the gate oxide breakdown voltage, using thick oxide layers still limits this to around $5-5.5V$ (in the TSMC 180nm BCD technology). Figure 2.2 also shows that the gate extends across the channel region across the drift region, this is done in order to reduce the electric field potential along the surface of the drift region (and leads to increased gate capacitance). Finally, the HV deep n-well is placed to isolate the active part of the device from the substrate. Inspecting the lateral profile of the DMOS an implicit BJT parasitic can be seen, due to the doping profile of the implant, the

p-body, and lightly doped n-well, a very effective bipolar parasitic has been created across the source and drain terminals of the device. In order to prevent this parasitic from being turned on the source and bulk of the device are connected together. This parasitic junction is therefore often implicitly drawn in the symbol of the device. The presence of the deep n-well creates a diode between the drain and the substrate. When the drain is pulled below the substrate, which can occur with an inductive load, the diode is forward-biased and electrons are injected into the substrate. These are minority carriers in the p-substrate and can cause latch-up in neighboring parts of the circuit.

2.2.1. Folded DMOS and guard/isolation rings

In order to keep reasonable aspect rations of multi-finger structures DMOS devices are folded around either their drain or source as shown in Figure 2.3. In order to add isolation around DMOS devices various guard rings are placed around the active transistor area, Figure 2.2 shows a simplified top view of a DMOS device with added isolation. The different widths (and distances) of these implanted barriers depend on the desired peak voltage the device should handle. The wide barriers can cause a significant increase of parasitic capacitance on the device terminals and furthermore due to the required distances from the different rings the DMOS device becomes very expensive in area consumption for small transistors. The deep n-well not only creates the parasitic substrate diode but also a parasitic PNP transistor. The device goes in forward bias in case the source is pulled higher than the drain, and again this can occur when driving an inductive load, as a result, holes are injected in the substrate. A significant part of the holes are collected in the substrate since the holes are majority carriers and a large voltage difference exists between the deep n-well and the substrate, this leads inevitably to dissipation in the substrate region. The holes can thus give rise to a rise in the substrate potential and can cause problems in neighboring devices. For this reason, a p-guard ring is present to firmly fix the substrate potential around the periphery of the device. The size of this ring can be sized at a minimum width in most cases. Depending on the specific type of DMOS transistor the amount of implanted wells and barrier rings can vary. In almost all cases at least one n-guard and one p-guard ring are present in the device. The implanted n-guard is responsible for minimizing the amount of injected electrons reaching the substrate and causing latch-up risks. In order to make the electron collection more effective the n-guard is often connected to a positive voltage.

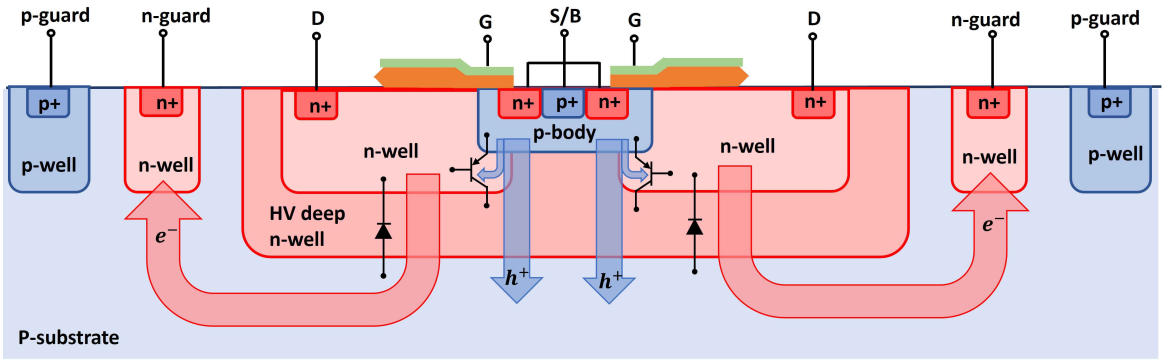

Figure 2.3: Cross section showing the parasitic devices in a general folded DMOS device structure with its source centered and with guard rings [26].

2.2.2. TSMC 180nm BCD

For the resonant pulser design careful design considerations on the circuit level design and layout will be required in order to minimize latch-up risks in the circuit. For this reason, only fully isolated type DMOS transistors (in the technology often indicated by 'NBL') are considered, Figure 2.4 shows a cross-section of such a device in TSMC BCD 180nm. These devices do not provide the option to separate the bulk potential from the substrate by means of placing an additional p+ ring around the active device to act as bulk contacts, this ring is shorted to the source/bulk implant in the active device region. The fully isolated type devices provide full vertical isolation by means of buried n and p implants. This provides better control of the parasitic currents and lowers the effect of the drain substrate diode and the substrate PNP significantly. These devices do come with additional area costs in order to create

the deep buried layers and the deep diffusion required for the vertical contacts.

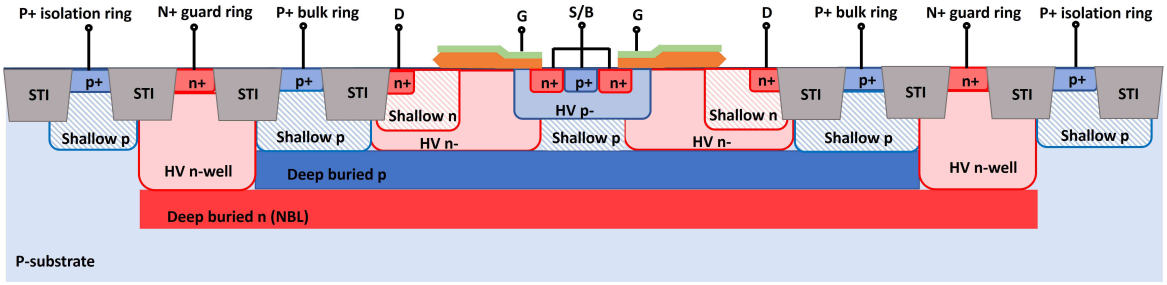

Figure 2.4: Cross section of a general NBL-based HV NMOS DMOS device in TSMC 180nm BCD (obtained from technology PDK).

Alternatives to the presented BCD technology that can offer better HV isolation are technologies that enable deep trench isolation (DTI). These are additional deep lateral dielectric isolation barriers that extend to deep buried layers. It consumes less area compared to the isolation provided by the guard rings but comes at a more costly price. A second and even more expensive solution would be to use a silicon-on-insulator (SOI) process. This technology uses a buried oxide to achieve full dielectric isolation and eliminate the risks of latch-up and leakage. This option however requires expensive special wafers and is not a viable solution for cheap portable US imaging systems.

2.3. Transducer types and model

In order to produce the ultrasound pressure waves a US transducer is used that is driven by the transmit channel of a US ASIC. The most common US transducer's are bulk piezoelectric (PZT), capacitive micromachined (CMUT), and piezoelectric micromachined transducer's (PMUT). Figure 2.5 shows a simple cross-section of these devices [27], [28]. The different transducer's bring their own pros and cons considering US imaging. The transducer's can be split up into either bulk transducer's or micromachined transducer's. The important benefit that the micromachined PMUT and CMUT bring is their CMOS compatible integration. The bulk piezo transducer's on the other hand are more mature compared to the micromachined transducer's, but their more complex integration with the ASIC does not make them a good contender for the target application. The micromachined transducer's use a thin membrane that causes a deflection inside a cavity and thus produces a pressure wave in the medium. Modeling of CMUT transducer's is often more difficult compared to bulk transducer's since these devices are inherently non-linear.

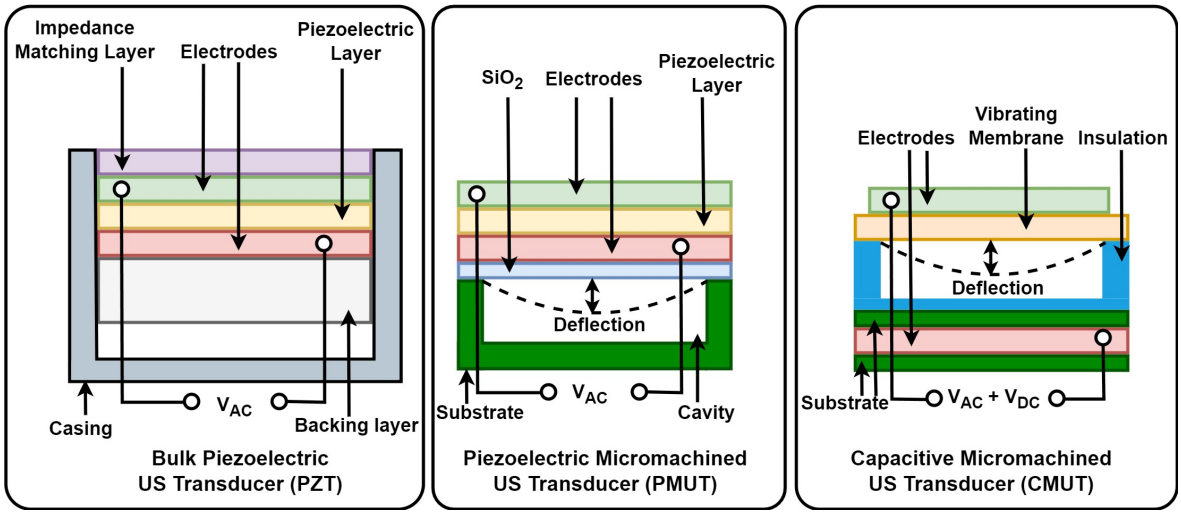

Figure 2.5: Cross section of a bulk piezo electric transducer (PZT), PMUT and CMUT [27], [28].

This leaves either the PMUT or CMUT devices as the best possible target transducer for the reso-

nant pulser. One important distinction between the two is the HV bias voltage that CMUTs require in order to operate efficiently. The membrane in a CMUT needs is biased biased in order to put the device in a 'collapse' mode in order to increase both the transmit and receive sensitivity [29]. This bias voltage can exceed 100V in many cases. Another emerging alternative are so-called pre-charged CMUTs [29], [30], these CMUT devices do not require an external HV bias to operate and pose as an interesting choice as a future target transducer.

In order to model the electrical behaviour of the transducer a Butterworth Van-Dyke (BVD) model is considered [31], [32]. Figure 2.6 shows the equivalent circuit of the BVD model together with its frequency domain behaviour. The simple four-element BVD model consists of 2 parallel branches. It is often used as a simple model of a piezo resonator near resonance. In resonance, depending on the transducer the static electrical capacitance C_p (capacitance of the electrodes) of the device could be very large. The RLC branch is often referred to as the motional branch since it represents the electromechanical behaviour of the resonator. The capacitor C_m models the compliance (flexibility), the inductor L_m models the mass of the membrane, and R_m represents the mechanical dissipation. The energy dissipated in this R_m is thus responsible for producing the ultrasound pressure wave (including the other losses associated with the transducer), and dominated the impedance at resonance. Inspecting the BVD model the total impedance can be described using equation 2.1.

$$Z_{BVD} = \frac{1}{j\omega C_p} \cdot \frac{(j\omega)^2 L_m C_m + j\omega R_m C_m + 1}{(j\omega)^2 L_m C_m + j\omega R_m C_m + 1 + \frac{C_m}{C_p}} \tag{2.1}$$

The impedance shows a band pass (BP) behaviour that is characterized by the series and parallel resonance frequencies associated with the two parallel branches. The series and parallel resonance frequencies are given in Equations 2.2 and 2.3 respectively.

$$\omega_s = \sqrt{\frac{1}{L_m \cdot C_m}} \tag{2.2}$$

$$\omega_p = \omega_s \cdot \sqrt{1 + \frac{C_m}{C_p}} \tag{2.3}$$

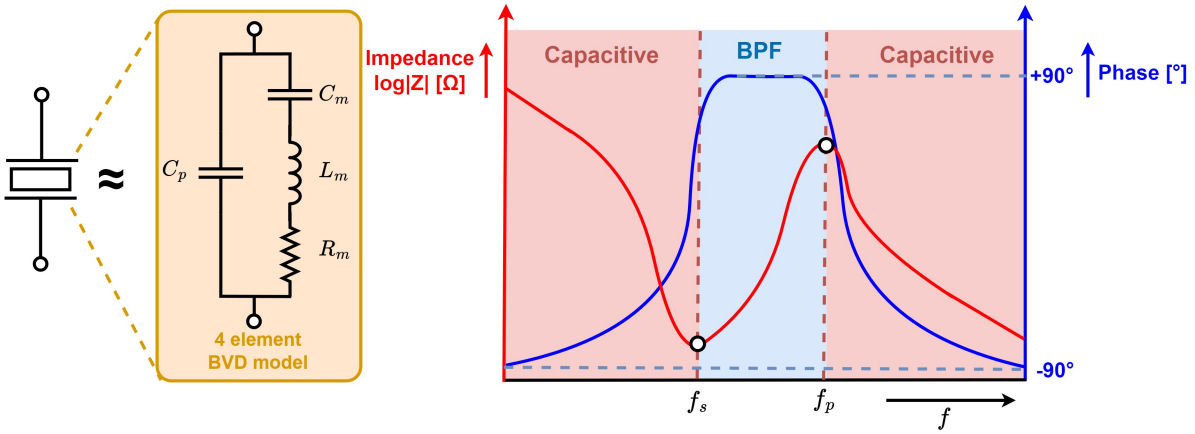

Figure 2.6: Approximation of the transducer with a BVD model (left) and its corresponding frequency behaviour (right).

2.4. Feasability study

2.4.1. Energy efficiency analysis

Linearized model and operation principle

The goal of this design is to obtain an energy-efficient HV pulser. In order to estimate the theoretical energy efficiency a simplified analysis is performed following some assumptions. First, the transducer is considered to be an ideal capacitor C_p for now, which receives energy from an ideal inductor L.

The simplest implementation of the resonant pulser core is shown in Figure 2.7. Here four switches S_1, S_2, S_3, and S_4 are modeled as an ideal switch with a series R_{on}. The switches S_1 and S_2 can be implemented with low voltage (LV) transistors while S_3 and S_4 are HV transistors. For now the associated switching losses of the transistors and their required gate drivers and level shifters are ignored. In Figure 2.7 the associated timing diagram of this simplification of the resonant pulser is shown. Here the main 5 operational phases of the resonant pulser are shown. In the third phase ϕ_{hold} the switches S_2 and S_4 are switched momentarily in order to properly discharge any residual energy left on the inductor. Here both the charging and recycling phases are considered ideal. This implementation only shows a single-element transducer pulser without the ability to receive echoes.

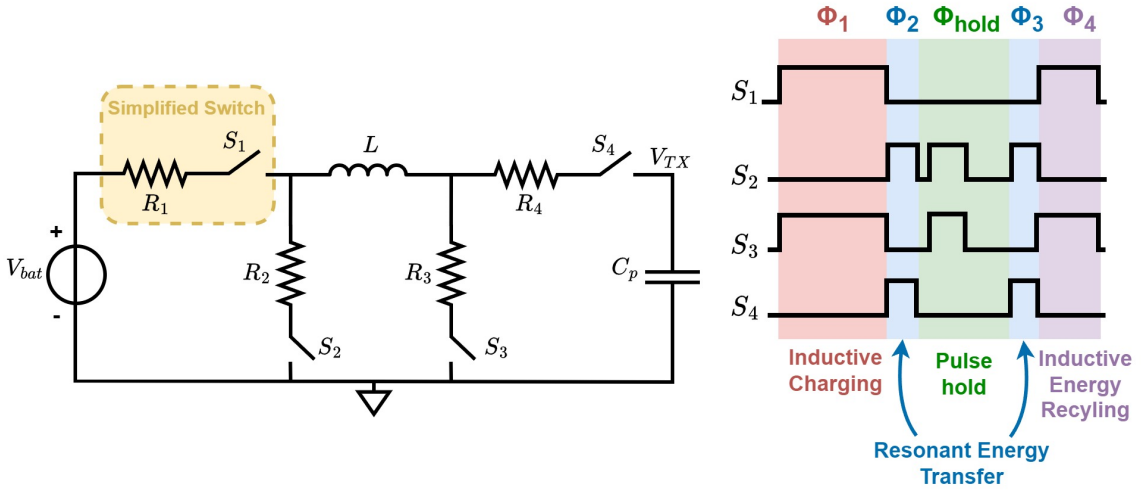

Figure 2.7: Simplified circuit model of the resonant pulser core and its simplified timing diagram.

During the first charge phase, the inductor current I_L increases approximately linear by a rate equal to $\frac{V_{bat}}{L}$, where V_{bat} is the input battery voltage of the system. In the time period of the first phase T_{Φ_1} the inductor is charged to a peak current of I_{pk}. At the end of the charging period, the total energy stored on the magnetic field of an ideal inductor equals LI_{pk}^2. In the following operational phase, the energy in the inductor magnetic field is transferred to the transducer due to the resonance between L and C_p at a frequency $f_0 = \frac{1}{2\pi\sqrt{LC_p}}$. This leads to a sinusoidally increasing and decreasing transducer transmit voltage V_{TX}. Ideally $\phi_2 = \phi_3 = \frac{1}{4f_0} = \frac{\pi}{2}\sqrt{LC_p}$ in order to completely transfer all inductive energy to the transducer and vise versa. This would then lead to a transmit voltage of:

$$V_{TX} = \frac{T_{\phi_1}}{\sqrt{L \cdot C_p}} V_{bat} = 2\pi T_{\phi_1} f_0 V_{bat} \tag{2.4}$$

This already shows some important properties of the resonant pulser. First, the transmit amplitude can be controlled by controlling the timing of the circuit. Second, the transmit amplitude can exceed the low input voltage of the circuit and create a much higher transmit pulse without requiring a dedicated HV supply. Typically the transducer is driven with pulses near/at its resonance frequency, this would lead to $T_{\phi_{hold}} = \pi\sqrt{L_m C_m}$. The time period of ϕ_{hold} is limited in the extreme case where $T_{\phi_{hold}} = 0$. In this case, the resonant energy transfer frequency f_0 equals the transducer resonance frequency f_s which leads to a limit on both L and C_p equal to $L_m C_m = LC_p$. The shape of the generated pulse has consequences on the transmitted acoustic energy. Since the frequency response of the transducer has a band pass filter (BPF) characteristic, the energy falling in the passband of the transducer is the energy that is translated in acoustic power. Both the pulse width and the number of consecutive pulses alter the amount of energy dissipated in R_m. Sending a short pulse train of 2 or 3 pulses is a common technique used to increase the peak pressure of the ultrasound wave [23]. This would also lead to a maximum time period for both T_{ϕ_1} and T_{ϕ_4} in case only a single inductor is used.

Inductive charging phase

First, the influence of the size of L, C_p, and f_s are investigated in relation to the total pulser energy efficiency before the implementation for both the transducer and the switches is discussed. In the first charging phase ϕ_1, the circuit forms an RL series circuit from which we can determine the charging time T_{ϕ_1} from the inductor peak current I_{pk} as follows:

$$V_{R_{\phi_1}} = V_{bat} \cdot \frac{R_{\phi_1}}{R_{\phi_1} + sL} \cdot \frac{1}{s} \tag{2.5}$$

Where $R_{\phi_1} = R_1 + R_3$ and $V_{R_{\phi_1}} = I_{pk} R_{\phi_1}$. Rewriting (2.5) the total amount of energy supplied and dissipated in this phase E_{ϕ_1} is given in Equation 2.7.

$$T_{\phi_1} = -ln\left(1 - \frac{I_{pk} R_{\phi_1}}{V_{bat}}\right) \cdot \frac{L}{R_{\phi_1}} \tag{2.6}$$

$$E_{\phi_1} = \int_0^{T_{\phi_1}} I_{\phi_1}(t)^2 R_{\phi_1} dt \tag{2.7}$$

The current $I_{\phi_1}(t)$ can be determined by applying Kirchoff's current law which gives:

$$L\frac{dI_{\phi_1}(t)}{dt} + R_{\phi_1} I_{\phi_1}(t) = V_{bat} \tag{2.8}$$

$$I_{\phi_1}(t) = \frac{V_{bat}}{R_{\phi_1}}\left(1 - e^{-\frac{R_{\phi_1}}{L} T_{\phi_1}}\right)$$

Substitution then leads to:

$$E_{\phi_1} = \frac{V_{bat}^2}{R_{\phi_1}}\left(\frac{2R_{\phi_1}T_{\phi_1}}{R_{\phi_1}} - \frac{3L}{R_{\phi_1}} + \frac{4Le^{-\frac{R_{\phi_1}}{L}T_{\phi_1}} - \frac{2R_{\phi_1}T_{\phi_1}L}{L}}{R_{\phi_1}} - \frac{L}{R_{\phi_1}} e^{\frac{-2R_{\phi_1}T_{\phi_1}}{L}}\right) \tag{2.9}$$

$$E_{\phi_1} = \frac{V_{bat}^2}{R_{\phi_1}}\left(T_{\phi_1} + \frac{2L}{R_{\phi_1}} e^{-\frac{R_{\phi_1}}{L}T_{\phi_1}} - \frac{L}{2R_{\phi_1}} e^{-\frac{2R_{\phi_1}}{L}T_{\phi_1}} - \frac{3L}{2R_{\phi_1}}\right)$$

The total amount of energy that is stored in the inductor at the end of the charging phase E_L is given by:

$$E_L = \frac{1}{2} L I_{pk}^2 \tag{2.10}$$

The total amount of energy delivered from the input source E_{boost} is then defined as:

$$E_{boost} = E_{\phi_1} + E_L \tag{2.11}$$

Resonant energy transfer and hold phase

In phase ϕ_2 the magnetic energy stored in the inductor is transferred by resonance to the transducer, and the energy stored on the transducer E_{cap} (which is now approximated only as a single capacitor C_p) is then given by:

$$E_{cap} = C_p(V_{TX}^2 - V_{bat}^2) \tag{2.12}$$

For the correct operation of this phase, the goal is to achieve the rising edge of the pulse by using the first quarter of the oscillation that occurs during the resonant energy transfer. This means that the time T_{ϕ_2} is determined from the (undamped) resonance frequency ω_0 and the total resistance in the current path R (=R_{ϕ_2}):

$$T_{\phi_2} = \frac{\pi}{2\omega_d} \tag{2.13}$$

$$\text{where} \quad \omega_d = \omega_0\sqrt{1-\zeta^2}, \quad \omega_0 = \frac{1}{\sqrt{LC_p}} \quad \text{and} \quad \zeta = \frac{R}{2}\sqrt{\frac{C_p}{L}}$$

In this phase, the total resistance in the current path equals $R_{\phi_2} = R_2 + R_4$. Then the total amount of dissipated energy in this cycle E_{ϕ_2} is given by:

$$E_{\phi_2} = \int_0^{T_{\phi_2}} I_{\phi_2}(t)^2 R_{\phi_2} dt \tag{2.14}$$

The current I_{ϕ_2} is then simply described by the damped resonance oscillation and the corresponding time constant $\tau = \frac{L}{R_{\phi_2}}$. Substitution then yields:

$$E_{\phi_2} = \int_0^{T_{\phi_2}} (e^{-\frac{R}{2L}t} \cdot cos(\omega_d t))^2 R_{\phi_2} dt \tag{2.15}$$

$$E_{\phi_2} = \frac{L \cdot e^{-\frac{R}{L}T_{\phi_2}}(2LR_{\phi_2}\omega_d \cdot sin(2T_{\phi_2}\omega_d)) - R_{\phi_2} \cdot cos(2T_{\phi_2}\omega_d) + \omega_d(4L^2 \cdot e^{\frac{R}{L}T_{\phi_2}} - 4L^2) + 2R_{\phi_2}^2 e^{\frac{R}{L}T_{\phi_2}} - R_{\phi_2}^2}{2(4L^2\omega_d^2 + R_{\phi_2}^2)}$$

At the end of the cycle ideally, all energy from the inductor is transferred perfectly to the transducer, the peak inductor current can then also be found from the following expression

$$\frac{1}{2}LI_{pk}^2 = E_{\phi_2} + \frac{1}{2}E_{cap} \tag{2.16}$$

Now the peak current I_{pk} that the inductor has to be charged to achieve a desired output voltage can be derived using the fact that the total amount of energy stored on the inductor E_L is equal to the total amount of energy dissipated in phase ϕ_2. The amount of energy left on the transducer equals $\frac{1}{2}E_{cap}$. From this one can obtain:

$$I_{pk} = \sqrt{\frac{C_p(V_{TX}^2 - V_{bat}^2)}{L - 2E_{\phi_2}}}$$

In the subsequent phase ϕ_{hold} the transducer is left floating, in case the transducer is modeled capacitively the transmit voltage would remain constant during the entire cycle. After this cycle, the energy is transferred back to the inductor in phase ϕ_3. During this phase, the total resistance in the path of the current equals $R_{\phi_3} = R_{\phi_2}$. The charge on the transducer is flown back to the inductor which gives rise to a peak current $I_{pk,2}$ for which hold $I_{pk_2} < I_{pk}$. The total energy that is present on the inductor at the end of the cycle can be used to find $I_{pk,2}$ similar to the derivation done in ϕ_2.

$$\frac{1}{2}LI_{pk,2}^2 = \frac{1}{2}E_{cap} - E_{\phi_{hold}} \tag{2.17}$$

$$I_{pk,2} = \sqrt{\frac{C_p(V_{TX}^2 - V_{bat}^2) - 2E_{\phi_{hold}}}{L}}$$

Where $E_{\phi_{hold}}$ amounts to the total dissipated energy in the phase, the time duration of this phase equals $T_{\phi_3} = T_{\phi_2} = \frac{\pi}{2\omega_d}$.

$$E_{\phi_3} = \int_0^{T_{\phi_3}} \left(\frac{V_{TX} - V_{bat}}{\omega_d L} \cdot e^{-\frac{R}{2L}t} \cdot sin(\omega_d t)\right)^2 R_{\phi_3} dt \tag{2.18}$$

$$E_{\phi_3} = \frac{e^{\frac{R}{L}T_{\phi_3}}(V_{TX} - V_{bat})^2(R_{\phi_3}^2 \cdot cos(2T_{\phi_3}\omega_d) - 2LR_{\phi_3}\omega_d \cdot sin(2T_{\phi_3}\omega_d) + (4L^2 \cdot e^{\frac{R}{L}T_{\phi_3}} - 4L^2) - R_{\phi_3}^2)}{2LR_{\phi_3}\omega_d^2(4L^2\omega_d^2 + R_{\phi_3}^2)}$$

Inductive energy recycling phase

In the final operation phase ϕ_4 the magnetic energy on the inductor is recycled back to the source. The discharge time of the inductor follows again an RL series decaying exponential which can be described as:

$$\frac{V_{bat}/R_{\phi_4}}{I_{pk,2}} = e^{-\frac{R}{L}T_{\phi_4}} - 1 \tag{2.19}$$

Here the resistance $R_{\phi_4} = R_{\phi_1}$. Rewriting equation 2.19 then yields the total recycling time needed to perfectly recycle all energy back to the source, T_{ϕ_4}.

$$T_{\phi_4} = -\frac{L}{R} log\left(\frac{\frac{V_{bat}}{R_{\phi_3}}}{I_{pk,2} + \frac{V_{bat}}{R_{\phi_3}}}\right) \tag{2.20}$$

Then the total dissipated energy during the recycling processes due to the finite on-resistance of the switches E_{ϕ_4} is given by:

$$E_{\phi_4} = \int_0^{T_{\phi_4}} \left(\frac{-V_{bat}}{R_{\phi_4}} + e^{-\frac{R_{\phi_4}}{L}T_{\phi_4}} \cdot \left(I_{pk,2}^2 + \frac{V_{bat}}{R_{\phi_4}}\right)\right)^2 R_{\phi_4} dt \tag{2.21}$$

$$E_{\phi_4} = \frac{e^{-\frac{2R_{\phi_4}}{L}T_{\phi_4}} \cdot \left(\left(2R_{\phi_4}V_{bat}^2T_{\phi_4} - 3LV_{bat}^2 - 2I_{pk,2}^2LR_{\phi_4}V_{bat} + I_{pk,2}^4LR_{\phi_4}^2\right) \cdot e^{\frac{2R_{\phi_4}T_{\phi_4}}{L}}\right)}{2R_{\phi_4}^2} + \frac{e^{-\frac{2R_{\phi_4}}{L}T_{\phi_4}} \cdot \left(\left(4LV_{bat}^2 + 4I_{pk,2}^2LR_{\phi_4}V_{bat}\right) \cdot e^{\frac{R_{\phi_4}T_{\phi_4}}{L}} - LV_{bat}^2 - 2I_{pk,2}^2LR_{\phi_4}V_{bat} - I_{pk,2}^4LR_{\phi_4}^2\right)}{2R_{\phi_4}^2}$$

Now we define the total recycled energy in 1 pulse $E_{recycled}$ to be equal to:

$$E_{recycled} = \frac{1}{2}LI_{pk,2}^2 - E_{\phi_4} \tag{2.22}$$

Finally, a measure for the total amount of energy it would cost to produce a single pulses E_{pulse} to be equal to:

$$E_{pulse} = E_{boost} - E_{recycled} \tag{2.23}$$

And in order to compare the quantity in regards to a traditional square wave pulser the energy is normalized to CV^2 and becomes:

$$E_{pulse,CV2} = E_{pulse}/E_{cap} \tag{2.24}$$

Total energy estimation

From the analysis that has been performed thus far a total energy consumption estimation can be made. For this, all series switch resistances are taken equal as $R_1 = R_2 = R_3 = R_4 = 5\Omega$. The input voltage $V_{bat} = 3.6V$ which is commonly used in lithium-ion cells. The battery voltage however varies as a function of the depth of charge of the battery and needs to be taken into account during the design of the pulser. Now in order to determine how different values of the transducer capacitance C_p and inductance L affect the total achievable energy efficiency of the resonant pulser the total supplied energy in the first charging phase E_{ϕ_1} and the total recycled energy $E_{recycled}$ are plotted in Figures 2.8 and 2.9 respectively. From this, the total energy supplied from the source to produce a single pulse is shown in Figure 2.10.

The results in figures 2.8, 2.9 and 2.10 show some important properties that will determine which transducer will be suitable for the resonant pulser to achieve high energy efficiency. Given an equal fixed resistance for each of the switches as done in the simulations, a larger capacitive load will lead to lower energy efficiency as expected. The size of the inductor (disregarding the resulting energy transfer resonance frequency due to C_p) shows that a larger inductor benefits the energy efficiency greatly. This is due to the fact that the generated output pulse amplitude scales approximately inversely with the square of the charged peak inductor current. The lower peak current in turn reduces the dissipation losses due to the finite on-resistances of the switches. This leads to the conclusion that the resonant pulser will be best suited toward low frequency pulsing ideally with an electric capacitance that is not very large. This however presents a trade-off in the choice of the transducer, a low resonance frequency is in some cases characterized by the device having a large mass. This translates often to a rather large electrical capacitance, requiring the design to pulse a large load and thus dissipate more energy. However, in case the losses can be made small the inductive energy recycling operation of the resonant pulser can still yield a high energy efficiency in case of a large C_p. The low-frequency transducer that was available is a 2.57MHz CMUT transducer. The electrical parameters of the device modelled to the

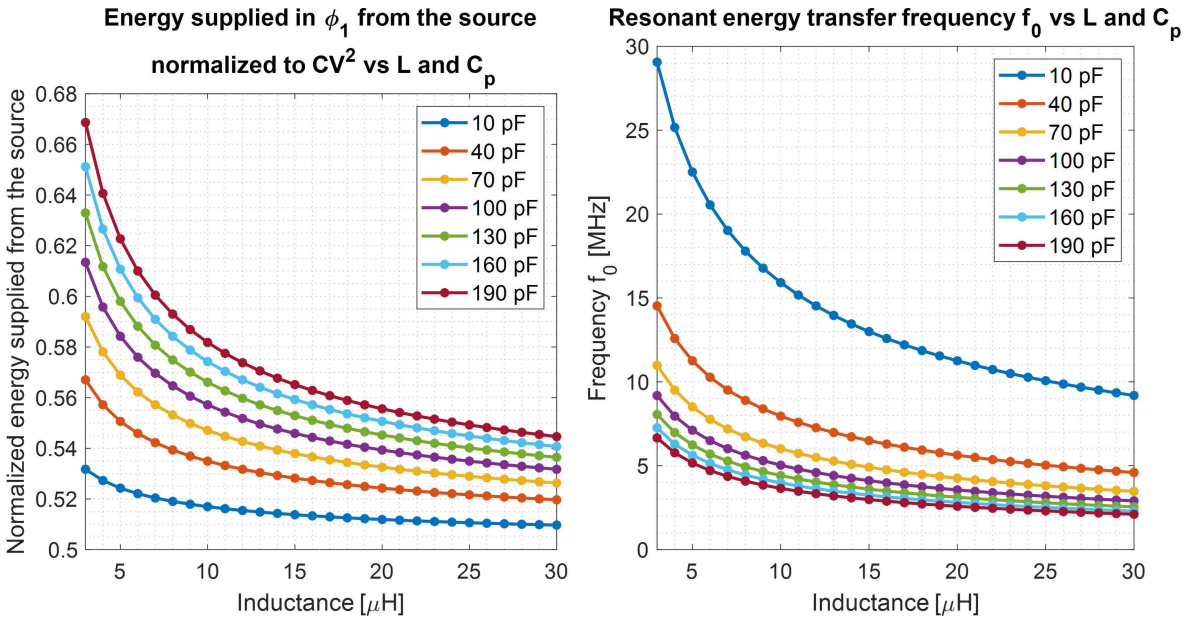

Figure 2.8: Plot of the calculated supplied energy in ϕ_1 and resulting resonance frequency f_0 for different transducer capacitance values C_p and inductance values, where $R = 5\Omega$, $V_{TX} = 30V$ and $V_{bat} = 3.6V$.

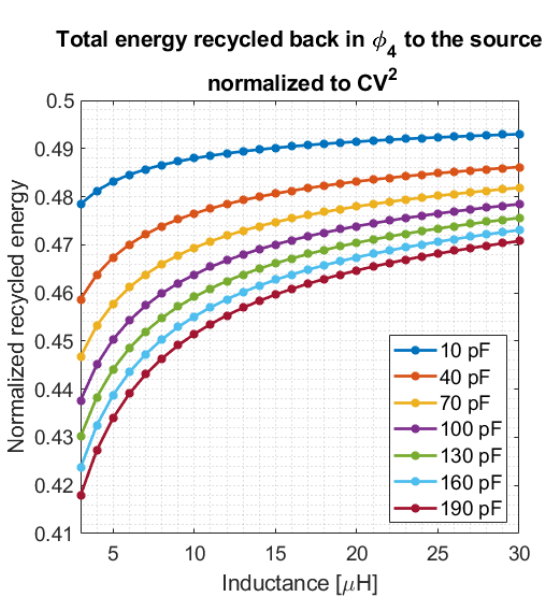

Figure 2.9: Plot of the calculated supplied energy in ϕ_1 for different transducer capacitance values C_p and inductance values, where $R = 5\Omega$, $V_{TX} = 30V$ and $V_{bat} = 3.6V$.

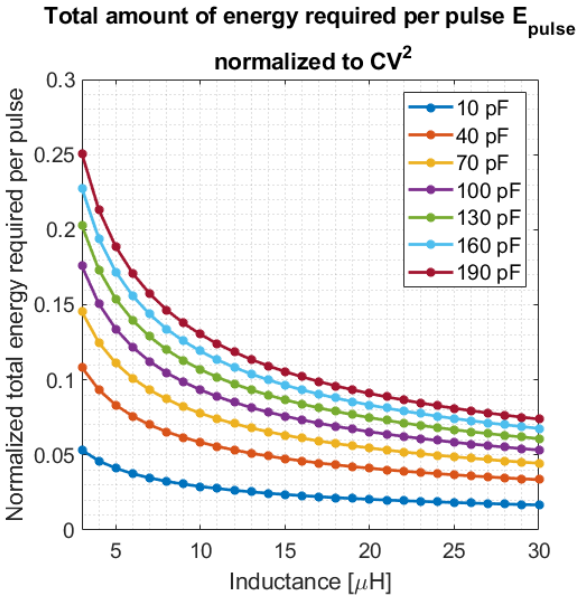

Figure 2.10: Plot of the total required energy per pulse normalized to CV^2 for different transducer capacitance values C_p and inductance values, where $R = 5\Omega$, $V_{TX} = 30V$ and $V_{bat} = 3.6V$.

BVD model are presented in Table 2.1. Figure 2.11 shows the impedance and phase measurements of the transducer for varying DC bias voltages, the CMUT is biased under nominal operation at $120V$. The electrical capacitance of the device is approximately equal to $118.8pF$.

Table 2.1: Low frequency 2.57MHz CMUT BVD model parameters

BVD model parameter	Value
C_p	$118.8pF$
C_m	$56.1pF$
L_m	$68\mu H$
R_m	1606Ω

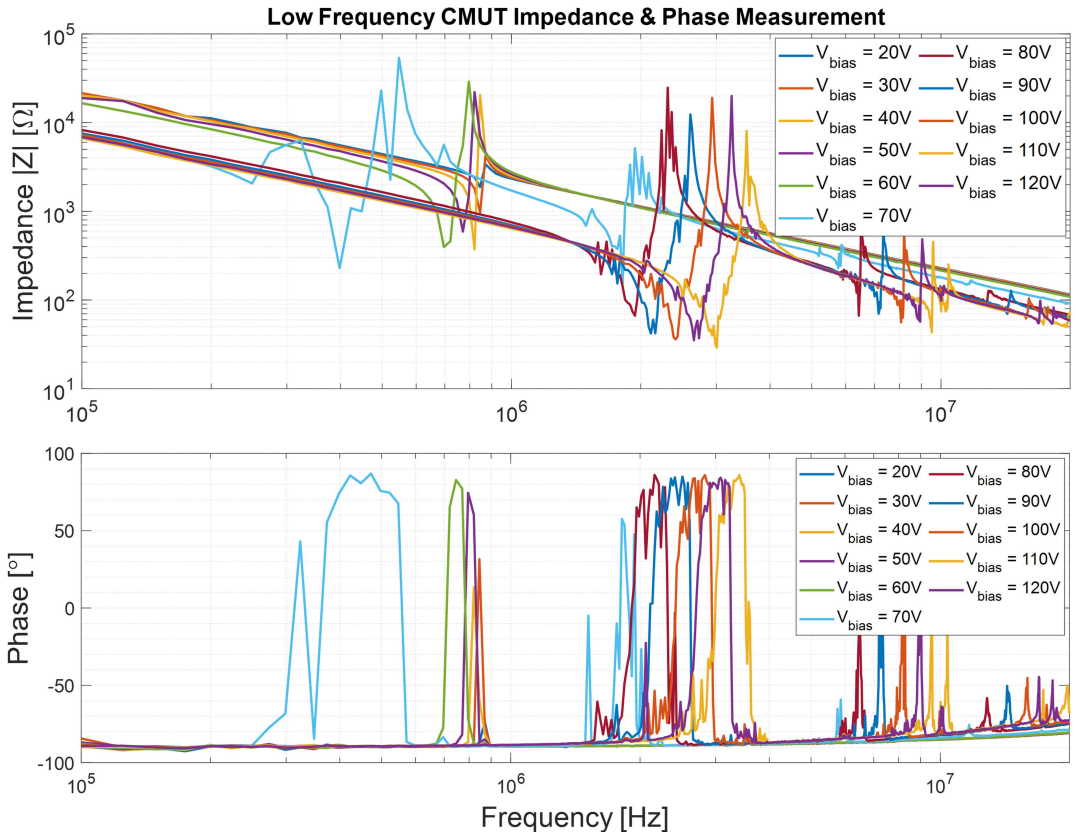

Figure 2.11: Impedance and phase measurements of the low frequency CMUT transducer for varying DC bias voltages.

2.4.2. Energy efficiency analysis with the BVD model

According to the BVD model parameters the maximum value of the inductor can be derived, this is the case for $L_m C_m = L C_p$ which yields $L \approx 32.1\mu H$. In order to choose a suitable size of the inductor and thus the resonant frequency used to transfer the energy from the inductor to the transducer f_0 the current assumption of an ideal capacitive load has to be reconsidered. Compared to prior art the resonant pulser does not have access to an HV supply, which means that during transmission the transducer is left floating and is not connected to a supply in order to generate the pulse. In terms of energy dissipated in the transducer (power dissipated in R_m) it does not create a big difference since practically the same package of energy is supplied to the transducer and dissipated during one cycle. The issue that arises here is the resulting parallel oscillation due to the mechanical branch that is introduced by the inductance L_m.

The BVD model that models the CMUT causes a damped RLC oscillation (parallel resonance) in case the transducer is left floating, and energy left on the electric field on the big electrical capacitor C_p is transferred to the parasitic inductance of the CMUT. This effect reduces the effectiveness of the inductive energy recycling proposed for the resonant pulser. The longer the hold phase of the pulse ϕ_{hold} the lower the transducer voltage V_{TX} becomes at the end of ϕ_{hold} due to the damped oscillation. The resulting generated peak current in the inductor during ϕ_3 is thus also reduced.

In order to model this in the MATLAB model that was used to perform the prior energy efficiency simulations an additional set of differential equations is used to calculate the resulting damped trans-

ducer oscillation. For this, an initial condition on the top node of the transducer BVD model is assumed with an equivalent capacitance equal to the parallel combination of C_p and C_m. An initial DC voltage ($v_{pk,initial}$) equal to the resulting peak transmit voltage that is reached at the beginning of the hold phase is calculated right before the transducer is left floating. The resulting damped oscillation $v_{osc}(t)$ can then be described as:

$$v_{osc}(t) = v_{pk,initial}\sqrt{1+\left(\frac{\alpha}{\omega_d}\right)^2} \cdot cos\left[\omega_d - arctan\left(\frac{\alpha}{\omega_d}\right)\right] \tag{2.25}$$

$$\text{with,} \quad \alpha = \frac{R}{2\alpha} \quad \text{and} \quad \omega_d = \sqrt{\omega_0^2 - \alpha^2} = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

Figure 2.12 shows what the voltage and current waveform would look like in case the transducer is modeled according to the BVD model. The reduced peak transducer output voltage $V_{TX,pk}[\phi_3]$ leads to less effective energy recycling due to the reduced peak current built up on the inductor $I_{pk}[\phi_4]$.

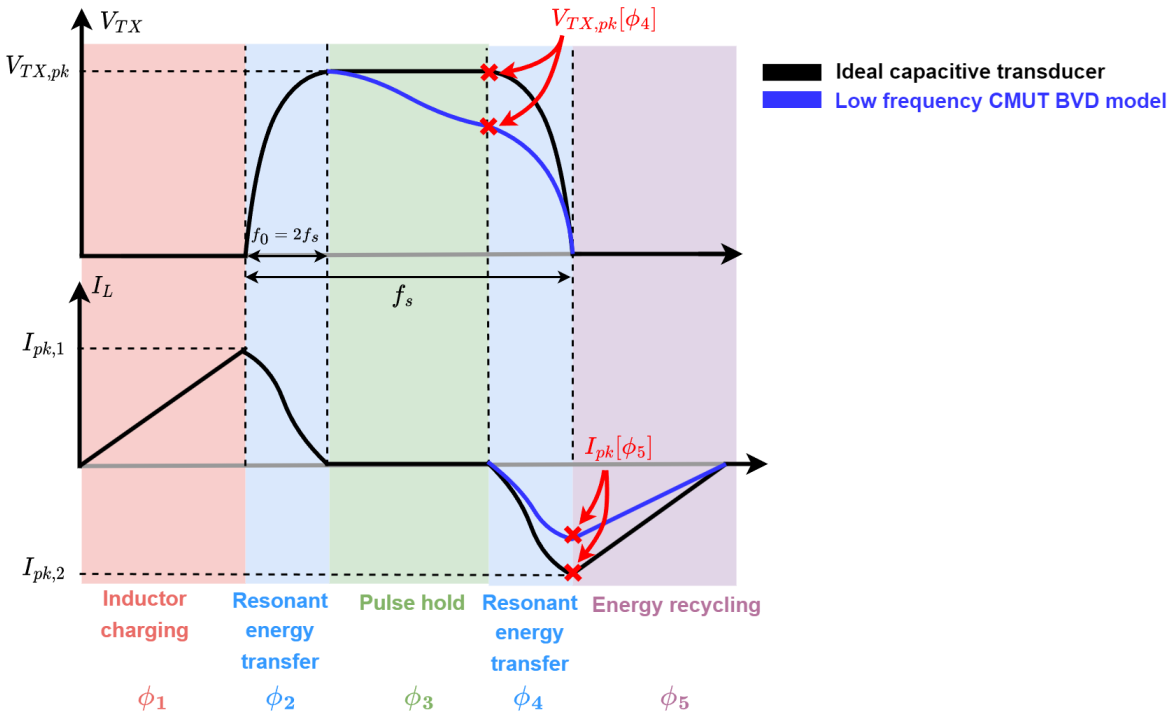

Figure 2.12: Example of the transducer voltage and inductor current waveforms showing the influence of a non-capacitive transducer.

Figure 2.13 shows the resulting $V_{TX,pk}[\phi_3]$ for varying L and thus varying f_0 given the low-frequency CMUT BVD model. Including this in the total energy efficiency simulation yields the results shown in Figure 2.14. The results show that choosing f_0 much smaller than f_s leads to a much less efficient design than previously presumed. Currently, only the dissipation losses are taken into consideration, the switches however need to be very large (especially the HV switches) in order to achieve sufficient low R_{on}. This will lead to considerable gate drive losses which will determine how large the switches need to be sized. Before that, the total amount of switches need to be determined by means of defining the topology of the pulser core.

From the results presented in this section the resonant pulser shows to be able to generate the required HV pulses for US imaging in an energy-efficient manner in case both the inductance L and thus in turn the resonance frequency used to transfer the energy f_0 are chosen sufficiently large and small respectively. The total resistance in the path of the current flow will be limited in the end by both the available chip area and the total gate drive losses which depend on both the sizes and amount of the devices and the type of device used.

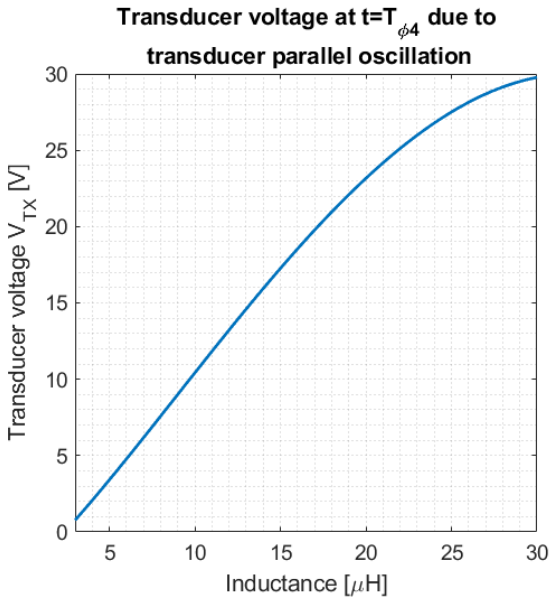

Figure 2.13: Resulting transducer voltage at the start of the recycling phase for $V_{TX} = 30V$ due to the parallel oscillation of the transducer modeled according to the BVD model by leaving the transducer float.

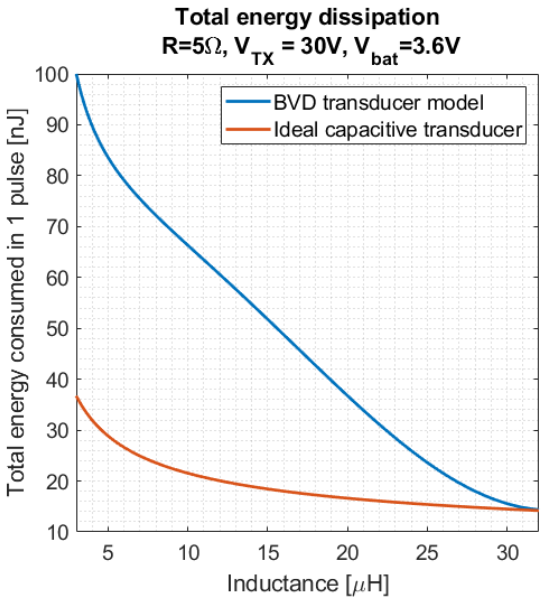

Figure 2.14: Plot of the calculated total energy required for 1 HV pulse for varying L (f_0) with the low frequency CMUT comparing the BVD model with an ideal capacitive transducer, for $R = 5\Omega$, $V_{TX} = 30V$ and $V_{bat} = 3.6V$.

2.5. High side switch configurations

The core of the pulser which has been shown earlier already consists of a minimum of 4 switches. Figure 2.15 shows a simplified circuit diagram of the proposed pulser core. The four switches implemented by transistors M_1, M_2, M_3 and M_4 are driven by both a gate driver and a LV level shifter. The level shifter interfaces the low voltage $1.8V$ control signals to $5V$. One of the difficulties in this design is to operate the high side HV switch M_4 (which could possibly either be a PMOS or NMOS HV transistor). As explained in an earlier chapter the HV devices in a BCD technology can only sustain the HV on their drain terminal, the gate of the device is still separated with a $5V$ limited thick oxide layer limiting the V_{GS} to $5V$. In prior art, an HV level shifter is often used in a conventional class-D pulser to operate the PMOS gate between $V_{DD,HV}$ and $V_{DD,HV} \pm 5V$ depending on either an NMOS or PMOS transistor is used. Since our goal is to omit the HV supply entirely another way has to be found to operate the high side HV switch.

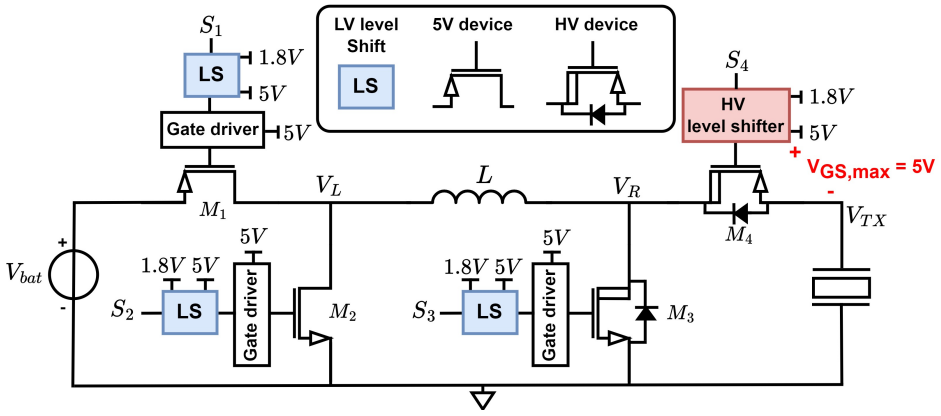

Figure 2.15: Simplified schematic of the proposed resonant pulser core, showing the minimum required 4 transistors needed for operation with an HV PMOS as high side switch.

From the previous analysis we can split the design of the resonant pulser core into two cases: the resonant pulser either operates with a hold phase ϕ_{hold} ($f_0 > f_s$) where a square-like pulse is generated,

or without a hold phase ϕ_{hold} ($f_0 = f_s$), where the resulting pulse is a half sine wave. In the first case, the high-side switch needs to be turned on and turned off when the energy from the inductor has been transferred to the transducer. On the other hand, in the second case, where we excite the transducer with a half-sine wave pulse, the high side switch only needs to be turned on to pass the energy from the inductor to the transducer and back. This could possibly lead to a smaller design. However, both designs offer advantages and disadvantages which will be discussed in the subsequent sections.

2.5.1. High side HV switch for $f_0 > f_s$

For the first case, where we want to create an HV square wave-like pulse, we need to turn the high side HV switch on and off in order to create the proper waveform. To make this operation possible without the need for an HV supply, a complementary switch structure is proposed. Figure 2.16 shows the structure of the switch on the right-hand side of the inductor together with its timing diagram. The parallel HV NMOS and PMOS transistors resemble a transmission gate, in addition to another HV NMOS M_{N2} and a $5V$ PMOS transistor M_{P2}. To understand the functionality of this circuit we first assume the following initial conditions: $V_N = 0V$ and $V_P = -5V$. Under these conditions, the high-side switch is turned on by applying a positive $5V$ signal on S_A pushing the top plate of capacitor C_1 and enabling PMOS M_{P1}. This happens when transistor M_3 is turned off after the inductive charging phase has been completed. After V_{TX} reaches its desired output voltage the PMOS is turned off by pulling S_A low. During the falling edge of the pulse the HV NMOS M_{N1} is enabled by pulling S_B high, and S_C is used to discharge node V_N after V_{TX} has reached $0V$ again. The diodes D_1 and D_2 are HV $5V$ Zener diodes. Now in order to obtain the desired initial conditions on nodes V_P and V_N an initial test pulse is generated. Initially, both nodes V_P and V_N are at ground potential meaning that M_{P1} is turned on. During the inductive charging phase M_{P1} is shorted by M_3. After M_3 is turned off the resonance energy transfer phase begins where the transducer gets charged. After V_{TX} has reached its peak value M_{P1} is turned off by applying a positive $5V$ voltage on S_A. At the same moment M_{N1} is turned on by applying a positive $5V$ voltage on S_B. After the transducer has been discharged M_{N1} is turned off by discharging node V_N. At this time node V_P has also been discharged through Zener diode D_1 however, at that moment S_A is still kept high. Now by pulling S_A low node V_P is pulled to $-5V$ turning off M_{P1}.

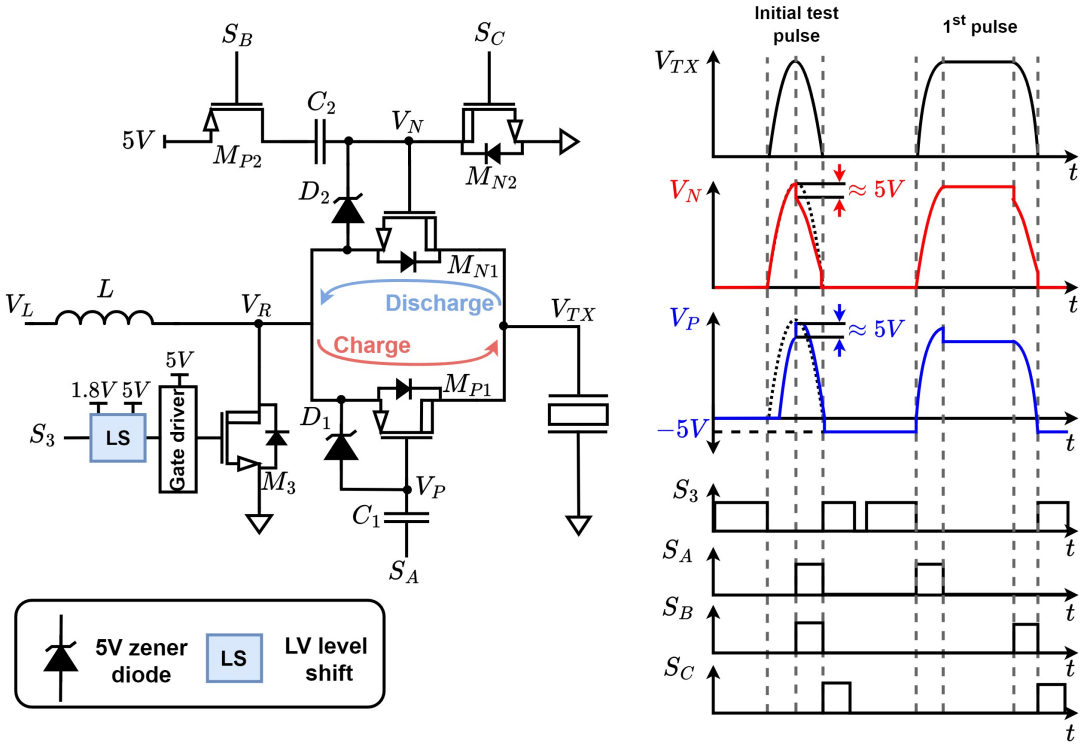

Figure 2.16: Schematic of the proposed high side HV switch that can operate for $f_0 > f_s$.

After the initial half sine test pulse the structure can be used to create the desired square wave-like waveforms. The proposed implementation of the high-side switch shows some obvious disadvantages compared to the ideal switch. In total 3 HV devices are required, even though M_{N2} can be sized small this still leads to a considerable amount of additional area. Besides the need for both an HV NMOS and PMOS are expensive for the amount of area they will consume since they will need to be sized large in order to minimize the losses in the circuit.

2.5.2. High side HV switch for $f_0 = f_s$

The second case that can be considered for the design of the resonant pulser core is pulsing at $f_0 = f_s$. This means that the resulting HV pulses are half sine waves. According to the prior energy efficiency simulation, operating the resonant pulser using the largest possible inductor leads to the lowest losses as one would expect. The resulting architecture however can be different from the prior case since there is no need to turn off the high side switch when V_{TX} reaches its peak value since the hold phase is omitted and the high-side switch is on during both ϕ_2 and ϕ_3. Besides the fewer switching events, other parts of the required system that are needed to operate the resonant pulser are less complex and more energy efficient, which will be highlighted in the next sections.

Since the high side switch only needs to be turned on during the HV operation the structure shown in Figure 2.17 is proposed. The structure shows a bootstrapped switch that is able to pass the inductor's energy to the transducer. The design is based on a similar design presented in [33], here an HV bootstrapped switch is used to pass external HV pulses to a transducer element in an IVUS probe. The high-side HV transistor M_4 is an NMOS transistor that is turned on by creating a $5V$ overdrive on its gate using a set of Zener diodes, capacitors, and one additional HV NMOS transistor M_{BS}. Zener diode D_2 and capacitor $C_{BS,2}$ are used to create a $V_{gs} = 5V$ on M_{BS}. This transistor is used to bias the gate of M_{BS} V_{G3}, at $5V$. This is done at a slight moment before the charging phase ϕ_1 is finished and thus turns on the high side HV transistor. Depending on the sizing of M_3 and M_4, the transducer voltage V_{TX} might rise slightly prior to the pulse being sent. When the switches M_1 (PMOS input transistor of the pulser) and M_3 close and the high voltage pulse is generated on the transducer, Zener diode D_1 and capacitor C_1 are responsible for keeping the gate of the high side switch at a $5V$ difference compared to the source terminal. After the pulse has been sent M_4 is turned off by M_{BS}.

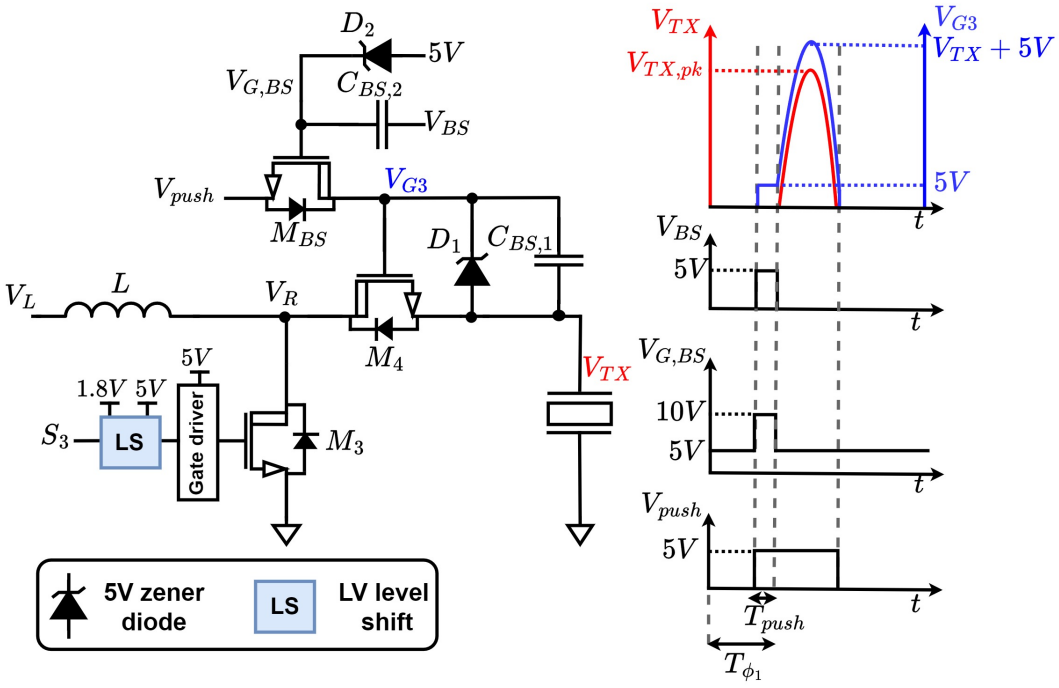

Figure 2.17: Schematic of the proposed high side HV switch that can operate for $f_0 = f_s$.

There are several design considerations that need to be taken into account for the proposed boot-

strap high-side switch structure. Unlike the prior topology shown in Figure 2.16, only a (large) HV NMOS transistor is required together with a small HV NMOS transistor, leading to a smaller footprint or lower dissipation losses since the switches can be sized larger. The transistor M_{BS} can be made very small (limited by the minimum size of the HV switch that will be chosen later on) which means that capacitor $C_{BS,2}$ can be sized small as well. However, this makes charging the node V_{G3} slower. Given the specification during the circuit design phase for the time T_{push} a minimum width for M_{BS} can be found. The large gate capacitance of transistor M_4 and capacitor $C_{BS,1}$ lead to a voltage division leading to a large capacitor $C_{BS,1}$ or a trade-off between the size of the high side switch. The resulting voltage division will in turn increase the on-resistance of the high-side switch.

In both designs, $5V$ Zener diodes are used to create and sustain the required $5V$ overdrive across the HV transistors together with a capacitor. These diodes unfortunately also require to be resistant against HV. The diodes occupy only a small active area compared to the required isolation and guard rings. Zener diode D_2 (in FIgure 2.17) can however be sized with smaller guard rings compared to Zener diode D_1 that sees the HV directly on its anode. Careful layout is required to make sure the resulting chip will be protected against latch-up-related issues.

2.6. Overall resonant pulser architecture

this section will present the architecture topology of the required circuits around the resonant pulser core in order to operate the pulser. Again as in the previous section, separate descriptions will be given for cases where the resonant pulser is operated with $f_0 > f_s$ and with $f_0 = f_s$. Afterwards, a comparison is drawn between the two cases and a choice is made for the resonant pulser topology.

2.6.1. Architecture considerations for $f_0 > f_s$

In order for the resonant pulser core to function, low-voltage electronics are placed around the core to fulfill all required operations such as operating the timing and control of the pulser. The most important functions that are required to be fulfilled by the other circuitry are detecting the zero current crossings of the inductor current and achieving the desired transmit voltage.

Pulse amplitude control

Since the resonant pulser achieves its desired transmit voltage by varying the inductor charging time the peak voltage detection can simply be done by measuring the pulser output voltage at a time $T_{V_{TX}}$. This timing moment can be set equal to around a quarter of the transducer resonance period in order to take a sample in the middle of the pulse. In order to measure the transducer output voltage an attenuator is required in order to interface with the LV electronics and avoid requiring additional HV devices. Figure 2.18 shows an example of a simplified architecture implementation.

In order to obtain the desired pulse amplitude the inductive charging phase ϕ_1 can be calibrated. The number of calibration cycles required depends on the size of the inductor, the circuit clock frequency f_{clk}, the transducer capacitance, and the input voltage. The maximum deviation of these parameters from their nominal values yields the required calibration period and the smallest time period yields the final resolution of the pulse amplitude. This would be equal to either the system clock frequency or a smaller time period in case a finer time base is used if required. For this, we can define the sensitivity of the resonant pulser as the required inductor charge time to obtain a $1V$ difference in pulse amplitude which approximates a linear function in the ideal case. The sensitivity of the resonant pulser is expressed in $[ns/V]$. According to the system specification, an sensitivity is required to yield a pulse amplitude accuracy of $\pm 300mV$. For the comparison process during calibration, a dynamic comparator could be used which is controlled by a control circuit that uses the resulting comparator output to adjust the inductor charging time. The sampling moment of the dynamic comparator can be done halfway through the pulse period.

Zero crossing detection

The second important task is to detect the zero crossings (ZCD) of the inductor current. Figure 2.18 shows the required timing moments that need to be detected. Due to the fast operation of the pulser ($2.5MHz$), the resulting time window to perform the ZCD is small. Triggering the ZCD too late or early will result in an error in the rising edge of the pulse or incomplete recycling of the inductor energy. The 50 MHz system clock is too coarse to be used in combination with a dynamic comparator. Using a much

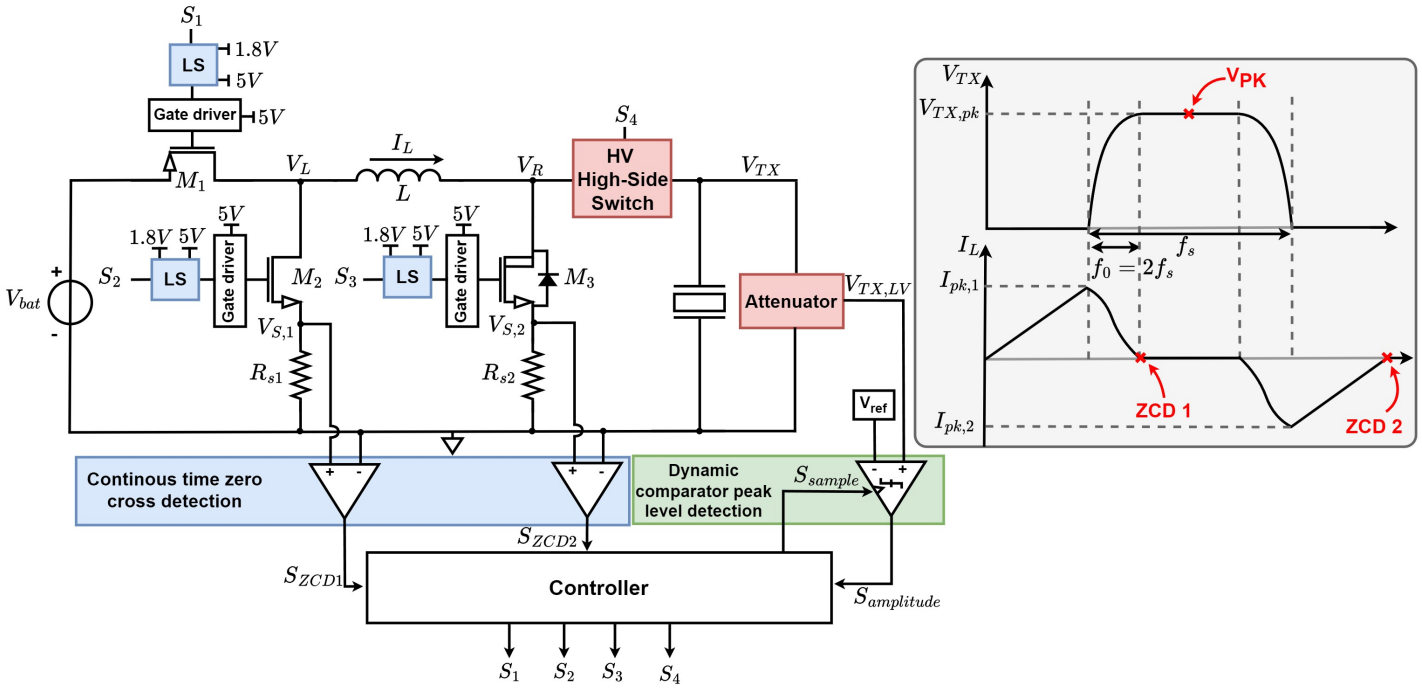

Figure 2.18: Simplified schematic of the proposed resonant pulser architecture that can operate for $f_0 > f_s$.

higher clock frequency or a clock multiplier (around a GHz) is not practical and will lead to considerable power dissipation. The other option is to use continuous time (CT) comparators. These comparators need a large bandwidth and low offset in order to produce the desired control signals. Figure 2.18 shows a simple implementation of these CT comparators which sense the inductor current across a small shunt resistor R_{s1} and R_{s2}. These resistors are in the current path of the resonant pulser core which means that their resistance needs to be very small ($\leq 1\Omega$) in order not to dominate the dissipation losses. Since the discharge rate of the inductor is rather high, early simulation results show that a zero crossing detection speed of only several ns is required, one will quickly come to the realization that implementing such high bandwidth amplifiers will inevitably lead to high power dissipation (simple implementations using a multistage 5 transistor OTA's show already current consumption around 10's mA).

One possible solution is to implement a slow CT comparator which is triggered at an offset at a timing moment δt_0 before the actual zero crossing. One method to implement this would be to accurately design the comparator delay or to add an offset at the input of the comparator. One problem would be to operate such a circuit around the variations in circuit and system parameters like the inductor size and input voltage. A static offset would in that case become useless, unless dedicated calibration is performed on the delay or offset.

Instead of comparing the sensed current to ground potential, a comparison could be made with a signal that is proportional to the rate of change of the discharging current. Figure 2.19 shows one possible implementation of such a solution. This could be achieved using a differentiator that is used to generate a trigger signal ΔV_{i_L} which in turn will yield a constant delay δt. The differentiator could be implemented either as a passive or active circuit and then either the delay of the comparator and/or the gain of the differentiator could be used to obtain an accurate zero cross-detection. However, the differentiator will also draw static power and require time to accurately settle. In case the inductor current remains constant during operation a high pass filter could be considered, this would still require a separate calibration circuit in order to set the propagation delay of the comparator to the desired time delay.

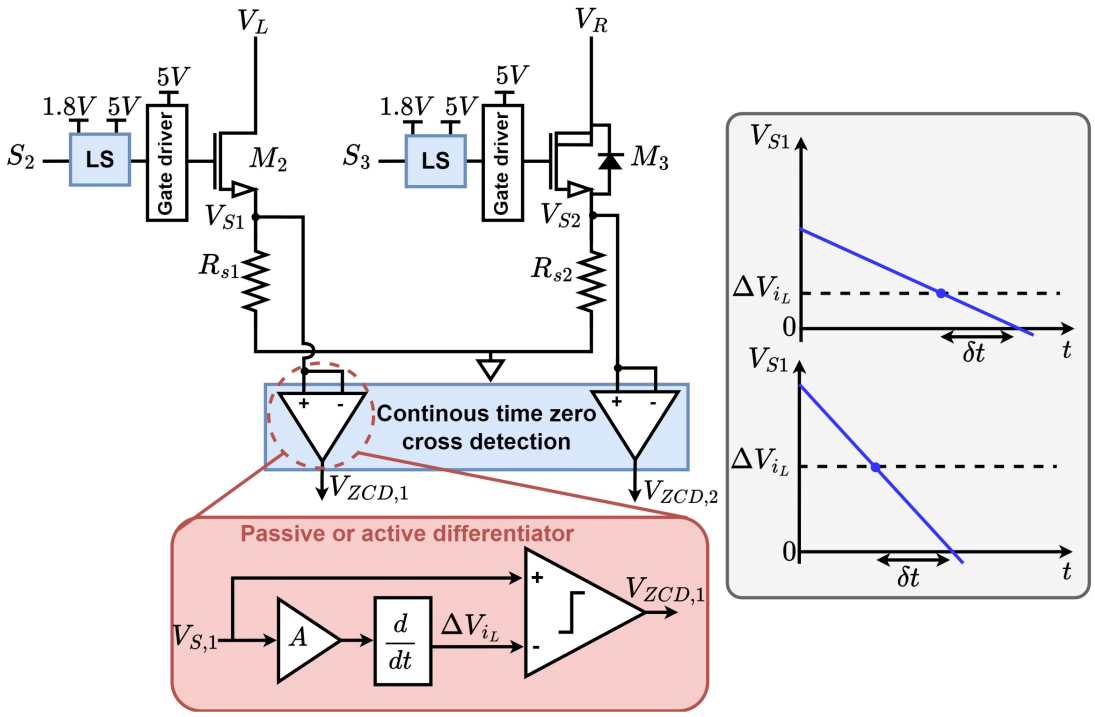

Figure 2.19: Zero cross detection based on creating a constant time delay using a differentiator.

2.6.2. Architecture considerations for $f_0 = f_s$

For the extreme case where the inductance of the resonant pulser is maximized leading to a pulser operating with $f_0 = f_s$ the energy efficiency estimation promises to be the highest when only considering the dissipation losses and a non-ideal transducer model. Figure 2.20 shows a simplified schematic of the proposed circuit architecture of the resonant pulser, pulsing at $f_0 = f_s$.

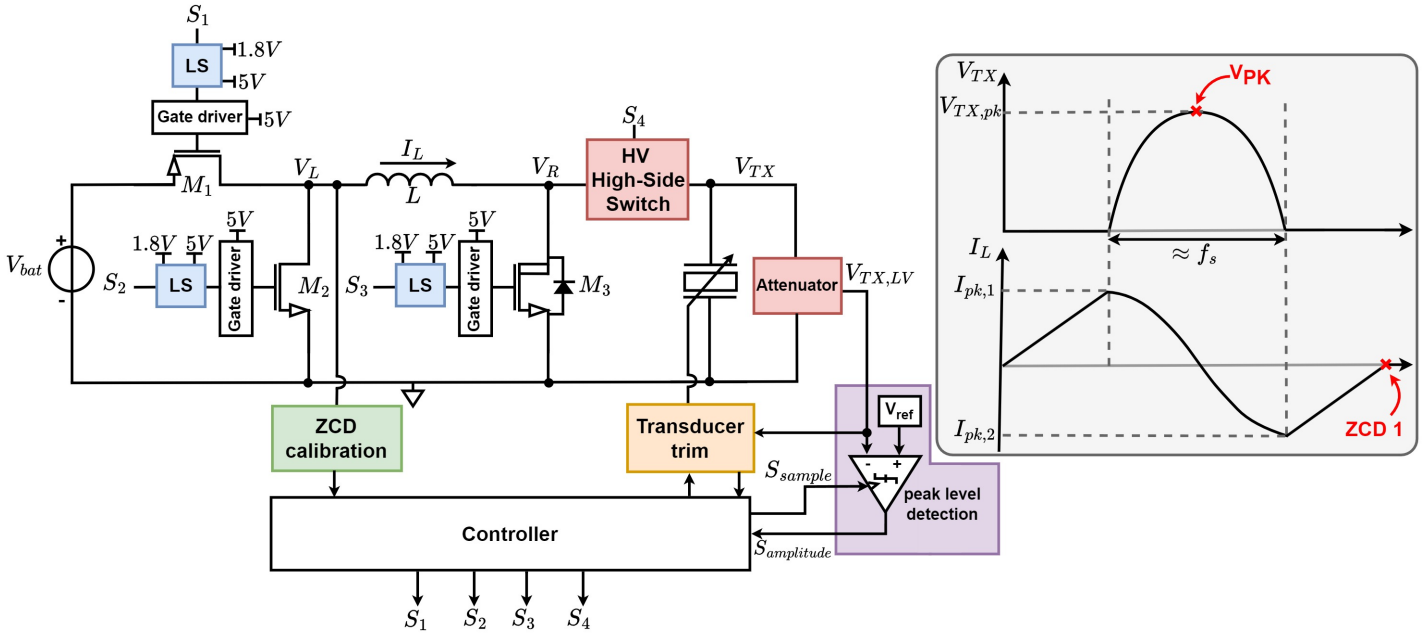

Figure 2.20: Simplified schematic of the proposed resonant pulser topology that can operate for $f_0 = f_s$.

The half-sine wave excitation of the transducer leads to a simpler system implementation compared to the prior case where $f_0 > f_s$. The only ZCD that has to be measured is at the end of the HV pulse during the energy recycling phase. The calibration of the transducer voltage can be performed by measuring the attenuated output voltage at a time equal to $0.5T_s$. Using the system clock frequency of 50MHz a $200ns$ wide pulse can be simply created and a sample can be taken at the rising edge of the 6th clock pulse. Using only the clock timing leads to a more elegant synchronous operation of the entire pulser.

One obvious problem that arises is that the design now requires trimming of the transducer capacitance C_p. In order to match the half-sine pulse close to $2.5MHz$ a trimming circuit needs to be added which can span a range that will cover the maximum deviation in both L and C_p. Furthermore, large parasitics (mainly from the HV devices) also need to be taken into account. The trim operation itself might also become a slight reliability issue. This can be understood from examining the proposed high-side switch implementation in the previous section. The body diode of the high-side HV NMOS transistor goes into forward bias in case the transducer voltage drops below the forward bias voltage of the diode (around $550 - 600mV$). This means that the trimming circuit needs to prevent this from occurring.

Calibration based ZCD

The ZCD, however, can be implemented more elegantly compared to the prior case. For this we exploit the fact that the pulser requires a short amplitude calibration cycle anyway. The ZCD timing can be calibrated by measuring the resulting voltage spike that occurs on the low voltage node of the inductor V_L. In case residual energy is left on the inductor the current generates a voltage spike across the large off-resistance of the LV transistors. The number of required calibration cycles and the required time step size need to be determined from simulation in order to keep the residual energy in the inductor at a minimum. The ZCD calibration itself can only be performed after amplitude calibration.

The calibration of the ZCD by sensing the voltage on node V_L cannot be used as easily in the prior case with the pulser design for $f_0 > f_s$. In case the first ZCD is triggered too late the resulting transducer peak voltage on the transducer still corresponds correctly to the peak current developed through the inductor in the charging phase. In this case, a peak detection circuit would be required to correctly measure the transducer peak voltage and perform the calibration. The problem occurs in case the first ZCD is taken too early. Now a situation arises where the measured V_{TX} is too low and the ZCD has measured to be taken too early. Now ambiguity exists since we don't know if the charged peak current in the inductor itself resulted in a too-low V_{TX} or that the early ZCD triggering resulted in the low V_{TX}, this shows that the two calibration phases cannot be performed orthogonal from each other. A possible solution would be to first make sure the ZCD is triggered always too late and calibrate V_{TX} first before the ZCD is calibrated. This could lead to many required calibration cycles which would be wasteful in an energy-limited US ASIC design.

2.6.3. Architecture comparison

From the discussion given in the previous two subsections on the different architecture considerations a suitable choice for the prototype ASIC can be made. Table 2.2 presents a list summarizing the most important advantages and disadvantages of the two architecture choices. Since the goal of this prototype for the resonant pulser is to obtain an energy-efficient HV US pulser that can be used in a portable battery-powered application and not in a high-end imaging system the advantages that the half-sine implementation offers do not outweigh the benefits the rectangular pulse like implementation offer. Hence the half-sine pulse implementation is chosen as the desired topology for the prototype ASIC.

Table 2.2: Comparison between the two resonant pulser architecture proposals.

Rectangular pulse architecture (with hold phase ϕ_{hold})	**Half-sine wave pulse architecture (without hold phase ϕ_{hold})**
$f_0 > f_s$	$f_0 = f_s$
$L < L_{max}$	$L = L_{max} \approx 32\mu H$
Possibility to generate pulse trains, better axial resolution	No possibility to generate pulse trains (unless two inductors are used in a ping-pong-like configuration)
High side switch requires both an HV PMOS and two HV NMOS	High side switch does not require an HV PMOS and requires only 1 additional HV NMOS.
Less energy can be recycled back	Excitation by half sine wave instead of rectangular aperture might have (slight) consequences for imaging quality (axial and lateral resolution)
More switching events per pulse cycle	Can be (much) more efficient due to lower energy dissipation per cycle, peak detection, and ZCD is more robust and possibly free of static power consumption
Needs (possibly much) more calibration cycles to obtain accurate ZCD	Requires trimming of the transducer elements
Less robust in terms of orthogonal amplitude and ZCD calibration	

2.6.4. Effect of component non-idealities

Inductor non-idealities

There are additional non-idealities that will affect the pulser efficiency during measurement. The first is the off-chip inductor: a real inductor will only behave as an inductive element for a limited frequency range. The frequency at which an inductor will start behaving as a capacitor is called the self-resonance frequency (SRF) of the inductor. This is modeled simply as a capacitor C_{SRF} which is in parallel with the inductance L. The inductor also has a finite DC resistance R_{DC} characterized as a series resistor to the inductor. The SRF, R_{DC}, and the physical size of the component are trade-offs with each other. The effect of the R_{DC} is obvious as it will increase the dissipation losses linearly in the resonant pulser since it is series with the current path, which lead to a requirement of having sufficiently low R_{DC} compared with the on-resistances of the switches in the resonant pulser core. The SRF impacts the total impedance of the resonant pulser and hence lowers the effectiveness of charging and discharging the inductor. During this resonant pulse period the capacitance of the inductor is in parallel with the transducer, hence increasing the total load capacitance and thus lowering the maximum achievable inductance. This will thus lead to lower energy efficiency.

In Figure 2.21 the impedance characteristics of a $30\mu H$ inductor with varying SRF is shown. The difference in impedance at $2.5MHz$ is plotted in Figure 2.22. From this it becomes clear that a high SRF is beneficial, however, this poses a trade-off with the DC resistance of the inductor. An SRF $> 4f_s$ seems reasonable to achieve combined with very low (non-dominant) R_{DC} for commercially available SMD inductors.

External transducer non-idealities

For the prototype ASIC the transducer's are connected externally to the ASIC. The external CMUT array connects via a long flex PCB cable. The resulting large inductance also needs to be taken into consideration, since a large inductance in the ground loop that connects to the ASIC can cause voltage ringing in the substrate.

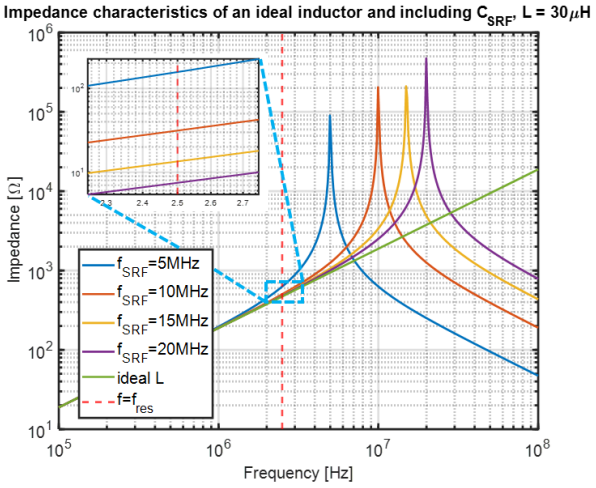

Figure 2.21: Impedance plot of an ideal inductor and including an SRF at different frequencies for $L = 30\mu H$.

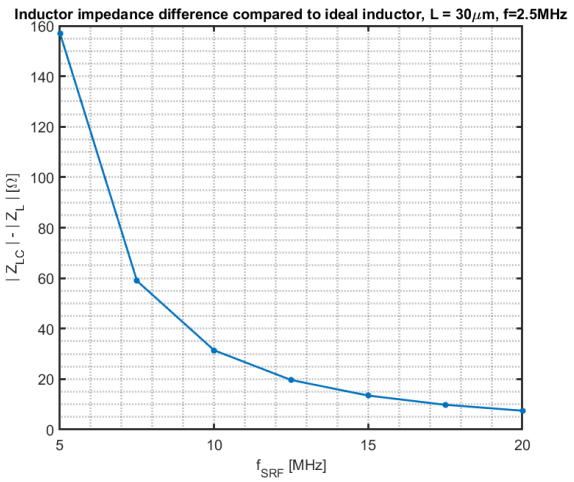

Figure 2.22: Total inductor impedance difference at $2.5MHz$ resonance frequency compared to an ideal inductor.

2.7. Gate drive losses and HV transistor choice

The final part of the architecture discussion is determining the sizing of the main switches of the pulser core. Previously, the energy efficiency calculations were only considering the dissipation losses associated wih the on-resistance of the switches. Of course, reducing these dissipation losses by increasing the switch size is limited by the gate drive losses required to switch the transistors. Since there is no specific area requirement for this design, the final sizing of the transistors will be kept to a reasonable size in order to make the argument that the pulser design can achieve high efficiency for larger arrays. The following analysis will show roughly how the dissipation and gate drive losses scale with the size of the different transistors.

The high-side LV PMOS and low-side HV NMOS are responsible for most of the dissipation losses that occur during the charging and discharging of the inductor. Besides, only the high-side HV transistor and bootstrap circuit are required per transducer, therefore it would be beneficial to size this part of the circuit smaller.

The gate drivers are driven by a low voltage level shifter. Its power consumption is neglected at this stage. The level shifter output forms the input capacitance seen at the input of the gate driver C_{in}, the output switch which the driver has to drive forms the load capacitance which equals the gate capacitance of the output switch C_{gg}. The number of required stages N in the driver will depend on the required switching speed and poses another trade-off with power dissipation. In order to make a first estimate an inter-stage fan-out f of 4 is chosen. From this, we can describe the number of required (even) stages as:

$$N = \log_f(F) \quad \text{, where} \quad F = \frac{C_{gg}}{C_{in}} \tag{2.26}$$

The amount of added dynamic power dissipation per switching event changes from $C_{gg}V_{DD,5V}^2$ to

$$\sum_{k=0}^{N} \frac{1}{4^{N-k}} C_{gg} V_{DD,5V}^2 \tag{2.27}$$

Figures 2.23 and 2.24 show the on-resistance R_{on} and total gate capacitance C_{gg} for varying transistor widths respectively. As expected, the on-resistance is inversely proportional to the transistor width and the gate capacitance scales linearly with the gate area. Besides the standard NLD HV DMOS transistors the TSMC BCD technology also offers special low R_{on} transistors. These transistors can only operate as switches which makes them good contenders for the main resonant pulser switches. For the $5V$ devices, the low on-resistance variant makes only a small difference in having a slightly lower R_{on} compared to standard $5V$ NMOS devices. For the HV devices, the difference is rather substantial, since the target pulsing voltage is at $30V$ the required voltage rating of these devices should be higher

than $30V$ due to the required calibration process of the pulse amplitude. For the design of the resonant pulser core the $40V$ NLD low R_{on} transistors are used for the high-side and low-side HV switches, and the HV transistor that connects to the gate of the high-side HV switch is implemented using the 45V NDL transistors due to its (considerable) smaller footprint for small transistor width.

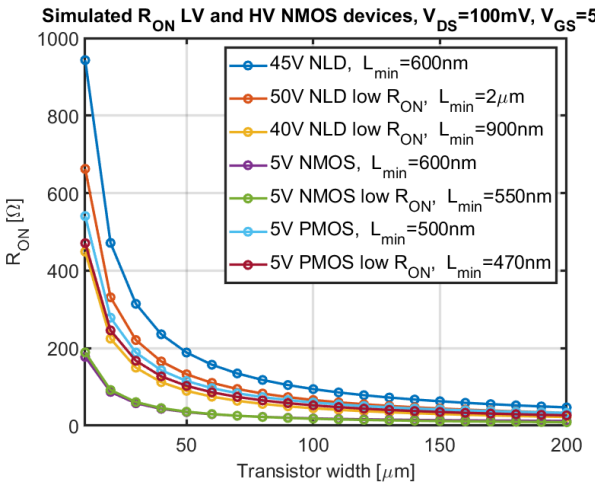

Figure 2.23: Simulated on resistance R_{on} for different NMOS devices and device width at minimum transistor length.

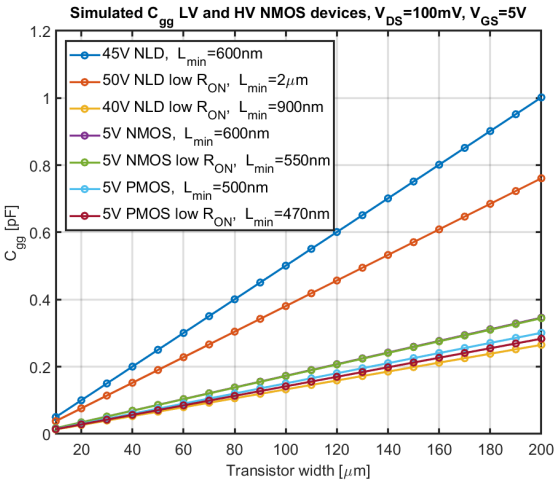

Figure 2.24: Simulated total gate capacitance C_{gg} for different NMOS devices and device width at minimum transistor length.

Figure 2.25 shows the result of including the gate drive losses during the operation of the resonant pulser. Here the previous extracted values of R_{on} and C_{gg} are used for each of the transistors. The width of one of the transistors is varied while the others are assumed to be kept at a constant width of $1000\mu m$. From these results, it becomes clear that the energy dissipation of the resonant pulser, especially for higher transmit pulses is dominated by the dissipation losses instead of the gate-drive losses. The contribution of the LV high side PMOS and the HV low side NMOS is most dominant as expected. Table 2.3 presents the sizing of each of the switches.

Table 2.3: Transistor types and sizes for the resonant pulser core switches (all transistor lengths are taken at minimum).

Transistor number	Transistor type	Transistor width
M_1	$5V$ low R_{on} PMOS	$1500\mu m$
M_2	$5V$ low R_{on} NMOS	$760\mu m$
M_3	$40V$ low R_{on} NLD NMOS	$1000\mu m$
M_4	$40V$ low R_{on} NLD NMOS	$3000\mu m$

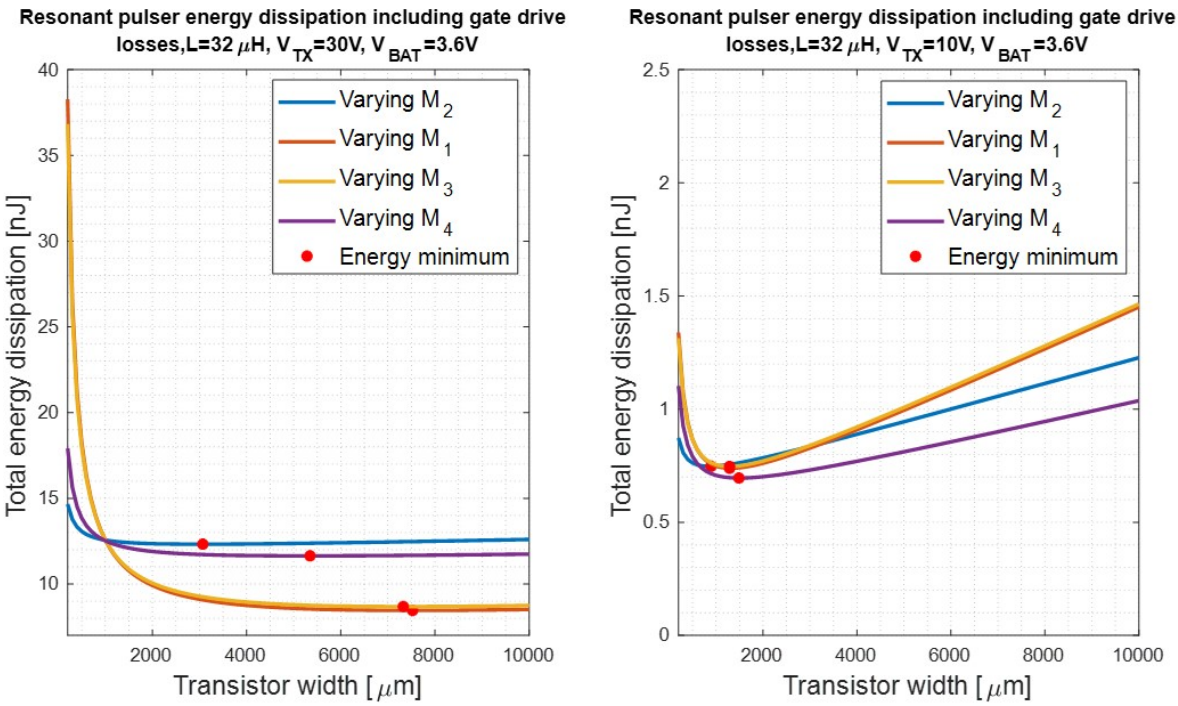

Figure 2.25: Calculated total energy dissipation of the resonant pulser including gate drive losses, here one of the four resonant pulser core transistor width is varied while the other are kept at a width of $1000\mu m$. The gate driver are assumed ideal with an inter-stage fan-out $f = 4$.

2.8. High-level system overview

Figure 2.26 shows a simplified schematic overview of the proposed architecture for the resonant pulser. Besides the previously discussed core of the pulser additional circuitry is required around the pulser in order to function correctly. Due to half sine wave excitation used to create the HV pulse a trimming circuit is required to match the total impedance during resonant energy transfer. Since the range of variation on both the transducer capacitance and off-chip inductor are rather larger, this will inevitably lead to a large trim network which will take up a considerable amount of chip area. Therefore it will be beneficial to create a trim network that can be shared among all channels since only one transducer can be pulsed at a time during transmit anyway.

Since only a single transducer is pulsed in one transmit cycle a large part of the total transmit circuit can be multiplexed in order to save a considerable amount of area. For this design, only the high side HV transistors M_4 and a small second HV transistor required for the bootstrap operation are required. This design thus eliminates the need for an HV PMOS device which saves a considerable amount of area, second, the high side HV transistor does not dominate the energy dissipation of the design compared to the low side HV transistor which means that the high side transistor can be sized considerably smaller per channel.

Both transmit amplitude and inductor zero current crossings are calibrated before the transmit can start. Each channel will also implement a transmit/receive (T/R) switch in order to receive echo signals. The scope of this thesis is limited to this point of the receive chain, the receive circuit will be implemented off-chip during measurements. The low voltage battery input is used in order to derive the required bias voltages/currents and in order to generate and regulate internal $1.8V$ and $5V$ supplies. All non-critical digital logic and all the control will be implemented off-chip for this prototype on an FPGA. This is done in order to maximize the testability of the chip.

For the prototype that will be designed in this thesis the amount of channels is limited to only 2 in order to show that the resonant pulser can perform a pulse-echo measurement. Besides this also another version will be designed which can only transmit on a single element and will not include the ability to receive echoes. This is done in order to show the maximum achievable energy efficiency of the resonant pulser, here the sizing of the main pulser will also be slightly different.

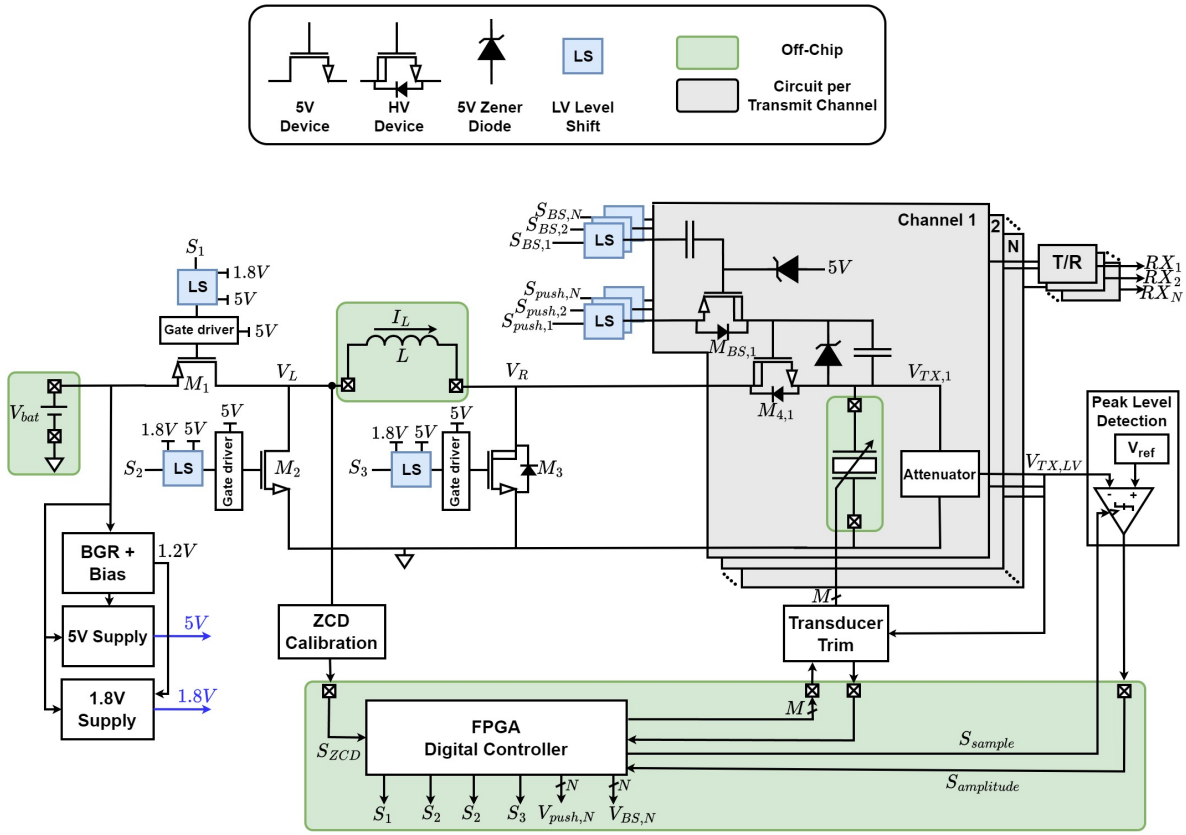

Figure 2.26: Simplified overview of the proposed architecture for the resonant pulser for N transmit channels.

3

Circuit level design

This chapter will discuss the circuit-level implementation of the resonant pulser. The different building blocks presented in the architecture-level analysis of the pulser are verified by means of simulation and a final energy efficiency simulation will show that the resonant pulser achieves energy efficiency lower than CV^2.

3.1. Resonant pulser core

This first section presents the proposed implementation of the core of the resonant pulser. Figure 3.1 shows a simplified circuit diagram of the proposed pulser core. To control switches M_1, M_2, and M_3 an LV level shifter is required in order to shift the $1.8V$ control signals to the $5V$ domain and an appropriate gate driver.

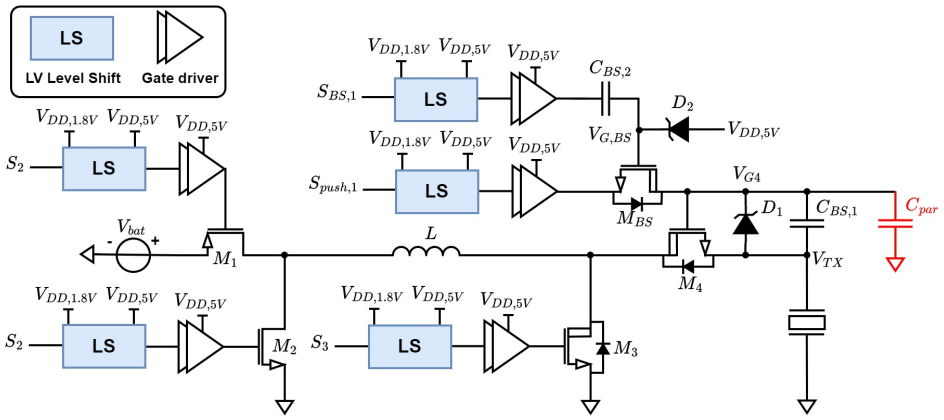

Figure 3.1: Circuit schematic of the resonant pulse core for 1 transmit channel.

The LV level shifters can be implemented either by a dynamic or a static architecture. Figure 3.2 shows the circuit implementation for a current mirror-based level shifter and a cross-coupled-based level shifter respectively [34], [35]. The current-mirror based level shifter employs a basic current mirror as a pull-up network, resulting in high current flow through the level shifter in case the output level is high. In order to minimize dissipation losses, the cross-coupled level shifter is implemented. It makes use of positive feedback in order to increase the switching speed of the level shifter and eliminates static current flowing through the circuit. In order to optimize the switching speed of the pulser's large transistors the cross-coupled level shifters were designed to obtain minimum delay, hence making a better trade-off in the required size of the gate driver to obtain proper switching speed. The importance of properly fast switching speed is further explained in the implementation of the trim circuit.

To control the high-side switch M_4 the HV level shifter is implemented as an HV bootstrap circuit, in which the capacitor $C_{BS,1}$ and $5V$ Zener diode D_1 maintain the required $5V$ overdrive while the HV pulse is generated. This capacitor is charged ideally to $5V$ using HV transistor M_{BS} shortly before the

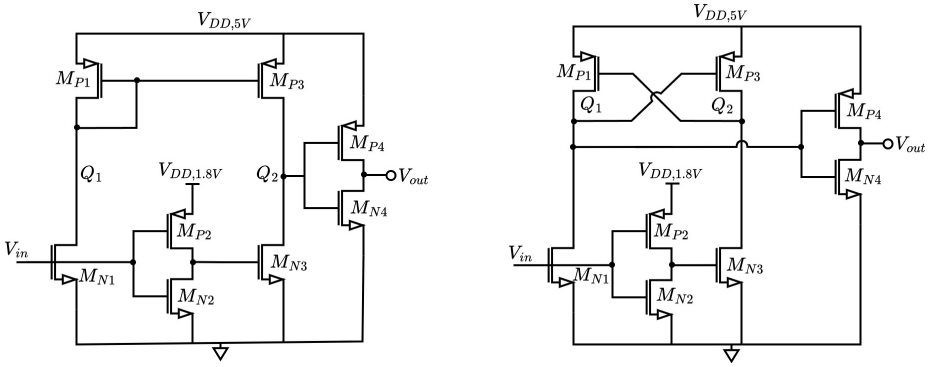

Figure 3.2: Circuit schematics of two types of LV level shifters, (left) current mirror-based architecture. (right) cross-coupled-based architecture [34], [35].

pulse is generated and is discharged after the pulse ends. M_{BS}, in turn, is turned on and off through a voltage-doubler consisting of Zener diode D_2 and capacitor $C_{BS,2}$. Mainly due to the parasitic drain capacitance of the transistor M_{BS} (C_{par} in Figure 3.1) the resulting overdrive voltage on M_4 will be smaller due to attenuation since a capacitive divider is formed, this can be described by:

$$V_{G4} = 5V \cdot \frac{C_{BS,1}}{C_{BS,1} + C_{par}} \tag{3.1}$$

In order to obtain sufficiently high overdrive, either capacitor $C_{BS,1}$ should be increased or M_4 should be decreased in size. Additionally, Zener diode D_1 adds additional parasitics in parallel to the transducer which reduces the efficiency of the pulser slightly. The diode also has guard and isolation rings sized properly to sustain voltages of $30V$. M_{BS} is implemented with a $45V$ NLD NMOS transistor instead of the $40V$ low R_{on} NMOS used for M_{3-4}, which is done since the $45V$ NLD NMOS consumes less area for small transistor widths. The resulting higher R_{on} and gate capacitance has very minimal influence on the resulting performance of the pulser. In order to charge and discharge node V_{G4} within a single clock cycle, M_{BS} is sized $30\mu m$ wide, $C_{BS,1}$ is implemented using a $10pF$ MIM capacitor and $C_{BS,2}$ as a $1pF$ MIM capacitor.

Finally, the gate drivers are simply implemented using $5V$ inverters where the gate driver of M_{1-2} are optimized for power whereas M_3 is optimized for speed. The gate drivers for the HV bootstrap circuit can be made small, Table 3.1 presents the fan-out and the number of stages used for the gate drivers.

Table 3.1: Gate driver sizes of the resonant pulser core.

Gate driver control signal	Number of stages	inter-stage fan-out
S_1	6	4
S_2	4	4
S_3	8	3.15
S_{push}	4	4
S_{BS}	2	4

Transistor number	Device dimensions
M_1	$W = 1500\mu m$, $L = 470nm$
M_2	$W = 760\mu m$, $L = 600nm$
M_3	$W = 3000\mu m$, $L = 900nm$
M_4	$W = 1000\mu m$, $L = 900nm$
M_{BS}	$W = 30\mu m$, $L = 600nm$

3.2. Transducer trim circuit

3.2.1. Transducer trim operation principle

Prior to the start of the transmit cycle, all the transducer elements in the array require trimming in order to compensate for the deviation in L and C_p and thus in their resulting resonance frequency. This trim operation is only required to be performed once after initial start-up and can be turned off afterward. The need for this initial trim is easily justified due to the relatively short operation cycle and very low duty cycle for the target application of US patches (total operation duration days or weeks with measurement intervals of tens of minutes) compared with additional long-term drift in C_p due to aging effects which can also occur. Therefore it is acceptable for the circuit to have relaxed requirements on its power consumption. Figure 3.3 shows the proposed circuit schematic for the transducer trim operation.

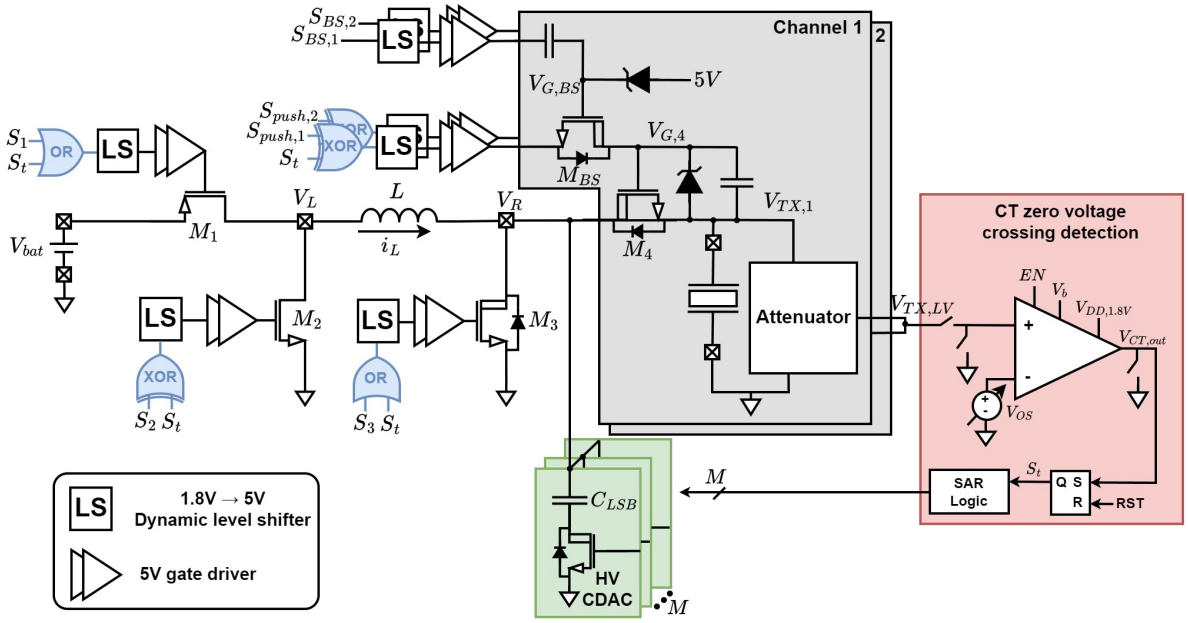

Figure 3.3: Simplified schematic of the transducer trim circuit.

The circuit uses three main blocks to function: a continuous time (CT) zero voltage detection circuit, a HV CDAC, and a few OR and XOR gates (and the associated digital logic). In order to trim the transducer a capacitive trim network is used in order to adapt the total load capacitance during pulsing, hence adjusting the pulse frequency to match the transducer's resonance frequency. The trim network can be implemented as an HV capacitive digital-to-analog converter (HV CDAC). A circuit that interfaces with the attenuated transmit pulse needs to detect if the resulting pulse width is shorter or longer than the target pulse width of $200ns$, so that a binary search can be performed in order to perform the trimming operation. For the CDAC implementation it is not convenient to add series capacitances in order to subtract capacitance in case L and C_p are larger than the target impedance. Any series capacitance added will also attenuate the HV pulse which is very wasteful during the operation of the pulser. Also, the implementation for the series switches which would be required is not trivial and could lead to large area consumption. Therefore the trim operation will instead always trim up towards a set target impedance which is set by the maximum deviation in L and C_p. The LSB capacitance size of the CDAC is set by the accuracy in the pulse width that the pulser requires. This has a strict requirement that has to do with a reliability concern since the high-side HV NMOS (M_4) body diode can get forward biased. In case the pulse width is too short, the synchronous operation of the resonant pulser will lead to a situation where the output node V_{TX} drops below the body diode forward voltage V_F. This will lead to a large current flowing into the substrate and potentially causing latch-up in the circuit. Therefore the trim circuit has to be a continuous time (CT) circuit that monitors the transducer voltage and controls the switching logic of the pulser core in order to advance the recycle phase and hence keep $V_{TX} > V_F$.

3.2.2. HV CDAC architecture

First, for the CDAC implementation it is desirable to place the capacitive network such that it can be shared by all transmit channels in order to save a substantial amount of area. Therefore the CDAC is connected to node V_R, which is the right (HV) node of the inductor, instead to the pulse output node V_{TX} where it has the same influence on the transmit pulse. Besides the added capacitance from the HV CDAC there is already a substantial amount of additional parasitic capacitance (C_{par}) present, mostly due to the large junction capacitances of the low side HV transistor (which has guard rings already properly scaled to handle $30V$ that also add to the total parasitics). From simulation, the total output capacitance (excluding the HV CDAC) equals $133.3pF$, consisting of the transducer capacitance of $118.8pF$ and $14.5pF$ of parasitic capacitance. The LSB value of the CDAC is set to $C_{LSB} = 1.1pF$, and the CDAC size is set to 6-bit. This corresponds to a size of the HV CDAC that is able to handle the required trim range and results in achieving sufficiently close trimmed pulse frequency. Due to the HV that is seen across the capacitors, MOM capacitors are used which can sustain very high voltages compared to MOS and MIM capacitors, which are both limited to $5V$. Due to the large size of the CDAC the parasitic top plate capacitance is rather substantial. The HV CDAC can either be implemented using top plate or bottom plate switches (see Figure 3.4).

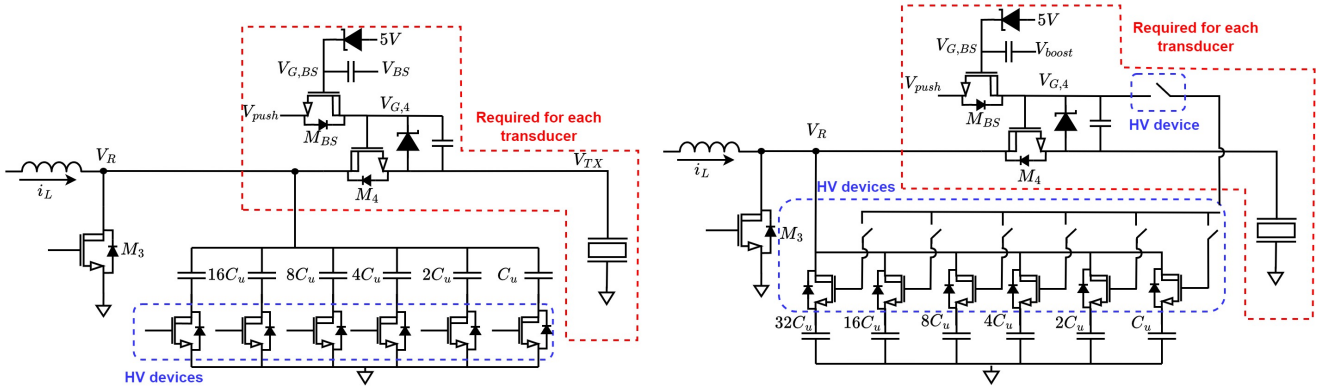

Figure 3.4: Trim circuit 6-bit CDAC implementations, (left) bottom plate HV switches, (right) top plate HV switches and bootstrap connection.

In case one would implement the bottom plate switched architecture the implementation of the HV switches is very simple since the source connection is to ground. This however leads to all the top plate parasitics of the CDAC always being connected in parallel to the transducer, leading to a larger output capacitance and thus larger inductor charging current, ultimately lowering the efficiency further. Luckily the reactive energy on the capacitors is also recycled, reducing the expected additional losses.

The CDAC implementation using switches on the top plate of the MOM capacitors prevents the additional loading of the transducer. However, a more complicated switching strategy is required for it to function. Similar to the high-side HV switch, a $5V$ overdrive is required across the CDAC switch in order to properly turn on the switch and avoid exceeding the $5V$ oxide breakdown voltage of the HV device. For this the HV bootstrap circuit that is already in place for each channel can be used. This does require a larger bootstrap capacitor $C_{BS,1}$ or a smaller high-side HV NMOS in order to obtain and sustain an overdrive close to $5V$. It will also require additional HV switches to select the correct activated bootstrap voltage, resulting in more HV devices.

The impact of the additional parasitic capacitance in regard to the energy efficiency will likely not be very large (since the reactive energy on the capacitors gets recycled) compared to the area trade-off, therefore the bottom plate switches are implemented. The width of the HV switches are binary scaled together with the MOM capacitors in order to obtain a fixed time constant τ which is much larger than the transducer resonance frequency in order to avoid loading the transducer, $\frac{1}{\tau} >> f_s$. With the HV switch that is connected to the LSB capacitor having the device minimum width of $20\mu m$.

3.2.3. Zero-crossing detection

The second part of the trim circuit consists of the CT zero voltage detection circuit. This part of the circuit is responsible for detecting when the HV output node V_{TX} drops below $0V$ in case the pulse

width is shorter than $200ns$. In case the pulse width is shorter during the trim operation a set of OR and XOR gates are used that are able to advance the energy recycling phase by means of using the latched output generated by the CT zero voltage detection circuit together with the synchronously generated pulser control signals. Figure 3.5 shows the circuit diagram of the CT circuit.

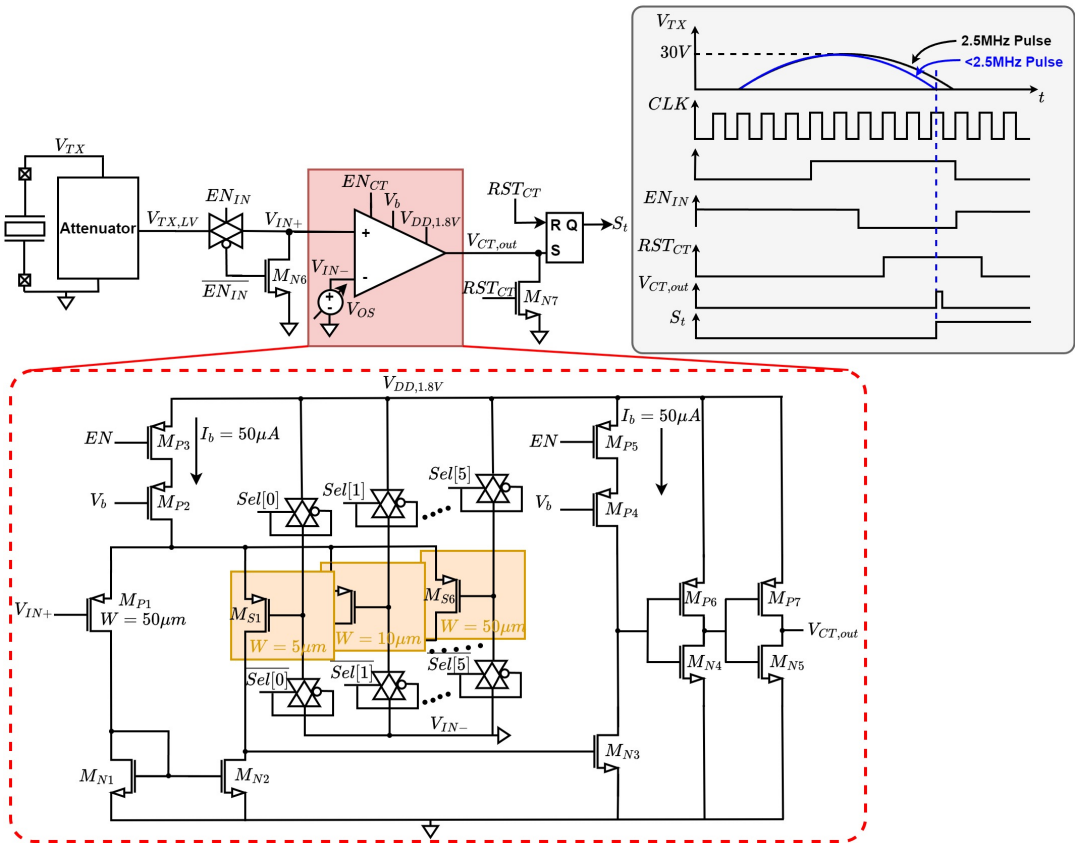

Figure 3.5: Circuit schematic of the CT zero voltage detection circuit used during the transducer trim operation.

For now an ideal attenuator is assumed with a 20x attenuation ratio. A transmission gate (TG) and 2 NMOS transistors are used in order to pass the attenuated input signal to an open loop amplifier and in order to properly pull its output and input to ground in case the amplifier is not used. An SR latch is used as a memory element in order to control the resonant pulser's core main switches until the synchronous part of the recycling phase starts.

The open loop amplifier acts as a static comparator, an adjustable offset voltage at the negative input is used in order to compensate for the finite propagation delay of the comparator, gate driver and level shifter delay. By adjusting the delay properly the circuit is able to perform the trim operation while keeping the HV output a safe distance away from V_F. Choosing an offset that is too large on the other hand will result in too much capacitance being trimmed, leading to a non-ideal half sine wave pulse and in turn lower efficiency.

The comparator is implemented as a 2-stage amplifier, a 5 transistor PMOS-input OTA and a second CS stage. Two inverters are used at the output in order to produce a faster rising edge. The adjustable offset voltage is implemented by skewing the current through the input branches of the input pair, by means of adjusting the width of the input transistor connected to the negative input terminal V_{IN-}. This terminal is connected to ground and provides input widths between $5\mu m - 50\mu m$. The comparator consumes around $100\mu A$ static current and can be turned off when the trim operation has been completed. The other control signals are timed such that the comparator only detects the correct falling edge zero crossing and has a short period available for the comparator to correctly settle after it has been turned on. Figure 3.5 also shows the timing diagram used during the operation of the trim circuit.

3.2.4. Transducer trim simulation performance

An important detail for the operation of this circuit is the pulse amplitude that is used during the trim operation. One could make the argument that using a low voltage pulse ($5 - 10V$) would make the design easier since the lower slope through $0V$ would relax the timing requirements. However, due to the large junction capacitance (the capacitance of which is a function of its bias voltage) added by the HV transistors, a higher transmit pulse will lead to a slightly higher frequency pulse. This means that during the trim operation, a $30V$ pulse needs to be generated in order to perform the trim operation correctly. In that case, it will guarantee if a lower pulse amplitude is selected the resulting pulse avoids forward biasing the body diode if the circuit operates synchronous on a clock. Figure 3.6 shows the simulated DAC transfer and DNL obtained from using unit $1.1pF$ MOM capacitors.

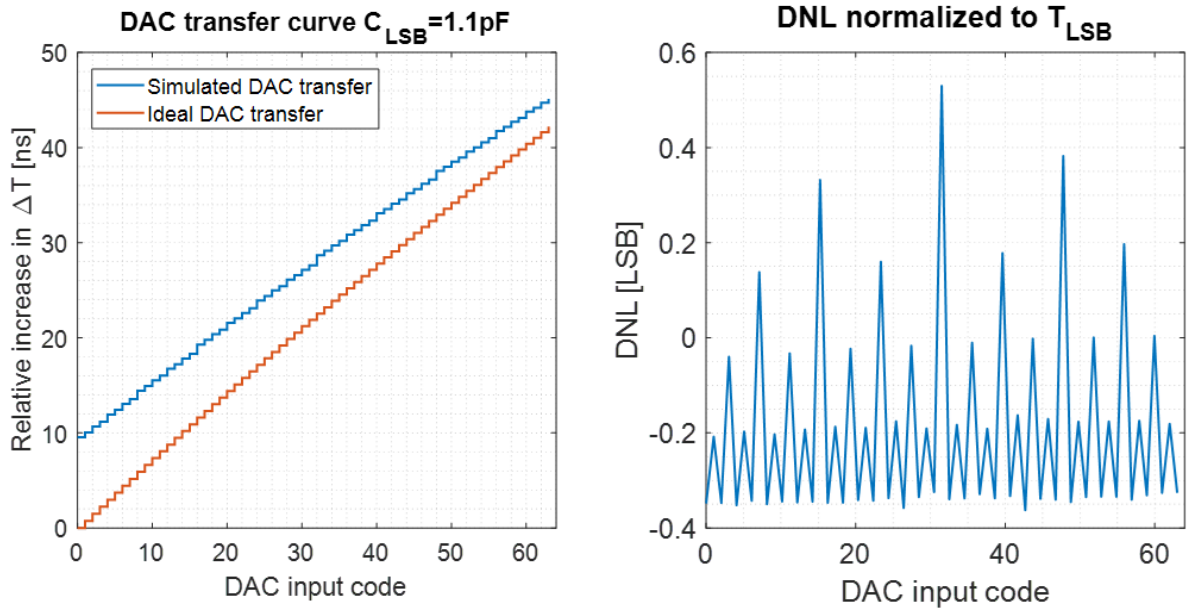

Figure 3.6: Simulation results of the HV CDAC linearity in the resonant pulser ASIC: DAC transfer curve (left) and DNL (right).

The DAC output is defined as the relative increase in pulse width ΔT. The ideal DAC transfer assumes the $133.3pF$ output capacitance (without the CDAC connected) and ideal $1.1pF$ capacitors. The simulated results show an initial jump at code DAC[0], this is due to the aforementioned top plate parasitics adding to the $133.3pF$ output capacitance. For the HV CDAC it is only important that the DAC shows no non-monotonicity in order to properly perform the binary search process. The accuracy needs to be accurate within 1 LSB in order to achieve a proper timed half sine wave. The differential non-linearity (DNL) is given by:

$$DNL(n) = \frac{S_{out}(n+1) - S_{out}(n)}{\text{ideal LSB step width}} - 1 \tag{3.2}$$

Where $S_{out}(n)$ is the output quantity of the DAC corresponding to a DAC input code n. Since the DAC is used to adjust the pulse width (T_{pulse}) the DNL can be written as:

$$DNL(n) = \frac{T_{pulse}(n+1) - T_{pulse}(1)}{\pi\sqrt{C_p \cdot (1.1 \cdot (n+1)) \cdot L} - \pi\sqrt{C_p \cdot (1.1 \cdot n) \cdot L}} - 1 \tag{3.3}$$

The resulting DNL expression has an LSB step width that is a function of n. The peak DNL is reached at 0.53 for code DAC[31] as expected. Also, a mismatch analysis was run for the DAC code that reached the highest and lowest DNL (these being DAC[31] and DAC[9] respectively). The resulting 3σ deviation in terms of resulting ΔT was determined to be $3\sigma_{DAC[31]} = 9.25ps$ and $3\sigma_{DAC[9]} = 17.8ps$. This shows that the influence of mismatch has negligible influence on the resulting accuracy of the trim operation. The total timing range reached by the HV CDAC has been designed and validated to be sufficient across the aforementioned system variation range (assuming $L = 30\mu H$).

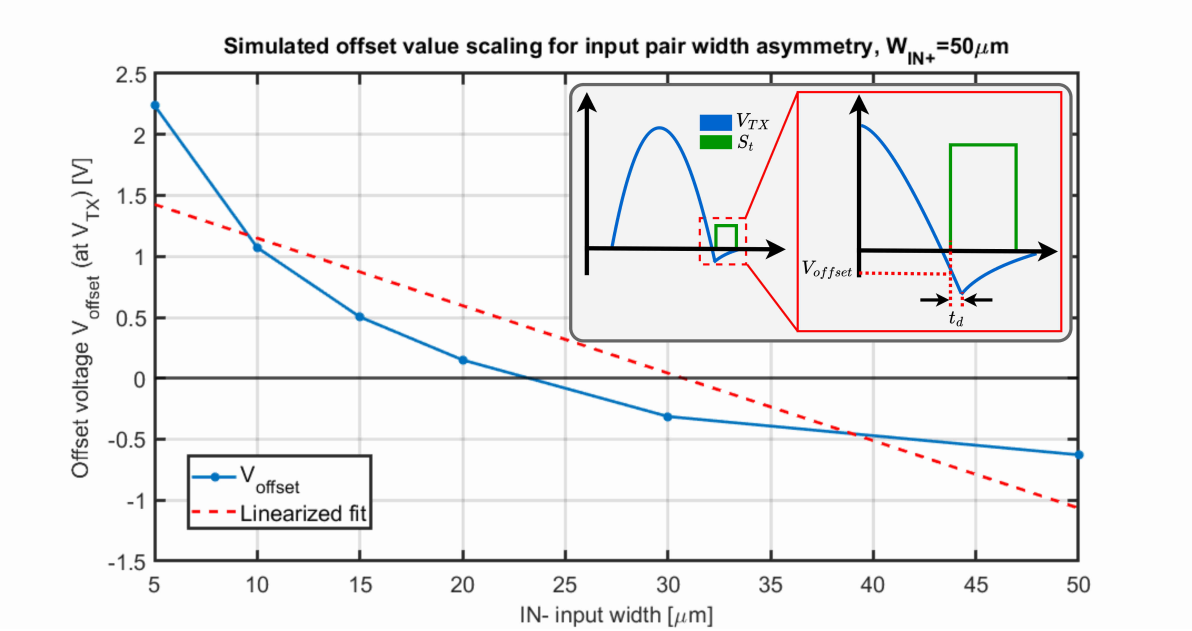

Figure 3.7: Simulated offset generated by input pair asymmetry for the CT trim circuit, assuming a $30V$ pulse and ideal attenuator.

Figure 3.7 shows the simulated offset voltage for varying input pair asymmetry fot the zero-crossing detector. The offset is measured by means of determining the output voltage V_{TX} at the point the output of the latch is triggered by the CT trim circuit (signal S_t). This means that the propagation delay of the comparator is now also included. This however is not the minimum reached output voltage of the HV output since the delay of the level shifters and gate drivers also needs to be taken into account. For the design of the gate drivers the driver driving the low-side HV NMOS is optimized for speed since it determines how fast the HV output node can be pulled back to ground. It also is the largest transistor in the system which causes this HV transistor to dominate in the gate drive losses in the circuit.

Figure 3.8 shows the simulated performance of the entire trim circuit. The figure shows the minimum reached voltage on the HV node during the trim operation. In 6 trim cycles (annotated as Trim[0]-Trim[5]) the transducer is trimmed and after that a synchronous pulse is sent using the obtained trim setting (annotated as Sync Pulse). The results show that for an offset corresponding with a transistor width smaller or equal to $15\mu m$, the trim operation is always able to keep the body diode from conducting. In case $W = 5\mu m$ however, the pulse is trimmed too much resulting in a non-ideal half sine wave pulse. Across temperature variation between $0°$ and $40°C$ the worst case $V_{TX,min}$ is reached at $-102mV$ and across corners at $-467.5mV$ at a width of $15\mu m$.

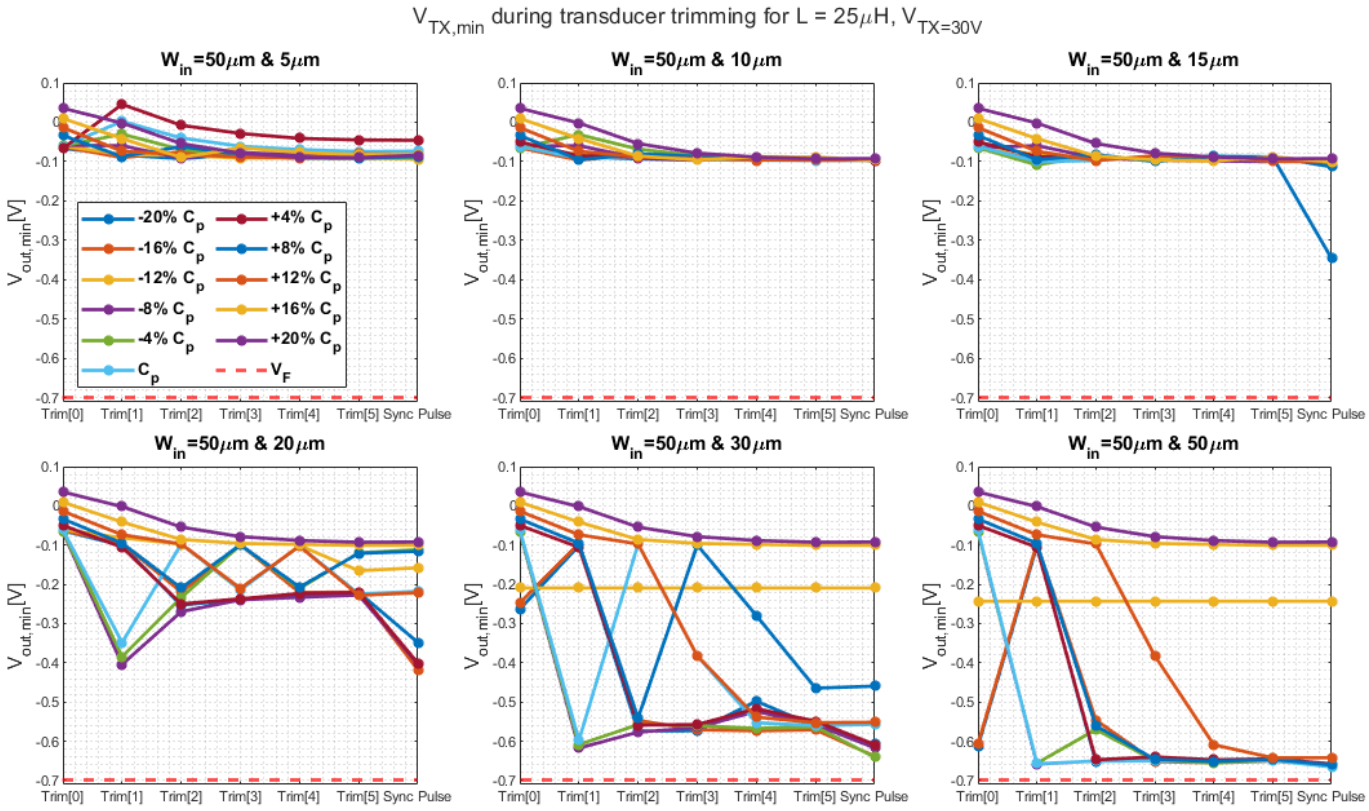

Figure 3.8: Simulation results of the CT trim operation performance across varying offset values and transducer capacitance values.

3.3. Amplitude calibration

3.3.1. Amplitude calibration operation principle

The transmit pulse amplitude for the resonant pulser can simply be altered by adjusting the charging time of the inductor. Due to the many parameter variations present in the circuit, the amplitude of the pulse needs to be calibrated. Using a binary search process, the timing of the charging phase is adjusted in a few cycles. For this the 50MHz clock is used as the timing reference. However, depending on the delay resolution of the circuit, i.e. the time required to obtain a $1V$ difference in output amplitude, an on-chip fine delay block could be required to obtain the $\pm 300mV$ pulse accuracy.

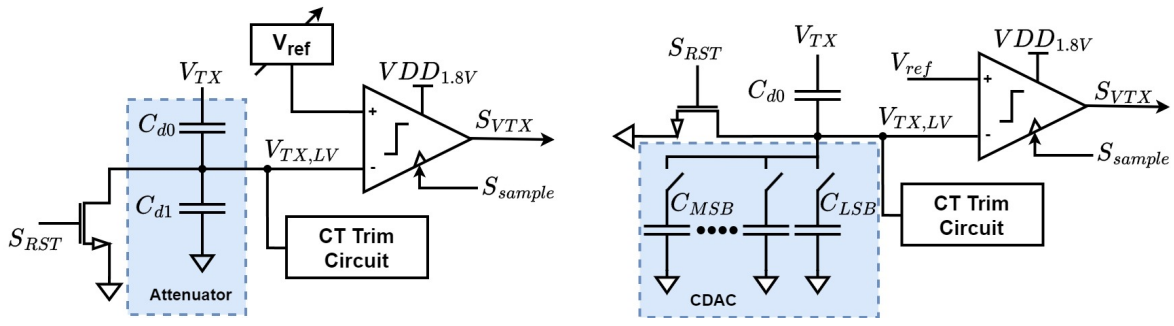

Figure 3.9: Different implementations of the amplitude calibration circuit, using an adjustable voltage reference (left) or adjustable attenuation factor(right).

Figure 3.9 shows two methods to implement the amplitude calibration circuit. The first uses an adjustable voltage reference that is used by a dynamic comparator that senses the attenuated transmit pulse at a sample moment halfway during through the pulse width. The attenuator is implemented

using two capacitors C_{d0} and C_{d1}. The other uses a fixed reference voltage, i.e. the $1.2V$ reference generated by the band gap reference, and a CDAC to create an adjustable attenuation ratio. The capacitor C_{d0} needs to be a MOM capacitor since it's exposed to the HV pulse. In order to achieve a well-defined attenuation C_{d1} and the CDAC capacitors are also implemented as MOM capacitors. Simulation results led to the conclusion that achieving an accurate and small implementation of the calibration circuit using the second method is difficult to realize. The maximum allowable error voltage for the amplitude calibration equals $\frac{0.3V \cdot 1.2V}{30V} = 12mV$, i.e. a reference of $1.2V$ yields a maximum attenuation factor of 25. In order to achieve the highest linearity, top plate switches are used which can be implemented using low voltage transistors. By carefully tuning the unit capacitance still a static error of approximately $15mV$ was reached. After layout it would be very difficult to obtain the required accuracy. Furthermore, additional sources of error are also introduced which need to be accounted for in the amplitude calibration circuit. The attenuator non-linearity, comparator offset and noise and finite accuracy of the voltage reference all add an error source which has to be within the error voltage budget.

3.3.2. Adjustable voltage reference based amplitude calibration

The method employing an adjustable voltage reference presents a more accurate and simpler solution to achieve the desired pulse amplitude control. The different voltage levels can simply be generated using a resistive-based voltage reference. This does on the other hand mean that the comparator threshold is changed across a large range, requiring the comparator to have a very wide input common-mode (CM) range. To generate the reference voltages either the $1.2V$ BGR voltage could be used or the $1.8V$ generated by the internal linear regulator. The BGR does require an additional buffer in order to supply the required current. It is however more accurate than the $1.8V$ regulator. Assuming the comparator employs an NMOS input pair, the lowest allowable threshold is set at $500mV$, in order to avoid driving the input pair to cut-off (also considering PVT variation). Using the $1.8V$ results in a larger range of programmable transmit amplitudes compared to using the BGR voltage. In order to allow for some headroom the reference voltage range is taken between $500mV$ and $1.5V$, which leads to an attenuation factor of $30V/1.5 = 20$ (compared to a factor of 25 in case of the BGR voltage). The linear regulator does have some ripple and a static error in the produced output voltage.

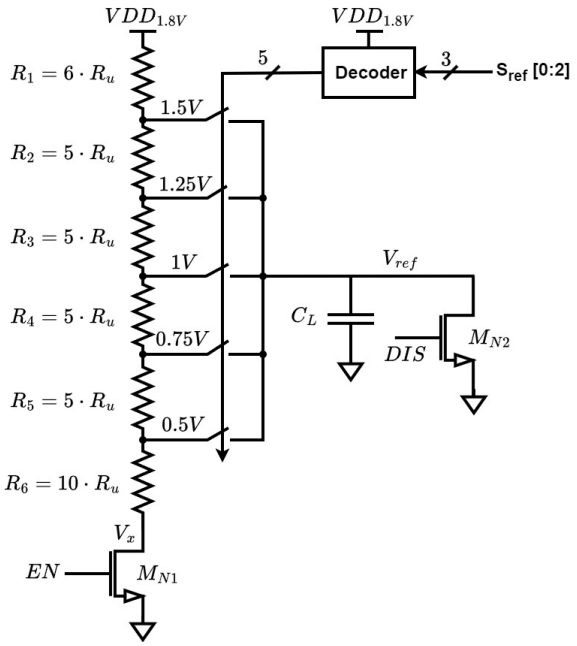

Figure 3.10: Schematic of the adjustable resisitive voltage reference.

Figure 3.10 shows the circuit implementation of the resistive voltage reference. The circuit implements a resistive ladder to generate 5 different voltage levels corresponding to transmit amplitudes of $30, 25, 20, 15$ and $10V$. In order to improve matching, unit resistors are implemented of $R_u = 1.5k\Omega$,

giving a total resistance of $R_{tot} = 54k\Omega$. The resistors are p+ poly resistors due to their high density. By means of a control signal provided by the digital controller, one of the 5 voltage levels is used to charge a small 1pF MIM capacitor C_L, creating a simple sample and hold circuit (S/H). The size of the capacitor is chosen in order to be around the same order of magnitude as the capacitance seen at the other terminal of the comparator (which is dominated by the capacitive attenuator). This is done in order to reduce the asymmetric voltage difference that occurs due to the charge kickback from the comparator during comparison. In case the comparator input overdrive becomes very small a false comparison could occur leading to an error in the final calibration cycle. Transistor M_{N1} is sized to be $100\mu m$ wide in order to obtain approximately $100\mu V$ at node V_x. From the resulting charging current and bandwidth limitations of the linear regulator the required charge time for the reference voltage becomes $3T_{CLK}$, and the charging of reference voltage during the amplitude calibration cycles is run at the beginning of the inductor charging phase.

Table 3.2: Simulation results of the resistive voltage reference

V_{ref}	**Deviation [mV]**
1.5024	2.42
1.2456V	4.40
999.60mV	0.40
751.10mV	1.10
503.38mV	3.38

Table 3.2 shows the simulated accuracy of the different voltage levels. By means of a mismatch simulation the maximum deviation was found to be $3\sigma(\Delta V_{ref}) = 6.3mV$. The resistive reference also adds thermal noise; this however is negligible, assuming the load capacitor introduces the dominant pole for the bandwidth as $\frac{1}{2\pi R_{tot} C_L} = 3.8MHz$, $v_{rms} = \sqrt{4kTR_{tot}B} = 60\mu V$.

3.3.3. Capacitive attenuator

The capacitive attenuator makes it possible for the HV pulse to interface with the low voltage electronics. The accuracy and linearity of the attenuator play an important role in the total accuracy of the amplitude calibration process. The attenuation factor$\beta = \frac{C_{d0}}{C_{d0}+C_{d1}} = \frac{V_{TX,LV}\,(\text{peak})}{V_{TX}\,(\text{peak})}$ should be designed such that the targeted $30 - 10V$ pulse amplitude range falls within the comparator supply voltage of $1.8V$. The top MOM capacitor C_{d0} should be designed much smaller than the transducer's C_p in order to avoid significant loading. Capacitor C_{d1} should be big compared to the input capacitance C_{in} of the dynamic comparator in order to maintain an accurate attenuation ratio. Mismatch in the attenuation factorwill lead to a gain error G_ϵ besides the static error introduced by the attenuator non-linearity. In order to obtain the required accuracy the capacitors are made from identical unit MOM capacitors C_u. The attenuator shares its bottom capacitor C_{d1} across channels. During transmit on one of the channels the top capacitor $C_{d0,N}$ of the other channels is connected to ground. This leads to a smaller attenuator but does lead to increased cross-talk between the different transmit channels. From simulation the unit capacitance is taken as $C_u = 176fF$ with $C_{d01} = C_{d02} = 2C_u$ and $C_{d1} = 32C_u$.

Figure 3.11 shows the simulated attenuation factor as a function of the transmit amplitude. A clear non-linearity is visible which can be explained by investigating the different devices connected to the attenuator. The HV NMOS and the LV NMOS discharge transistor each add a bias-voltage dependent (drain-to-bulk) junction capacitance $C_{j,DB}$ which can be described as:

$$C_{j,DB} = \frac{C_{DB0}}{\sqrt{1 + \frac{V_{DB}}{V0}}} \tag{3.4}$$

From this, one can readily conclude that the higher pulse voltage leads to a slightly lower $C_{j,DB}$ connected in parallel to C_{d1} leading to a slightly higher β. The simulated variation in β already leads to a static error which contributes significantly to the total error budget. Due to the attenuation, the resulting gain error is highest for the highest transmit amplitude. The implemented attenuator therefore has the lowest deviation in attenuation factor for $V_{TX} = 30V$ resulting in the overall best performance.

Besides the static error introduced by the non-linearity, the capacitor mismatch introduces an additional gain error. For a $30V$ and $10V$ pulse a mismatch analysis was performed in order to obtain

the $3\sigma(G_\epsilon)$. This analysis has been performed for both a $30V$ and $10V$ transmit pulse and is shown in Figure 3.12. The total measured gain error present at the input of the comparator due to the attenuator mismatch for the $30V$ pulse is $\pm 3\sigma(G_\epsilon) = 4.12mV$ and for the $10V$ pulse $\pm 3\sigma(G_\epsilon) = 1.42mV$.

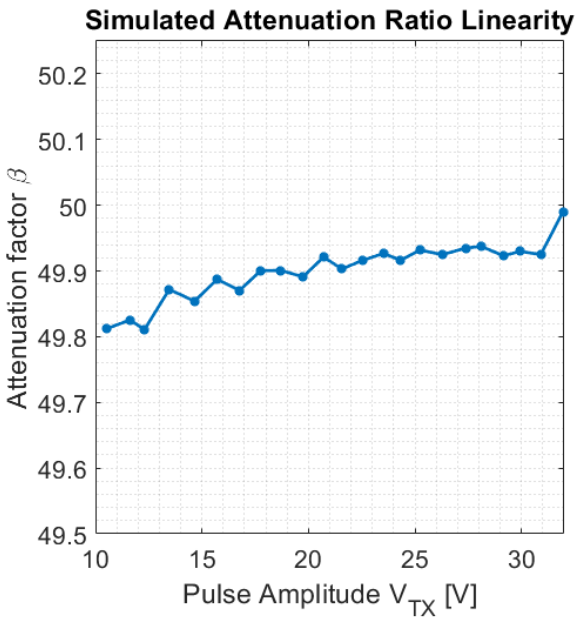

Figure 3.11: Simulated attenuator linearity vs transmit amplitude.

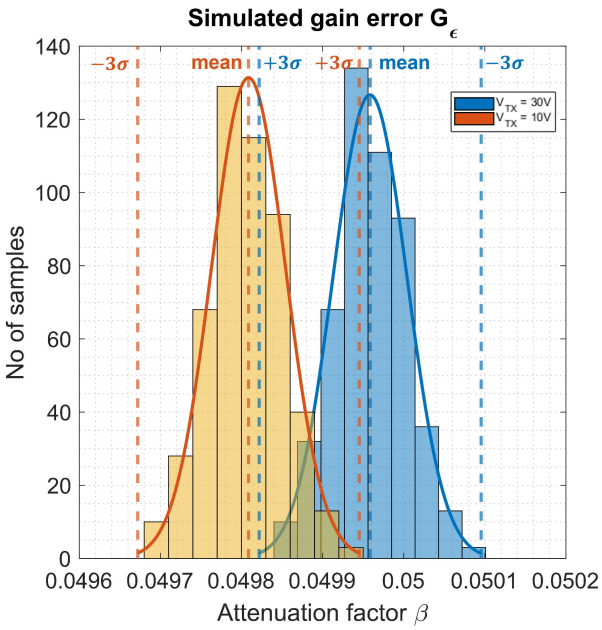

Figure 3.12: Monte-Carlo mismatch simulation showing maximum obtained attenuator gain error G_ϵ.

3.3.4. Dynamic comparator

The final circuit block required for the amplitude calibration circuit is the dynamic comparator. The comparator samples the attenuated HV pulse at exactly the middle of the pulse period ($5T_{CLK}$ from the start of the pulse generation phase). The calibration process involves the entire pulser, i.e. a pulse is sent, a single SAR decision is taken, and after that, a subsequent pulse is sent until the conversion has been completed. By doing this, instead of performing the entire SAR conversion from 1 pulse, the calibration process becomes more robust. This leads to relaxed timing requirements for the comparator. The comparator should furthermore handle a very wide input CM range from $500mV - 1.5V$ across PVT. The comparator also introduces input referred offset, charge-kickback and noise which all add to the total input referred error budget of $15mV$.

This work implements a single clock phase dual tail comparator presented in [36] (see Figure 3.13). The comparator works by means of first pre-charging the parasitic capacitors at the nodes $DI+$ and $DI-$ (C_{DI+} and C_{DI-}) to VDD during the reset phase of the comparator, i.e. $CLK = 0$. After the pre-charging, transistors M_{P4}, M_{P5}, M_{N6} and M_{N7} turn off the latch and M_{N4} and M_{N5} ensure the comparator outputs are at $0V$. The operation of the comparator is based on the discharge process of the DI nodes, which happens at different rates depending on the gate voltage at the input of the comparator. Unlike the standard dual-tail comparator which uses a second clock phase, the latch is triggered automatically if the voltage difference on the DI nodes has become sufficiently large. This process improves the meta-stability of the comparator since the integration time is prolonged in case it is required for a small input overdrive voltage. The current in the pre-amplifier and the latch can be designed separately from each other. On the other hand, the fact that the comparator needs to charge and re-charge the parasitics at the DI nodes does lead to a slower comparator.

In order to obtain a low contribution of the input-referred offset from the comparator, the input pairs are sized relatively large ($20\mu m$), which does result in larger kickback. The sizing of the input pair is based on the maximum amount of kickback that could be handled at the input of the comparator. Due to asymmetry in the total capacitance seen at each of the gates of the input pair, the kickback could result in a false comparison in case the input overdrive between the input transistors becomes very small in the final conversion step.

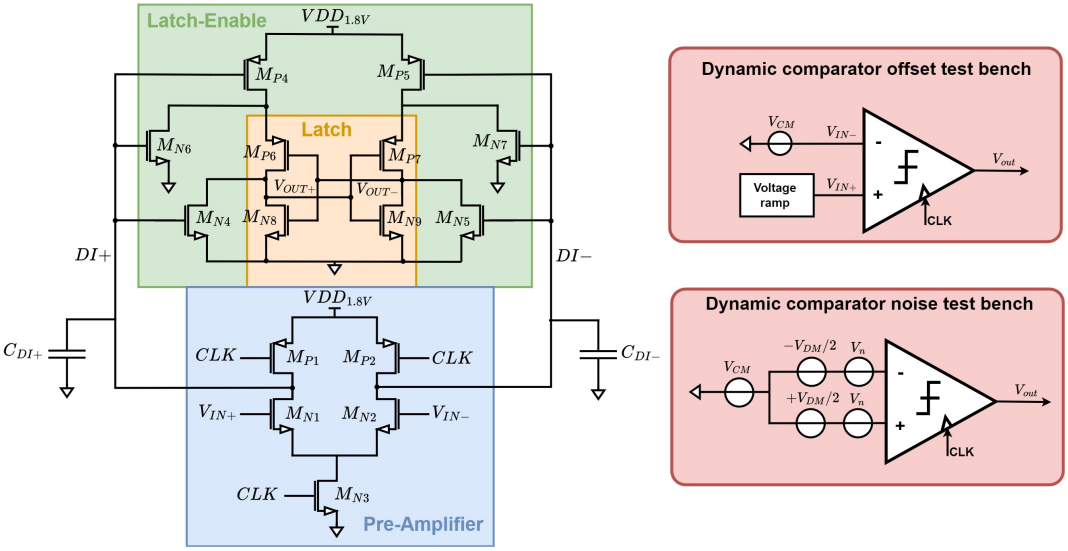

Figure 3.13: Schematic of the single clock phase dual-tail dynamic comparator.

The dynamic comparator also has an input referred noise contribution that needs to be simulated. Since dynamic comparators do not have a steady-state operating point, the noise cannot be determined using standard noise analysis. Instead, a time-domain noise analysis needs to be performed. The work presented in [37] shows a stochastic analysis of dynamic comparator noise and presents a few important methods to reduce the noise, all arising from reducing the overdrive voltage of the input pair. First, the W/L ratio of the input pair should be increased; in this design it is already maximized. Second, the discharge current can be decreased by adjusting the size of the tail current source transistor M_{N3}. This limits the current through the input pair and thus increases the required integration time and effectively reduces the noise from the pre-amplifier. By performing PVT analysis across the V_{CM} range of interest, M_{N3} is sized at its minimum width of $220nm$.

By enabling transient noise in the simulation an input voltage of $V_{CM} = VDD/2$ and a differential mode (V_{DM}) input signal are provided at the input ($V_{CM} + V_{DM}/2$ and $V_{CM} - V_{DM}/2$). By means of taking 500 comparisons and averaging their result for varying $V_{DM} \pm 750\mu V$ an error function is obtained from which the noise has been determined to be $\sigma(V_{n,comp}) = 91.056\mu V$ (see Figure 3.14). Furthermore, the comparators performance has been validated across PVT for varying input V_{CM} in the range of $450mV - 1.55V$.

The input referred offset ($V_{OS,comp}$) of the comparator can be determined by comparing a very slowly varying input ramp signal to $V_{CM} = VDD/2$. By means of a mismatch analysis the offset can be determined by means of calculating the offset voltage at which the comparator triggers. By using a slowly varying input signal (compared to the clock frequency), the accuracy of the offset simulation has been set around $1\mu V$. Figure 3.15 shows the simulated $V_{OS,comp}$ of the comparator from which we obtain $\sigma(V_{OS,comp}) = 2.15mV$.

3.3.5. Amplitude calibration simulation

The final step is to obtain the resonant pulser sensitivity. Based on the $\pm 300mV$ transmit pulse accuracy requirement a suitable finer delay measurement compared to the $50MHz$ clock needs to be implemented. The pulser's sensitivity also determines the number of cycles to perform the amplitude calibration. For an inductor size of $27\mu H$ and a trimmed system, the sensitivity is determined for the worst case situation, i.e. the smallest possible charge time required for a given V_{TX} which is the case for the highest battery voltage ($3.9V$). Figure 3.16 shows the simulated delay resolution of the whole system for varying input battery levels. The worst case result for $V_{bat} = 3.9V$ in the FF process corner, the simulated sensitivity then equals $18.18\frac{ns}{V}$. Given the $300mV$ accuracy requirement on the transmit pulse the required minimum charge time step needs to be at most $5.45ns$.

In order to implement the finer time steps either a circuit providing a higher frequency reference or a delay-based timing reference could be used. In applications where a constant high accuracy high

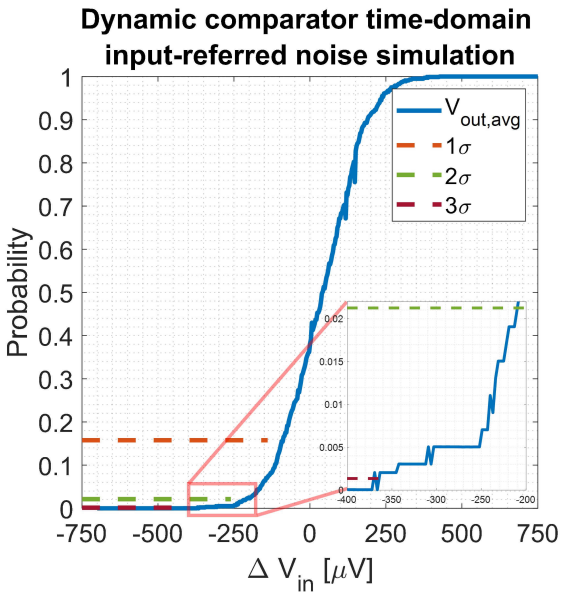

Figure 3.14: Simulation result of the input-referred noise from the single clock phase dual tail comparator, $1\mu V$ ΔV_{in} accuracy averaging 500 samples per ΔV_{in} step.

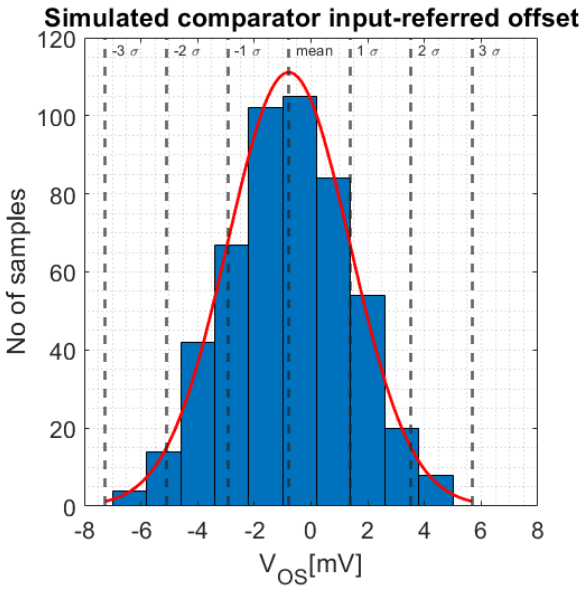

Figure 3.15: Monte-Carlo analysis result for the dynamic comparator input referred offset, $n = 1000$.

frequency reference is required often PLL (phase-locked loop) or a DLL (delay-locket loop) are used [38]. These systems however pose both difficulties in their design and power consumption. Since the required accuracy is quite relaxed for the resonant pulser, a simple tapped delay line is used. A delay line consisting of minimum sized inverters is used to obtain time delays of $5, 10$ and $15ns$. Furthermore, a multiplexer is then controlled in order to switch from the coarse time steps provided by the FPGA to the fine time steps. Figure 3.17 shows the performance of the tapped delay line across PVT, the maximum deviation for the delay stays below the required maximum time step.

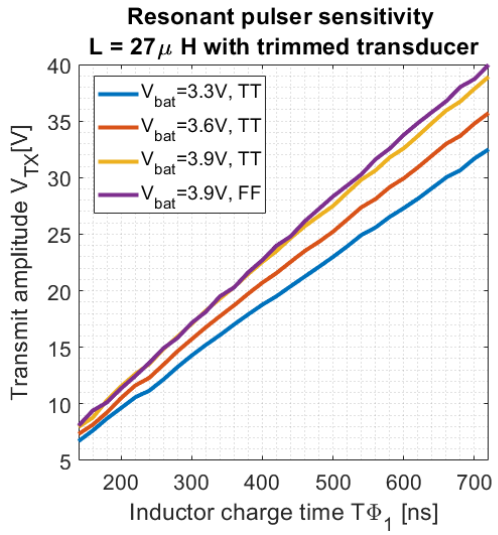

Figure 3.16: Simulated sensitivity of the resonant pulser across varying input battery voltage levels.

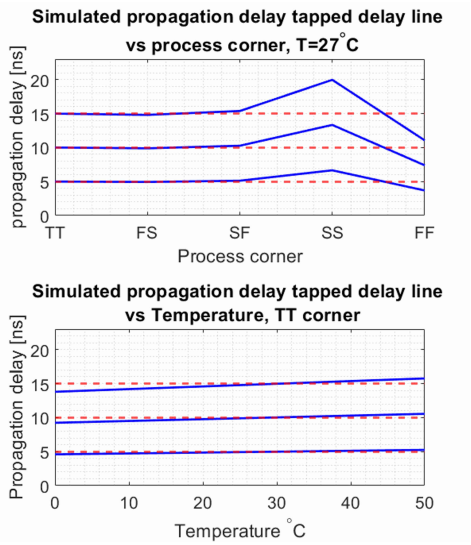

Figure 3.17: Simulated propagation delay of a inverter based tapped delay line across corner and temperature.

From the obtained sensitivity, it follows that in total 8 amplitude calibration cycles are required. These calibration cycles use a binary search in order to obtain the required amplitude accuracy. In the first 6 cycles, the coarse timing from the $50MHz$ clock is used and in the final 2 cycles the fine delay is used. In order to properly evaluate the performance of the amplitude calibration circuit a worst-case

simulation is performed where each of the different error sources (at 3σ) are included in the circuit (see Figure 3.18). By adjusting the timing of the resonant pulser, the accuracy of the pulser is determined for both a $30V$ and $10V$ pulse. The amplitude calibration circuit is able to obtain a pulse accuracy within the requirement.

Finally, a complete simulation is run that shows the resonant pulser achieving the desired transmit amplitudes within 8 calibration cycles. Figure 3.19 shows the simulation results, here the first 6 calibration cycle perform the coarse time conversion and the last 2 cycles perform the fine conversion. The largest deviation in transmit amplitude is $264mV$.

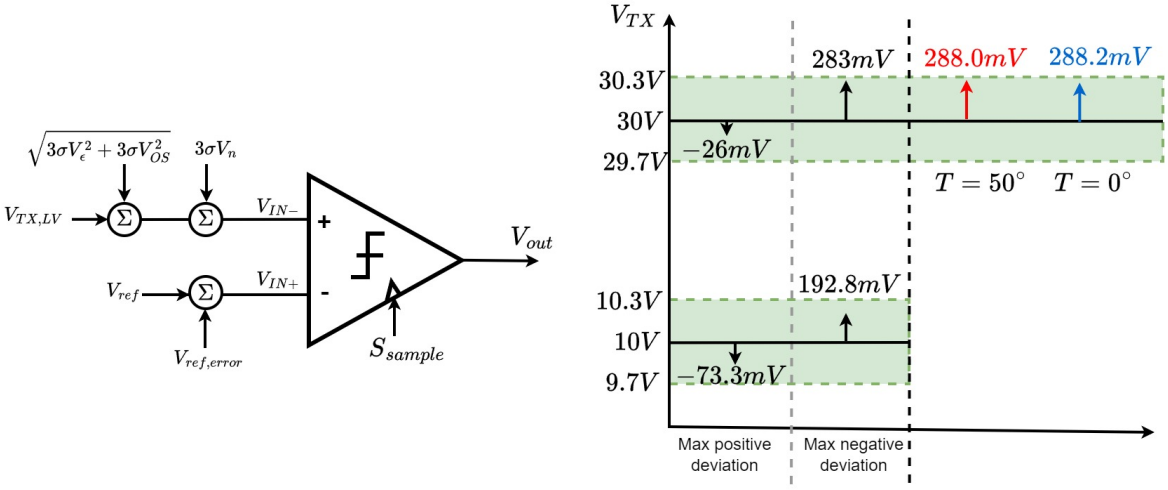

Figure 3.18: Simplified amplitude calibration test bench with the included error sources and accuracy simulation results.

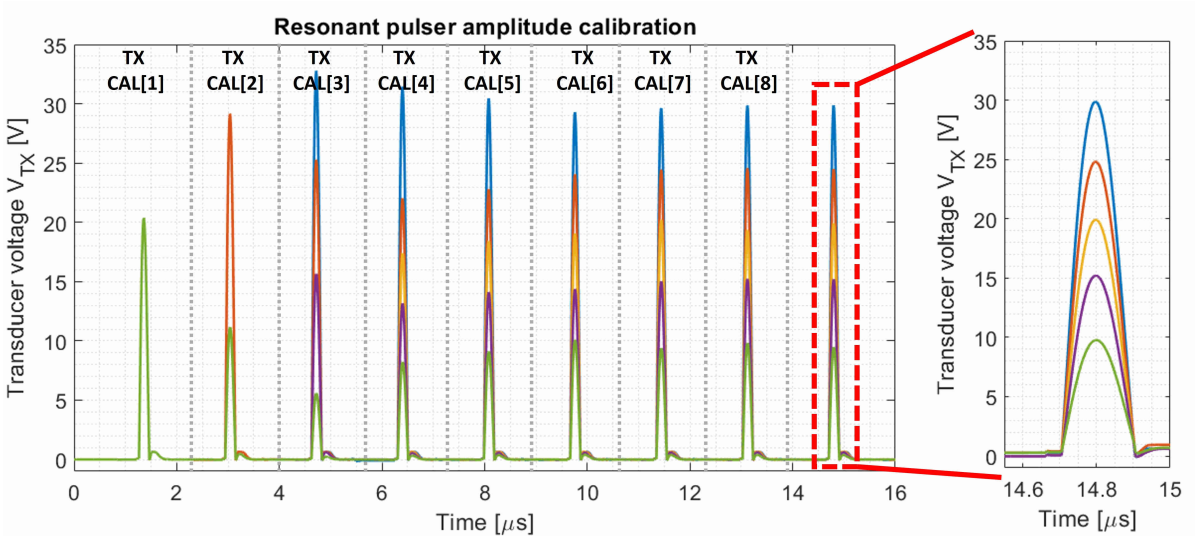

Figure 3.19: Simulation result of the resonant pulser performing the amplitude calibration on the 5 programmable transmit amplitudes, $V_{bat} = 3.6V$, $L = 27\mu H$ with a trimmed transducer.

3.4. Energy recycling calibration

3.4.1. Operation principle & circuit implementation

The third and final calibration loop calibrates the energy recycle timing of the resonant pulser. Residual energy that is left on the inductor after recycling the energy back to the input source generates a voltage spike across the high off-resistance of the $5V$ switches of the pulser. By means of detecting the presence or missing of the voltage spike the timing of the recycle phase is adapted. The work

presented in [39] makes use of this technique in a boost converter design targeting energy harvesting applications. By sampling the resulting voltage spiking due to residual inductor energy the oscillation frequency of the circuit is adapted from a digital counter. Methods like this provide the important benefit that no static power is consumed during calibration.

This technique can be implemented by turning on the LV NMOS transistor one clock cycle after the LV PMOS turns off, so that any residual inductor current can generate the voltage spike required for the calibration to function. After the detection has taken place, the LV NMOS is turned on in order to properly discharge the inductor. Figure 3.20 shows the proposed circuit to perform the energy recycling calibration. A $5V$ dynamic comparator is used to compare the voltage on node V_L and a reference voltage at $V_{DD,5V}/2$. The dynamic $5V$ comparator is the same single clock phase dual tail comparator architecture used in the amplitude calibration circuit, now resized using $5V$ devices. The same design considerations were considered here, trade-offs in charge kickback, offset, noise and speed were made to optimize the design. The reference voltage is generated by means of a simple S/H circuit consisting of a resistive divider, switches and a capacitor C_L. The resistors R consist each of a series connection of 4 unit resistors $R_u = 4k\Omega$, implemented as p+ poly resistors. The capacitor C_L is a $1pF$ MIM capacitor. A level-down shifter is used to converter the $5V$ digital comparator output to a $1.8V$ signal. Furthermore, an inverter-based delay cell is used to generate a delay ΔT_M which is level shifted to $5V$ in order to trigger the comparator.

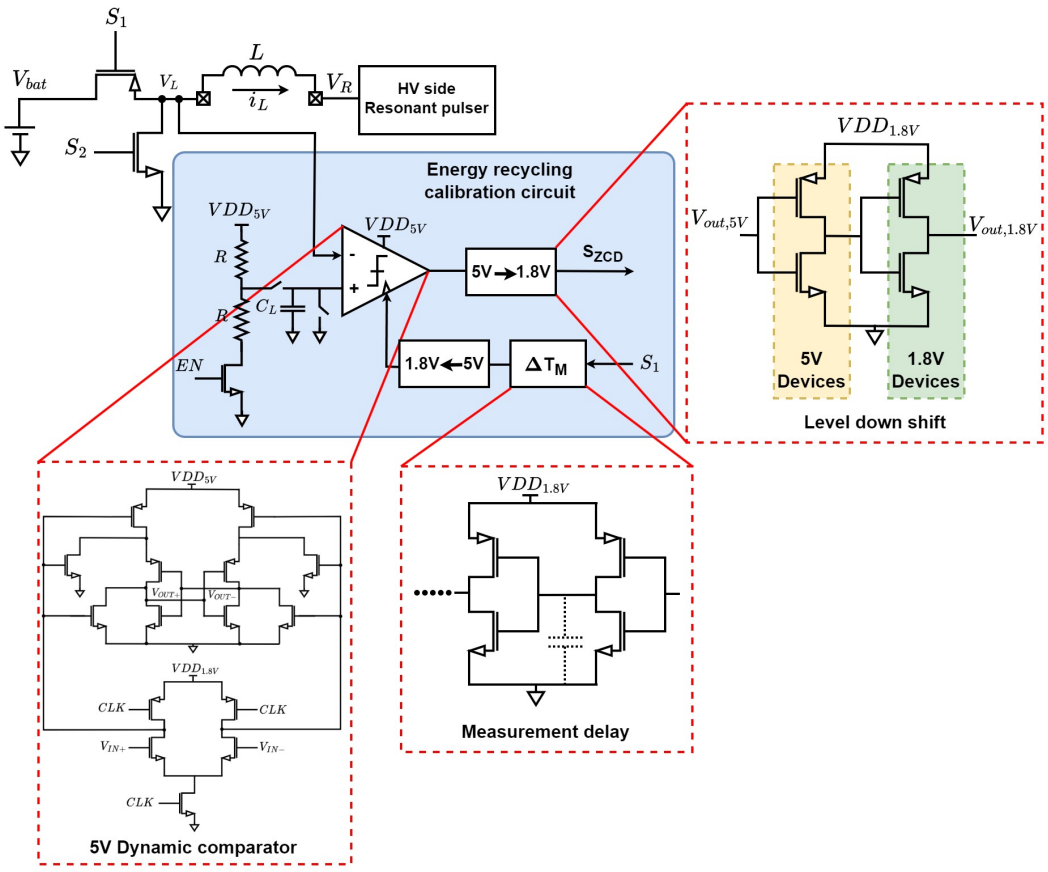

Figure 3.20: Schematic of proposed the energy recycling calibration circuit.

Figure 3.21 shows an example of the resulting voltage and current waveforms of the resulting voltage spiking and inductor current implemented in the resonant pulser. It shows why an additional 'measurement delay' ΔT_M needs to be inserted in order for the circuit to perform correctly. At the time moment the LV PMOS opens either the inductor current is still negative (phase ϕ_3 is too short) or has already crossed $0A$ and the inductor is being charged from the battery again (phase ϕ_3 is too long). In the first case, the node V_L will quickly fall to ground level when the switches close. In the second case the residual positive inductor current will create a voltage spike where the width of the resulting voltage

spike is proportional to the amount of residual inductor energy. Now ΔT_M needs to be chosen such that the circuit can correctly discriminate between early and late openings of the switch. In case ΔT_M is chosen too short the situation could arise where a false positive output is detected in case Φ_3 is too short, and vice versa in case ΔT_M is chosen too long a false negative output is detected in case Φ_3 is too long.

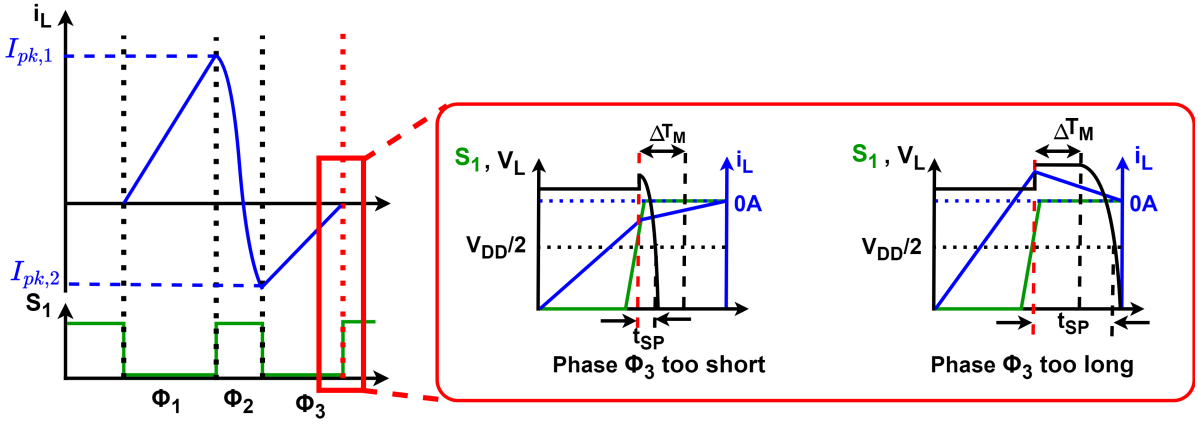

Figure 3.21: Example of voltage spiking due to residual inductor energy at the end of the recycling phase implemented with the resonant pulser.

The work presented in [40] investigates the relation of the measurement delay in regards to the propagation delay t_{SP}. In order to minimize the errors, ΔT_M should equal the propagation delay t_{SP0} obtained in the optimal case that the inductor current i_L reaches zero at the end of phase ϕ_3. By means of simulation, the timing of the pulser is accurately adjusted to obtain $t_{SP0} = 5.9ns$. This already includes the delay from the level shifter and gate driver of the LV PMOS and the level shifter delay connected to the ΔT_M delay cell. Similar to the analysis of the amplitude calibration circuit, the total accuracy of the energy recycling calibration can be determined. The accuracy of the energy recycling calibration is limited by the smallest time step available. Here, the fine delay cell from the amplitude calibration circuit is adopted in order to obtain $5ns$ fine timing steps.

The number of required calibration cycles is determined by finding the maximum deviation a given recycle period ϕ_3 can have for a given inductor charge time ϕ_1 that has been found from simulation under nominal conditions. The resonant pulser yields the largest deviations between the charge and recycle phases for operating at the lowest battery voltage, largest inductor value under the SS process corner (which yields the longest required recycle time for a given inductor charge time). And the other way around, for the highest battery voltage, the smallest inductor value under the FF process corner (which yields the shortest required recycle time for a given inductor charge time). Under these conditions, the largest measured deviation in residual inductor current is found to be $10.04mA$ which is 16.7% of the initial inductor current at the start of the recycle phase. From the resulting energy recycle period it was found that a total of 4 binary calibration cycles (2 coarse binary steps and 2 fine binary steps) give a sufficient range to guarantee the proper operation of the circuit.

3.4.2. Energy recycling calibration simulation performance

In order to evaluate the accuracy of the calibration circuit a worst case analysis is performed similar to that in Section 3.3.5. By identifying all error sources and creating a simulation test bench in which these errors are all included, the performance of the calibration circuit can be verified. The input pair of the comparator is sized to $15\mu m$ wide resulting in an input-referred offset of $\pm 3\sigma(V_{OS}) = 18.22mV$. The input-referred noise has been determined to be $\pm 3\sigma(V_n) = 1.119mV$. The higher noise compared to the $1.8V$ dynamic comparator is mainly due to the much longer minimum transistor length of $500nm$ for $5V$ NMOS transistors. Furthermore, an error is introduced to the reference voltage to account for the inaccuracy of the charge pump and a timing skew is injected for the sampling signal δt. The skew varies between the longest and shortest difference in the delay from the input signal to the comparator clock input. From PVT simulation this is determined to be $+\delta t = 0.267ns$ and $-\delta t = -0.282ns$. Figure 3.22 shows a simplified diagram of the test bench used in order to evaluate the performance of the

energy recycling calibration circuit.

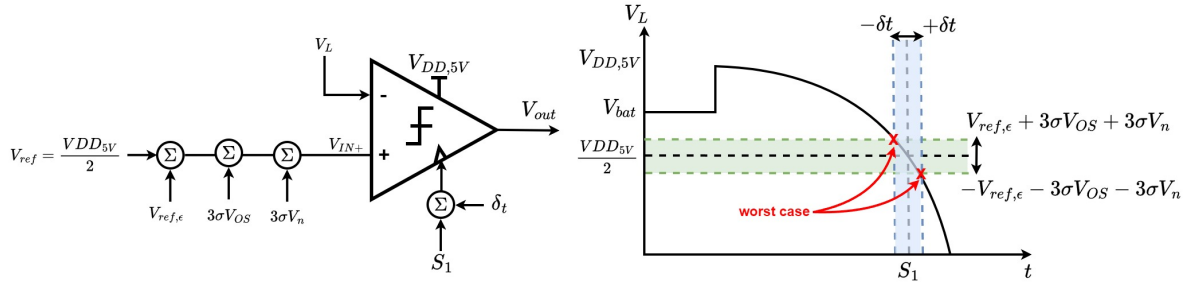

Figure 3.22: Simplified energy calibration test-bench including the different error sources and where the worst case condition lie.

By performing this worst case simulation the performance of the calibration circuit was checked across PVT. Under all circumstances, the circuit was able to correctly calibrate the energy recycling phase to an timing accuracy of $5ns$. Figure 3.23 shows the simulation results of the energy recycling calibration during the operation of the entire system.

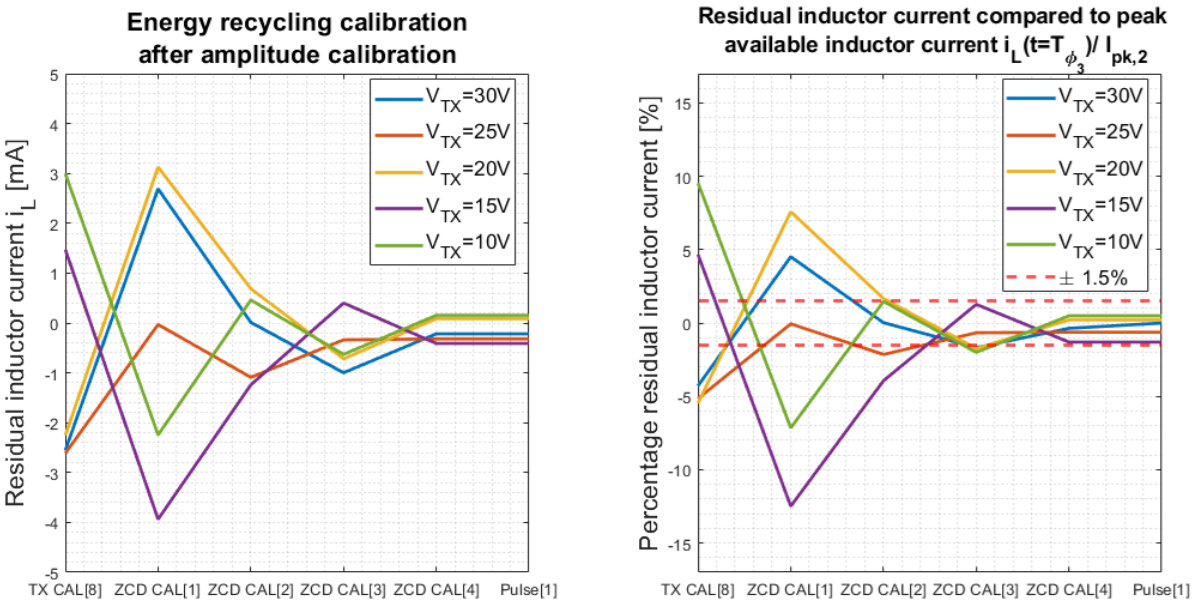

Figure 3.23: Simulation results of the energy recycling calibration for varying calibrated transmit amplitudes.

After amplitude calibration (cycles ”TX CAL [1-8]”) the energy recycling phase is calibrated in 4 cycles ”ZCD CAL[1-4]” whereafter the synchronous pulsing can start (where the first pulse is indicated as ”Pulse[1]” in Figure 3.23). This has been simulated for the 5 different transmit amplitude levels and it shows that the circuit is able to reduce the residual current in the inductor to below $\pm 1.5\%$ of its initial value. Further reduction of the residual inductor current is possible in case an even finer time base is available, However, inaccuracies in the $5V$ supply due to ripple and systems variations (e.g. varying battery voltage, L and C_p) over time make it not worthwhile to reduce the residual inductor energy much further.

3.5. Regulated $5V$ charge pump

3.5.1. Operation principle

The resonant pulser derives an internal $5V$ voltage supply from the input battery supply in order to drive the $5V$ transistors used in the pulser. Since the target output voltage is only $\approx 40\%$ higher than the input supply a single-stage charge pump is proposed in order to obtain a simple and efficient solution [41], [42]. Figure 3.24 shows a simple example of the operation of a single-stage charge pump.

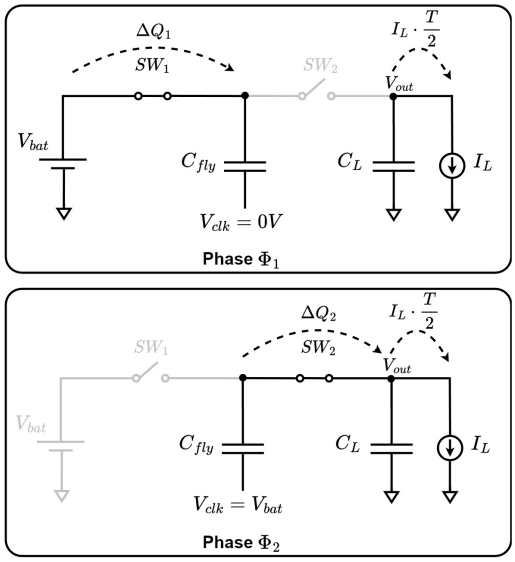

Figure 3.24: Simplified circuit diagram of a single stage charge pump [41].

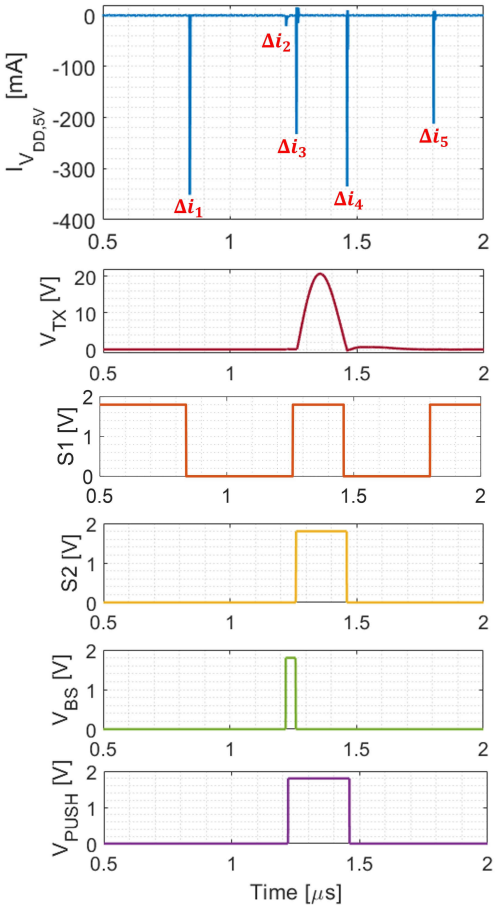

Figure 3.25: Transient simulation of the current drawn from the $5V$ supply together with the transmit output and pulser core control signals.

By charging a 'flying capacitor' C_{fly} to the input voltage a charge transfer ΔQ_1 takes place. The charge pump switches the top plate connection of C_{fly} from the input source to a larger load capacitor C_L and pushes the bottom plate of the flying capacitor to the level of the input supply, leading to a second charge transfer ΔQ_2. The large load capacitor is then able to supply the instantaneous load currents required by the system. By inspecting this simple example the maximum steady state output voltage that can be reached equals:

$$V_{out|steady-state} = 2V_{bat} - \frac{I_L \cdot T}{C_{fly}} \tag{3.5}$$

The ripple on the charge pump output $\Delta V_{DD,5V}$ can be reduced simply by choosing a larger C_L. In the design of this system, only on-chip capacitors are considered limiting the maximum size for C_L. The sizing of both C_L and C_{fly} are based on the total current drawn by the system from the $5V$ supply and the time intervals in between large current transients. The resonant pulser system is designed such that only dynamic current is drawn from the $5V$ supply. The power dissipated during the switching moments of the resonant pulser core dominates the power dissipation on the $5V$ supply. Figure 3.25 shows the current drawn from the $5V$ supply in a single pulse cycle. Five distinct transients Δi_{1-5}

are indicated which coincide with the different major switching moments of the resonant pulser core's switches. Since these timing moments are known to the system beforehand, the charge pump can be controlled by the digital controller in a feed-forward manner in order to enable the charge pump properly right before these switching events. Table 3.3 presents the simulated charge drawn from the $5V$ supplies during these switching moments.

Table 3.3: Simulated charge consumed by the resonant pulser during the 5 major switching events

Current transient	Total charge [pC]
Δi_1	72.15
Δi_2	66.64
Δi_3	65.16
Δi_4	81.05
Δi_5	60.57

The size of C_L is set to $200pF$ in order not to occupy too much area. C_L is implemented with $5V$ MOS capacitors and C_{fly} is implemented as a $10pF$ MIM capacitor which is placed on top of the charge pump circuit in order to optimize for the area. The size of C_L limits the output ripple to at most $201mV$. The size of C_{fly} is chosen in order to achieve fast enough pumping in between the large current transients in order to achieve the desired $5V$ output voltage during the large switching events. From figure 3.25 it becomes clear that the timing between moments Δi_2 and Δi_3 is the most problematic due to the short time span in between the two switching moments, this being the time required for the bootstrap voltage to settle which equals $2T_{CLK}$. By choosing $C_{fly} = 10pF$, the resulting voltage drop before switching moment Δi_3 is minimized while obtaining sufficient accuracy by the charge pump.

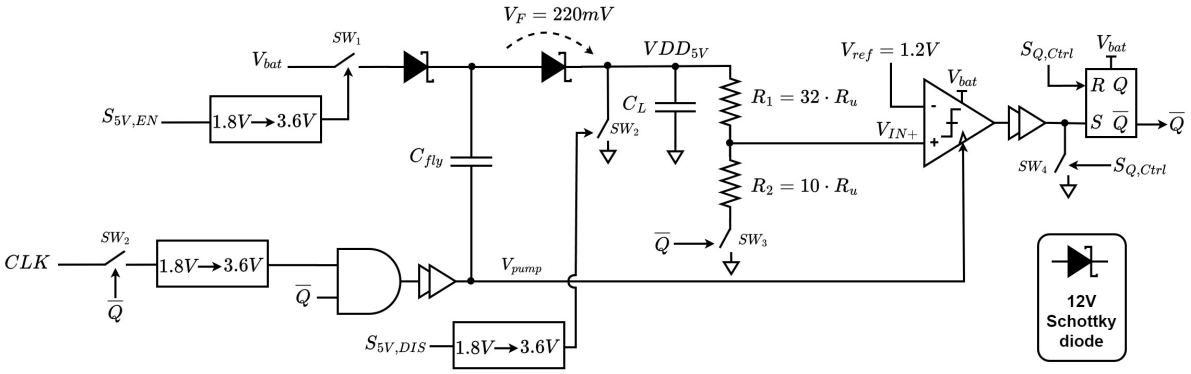

Figure 3.26: Circuit schematic of the implemented regulated $5V$ charge pump.

3.5.2. Circuit implementation

Figure 3.26 shows the circuit schematic of the implemented regulated $5V$ charge pump circuit. The charge pump uses Schottky diodes instead of switches. This provide the benefit of a simpler implementation. The efficiency of the charge pump is dominated in this design by the forward voltage drop of the input voltage across the Schottky diodes of approximately $220mV$. In literature bootstrapped switches are often used in order to achieve very low voltage drops during switching. This however comes at the expense of requiring 4 clock phases in order to operate the charge pump [42].

The regulation of the charge pump is performed by comparing the charge pump output with the $1.2V$ bandgap reference voltage by means of a resistive divider. The dynamic comparator is again implemented using the single clock phase dual tail comparator, now using the battery voltage supply. The comparator output triggers an SR latch which controls the charge pump by turning off the resistive divider and the pumping clock signal. The provided $1.8V$ clock signal is level-shifted to a $3.6V$ clock signal that is used to push the bottom plate capacitor of the flying capacitor. The resistors are implemented by means of a unit resistor $R_u = 2.5k\Omega$ which again are p+ poly resistors. A switch at the battery voltage input (SW_1) is added in order to also use an external $5V$ supply during testing of the ASIC. In order to properly enable the charge pump at startup, a switch (SW_2) is added to discharge the

load capacitor to ensure that the ASIC startup sequence is performed correctly.

The charge pump can be enabled by a control signal $S_{Q,Ctrl}$ which resets the latch and pulls the comparator output momentarily to ground. Due to the time constant between the charge pump output and the comparators input V_{IN+} there is a settling time required before the comparator input is accurately settled before the control signal $S_{Q,Ctrl}$ can be put low again. The total resistance is chosen such that the comparator input is able to correctly settle across PVT within 1 clock cycle. The control signal $S_{Q,Ctrl}$ is pulled high 1 clock cycle before one of the resonant pulser switching events (Δi_{1-5}) and is sustained high for 2 clock cycles, ensuring proper functioning of the charge pump. Figure 3.27 shows the simulated waveforms of the charge pump during current transient Δi_1 (at the start of phase ϕ_1). It shows the required settling time of the comparator input node together with the charge pump control signal and latch output signal.

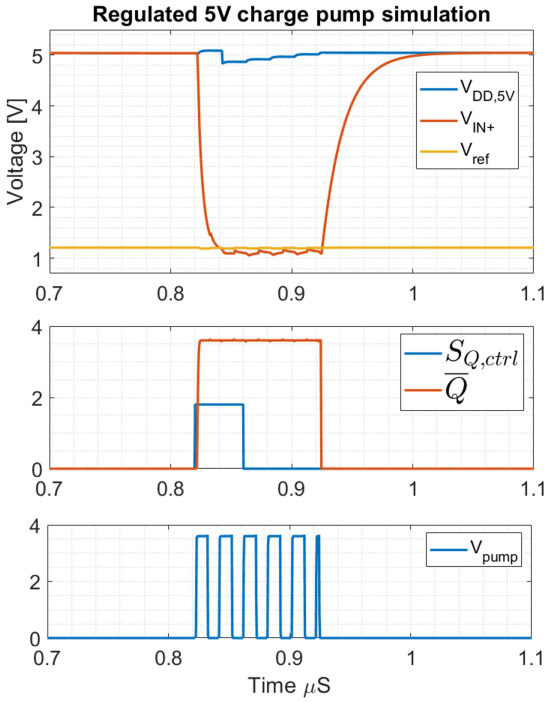

Figure 3.27: Simulation waveform of the regulated charge pump during switching moment Δi_1.

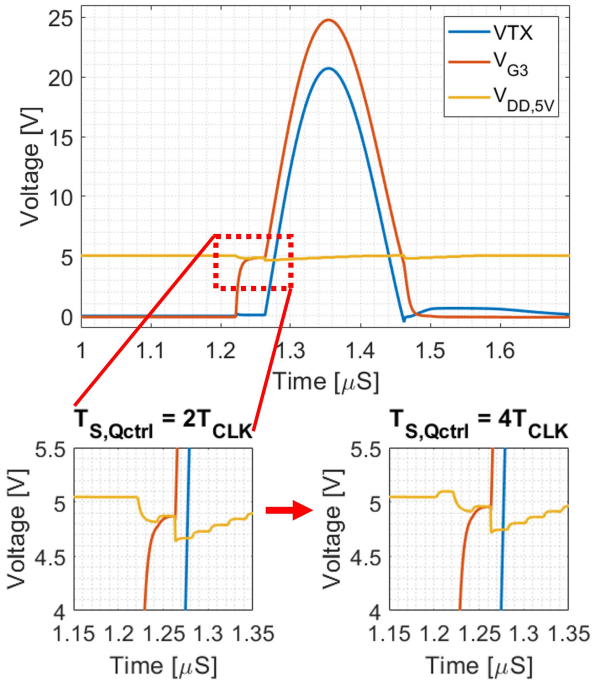

Figure 3.28: Regulated charge pump during timing moment Δi_2, showing the difference in timing of $S_{Q,Ctrl}$.

There is a single problem that arises using this control technique. During the $40ns$ time period required for the HV bootstrap circuit to settle the high-side HV transistors gate to $5V$, the charge pump is unable to reach its steady state output within 2 clock cycles due to the large amount of charge drawn from the $200pF$ load capacitor (i.e, current transient Δi_2). Figure 3.28 shows the simulated waveforms. The resulting V_{gs} across the HV transistor drops by approximately $150mV$, increasing the R_{on} of the device slightly. In order to avoid this the control signal is instead sent two clock cycles earlier compared to the other timing moments as shown in Figure 3.28. As a result, the HV bootstrap circuit is able to properly charge the gate of the HV transistor to $5V$.

3.5.3. Simulation performance

Table 3.4 shows the simulated performance results of the regulated charge pump across corners, here the steady state voltage of the charge pump that is reached initially after start-up is compared with the charge pump output after a single HV pulse has been sent.

It shows that the charge pump achieves a maximum deviation of $120mV$ in the FF corner. Since the accuracy of the charge pump is only limited by the accuracy required by the energy recycling circuit (in order to generate the $V_{DD,5V}/2$ reference voltage) and the $5.5V$ oxide breakdown voltage of the $5V$ transistors, the accuracy of the charge pump is proven to be sufficient.

Table 3.4: Simulated results of the accuracy of the regulated $5V$ charge pump vs process corner

Process corner	$V_{DD,5V}$ (initial) [V]	$V_{DD,5V}$ (after Δi_5) [V]
TT	5.046	5.045
SF	5.044	5.041
FS	5.049	4.945
FF	5.082	5.120
SS	4.941	4.989

3.6. Capacitor-less 1.8V linear regulator

3.6.1. General linear regulator structures and alternatives

The resonant pulser also requires a $1.8V$ supply voltage in order to operate. Some of the circuit components that make use of the $1.8V$ supply are the LV digital circuits, dynamic level shifters, dynamic and static comparators, generating bias voltages, and the amplitude calibration reference voltages. The supply can be generated using a linear regulator, or, a switch-capacitor DC-DC converter. For the latter, due to the relatively slow clock frequency of the system, obtaining a sufficiently low ripple is difficult to implement within a small die area. Also, since the battery supply is not constant the converter architecture would need to be reconfigurable. Therefore, a linear regulator is adopted. The resonant pulser is designed such that the current drawn from the $1.8V$ supply is minimized compared to the $5V$ supply, the power consumption of the linear regulator becomes (far) non-dominant. The most used type of linear regulator is an LDO (low-dropout regulator). Figure 3.29 shows a simplified diagram of a linear regulator together with a traditional implementation of an LDO. The regulator's accuracy and bandwidth should be designed sufficiently to achieve the desired accuracy during amplitude calibration (which forms the strictest requirements on the regulator compared to the other circuity powered by the regulator).

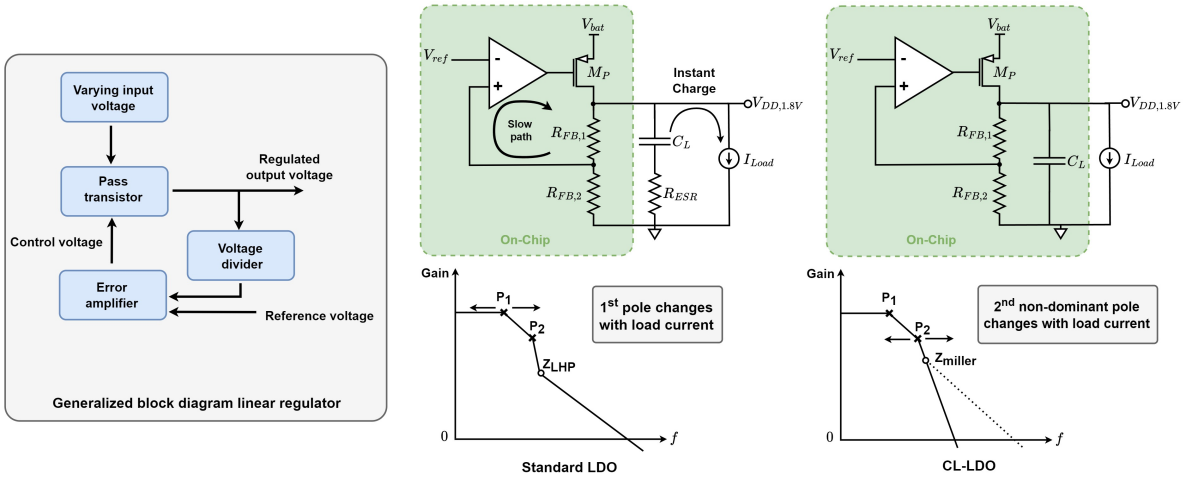

Figure 3.29: Simplified block diagram and circuit diagram of a traditional LDO and CL-LDO with their corresponding frequency behaviour for varying load current.

A linear regulator is built using a simple control loop consisting of a pass transistor (often a PMOS transistor in case of an LDO) supplying the required current from the input source, and a voltage divider in order to make a comparison with a reference voltage using an error amplifier that controls the pass transistor [43]. The reference voltage used in this implementation will be the $1.2V$ bandgap voltage. Due to the limited bandwidth of the error amplifier and limitations of the sinking/sourcing capabilities of the pass transistor the regulator is unable to react fast upon load current transients drawn from the regulator output. For this reason, often a large off-chip load capacitor ($\approx 100's\ nF$ or $\approx \mu F$) is placed at the output which introduces a dominant pole and a left half plane (LHP) zero due to the capacitor equivalent-series resistance (ESR) and provides an instant discharge path to the output [43]. This will ensure a good transient response and ensure stability of the regulator by heavily limiting the bandwidth of the regulator.

The difficulty in this design is the aim is to only have 1 off-chip component, the inductor. This means that only a small on-chip capacitor can be used, which calls for proper frequency compensation and a method to provide better load regulation, Such circuits are often named 'capacitor-less LDOs' (CL-LDO) [44]. In this design, the load capacitor C_L is set to $200pF$, as in the case of the $5V$ charge pump load capacitor, in order to have a small footprint for the entire system. Figure 3.29 shows the differences in the frequency stability of both a traditional and CL LDO. Due to the much smaller C_L of the CL-LDO the output pole of the regulator forms the non-dominant pole of the system and moves as a function of the load current (the pole frequency inversely proportional to I_{Load} in this case). In order to ensure sufficient phase margin active frequency compensation using techniques like miller compensation are often utilized [44].

3.6.2. Proposed linear regulator design

In order to improve the transient response of the regulator a regulator using a NMOS pass transistor is proposed instead of a PMOS transistor. Since this design does not require low-dropout operation an NMOS transistor provides better sinking capabilities compared to a PMOS and a smaller transistor for the same maximum I_{Load} requirement. Figure 3.30 shows the proposed CL-linear regulator.

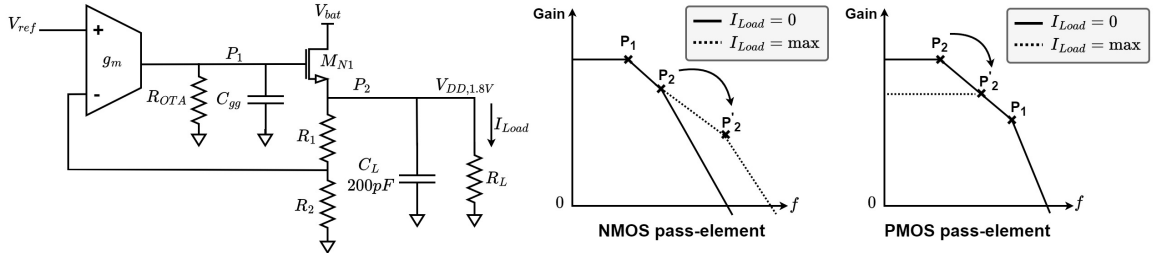

Figure 3.30: Schematic of the proposed NMOS CL-linear regulator.

From simulation under nominal conditions the average static current consumption and peak current consumption on the $1.8V$ supply are determined for the design of the regulator. On average the static current consumption is approximately $150\mu A$ while the peak current consumption required is approximately $1.2mA$. In order to guarantee stability the regulator is designed to deliver a maximum load current of $I_{Load,max} = 10mA$. The size of the NMOS M_{N1} can be determined using the following equation:

$$\frac{W}{L} = \frac{2I_{load,max}}{\mu_n C_{ox} V_{dsat}^2} \tag{3.6}$$

From equation 3.6.2 the width of the $5V$ NMOS transistor M_{N1} is set to $500\mu m$. The resulting gate capacitance of the transistor C_{gg} makes the OTA output pole dominant. This pole resides at a frequency f_{P1} given by:

$$f_{P1} = \frac{1}{2\pi R_{OTA} C_{gg}}, \tag{3.7}$$

where R_{OTA} is the output impedance of the OTA. The non-dominant pole f_{P2} which is now a function of the load current is given by:

$$f_{P2} = \frac{g_{MN1}}{2\pi C_L} = \frac{\sqrt{2\beta I_{Load}}}{2\pi C_L}, \tag{3.8}$$

where the output resistance of the regulator is $\approx \frac{1}{g_{MN1}}$, and we assume $\frac{1}{g_{MN1}} << R_L || (R_1 + R_2)$. The open loop gain A_v of this regulator assuming $R_L << R_1 + R_2$ is given by:

$$A_v = G_m R_{OTA} \cdot \frac{g_{MN1} R_L}{1 + g_{MN1} R_L} \quad , \quad \text{if,} \quad g_{MN1} R_L >> 1 \quad \text{then} \quad A_v \approx G_m R_{OTA} \tag{3.9}$$

Providing effective frequency compensation due to the moving pole can still be difficult, however, due to the relatively small load current that needs to be provided, using traditional compensation techniques can already prove to be sufficient. To ensure stability either the dominant or non-dominant pole

can be compensated. The advantage of compensating the non-dominant pole is that the regulator won't need to suffer from severe bandwidth reduction. The output pole P_2 can be compensated by either making the pole always fall out of the expected bandwidth or by accommodating the movement of P_2 by adding a zero.

For the first case, C_L could be reduced. This would make the response to load-current transients much worse. Alternatively, the feedback resistors could be made smaller, which would increase the quiescent current I_q consumed by the regulator.

For the second case, the added zero should be placed near the output pole frequency in the case for $I_{Load} = 0$, the resulting pole that is added by placing a zero should fall outside the maximum closed-loop bandwidth of the regulator to ensure stability. Figure 3.31 shows the proposed schematic of the linear regulator including the required frequency compensation. For this design an additional zero is added in the feedback path of the regulator. The large feedback resistors R_1 and R_2 are used together with an added capacitor C_z in order to introduce a low frequency zero. The frequency of this zero resides at $\omega_z = \frac{1}{R_1 C_z}$. The addition of this zero also adds a pole at a frequency $\omega_p = \frac{1}{(R_1 || R_2) C_z}$ which is at a frequency 1.5x higher than the zero frequency. During the design of the compensation, the resulting pole is made sure to be set outside the maximum close-loop bandwidth.

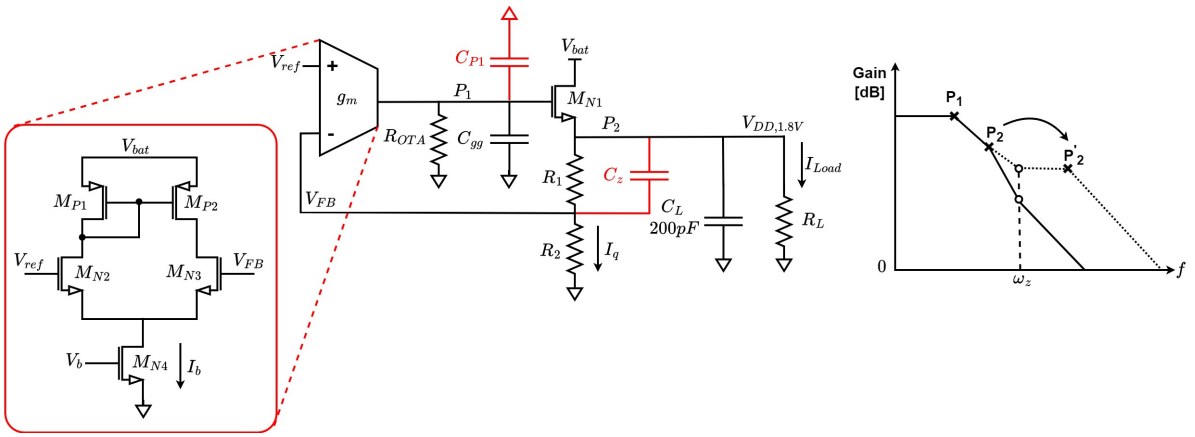

Figure 3.31: Schematic of the proposed frequency compensation for the linear regulator.

By investigating the pole frequencies using simulation, the limited movement of the dominant pole in this system and the placement of the poles makes the proposed frequency compensation a sufficient solution to yield a stable regulator. In order to increase the minimum phase margin (which is at $I_{Load} = 0$) a capacitor C_{P1} is added to move the dominant pole to a lower frequency, trading off some bandwidth for additional stability.

The g_m stage is implemented using a 5-transistor OTA which draws a bias current of $I_b = 5\mu A$. The feedback resistors R_1 and R_2 are implemented using $25k\Omega$ unit resistors creating $R_1 = 75k\Omega$ and $R_2 = 150k\Omega$. These resistors are implemented as p+ poly resistors. The load capacitor C_L is implemented as a $200pF$ $1.8V$ MOS capacitor. Capacitor C_z is $5pF$ and C_{P1} is $8pF$. Both are implemented as MIM capacitors which can be placed on top of the regulator during layout. The resulting quiescent current I_q is $8\mu A$.

3.6.3. Simulation performance

Figure 3.32 shows the stability analysis simulation results where the phase margin of the regulator is plotted against varying load currents for different process corners. The proposed frequency compensation is able to keep the regulator stable at minimum load current and across a range much larger than the expected current that will be drawn from the supply during the operation of the pulser. Under typical conditions (TT corner and $T = 0°C$) the minimum phase margin is $49.1°$, and in the worst case $48.06°$. Across temperature the influence on the minimum phase margin is small (see Figure 3.33). The results show that the phase margin quickly rises for a load current of a few 100 μA and remains stable till $10mA$. The resulting bandwidth and $200pF$ load capacitor are able to provide a sufficient fast transient response for the system. The resulting transient response of the regulator due to the limited bandwidth to achieve proper stability and gain of the g_m cell provides proper performance to achieve

proper operation of the resonant pulser as already shown in the prior section(s).

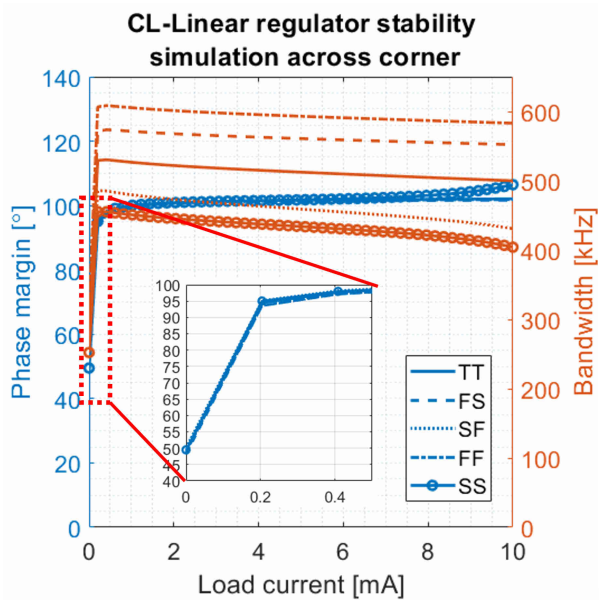

Figure 3.32: CL-Linear regulator phase margin and bandwidth simulation for varying load current across process corner.

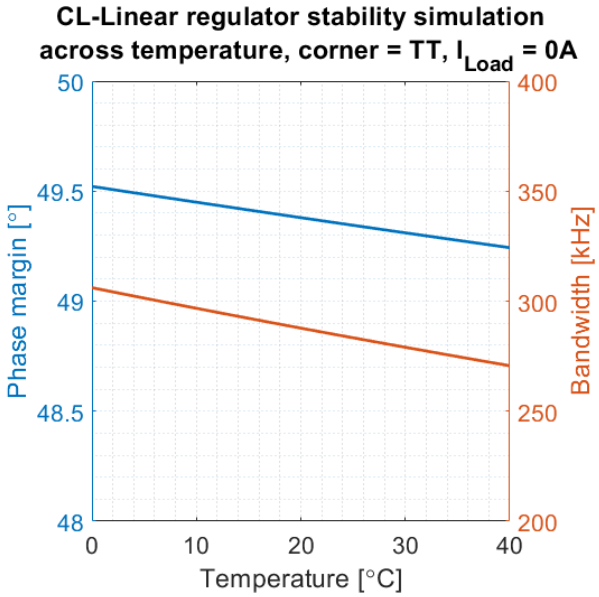

Figure 3.33: CL-Linear regulator phase margin and bandwidth simulation for varying load current across temperature for worst-case stability, i.e. $I_{Load} = 0A$.

3.7. Bandgap reference and biasing

3.7.1. Circuit implementation

One of the final blocks that need to be added to the system are the biasing and bandgap reference voltage. Since the 180nm BCD technology offers bipolar PNP transistors these are used in the implementation of the BGR circuit. Furthermore, the BGR circuit is supplied directly from the input battery supply which can vary between $3.3V - 3.9V$. Therefore a circuit that is able to generate a supply-independent current is necessary. In order to generate a voltage that is nominally independent of temperature either a summation of two voltages having opposite temperature coefficients (TCs) can be performed, or a summation of two opposite TC currents can be performed whereafter the resulting current flows through a resistor to generate the required voltage [45]. For the implementation of this BGR, the latter technique will be used due to its simplicity.

Figure 3.34 shows a typical core of a BJT BGR [45], [46]. Here a pair of two NPN BJTs are used whose emitter areas differ by a factor n and an amplifier ensures $V_x = V_y$, this condition leads to the following expression:

$$V_{BE1} = V_{BE2} + I_{D,MP2} \cdot R_1 \tag{3.10}$$

$$V_T \ln \frac{I_{D,MP1}}{I_{S,Q1}} = V_T \ln \frac{I_{D,MP2}}{I_{S,Q2}} + I_{D,MP2} \cdot R_1$$

Assuming the emitter area of Q_2 equals an n amount of parallel unit BJTs of a size equal to the emitter size of Q_1 we have $I_{S,Q2} = nI_{S,Q1}$ which simplifies the equation to

$$I_{D,MP2} \cdot R_1 = V_T \ln(n) \tag{3.11}$$

Transistors Q_1, Q_2 and resistor R_1 create a proportional-to-absolute-temperature (PTAT) loop if the condition $V_x = V_y$ is held. Channel length modulation that is introduced by transistors M_{P1} and M_{P2} affects the matching accuracy of the two current branches I_x and I_y. Equation 3.11 shows that the voltage across R_1 is PTAT, and thus the current flowing through M_{P1} and M_{P2} if R_1 has 0 TC. By adding a voltage that has a negative TC, i.e. the V_{BE} of a BJT, a reference voltage with 0 TC can be created which can be described as:

$$V_{ref} = V_{BE} + V_T \ln(n) \tag{3.12}$$

Here it becomes clear that a 0 TC reference can be obtained in case a proper value for n is chosen. The work presented in [45] derives that a value of $\ln(n) = 17.2$ is necessary to obtain 0 TC, in order to avoid this impractical large scaling factor for the bias current $V_T \ln(n)$ is amplified before it is added to a V_{BE}.

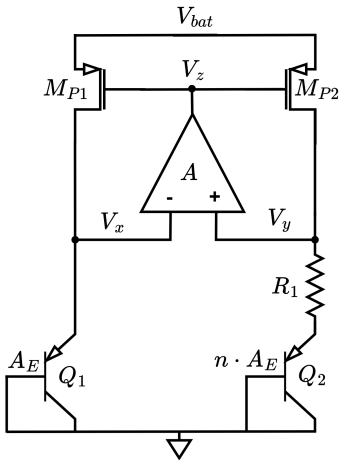

Figure 3.34: Basic BJT-based bandgap core.

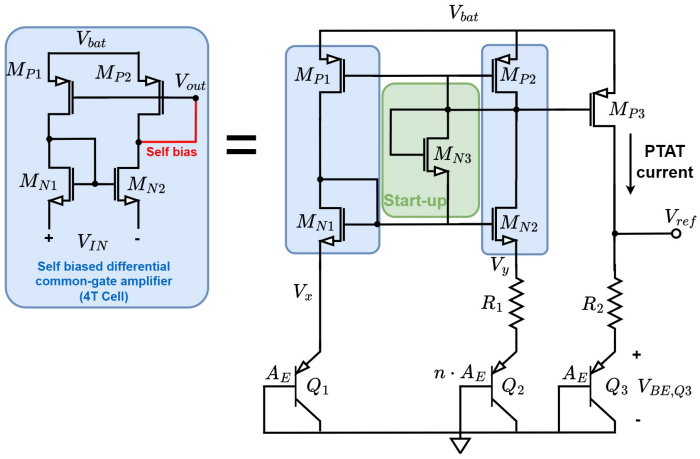

Figure 3.35: Implemented BGR circuit using a 4T common-gate amplifier and a simple start-up circuit.

Figure 3.35 shows the circuit implementation of the BGR circuit that generates a reference voltage of $1.2V$. Instead of using an OPAMP, a self-biased differential common gate amplifier is stacked on top of transistors Q_1 and Q_2. This structure reuses its biasing current to bias Q_1 and Q_2. The resulting PTAT current is copied to an additional current branch in order to perform the TC cancellation. The resulting reference voltage V_{ref} can simply be described as

$$V_{ref} = |V_{BE,3}| + \frac{R_2}{R_1} V_T \ln(n) \tag{3.13}$$

By properly sizing transistors M_{P1-2} and M_{N1-2} the resulting error in the generation of the PTAT current due to channel length modulation is avoided. For this design the resistors R_1 and R_2 are implemented using $5k\Omega$ unit p+ poly resistors creating $R_1 = 20k\Omega$ and $R_2 = 215k\Omega$. This type of resistor does have a slight positive TC however, to first order its TC does not matter. The BJT transistors have a unit emitter area A_E of $2\mu m \cdot 2\mu m$ and for this design, the current is scaled by a factor of $n = 6$. Finally transistor M_{N3} is added to be used during the start-up of the BGR circuit. During initial start-up, a situation could arise where initially all node voltages $V_{gs,MP1} = V_{gs,MP2} = V_{gs,MN1} = V_{gs,MN2} = 0$, resulting in no current flowing through any of the devices. Transistor M_{N3} avoids this by being turned on first and in turn turning on transistor M_{N1} and M_{P2}, where after transistors M_{N2} and M_{P1} are turned on and finally M_{N3} is turned-off (this holds under the conditions $V_{th,MN1} + V_{th,MN3} + |V_{th,MP2}| + V_{BE} < V_{bat}$ and $V_{gs,MN1} + V_{th,MN3} + |V_{gs,MP2}| + V_{BE} > V_{bat}$).

3.7.2. Simulation performance

Figure 3.36 shows the simulation results for the BGR circuit reference voltage across temperature and process corner. In the TT corner the total deviation in V_{ref} equals $\Delta V_{ref} = 4.77mV$. Figure 3.37 shows the simulation results now for varying the battery input supply, here in the TT corner $\Delta V_{ref} = 20.5mV$.

Figure 3.38 shows the transient start-up behaviour of the BGR circuit. The circuit is able to properly enable itself across process corners and settle properly within a time of $t_{start-up} = 400ns$.

Finally, Figure 3.39 shows the complete circuit schematic of the BGR circuit together with the required biasing branches for the resonant pulser. Here the biasing voltage for the CT comparator for the trim circuit is generated and copied to the circuit, also the biasing voltage for the linear regulator is generated and copied to the regulator OTA. Additionally, a small load capacitor $C_L = 3pF$ is added

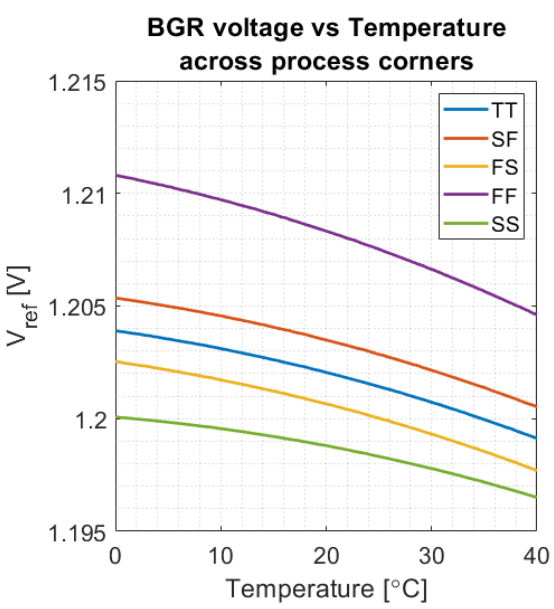

Figure 3.36: Simulation of the generated BGR reference voltage against varying temperature across process corner.

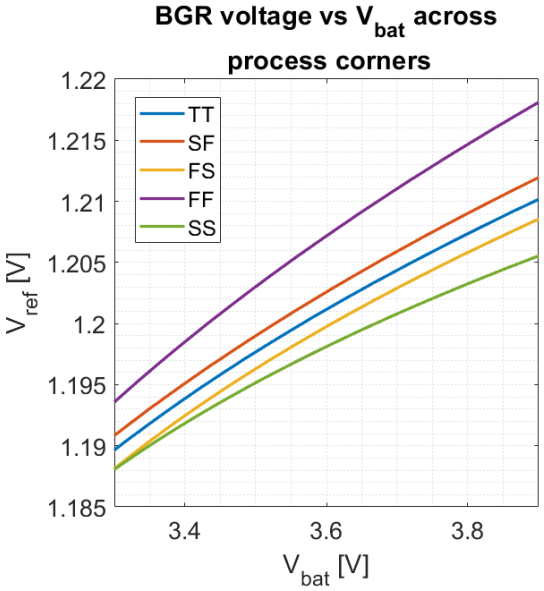

Figure 3.37: Simulation of the generated BGR reference voltage against varying input battery supply voltage across process corner.

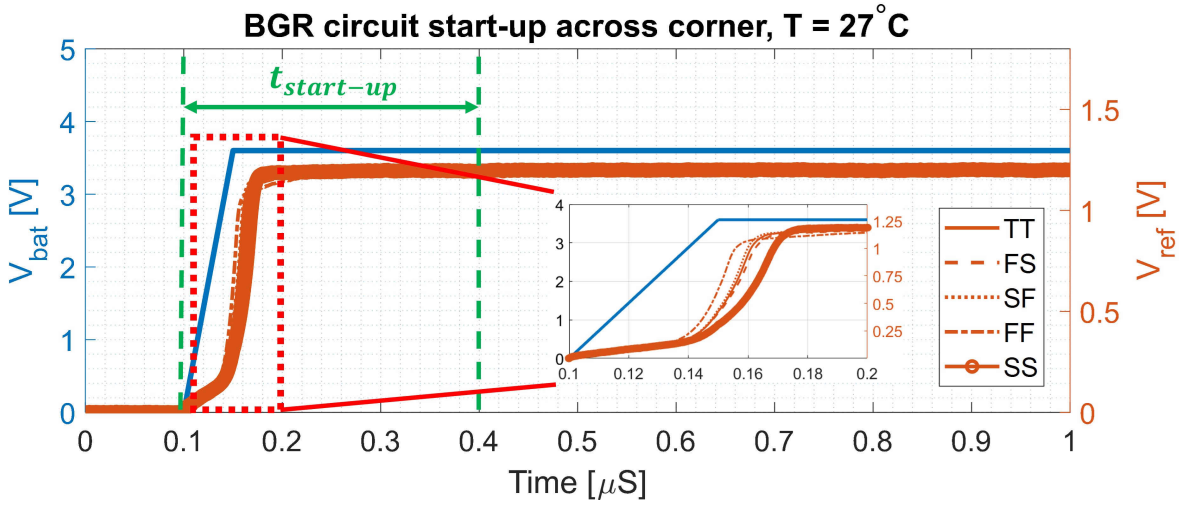

Figure 3.38: Simulation result of the transient start-up behaviour of the BGR circuit across process corner.

to obtain better regulation of the reference voltage due to e.g. charge kick-back that is introduced by the different comparators in the system that use the reference voltage. Transistors M_{P4} and M_{P7} are controlled by enable signals in order to turn on and off the biasing of the CT comparator and linear regulator. The accuracy of the reference source and biasing branches that are used by the different blocks in the system have already been verified in the prior section to work sufficiently across PVT and other system variations during the operation of the pulser.

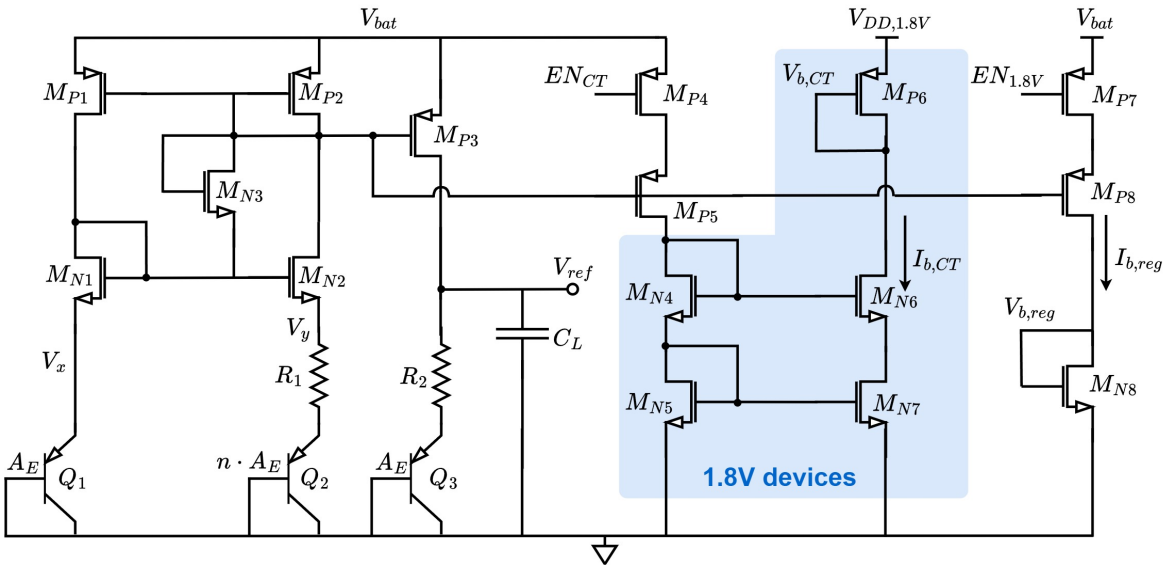

Figure 3.39: Complete circuit schematic of the BGR circuit together with the biasing branches required for the resonant pulser, all other NMOS and PMOS transistors are implemented using $5V$ devices.

3.8. Non-over operation

An important operational feature of the pulser is to guarantee non-overlapping operation during pulsing. Due to the difference in delay in the level shifters and gate driver delay of the switches of the resonant pulser's core, a situation could arise where the input battery supply gets shorted to ground. Figure 3.40 shows the problematic situation that could arise in case the propagation delay of the different switches varies too much across PVT. In simulations, this is also visible. In order to guarantee proper non-overlapping operation of the pulser a small delay element is enabled for the LV PMOS input transistor which is enabled during the operation of the switch during the energy recycling phase (ϕ_3). In this way, the delay of the LV PMOS is designed such that the resulting delay across PVT avoids shorting the input to ground.

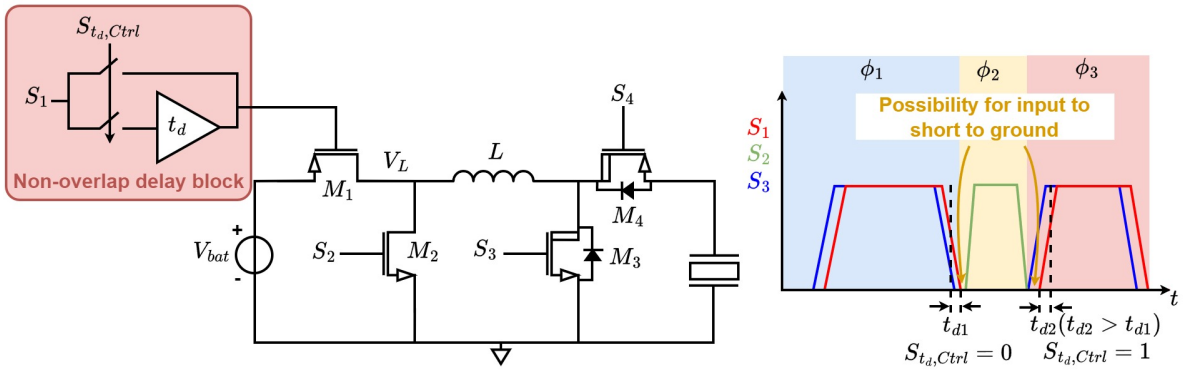

Figure 3.40: Simplified example of the resulting non-overlap operation of the resonant pulser.

3.9. TR switches

3.9.1. Switch topology

In order to perform a pulse-echo measurement during the measurement of the ASIC, each of the two channels contains a TR switch which makes it possible to measure the echo signal received by the transducer. In literature, different to incorporate a TR switch into a traditional class-D pulser consist of either adding a separate switch that connects to the transducer[47] or having an (often LV) switch built

into the pulser itself [6]. For the resonant pulser, the TR switch can, in theory, be implemented in both ways. Figure 3.41 shows the circuit implementation of both techniques.

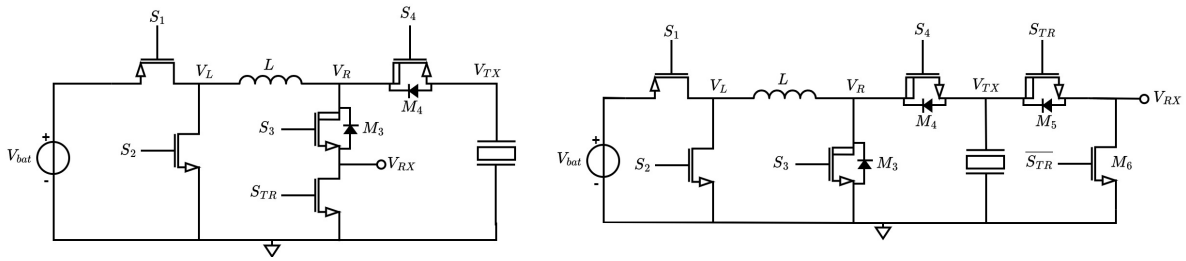

Figure 3.41: Simplified circuit schematic of two possible ways to implement a TR switch in the resonant pulser, (left) incorporating an LV switch inside of the pulser hence having a built-in TR switch, (right) a traditional TR switch using an HV switch to protect the receive channel.

The method using a built-in TR switch can be implemented by placing an LV $5V$ NMOS transistor underneath the low-side HV NMOS. During pulsing this LV transistor is turned on, preventing a high voltage from developing across the drain-source terminals of the device. During receive, this LV transistor is turned off, keeping V_{RX} floating. By turning on the HV transistors, the echo signals from the transducer are accessible from node V_{RX}. This technique leads to a dead time between TX and RX equal to the discharge time during the energy recycling phase (phase ϕ_3) before echoes can be received. More importantly, this technique is incompatible with the proposed channel multiplexing, since the low-side HV NMOS is shared with each transmit (and thus also receive) channel. Also, since this transistor is in the current path of the pulser during charging and discharging of the inductor its R_{on} needs to be made non-dominant which leads to a large transistor required on each channel. Therefore, the traditional option of using an additional HV switch that connects to the transducer is used to implement the TR switch for the resonant pulser. An additional benefit is that the dead time between RX and TX can be made very small, making the resulting reduction in the near field image negligible.

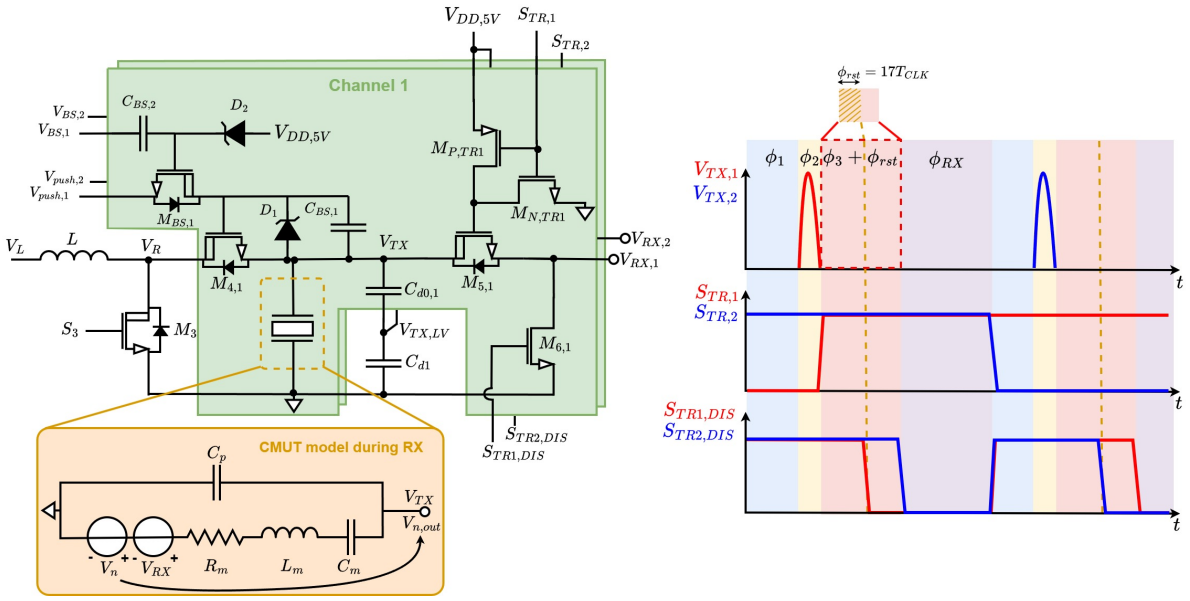

Figure 3.42: Circuit implementation of the TR switches on the 2 transmit channel implementation of the resonant pulser, also showing the timing diagram.

Figure 3.42 shows the detailed implementation of the TR switch in the resonant pulser together with its timing diagram. After a transmit pulse has been sent, the resonant pulser recycles the inductor energy back to the voltage source. Due to the fact that the transducer is not an ideal capacitor, energy is still present on the transducer in both the electrical field of C_m and in the magnetic field of L_m. Before

reception can begin the transducer needs to be properly discharged which is done by simply enabling the TR HV switch M_5 and keeping the TR LV NMOS M_6 enabled for a time period ϕ_{rst}, which equals the required time to guarantee V_{TX} has dropped to approximately $1mV$.

Another important function that the TR switches fulfill is in the operation of the capacitive attenuator. The resonant pulser uses a shared attenuator across the different transmit channels in order to save area due to the relatively large amount of space the MOM capacitors require, especially if each channel would require an entire attenuator (also, to achieve the desired linearity the MOM capacitors can't be scaled much further down). Since the resonant pulser only pulses 1 element at a time, the capacitor that is placed between the other transducer output and the midpoint of the attenuator is connected to ground via the TR switches of the other channel. The prior simulation results shown in the previous sections already contained the TR switches; hence their effect on the non-linearity of the attenuator already has been accounted for during the design.

3.9.2. Noise and crosstalk

The sizing of the TR switch, especially the HV transistor, involves a trade-off in between area consumption, added parasitic capacitance in parallel with the transducer, and the amount of added noise on the receive channel. Since the receive chain is implemented off-chip, there is no strict requirement on the noise figure (NF) of the TR switch. For this design, the TR switch is scaled to obtain a 3dB NF, the added noise from the TR switch is equal to the rms noise from the transducer (see Figure 3.42). Within the bandwidth of the transducer, R_m dominates the transducer noise which can be described as:

$$v_n = \sqrt{4kTR_m} = 5.16nV/\sqrt{Hz} \tag{3.14}$$

The rms noise that is then present at the drain of the TR switch at the resonance frequency of the transducer is found using:

$$v_{n,out} = v_n \frac{Z_{C_p}}{Z_{C_p} + Z_{L_m} + Z_{C_m} + R_m} = 1.408nV/\sqrt{Hz} \tag{3.15}$$

From this, we obtain the minimum transistor width of $W_{M,TR} = 80\mu m$, which adds around $522fF$ C_{dd} loading the transducer further with some additional capacitance. The LV NMOS transistor is sized $20\mu m$ wide. From simulation, the minimum required discharge time across PVT is found to be $\phi_{rst} = 334ns = 17T_{CLK}$.

The implementation of the shared attenuator does of course create a capacitive connection between the two transmit channels leading to crosstalk during transmit. Crosstalk between the different transmit channels leads to parasitic transmit on other transducer's. On an array this could become problematic since large parasitic transmit located at different elements could make the image reproduction process problematic. The crosstalk in the circuit is simulated between the two transmit channels and is shown in Figure 3.43. The crosstalk in dB is defined as:

$$\text{Transmit channel crosstalk} = 20 \cdot \log\left(\frac{|V_{TX,2}|_{max}}{|V_{TX,1}|_{max}}\right)[dB] \tag{3.16}$$

From the results, it is clear that the design provides enough suppression during pulsing in order to avoid parasitic transmit on the other transducer(s). For a $30V$ pulse the resulting peak voltage measured at the second transducer is below $60mV$.

3.10. Total prototype chip overview

3.10.1. Versions of the prototype

For the prototype design of the resonant pulser, two different designs were implemented. one that contains the entire design of the pulser as discussed so far i.e. a two-channel pulser including TR switches, and a second design that implements a single channel transmit only pulser. The two designs are indicated as 'TR' (transmit and receive) and 'TO' (transmit only) respectively. This single-element pulser has been optimized in the same way that the TR version has, the biggest difference in the sizing of the two ASICS is the twice larger input PMOS transistor ($3000\mu m$) in order to achieve a more efficient pulser.

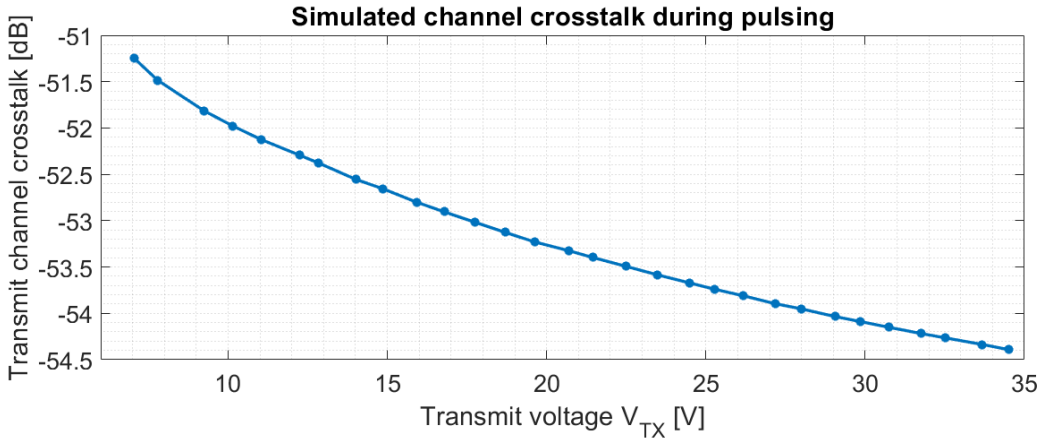

Figure 3.43: Simulation results for the channel crosstalk due to the shared capacitive attenuator for varying transmit amplitudes.

3.10.2. Digital controller

The final piece in the system design of the resonant pulser is designing the required digital controller. All of the logic is synthesized on an FPGA instead of implementing the logic on-chip, to achieve flexibility during the measurements of the chip. Since the required logic can all be synchronously clocked, an RTL (register transfer level) based FSM (finite-state machine) is designed in order to control the resonant pulser.

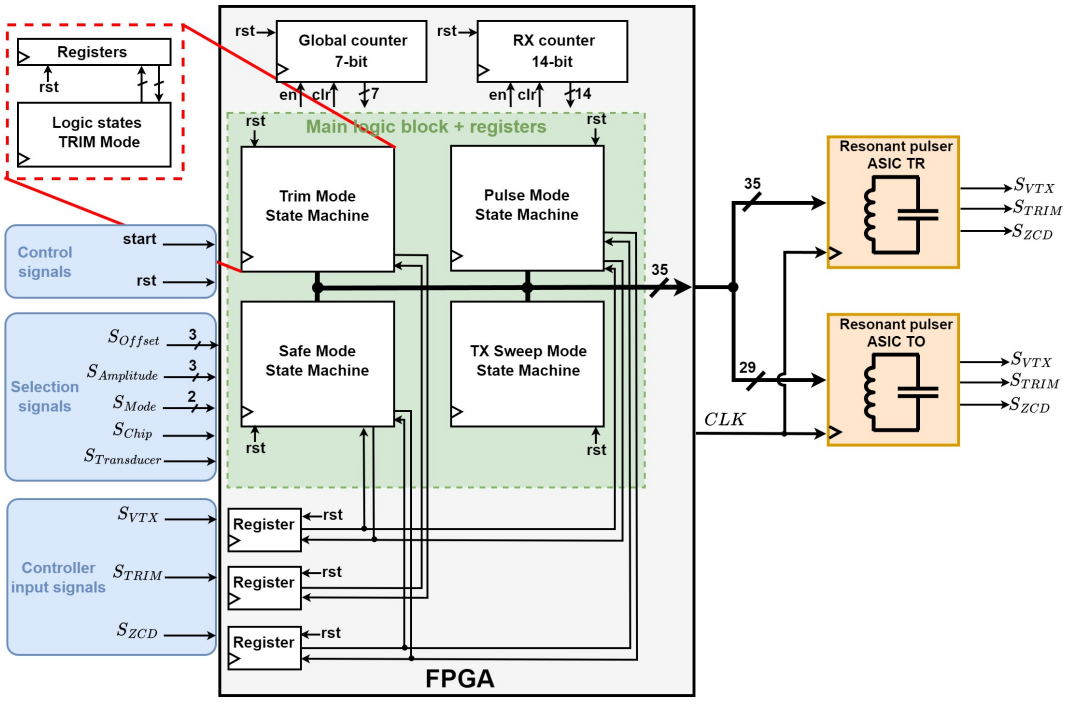

Figure 3.44: Simplified block diagram of the implemented digital controller on an FPGA.

Figure 3.44 shows a simplified diagram of the digital controller's implementation in synthesized Verilog. The controller contains 4 main modes of operation, the first being the 'TRIM Mode', which controls all logic required to perform the automatic trimming of the different transducer elements. The different trim settings are saved to registers which are used in the other modes in order to properly operate the pulser.

The second operation mode is the 'PULSE Mode' which performs first the automatic amplitude calibration depending on the desired transmit level that has been selected. After performing this automated

step (which happens at a very high RPF of $> 500kHz$) the pulser is pulsed according to the desired number of pulses and PRF which can be selected by defining a desired receive period. The energy recycling calibration is also automatically performed in the first 4 transmit cycles during the pulsing cycles. Also, the controller can be set to only pulse on one of the elements or ping-pong between the two transmit channels.

The third mode is the 'SAFE Mode' which is essentially the same logic as the prior Pulse Mode. Now, the CT circuit is continuously enabled in the background to monitor the transmit output to avoid causing latch-up-related problems in case the resulting trim settings are incorrect.

Finally, the pulser can operate in its 'TX SWEEP Mode' which performs a transmit amplitude sweep that can be used during the measurements of the chip in order to validate the transmit efficiency of the pulser for a wide range of transmit amplitude. The controller employs a global reset 'rst' and 'start' signal. Furthermore, the controller has a few selection signals at its input. Here 'S_{Offset}' is used to select and change the amount of offset used in the CT circuit during the trim operation of the resonant pulser. The signal '$S_{Amplitude}$' defines the desired transmit amplitude and 'S_{Mode}' selects the desired controller logic mode.

The selection signal 'S_{Chip}' is used to select between the different required logic states in the FSM's for the two systems. Finally, the selection signal '$S_{Transducer}$' is used to select whether the CMUTs or an ideal capacitor of $120pF$ is connected to the ASIC, this setting changes the predefined recycle period given a certain charge period during the amplitude calibration phase, these values are stored in a LUT (Look-up-table) and have been found from simulation results.

From the ASIC the FPGA receives 3 input signals, from the amplitude calibration circuit 'S_{VTX}', transducer trim circuit 'S_{TRIM}' and from the energy recycling calibration circuit 'S_{ZCD}'. All of the control signals from and to the FPGA are clocked on the chip in order to properly operate the pulser. Furthermore, the FPGA implements a global 7-bit counter used in the state logic in order to define and control the different operation phases of the pulser, a second 14-bit counter is used during the receive phase of the pulser, allwoing a minimum PRF of 5kHz to be selected.

Figure 3.45 shows a simplified FSM diagram of the PULSE Mode logic for the TR ASIC. Within 8 transmit pulses the amplitude gets calibrated where the first 6 cycles are performed using a binary search using the $50MHz$ clock, the final 2 pulses are generated using some logic and the build-in fine delay elements in order to achieve the proper transmit amplitude. In order to fully use the 6-bit range a non-binary search is used in order to add some redundancy to the search process. Also, the maximum charge time is capped at 37 clock cycles in order to guarantee a maximum transmit amplitude of $40V$ across system and PVT variations. This guarantees that the $40V$ limit on the HV transistors does not get exceeded. After amplitude calibration pulses are sent according to a desired RX period for a number of M pulses, here during the first 4 pulses also the energy recycling is automatically calibrated.

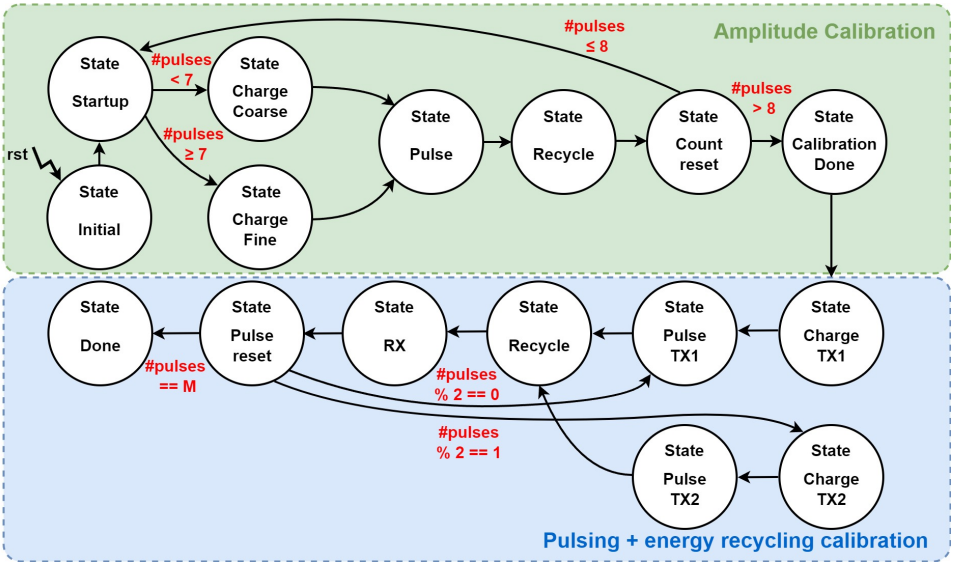

Figure 3.45: Simplified FSM diagram of the PULSE Mode logic for the TR ASIC. The pulsing is alternated between the two channels and a total of M are sent.

3.10.3. Prototype chip

Figure 3.46 shows a total circuit overview of the resonant pulser, the 2-channel resonant pulser contains all of the prior discussed circuit blocks and some small additional (digital) blocks. The three output signals from the ASIC to the FPGA are clocked on the ASIC with a D-type flip flop (DFF), furthermore, all timed control signals from the FPGA to the ASIC are also clocked with a DFF. All non-timing critical and selection signals are fed in directly from the FPGA instead of loading the digital values inside a shift register, this is done since enough IO pads are available for the design of the ASIC, this also adds some additional flexibility during testing of the ASIC. For the sampling signal which is triggered halfway through the pulse generation, the sampling moment can be controlled to have the $5ns$ fine delay control and can be triggered on the falling edge of the clock.

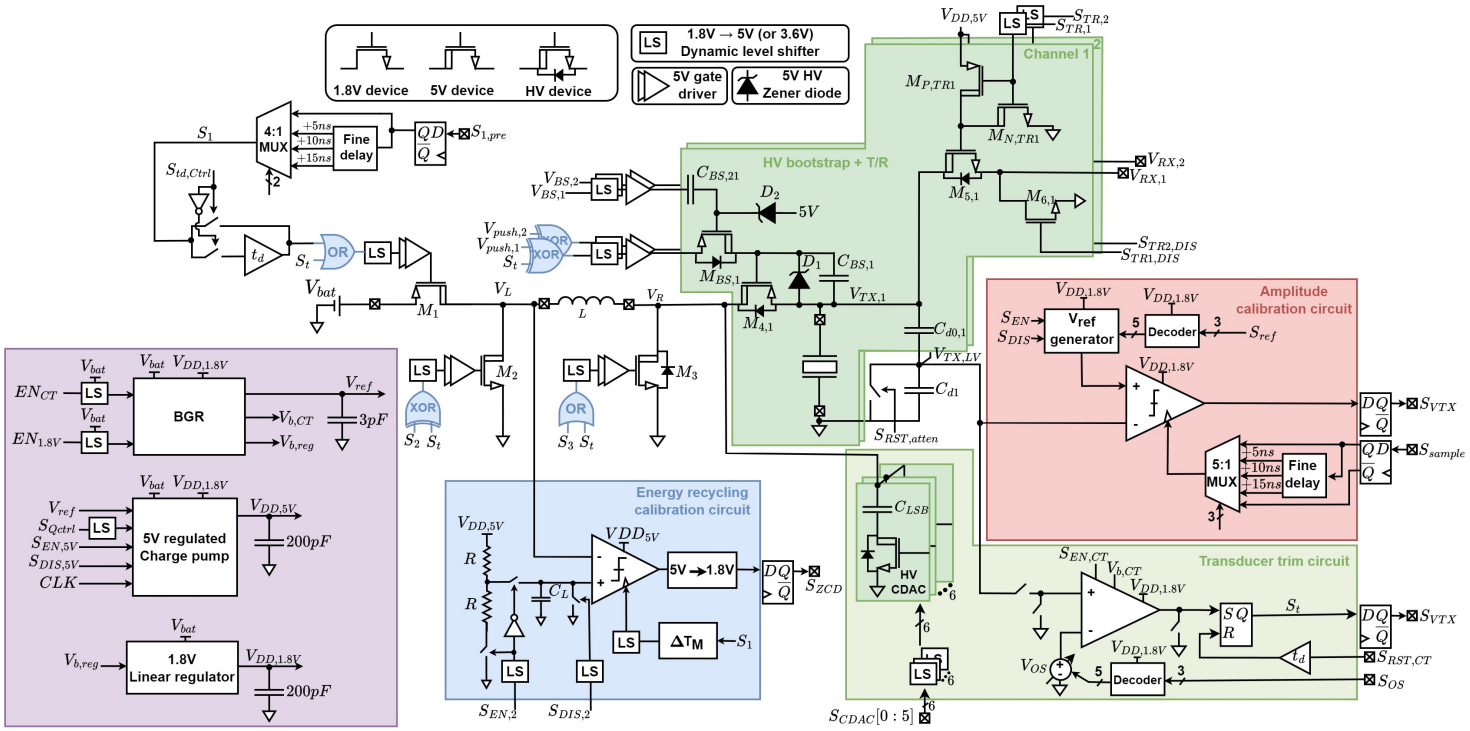

Figure 3.46: Simplified circuit overview of the TR resonant pulser, implementing 2 transmit channels.

3.10.4. Energy efficiency

This section presents the simulated energy efficiency of the resonant pulser ASIC for generating a single calibrated pulse. Figures 3.47 and 3.48 show a breakdown of the total energy consumption of both ASICs. Here it becomes clear that the energy consumption is dominated by the acoustic dissipation in R_m. As expected from the analysis performed in the previous chapter, the dissipation losses through the switches M_{1-4} dominate the energy dissipation in the ASIC compared to the gate drive losses and other required circuitry in the ASIC.

Figure 3.49 shows how this total energy consumption varies as a function of the pulser's transmit amplitude. For the TR ASIC the energy consumption remains roughly equal for transmit pulses between $15V - 30V$, only for small transmit pulses of $10V$ the contribution of the gate drive losses becomes more dominant resulting in relatively higher energy consumption. This is also visible for the TO ASIC, which has been designed to approximately achieve the same efficiency at $10V$ as the TR ASIC whereas it achieves slightly higher efficiency for higher pulse amplitudes. Figure 3.50 elaborates further on this observation. Here a breakdown is shown of the different sources of energy dissipation and how they relatively scale with transmit amplitude. For all these results the energy is normalized to the energy consumed by a class-D pulser driving an ideal $120pF$ capacitor. Whereas the actual total load driven by the resonant pulser in simulation is actually higher due to parasitics and the HV CDAC (and the energy dissipated in R_m). With this in consideration, it shows that the resonant pulser achieves a peak

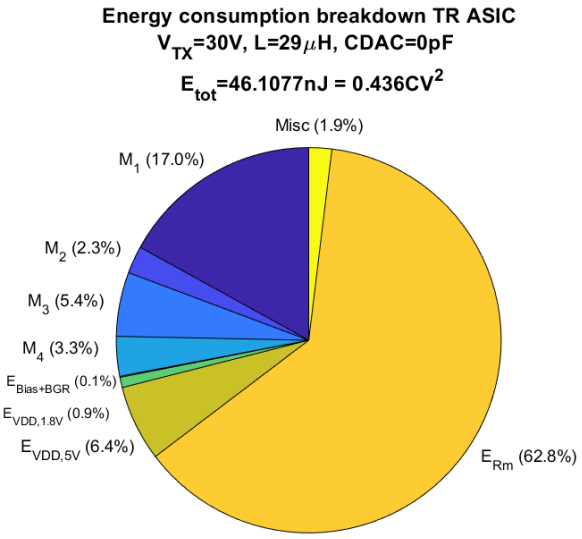

Figure 3.47: Breakdown of the energy consumed in the generation of a single $30V$ transmit pulse with the TR ASIC

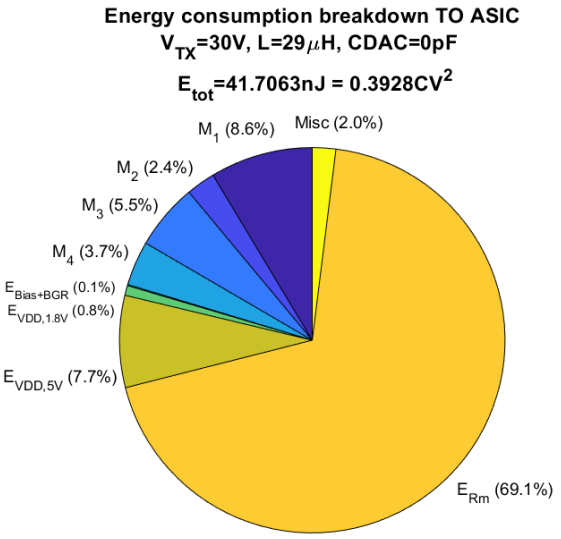

Figure 3.48: Breakdown of the energy consumed in the generation of a single $30V$ transmit pulse with the TO ASIC

energy efficiency of $0.39CV^2$, which corresponds roughly with the calculated efficiency in the feasibility analysis.

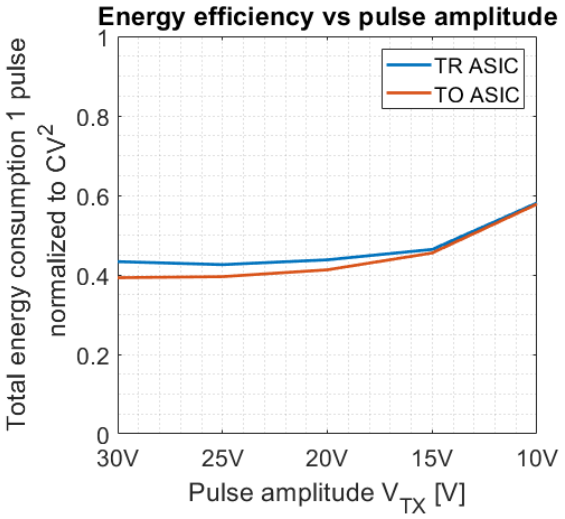

Figure 3.49: Total normalized energy consumed by the resonant pulser vs pulse amplitude.

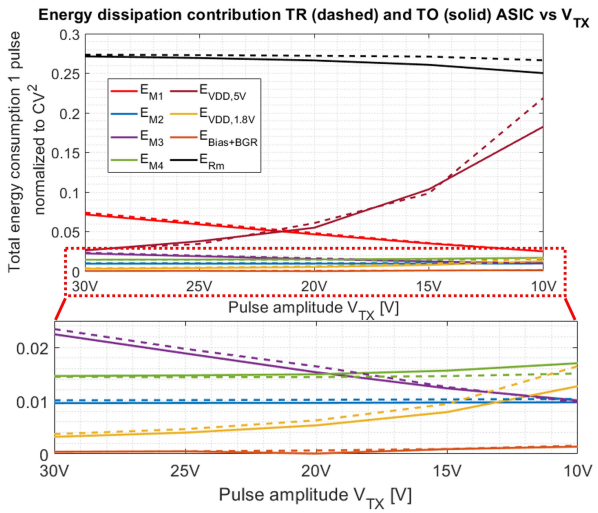

Figure 3.50: Breakdown of the amount of energy consumed by the resonant pulser vs pulse amplitude.

In literature often the average power consumption of the pulser is measured at the input of the system [14], [17] and [15], just like how the energy efficiency has been determined in this section so far. This of course makes the efficiency of the pulser dependent on the type of transducer that has been used. For this reason, often a capacitive load is used instead of a transducer to report the efficiency of a pulser design. The effect on the size of the parasitic capacitance of the transducer and the resonance frequency of the transducer has already been highlighted during the feasibility analysis. Of course, within the BW of the transducer, R_m dominated the impedance of the transducer and hence determines the 'efficiency' of the resonant pulser, to be more specific the amount of energy that can effectively be recycled back. Figure 3.51 shows how the dissipated energy for generating a single $30V$ pulse varies of varying R_m with the $2.5MHz$ CMUT BVD model. The highest amount of energy dissipated in R_m occurs as expected around the value of R_m where the motional branch of the transducer BVD model becomes critically damped, this of-course also relates to the total R_{on} of the switches compared to the value of R_m. If we define the 'acoustic efficiency' as $E_{Rm}/E_{battery}$ where $E_{battery}$ is the amount

of energy supplied from the input battery supply we can see that an efficiency of almost 75% can be obtained in case the transducer would be closer optimized for its transmit efficiency. This of course leads to diminishing returns on the operation of the resonant pulser since the residual energy left on the transducer decreases.

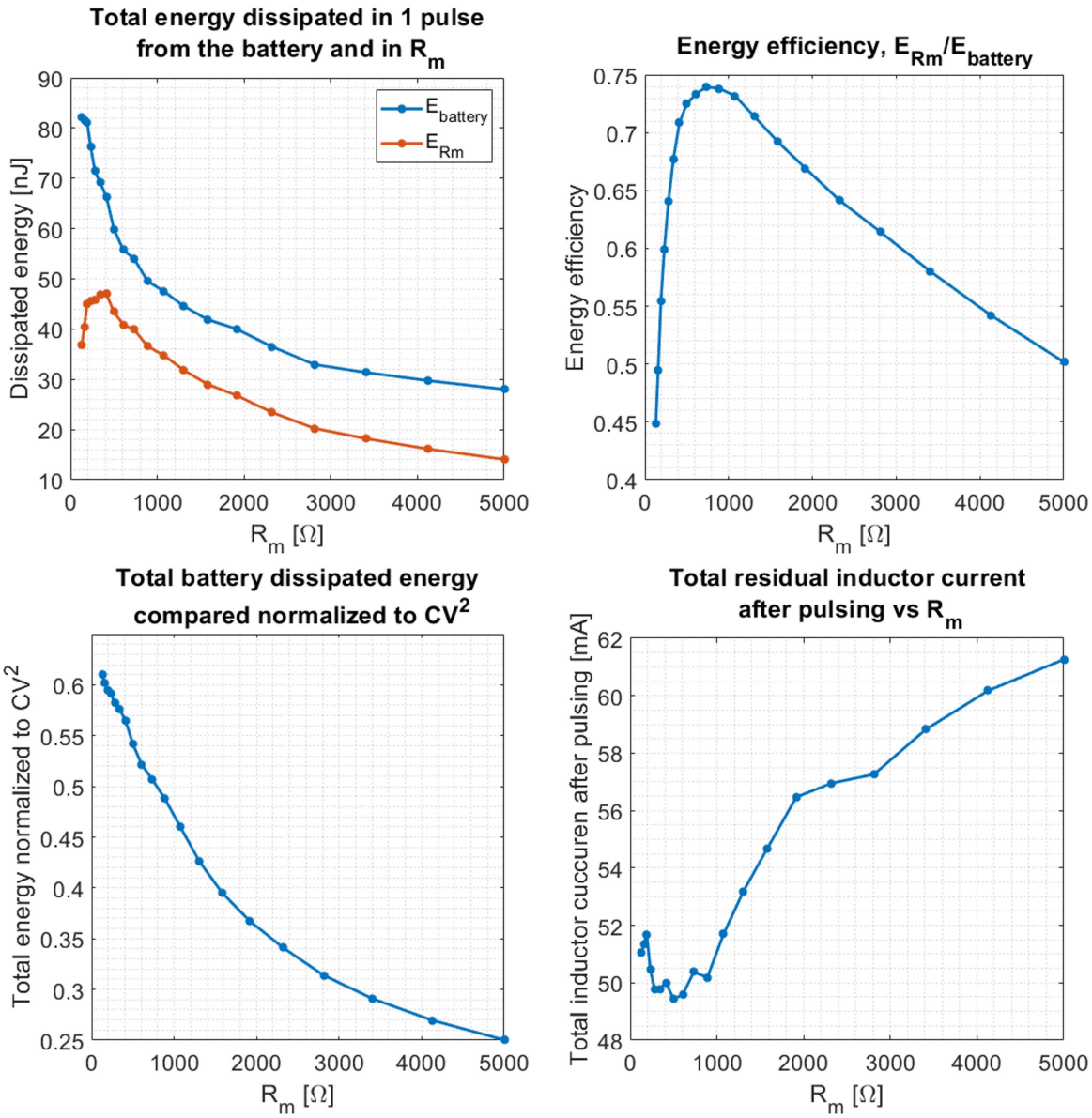

Figure 3.51: Dissipated energy and acoustic efficiency of the TR ASIC vs varying transducer R_m during the generation of a single $30V$ pulse.

4

Chip level design

A chip layout has been designed and taped out for the resonant pulser prototype ASIC. This section will discuss a selection of relevant issues and considerations faced during the layout process of the ASIC. Both TR and TO ASICs have been taped out, and their post-layout performance has been thoroughly simulated and verified. Furthermore, considerations in regard to the measurements for the ASIC are also discussed, including the padring design of the ASIC and its total power efficiency.

4.1. Design for test

In order to properly perform all required measurements for the ASIC some small additions are added to the design of ASIC prior to layout. For the measurements both electrical and acoustic measurements will be performed, the current design of the ASIC has a few reliability concerns that need to be addressed. The first concerns the CMUT array that is pulsed, Figure 4.1 shows a picture of the CMUT array which consists of 64 elements. The CMUT elements share a common HV bias network consisting of a large resistor of $1M\Omega$ and a capacitor of $47nF$. The other terminals of the CMUTs are individually accessible through the flex PCB connector. The long flex cable introduces a large parasitic inductance in the ground loop which connects to the ASIC (approximately 100's of nH). This large inductance might cause substantial ringing in the substrate of the ASIC especially since the substrate already is quite active during the HV transmit period. This might cause problems during the trim phase of the transducer since the CT circuit actively makes a comparison to substrate ground in order to correctly perform the trim operation and avoid causing any body diodes to get set in forward bias.

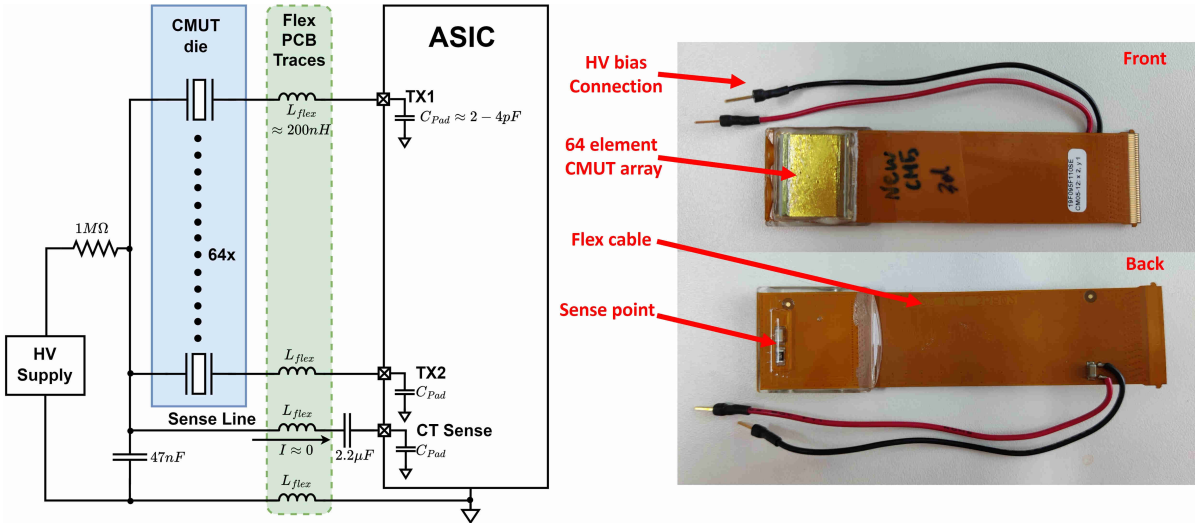

Figure 4.1: Circuit implementation of the proposed sense line and its connections to the CMUT die and ASIC(left), picture of the 64-element CMUT array (right).

To mitigate this problem, the CT circuit reference input can be switched between substrate ground and a sense line connecting to an appropriate sense point on the CMUT array, in order to avoid false triggering of the CT circuit due to heavy substrate ringing. The sense line connects between the R and C of the HV bias circuit of the CMUT array, which are attached behind the CMUT array and could be made accessible by a small modification. By means of inserting a $2.2\mu F$ capacitor an appropriate AC coupling is made which can connect to a pad.

Up to 2 transducer's can be pulsed which can be selected from a set of 4 transducer's. During pulsing all other elements have their top electrode shorted to ground in order to avoid any edge effects on the array, the 2nd and 63rd elements are used for pulsing together with elements 16 and 48.

A second additional design consideration was to make the internal $1.8V$ and $5V$ supplies also externally available. By means of the ability to switch off both supplies and disconnect the input supply from the charge pump, an external supply voltage $V_{DD,ext,1.8V}$ and $V_{DD,ext,5V}$ can be supplied to the ASIC in case issues arise in properly generating the supplies internally.

The final additional piece of circuitry that needs to be added to the ASIC design is overvoltage protection on the internal $5V$ supply and HV ESD (electrostatic discharge) protection to the pads that connect to the transducer's. For the $5V$ supply, a simple series resistor and Zener diode are added to the output of the 5V supply. The Zener diode has a reverse Zener voltage equal to approximately $5.7V$. A 200Ω p+ poly resistor is placed in series in order to limit the current flowing through the diode. Finally, the ASIC requires protection against ESD on the HV pads. ESD can be a dangerous phenomenon that can easily destroy (part of) the ASIC during bonding of the ASIC or just touching the pad. The other analog and digital pads connect to IO cells underneath which contain appropriate LV ESD protection circuitry. The exposed metal pads that connect the pulser output to the transducer's require an HV ESD protection circuit. Figure 4.2 shows the circuit schematic and the layout of the implemented HV ESD protection circuit [48].

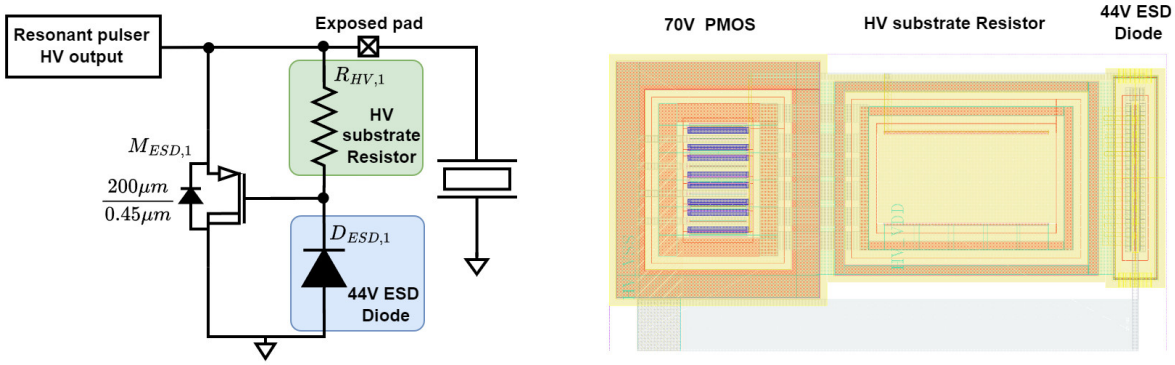

Figure 4.2: Circuit schematic and layout of the HV ESD protection circuit.

The circuit uses a custom $44V$ ESD diode together with an HV resistor of $3.3k\Omega$ and an HV PMOS transistor to form an ESD clamp. The HV resistor together with the capacitance associated with the ESD diode forms a high-pass filter. A very fast rising voltage will trigger the PMOS transistor in order for the high current to be dissipated instead of damaging circuitry in the core of the chip. Unfortunately, only $26V$ and $44V$ ESD diodes are available, posing a risk to the $40V$ limited HV transistors used in the design of the pulser. Also, since no simulation models are available for the ESD diode, the circuit cannot be characterized through simulation. Since the ESD clamp is directly connected to the pulser output additional parasitic capacitance from the HV PMOS transistor is added in parallel to the transducer. It increases the load impedance and hence lowers the efficiency of the pulser slightly. However, this will be negligible compared to the load capacitance which is already present in the circuit. An HV ESD clamp is also placed at the HV connection side of the inductor.

4.2. Floorplan

Figure 4.3 presents the layout floorplan for the TR ASIC. Since for the design of the ASIC in this thesis the area consumption for the prototype chip is not of great importance, an emphasis is laid on designing the pulser with minimizing risk on latch-up. All of the HV blocks are sufficiently separated from any neighboring LV electronics and ample space is left in between the different blocks in order to properly

bias the substrate as much as possible. furthermore, all separate LV design blocks are shielded with biased guard rings to minimize latch-up-related issues.

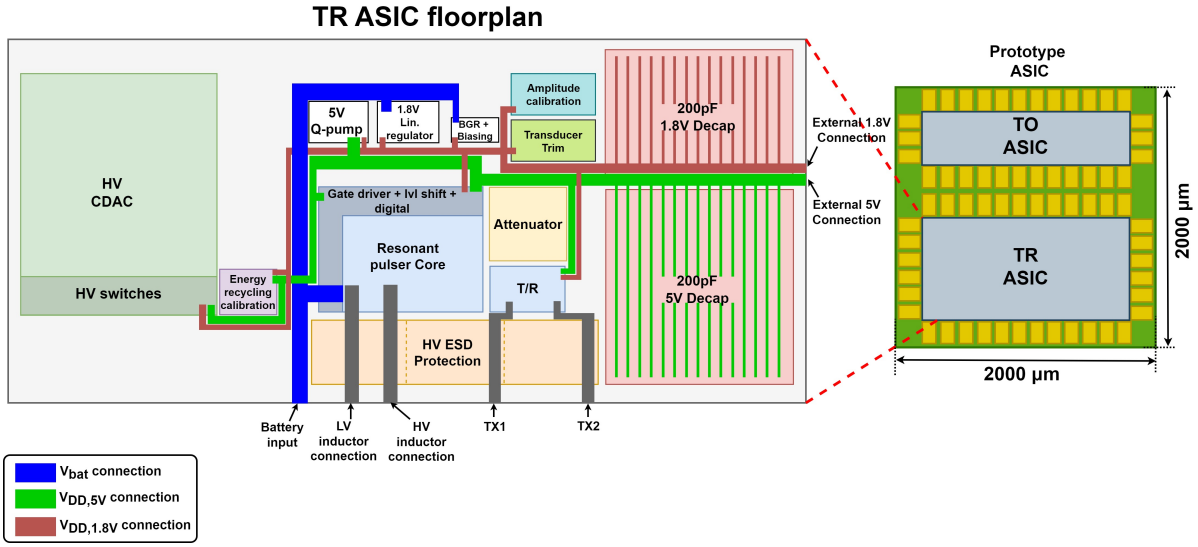

Figure 4.3: ASIC floorplan for the resonant pulser TR ASIC.

The placing of the different blocks is done so that crossings of the different supply lines are minimized. In cases where long and wide metal connections are used to connect for example the input battery supply, proper ground planes are run underneath or next to the supply line in order to minimize ground loops and act as additional shielding.

A similar floorplan is also used for the TO ASIC. Some of the individual designs of the different blocks were directly reused while others were redesigned or modified in order to fit better in the residual space left on the ASIC.

A total area of 2x2mm is taped-out (including sealring), which contains the two separate ASICs with each their own padring and one single sealring. During bonding of the ASIC one of the two padrings is bonded to access either the TR or TO ASIC.

4.2.1. Layout considerations

4.2.2. Capacitive attenuator

During amplitude calibration of the transmit pulse the attenuator introduces the largest amount of error. The attenuation factor of 20 leads to a rather large gain error which gets introduced by a mismatch in the attenuator. In order to minimize this mismatch the MOM capacitors are placed in a common-centroid layout (see Figure 4.4) with dummy capacitors around the attenuator. The unit capacitors are designed with a large aspect ratio in order to reduce any fringing effects. The lengths of the metal fingers are $24\mu m$ and each capacitor consists of 10 fingers. Post-layout simulations show that the attenuator non-linearity is kept almost the same only now the attenuation ratio is shifted by 1.56%. This corresponds to an error of approximately $20mV$ which exceeds the total error budget. This error is due to the fact that parasitic capacitances associated with capacitors $C_{d0,1}$ and $C_{d,02}$ contribute capacitance to ground, resulting in a slightly higher attenuation ratio. In order to alleviate this problem the layout needed to balance out the parasitic capacitances better, Figure 4.4 shows the improved layout implementation of the attenuator.

Instead of using the first 5 metal layers to create the MOM capacitors, the first metal layer acts as a large shielding layer which is connected for the capacitors $C_{d0,1}$ and $C_{d0,2}$ to its top plate, i.e. the pulser output node. Also, a polysilicon layer is added to reduce parasitic capacitance from the attenuator to ground. In this way, the contribution of the resulting parasitics is balanced out. In order to more finely tune the attenuation ratio the unit capacitor is made twice shorter in length, trading in an increase in mismatch in order to achieve better overall performance. Finally, a p-type substrate guard ring is added around the attenuator since it resides close to the HV circuitry. The post-layout results are shown in Table 4.1. As expected the resulting mismatch-induced gain error is slightly higher for

the $30V$ pulse. However, the resulting non-linearity in the attenuation ratio is even better compared to schematic simulation results due to the balancing of the parasitics that has been performed.

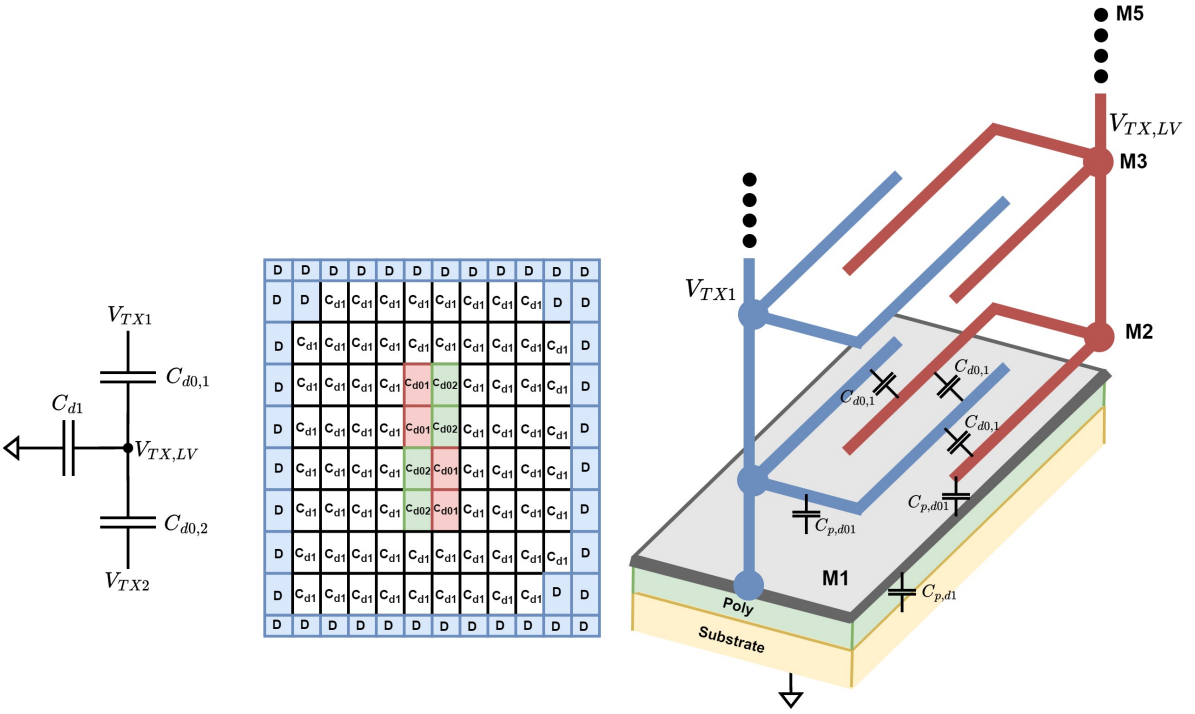

Figure 4.4: Common centroid layout of the attenuator and implemented shielding layer to increase the linearity of the attenuator.

Table 4.1: Post-layout simulated performance of the attenuator

	Schematic	Post layout
attenuation ratio β non-linearity $\frac{\beta(30V)-\beta(10V)}{\beta(10V)}$ [%]	0.550	0.186
$\pm 3\sigma V_\epsilon$ (30V) [mV]	4.12	4.25
$\pm 3\sigma V_\epsilon$ (10V) [mV]	1.42	1.38

4.2.3. Gate driver and HV transistor layout

During the layout design of HV and high current devices one must pay attention to proper sizing of the device structure and its interconnect in order to avoid large voltage drops and other reliability-related concerns associated with these circuits. The gate drivers used in the core of the resonant pulser that directly drive the HV devices are relatively large, and their associated current drive is also relatively large and even contributes to a large part of the power consumption in case low voltage pulses are generated. Figure 4.5 shows the layout of a single stage of a gate driver with its source and drain connections. The gates of these gate drivers are connected similarly on the second metal layer. The aspect ratio of the NMOS and PMOS and hence its total poly length and number of fingers is set between 1:2 and 1:3. This is done in order for the total resistance introduced by the length and high sheet resistance of the poly not to dominate the delay of activating the gate of the transistor. The width of the main interconnect W_{M1} is chosen such that $R_{M1} \leq \frac{R_{on,PMOS}}{10}$. The aspect ratio of the entire gate driver is chosen such that somewhat fixed height is obtained which helps which the supply and bulk connections. Additionally, since high currents are flowing, the effects due to electron migration are also considered. As a rule of thumb (taken from the technology PDK) the maximum amount of current flowing through a metal (except the top metal) should be limited to $1\mu m/mA$. Considering a maximum pulse amplitude of $30V$ we obtain $\frac{30V}{R_m}/\sqrt{2} = 13mA_{\text{rms}}$, however since we pulse at $2.5MHz$ with a PRF below $10kHz$ it is acceptable to take the minimum interconnect size for the HV devices between

$5 - 10\mu m$.

An example for sizing the layout interconnect of one of the gate drivers:
Considering the R_{on} of a PMOS to be 8.15Ω, $W_p = 20.9\mu m$, $L_p = 9.38\mu m$, with $R_{\square,M1} = 0.08$ and $R_{\square,poly} = 0.4$. The PMOS has a poly length of $500nm$ with 40 fingers, resulting in an effective poly width of $40{\cdot}0.05 = 20\mu m$. $R_{gate} = \frac{9.38}{20}{\cdot}40 = 0.19\Omega$. In order to obtain W_{M1} we calculate $\frac{R_{on,PMOS}}{10} = 0.08{\cdot}\frac{20.9}{W_{M1}}$ from this we obtain $W_{M1} \geq 2.05\mu m$

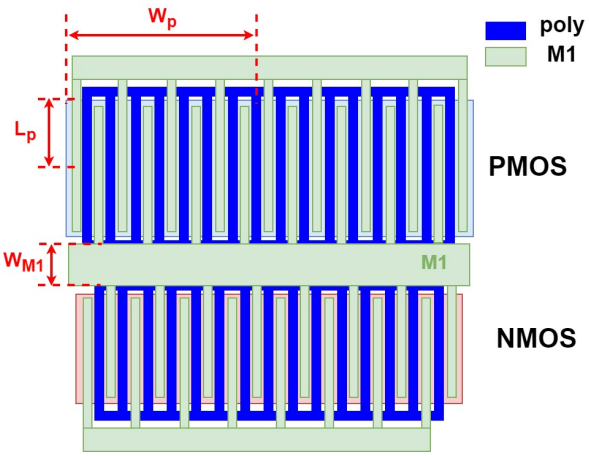

Figure 4.5: Example layout of a single stage from a gate driver.

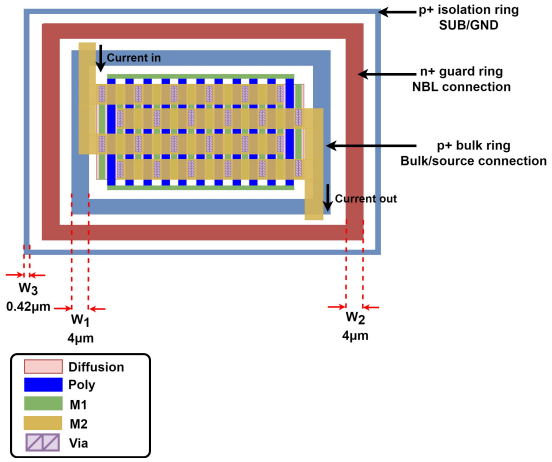

Figure 4.6: Layout and interconnect of an HV transistor.

Figure 4.6 shows an example of the implemented layout and interconnect of an HV device. The device is laid out such that the input and output path of the current sees roughly the same resistance, resulting in the current being distributed equally across the transistor. Furthermore, the p+ bulk ring and n+ guard ring are sized in order to properly sustain voltages up to $40V$ without risking latch-up. The n+ guard ring which connects to the NBL layer underneath the transistor is connected to the drain of the HV NMOS transistors (that being the highest potential available at its terminals). While the bulk ring (which is also connected to its source terminal) and p+ isolation ring are grounded. The p+ isolation ring is sized at its minimum width of $420nm$. This is done since all the HV devices are grouped together and additional rings and trenches for substrate connections around the HV area are placed in order to firmly fix the substrate potential to ground. All source and drain fingers are spaced so that at least 2 rows of contacts are formed which helps with reducing the contact resistance.

4.2.4. HV CDAC

The HV CDAC occupies the largest area on the ASIC since it requires to add a substantial amount of capacitance during trimming. The MOM capacitors occupy all 5 metal layers and are placed close to their HV switches which are shielded properly from the rest of the ASIC. Since the trimming operation is vital to the functionality of the pulser, the resulting parasitics and mismatch could cause problems during the trim operation. Figure 4.7 shows the implemented CDAC layout. In order to reduce mismatch, the MOM capacitors are laid out in a twisted common centroid layout, which only requires 3 metal layers for interconnect. Additional dummy capacitors are placed around the CDAC together with a wide substrate guard ring.

Figure 4.8 presents the post-layout simulation results on the HV CDAC linearity. It shows, as expected worse peak DNL and a slightly higher offset across the entire DAC range. This is simply explained by the additional parasitic capacitances after layout. The slight increase in resulting ΔT across the entire DAC range is acceptable, since the resulting range in adjustable pulse width is still well within the expected variation in resonance frequency due to variations in C_p and L. The higher peak DNL of 1.13, on the other hand could be problematic since the resulting time step could lead to a situation where the resulting resonance frequency is too short in case the largest transmit pulse is sent. By means of performing the same rigorous simulations as performed during the schematic design the performance of the trim operation is verified to still be well within requirements.

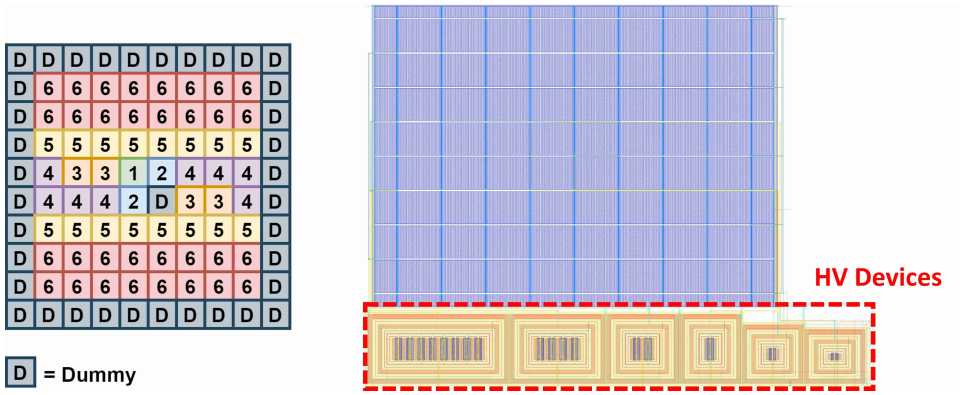

Figure 4.7: Twisted common centroid layout of the HV CDAC and layout of the CDAC with the required HV switches.

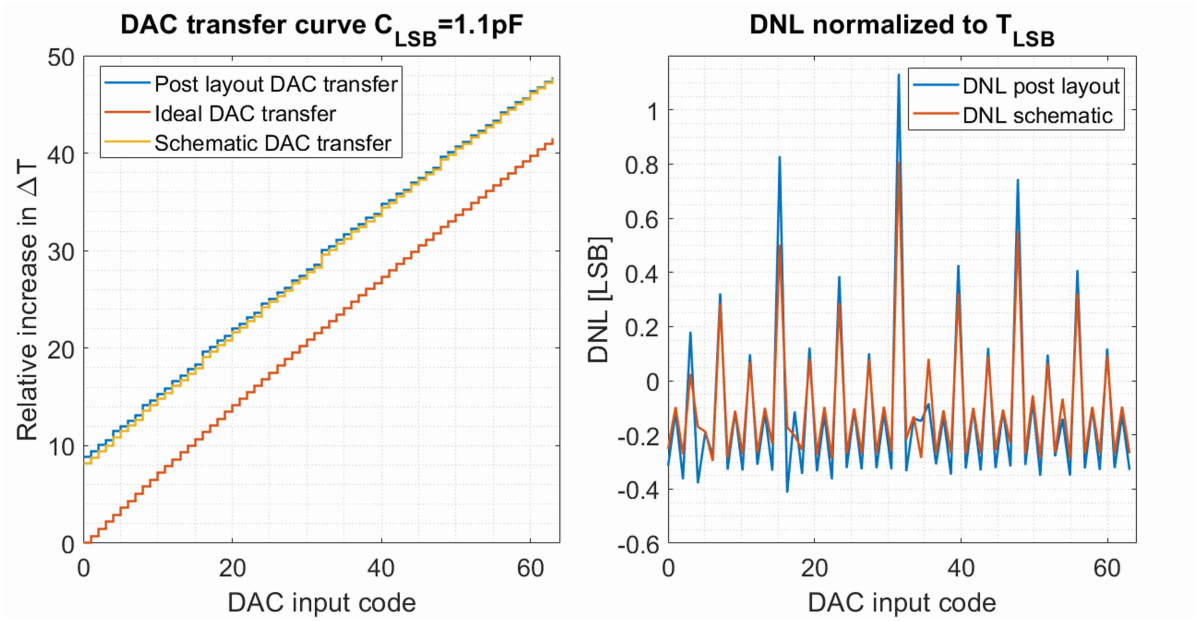

Figure 4.8: Post-layout simulation results of the HV CDAC linearity, (left) DAC transfer curve and (right) DAC DNL.

4.3. Padring and IO layout

For the ASIC two separate padrings surround the TR and TO ASICs totaling 57 and 47 pads respectively. Many of these pads connect to digital IO cells while others connect to different types of supply and ground cells. Since the number of pads that could be fitted exceeded the available 2x2mm chip area the ground pads were placed inside of the padring. Due to the size and pitch of the pads being larger than the pitch of the IO cells enough space could be created to fit enough ground pads on each of the ASICs. Furthermore, the padring was modified such that the padring supply and post-driver supply were separated from each other. This was done since the padring was required to operate at $5V$ while keeping the IO core voltage at $1.8V$. The input battery supply pad, and the pad connecting the low voltage side of the inductor swing between ground and $3.6V$ and $5V$ respectively.

Digital drivers were inserted at each of the digital IO cells in order to properly drive the signals to the ASIC core. Since a relatively large distance had to be bridged additional islands of digital drivers were also placed inside of the ASIC. In order to create a proper clock distribution for the flip-flops used to synchronize all digital signals on the ASIC, a simple clock three and clock driver was created to distribute the clock alongside the padring.

The ASIC layout and padring were designed such that all analog and high current paths are connected to one side of the padring and are placed closest to the ASIC core compared to the other pads. Two wide top metal ring surrounds the inside periphery of the padring to supply the padring core IO

voltage of $1.8V$ and all ground connections. Figure 4.9 shows the layout of the designed padrings for the resonant pulser ASICs.

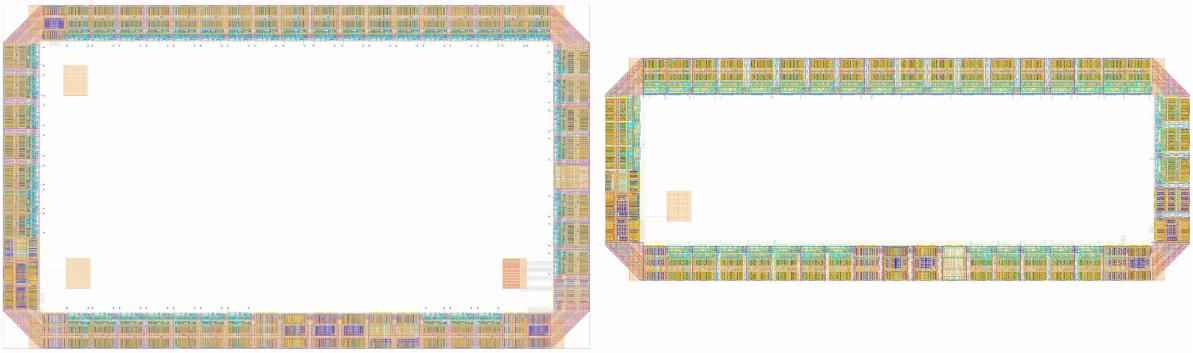

Figure 4.9: Layout image of the padring design for the TR (left) and TO (right) ASICs.

4.4. Final ASIC layout

The final layout and dimensions of the ASIC are shown in Figure 4.10.

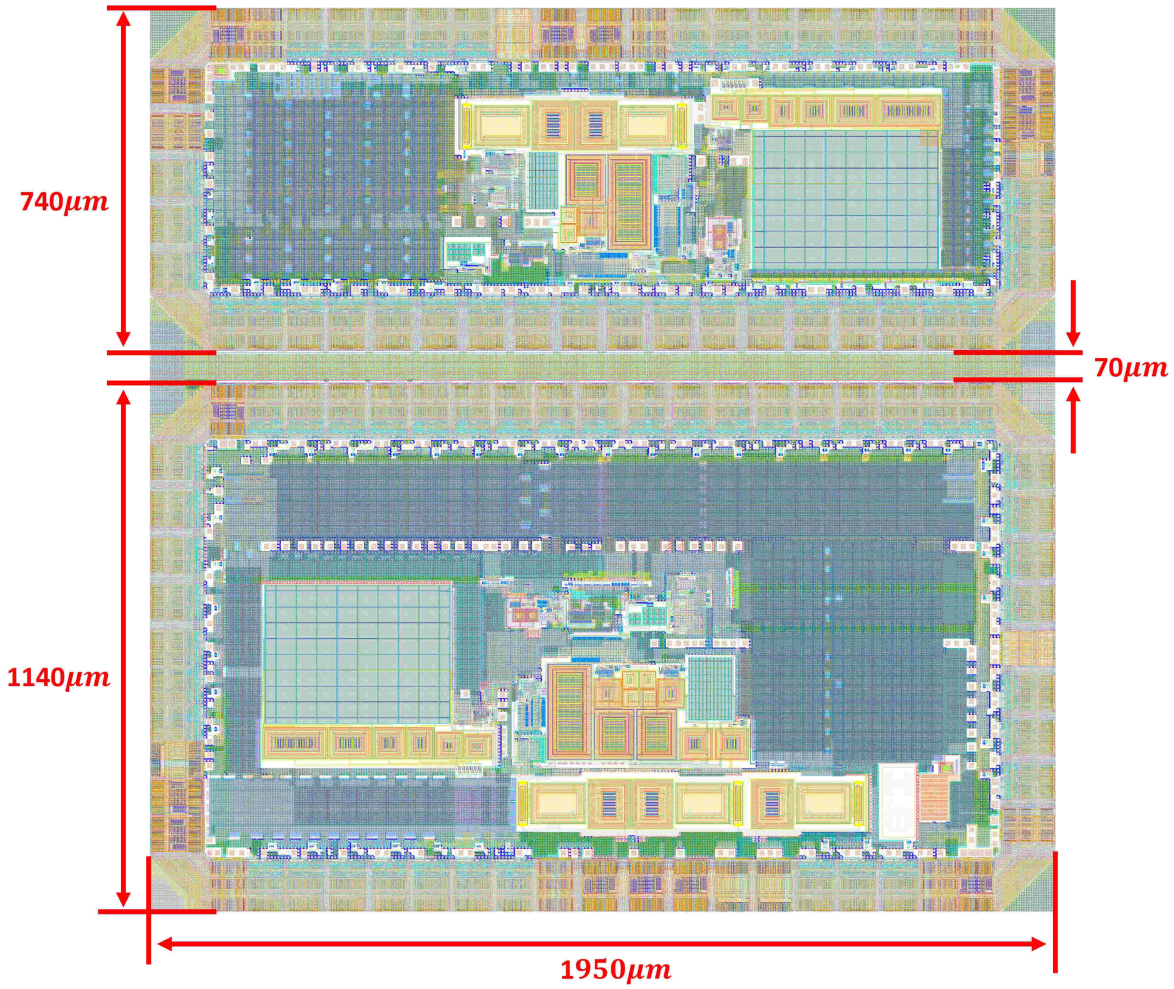

Figure 4.10: Layout of the complete resonant pulser ASIC, showing both the TR (bottom) and TO (top) ASIC and their dimensions.

Figure 4.11 presents an overview of the circuit block placement in the layout of both ASICs. A micrograph of the fabricated ASIC is shown in Figure 4.12 together with the approximate dimensions of the active occupied area of both ASICs.

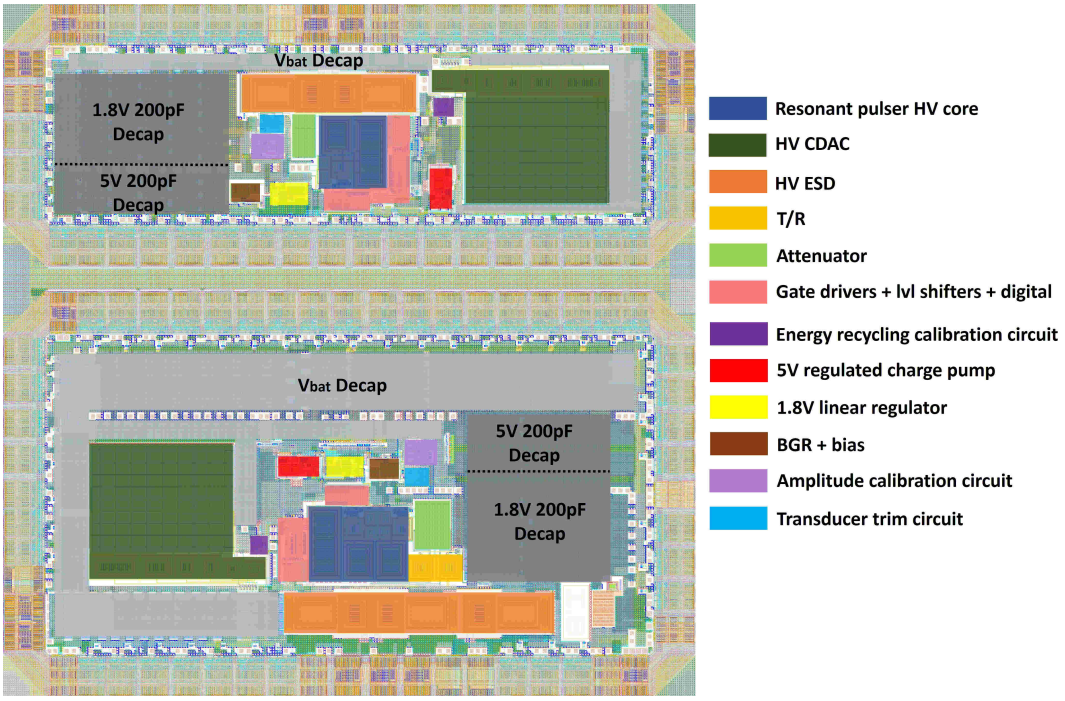

Figure 4.11: ASIC layout overview of the different circuit block placements.

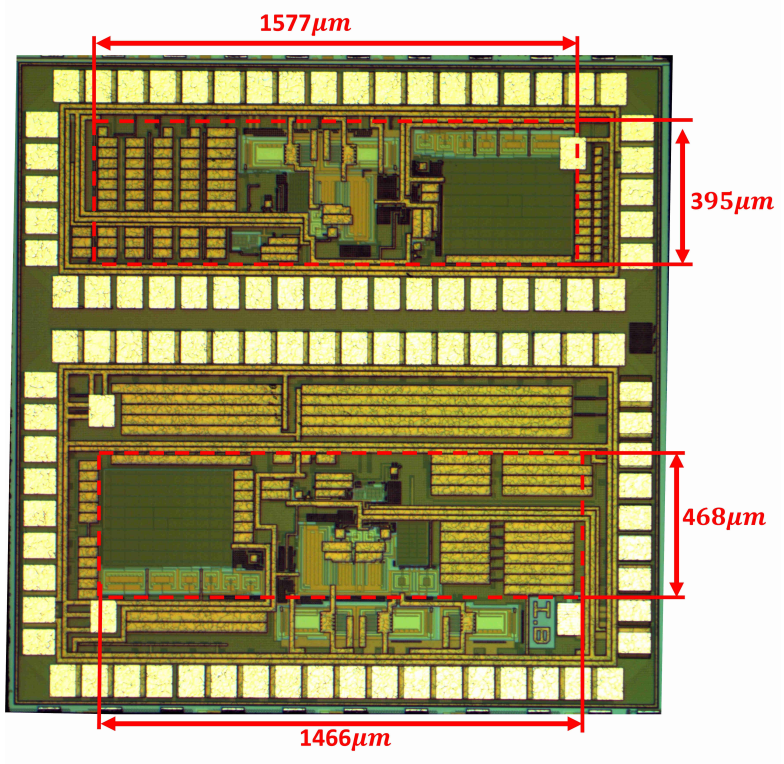

Figure 4.12: Chip micrograph of the fabricated resonant pulser ASIC.

4.5. Post-layout simulations

After validating each block of the resonant pulser by post-layout simulation, the power efficiency of the system has been determined. The padring, digital drivers, flip flops, and clock driver are connected with the padring IO core supply and hence do not contribute to the ASIC power consumption. The following simulation results use an ideal inductor model, $L = 29\mu H$ connected to the TR ASIC. This inductor value corresponds to the maximum allowable value, meaning that the HV CDAC does not need to add any additional capacitance in order to match the resonance frequency. Besides simulating the ASIC connected to the CMUT BVD model also ideal $120pF$ capacitors are simulated. These conditions lead to the highest achievable efficiency.

Figure 4.13 presents the simulated ASIC power consumption as a function of varying TX voltage. The TR ASIC is able to achieve a peak efficiency of $0.15fCV^2$ in case ideal capacitors are connected to the pulser. From the analysis performed on the energy dissipation in the CMUT transducer in the previous chapter, the additional acoustic dissipation in the CMUT transducer decreases the efficiency in terms of the amount of power dissipated from the input battery supply. However, even considering the CMUT transducer a peak efficiency of $0.43fCV^2$ is reached.

Figure 4.14 shows the simulated power efficiency as a function of the input battery voltage. The resonant pulser consumes slightly less power at higher input voltages as expected. Between $3.3V - 3.9V$ the resonant pulser average power consumption varies only by $\approx 0.02fCV^2$.

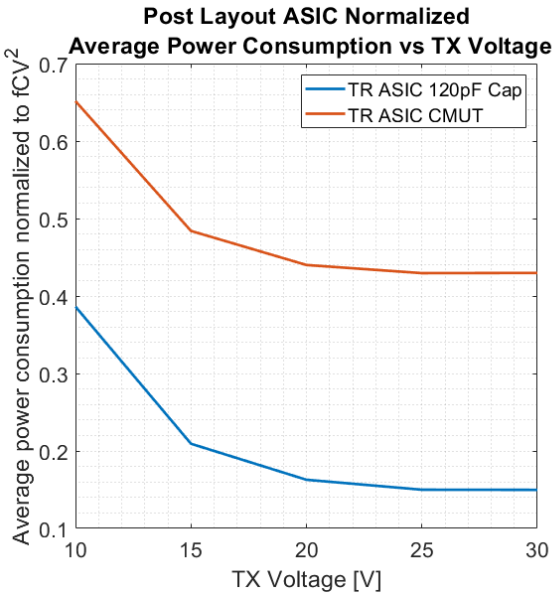

Figure 4.13: Post layout total ASIC average power consumption vs TX voltage, TT corner, $T = 27°C$, $V_{bat} = 3.6V$, $f_{PRF} = 400kHz$, maximum L, and CDAC = 0.

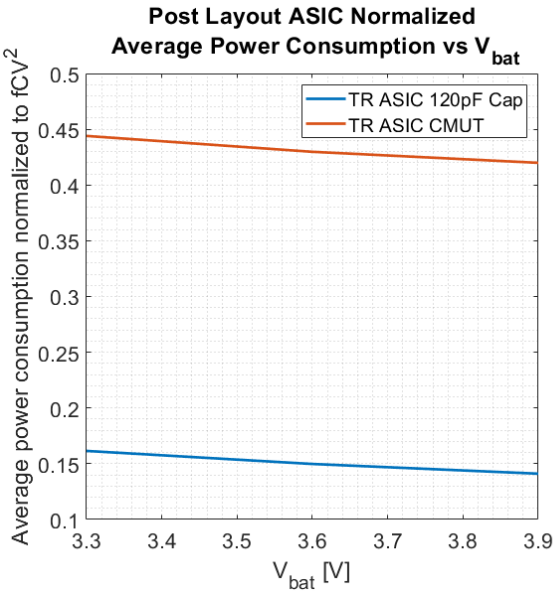

Figure 4.14: Post layout total ASIC average power consumption vs V_{bat}, TT corner, $T = 27°C$, $V_{TX} = 30V$, $f_{PRF} = 400kHz$, maximum L, and CDAC = 0.

Figures 4.15 and 4.16 present the average power consumption against PVT variation. Across process corners the efficiency of the resonant pulser varies considerably at the FS and SS corners. Due to both larger R_{on} (and thus a much larger charging time and less efficient energy recycling), higher gate drive losses, and additional parasitics at the output of the pulser, the efficiency becomes considerably worse. At the other end in the FF corner, the efficiency only increases slightly. The performance across process corners could have been better balanced out by resizing the core of the resonant pulser accordingly. For the prototype, a fabricated wafer close to TT corner was considered hence optimizing the pulser specifically at that corner would most likely result in the highest measured efficiency during chip measurements.

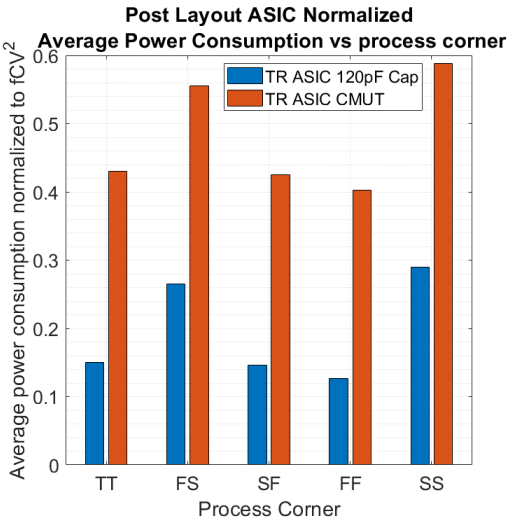

Figure 4.15: Post layout total ASIC average power consumption vs process corner, $V_{bat} = 3.6V$, $T = 27°C$, $V_{TX} = 30V$, $f_{PRF} = 400kHz$, maximum L, and CDAC = 0.

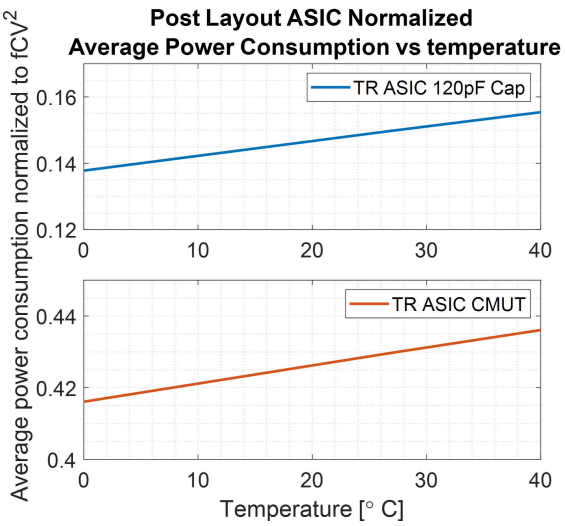

Figure 4.16: Post layout total ASIC average power consumption vs temperature, $V_{bat} = 3.6V$, TT corner, $V_{TX} = 30V$, $f_{PRF} = 400kHz$, maximum L, and CDAC = 0.

Figure 4.17 presents the efficiency of the pulser against varying inductor non-ideality. Variations in the self-resonance frequency of the inductor show, as expected, that the efficiency increases for higher f_{SRF} compared to the pulse frequency. The resulting decrease in efficiency due to the inductor DC resistance shows to be approximately linear for the $30V$ pulse.

Finally, the decrease in energy efficiency due to the trim operation is investigated. By varying the size of the inductor and obtaining the appropriate CDAC settings after the trim operation, the average power consumption is simulated for a calibrated $30V$ pulse. Figure 4.18 shows the simulation results. As expected, the approximately linear increase in power dissipation for smaller L is due to both the larger load being charged and a higher peak charging current flowing through the inductor.

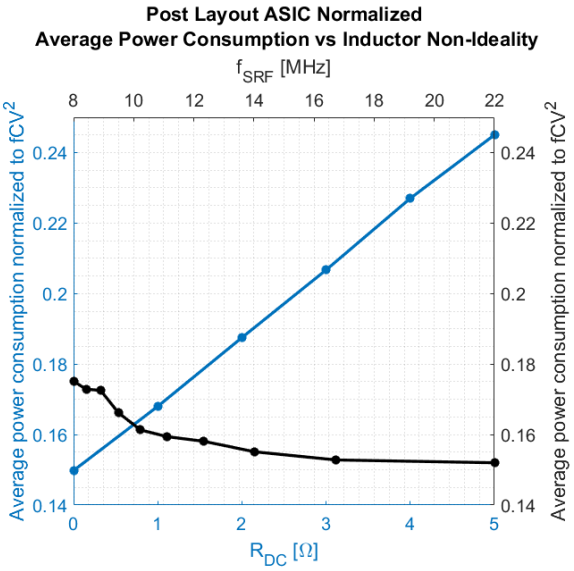

Figure 4.17: Post layout total ASIC average power consumption with an ideal $120pF$ load capacitor vs inductor DC resistance R_{DC} and inductor self resonance frequency f_{SRF}, $V_{bat} = 3.6V$, TT corner, $V_{TX} = 30V$, $f_{PRF} = 400kHz$, $L = 29\mu H$, and CDAC = 0.

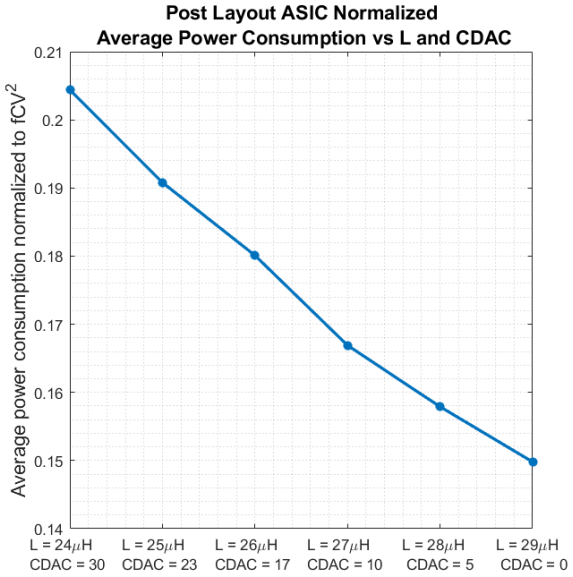

Figure 4.18: Post layout total ASIC average power consumption with an ideal $120pF$ load capacitor for varying L and corresponding CDAC decimal output code after trim,$V_{bat} = 3.6V$, TT corner, $V_{TX} = 30V$, $f_{PRF} = 400kHz$.

5

Measurements

This chapter describes the measurement setup and measurement results of the resonant pulser ASIC. Design considerations for the measurement board are presented together with an overview of the designed test setup. Electrical measurements were performed on both CMUT transducer's and capacitors in order to characterize the ASIC. Also, acoustic measurements were performed using the CMUT transducer's in both transmit and pulse-echo configurations.

5.1. Measurement setup

Figure 5.1 presents a block diagram of the measurement setup. The main measurement board is driven by an FPGA providing all required control signals for the ASIC to function. The measurement board contains sockets for both the TR and TO ASICs, one of which is connected to the measurement board at a time.

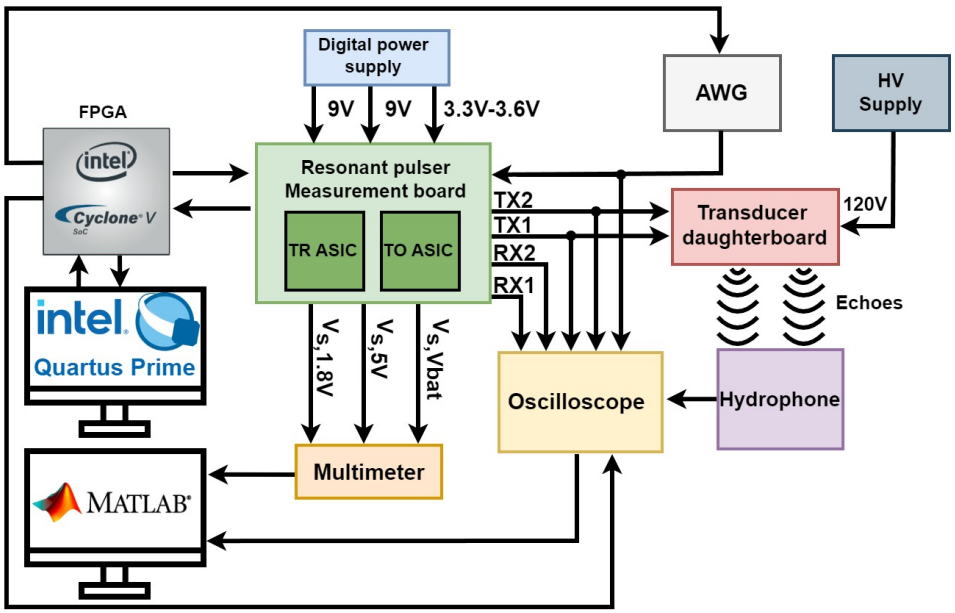

Figure 5.1: Schematic diagram of the resonant pulser measurement setup..

The measurement board is powered by a power supply providing a $9V$ input voltage used to power everything on the measurement board except the battery input for the ASIC, this is a separate DC input provided from the power supply. A multimeter is used to measure the power efficiency of the ASIC and an oscilloscope is used to obtain all the waveforms of interest. The measurement board interfaces with a transducer daughterboard where either the CMUTs transducer's, capacitors, or a PZT element can

be connected to the ASIC output. In order to perform transmit measurements, a hydrophone is used inside a water bag in order to record the pressure waves. Additionally, an external HV pulse (generated by an arbitrary waveform generator) can be used to send pulses to the transducer's in order to perform a comparison between the half-sine wave excitation of the resonant pulser and a comparable external HV pulse.

5.2. Measurement PCB

Figure 5.2 presents a simplified schematic diagram of the measurement board. The FPGA signals need to be level shifted from $3.3V$ to $5V$ in order to interface with the ASICs padring. The FPGA provides three trigger outputs that are used to trigger the oscilloscope and AWG. By means of 10 switches, parameters like transmit pulse amplitude, operating mode, transducer type, and trim offset voltage can be set. A set of 4 push buttons is used to control the operation during pulsing, and a set of 16 LEDs is used to act as a simple debug tool for the FPGA.

The board uses linear regulators in order to obtain all the required supply voltages on the board. The battery input voltage of the ASIC is fed in directly from the DC supply and by means of using a 56Ω current sense resistor (R_s) the current consumption is measured. An identical current sense resistor is used on the two regulator outputs that provide the optional external $1.8V$ and $5V$ supply voltages for the ASIC core to measure the total ASIC power consumption.

The inductor used during measurements is the SRR1240-270M, which is a power inductor characterized as $27\mu H \pm 20\%$, $R_{DC,max} = 85m\Omega$, $I_{sat} = 2.25A$ and $f_{SRF} = 15.5MHz$. The inductor has a relatively small footprint (12.5mm x 12.5mm x 4mm) compared with comparable commercially available alternatives. However, inductors as small as a 0806 (imperial) package are also available which would also be usable for the resonant pulser. The LQH2MCN270K02L is characterized as $27\mu H \pm 10\%$, $R_{DC,max} = 3.25\Omega$, $I_{sat} = 180mA$ and $f_{SRF} = 30MHz$. The much smaller package does make a clear trade-off with the much higher DC resistance of the inductor, making it a less attractive option considering it will dominate over the transistors R_{on} in the resonant pulser.

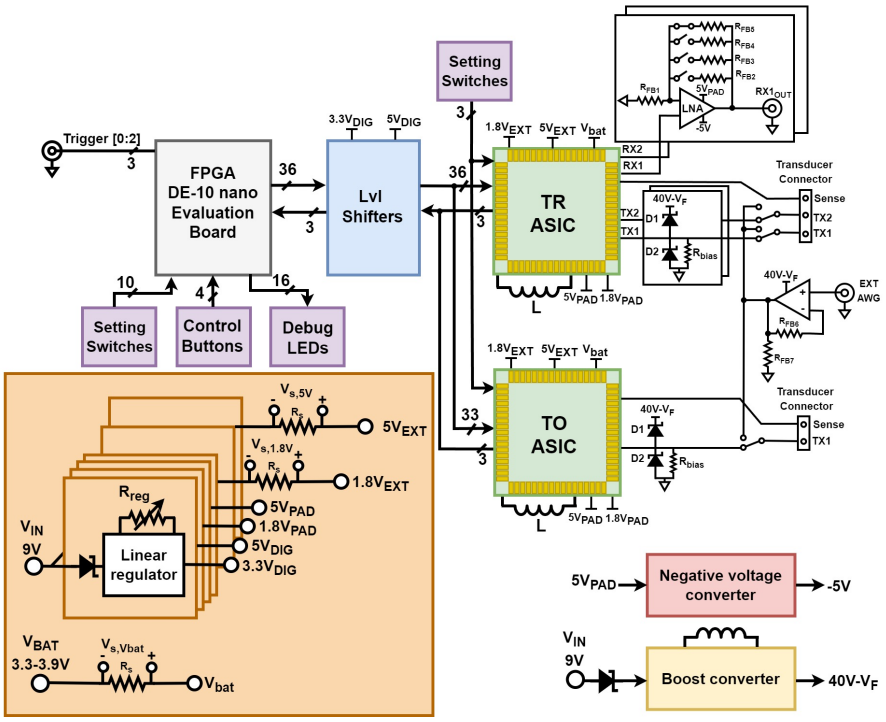

Figure 5.2: Simplified schematic diagram of the resonant pulser measurement board.

A situation could occur in which the transducer's (or capacitors) are not correctly connected to the ASIC or in case a bug occurs in the FPGA code for the timing of the switching of the resonant pulser core, leading to a much higher voltage than $40V$ being created on the HV output node(s) of the resonant pulser. A diode clamp consisting of diodes D_1 and D_2 (see Figure 5.2) is placed on the

ASICs transducer output nodes limiting the output to $[-V_F, 40V - V_F]$ (where V_F is the forward voltage of the diode). Since the diodes are placed in parallel to the transducer their junction capacitance has to be low. Special high-voltage low-capacitance Schottky diodes are used that offer very low junction capacitance ($\approx 0.45pF$). Finally, an HV opamp is used in order to amplify an external pulse from an AWG to a $30V$ pulse in order to perform a comparison between the resonant pulser and an external pulse.

For the TR ASIC, LNAs are used to amplify the received echoes from the CMUT transducer's. The amplifier gain can be set to 5, 10, 15, and 20. The Schottky diodes have a rated leakage current of $10nA$ which could result in parasitic charging of the transducer's C_p in case of any imbalance in the diodes leakage current (the input bias current of the LNA also leads to this problem however this is much smaller $\approx 2pA$). Therefore, a bias resistor R_{bias} is added in parallel with diodes D_2. The resistor discharges any build-up charge on the transducer. The resistor also attenuates the received echo signals. Therefore its value is chosen much higher than R_m ($R_{bias} = 50k\Omega$). The noise added by the resistor gets filtered by the transducer capacitance, hence not increasing the received echoes noise floor. Figure 5.3 shows a picture of the resonant pulser measurement board.

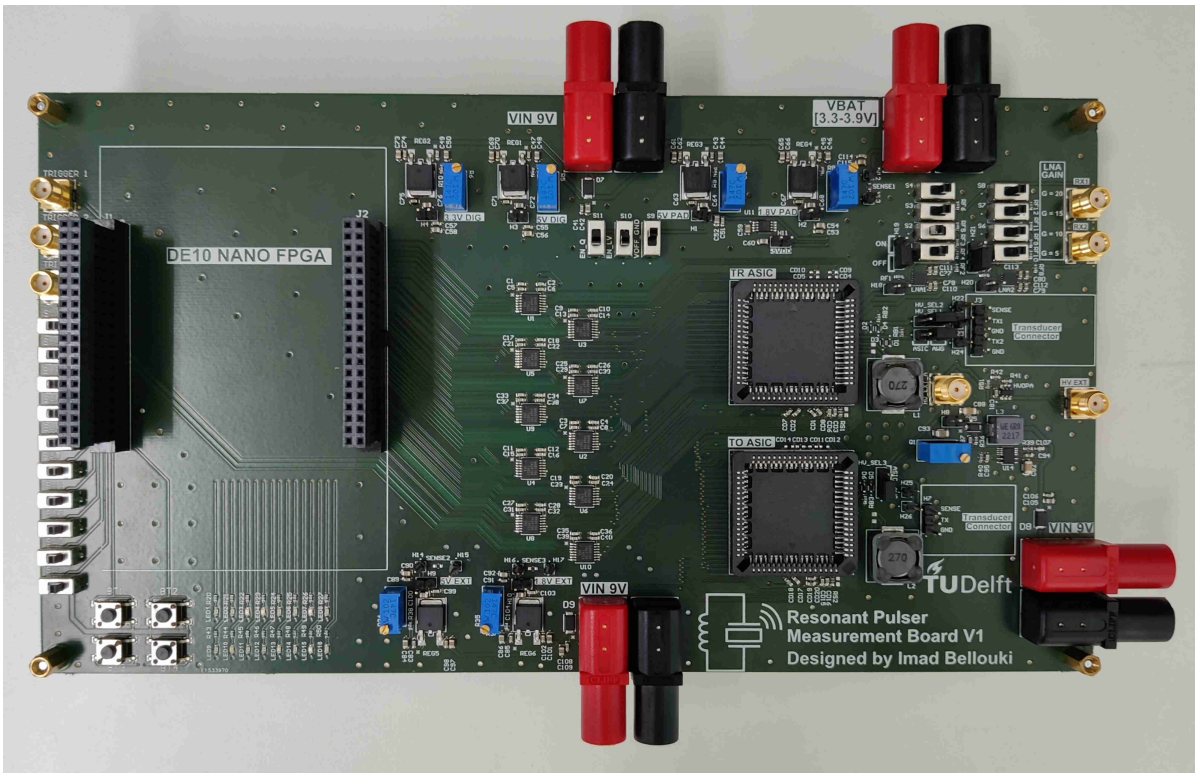

Figure 5.3: Picture of the resonant pulser measurement board.

5.3. Transducer daughterboards

5.3.1. CMUT daughterboard

The different transducer's are connected by means of connecting a daughterboard to a 4 or 5-pin header on the measurement board. Figure 5.4 shows the daughterboard to connect the CMUT transducer's to the resonant pulser ASIC. The CMUT transducer's connect via an FFC connector on the daughterboard to the flex PCB which contains the CMUT array and wires that connect to a $120V$ HV supply in order to set the CMUT bias. By means of soldering 0Ω jumpers 2 sets of elements can be selected, these being elements 2 and 63 or elements 16 and 47.

5.3.2. Capacitor daughterboard

The daughterboard that connects capacitors to the ASIC simply adds a set of up to 7 $20pF$ capacitors from which 2 can be selected by means of placing jumpers. In this way, an approximate $\pm 20\%$ variation

on the load capacitance can be created.

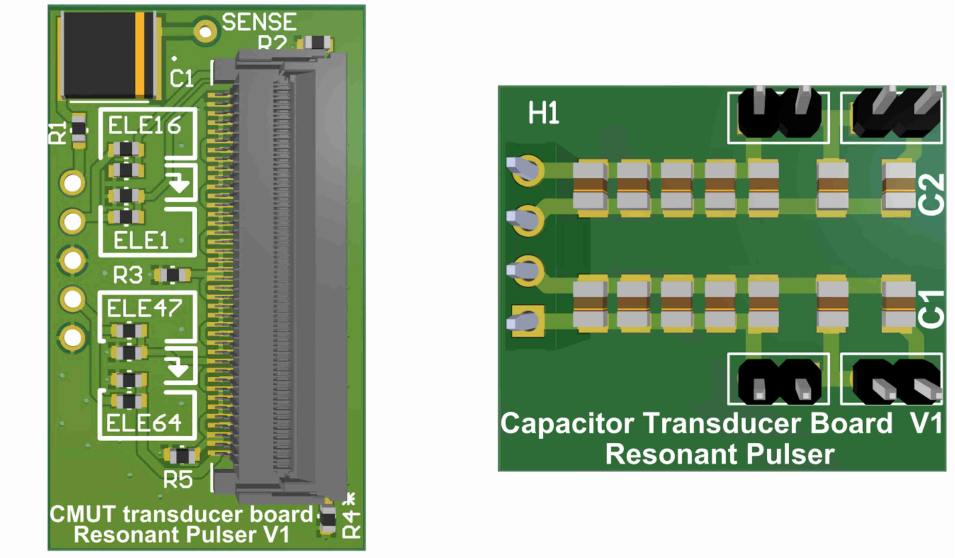

Figure 5.4: Daugterboards for connecting the CMUT transducer's (left) and capacitors (right).

5.3.3. PZT transducer

As an additional experiment, the option to test the resonant pulser using a PZT element was also considered. From prior analysis, it was already shown that the resonant pulser won't be very efficient for PZT transducer's. However, showing that the resonant pulser is at least able to generate HV pulses directly from a battery supply in that case is still a valuable experiment result. This required the design of a simple single-element PZT transducer that complies with the required capacitance and center frequency for which the resonant pulser was designed.

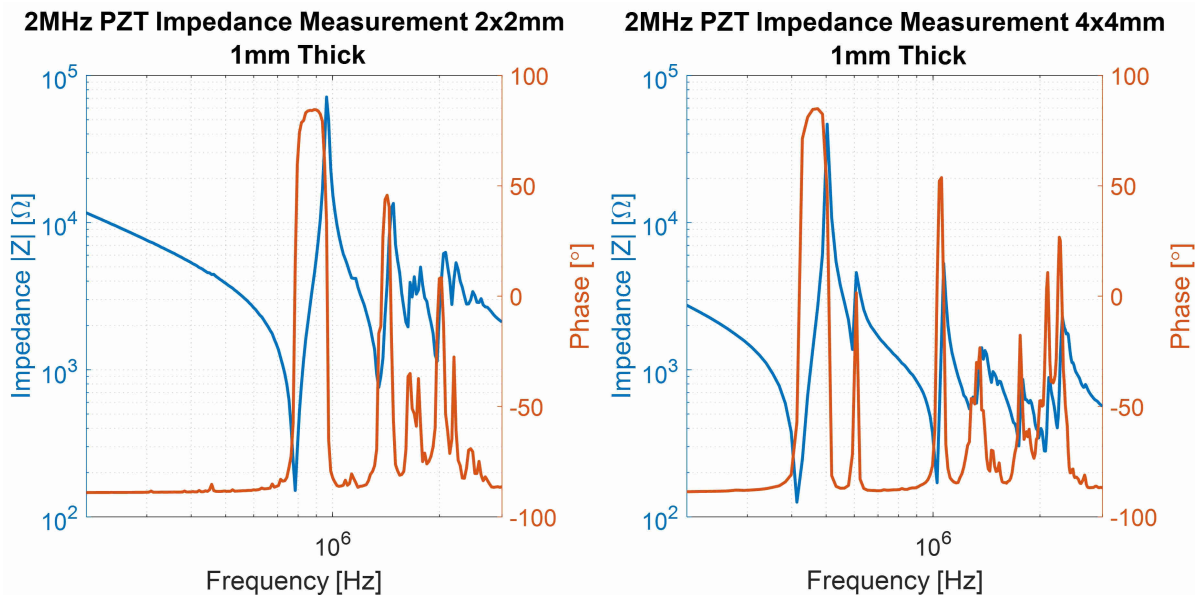

Figure 5.5: Impedance measurement results of two 1mm thick PZT samples with surface areas of 2x2mm and 4x4mm.

Figure 5.5 shows impedance measurements of two different sized PZT elements, having a surface area of 2x2mm and 4x4mm both with a thickness of 1mm. The PZT element was targeting a $2MHz$ center frequency, the measurements however show a measured series resonant frequency below $1MHz$ in both cases. This is due to the high aspect ratio (AR) of the samples resulting in the PZT not res-

onating in its thickness mode correctly. Figure 5.6 presents measurement results on resulting series resonance frequencies for varying AR and PZT thickness [49]. The results show that a PZT requires an AR ≤ 1 to properly resonate and achieve a resonance frequency only dependent on its thickness.

Investigating the measurement results shows that for a thin enough PZT element an approximate $2.5MHz$ transducer can be fabricated, by sizing a single element correctly multiple elements can be connected in parallel in order to obtain the targeted $120pF$ capacitance. For fabricating the PZT a $500\mu m$ thin PZT is available, which for AR $\approx$ 0.25-1 would result in an approximate $2.5MHz$ resonance frequency. From the impedance measurements shown in Figure 5.5 the capacitance of the transducer is derived to be $C_{p,PZT} = 70.79pF$ and $C_{p,PZT} = 141pF$ for the 2x2mm and 4x4mm PZT samples respectively. By scaling the capacitance for the $500\mu m$ PZT a design consisting of 6 elements of each being 293μm x 293μm in size yields an approximate $120pF$ $2.5MHz$ transducer with a resulting $AR = 0.59$. Figure 5.6 shows a schematic drawing for the proposed PZT transducer, the transducer can be fabricated directly on a PCB consisting of 2 solder pads where a strip of aluminum foil can be used to connect the top electrodes to the other solder pad.

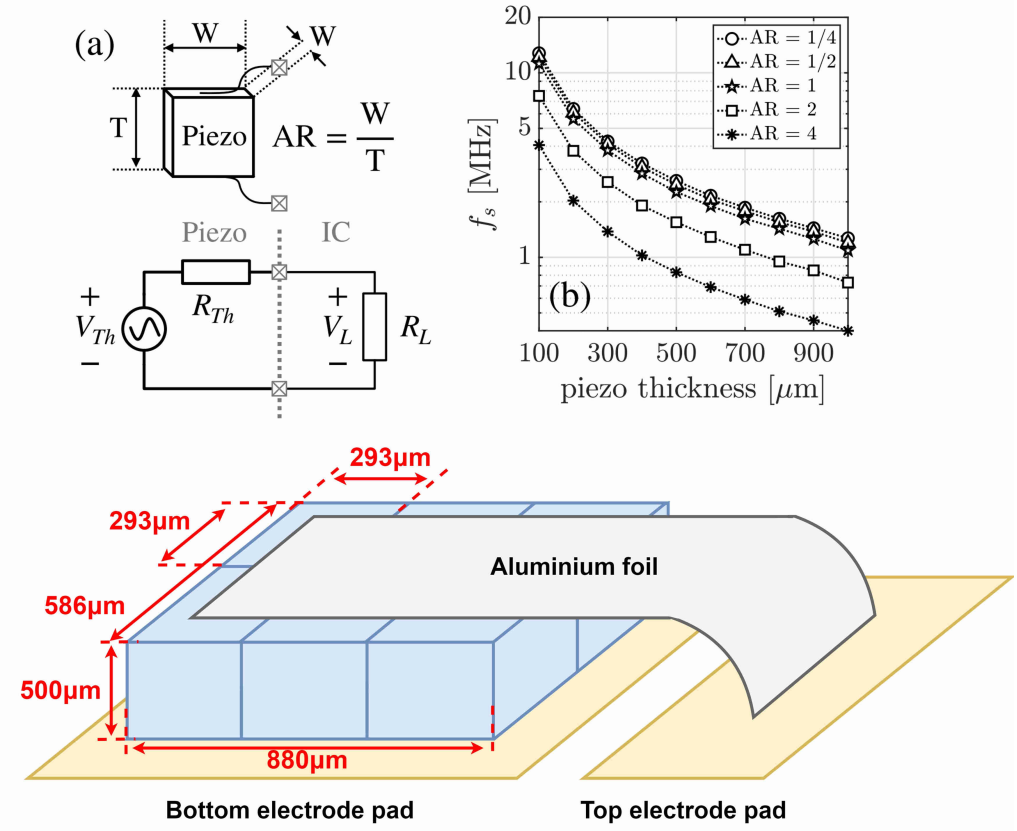

Figure 5.6: Experimental measurements results for PZT series resonance for varying AR and PZT thickness [49] (top), and schematic picture of the proposed 2.5MHz single element PZT transducer and its connections to 2 PCB solder pads (bottom).

The daughterboard PCB for the PZT element has already been fabricated however, due to time limitations the PZT element has not been fabricated and measured yet.

5.4. Electrical measurements

This section presents the electrical measurement results for the TR ASIC. After validating the measurement setup and performing the required start-up procedures, the capacitor daughterboard was attached to the ASIC and was used to perform all the electrical measurements. Figure 5.7 shows a picture of the measurement setup used to perform all electrical and acoustic measurements. When connecting the CMUT array a waterbag is placed on top of the ASIC with a layer of acoustic gel in order to better match the acoustic impedance of the water interface.

Due to the presence of quite a substantial amount of parasitic capacitance on both the measurement

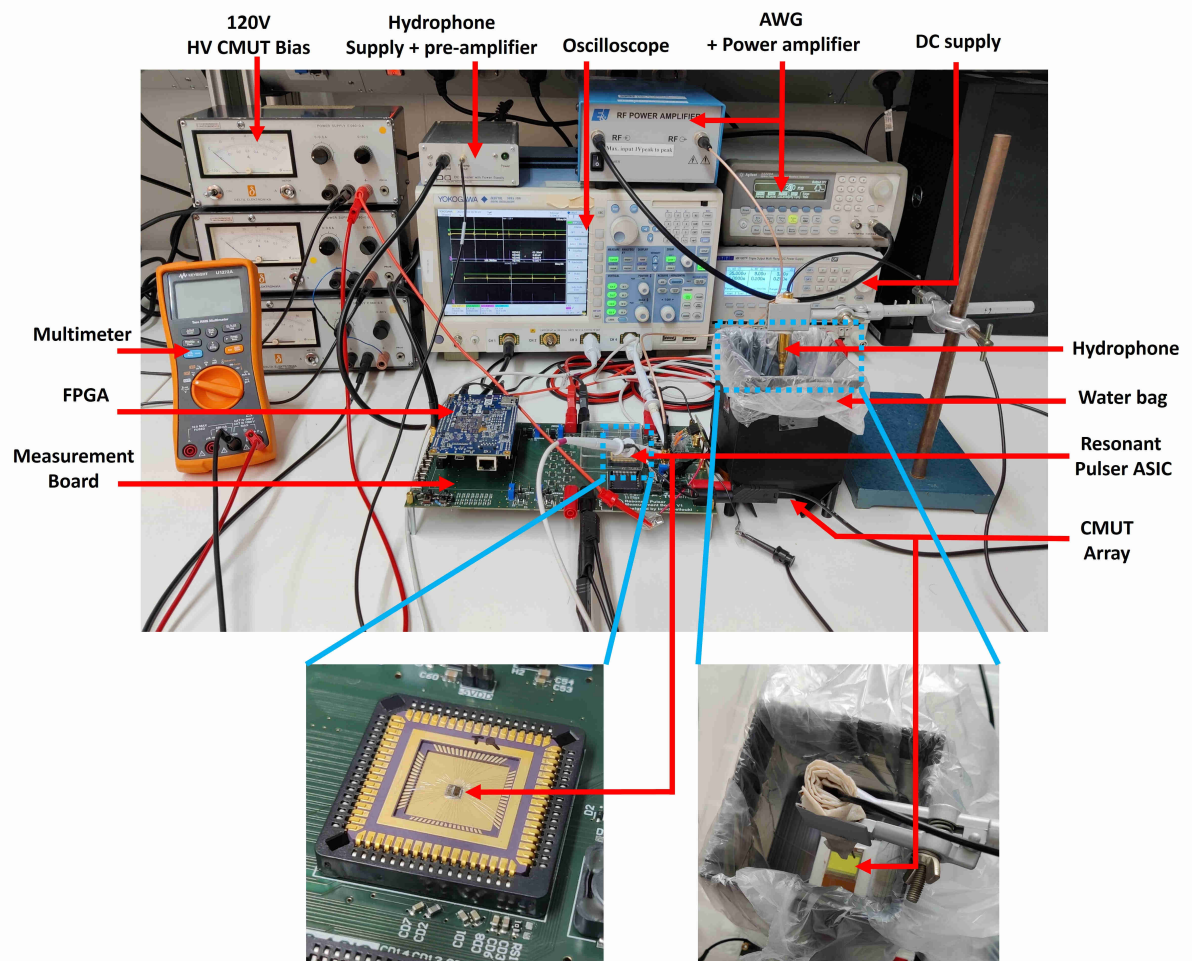

Figure 5.7: Picture of the measurement setup for performing all electrical and acoustic measurements for the resonant pulser ASIC.

board and daughterboard, some modifications had to be performed to reduce the load capacitance in order to perform the trim operation correctly (see Section 3.2.4). By setting the offset according to an input pair width of $15\mu m$, which had been determined from simulation to be sufficient for correctly trimming the transducer's, the ASIC successfully performed the transducer trim operation as shown in Figure 5.8. In 6 calibration cycles, the transmit pulse width is correctly trimmed to $200ns$ wide for an approximately $30V$ pulse. The trim calibration is correctly performed on both transmit channels automatically whereafter a 7th synchronous pulse is sent with the found trim settings in order to verify the pulse shape and resulting pulse frequency. By varying the load capacitance connected to the ASIC the functionality of the trim calibration has been verified.

After the transducer or load capacitor has been correctly trimmed the resonant pulser performs its pulse amplitude calibration, as shown in Figure 5.9. In 8 cycles, the ASIC correctly calibrates all 5 programmable amplitude levels. Inspecting the final transmit amplitude levels shows an accuracy of approximately $\leq 500mV$ except for the $25V$ pulse which has a deviation of approximately $700mV - 900mV$. From post-layout simulations, the main culprit behind the worse accuracy during amplitude calibration is the internal $1.8V$ linear regulator. It's the reduced bandwidth due to additional parasitics results in slightly worse performance during the creation of the reference voltages. By slightly altering the FPGA code to prolong the charge time of the reference voltage for the amplitude calibration by 2 additional clock cycles, better accuracy for the $25V$ pulse was obtained. However, this did worsen the accuracy on other amplitude levels slightly. Of course, other parts of the system also play a role in the resulting worse amplitude accuracy, like the accuracy from the fine-tapped delay line and comparator offset and noise. However, post-layout simulations show that the amplitude calibration accuracy stays within $400 - 450mV$ for all 5 amplitude levels (if the linear regulators worse performance is excluded).

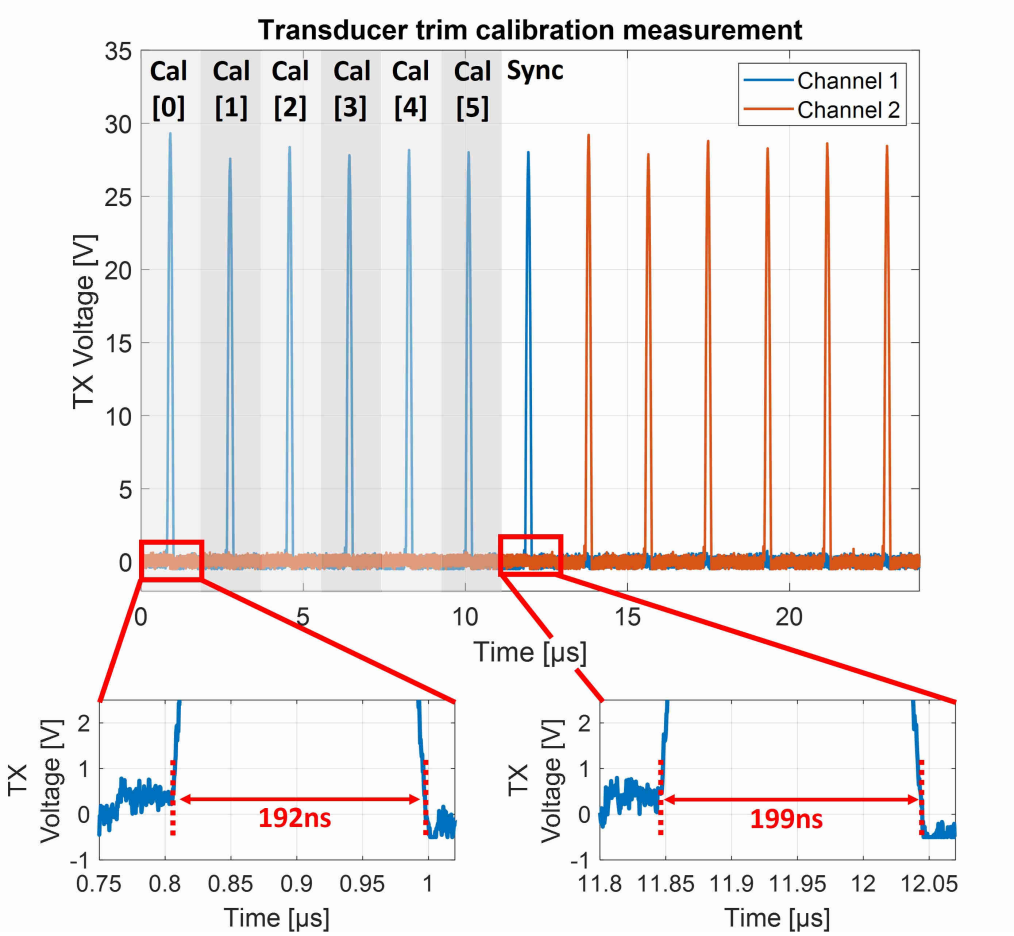

Figure 5.8: Measured transducer trim calibration with the TR ASIC with a capacitive load.

The resulting accuracy of the obtained pulse amplitude would probably still be sufficient considering both the possible large deviation in transmit efficiency from transducer to transducer and the relaxed imaging requirements on the transmit side due to the averaging nature of US imaging.

Figure 5.10 shows the regulation performance of the ASIC on its calibrated pulse amplitude against varying input battery supply. As expected there is a slight variation in calibrated TX voltage. For lower supply voltages, the performance is comparable to the nominal input supply of $3.6V$. However, at higher supply voltage the performance is worse. Currently, the main culprit behind this remains the degraded accuracy of the internal linear regulator.

Finally Figure 5.11 shows the measured average power consumption of the TR ASIC for varying TX amplitude levels. A peak efficiency of $0.37fCV^2$ is reached. The average power is normalized to fCV^2, and the capacitance for which the power was normalized was found by measuring the total capacitance at the transmit node on the measurement board. By connecting a resistor, an RC filter was created from which the total capacitance present at the output of the ASIC could be determined.

The measured efficiency is worse than expected and the peak efficiency is reached at $20V$ instead of the designed $30V$. During measurements, the required calibrated charge time for the inductor was noticeably higher than expected from post-layout simulations. And during energy recycling the required recycling time was noticeably shorter than expected. This would result in both a lower current flowing to and from the inductor, decreasing dissipation losses, and in less of the remaining energy on the CMUT being recycled back to the battery input. The former would explain the lower TX voltage at which the peak efficiency is reached (due to the lower dissipation losses). The main hypothesis of why the total energy dissipation is higher than expected is due to the non-linearity of the inductor. The inductor's non-linearity would result in an average inductance during pulsing which could be higher or lower than the expected inductance that had been measured with an RLC meter. Additional non-idealities that have not been considered during the analysis could lead to additional losses (e.g. hysteresis losses)

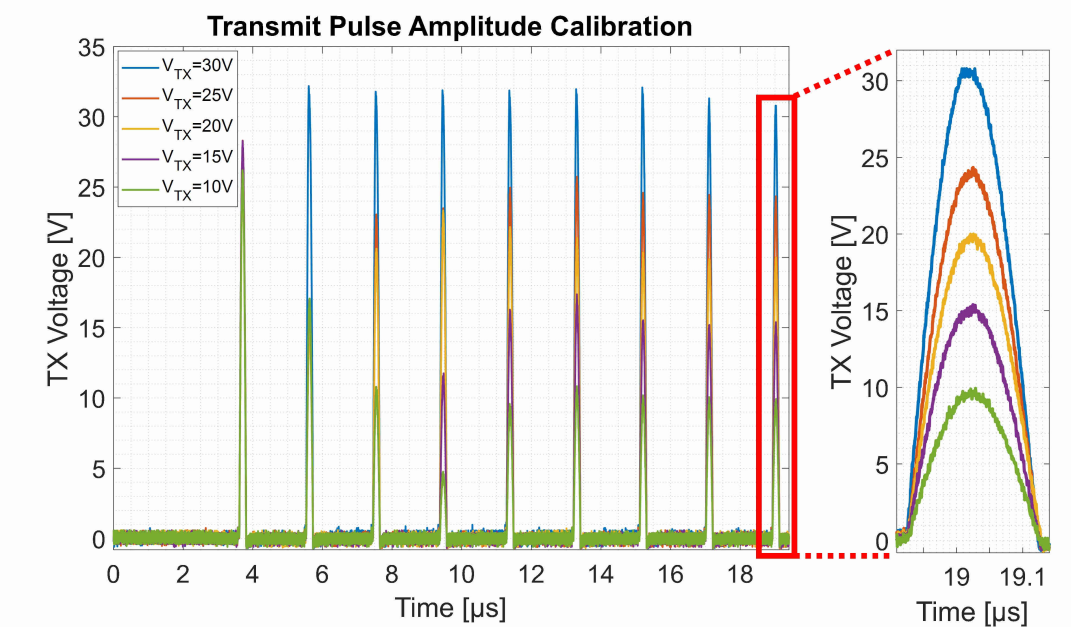

Figure 5.9: Measured transmit pulse amplitude calibration with the TR ASIC, showing calibration to all 5 programmable transmit levels.

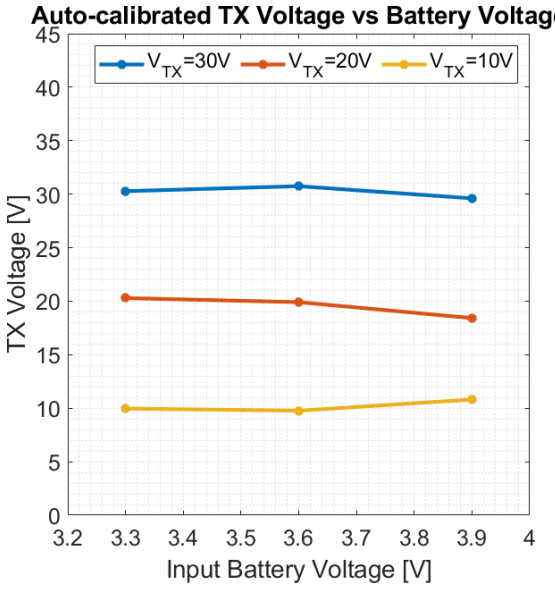

Figure 5.10: Measured transmit amplitude auto-calibration against varying battery voltage for the TR ASIC.

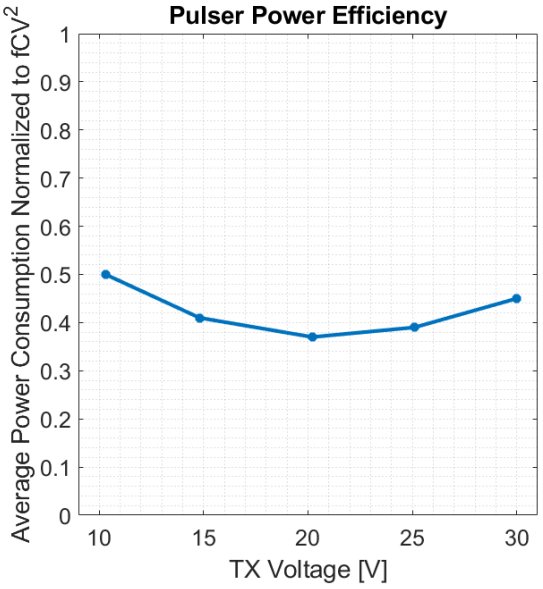

Figure 5.11: Measured TR ASIC average power efficiency for varying transmit amplitudes.

resulting in the resonant energy transfer not being perfect and the energy recycling phase being less effective. The inductor used during measurements is a power inductor with a ferrite core which could be relatively easily susceptible to additional losses (besides ohmic losses) compared with more expensive small-signal inductors designed for linearity across a larger current, voltage and frequency range (often used in applications like class-D amplifiers).

Regardless of the higher power consumption, the ASIC still performs competitively compared to state-of-the-art efficient HV pulser's with the added benefit that the HV pulse here is directly supplied from a low-voltage battery avoiding additional conversion losses. From these observations, a few conclusions can already be drawn to answer the question 'Under which circumstances does the resonant pulser become an interesting option as a building block in a US system?'. First, low-frequency puls-

ing, i.e. only a few MHz, during initial analysis it became quickly clear that the dissipation losses due to the large current that is required by the inductor dominate the energy losses in the system. The required peak current depends on the size of the transducer load, to obtain an even more efficient design ideally C_p needs to be not too large. Depending on the size of R_m and the sizing of the resonant pulser switches a large C_p can still yield an efficient design (like the one designed in this thesis) since the energy recycling process is rather efficient. Finally, the most obvious choice for implementing the resonant pulser is in cases where the transducer R_m is very large, which is the case for transducer's like CMUTs compared to PZT transducer's where R_m can often be very small (around or even below 100Ω).

5.5. Acoustic measurements

After electrical verification, the ASIC was connected to the CMUT array in order to perform both transmit measurements and pulse-echo measurements for acoustic verification of the pulser. Figure 5.12 shows the acoustic measurement setup. For the measurements the two elements that are connected to the ASIC are the 2nd and 63rd element on the 64-element CMUT array. These elements are spaced 19.2mm apart. On the array, the elements are placed side by side and have a very long length compared to their pitch, leading to a pressure wave that is very wide across the width of the transducer. By clamping a hydrophone to a stand a position where both pressure waves are detectable with the hydrophone can easily be found due to the wide beam profile of the pressure waves. The resulting approximate distances from the hydrophone to the CMUT elements are indicated in Figure 5.12.

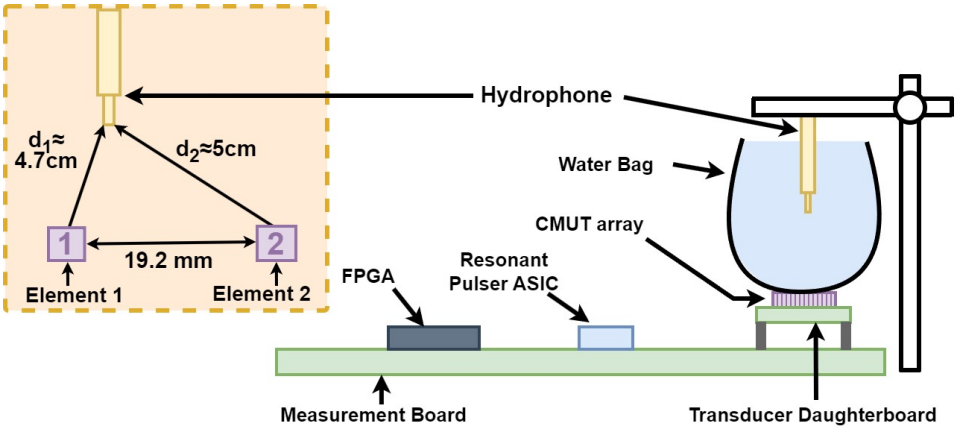

Figure 5.12: Schematic description of the acoustic measurement setup.

Figure 5.13 shows the TR ASIC transmit measurements captured by the hydrophone. On both transmit channels $30V$ pulses are generated, the resulting pressure wave is recorded by the hydrophone where the time of arrival corresponds to the measured distances from the transducer's to the hydrophone. The hydrophone is aimed to focus mainly on the 1st CMUT element, resulting in the received pulse from the 2nd element being much weaker due to the directivity of the hydrophone. At the exact time moment the HV pulse is generated a sharp peak is visible in the hydrophone received signal, which is due to electrical coupling between the measurement equipment.

In order to check whether the half sine pulses generated from the ASIC lead to any degradation in acoustic performance a measurement is performed where an external HV pulse is provided to the CMUT transducer's. Figure 5.14 shows the measurement results for the TR ASIC generating a $30V$ pulse and an external $30V$ pulse generated using an AWG. The AWG creates a $5V$ square wave which feeds into a power amplifier to amplify the pulse to $30V$. The amplifier has a limited bandwidth resulting in a droop in the amplified HV square wave. Due to the limited bandwidth of the probes used and the large loops in the measurement setup, large spikes are visible at the falling and rising edges of the external HV pulse. The measured pressure waves with the hydrophone show similar peak pressure being generated. The external pulse does seem to be a bit lower however this could be explained by the fact that the resulting external pulse is not able to hit the CMUT at its exact center frequency, resulting in less acoustic dissipation in the transducer. Most importantly, the two pressure waves do

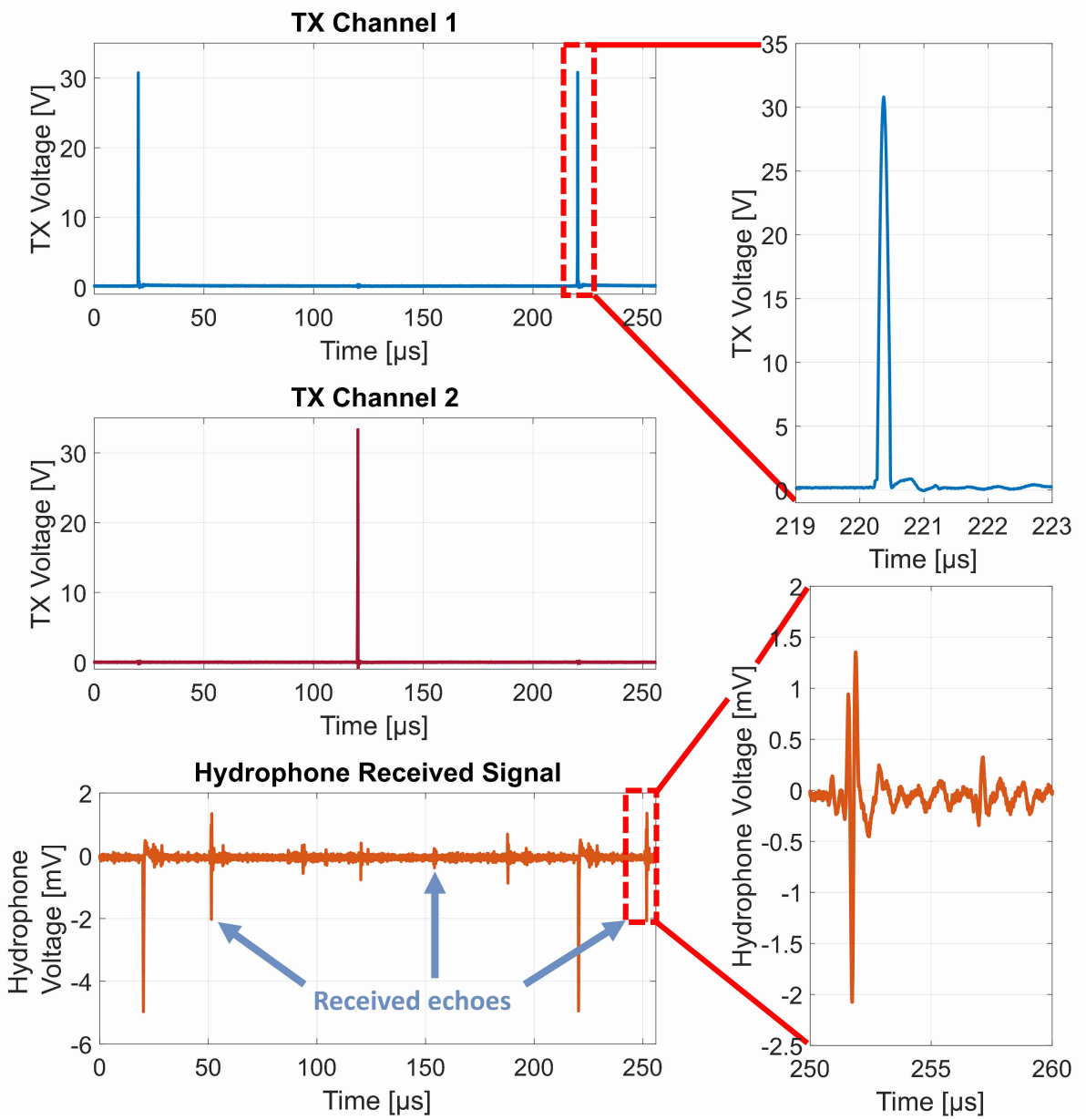

Figure 5.13: Acoustic measurement results with CMUT transducer's during a $30V$ transmit measurement on both TR ASIC transmit channels using a hydrophone.

not show a very large difference, from which we can draw the conclusion that the half-sine excitation generated by the resonant pulser most likely does not degrade acoustic performance.

Finally, a pulse-echo measurement is performed in order to verify the TR switches on the resonant pulser. For the measurement, the reflection on the water surface is used and the received echo is measured on the receive channel of the ASIC. Figure 5.15 shows the measurement results in case a $30V$ pulse is sent and the water level in the waterbag is varied. As expected the first received echoes clearly correspond with the measured distance and thus the roundtrip distance from the ASIC to the water surface. The large voltage spike that is visible at the exact timing moment the pulse is created is due to the parasitic capacitance present on the PCB which gets charged through the TR switch during the generation of the pulse and discharging of the CMUT before reception can start.

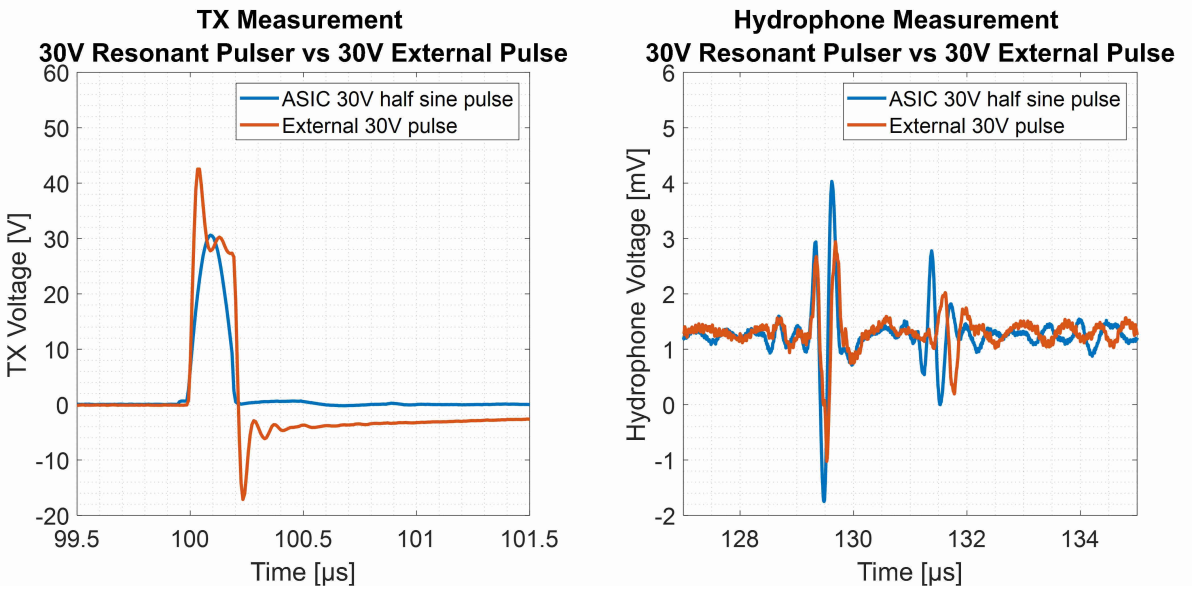

Figure 5.14: Comparison between the resonant pulser ASIC generating a $30V$ pulse and an external $30V$ pulse, transmit voltage (left), and received hydrophone signal (right).

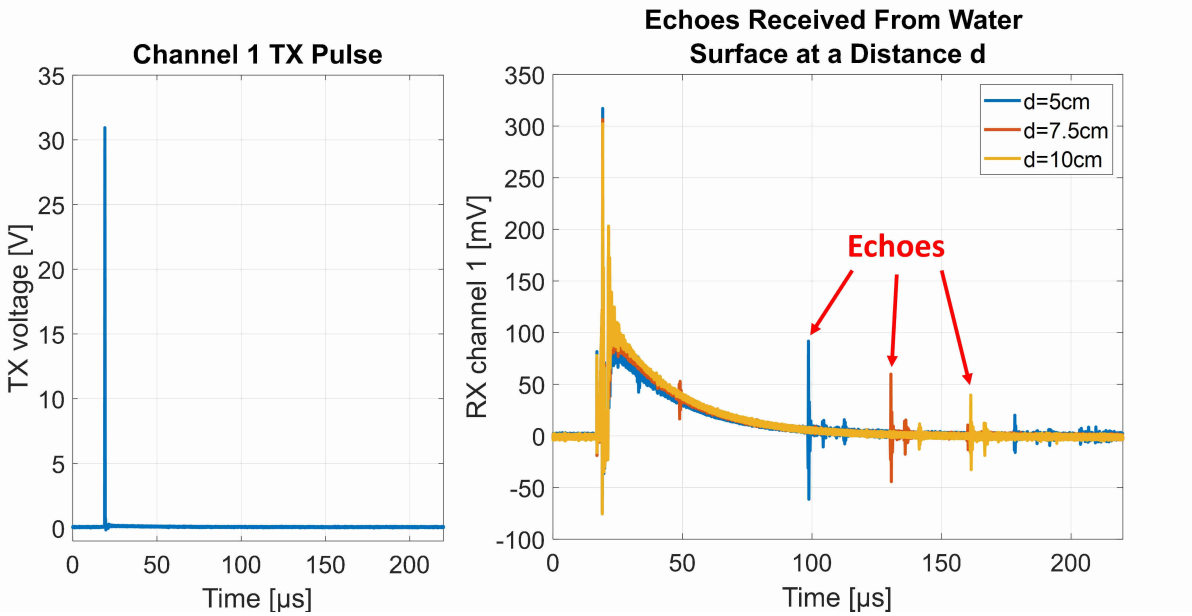

Figure 5.15: Pulse-echo measurement results for the TR ASIC, varying water surface depth between 5, 7.5 and 10cm from the array.

6

Conclusions and future work

6.1. Conclusions and thesis contribution

The goal of this thesis was to design an ASIC capable of generating HV pulses targeting portable US imaging applications. The pulser was required to be efficient and be driven directly from a low-voltage battery supply. A chip has been taped out and measured which demonstrates and verifies the functionality of the resonant pulser. The most important result for this thesis is the simple and efficient core of the resonant pulser, able to achieve a measured peak efficiency of $0.37fCV^2$ while no HV supply needs to be generated or regulated during the operation of the ASIC. It promises to alleviate one of the bigger challenges facing future portable US imaging systems by removing a large overhead consisting of the need to generate and regulate an HV supply on-chip. Especially for wearable applications like US patches, where the time between measurements can be very low, the use of an HV supply would require off-chip decoupling capacitors (which are orders of magnitude larger than the total capacitance of the transducer array) to be recharged before every measurement, leading to a substantial amount of additional losses. The resonant pulser, in contrast, generates HV pulses directly from the battery supply avoiding these conversion losses.

The circuit architecture avoids requiring an additional HV transistor (an HV PMOS) in order to operate which reduces area consumption and by means of multiplexing a large part of the pulser core an area-efficient circuit implementation is achieved for the resonant pulser. Depending on the size of the transducer's electrical capacitance a compact and efficient pulser design can be obtained. One of the interesting aspects of the resonant pulser is that the transmit amplitude voltage is timing-based, resulting in a flexible solution for portable systems requiring high voltage pulses. The amplitude calibration and energy recycling calibration are able to adjust the charging and discharge timing of the pulser accordingly, resulting in accurate transmit pulses and properly recycling residual energy left on the transducer.

The implemented resonant pulser ASIC has proven to be robust against variations in both C_p, L, and V_{bat} across their expected range. Trimming of the transducer is vital to the implemented design of the resonant pulser, the additional losses due to the added capacitance from the CDAC are unfortunately indispensable. The energy recycling process does reduce the expected losses due to the larger load the pulser has to drive and the resulting higher peak current present due to a smaller inductor as has been shown in Section 4.5. However, the resulting simple synchronous operation of the pulser which is free of static-power dissipation presents itself as an interesting option for US imaging ASIC design.

Table 6.1 presents a comparison table of the measured resonant pulser ASIC performance and draws a comparison to prior art efficient HV pulser's. It shows that the achieved efficiency of the ASIC is competitive with other HV pulser's. Designs obtaining higher efficiency like the work presented in [17],

[14], and [11] all require either an external HV supply or suffer from large additional conversion losses from operating the regulated on-chip HV supply, besides operating at a (much) lower frequency. Most importantly this work presents the first pulser able to generate a HV transmit pulse directly from a battery supply.

Table 6.1: Summary of the performance of the resonant pulser prototype ASIC and comparison between prior art.

	[10]	[17]	[12]	[14]	[4]	[11]	[50]	**This work**
Transducer	CMUT	PMUT	PMUT	PZT	PMUT	CMUT	PMUT	**CMUT**
Operating frequency	3.3MHz	1MHz	5MHz	5kHz	8MHz	250kHz	250kHz	**2.5MHz**
TX voltage	30V	28.7V	13.2V	30V	32V	32V	24V	**30V**
Technology	180nm BCD	180nm BCD	180nm CMOS	180nm BCD	180nm BCD	180nm BCD	800nm IGZO	**180nm BCD**
Load capacitance	40pF	1nF	15.4pF	470pF	17.5pF	240pF	36pF	**120pF**
Theoretical C_p loss reduction	50%	NA	50%	100%	NA	83.3%	NA	**100%**
Measured C_p loss reduction	38%	75.4%	42.2%	73.1%	NA	80%	22%	**63%**
# Off-chip components	2	5	NA	NA	2	5	NA	**1**
External supply voltage(s)	1.8V, 3.3V, 30V	1.2V, 5V	3.3V	1.8V, 5V, 30V	1.8V	1.8V, 32V	6V, 12V	**3.6V**
HV supply	External	Supply Multiplier	External	External	Charge Pump	External	External	**Not needed**

6.2. Improvements and future work

The main focus of this work was to design and measure a prototype chip of an ASIC capable of generating HV pulses directly from a battery supply. The main concept of the resonant pulser has been proven rather successful. Nonetheless, individual blocks in the current circuit design can most likely be improved in order to increase the performance of the pulser. Besides providing improvements to the designed prototype several other interesting architectural alternatives could be further explored, which could lead to better performance in possibly either energy efficiency or imaging quality. Some suggestions are provided below:

- The reduction in energy efficiency due to additional inductor non-linearity has to be further investigated. Optimizing the inductor could possibly boost the power efficiency of the pulser significantly. Besides, a better understanding of the possible inductor non-idealities that have been missed in the analysis in this thesis should lead to a better optimized pulser design. In case a transducer with a larger C_p would be used (which should also be available at low resonance frequencies) the inductor size could be reduced substantially opening the possibility of using on-chip inductors,bond wires as inductors or PCB traces, possibly avoiding the need for linear and efficient commercially available inductors.

- The measurement setup can be improved to better analyze the performance of the ASIC and more accurately measure the efficiency of the pulser, e.g. the ability to monitor the inductor current. Besides, the TO ASIC still has to be measured and is expected to provide slightly higher efficiency.

- Also, a more detailed and careful acoustic evaluation of the resonant pulser should be performed. For this, a larger array integration is required also in order to perform beamforming using a syn-

thetic aperture imaging technique.

- The possibility to adapt the resonant pulser to send pulse trains could be implemented. The current design is unable to do this because the combination of the transducer's center frequency, C_p, and battery supply results in a required inductance which leads to charge and discharge time longer than the available time period to create a pulse train. One option would be to design the resonant pulser to operate at $f_0 > f_s$ in order to create square wave-like pulses as discussed in Chapter 2. This would lead to a reduction in either C_p and/or L, in case only L scales down it would result in possibly much higher current flowing through the switches. From the analysis done in Chapter 2 it was concluded that such a circuit architecture would lead to reduced efficiency. Alternatively, a configuration could be designed where 2 inductors operate in a ping-pong fashion. By charging a second inductor while the first inductor charges the transducer, pulse trains could be generated in case the charge and discharge time of a single inductor are too long.

- Bipolar pulsing can also be explored, as a means to increase the acoustic performance of the pulser. It would require an additional HV switches in order to flip the polarity of the inductor or keep the inductor connected and use back-to-back isolated switches. Additional circuity to properly detect the required switching moments should in that case be investigated, or it would require a redesign of the switches. The resulting increase in roundtrip SNR could make it a valuable addition to the resonant pulser.

- For a more mature prototype the digital circuits need to be synthesized (and optimized) and placed on the ASIC and a strategy to efficiently address each of the transmit channels needs to be worked out together with the required calibrations that need to be performed for each of the transmit channels.

- Finally, a more mature prototype could be designed to be used with either PMUT or pre-charged CMUT transducer's [30] in order to remove the HV bias supply from the measurement setup.

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A

PCB layout

A.1. Measurement board layout

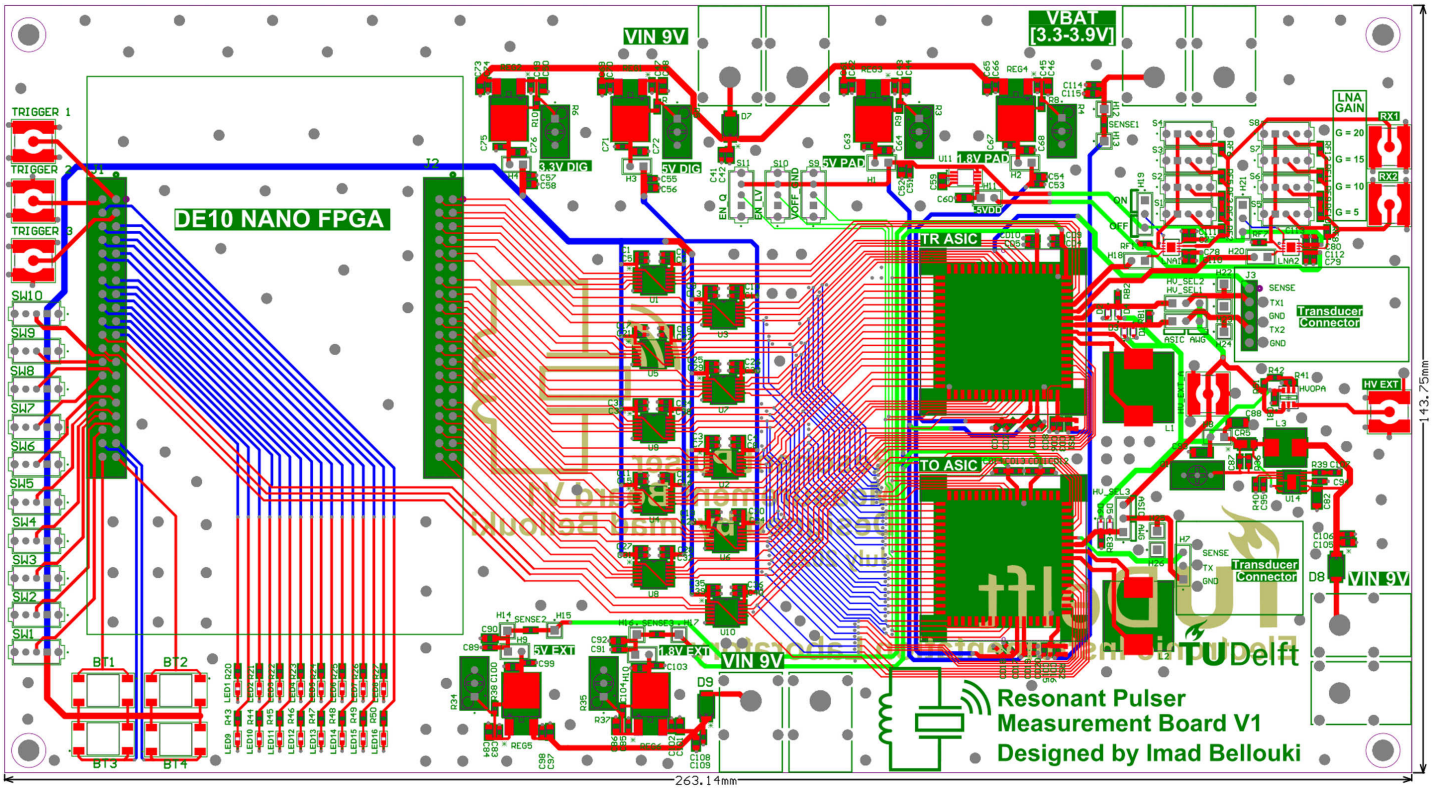

Figure A.1: Measurement board PCB layout.

A.2. Transducer daughter boards layout

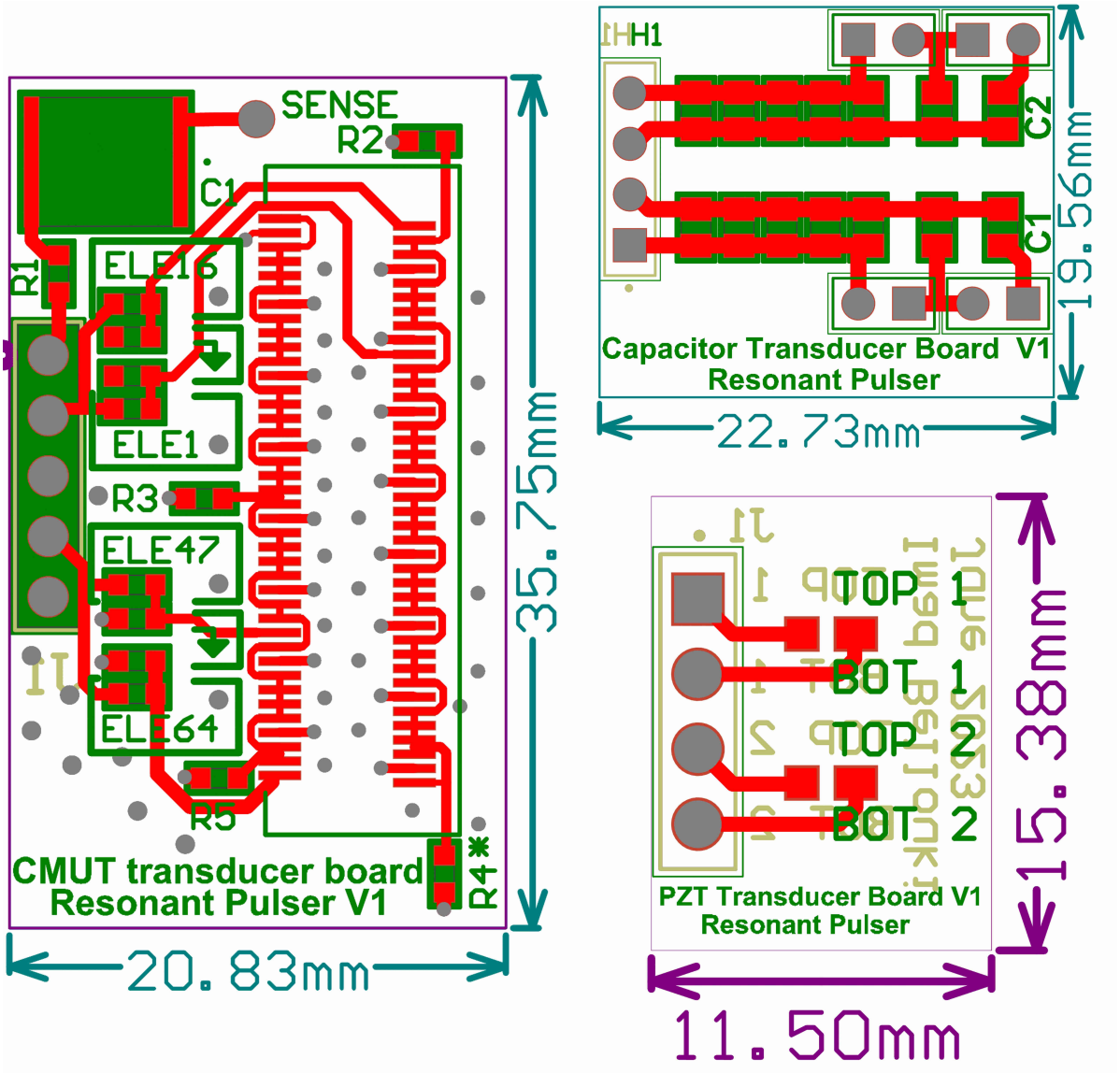

Figure A.2: Transducer daughter boards layout, (left) CMUT daughter board, (right top) capacitor daughter board, (right bottom) PZT daughter board.

This work presents the first ASIC able to generate HV pulses directly from a low-voltage input supply. The design was aimed at implementing an energy efficient HV pulser for portable ultrasound imaging applications. By omitting the need for generating and regulating an HV supply to create excitation pulses for an ultrasound transducer a significant amount of power is saved in the end-to-end efficiency of the system.

The pulser (called the “resonant pulser”) uses resonant energy transfer between an off-chip inductor to supply energy directly to a transducer. The same resonant energy transfer is used in a similar manner to recycle residual reactive energy left on these transducers back to the input supply, saving a considerable amount of power.

The resonant pulser contains 5 programmable transmit amplitudes between 10-30V which are automatically calibrated. Likewise, the resonance frequency and the energy recycling circuitry are also automatically trimmed and calibrated respectively. Resulting in an elegant, energy-efficient and area-efficient design.

Two prototype chips have been taped out in TSMC $0.18\mu m$ BCD Gen2 technology. One of the ASICs implements a single pulser design which has been optimized for power efficiency, while the second ASIC implements 2 transmit channels and the ability to receive echoes. The two-channel ASIC has been measured both electrically and acoustically with CMUT transducers. The resonant pulser has been demonstrated to generate the different programmable pulse amplitudes correctly with a $1V$ accuracy. And furthermore, both transducer trimming and energy recycling calibration have been tested successfully. The ASIC measured a peak efficiency of $0.37fCV^2$.

The ASIC is also the first reported chip targeting portable ultrasound to require only a single off-chip component to function. Besides the pulser being 63% more efficient compared to a Class-D pulser it saves a considerable amount of power considering the omission of a HV supply.

Imad Bellouki
Delft, December 2023

TU Delft