High Density Flexible Interconnect for Minimally Invasive Medical Instruments

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High Density Flexible Interconnect for Minimally Invasive Medical Instruments

by

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Abstract

Flex-to-rigid (F2R) is a technology platform for the fabrication of miniature partially flexible sensor systems for minimally invasive medical instruments. Because of the flexibility, these sensor systems can be wrapped around cylindrical medical instruments such as catheters or guidewires. F2R is a post-processing technology whereby flexible interconnects, consisting of an AlCu routing layer sandwiched between two layers of flexible polyimide, are fabricated on a silicon wafer. This is followed by a separation step whereby individual elements are singulated by Deep Reactive Ion Etching (DRIE) and Reactive Ion Etching (RIE). The F2R fabrication is based on standard IC fabrication technology, which allows the devices to scale down so that all kind of sensing functionalities and electronics can be integrated into the tip of a catheter.

This thesis focuses on the improvement of the F2R technology. One of the objectives was to increase the density of the devices. By patterning the metal interconnects by RIE, instead of wet etching, very high density interconnects are fabricated. Corrosion-free interconnects down to 0.8 µm width were fabricated using this new developed process. Furthermore, the vias between the two metal layers in F2R were improved. Small pitch vias down to 3 µm diameter were fabricated by etching small tapered holes in the polyimide layer and sputtering metal in these contact holes.

Because of the in-body application of F2R, a perfect adhesion between the several layers is required. The polyimide-polyimide adhesion is known to be troublesome. Therefore, improving the adhesion of this interface was explored in this work. A perfect adhesion was obtained by a novel method which combines a thin layer of SiC and SiO_2 into an adhesion improvement layer between the polyimides.

The developed fabrication processes, high density interconnects, small pitch vias and the adhesion improvement, were integrated into the F2R process flow. Test devices, consisting of a silicon island with bond-pads and test structures and a flexible part with meandering interconnects, were fabricated using this improved process flow. Bending tests showed that bending radii of the flexible interconnects down to 10 µm are achievable while not damaging the interconnects. This extreme flexibility is required to wrap a high density imaging system around a guidewire to fabricate a 360 µm diameter F2R IVUS catheter. An analysis is presented that describes the relation between the geometry of the F2R technology and how such a device can be folded around a cylindrical instrument. It is found that using the same F2R technology, such a system can be scaled down to a smaller diameter relatively straightforward.

Preface

After a year of work, this thesis concludes my master Electrical Engineering degree. This work is conducted in the field of microelectronics, more specifically, flexible electronics. During my master graduation project I worked at Philips research on the improvement of the Flex-to-Rigid (F2R) technology platform. This technology platform uses IC and MEMS technology to fabricate partially flexible sensor system for medical instruments. Experimental work on the improvement of the fabrication process has been conducted in the Philips Innovation Services cleanroom in Eindhoven.

First of all, I would like to thank my supervisor Ronald Dekker for the opportunity of doing this thesis and the support during this project. Besides doing my master thesis, I also enjoyed working there and I learned a lot during my internship at Philips. Secondly, I would like to thank Aslihan Arslan for her help in the start of this project and the guidance in the first months. Furthermore, my thanks goes to Marcus Louwerse, Shivani Joshi, Angel Savov and Lambert Bergers for both their help in the cleanroom and the usefull discussions we had.

Michel van der Kaay

Eindhoven, August 2017

Contents

1 Introduction

In recent years Micro-Electro-Mechanical systems (MEMS) have improved and made it possible to develop all kinds of micromachined sensors for applications in different fields. One of these applications is the development of minimally invasive instruments for diagnosis and therapy for Coronary Artery Diseases (CAD). In these diseases the blood flow to the heart is partially or totally blocked. CAD is one of the leading causes of death with 7.4 million deaths per year worldwide [1]. Problems such as deposits of coagulated blood, fatty tissues or calcium on the wall of the vessel are generally treated by minimally invasive procedures using catheters assisted by a guidewire. Integrating sensing functionalities at the tip of the catheter can allow more accurate and reliable prevention and treatment of CADs. The usage of minimally invasive instruments is depicted in Figure 1.1.

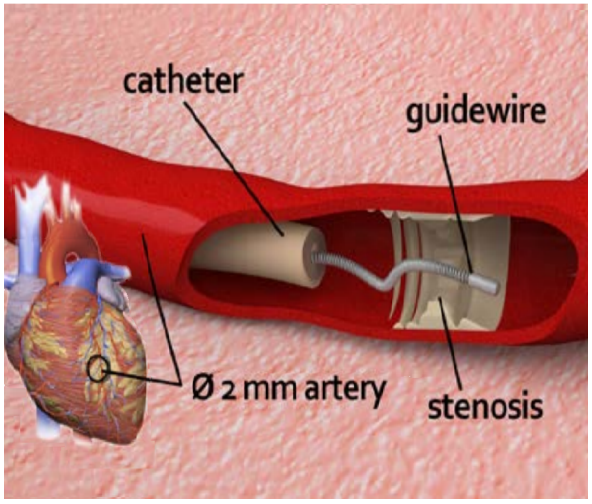


Figure 1.1: Minimally invasive instruments are used during an intervention in a coronary artery. The stenosis is a abnormal narrowing of the artery. First a flexible guidewire is inserted, then the catheter is assisted by the guidewire [2].

A frequently used sensing functionality is intravascular ultrasound (IVUS). IVUS is an imaging technique where arrays of ultrasound transducers are used to acquire images from the inside of a vessel. A side looking (SL) feature on IVUS imaging catheters give a cross-directional view from the inside of the vessel. The combination with a forward looking (FL) imaging system can potentially give a real time 3-D visualisation of the artery [3].

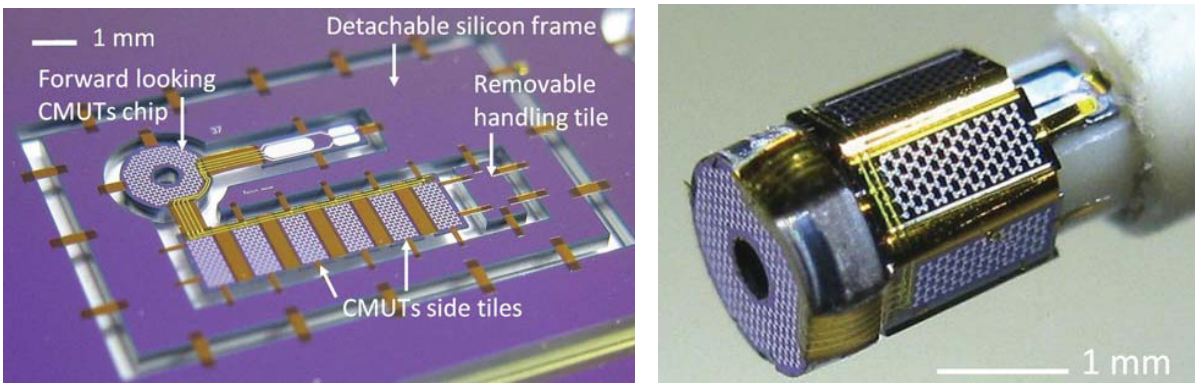
However, using micro-systems and sensors on conventionally shaped (square or rectangle) silicon chips can give problems since medical instruments are usually cylindrically shaped. To fit sensing functionalities in and around the tip of a catheter, a solution can be to use partially flexible sensor systems. The sensors should be fabricated on arbitrarily shaped silicon islands connected by flexible interconnects. Through this approach the state-of-the-art in microelectronics can be applied to the world of minimally invasive surgery. Furthermore, new developments can be relatively easily implemented in such a system in contrast to a design specifically for one sensor. Also instruments such as flow and pressure sensors can be integrated using this technology [4–6]. Besides, the scaling down of this IC technology approach is more straightforward compared to an approach where a standard flex foil solution is used.

1.1. Flex-to-Rigid technology platform

Flex-to-Rigid (F2R) is a novel technology platform for the fabrication of partially flexible miniature sensors connected by flexible high density interconnects [4]. This process has been designed to overcome

the problems with the difference in shapes and to squeeze sensing functionalities in a small volume.

In F2R, rigid silicon parts are combined with flexible polyimide structures with embedded interconnects. In this novel technology platform the devices are fabricated using standard IC and MEMS technology in a planar process and can be folded into the desired form after release from the wafer. An example of a planar and mounted F2R device is shown in respectively Figure 1.2a and 1.2b. The sensors are fabricated on the rigid silicon island connected by polyimide bridges which contain the embedded metal rerouting layer. This metal layer, which is sandwiched between polyimides, forms the electrical flexible interconnects between the sensor islands. The metal layer lies in the neutral stress plane which allows for very high flexibility of the interconnects.



(a) (b)

Figure 1.2: (a) A F2R demonstrator suspended in a silicon frame by polyimide hinges. (b) A mounted F2R demonstrator at the tip of a 2mm catheter[5]

1.1.1. Design requirements

To fit all these sensing instruments on the tip of minimally invasive instruments with the F2R approach it has to fulfill the following design requirements [6];

1. The available volume is small, and in the case of ($360\mu m$ diameter) guide-wires extremely small. This makes it unavoidable to render the sensor assembly at least partly flexible so that it can be folded into, or around the instrument, even more so since some sensing functionality, such as flow, has to be performed on the perimeter of the instrument.

2. Most of the instruments are round, so the technology platform should allow for the fabrication of round, or in general, arbitrarily shaped silicon elements which can e.g. be mounted on the tip of the instrument.

3. From a stand point of manufacturability, as much as possible known and proven production methods should be used. Processing of non-standard materials should be avoided as much as possible, or at least moved to the end of the fabrication sequence.

4. For the few “intelligent” minimal invasive instruments which are on the market today, the assembly costs by far outweight the fabrication costs of the sensor itself. Ease of assembly is therefore of paramount importance. Standard and well established manufacturing techniques should be used as much as possible.

5. It must be possible to scale the concept down so that it can be used as an integration platform for the smallest catheters and guide-wires with diameters down to $360\mu m$.

With the guidance of these requirements on the design, F2R will be a low cost, flexible and scalable platform where the state of the art of sensor and IC technology can be applied.

1.1.2. CMUT

With F2R, IVUS can be implemented on the tip of catheter by fabricating ultrasound transducer arrays on the silicon tiles. The first IVUS devices used piezoelectric elements as imaging sensors [7]. However, using Capacitive Micromachined Ultrasound Transducer (CMUT) technology has some major advantages. From a manufacturability point of view the micromachined CMUTs are easier and less costly to fabricate compared to the piezoelectric elements [8] and allow for further miniaturization. CMUT technology also allows for scaling to higher frequencies and a larger bandwidth. Hence, for fabricating arrays of transducers CMUTs are the most logical choice. Moreover, the integration with electronics is easier with CMUTs. In Figure 1.3 the cross-section of a schematic CMUT device is shown.

The bottom electrode of this capacitor is generally doped silicon, however also a metal layer can be used as electrode. Next, the first insulating layer, for example silicon nitride, is deposited. On top of this layer a sacrificial layer is deposited and patterned using standard IC processing, this will define the cavity. Subsequently this will be covered by another insulating layer, this layer will form the membrane of the device. Small through-holes are made to create an opening for the etchant, the sacrificial layer can be wet etched using an etchant with a very high selectivity to the insulating layer. Subsequently the top electrode metal is deposited and patterned. Finally the device is covered with a passivisation layer [9].

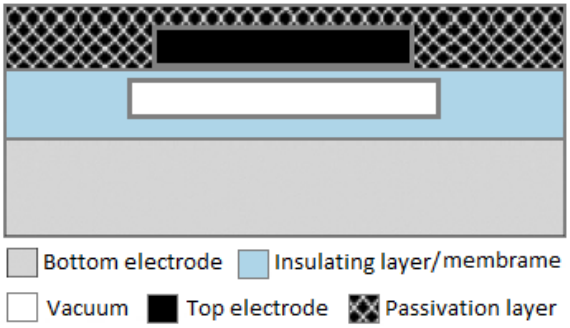


Figure 1.3: A schematic cross-section of a CMUT device. Using micromachining a cavity is created in an insulating layer on top of doped silicon (bottom electrode), on top op the insulating layer a top electrode (metal) is fabricated. The part between the part between the vacuum and the top electrode is the membrane.

The capacitor is formed between the bottom and top electrode. The capacitance is modulated by the vibration of the membrane. When an AC signal is applied to the CMUT the membrane will start to vibrate and produce ultrasound waves. Beside transmitting the CMUT can also receive ultrasound signals. If waves are applied to the device, an alternating signal will be generated since the capacitance is modulated by the waves.

1.1.3. Polyimide

Polyimide (PI) is polymer with many interesting properties such as a high resistance to heat and chemicals, good mechanical properties and excellent flexibility. Due to these excellent properties polyimide is used in many fields, also in the microelectronics industry. For F2R this material is as used for the fabrication flexible interconnects. Since the good heat en mechanical resistance polyimide can be used in combination with standard IC processing for MEMS applications. Polyimide is applied by pouring it as a solution on the wafer. By spin coating, the layer equally spreads. The rotation speed during the spin coating will determine the polyimide thickness. Subsequently the wafer with the polyimide layer is cured in an oven with a nitrogen environment. After the curing, the polyimide is a flexible solid heat resistant layer.

PI can be patterned using lithography, masked with photoresist, or alternatively an oxide or metal hard mask can be used. Uncured polyimide can be both wet and dry etched [10], however, cured PI can be only etched dry. For dry etching of PI, Reactive-Ion etching (RIE) is used [11]. RIE is a technique where a chemically reactive plasma is created and applied to the wafer surface. The reactive ions attack the surface and etch the targeted material. To etch PI by RIE, the etchant is an oxygen based plasma.

When using photoresist as a mask the selectivity is poor since the organic photoresist is also etched in the O_2 plasma. With a hard etch oxide or metal hard mask the selectivity is very high, so higher aspect ratio (ratio between height and width of the trench) vias can be fabricated [10, 11].

1.1.4. F2R basic process flow

The fabrication of F2R starts with a processed silicon substrate that may already contain the ASIC circuits and sensor technology. The process flow is depicted in Figure 1.4, the different steps, marked with a letter, will be explained in the text below.

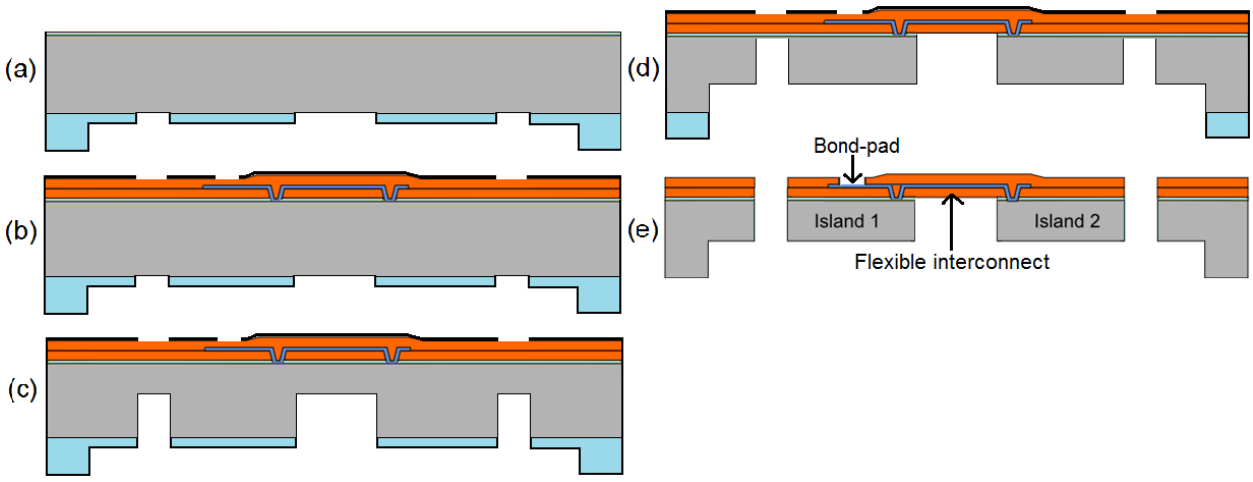


Figure 1.4: The simplified F2R process flow [6]. The different pictures, marked with a letter, are described in the text below.

Backside mask definition

Before the front side processing starts, a hard mask is fabricated on the backside. This back mask will be used later to define the thin ridged silicon islands and the silicon handling tiles. The hard mask is fabricated using two lithography and etching steps, resulting in two different thicknesses of the mask. A Plasma Enhanced Chemical Vapor Deposition (PECVD) silicon oxide layer is deposited on the backside. Next, a photoresist layer is spin-coated and exposed with the image on the wafer stepper. Using the photoresist as mask the oxide is etched in a RIE etcher to create the first hard etch mask. Repeating this process with the second lithography mask completes the oxide hard etch mask. The hard mask is shown in Figure 1.4a. The pre-processed silicon substrate (grey) with the back hard etch oxide mask (blue).

Polyimide deposition and metal routing

The next step is to fabricate the layers of PI (orange) and the metal routing, this is shown in Figure 1.4b. First the bond-pad aluminium layer is sputtered and patterned using standard lithography and wet etching. Next, the first polyimide layer is spin coated and cured. This layer is pattered using a thick photo resist and O_2 RIE. During the patterning of the first polyimide layer also the vias in the polyimide between the first and the second metal layers are defined. Then the redistribution metal layer is sputtered, the purpose of this layer is to fill the vias and to fabricate the metal interconnects. This layer is patterned using lithography and in the current process etched with a wet etchant. On top of the interconnects the second layer of PI is spin coated and cured. Finally a metal layer is applied (black), this layer has the purpose of a hard etch mask for the second PI layer. The second PI layer is etched at the end of the processing.

Backside etching

In the next processing step the backside mask is used to etch through the silicon using Deep Reactive Ion etching (DRIE). DRIE is an anisotropical etching technique for creating high aspect ratio structures. DRIE consists of a repetition of small isotropic etch steps and sidewall passivisation to allow for very anisotropical etching. In the first DRIE etch the silicon will be thinned down on the places where the islands will be located. This is shown in Figure 1.4c. Figure 1.4d shows the final step of the backside etching of the wafer. First the thin oxide mask is removed using RIE. The resulting hard etch mask is then used to etch all the way through the silicon with DRIE. The islands are separated during this process, but they are suspended in the silicon frame by the PI hinges.

Polyimide patterning and separation

In the last processing step, the PI is patterned using O_2 based RIE using the earlier deposited and patterned metal hard-etch mask. During the etch, free standing structures are created and the bond-pads are opened. Afterwards this metal mask is removed using wet etching. The fully processed sensor islands suspended in the polyimide hinges are shown in Figure 1.4e. Finally the F2R structures are suspended in the silicon frame by polyimide hinges and can be released from the frame. The devices can be separated by laser cutting or by cutting with a knife through the PI hinges. After this stage the fully processed devices are ready for assembly.

1.2. Aim of the Thesis

The research objective of this Thesis is driven by the further development of the F2R technology platform. In the last few years a lot of progress has been made in the development of F2R. However, to achieve the final goal, creating a low cost platform that can integrate state-of-the-art sensing functionalities for smart catheters and guidewire down to 360 µm diameter, F2R has to be developed further. The major challenges are miniaturization of the ultrasound transducer islands around the guidewire, increasing the density and decreasing the pitch of the flexible interconnects.

The theoretical investigation of the miniaturization of the IVUS islands around the guidewire is one of the objectives of this work. As shown in Figure 1.2b the tiles, connected by flexible interconnects, are folded around a cylindrical shaped medical instrument. More and thus smaller transducer islands are required for higher resolution images. To improve and miniaturize such an IVUS system the tiles should be made smaller. The circumference of the guidewire should obviously be smaller than the width of all the tiles combined. However, more geometrical aspects should be taken into account to ensure that the bending radius of the tiles connected by flexible interconnects is smaller than the diameter of the guidewire. Current research on F2R is lacking analytically analysis on the geometry of the miniaturization of the islands around a guidewire. This theoretical analysis is one of the research goals of this Thesis.

For reliable microfabricated devices the adhesion between the different layers should be strong. In F2R these interfaces are between polyimide and the substrate and the first PI layer to the second PI layer. Both during the assembly and the in-body application the adhesion between these layers should be very good and reliable. In the current F2R process the adhesion of polyimide to the substrate is good, but the self-adhesion of polyimide is poor. To improve the polyimide-polyimide adhesion, in this Thesis this adhesion will be investigated. Experiments with different adhesion promotion techniques and layers will be conducted. The goal is to find a procedure resulting in a reliable, consistent and very strong adhesion between the polyimide layers. It should also be possible to integrate this adhesion promotion technique(s) with the F2R flow with adding as little as possible extra complexity.

The other goal of the work is to research high density flexible interconnects. To integrate more sensors in the same, or even smaller, volume, the density of the interconnects should be increased. Furthermore, for the down scaling of F2R, flexible interconnects with a smaller interconnects pitch are required. The challenge of the design and fabrication of these high density interconnects is addressed in this work. In the current F2R process the interconnects are defined using wet etching, however this results

in low aspect ratios, non-straight sidewalls and a high pitch between the interconnects. Using RIE can solve these problems and give smaller pitch interconnects. The introduction of dry etching of the metal interconnects can give some additional challenges like corrosion of the metal. Furthermore, the effect of the reactive ion plasma to the polyimide surface is unknown. The objective is to fabricate dry etched 1 µm till 3 µm width flexible interconnects with a separation between the interconnects of < 1 µm.

Likewise, the dimension of the contact holes in the PI layer to connect the metal layers should also decrease, this is also an objective of this work. In the current F2R process the diameter of the vias is 6 µm, the goal of this work is the fabricate 3 µm diameter vias. Finally, all these individual processes will be integrated in the fabrication of flexible interconnect test structures based on the F2R process flow, with the new techniques included.

With guidance of the design requirements listed in 1.1.1, the F2R platform will be improved and a new techniques developed. This Thesis will make a step in this development of a new generation F2R by achieving the goals described in this Section.

1.3. Organization of the Thesis

In Chapter 2 a relation is found between the geometry of the F2R technology and how a F2R IVUS device can be wrapped around cylindrical medical instrument. Chapter 3 explains the project outline, the mask design and the used materials. The dry etching of the flexible interconnects is shown in Chapter 4. Next, the fabrication of the small pitch contact holes is explained in Chapter 5. The investigation of the polyimide-polyimide adhesion is discussed and demonstrated in Chapter 6. In Chapter 7 the fabrication of the flexible interconnect test devices is explained. This also includes the integration with the dry etched interconnects, small pitch vias and the adhesion layers with the F2R process flow. The results of electrical measurements and the bending test are shown in Chapter 8. Finally, this Thesis is concluded in Chapter 9.

2

High density tapered islands

2.1. Introduction

To implement a side-looking IVUS imaging system on a catheter, Ultra-Sound transducers need to be placed on the perimeter of the catheter. Silicon IVUS tiles, connected by flexible interconnects, are wrapped around the cylindrical instrument. This array of sensor islands can be bent around a cylindrical instrument, for example a guidewire or catheter. The bending radius of this array depends on the size and shape of the islands. Additionally, it also depends on the dimensions of the flexible interconnects between the islands. Using these parameters a geometrical model can be made to find the relation between the various dimensions and the bending radius. In this Chapter a mathematical relation between the geometrical parameters and the bending radius is derived. With this relation multiple configurations are calculated and analyzed.

The silicon islands are created using the F2R process, this process flow explained in Section 1.1.4. During the backside etching the silicon islands are defined. Besides the size and thickness of the islands also the angle of the etching can be adjusted during this stage. DRIE can be used for highly anisotropic etching of structures with high aspect ratio and very straight walls, however, the process can be made more isotropical by adjusting the etch steps. During DRIE small isotropic etch steps are used, alternated with side wall passivation steps to prevent etching of the side wall. A tapered sidewall profile can be achieved by adjusting the duration of the steps over time. Another method is to not use sidewall passivation and alternate between isotropic and anisotropic steps [12]. In this case the scallops created in the previous cycles expand every isotropic step, thus the first scallops of the trench are the widest. Figure 2.1 shows a tapered trench etched using a combination of normal DRIE and anisotropic steps. The usage of such techniques allows for etching under a controlled angle, hence smaller bending radii are possible.

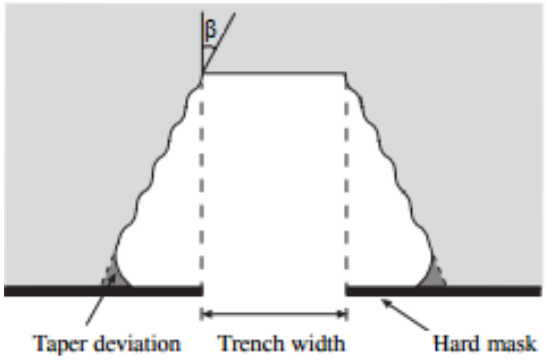


Figure 2.1: A tapered trench etched by a combination of DRIE and anisotropic steps [12]. The hard mask defines the trench width. Due to the isotropic steps the older scallops widen. This result in a taper deviation for the first scallop.

In this Chapter a relation is found between the geometry of a F2R IVUS device and the bending radius. With a etching angle for the DRIE etching of the silicon islands the bending radius can be small, this relation will be investigated. Also the effect of the trench aspect ratio and the thickness of these islands and the number of islands on the bending radius will be investigated. The main point of interest is to find the required required etching angle of the silicon islands for specific configurations. The analysis of the relation between these parameter and the bending radius will give a better understanding of the design space of a next-generation F2R devices.

2.2. Trapezoid model

When the silicon tiles are etched from the backside under an angle, the combination of these tiles connected by flexible interconnects is more easily bent around a small radius cylinder. The cross-section of the silicon islands have an isosceles trapezoid shape. Figure 2.2 depicts how two of these tiles are touching each other at the bottom and are separated by a flexible interconnect at the top. This 2D model of the islands can be used to find the a relations of the following parameters. The width W of the islands is defined by line segment $|AD|$, the thickness t by line segment $|CE|$, the space between the tiles s by $2 \cdot |DN|$, the inner bending radius r_{in} is defined by line segment $|KO|$, the etching angle is β and the angle between the tiles when maximum bent is α. In this Section a relation between the bending inner radius (r_{in}) and W,t,s and β is found.

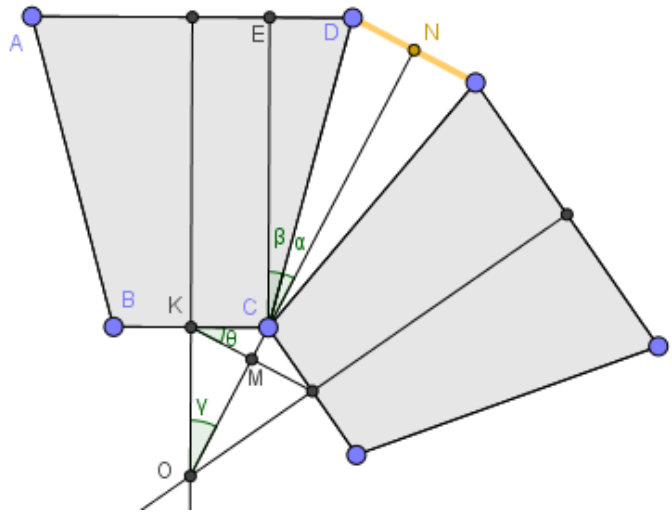


Figure 2.2: The 2D geometric model where two silicon tiles(grey), connected by flexible interconnects (yellow) are touching.

Line KO bisects the trapezoid, and is parallel with line CE. Therefore the following relation can be found:

$$\alpha + \beta = \gamma. \tag{2.1}$$

The segment $|CD|$ is

$$|CD| = \frac{|CE|}{\cos\beta} = \frac{t}{\cos\beta}. \tag{2.2}$$

The angle α is

$$\alpha = \sin^{-1}\left(\frac{s}{2} \cdot \frac{\cdot \cos\beta}{t}\right). \tag{2.3}$$

The length of sections $|KC|$, and $|KO|$ can be found using geometry,

$$|KC| = \frac{|AD|}{2} - |DE| = \frac{|AD|}{2} - |CE| \cdot \tan\beta, \tag{2.4}$$

$$|KO| = \frac{|KC|}{\tan(\alpha+\beta)} = \frac{\frac{|AD|}{2} - |CE| \cdot \tan\beta}{\tan(\alpha+\beta)}. \tag{2.5}$$

Thus the relation between r_{in} and W,t,s and β is

$$r_{in} = \frac{\frac{W}{2} - t \cdot \tan\beta}{\tan\left(\sin^{-1}\frac{s\cdot\cos\beta}{2t} + \beta\right)}. \tag{2.6}$$

2.3. Trapezoid tiles around a cylinder

The next step is to analyse how the trapezoid tiles can fit around a cylinder. A number of n trapezoid shaped silicon sensor islands need to fit around a cylindrical structure. A higher number of tiles has some advantages but also disadvantages. For example, the acoustical performance can be better with more tiles. Furthermore the structure can be bent more easily since their are more flexible parts. However, the fill-factor of the CMUTs on the periphery is smaller due to lost space on for example more interconnects. Moreover, more islands, resulting in smaller islands can make it more difficult to integrate electronics in the small islands. A good analysis of the relations between geometry the will help to understand the problem better.

In Figure 2.3 a schematic cross-section of 8 islands around an imaginary cylinder is shown. The islands are touching, thus in a maximum bending situation. In this Section a relation between r, W, t, s, n, α and β is derived.

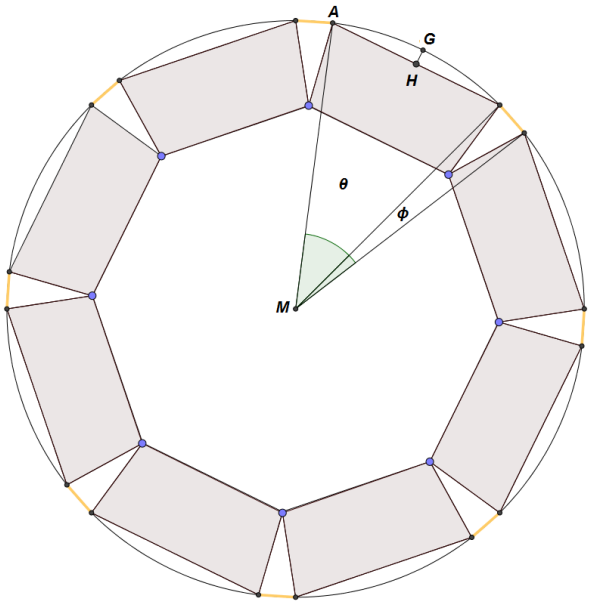


Figure 2.3: Cross-section of $n = 8$ trapezoid tiles around a cylindrical structure. ϕ and θ are the angle of the circle of respectively the interconnect part (yellow) and the silicon part (grey).

With trigonometry an equation for ϕ and θ can be found:

$$\phi = 2 \cdot \sin^{-1}\frac{s}{2 \cdot r_{out}}, \tag{2.7}$$

$$\theta = 2 \cdot \sin^{-1}\frac{W}{2 \cdot r_{out}}. \tag{2.8}$$

Furthermore a relation between the width W of the islands and the angle θ can be found,

$$W = 2 \cdot r_{out} \cdot sin(\frac{1}{2}\theta). \tag{2.9}$$

The total circle is composed of n angles of $\phi + \theta$, thus,

$$\theta = \frac{2 \cdot \pi}{n} - \phi. \tag{2.10}$$

Substituting equation 2.10 in equation 2.9 gives

$$W = 2 \cdot r_{out} \cdot \sin\left(\pi/n - \frac{1}{2} \cdot \phi\right). \tag{2.11}$$

Substituting equation 2.7 in equation 2.11 gives

$$W = 2 \cdot r_{out} \cdot \sin\left(\pi/n - sin^{-1}\left(\frac{s}{2 \cdot r_{out}}\right)\right). \tag{2.12}$$

A relation for the inner radius can be found from Figure 2.3,

$$\tan\left(\frac{\theta}{2}\right) = \frac{1/2|AH|}{|MH|} = \frac{1/2 W}{r_{in} + t}. \tag{2.13}$$

From this expression a relation can be found for r_{in}. Since this equation should be equal to equation 2.6 an implicit relation between the variables of interest can be found. The derivation of this equation if shown in Appendix A. This implicit relation is,

$$\frac{1}{r_{out} \cdot \sin\left(\pi/n + sin^{-1}\left(\frac{s}{2 \cdot r_{out}}\right)\right)} - t = \frac{r_{out} \cdot \sin\left(\pi/n - \sin^{-1}\frac{s}{2 \cdot r_{out}}\right) - t \cdot \tan\beta}{\tan\left(\sin^{-1}\frac{s \cdot \cos\beta}{2t} + \beta\right)} \tag{2.14}$$

Now a relation is found between t, s, n, β and r_{out}. This expression can be numerically solved to find the required etching angles for a several configurations with different radii.

2.4. Results

Equation 2.14 was solved numerically for the etching angle β using different values of the number of islands n, trench width s, island thickness t and outer radius r_{out}. Numerical calculation shows that there is no dependency between β and r. This means that if s, t and n are constant while r is varying, the required etching angle is constant. Of course the width W of the islands will decrease with a decreasing radius r. Furthermore, it is found that the absolute values of t and s are not relevant, only the ratio of t/s is sufficient for numerical solving of the equations. This is convenient because t/s can be defined as the trench ratio in the DRIE backside etch process. Although no explicit solution could be found for β, with the numerical analysis solutions can be found in the form of:

$$\beta = f(n, t/s). \tag{2.15}$$

A relation for β can be found only dependents on the number of islands an their trench aspect ratios.

Table 2.1: The required etching angle β for some important number of silicon islands. Negative angles are considered as 0° is required.

n	β ($\frac{t}{s} = 20$)	β ($\frac{t}{s} = 8$)	β ($\frac{t}{s} = 4$)	β ($\frac{t}{s} = 2.5$)
8	21.1°	19.1°	15.6°	11.19°
16	9.84°	7.70°	4.09°	0°
24	6.07°	3.93°	0.32°	0°
32	4.20°	2.04°	0°	0°
48	2.32°	0.17°	0°	0°
64	1.38°	0°	0°	0°

The required etching angle for some specific number of islands n and the trench aspect ratio t/s, found by the numerical analysis, is listed in Table 2.1. The results found by the numeric analysis shown in the table are confirmed with a geometric software tool. As expected, the table shows situations where there

is no etching angle required. However, to achieve a higher trench ratio an etching angle is required. This angle strongly depends on the number of islands, since more islands makes it easier to bend the structure. To realize a high trench ratio in combination with a smaller number of islands a large etching angle is required.

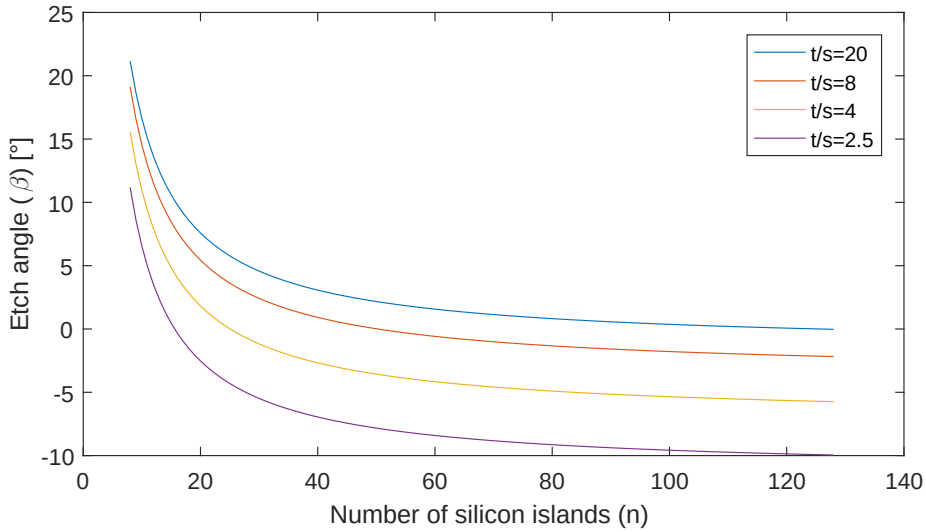


Figure 2.4: The relation between the number of islands n and the corresponding etch angle β for different t/s ratios.

Figure 2.4 shows the result of the calculation of the relation between the etch angle β and the number of islands n for different trench aspect ratios t/s. With an increasing number of islands the required etching angle decreases. Furthermore, a higher trench aspect ratio requires a larger angle for the back-side etching. An interesting observation is that the difference between the graphs for different trench aspect ratio is constant, which means that the derivative of these graphs equal. This is not obvious from equation 2.14.

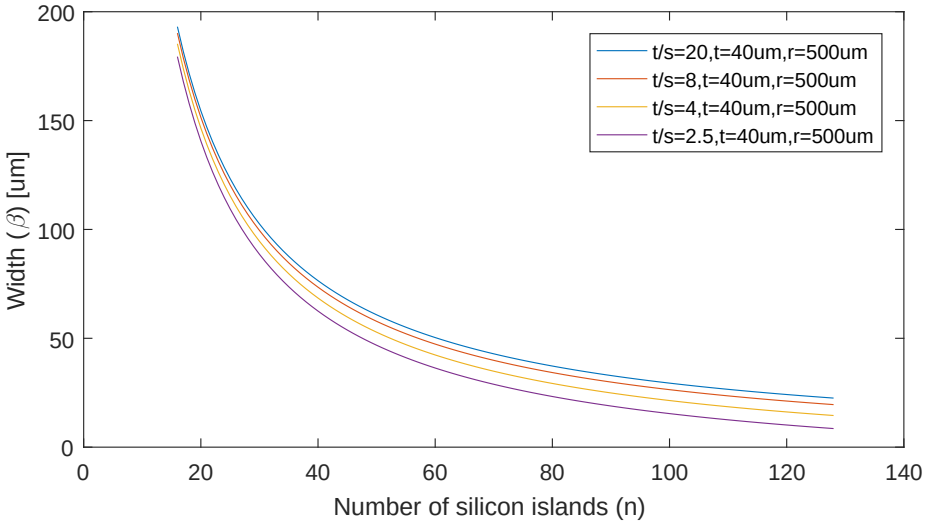


Figure 2.5: The relation between the number of islands and the corresponding island width W for different t/s ratios.

Figure 2.6 shows the required bending radius of the interconnects assuming the interconnects describe an arc between two tiles with an angle of $^{2\pi}/_{n}$. The minimal required bending radius required increases linear with the number of islands because the angle of the arc decreases linearly. In case the interconnects would be assumed to describe a chord (as in the analyses in this 2.3) the bending radius would be infinitesimal.

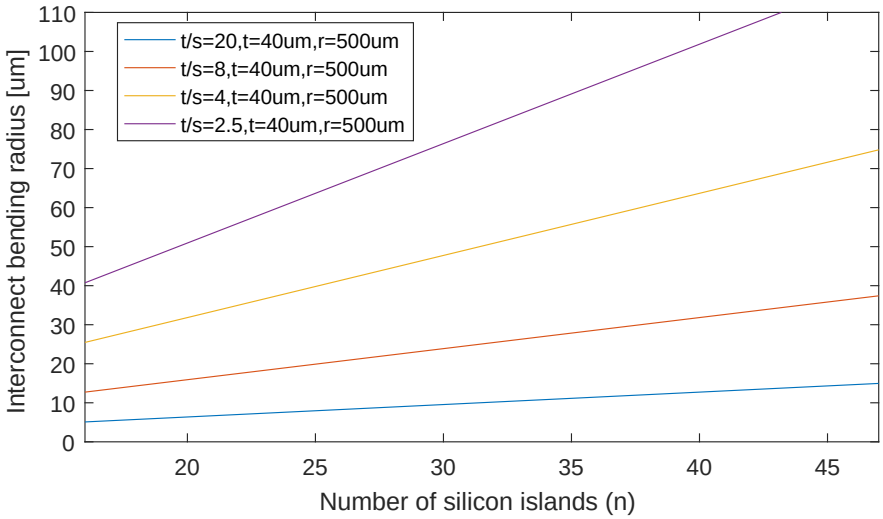


Figure 2.6: The relation between the number of islands and the required bending radius of the interconnects for different t/s ratios.

For an increasing number of tiles, the width of these tiles obviously decreases. Figure 2.5 depicts this reciprocal relation between the width W and the number of tiles n for different trench aspect ratios t/s. For an increasing number of islands the width of the islands is decreasing faster than $1/n$, since the amount of lost area due to trenches is likewise increasing. When a higher trench aspect ratio is used, the width of the islands can be larger which is beneficial for the performance. Obviously, this effect becomes stronger and more important when more islands are used. From Figure 2.5 it seems that the difference in width of the islands is relatively small for the different trench aspect ratios, however, this small difference can still have a large impact on the number of CMUT elements that can fit on the tiles.

The importance of the size of the tiles is better understood if an analysis is done on how many CMUT elements fit on the tiles as function of the number of tiles and thus the width. Figure 2.7 shows the total number of 25 μm CMUT elements that fit on all the islands in a 2D cross-section. Due to the rounding down to integers of the number of CMUT elements the graph has a saw-tooth shape. This results in local maximums where the CMUTs fit optimal on the tiles. The trend through these maxima shows a big difference between the different trench aspect ratios. Mainly for a high number of islands a high trench aspect ratio is important for fitting as many as possible CMUTs around the guidewire or catheter.

2.5. Discussion

In this chapter the analysis of the bending of the ridged islands connected with flexible interconnects is merely based on the geometry of the system in 2D. The physics of bending also effects the actual physical bending radius, hence this model is not complete. The interconnects are ultra flexible, however, the minimum bending radius is non-zero. In [4] it shown that bending radii of $50\mu m$ are possible. When high trench aspect ratios are used in combination with a limited number of islands, the interconnects have relative large bending over a small distance. There are a lot of situations where the required bending radius of the interconnects is smaller than the reported 50 µm. Therefore, smaller bending radii are investigated in Chapter 8.

In the model it is assumed that the tiles are connected in the shortest possible manner as shown in Figure 2.2. This would require an infinite flexible connection. Hence, in practice the shape of the inter-

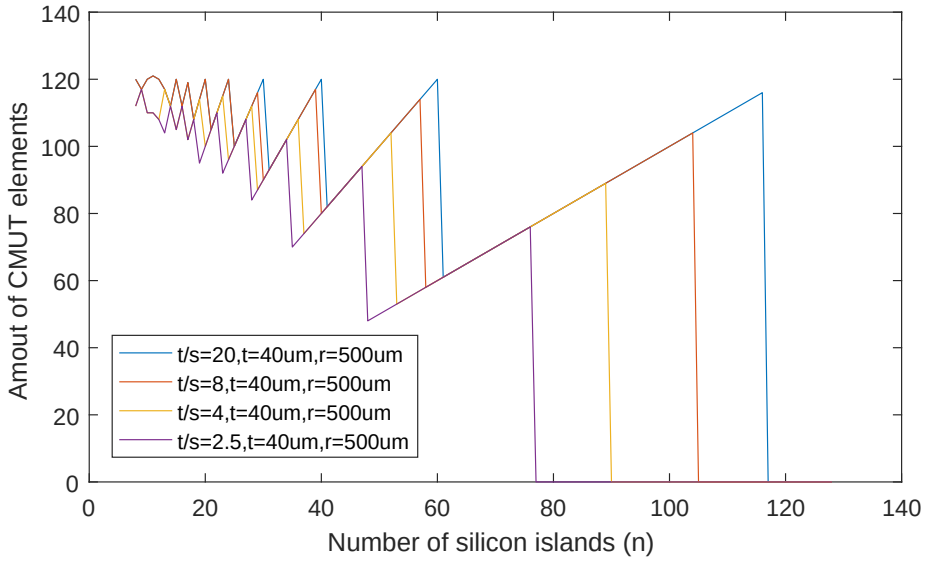


Figure 2.7: The relation between number of islands and the total number CMUT elements(with $25\mu m$ pitch) for different t/s ratios.

connect will be different. This results in that the actual trench-width after bending will be smaller than etched trench-width s. Thus an extra margin has to be taken into account for the width of the trenches.

Furthermore, this model gives a solution for the situation where the silicon tiles are touching at the bottom. This is actually undesirable for the acoustical performance. The performance of the CMUTs will likely deteriorate if the islands are touching because some of the vibrational energy will be lost by the acoustical conductance between the silicon islands. If they are not touching they are more isolated, and thus more energy can be put in the actual signal. Moreover, in practice the silicon area can not be fully covered with CMUTs, and thus some area will be lost.

Higher trench aspect ratios can allow for more CMUT elements fitting on the outside of the cylindrical instrument. One can argue to place more CMUTs on the longitudinal direction of the cylinder, in this direction there is more space available. Partially this is true, however, also in this direction there are limits in the design. Furthermore, a great advantage of having a high trench aspect ratio is that artifacts in the acoustical imaging can be avoided. Ideally the transducers would sense equally in all directions. With a smaller space between the islands, the imaging artifacts can be reduced.

2.6. Conclusion

To conclude this chapter a relation between the geometrical parameters of a F2R IVUS system is found. The introduced model gives a better understanding of how these technology and design parameters relate to each other. Hence, this model defines the design space of F2R for IVUS. Moreover, the model shows how the down scaling of the platform can be implemented for the smallest catheter and guide-wire. Using the same technology (silicon island thickness, etching angle, trench aspect ratio and number of islands), the system can be scaled down to smaller diameters. Only the width of the islands have to be decreased to decrease the diameter of the catheter. Therefore, to fabricate a smaller catheter, the next generation F2R platform the process steps barely have to be changed. This is in accordance with design requirement 5 in Section 1.1.1.

3

Design of the next generation high density flexible interconnects

3.1. Introduction

For a next generation F2R technology platform high density ultra flexible interconnects are required. To develop these high density flexible interconnects test structures were designed, fabricated and tested. This chapter describes the design, function and purpose of the test structures. Furthermore, the used materials in this project are explained.

The flexible interconnects are fabricated using a process flow based on the F2R process flow as described in Section 1.1.4. The full process consist of six lithography steps, with six corresponding masks. To decrease the complexity, first the separate processes and techniques were experimentally performed and optimized. Afterwards, the full process was performed by integrating the developed process into the F2R process flow.

3.2. Mask design

The design consist of tree different kind of test structures: flexible interconnects, vias and daisy chains. Figure 3.1 shows the mask design and the three areas of test structures, moreover, the different colors indicate the different mask layers. Area 1 consists of the bond pads with interconnects in between; on the left part of this area the silicon substrate is etched away, hence the interconnects are flexible. Area 2 contains the vias in the polyimide; many vias in varying size are located in this area. Area 3 contains the daisy chains; these are structures to test electrical connection between the layers through the vias.

For the development of high-density interconnects for next generation F2R, small pitch vias to connect different metal layers are required. Between the metal layers that should be connected there is a layer of PI. First a layer of resist on top of the of the polyimide surface is patterned using lithography. Next, this hole in the resist is transferred to the polyimide by means of dry etching. By sputtering metal, the next metal layer is deposited, but also the contact holes are filled with metal. The contact holes in the polyimide layers are first fabricated and optimized in a separate process, this is shown in Chapter 5. The mask used for these contact hole test structures is shown in Figure 3.2. The mask contains several circular holes ranging in diameters from $1.2\mu m$ to $6.0\mu m$.

To test the electrical connection between the two metal layers daisy chains are used as a test structure. Figure 3.4 depicts an example of a daisy chain mask design. A daisy chain consists of vias and small interconnects in a chain. The mask contains several daisy chains for vias ranging in diameters from $1.2\mu m$ to $6.0\mu m$. The number of elements in series in the chain is ranging from 4 to 128. The fabrication of the daisy chains is shown in Chapter 7

The most important and novel step in this work is the definition of the interconnects by means of dry etching of the metal layer. In the process flow the metal layer is etched on top of a PI layer. Since this step is very experimental, the fabrication of interconnects is first performed on oxide to experiment with

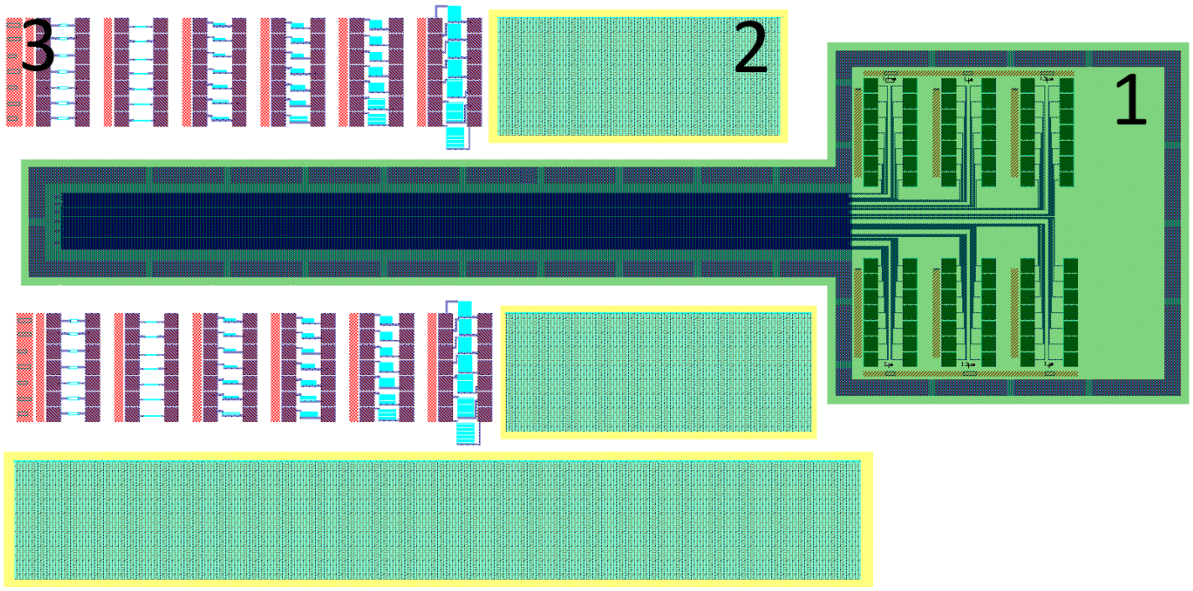


Figure 3.1: Mask design with tree types of test structures. In area 1, 2 and 3 are respectively the flexible interconnects, the vias and the daisy chains located.

the dry etching of AlCu. Next, this extra complexity is introduced by performing a similar process on a PI layer instead of an oxide layer. It is expected that the porous layer of polyimide will show a uptake of chlorine and the problem of post-etch corrosion would be even worse then for the interconnects on oxide. Furthermore, the effect of the chlorine based plasma on the polyimide surface is unknown. Figure 3.3 shows in more detail the mask for the fabrication of the interconnects. This mask is used in the metal dry etching step to define the interconnects. The part where the bond-pads are located will be a ridged thin silicon substrate. The largest part of the interconnects will be flexible, the silicon substrate on which the interconnects are fabricated will be fully etched away. In Chapter 4 the dry etching of the interconnects will be explained and the result will be shown, in Chapter 7 the fabrication of the full process including the backside etch is shown. Electrical measurements can be performed on different flexible interconnects by probing the bond-pads.

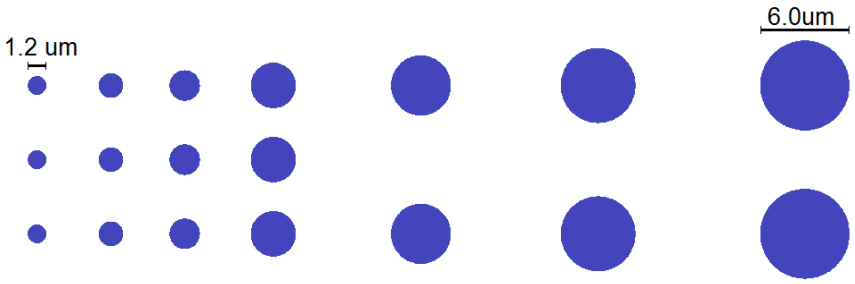


Figure 3.2: The different sized holes in the mask for the fabrication of the vias in the PI layer. The size is ranging from a diameter of $1.2\mu m$ to $6.0\mu m$.

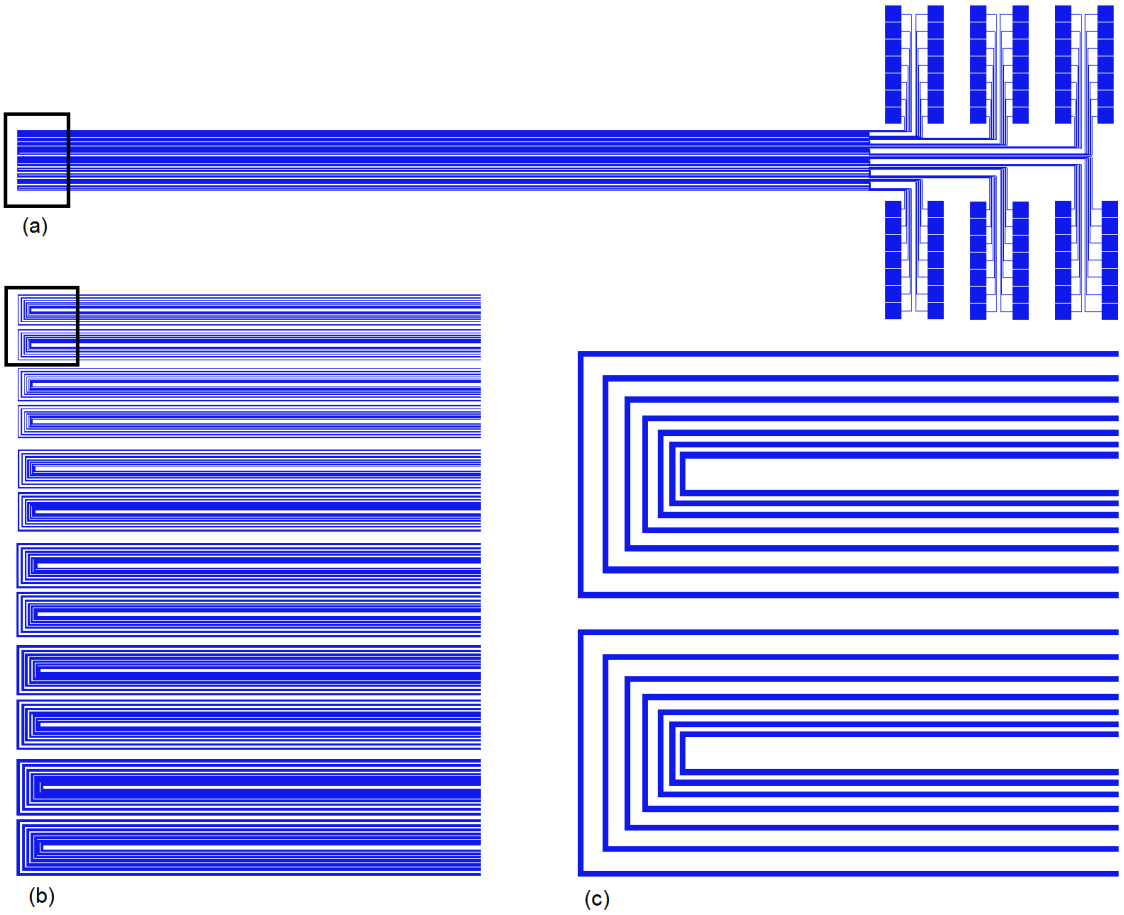


Figure 3.3: The mask design of the interconnects. The framed area in figure (a) is shown larger in figure (b). Likewise, the framed area in figure (b) is shown larger in figure (c). (a) shows the full interconnects, the bond-pads are located on the right. Each interconnect goes two times back and forth to the bond pad area. The width of the part where the connections go back and forth is $10mm$. (b) shows interconnects with ranging widths from $800nm$ to $3\mu m$. (c) shows spacings between the interconnects ranging form $800nm$ to $3\mu m$.

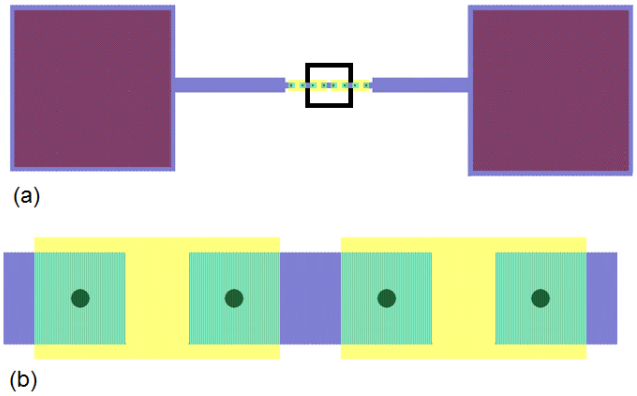


Figure 3.4: The mask design for one of the daisy chains. (a) shows two measurement pads (purple) connected by a daisy chain, the framed area is shown larger in (b). (b) shows a daisy chain to connect the top layer (blue) with the bottom layer (yellow) using contact holes.

3.3. Materials

For the fabrication of the test structures for the flexible MEMS devices the same materials are used as in the current F2R process to be compatible with the F2R process. The process starts with double sided polished silicon wafers, since these wafers are required for processing on both sides of the wafer. In this Section the used materials in the fabrication process are explained.

3.3.1. Silicon Oxide

In the fabrication of flexible interconnects silicon oxide is used for multiple applications. Silicon dioxide is an insulator which can be grown and deposited in several ways. Since polyimide has a good adhesion to oxide, first a layer of oxide is deposited on the silicon wafer. Beside this, oxide is used as hard mask for the backside etching of the silicon.

3.3.2. Silicon Carbide

Amorphous silicon carbide (a−SiC) is a material with a wide variety op application is semiconductor and MEMS technology. One novel application of SiC is as an adhesion improvement layer, since SiC is capable of forming chemical bond with some materials. During this project SiC is researched as an adhesion promotor.

Plasma-enhanced chemical vapor deposition

During this project *plasma-enhanced chemical vapor deposition* (PECVD) deposition is used. PECVD is a technique whereby using a plasma a thin layer of a material is deposited onto a solid substrate. Both silicon carbide and silicon oxide are deposited using PECVD. One reason PECVD is chosen because is it can be deposited at relative low temperatures. Furthermore, the stress in the film can be controlled and minimized by adjusting the deposition parameters. Low stress in the layer is important to prevent unwanted bending of the thin substrate. Another reason to choose PECVD is that it is found in earlier work that the adhesion between oxide and polyimide is superior when a PECVD instead of an other deposition technique for silicon oxide is used.

3.3.3. Polyimide

The flexible material for the interconnects is polyimide, this material is already discussed in Section 1.1.3. During the processing PI is spin coated on the wafer and cured in a nitrogen environment. For this project the same polyimide is used as in the F2R process flow. This polyimide is paternable using either dry etching or laser ablation techniques.

3.3.4. Aluminium

The main application of aluminium (Al) in the this process is as a electrical conductor. Additionally, aluminium is also used as a hard mark on PI in the last processing step. The process flow consist of the two metal aluminium layers. The first aluminium layer serves as the bottom layer for the contact holes and daisy chains. The second aluminium layer is the top layer for the contact holes and daisy chains, also, these layers are the flexible metal interconnect layer.

Physical Vapor Deposition

Aluminium or aluminium alloys can be deposited by *Physical Vapor Deposition* (PVD). PVD is a process where physically a material is transferred from a source to substrate. Hence, a thin layer is deposited on the surface of the wafer. The most common form of PVD is sputtering, this also used during this process. During the sputtering process atoms are ejected from a solid, and travel through the vacuum before they are deposited on the substrate[13].

Aluminum Alloys

Besides pure aluminium, aluminium alloys are also widely used in the IC and MEMS industry. For example the addition of Si to aluminium can prevent the problem of junction spiking at the interface of Si and Al [13]. This can happen since the solubility of silicon in aluminium can rise at high temperatures and thus at the Si-AL interface Si can dissolve in the solid and Al and creating junction spiking. Also small quantities of copper (Cu) can be added to Al to form the alloy Al:Cu, where 0.5-4wt% is common. In general the main reason to add copper to aluminium is to improve the electromigration resistance

[13]. Electromigration is the process where atoms in the metal lattice are displace due to the momentum transfer between the atoms and electrons.

The main reason that AlCu (instead of pure Al) is used in F2R is that AlCu bond pads can be made solderable using a process called ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold). However, a disadvantage of using AlCu instead of pure Al is that the resistivity of the alloy is higher. Furthermore, the dry etching of AlCu alloy can be more challenging compared to pure Al since the Copper compound is non-volatile in the Chlorine based plasma. Additionally, the post-etch corrosion is expected to be driven even more rapidly because Al and Cu can form a galvanic couple, this will be further explained in Chapter 4.

4

Dry etching of aluminum-copper

4.1. Introduction

One of the objectives of this work is the development of small pitch flexible interconnects for the next generation F2R platform. In the current F2R process these interconnects are fabricated from an AlCu layer and patterned using a wet PES etch. The disadvantage of this isotropic etch, is that it is not possible to fabricate small width interconnects. Furthermore, due to the isotropical character a significant amount of area is lost. A straightforward approach to improve the density of the interconnects is to use anisotropical dry etching instead of isotropic wet etching. Using a dry etch, both the interconnects can be fabricated with a smaller width and the area lost between the interconnects can be reduced. However, using dry etching can also introduce new challenges. For example the problem of post-etching corrosion can arise. Besides this, the effect of the RIE on the polyimide surface is unknown.

4.2. Dry etching of aluminum alloys

In the fabrication of MEMS devices and integrated circuits the etching of aluminum and aluminum alloys is a very important step, since the density of these devices is often dependent on the occupied area of the interconnects. Anisotropical etching permits a higher density of the interconnects, since smaller separation between the interconnects can be used. In F2R the pitch of the interconnects is limiting the density of the transducer elements. Therefore, using dry etching instead of wet etching is a logical step to increase the density of the interconnects and thus the density of the CMUTs.

For dry etching of aluminum (alloys) the etchant is chlorine based, since Cl reacts with aluminium, and the reaction product (mostly $AlCl_3$) is volatile. The problem of post-etch corrosion arises from the remaining Cl and Cl-containing residues. These residues can remain on the sidewalls or resist. When these residues absorb moisture (for example from the moisture in air) HCl is formed. HCl is highly corrosive to the Al. The reaction of HCl and Al forms $AlCl_3$, which continues the corrosion as long as moisture is available [14].

Freshly exposed aluminium etches relatively easy in a chlorine based plasma. However, if the surface is covered in a layer of (native) aluminum oxide the reaction will not start since Al_2O_3 does not react with Cl_2 or Cl. For this reason, the native oxide with a thickness of few nm has to be removed, this is done in the breakthrough step. This breakthrough step contains special chemistry to remove the native oxide with ion bombardment. After this step the main etch step etches the new exposed aluminum(-copper).

When Cu is added to aluminum the problem of post-etch corrosion can be even more severe. Since aluminum and Al-Cu compounds ($CuAl_2$) can form a galvanic couple the corrosion process can be driven even more rapidly [14, 15]. A galvanic couple occurs when two different metals are in contact with each other. To prevent post-etch corrosion, the Cl containing residues should be removed as quick as possible after the etch process. Cl residues can be removed by dissolving it in for example water.

4.3. Selectivity

Etch selectivity is an important figure of merit of an etching process. It gives the ratio between the etch rate of the target layer and an underlying layer or the mask layer. For most processes, a high selectivity is desired since then only the targeted layer is etched. The selectivity of aluminum on oxide during the etch process is known to be good. The selectivity to polyimide is unknown, but it is expected to be lower than the selectivity to oxide because polyimide is not as hard as oxide.

To determine the etch rate and selectivity towards oxide, polyimide and aluminium in a chlorine RIE etch, a experiment was conducted. A wafer with on top a layer of polyimide or oxide was etched for a fixed time. Afterwards the decrease in thickness of the layers and thus the etch rate was determined. The oxide thickness was determined using an optical measurement with the Nanospec measurement tool. The thickness of the polyimide layer was determined by measuring the height difference of a scratch made in the polyimide layer with the Dektak step height measurement tool. The etch rate of AlCu is measured using end point detection to determine the required etching time for a fixed thickness. During the etch endpoint detection (EPD) was used. This EPD determines by means of the optical spectrum measurement the status of the process and can detect an Endpoint (EP). Table 4.1 shows the result of the etch rate experiment and the resulting selectivity.

Table 4.1: Etch rate and selectivity in aluminium etch recipe

	Oxide	Polyimide	AlCu
Etch rate [nm/s]	1.1	4.0	9.3
Selectivity	8.5	2.3	n/a

4.4. Interconnects on Oxide

To reduce the complexity, first the interconnects are fabricated using only mask re-routing layer, on top of an oxide layer. The used mask is shown in Figure 3.3 and it contains the meandering interconnect test structures. The process flow used for the fabrication of the interconnects is shown in Appendix B.3. In Figure 4.1 the schematic process flow is shown, the sub-figures are explained below. First the silicon wafer is cleaned and alignment marks are etched in the silicon. Next, a layer of 700 nm AlCu (1wt% Cu) was sputtered on the wafer (Figure 4.1a). Then a layer of SPR660 photoresist was spin coated with a thickness of 1200 nm (Figure 4.1b). This resist was chosen because it is suitable for patterning small structures. Next using the wafer stepper (ASML stepper PAS5500/100) the photoresist was exposed with the mask and developed using a standard development recipe (Figure 4.1c). The energy of the exposure was determent using an energy-focus matrix. This means, that all dies are exposed with different energies and focus. After microscope inspection the best resulting die was chosen to obtain the best energy and focus. On some of the wafers the resist was baked at 125 °C. The advantages of an extra baking step is that the resist is more crosslinked and thus better resistant during the harsh chlorine etch. However, the disadvantage is that the resist reflows and the dimension control can deteriorate. Furthermore, the resist can be more difficult to strip after etching since it is more crosslinked.

After the lithography, the layer of AlCu with photoresist mask is etched on a STS CPX clustertool. Using EPD an endpoint can be detected. At this moment the most area of the layer is etched. After the EP the over-etch starts. During this phase the residues are etched. The occurrence of these residues is caused by the non-uniformity of the etch tool and a slightly lower etch-rate in and near small structures. 10% Over-etch time is common, and normally sufficient to remove the residues of the target layer (Figure 4.1d).

After the chlorine etch, anti-corrosion measures need to be taken to prevent post-etch corrosion. First in the same chamber as where the wafer is etched a H_2N_2 plasma treatment is performed. This is treatment is done without breaking the vacuum, thus the wafer does not see moisture which can cause the corrosion process to start. During this passivation step, the hydrogen ions absorb the Cl or Cl-

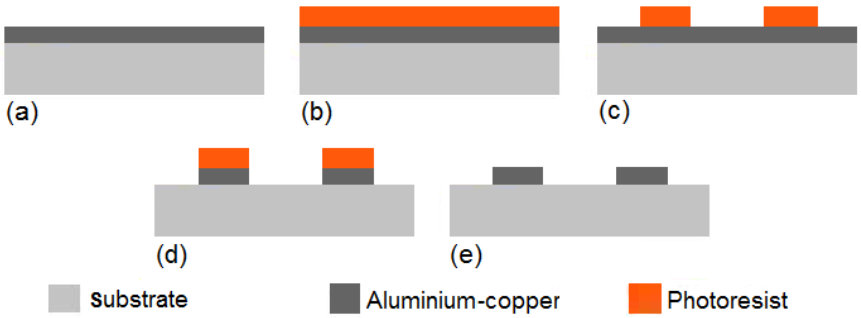


Figure 4.1: Schematic cross section of the regular etch process flow, the sub-figures are marked with a letter and are explained in the text.

containing residues from the wafer. After the passivation, the wafers are immersed in a DI water bath as soon as possible to absorb the remaining residues. The wafers are transported in the water bath to a rinse and dry tool. Because the AlCu can start corroding during the stay in the water bath, it is important that they are dried as fast as possible. Finally, the photoresist needs the be stripped. The resist can be stripped using either an oxygen plasma or a NMP based wet stripper microstrip (Microstrip 5010 Fujifilm) (Figure 4.1e).

4.4.1. Results and discussion

The process flow described in Appendix B.3 is performed to experiment with the interconnects on oxide. The optimal energy of the stepper exposure was determined to be 250 m J cm^{-2} with a focus of zero. A SEM image of the patterned resist before the post-exposure bake is shown in Figure 4.2. The resist looks properly patterned. The baking step only results in a minor reflow, the interconnects widen very little. The width is measured using the SEM, the 0.8 µm interconnects are before the bake approximately 780 nm and after the bake 820 nm. Both interconnect widths hardly differ from the designed width.

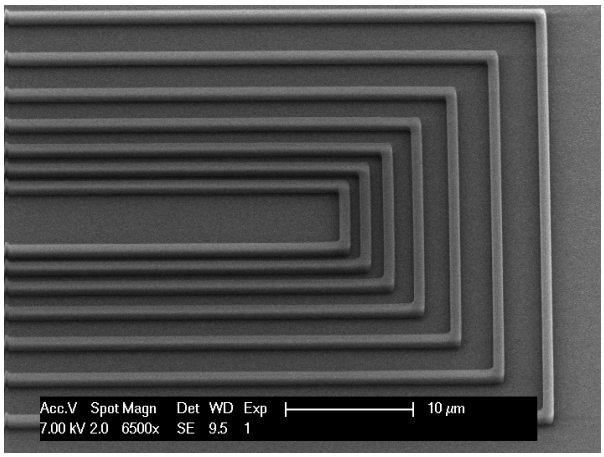
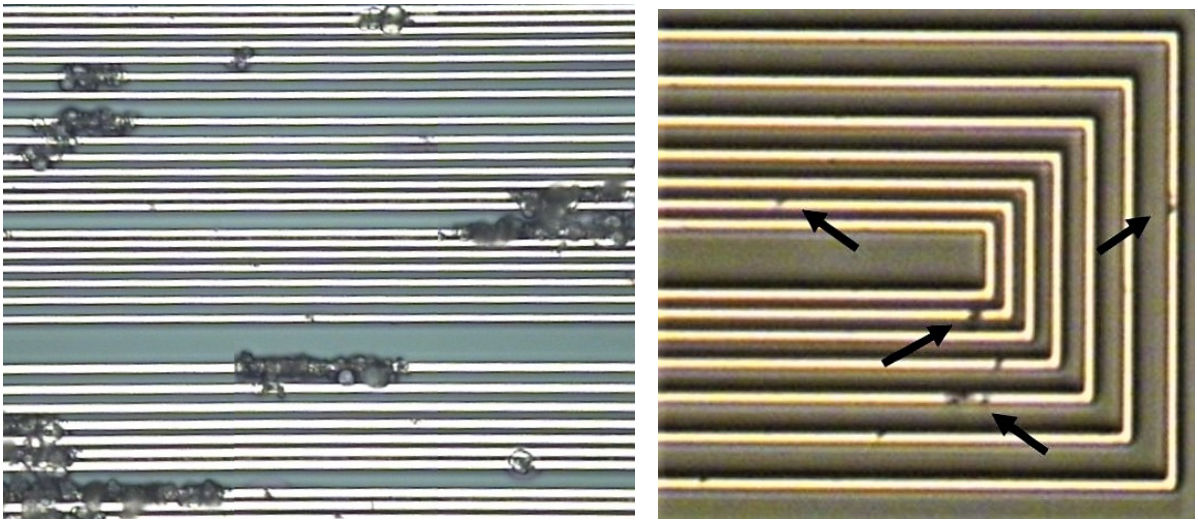


Figure 4.2: Patterned photoresist on top of the AlCu layer.

During the etching a clear endpoint was observed, after which an approximately 10% over-etch was used. The first attempt of etching AlCu did not include a water bath directly after the etching. This resulted in severe corrosion (Figure 4.3a). The corrosion increases over time, after a day the corrosion was more intense. Apparently, a H_2N_2 passivation done is insufficient in removing the Cl residues, since, the remaining Cl results in severe corrosion, which increases over time.

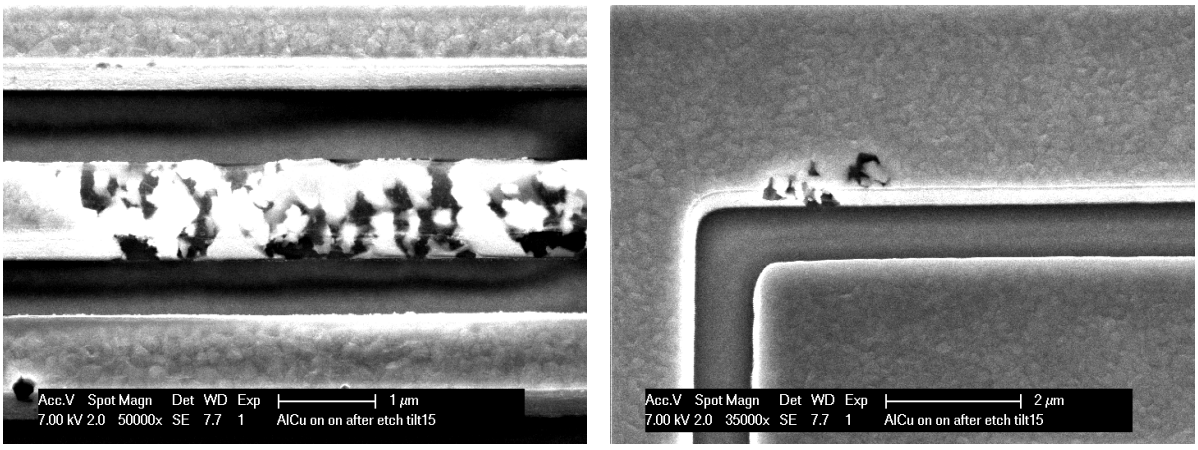
The results are significantly better when the water immersion is performed directly after the dry etching step. However, on some places on the interconnects so called 'mouse bites' occur. These are places



(a) (b)

Figure 4.3: Aluminum-copper interconnects with (a) severe corrosion (b) 'mouse bites'.

where the aluminum is eaten away. This is shown in Figure 4.3b and in more detail in Figure 4.4. These 'mouse bites' only occur on the wafer which did not have a post-exposure bake. These mouse bites occur because the photoresist is heavily eroded [16]. A non baked photoresist is apparently not sufficiently resistant to the attack of the plasma. As a results on some places the interconnects are exposed to the plasma and partially removed. Electrical resistance measurements show that most interconnects which have 'mouse bites' are not conducting, only for some of the wider interconnects there is a conductance.



(a) (b)

Figure 4.4: SEM image of 'mouse bites' in a (a) low width interconnect (b) relative high width interconnect.

The wafer where all anti-corrosion measures were taken (H2N2 treatment, quick rinse and dry and a photoresist post-exposure bake) showed corrosion free interconnects. Due to the passivation step and rinse the Cl residues are removed and the bake toughens the resist to withstand the harsh chlorine plasma. A microscope image of the resulting interconnects on oxide is shown in Figure 4.5. This exact process flow was reproduced three times to ensure that the process is reliable for the fabrication of aluminum-copper interconnect. Two out of the three attempts gave the same good results. However, during one attempt, after the dry etching the wafer was put too long in the water bath after due to logistic problems. The wafer was in the water bath for approximately eight minutes instead of one. This re-

sulted in some corrosion of the interconnects. In literature it is also observed that AlCu starts corroding after a too long contact with DI water [15].

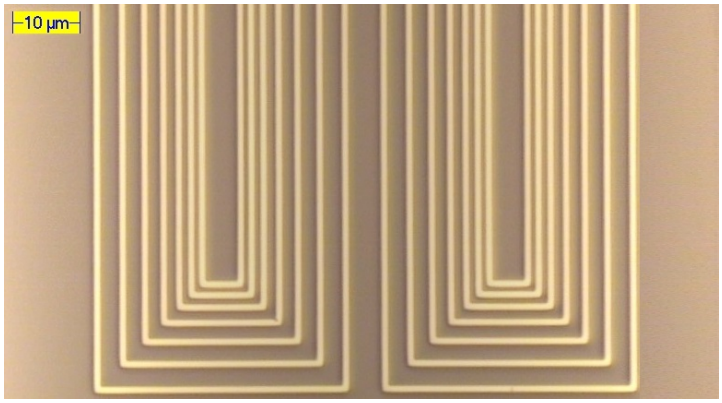


Figure 4.5: Image of the aluminum interconnects on oxide without corrosion.

Electrical resistance measurement confirms the successful fabrication of the interconnects. The resistance was measured by placing probing needles on the bond-pads and measure the resistance using a multi-meter (keithley 2700). On the wafers where corrosion was observed, some of the interconnects had a very high resistance, or no connection at all. However, on the wafers where the correct post-etch corrosion prevention measures were taken, all the interconnects had a resistance as expected. The average resistance of the interconnects as function of the width of the interconnects is shown in Figure 4.6. The resistance matches very well with calculated resistance values based on the resistivity of AlCu 1wt% ($2.74 \cdot 10^8 \Omega m$ at $293^\circ C$ [17]) and the geometry of the interconnects. The figure also includes the stand deviation of the measurements plotted as error-bars.

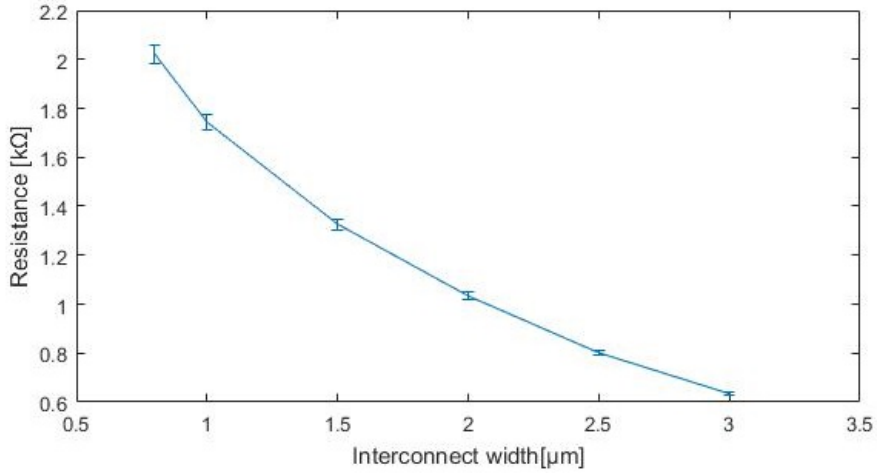


Figure 4.6: Plot of the average resistance of the interconnects versus the width, including the standard deviation plotted as error-bar.

From the measurement data a significant difference has been observed in resistance between equal width but different pitch (distance until neighbouring interconnects). Therefore the standard deviation was calculated separately for each set of measurements with equal width and pitch. Figure 4.7 shows the resistance versus the pitch of the interconnects for different interconnect widths. The resistance clearly decreases for a increasing pitch. This could either mean that the interconnects are thinner due to influences in the fabrication process, or because of the difference in length of these interconnects. Measurements of the width of the interconnects in the SEM do not show differences for the different pitch interconnects, thus the first hypothesis can be falsified. In the mask design there is small dif-

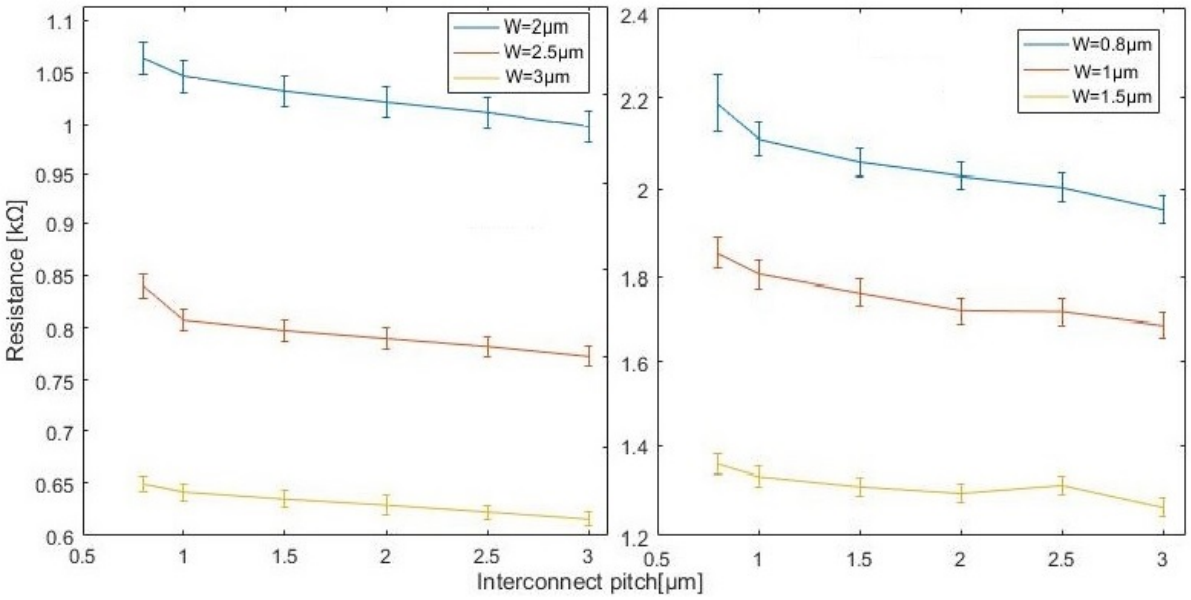


Figure 4.7: The resistance as function of the pitch (distance until neighbouring interconnect) for different width interconnects including the standard deviation as error-bars.

ference in patch length due to the placing of the bond-pads, the difference between the longest and shortest interconnects is 5.8 %. The difference of between the highest and smallest pitch is between 5 % and 8 %. Taken into account the standard deviation, it is very likely the difference in resistance is caused by the difference in length of the interconnect. The Figure also shows that the absolute standard deviation is larger for the smaller width interconnects. However, the normalized deviation is very similar for all type interconnects. This means that the deviation is primarily not caused by measurement error but more likely by a physical deviation in the process.

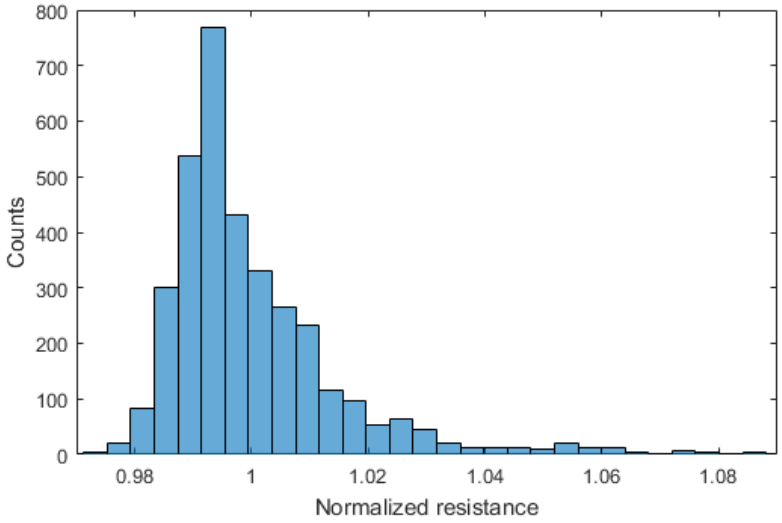


Figure 4.8: A histogram of the normalized resistance values of all the interconnects on one wafer.

To learn more about the distribution of the resistance values of the fabricated interconnects a histogram was plotted. Figure 4.8 depicts this histogram of the normalized measurement data of all the interconnects on one wafer. The distribution has the characteristic of a skewed normal distribution since the mode is lower then the mean (normalized mode=0.993) and the distribution is non-symmetrical. This means that is more likely that the resistance of an interconnect is higher than the mode. Furthermore,

there are more interconnects with a resistance lower than the average, however, the deviation of average of the interconnects with a higher resistance is on average larger. This means that it is more likely that there is more metal removed from the interconnect with respect to the mode, than that less metal is removed. This can be explained by very small amounts of local corrosion which can cause the removal of conducting material and thus the resistance to increase. On the other hand, there is no physical counterpart of corrosion which does decrease the resistance of the interconnects. This causes the non-symmetric skewed distribution.

4.4.2. Conclusion

It is found that using 1.2 µm SPR660 resist in combination with a post-exposure bake a good mask for the dry etching of the interconnects can be fabricated. With a chlorine based plasma the AlCu is properly etched after a 10 % over-etch. To prevent post-etch corrosion an H_2N_2 treatment was done to absorb Cl residues, after which immediately the water immersion and drying step was performed. Using this process flow consistently corrosion free high density interconnects can be fabricated on oxide. The resistance of the interconnects is in accordance with the expected value, moreover, the pitch does not effect on the resistance per length of the interconnect.

4.5. Two step etch process

As alternative to the regular AlCu etch process (explained in Section 4.2), a 2-step etch process has been researched. This 2-step process starts with double thickness AlCu layer, which is first etched halfway with a photoresist mask. Next, the resist is stripped, then the aluminum is etched further while masking itself. The result should be similar to the normal etch process. However, there are some possible advantages because the resist is stripped halfway during the etch. As explained the resist is known to absorb some of the chlorine during the etch, which can cause post-etch corrosion. Instead of trying to remove the Cl residues from the resist, the resist is removed completely with an oxygen plasma in between the two steps of the 2-step process without breaking the vacuum and exposing the wafer to moisture. Furthermore, when AlCu is etched on PI instead of oxide, stripping the resist can be more challenging, since an oxygen plasma cannot be used anymore. An disadvantage of the 2-step process is that the non-uniformity of the RIE tool has direct effects on the non-uniformity of the thickness of the interconnects over the wafer. Normally, the over-etch compensates for the non-uniformity of the dry etch tool, however, due the nature of the 2-step process, the non-uniformity will have effect on the non-uniformity of the interconnects over the wafer.

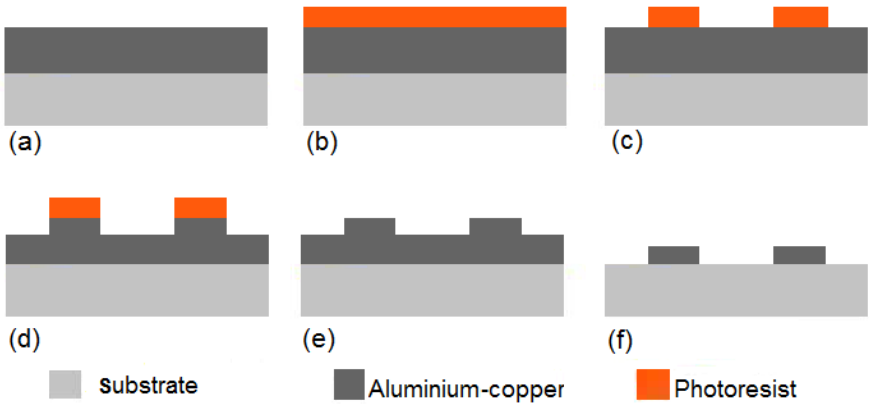
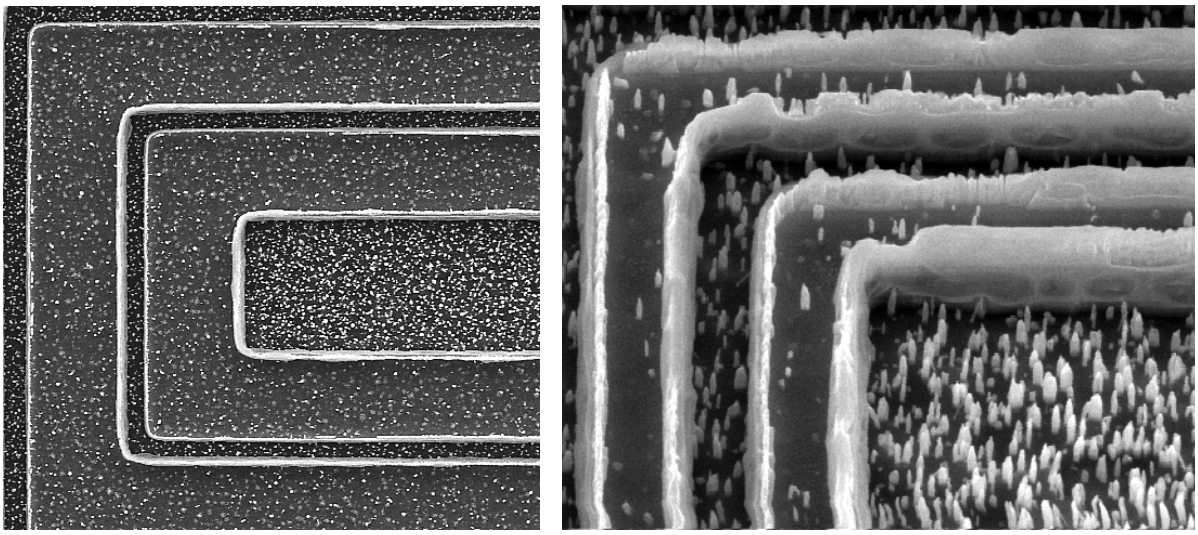


Figure 4.9: Schematic cross section of the two-step etch process flow, the sub-figures are marked with a letter and are explained in the text bellow.

The process flow is shown in Figure 4.9. The process start with a layer of AlCu of double thickness (1400 nm) on oxide (or eventually polyimide) (Figure 4.9a). Then a layer of SPR resist is spin coated (Figure 4.9b) and patterned using lithography (Figure 4.9c), similar as in the regular AlCu etch process. Next, the layer of AlCu is etched approximately halfway time based (Figure 4.9d). Subsequently, the

resist is stripped in the same machine using an isotropical oxygen plasma (Figure 4.9e). Finally, the layer of AlCu is etched further until the endpoint is reached and with an over-etch of 10 %. The exact process flow is described in Appendix B.4.

The 2-step process flow resulted in unexpected results. Although the 2-step etch with a resist strip in between was successful in fabricating the interconnects, grass-like structures were observed on the oxide and the interconnects. A SEM image of the interconnects with grass-like structures is shown in Figure 4.10. The pillars grow both on the interconnects and on the oxide, however the density of the pillars is higher on the oxide. The grass-like structures are most likely caused by a micromasking effect. Some micro particles, inside or on top of the AlCu layer start to mask the AlCu during the etch which result in micro pillars. The difference in density suggests that formation of the pillars starts both during the first and second etch stage. This means that the micromasking is most likely caused not only by something on top of the metal layer. The difference in height of the pillars also indicates that the micromasking is caused by something in the AlCu layer. Figure 4.10b shows a SEM image where the micromasking on the sides of the interconnects is shown. The edge of the interconnects has a very high density of pillars. This high density is probably caused by something masking the sidewall created in the first etch step of the process. This is not necessarily caused by the same effect as the other grass-like structures.



(a) (b)

Figure 4.10: 2step process interconnects with micromasking

Besides the micromasking effect, another disadvantage of the 2-step process is the non-uniformity of the process over the wafer. It was already expected that this would have an effect on the height of the interconnects, but the impact was larger than expected. The height difference was approximately 200 nm, while in the middle the height was around 600 nm. On the edges of the wafer, where the etching is faster, the height was only 400 nm.

4.5.1. Micromasking

Since the micromasking is not fully understood, the effect was further researched. On wafer where the interconnects are patterned using the regular echt process this micromasking effect is not observed. The two main differences are the method of masking, and the AlCu layer thickness. The micromasking possibly happens in the first etch stage, but definitely in the second stage. During the second stage, the wafer is etched everywhere, in fact there is no mask present. To simulate this last etch step, a bare AlCu wafer was etched. Both 700 nm as in the regular process and 1400 nm as in the 2-step process were used. Furthermore, also a 1000 nm AlCu wafer was used. For all wafers the etching was stopped just before the expected endpoint (based on the etch rate). Additionally, one 700 nm was fully

etched with a 10 % over-etch. The SEM images of the results are shown in Figure 4.11. From these images it is clear that the micromasking occurs on all wafers. Apparently, the thickness of the AlCu layer does directly effect the grass-like structures. However, the height of the micro-pillars seem to be proportional with the thickness of the layer. Moreover, these structures are both existent before and after the endpoint of the etch, but the height and sharpness of residues decreased.

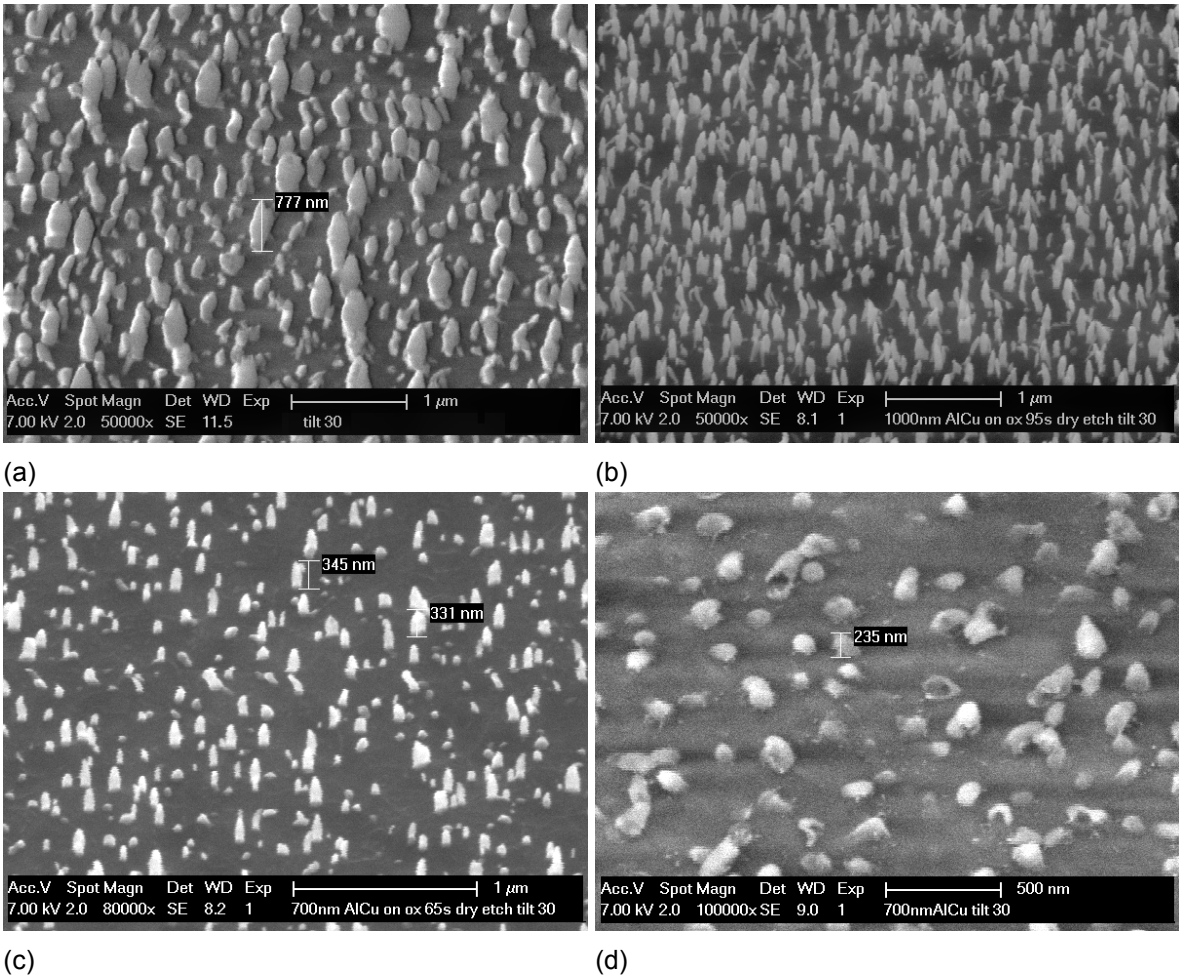


Figure 4.11: SEM image of micromasking in AlCu on a wafer with (a) 1400 nm AlCu stopped before endpoint (b) 1000 nm AlCu stopped before endpoint (c) 700 nm AlCu stopped before endpoint (d) 700 nm AlCu 10 % over-etch.

If Figure 4.11d is compared with the regular etch process, the only difference is the masking. Instead of a photoresist mask, no mask is used. Hence also the area where AlCu is etched is different. Since the micromasking occurred on all wafers where AlCu was etched without a mask, it raises the question whether the etching of pure aluminium would also also show micromasking. Therefore an experiment was conducted on a wafer with 1 µm of pure Al without a mask. A SEM image of the result is shown in Figure 4.12. The inspection of this wafer with pure Al showed that no grass like structures. This means that copper addition in aluminium causes the micromasking, but only when no masking is used. The cause of the micromasking effect is likely a non-volatile copper compound in the alloy which is not etched during the RIE. If aluminum-copper is deposited at higher temperatures non-volatile precipitates can start forming [18]. If the precipitates are becoming larger they cannot be removed by the chlorine plasma and thus create micromasking. When no masking is used a larger area of metal is etched, as a result the etch is less capable of removing particles which cause micromasking. The problem of micromasking could possibly be solved by optimizing the etch recipe for a larger open area, or AlCu optimizing the AlCu deposition process.

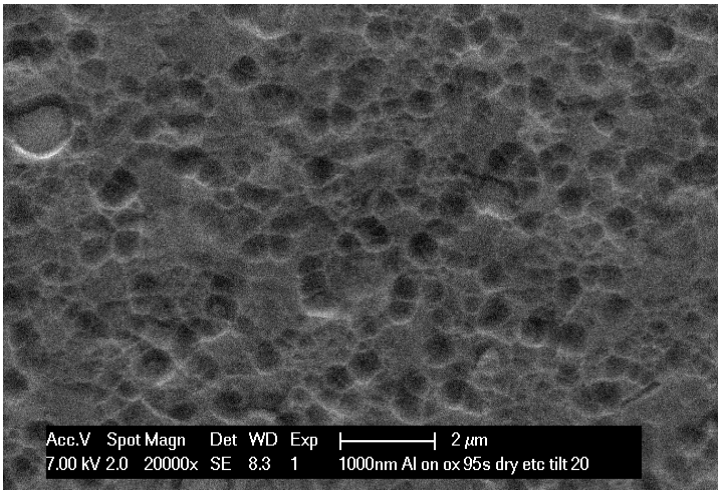
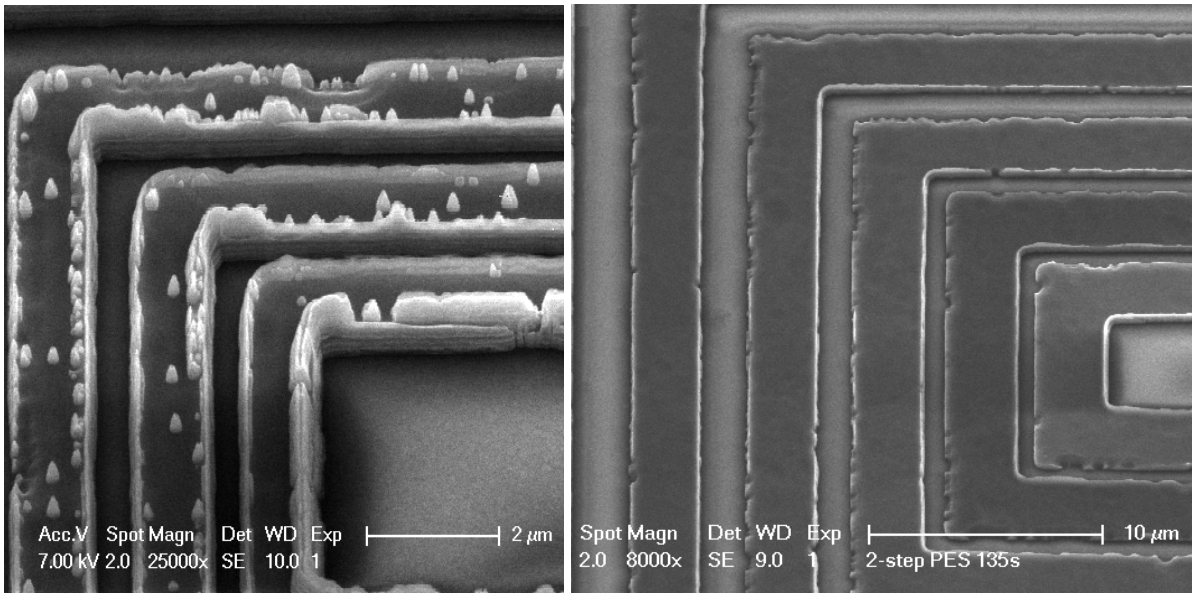


Figure 4.12: A SEM image of an etched (95 s) layer of 1 µm pure Al. The roughness is caused by the grain in the aluminum. No grass like structures are observed.

4.5.2. 2-step process with aluminium

Since the copper content in the AlCu is the reason of the micromasking, the 2-step process should theoretical work with pure aluminium instead of AlCu. Although pure aluminium is not desirable in the F2R flow since AlCu is required for the ENEPIG deposition (see Chapter 3), the principle of the 2-step process could be demonstrated using pure Al. Therefore, the process flow for the 2-step process was performed again, but then with Al instead of AlCu. The result in Figure 4.13a show that with pure aluminum there is apparently still a micromasking effect, however, only on top of the interconnects these grass-like structures occur. Therefore, the micromasking here has a different cause than the micromasking on the blanked AlCu wafers. It originated either from resist residues or sidewall passivation or both. This also proves that the micromasking during the 2-step AlCu etching was caused by multiple origins.



(a) (b)

Figure 4.13: (a) Interconnects fabricated using the 2step process with pure aluminium (b) after an additional PES etch of 135 s

An attempt was made to remove the sharp pillars caused by micromasking using an isotropical wet PES etch. Since the pillars have a relative large surface area they should etch relative fast in a isotropical etch. After 135 s the pillars on top of the sidewalls were removed. However, a lot of the metal from the sidewalls was also etched away. An image of the interconnects after the PES etch is shown in Figure 4.13b. Electrical resistance measurements showed that all interconnects were conducting and no short-circuits were measured. However, the resistance was two till four times as high as calculated, depending on the location on the wafer of the interconnect.

4.5.3. Conclusion

The 2-step etching process is experimentally confirmed, working interconnects have been demonstrated. However, there are a lot of disadvantages of the 2-step process compared to the regular process. First the non-uniformity over the wafer is very high. The etching without masking AlCu causes micromasking. Besides, using pure Al it is showed that the process causes micromasking by itself on top of the interconnects. Furthermore, the process is less reproducible since variations in the etch-rate (over time and over space) have direct effect on the height of the interconnects. Hence, the regular process is a more suitable method for fabricating the interconnects.

4.6. Interconnects on Polyimide

Since the rerouting AlCu layer is deposited on polyimide to fabricate flexible interconnects sandwiched between polyimide, the next step was to experiment with AlCu etching on PI. For this experimental fabrication a similar process as the regular process on oxide was used. The process flow is shown in Appendix B.5. First, polyimide is spin-coated on an oxide wafer, and cured in a N2 environment at 275 °C. Next, a layer of 700 nm AlCu is deposited using sputtering. The same lithography is used as for the regular process on oxide.

4.6.1. Results and discussion

To dry etch the AlCu on polyimide the same Cl based recipe is used as during the etch on oxide. An over-etch of 10 % was performed after the end point was observed. After the plasma etching the same anti-corrosion measures were taken as after etching on oxide. Finally, the photoresist was stripped in microstrip. Microstrip is a heated NMP based resist stripper which does not attacks cured polyimide. A microscope image of the dry etched lines on polyimide is shown in Figure 4.14. Most interconnects are properly patterned, however, the interconnects with a small gap between them have some residues in between the interconnects. These residues are most likely AlCu that is not properly etched. A similar observation is made from the SEM images depicted in Figure 4.15. The SEM images give a better view of the residues in between the lines. An electrical measurement confirmed that there was still metal between the lines, since a lot of short-circuits were measured between the small pitch interconnects.

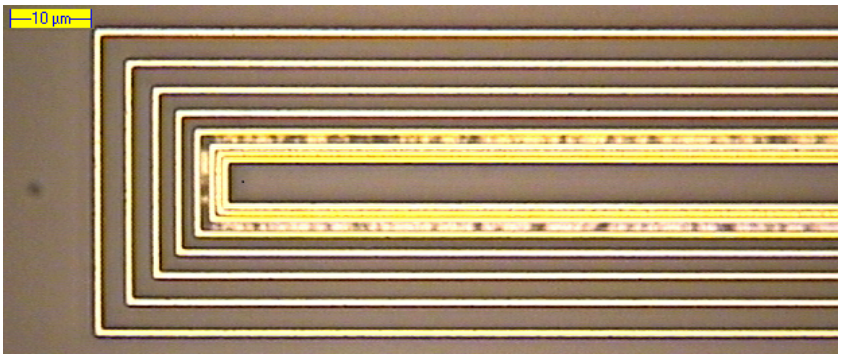
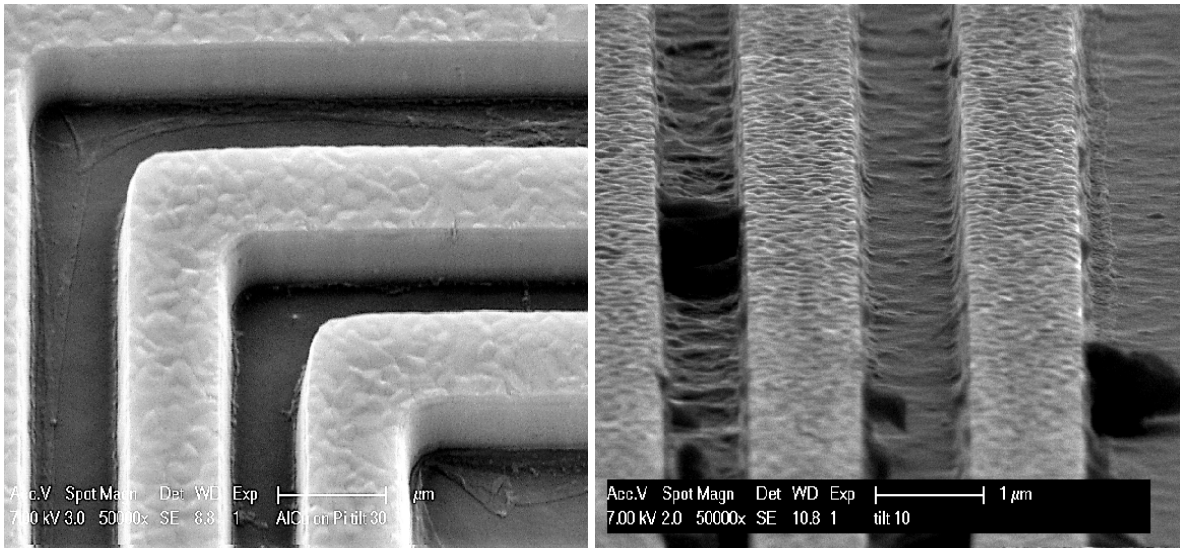


Figure 4.14: Dry etched AlCu on PI with residues between small pitch interconnects.

A solution was found in increasing the over-etch. First a 20 % over-etch was used, but this was still insufficient in removing all residues between the interconnect. An over-etch of 30 % was found to be sufficient. No residues or short-circuits were observed using this long over-etch. A cause of the

necessity of the long over-etch could be that polyimide is a relatively soft material. Hence, during the sputtering some of the aluminium is sputtered under the surface of the polyimide. In combination with that the etch rate in very small structures is lower than on larger places [14], as a result a longer over-etch is needed. Another possibility is the higher thermal resistance of polyimide layer which might result in a different etch behavior. During this over-etch the top of the surface of polyimide (max. 100 nm) is removed. Furthermore, the effectiveness of the anti-corrosion measures is showed again, even on polyimide, since there was no corrosion observed.



(a) (b)

Figure 4.15: Dry etched AlCu on top of PI with residues between the interconnects (a) view under an angle (b) cross-section (the big chunks are caused by the cleaving of the wafer).

Originally it was expected that the polyimide would show a similar uptake of chlorine as resist and thus that the corrosion problem of interconnects on polyimide would be even worse than on silicon oxide. However, since no corrosion was observed, either the polyimide is less prone to chlorine uptake, or the anti-corrosion measures are proven to be very effective.

Electrical resistance measurements give measurement result very similar to the result of the interconnects on oxide. No interconnects were measured with a resistance with a significant deviation ($< 3\sigma$) compared to the results from Section 4.4. However, the amount of measurement was limited to 10 dies on two wafers. Due to the deviation of the resistance of the interconnects it is difficult to accurately compare the data of the measurements of the interconnects on oxide to interconnects on polyimide.

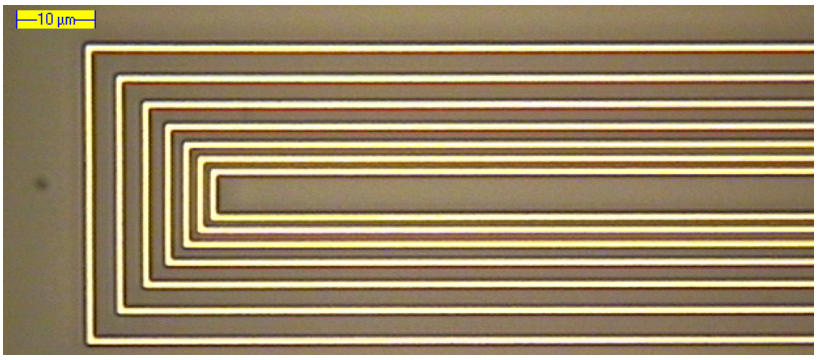


Figure 4.16: Dry etched AlCu on PI with a 30 % over-etch.

4.7. Conclusion

In this Chapter it is demonstrated that high-density interconnects can be fabricated both on oxide and polyimide using dry etching. A chlorine based plasma etches the AlCu, but can also cause post-etch corrosion. Post-etch corrosion and 'mouse bites' can be fully prevented by using a post-exposure bake, hydrogen passivation and directly rinsing the wafers after they leave the machine. It is shown repeatedly that when all these anti-corrosion measures are taken, corrosion can be prevented, both when the interconnects are fabricated on oxide or on polyimide. To properly pattern small pitch interconnects on polyimide an over-etch of at least 30 % is required, otherwise the surface of the polyimide between the interconnects still contains conducting metal residues. Furthermore, a 2-step etching process, where AlCu masks itself, is experimentally showed. However, major drawbacks are micromasking and poor uniformity.

5

Fabrication of small pitch contact holes

For the fabrication of the next generation F2R technology platform, one of objectives is to fabricate small pitch contact holes to electrically connect the top metal layer on the silicon wafer to the rerouting metal layer sandwiched between the PI layers. In the current F2R technology the vias have a diameter of 6 µm. The objective is to fabricate vias with a diameter of 3 µm. The mask design for the vias and the daisy chains is showed in Section 3.2. In this Chapter the experimental fabrication of the contact holes and daisy chains is explained, demonstrated and discussed.

5.1. Fabrication of contact holes

The contact holes are fabricated by dry etching a circular hole in polyimide. Then the hole is filled with metal by means of AlCu sputtering. To properly fill the hole and achieve a good step coverage, the hole should be tapered [19, 20]. A high aspect ratio via, with vertical sidewalls will have a poor metal coverage. This is because the deposition rate at the top of a trench is higher compared to at the bottom of the trench. If metal is deposited around or at the top corner of the trench, atoms are blocked and thus no atoms are deposited in the bottom corner of the trench, resulting in a poor or no coverage. A cross-section of a via with a poor coverage is shown in Figure 5.1.

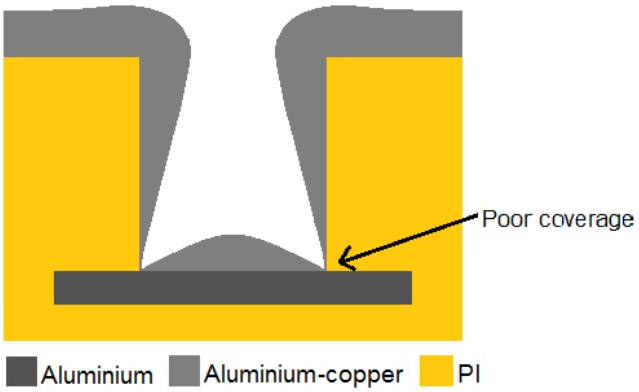


Figure 5.1: A sputtered non-tapered high aspect ratio via with poor metal coverage.

The schematic process flow is shown in Figure 5.2. First Al or AlCu is deposited and patterned using wet or dry etching, then the polyimide is spin-coated and cured. Next a suitable photoresist is spin-coated (Figure 5.2a). The resist is pattered using lithography (Figure 5.2b). This is followed by a post exposure bake to reflow the resist (Figure 5.2c). This reflow is necessary to create a tapering in the resist, which is transferred to the polyimide by means of dry etching. The next step is the etching of the polyimide (Figure 5.2d). In this etch the polyimide and the resist are both etched in an oxygen plasma, with approximately the same etch-rate. After the etch, the remaining resist is stripped in microstrip (Figure 5.2e). Finally, the hole is filled by sputtering metal (Figure 5.2f). The bottom and top metal layers are electrically connected through the via.

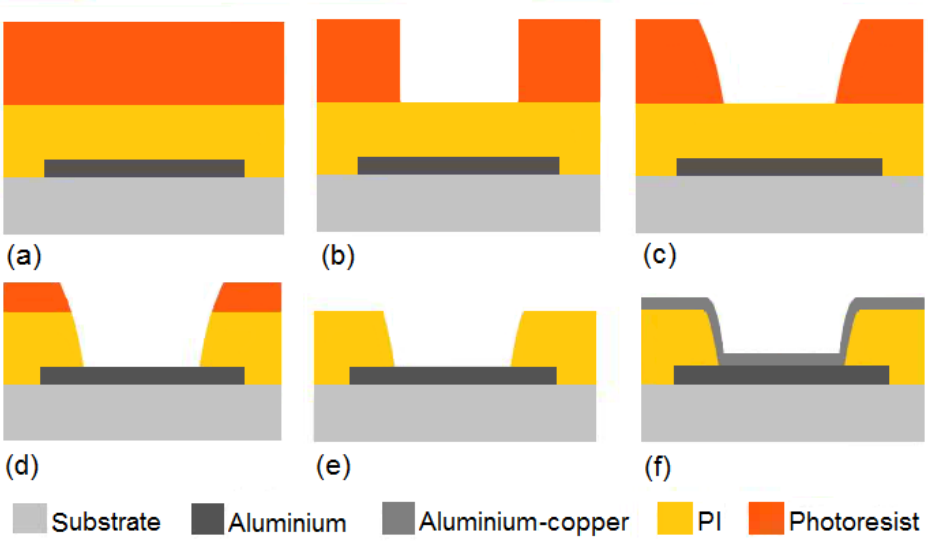


Figure 5.2: Schematic steps of the fabrication of contact holes in a PI layer.

The main challenge is to fabricate small pitch contact holes with a suitable taper. A sidewall slope of around 10 % is sufficient for good metal coverage over sputtering. Small holes with straight side walls could be easily be fabricated with a hard mask. To obtain a good step coverage of the sputtered metal the most convenient way is to have non-straight sidewalls. This can be achieved by making the RIE more isotropical. For example starting with an isotropical etch and during the etch changing to a fully anisotropical etch to create a so called 'wine glass' shaped via [22]. The downside of such a method is that more area is lost and thus the density of the vias will be smaller. Another method is using a reflow of the resist.

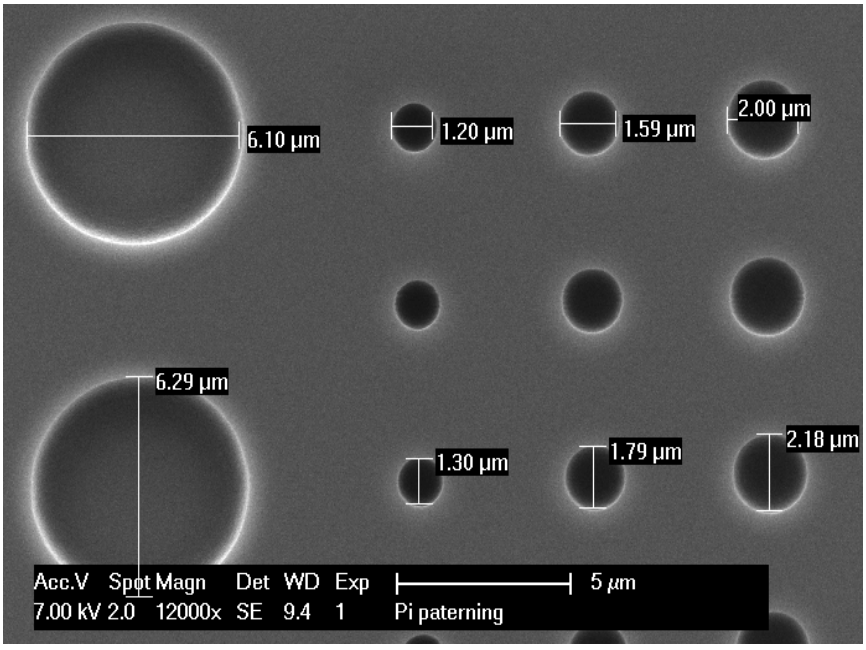


Figure 5.3: A SEM image of the HPR504 resist exposed with energy 80 m J cm^{-2} (Pt coated).

Two available and possibly suitable photo resists were HPR504 2.4 µm and AZ4533 3.9 µm. The HRP resist is better suitable for patterning small structures compared to the AZ resist, however the resist is relatively thin. The etch-rate of both resist was measured to be approximate 1.1 µm/min, slightly higher

than the etch-rate of polyimide. In a first attempt, the HPR resist was used. The resist was spin coated on the polyimide layer. Next, an energy-focus matrix was used to determine the energy and focus. To inspect the patterned resist on top of polyimide one wafer was sputtered with a thin layer of platinum (5 nm) to obtain a better SEM image. It was found that a low dose (80 m J cm^{-2}) gives the best result since the hole is the smallest and it is still properly patterned. A SEM image of the patterned hole in the resist is shown in Figure 5.3. The holes are only a few nm larger than the holes in the mask, and thus still very small. At this stage, the size is well-controlled, however, the size of the holes will change during the reflow and etching.

A post-exposure bake was performed to reflow the resist, by putting the wafers in an oven for 30 minutes at 125 °C. The next step is to etch the polyimide. The challenge in this step is to determine the endpoint. A proper endpoint detection is not possible during this etch because both the photoresist and the polyimide are detected, hence, an endpoint is only detected when all polyimide and resist is etched. Since the etch rate of polyimide in an oxygen plasma is known to be approximately 1 µm/min, the etch time has been estimated at 150 s. The result after the etch and stripping of the residual resist is shown in Figure 5.4.

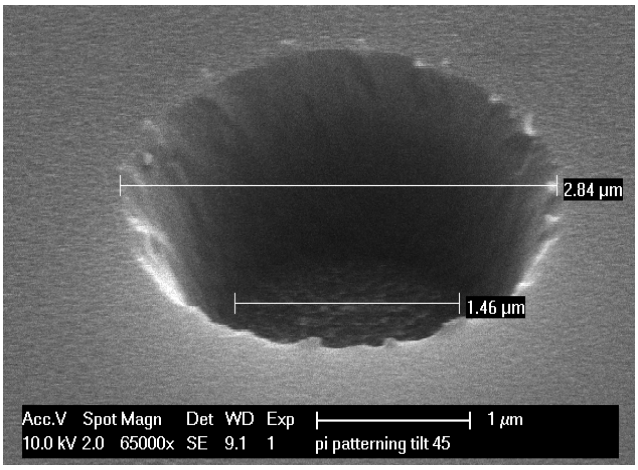


Figure 5.4: A SEM image of the etched contact hole with using HPR resist (Pt coated).

The hole is still small and with a slope in the sidewall. However, the bottom of the via does not look like the etch has landed on aluminum. A Dektek height measurement was performed to measure how much polyimide has been etched away. An scratch in the polyimide and a patterned area were measured to measure respectively the left-over polyimide thickness and height of the vias. This resulted in respectively 1.7 µm and 1.4 µm height differences. This means that on one hand the polyimide layer has been thinned down during the etch because the resist was gone, while on the other hand the polyimide has not been fully etched at the bottom. It appeared that the via was not completely opened. Apparently the polyimide etched significantly slower in these contact holes than expected. This can be explained by an effect called *aspect-rate dependence* (ARDE). This phenomenon refers to the tendency of small vias or openings to etch more slowly then in larger areas [14]. The result means that a thicker resist has to be used in combination with a longer etch. The 3.9 µm AZ4533 is therefore better suited.

Since it was found that a thicker resist was required to fabricate vias with the height of the full thickness of the original polyimide, the AZ4533 resist was used. An energy-focus matrix was used for the stepper exposure. After the exposure a reflow step was done. The wafer was cleaved into parts, that were baked at 105 °C, 115 °C and 125 °C for half an hour, in combinations with different energies and focuses. After the post-exposure bake all the samples were coated with Pt and inspected using the SEM. It was found that high energy did not allow for a good reflow, also the holes were larger than desired. The bake at 105 °C resulted in barely any reflow, 115 °C resulted in a small reflow, with some slope of the sidewall, the reflow at 125 °C resulted in a large reflow, more than required for a good coverage. The best result was found with a bake at 115 °C and an energy of 60 m J cm^{-2} (and zero focus). A SEM

image is shown in Figure 5.5.

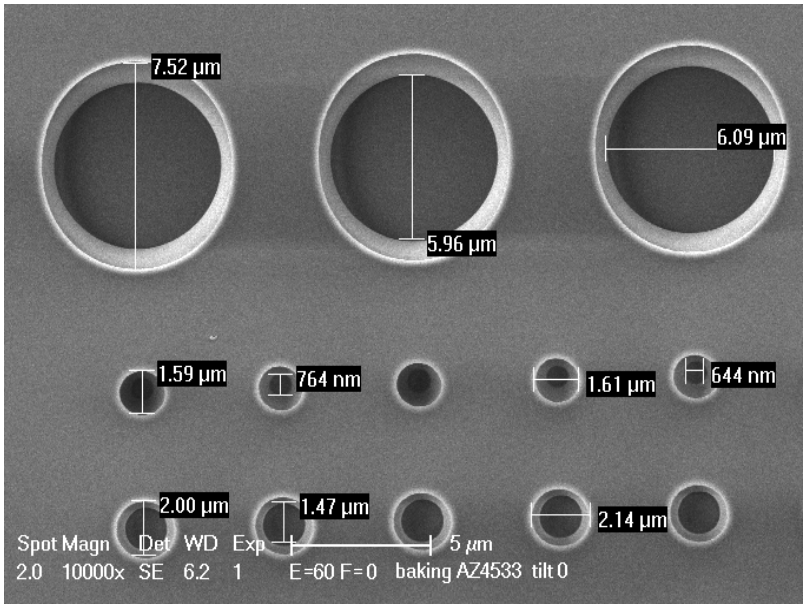


Figure 5.5: A SEM image of the patterned and reflowed (at 115 °C) AZ5344 resist (Pt coated).

After the resist type and thickness, energy, focus and reflow temperature were found, new wafers were prepared using these conditions. A longer etch was required, therefore one wafer was etched for 180 s and another for 210 s. On the wafer etched for 210 s there was no resist remaining, and thus the polyimide was eroded. During the etch a endpoint was detected around 200 s, this was probably the moment when the resist was gone. The result of the wafer etched for 210 s is shown in Figure 5.7. Because the resist was gone after a certain time, the polyimide around the vias was also etched. Due to this etching veil like residues around the top of the via were formed. It is assumed that this is a kind of micromasking effect. The wafer etched for 180 s had still resist left on the wafer protecting the polyimide, and resulted in properly etched contact holes (Figure 5.6). The sidewalls are sufficiently sloped with a tapering of 18°. Using the SEM, the aluminum grains are visible at the bottom of the hole, hence the via is fully etched. Only in the middle of the hole there is possibly some polyimide left, hence the etch should be a few seconds longer. However, it has to be noticed that the etch-rate is slightly variable depending on the time and machine and the condition of the machine. Hence in future work the etch time should be determined again. Figures 5.6 and 5.7 show that the slope and shape of the sidewall for different size vias is very similar. Calculations show that there is no significant change in the angle of the slope.

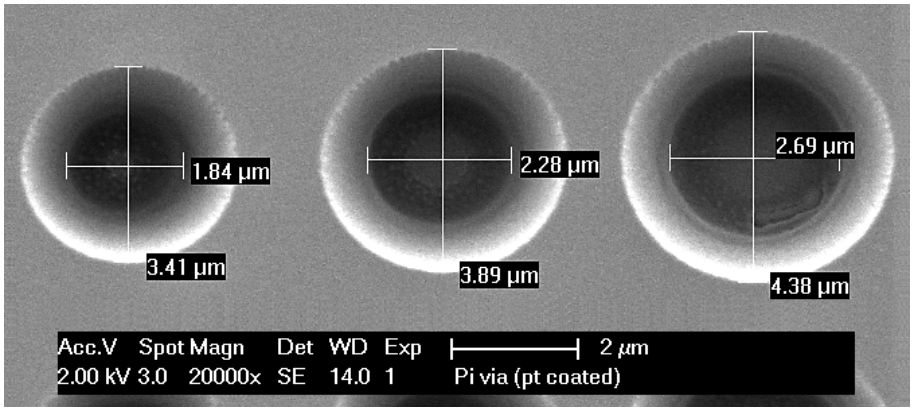


Figure 5.6: A SEM image of the etched (180s etched) contact hole with using AZ5344 resist (Pt coated).

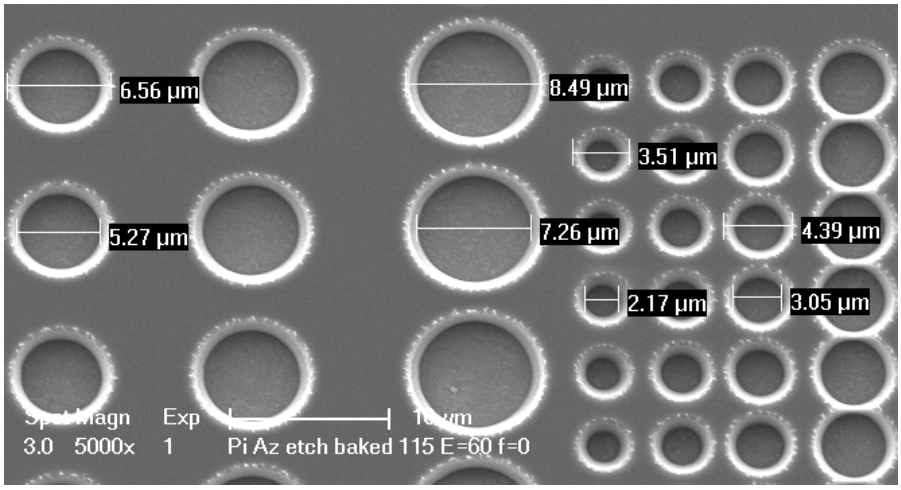
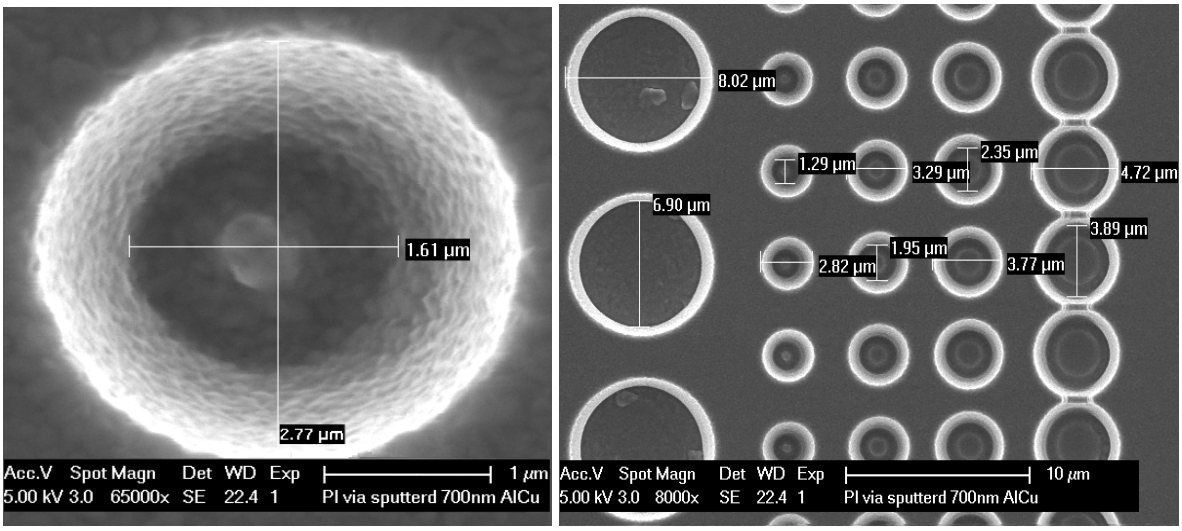


Figure 5.7: A SEM image of the etched (210s etched) contact hole with using AZ5344 resist (Pt coated).

Finally, the contact holes were filled with metal by means of the sputtering. 700 nm AlCu was sputtered in the hole, this is shown in Figure 5.8. The image shows that the metal is evenly deposited on the sidewalls. Due to the slope of the sidewall a good coverage is obtained. For larger vias the slope of the sidewalls, covered with metal, is slightly smaller than for vias a lower diameter.



(a) (b)

Figure 5.8: A SEM image of sputtered contact holes (180s etched) of (a) a close up (b) multiple vias.

5.1.1. Conclusion

It is found that small contact holes in the polyimide middle can be fabricated using a thick photoresist as mask (3.9 µm AZ4533). A low energy in combination with a post exposure-bake at 115 °C for 30 minutes as a reflow step results in small vias with a slight slope in the sidewall. An etch time between 180 s and 200 s gives good results. Unfortunately, an endpoint detection is not possible for the polyimide etching using PR as mask. The exact etch time is critical for a good result, but can variate since the etch-rate is slightly variable depending on the condition of the etcher. Therefore, the correct etch time should be checked periodically.

5.2. Fabrication of daisy chains

Daisy chains are test structures consisting of a concatenation of vias connected by interconnects. This test structure combines AlCu etching and the fabrication of the contact holes. Figure 5.9 shows the design and schematic of the resulting daisy chain. The mask design (Figure 5.2a) consists of two overlapping metal layers and a circular hole in the polyimide layer. A top view is shown in Figure 5.2b, at the place where the metal overlaps a tapered contacted hole is shown. A cross section is shown in Figure 5.2c.

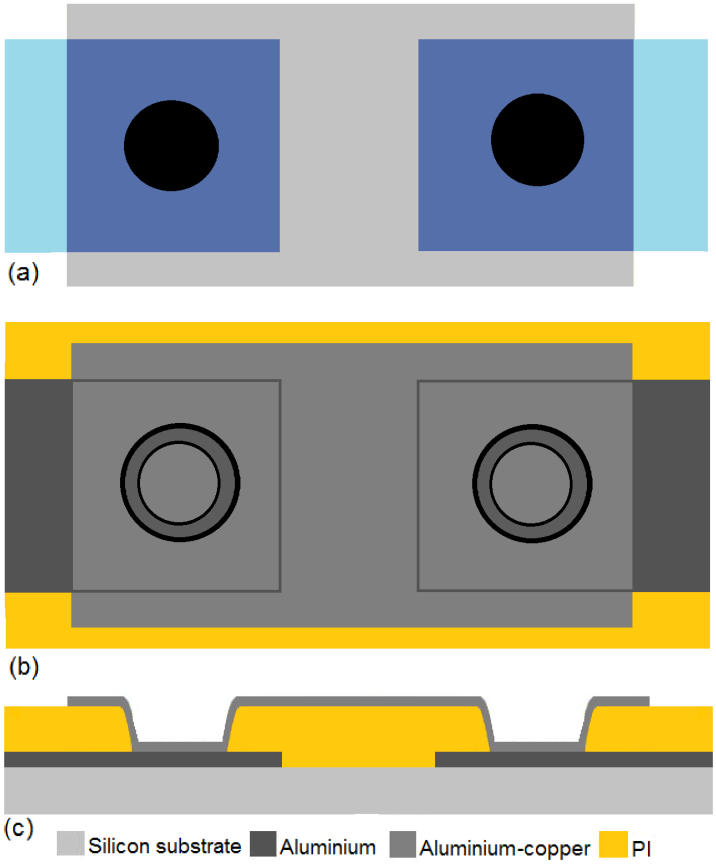


Figure 5.9: (a) mask design the fabrication of a daisy chain, (b) schematic top view of a daisy chain, (c) schematic cross-section of a daisy chain.

Since the process flow for the fabrication of the contact holes and the etching of the metal layers was already known, the fabrication of the daisy chains was relatively straightforward. The used process flow is a part of the full F2R process flow, shown in Appendix B.7. First a metal layer was deposited and patterned using a HPR resist and a PES etch. A microscope image of a part of the first metal layer is shown in Figure 5.10. The definition of the metal is not a sharp compared to when a dry etch would have been used, but sufficient for this application.

Next, the first polyimide layer was spin coated and cured. Subsequently, this layer was patterned using the process flow determined in Section 5.1. During the patterning of the PI layer the contact holes are fabricated. Next, the second metal layer is deposited by means of sputtering of 700 nm AlCu. The second metal layer is next to serving as the re-routing layers also filling the vias. This layer of AlCu is patterned as explained in Chapter 4. Figure 5.11 shows the patterned resist on top of the AlCu layer. The result after the etch is shown in Figure 5.12. Two etched and filled contact holes are shown. These contact holes are larger than expected. The diameter of the holes is approximately 4 µm, while the hole in the mask for this chain was 1.2 µm. The expansion of the vias is more than was observed during the experimental fabrication of the contact holes. The difference is caused by inconsistency during the process, most likely during the polyimide dry etch.

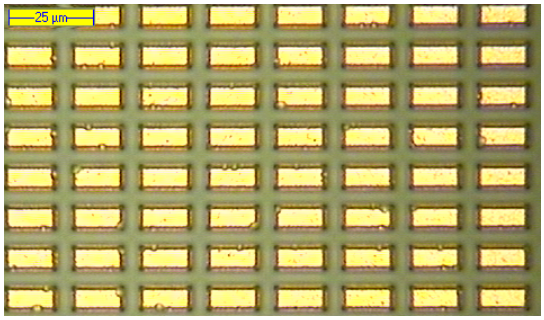
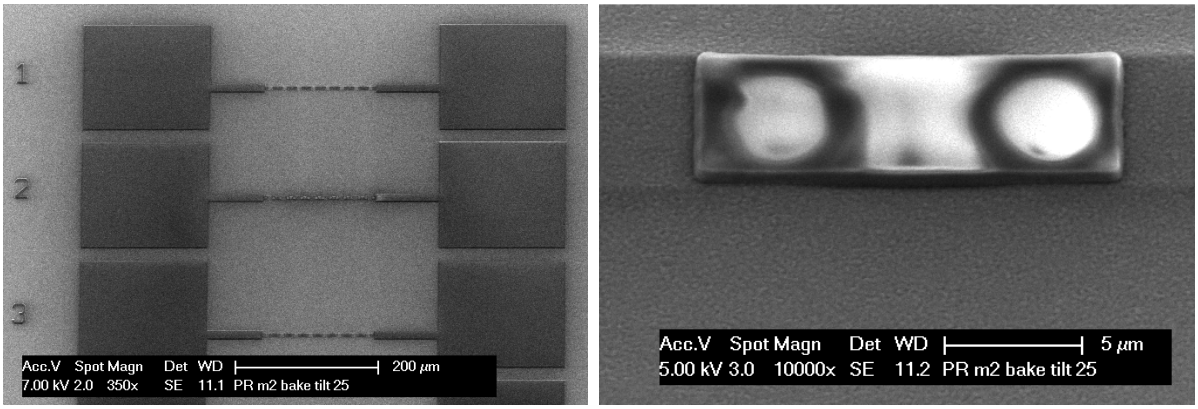
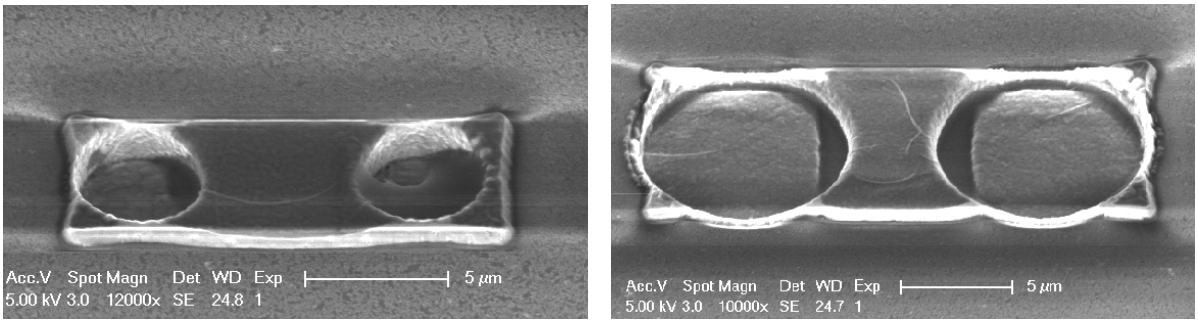


Figure 5.10: A part of the patterned first metal layer (M1).



(a) (b)

Figure 5.11: Pattered resist on top of M2 (a) a part of the daisy chains including bondpads (b) zoomed in on one part of the daisy chain, the topology of M1 is observed, also the vias under the resist are shown.



(a) (b)

Figure 5.12: Etched AlCu layer a top metal layer for a daisy chain with (a) relative small vias and (b) relative large vias. For the daisy chain with the large vias the pattered metal areas in both layers is to small with respect to the hole.

After the daisy chains were fully fabricated, the electrical performance and yield was evaluated. Resistance measurements were conducted by probing the bond-pads with needles connected to a multimeter. All daisy chains were properly functioning. A resistance is added by the measurement setup, the bond-pad and the metal rerouting. This offset is calculated and corrected for to calculate the resistance of the individual vias. Figure 5.13 shows the average resistance as function of the via diameter (on the mask). The graph also includes a linear fit. Although from a theoretical point of view there is no reason to expect an linear relation, this linear relation gives a good fit. Unexpectedly, the resistance is increasing for increasing via diameter. This is not the expected relation since larger vias have a more

conductive metal area and thus a lower resistance is expected. However, the resistance of vias is very complex. It is know that the resistance of the vias is mainly caused by the perimeter of the via. The resistance is dependent on a lot of variables such as the contact resistance between two metals, the exact shape of the vias and the thickness of the metal everywhere at the perimeter of the via. One explanation of that the resistance is lower in smaller holes is that the metal coverage in the vias is slightly better. Before the sputtering of the metal the slope of all vias was similar, but after the holes were filled, the vias are more tapered from seen from a top view. However, this can probably not fully explain this resistance difference. On other reason is that the patterned metal areas in the design were to small for the size of the via. A comparison of Figure 5.12a and 5.12b shows that, although in the mask design is accounted for the increasing size of the contact holes, the metal areas in both layers are to small. This means that in the case of a lager vias effectively a part of the perimeter the via is not conducting since there is not metal deposited there.

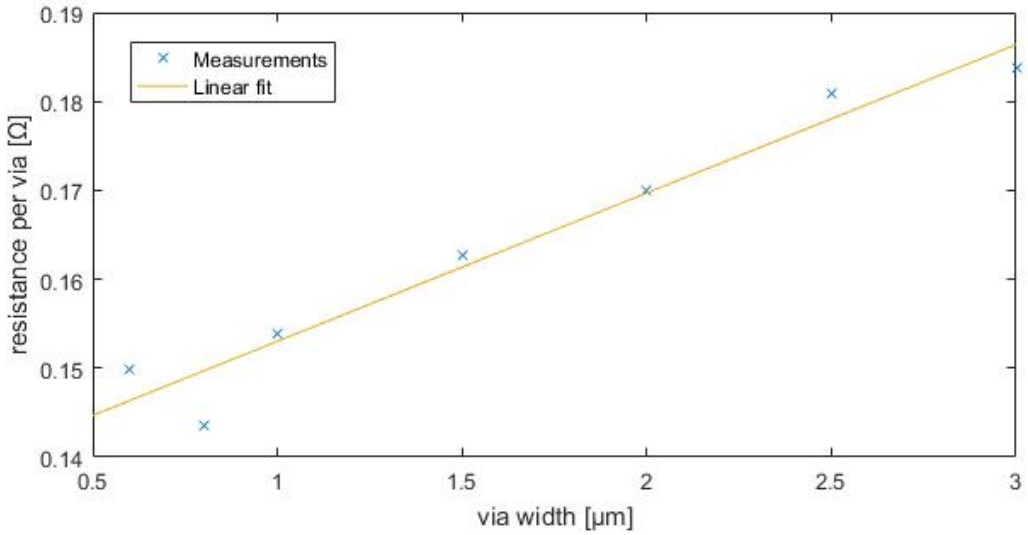


Figure 5.13: Average resistance per daisy chains a function of the via diameter and a linear fit trough the measurement data.

5.3. Conclusion

It is shown that small pitch contact holes in the polyimide layer, to electrically connect the metal layers, can be experimentally fabricated. Using a thick resist mask (at least 3.9 µm) holes in the polyimide (2.5 µm thickness) can be etched. A good metal coverage after sputtering is obtained by creating a slope in the soft mask by means of a reflow, and hence the slope is transferred to the contact hole in the polyimide. During the dry etch the dimension increases, smaller holes increase relatively more in size. Apparently, with the combination of a resist mask and very small holes, the dry etch is not fully anisotropical. Using the process flow of the fabrication of the contact holes and the metal etching daisy chains can be successfully fabricated. Electrical measurements confirm that both the vias and the daisy chains are properly functioning.

6

Adhesion of Polyimide

6.1. Introduction

In microfabrication a good adhesion between thin films is necessary. Both the adhesion of the deposited film to the substrate or layer below, and to the subsequently deposited layer should be sufficiently good. A poor adhesion between films can result in peel-off. This device failure can happen in the processing or operational stage of the device. For the application of F2R inside the body, maintaining a good adhesion can be even more challenging. For this wet environment a chemical bonding that is unaffected by water is required.

In F2R it is required that the thin films have a good adhesion to each other. These interfaces are silicon to polyimide, polyimide to polyimide and polyimide to aluminium. Aluminium and polyimide can form a chemical bonding and have sufficient adhesion [23]. Furthermore, the adhesion of polyimide to aluminium is less of an issue since the sandwiched metal layer has only a relatively small surface area. The other two interfaces are more important. First the polyimide to silicon interface will be discussed, subsequently the polyimide-polyimide interface will be discussed including the experiments performed to test and improve the adhesion.

6.2. Adhesion of polyimide to silicon

The most important adhesion in F2R is the adhesion between the silicon islands and the polyimide layer. The contact area between the silicon area and polyimide structures can be relatively small. This can result in high peeling forces during the assembly or usage of the F2R structures. A very strong adhesion is therefore required to prevent delamination between the polyimide and silicon. In earlier work an optimal process flow was found by using a layer of silicon oxide between the polyimide and silicon (unpublished). The PECVD layer silicon oxide will form a chemical bonding with the silicon. The oxide will not form a chemical bond to the polymer, however this can be achieved by using an adhesion promoter. From earlier research it was found that good adhesion can be obtained by spin-coating an organosilane-type adhesion promoter (VM-651 from HD Microsystems). This optimal process flow uses a oxygen descum to clean the surface and a sputter etch to roughen the surface. In combination with the adhesion promoter this leads to a very strong adhesion between PECVD silicon oxide and polyimide. The process flow is shown in Appendix B.1 in the stage '1st PI'. Since the strong and reliable adhesion between silicon (oxide) and polyimide was already demonstrated, this process flow is used in the F2R process and in this project.

6.3. Adhesion of polyimide to polyimide

The other interface in F2R where a good adhesion is required, is the polyimide to polyimide interface. The polyimide layers sandwiching the metal interconnects should have a perfect adhesion. If a second layer of polyimide is applied on the fully cured layer of polyimide, the adhesion between the layers can be poor. An approach for an improved adhesion to polyimide is roughening the surface by an oxygen plasma treatment. Such treatments have successfully been applied to achieve improved adhesion of polyimide [24, 25]. The mechanism which is improved here is the mechanical adhesion, since a

better interlocking of the layers is achieved. However, this mechanical adhesion is not sufficiently reproducible, reliable and strong for our application.

For the F2R research also experiments on the adhesion between polyimides have been conducted (unpublished). These experiments includes different cleaning and surface treatment steps such as an oxygen plasma treatment and sputter etch. Although with some combination of cleaning surface treatments good adhesion is achieved, these results were not properly reproducible. The adhesion result of the experiments were apparently dependent on one or more unknowns. Although extra experiments were conducted to find these unknowns, no optimal process flow for a consistent and strong adhesion was found.

An alternative self-adhesion promotion technique is interdiffusion across the interface between the two layers of polyimide [26, 27]. This interdiffusion allows the polymer chains to entangle with each other. The degree of interdiffusion is mainly dependent on the curing temperature of the two polyimides. If the first layer is cured at a low temperature, the polyimide is not fully crosslinked. Therefore it can still entangle with the second layer of polyimide. In the curing of the second layer both polyimides are fully cured, and all the solvent is removed. With this approach the chemical bonding can result in a strong adhesion between the polyimides. However, this requires the polyimide to be not fully cured during the process steps between the deposition of the two polyimides. Hence, this technique is not compatible with the F2R flow, since it is required that the polyimide is fully cured.

Because of the problematic self-adhesion of polyimide, the option of using another material as adhesion promoter layer was studied. Obviously this adhesion layer should be non-conductive. Both the adhesion of the first polyimide to the adhesion layer and the adhesion of the adhesion layer to the second polyimide should be strong. These interfaces can not be assumed to be equivalent due to the deposition techniques. For example the polyimide on top of silicon oxide can have a very good adhesion (with an adhesion promoter). However, silicon oxide deposited on top of polyimide does not necessarily have a good adhesion. Since the adhesion promoter is not usable in the situation the adhesion is not expected to be strong.

Another material which can have a good adhesion to polyimide is silicon carbide (SiC) [24, 28]. SiC is a compound of silicon and carbon with varying applications in different fields of electrical engineering [29]. A novel application of SiC is as an adhesion improvement layer. Since SiC consist of both silicon and carbon it can form a chemical bonding with both silicon based materials and organics such as polyimide [30]. Recent studies have shown that polyimide is capable of forming covalent carbon bonds with materials deposited by PECVD [30]. This covalent bond is unaffected in water. Studies show that this polyimide SiC interface does not delaminate in accelerated aging studies in water [28, 30].

6.4. Adhesion promotion layers

To investigate the possibility of using adhesion improvement layers, an experiment with different combinations of adhesion improvement layers was conducted. To test the adhesion resulting from the different process flows with the adhesion improvement layers, first these processes are completed after which a peel test is performed on the fabricated samples.

6.4.1. Method

To test the adhesion between two polyimide layers a modified brake and 90° pull test was used. After the experimental flowchart was completed, the adhesion was tested. The normal brake and pull test is a semi quantitative analysis where observers rate the adhesion. A sample is broken in the middle, from where the delamination is started. The force required to separate the polyimide foil from the substrate determines the adhesion between the polyimide and the layer beneath. If the foil breaks before delamination, the adhesion is assumed to be very strong. If the foil almost spontaneously delaminates the adhesion is assumed to be poor.

Testing the adhesion between two layers of polyimide it is more difficult adhesion since there is not a point to start the adhesion. However, an anti-adhesion layer in between the starting point can be

created. Platinum is known to have a very bad adhesion to polyimide, thus the material can be used as an anti-adhesion layer in between the layers of polyimide. An approximately 2 cm wide stripe of platinum is sputtered in the center of the wafer using a shadow mask. This shadow mask consists of cleaved pieces of regular wafers. The shadow mask on top a of polyimide wafer is shown in Figure 6.1. The shadow mask covers the sides during the sputtering, hence only on the exposed middle part platinum will be deposited.

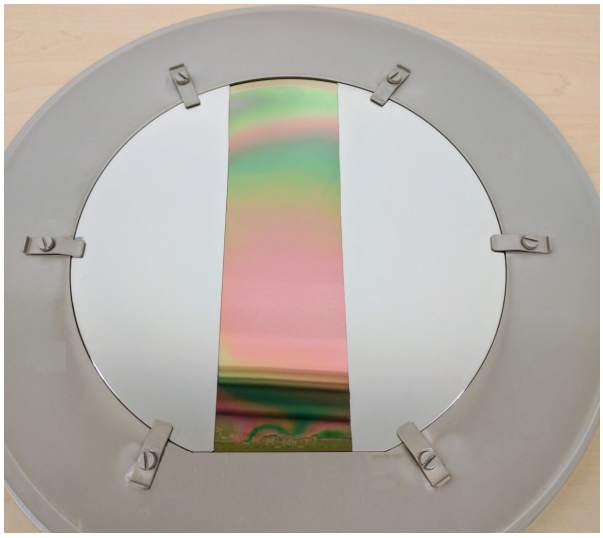


Figure 6.1: The shadow mask on a wafer to pattern a stripe of platinum.

Since the platinum is known to have a very bad adhesion to the polyimide, these areas provide the points where the second layer of polyimide could be delaminated to form a starting point for the break and pull test. In Figure 6.2 a schematic cross-section of the delamination process is shown. When the wafer is cleaved along the platinum, the top polyimide foil delaminates but does not tear. The two parts of the sample are now only connected by the top foil. Here the delamination starts. The delamination at the Pt part barely requires force. Once the Pt ends, the required force to continue the delamination is a measure of the polyimide-polyimide adhesion. The semi-quantitative observations of the force required for the delamination are the result of the experiment. Table 6.1 shows the semi-quantitative measures of adhesion that can be the result of the experiment.

To investigate the different adhesion improvement layers, four combinations of silicon carbide and oxide are used on separate wafers. In Figure 6.3 the layers are shown.

Table 6.1: Semi-quantitative measures of adhesion.

Measure	Description
- -	No adhesion, delamination occurs spontaneously
-	Poor adhesion, the second layer of PI delaminates easily
o	Medium adhesion, with some effort the second layer can be peeled off
+	Good adhesion, with a lot effort the second layer can be peeled off
++	Perfect adhesion, the second layer can not be peeled off, the second layer tears

6.4.2. Process flow

The process starts with on a normal 150mm diameter silicon wafer. The exact process flow is shown in Appendix B.1. First a PECVD layer of oxide is deposited, then a layer of polyimide is spin-coated. For the first polyimide on oxide the procedure is used as described in Section 6.2. On top of the polyimide

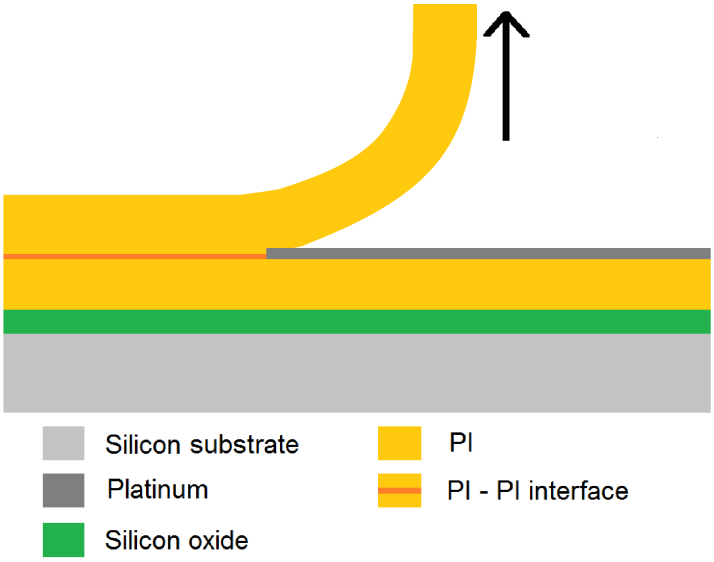


Figure 6.2: Schematic cross-section of the polyimide delamination process.

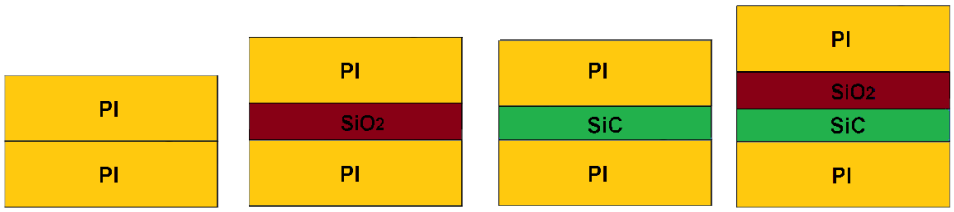


Figure 6.3: Different configurations of adhesion improvement layers.

layer the adhesion promotion layers are deposited. Directly prior to the deposition, a sputter etch is performed to roughen the surface of the polyimide. Next the platinum is sputtered with the shadow mask as shown in Figure 6.1. Then using the flow described in Section 6.2 is deposited the top PI layer. After the PI is cured the wafers are cleaved into the desired samples and the adhesion is tested.

6.4.3. Results

After the process flow as described in the section above was performed, the adhesion experiment was conducted. The reference sample where directly the polyimide on polyimide adhesion was tested without an adhesion promotion layers resulted in a medium adhesion. When only an oxide layer was used the adhesion was poor. Using only silicon carbide resulted in a medium adhesion, but still delamination was possible. A perfect adhesion was observed on the samples where both silicon carbide and silicon oxide were used. On none of these sample delamination was possible.

Table 6.2: Results of break and pull test for the adhesion improvement layers experiment. The result refer to the measures of adhesion as defined in Table 6.1.

Layer	PI-PI	PI-SiO2-PI	PI-SiC-PI	PI-SiC-SiO2-PI
Result	o	-	o	++

6.4.4. Discussion

The adhesion improvement layers test the feasibility of the multiple adhesion improvement layers. Although, a non-quantitative test method was used the results are useful to investigate the polyimide-polyimide adhesion. Since the difference in adhesion is large for this experiment this method is suf-

ficient. For the layers which did not result in a perfect adhesion, possibly the process flow could be optimized to improve the adhesion. However, this experiment shows clearly that the combination of silicon carbide and oxide results in the best adhesion. In case of a smaller difference between the adhesion results of the different layers additional experiments would have been necessary.

6.4.5. Conclusion

The results of the experiment clearly show that the samples with silicon carbide and silicon oxide results in a superior adhesion. The medium adhesion of the sample without an adhesion improvement layer is consistent with the experiments conducted in previous research. Since the adhesion of polyimide on oxide is known to be good, it can be concluded from this result that PECVD oxide on top of polyimide has a poor adhesion. I makes sense that a poor adhesion was obtained, since no adhesion promotor could be used. Furthermore, PECVD deposited silicon carbide has a very good adhesion on polyimide. However polyimide on SiC does not result in a very strong adhesion. The combination of first a layer of silicon carbide and then silicon oxide results in a very strong adhesion between the two layers of polyimide. Silicon carbide forms a chemical bonding to the polyimide, next the SiC and SiO2 can form a chemical bonding since pure silicon bonds are formed. Finally the oxide and polyimide can form a bonding using the known method of an adhesion promoter (VM651).

6.5. Wet environment test

For the in-body application of F2R the devices should be resistant to a wet environment. This means that the adhesion between the polyimide layers should be unaffected in a salinated solution. In the last section it is proven that a strong chemical bonding using adhesion promotion layers is possible. However, it is not yet shown that this bonding is unaffected in water. Therefore an experiment is conducted to test the adhesion of polyimide after it is exposed to a harsh wet environment.

6.5.1. Method

For this experiment samples from the previous experiment (Section 6.4) with silicon carbide and oxide as adhesion improvement layers were used. The exact process flow is described in Appendix B.1. The samples were put in salinated water (9g NaCl/l) in a 40^o C oven for 4 days to simulate the human body. Directly after the samples were taken from the water an adhesion test was performed by means of the break and pull test described in Section 6.4.

6.5.2. Results

When the samples came out of the water, visual no delamination was observed. The adhesion experiment resulted in that the second layer of polyimide teared during the pull for both samples. This means that the adhesion between the polyimide layers is still perfect.

6.5.3. Conclusion

Since the adhesion is still perfect after samples were put in heated water it can be concluded that the chemical bonding created by the adhesion promotion layers is very strong and unaffected by a harsh wet environment.

6.6. Process flow variations

Since a strong polyimide adhesion was achieved this new approach should be added to F2R. During multiple stages of the F2R process flow these improvements layers can be deposited and patterned. When these layers are deposited after the aluminium is sputtered and etched the effect of this process on polyimide should be studied. Therefore extra experiments were performed to test if the sputtering and etching of aluminum has influence on the polyimide surface and thus the adhesion to the next layer.

An other point of interest is whether a sputter etch on the polyimide surface right before SiC deposition improves the adhesion. A sputter etch can roughen the surface of the polyimide and hence improve the adhesion. Furthermore, the hypothesis is that a sputter etch creates reactive carbon on the PI surface and can create a chemical bonding with the carbon of the SiC. Another point of interest is whether a short oxygen descum on the polyimide surface before the SiC deposition (or sputter etch) has effect

on the adhesion.

6.6.1. Method

To investigate the effects of sputter etching, descum cleaning and aluminium sputtering and etching on the adhesion an experiment was conducted with different variations in the process. The combination of these three variations results in eight different process flows. Hence on 8 different wafers the process with these variations was performed. Using this approach both the individual steps and the combination of the variations can be studied. After the samples were fabricated the adhesion was tested using the adhesion break and pull test described in Section 6.4.

6.6.2. Results

The process flow is shown in Appendix B.2. The process flow is based on the process used during the previous experiment, but with the variations as described added. During the fabrication, on all wafers the this layer of platinum started to shown some small tears right before the spin-coating of the second layer of polyimide. On some places the tears resulted in delamination of the Pt layer. Fortunately the middle parts of all except one wafer were still useful since the tears were mainly located on the sides of the wafer. For seven of the eight wafers a sample was fabricated and thus the adhesion was tested. After the process was completed and the samples were ready, the same adhesion test was performed as in the previous experiments. The result of the test with the different process variations is shown in Table 6.3. The adhesion was perfect for all tested samples, every test resulted in a teared second polyimide layer and no delamination was observed.

Table 6.3: Results of the break and pull test for the adhesion experiment with process variation. The result refer to the measures of adhesion as defined in Table 6.1. Wafer 7 had an error during the fabrication and therefore no results are obtained from this wafer.

Wafer	1	2	3	4	5	6	7	8
Al deposition and etch	x	x	x	x				
Descum	x	x			x	x		
Sputter etch	x		x		x		x	
Result	++	++	++	++	++	++	n/a	++

6.6.3. Discussion

The influence of the variation in the experiment was not significant since no difference was observed in the experiment. There were no results from wafer 7 due to an error in the fabrication. However, it is highly likely that the adhesion result of this wafer would have been similar to the other wafers.

6.6.4. Conclusion

Since all the variants resulted in a perfect adhesion it can be concluded that a sputter etch or a descum is not required for a good adhesion. It is not proven that the theory of reactive carbon created by a sputter etch to achieve good chemical bonding is true. A descum is not required for a strong adhesion, however also no negative effect of a descum on the polyimide surface is observed. If in the process flow a descum is convenient, for example to clean the severe crosslinked resist from the surface, a short descum can be included in the process flow. The downside of using a descum is that some of the polyimide is etched. Furthermore, it is shown that the aluminium deposition and etching on the PI surface do not influence the adhesion.

6.7. Conclusion

Although in literature some methods are described to improve the polyimide self-adhesion, these methods are not compatible with F2R. The novel approach of using an adhesion promotion layer of silicon carbide and silicon oxide is the best option for a strong polyimide-polyimide adhesion in F2R. For the

in-body application of F2R a very strong adhesion between the layers is required, however, consistent and very good self-adhesion had not yet been achieved. The novel method with the two adhesion improvement layers resulted repeatedly and consistently in a perfect adhesion. Extra process steps such as a descum or sputter etch before the silicon carbide deposition are optional. This adhesion improvement method using extra adhesion layers is compatible with the F2R process flow. The layers can be deposited before or after the fabrication of the interconnects. However, in both cases additional process steps are required to pattern the additional layers. The extra process steps that are in accordance with design requirement 3 as listed in Section 1.1.1, since only production methods are used which are already being used in F2R.

7

Fabrication of high density flexible interconnects

7.1. Introduction

In the previous chapters the experimental fabrication and development of new techniques for improving the F2R process flow have been demonstrated. The main objective of this thesis is to develop these new fabrication techniques and integrate them in the F2R process flow. This integration will be shown in this chapter. For the fabrication of the full process flow the mask design explained in Chapter 3 is used. The general F2R process flow is explained in Section 1.1.4, this is also the process flow where this project is based on. The exact process flow used in this work is shown in Appendix B.7. The process is started with double side polished silicon wafers, to allow for backside processing. After cleaning and etching of the alignment marks, silicon oxide is deposited on both sides. The backside processing is explained in Section 7.3. The processing of the frontside is performed as explained in Chapters 4 and 5. On some wafers the deposition and patterning of the adhesion layers is integrated, this is explained in Section 7.2.

7.2. Integration of adhesion improvement layer

In Chapter 6 it was concluded that the polyimide-polyimide adhesion can be improved by depositing a thin layer of SiC and SiO2 between the deposition of the polyimide layers. The standard F2R process flow does not include adhesion improvement techniques or layers. In F2R the adhesion is not troublesome, spontaneous delamination has never been observed, however, it is also known that the adhesion is not strong. In this project, a part of the wafers will include the deposition and patterning of the adhesion improvement layers in the fabrication using the earlier optimized process flow the the polyimide-polyimide adhesion. There are three moments during the fabrication when the adhesion layers can be deposited and patterned, resulting in three different process flows. Figure 7.1 shows these tree process flows. The first option (flow (a)) for deposition of the adhesion layers, is directly after the curing of the first polyimide layer. In this case these layers need to be patterned before the etching of the polyimide. Since a soft mask is used to fabricate the contact holes, the contact holes are larger that the holes in the mask and thus an extra mask with larger holes is required for patterning the adhesion layers. Since this option needs an extra mask, this option is not the most convenient option. The adhesion layers could also be deposited after the patterning of the polyimide (flow (b)). However, a similar problem would occur, since the silicon carbide and silicon oxide should then be removed from the inside of the contact hole. An other problem related to the patterning of silicon carbide and silicon oxide and polyimide is that there is not an etchant (both dry and wet) that can etch etch silicon carbide with good selectivity to polyimide. Lift-off could be a possibility to pattern thin layers of silicon carbide and silicon oxide [30].

The adhesion layer could also be deposited after the deposition and patterning of the re-routing layer (flow (c)). In this variant the adhesion layers do not cause a problem for the vias since these layers are deposited on top the the AlCu layer. Directly after deposition of the adhesion layers the second

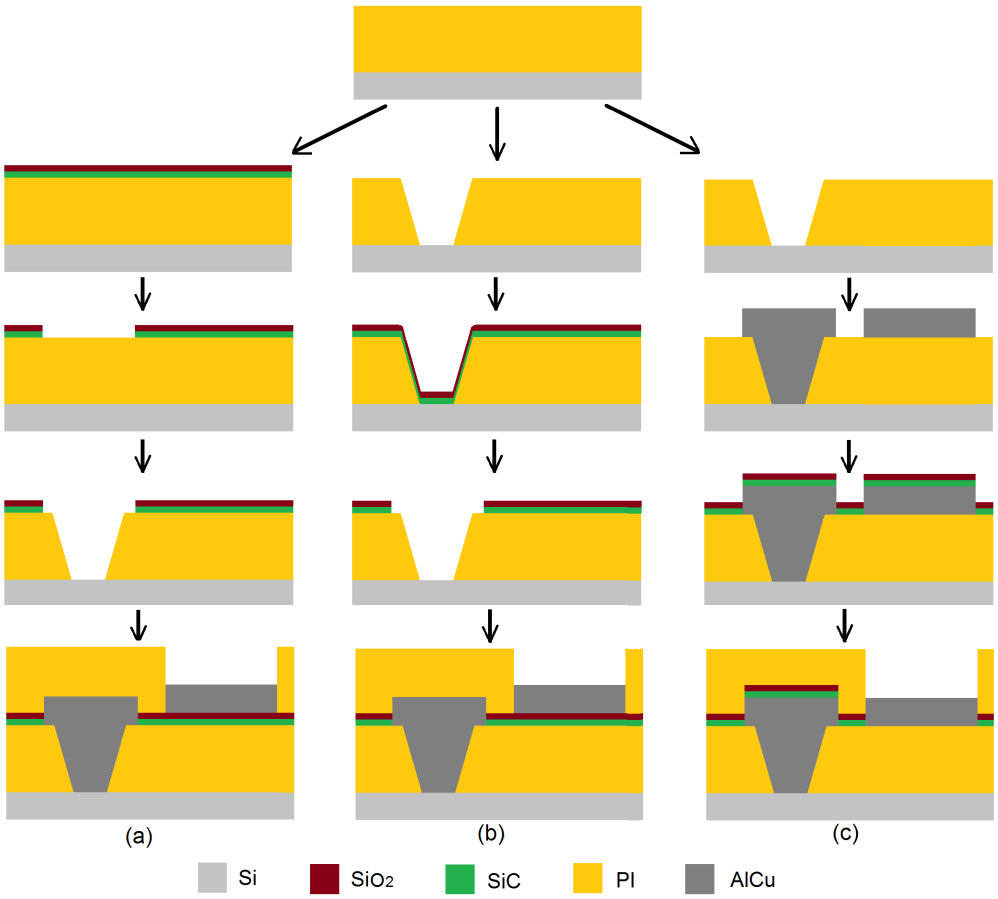


Figure 7.1: Tree different process flows for depositing and patterning the adhesion improvement layers between the polyimide layers. The cross-section includes a contact hole and a bond-pad. Although the different process flow the results are equivalent. In flow (a) first the adhesion layers are deposited and patterned, in flow (b) first the contact hole is etched and in flow (c) first the metal is deposited.

polyimide layer can be deposited. Although in the situation the adhesion layers should also be patterned, an extra masking step not required. Figure 7.2 shows in a schematic cross-section how the adhesion layers play a role with certain structures. Structure (1) shows an area where the wafer should be fully etched, the silicon was already etched from the backside, in order to fully etch the polyimide also the adhesion layers need to be etched. Structure (2) shows a via connecting the two metal layers, the adhesion layers do not cause problems here. Structure (3) shows a bond-pad, to make electrical contact with the bond-pad the adhesion layers should be removed. In both situations the silicon oxide and silicon carbide should be removed. This can be done with RIE and using the same metal hard mask as which is used for the polyimide etched. This option is the most convenient since it does not require and additional mask. Hence this approach chosen for the integration in the F2R process flow.

7.2.1. Etching of silicon carbide and silicon oxide

To pattern the silicon carbide and silicon oxide, RIE is used with the same metal hard mask as is used for the etching of the polyimide. First the polyimide is etched down to the adhesion layers in a regular oxygen plasma. Dry etching of silicon oxide is usually done in a fluorinated plasma. In the PInS cleanroom there is a lot of experience with silicon oxide etching. However, silicon carbide is new in the PInS cleanroom. RIE etching of SiC is possible in several (mixtures) of fluorinated gasses [31], this means that silicon oxide and silicon carbide are both etched in the same dry chemistry. The aluminium hard mask barely etched in the fluorinated chemistry. In [32] a selectively of 12 has been reported.

Since etching of silicon carbide was new in the PInS cleanroom, first an experiment has been conducted to optimize the dry etching of the combination of silicon carbide and silicon oxide . For the silicon carbide

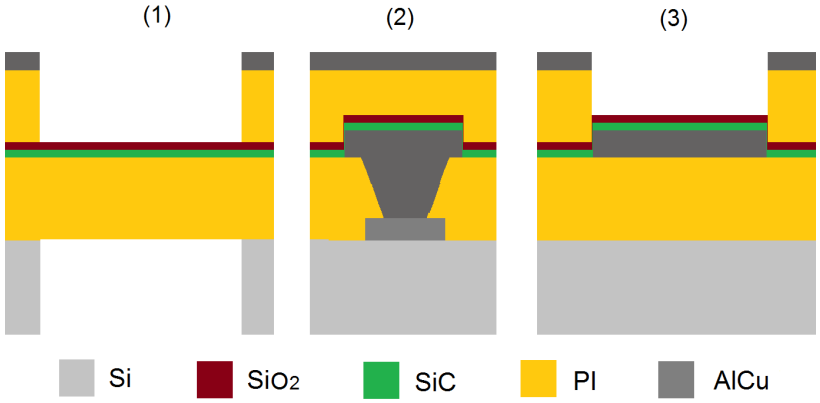


Figure 7.2: Schematic cross-section of adhesion layers in combination with (1) a trough wafer etch (2) a via and (3) a bond-pad.

and silicon oxide etching a recipe has be created consisting of SF6 as etchant. First, on a silicon wafer 188 nm silicon oxide and on top 217 nm silicon carbide has been deposited in a PECVD reactor. Next a layer of 200 nm aluminum was sputtered as a hard mask. The metal mask was patterned using standard lithography and a PES etch. During the dry SF6 etch no clear endpoint was observed, after one minute the etching was stopped. The etch-rate was determined using a Dektec height measurement, a height difference of 347 nm was measured. Thus the average etch was 347 nm/min. With this experiment the exact individual etch-rates could not be determined.

7.3. Backside mask and etch

In F2R arbitrarily shaped partially flexible devices are fabricated by means of a two step backside silicon deep reactive ion etching. For this two-step etch, also a two-step mask is required. The process flow of the side mask and etching is shown in Figure 7.3. In the top of this figure the top view of the final device is shown, a rigid frame with inside a partly flexible structure. Below, the cross-section of the backside processing steps are shown. In the first step (1) alignment marks are etched on the front side, and on both sides low stress silicon oxide is deposited. In the next step (2) resist is patterned using the first mask. Then the silicon oxide is etched on the places where later the silicon should be fully etched. After the resist is stripped the process is repeated with the second backside mask. During this step (3) the silicon oxide mask is thinned down resulting in a different mask. With this mask the silicon can be etched further. In some areas the silicon is fully etched and in other areas silicon is thinned down. Next, the frontside processing is performed, the polyimide and metal layers are deposited and patterned.

In step (4), after the frontside processing is completed, the first silicon DRIE backside etch is performed. In this project this step is time based and the silicon is etched halfway. The non-uniformity of the etch will have a direct effect on the thickness of the silicon island. This problem can be solved by using silicon-on-insulator (SOI) wafers. SOI wafers have a silicon oxide layer at a fixed depth underneath the surface of the silicon wafer. During the two-step DRIE backside process this buried silicon oxide layer could be used as an etch stop layer, and thus define the thickness of the silicon islands. However, this was not need for this project, therefore cheaper standard double side polished wafers were used.

After the first DRIE step, a silicon oxide etch is used to remove a part of the silicon oxide mask in step (5). The mask only remains on the silicon frame, since the silicon should not be etched there. In the final backside step (6) the silicon is fully etched, and the silicon oxide underneath the polyimide is removed. There is no need to stripping the remaining silicon oxide mask. In step (7) the polyimide is etched from the frontside, this completes the definition of the F2R structures. On some wafers the polyimide frontside etch also includes the etching of the adhesion improvement layers. Finally, the aluminium hard mask is removed in PES.

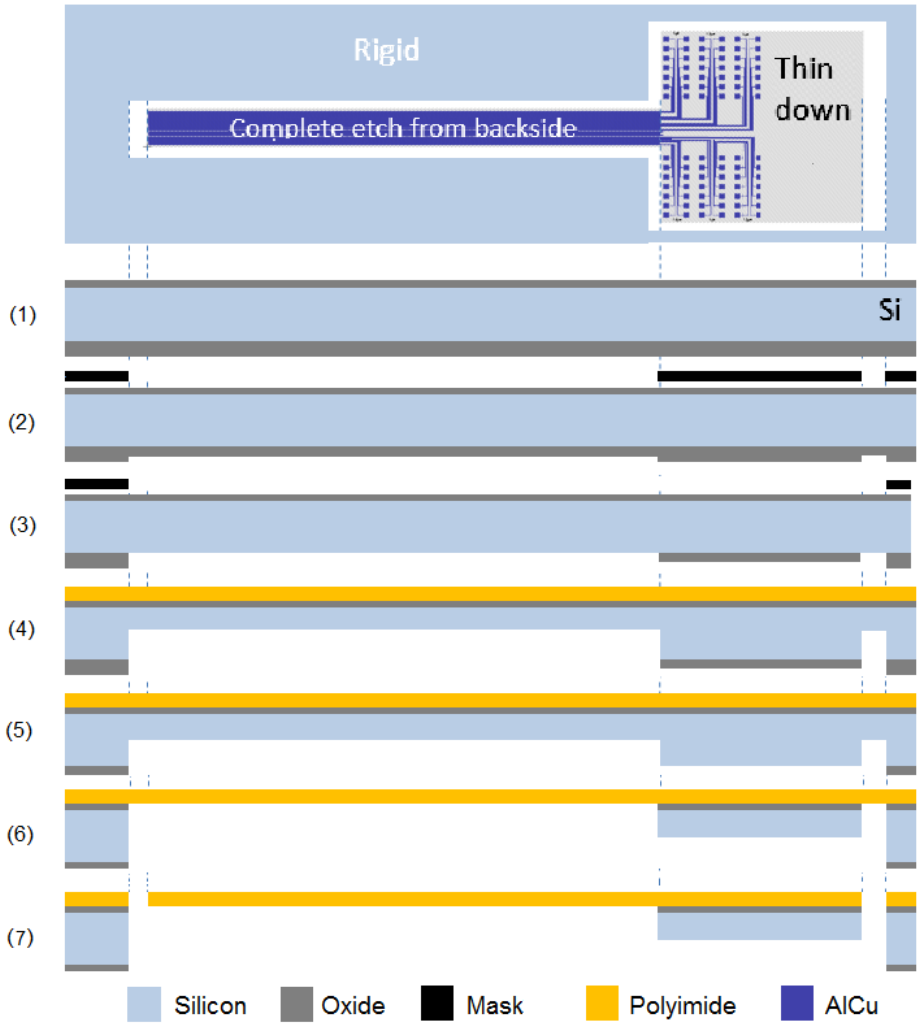


Figure 7.3: The schematic process flow of the backside processing. Between step (3) and (4) frontside is processed.

7.4. Results and discussion

Inspection after the patterning of the two-step silicon oxide hard mask on the back side shows a properly fabricated mask. A microscope image is shown in Figure 7.4, the different colors indicate the different silicon oxide thicknesses. A step height measurement measures a silicon oxide thickness of 0.9 µm and 5.5 µm on respectively the island and the frame.

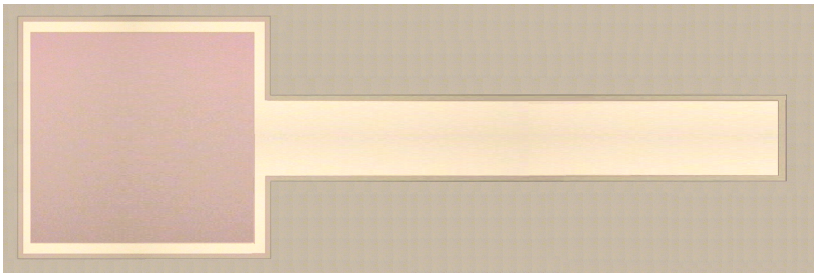


Figure 7.4: A microscope image of the back hard mask.

The frontside-processing resulted in properly functioning daisy chains and interconnects, these results are shown in Chapter 4 and 5. After curing of the second polyimide layer the hard mask is deposited,

this layer consist of 200 nm aluminum.

During the silicon DRIE no endpoint detection was available, therefore the etching was split in steps with step height measurements in between. After the two-step DRIE Si etch, the silicon was fully etched where necessary. The thickness of the islands is on average 160 µm, due to non-uniformity of the etching a difference of 10 µm is measured between the dies.

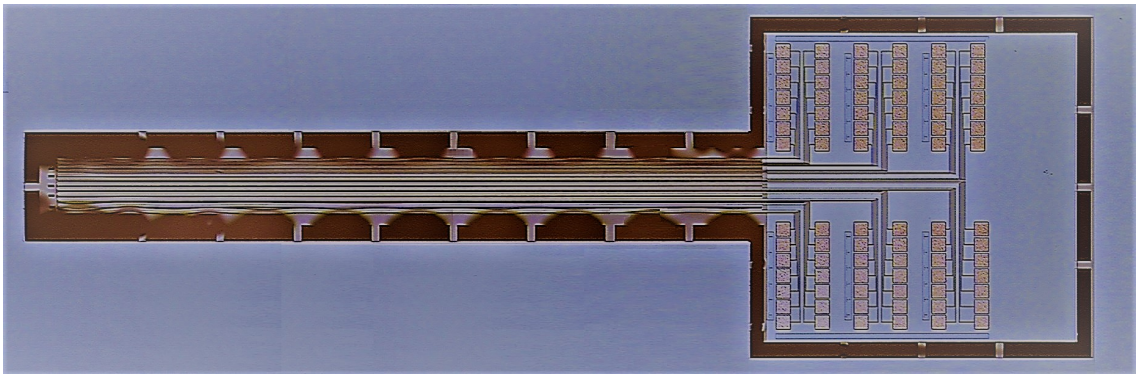
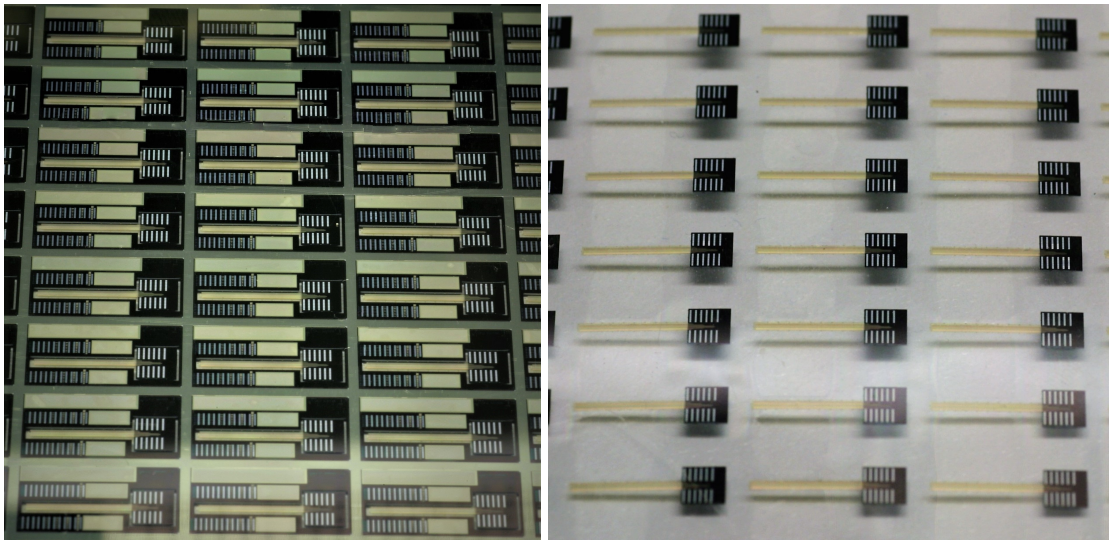


Figure 7.5: Microscope image of the front-side of a fully fabricated device. The dark blur is caused by the buckling of the flexible polyimide.

The polyimide etch from the frontside on the wafers without adhesion layer resulted in helium leakage during the etching. A flow of Helium is used to cool the wafer from the backside during the etching. This leakage serves as an alternative endpoint detection. After the etch the structures are only suspended in small polyimide hinges. The metal mask was stripped in PES, and the wafers are rinsed and cleaned in water and isopropanol. A microscope image of a structure suspended in the silicon frame is shown in Figure 7.5. The dark blur in the image is caused by the buckling of the flexible polyimide. The fabrication was completed by laser cutting the polyimide hinges. Figure 7.6b shows the devices before the separation from the wafer and after the separation. An image of a single separate device is depicted in Figure 7.7.



(a) (b)

Figure 7.6: Fully fabricated devices (a) in the silicon wafer as frame and (b) after separation between foil.

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The wafer with adhesion layers was etched from the frontside in a oxygen plasma to etch the poly-

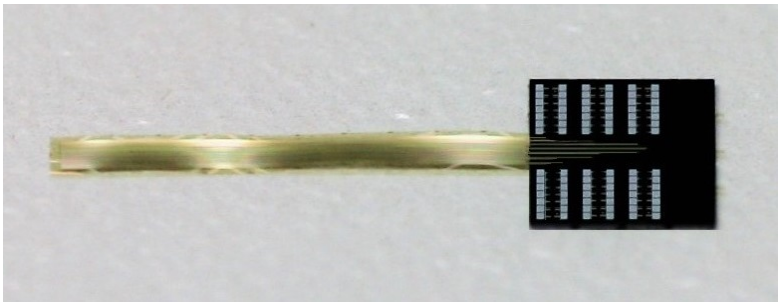


Figure 7.7: A separated device.

imide down to the adhesion layers. Next, the adhesion layers were etched for 30 s in SF6 with the developed recipe. With the previously determined etch rate this duration should be more than sufficient to completely etch the silicon oxide and silicon carbide layers. Unfortunately there is no suitable method to check if the silicon oxide and silicon carbide were completely removed. During the etching the helium leakage increased, but maximum leakage flow was lower than the polyimide etch without adhesion layers. After polyimide etching it was observed that not everywhere the adhesion layers were removed, since the polyimide was not everywhere completely removed. On most areas the polyimide was only partially removed, resulting in a flap of polyimide attached to the frame. This is shown in the microscope image in Figure 7.8. Since this flap of polyimide is only attached to the silicon frame and not to the flex, after separation of the device this flap was also separated from the device. Hence these flaps are not a major problem, but it indicates that the etching is not sufficient to completely etch the adhesion layers. What exactly happens during the etching is unclear. Furthermore, in some areas the polyimide was completely etched, although some areas were fully covered with polyimide. An example of these areas is shown in Figure 7.9. More experiments with the etching of SiC and SiO_2 are required to obtain a better understanding.

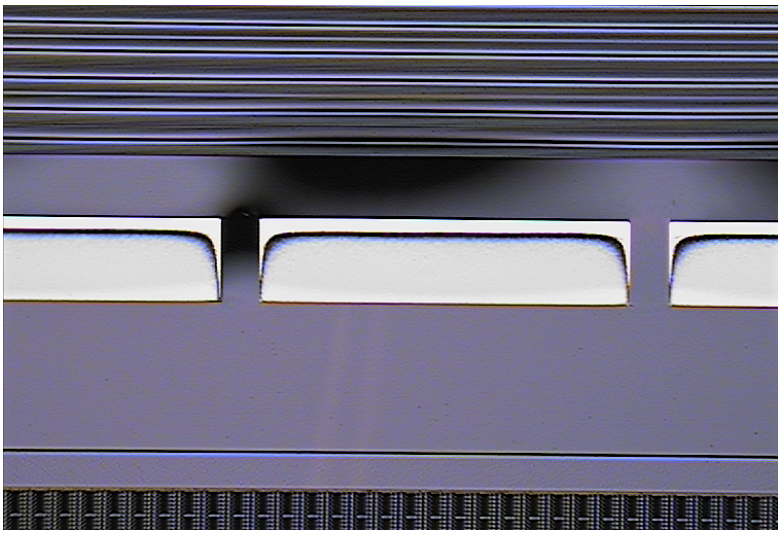


Figure 7.8: Area where the polyimide is not properly etched. A flap of polyimide is attached to the frame side.

An approach to improve the etching could be to increase the SF_6 etch to ensure that the adhesion layer is fully etched. There is not a major drawback in increasing this etch, since the polyimide underneath should also be etched, besides the selectivity to the aluminium mask is very good. However, the problem still remains that there is not a convenient way of determining when all the silicon oxide and silicon carbide is removed.

Moreover, an alternative approach can be to use a mixture of gases to etch both the silicon oxide ,

Figure 7.9: Result after polyimide etching on a wafer with adhesion layers. An area were the polyimide is not removed (left) and where the polyimide is fully removed (right).

silicon carbide and polyimides in one go. SiC is always etched in a fluorine based chemistry, however adding O_2 to the plasma can improve the etch-rate [33, 34]. Although the oxygen does not have an active or direct role in the process, it is observed that an addition of around 20 % till 40 % O_2 to SF_6 gives a higher etch-rate. At a very high percentage of oxygen the etch-rate drastically decreases.

Furthermore, for the polyimide etching the addition of SF_6 or CF_4 to the oxygen plasma can have positive effects. In some literature it is reported that the etch-rate increases when a small percentage of SF_6 or CF_4 is added [35, 36]. However, there are also situations reported where the etch-rate slightly decreases when fluorine based gases are added to the oxygen plasma [22],[37]. Nevertheless, the etch-rate of polyimide etching will never drastically decrease by the addition of fluorine-containing gases to the oxygen plasma, because polyimide etches also in pure fluorine-based gases. If a combination of these gases would be used, in one etch both the two polyimide layers, the silicon carbide and the silicon oxide could be etched. The etch-rate would be approximately the same, but the complexity will decrease. The leakage detection can be used to determine if all material is etched. Using this approach the aluminium hard mask will be sufficient since the selectivity will increase even further. Due to the addition of O_2 in the plasma the aluminum oxidizes and does not etch [34]. The selectivity will increase rapidly, after 40 % O_2 the selectivity reaches infinite [34].

7.5. Conclusion

In this chapter the successful fabrication of the high density flexible interconnect test devices is demonstrated using the earlier optimized process steps in combination with a two-step backside DRIE process. The integration with adhesion improvement layers is explained, and the most convenient way is included in the process flow. During the etching of the adhesion layers and the second layer of polyimide a problem occurred which resulted in a remaining flap of polyimide attached to the frame, most likely caused by insufficient etching of the adhesion layers. Nevertheless, after separation successful devices including the adhesion layers were obtained.

8

Measurements and results

8.1. Introduction

After the successful fabrication of the test devices, the flexible interconnects were tested both electrically and mechanically. This chapter describes the experiments and presents and discusses the results. The objective of these tests is to find the minimum bending radius and the failure modes. Furthermore, the difference is examined between the test devices with and without adhesion layers. Delamination during these tests is more likely on devices without adhesion layers. In [4] it is demonstrated that the bending of flexible interconnects down to a radius of 50 µm is achievable. However, to fabricate an IVUS ultra-sound catheter around a guidewire with a 360 µm diameter in some situations bending radii even less than 50 µm can be required (see Chapter 2).

8.2. Electrical measurements

The flexible interconnects have been measured in a similar manner as the intermediate measurement of the interconnects on the wafer. Using a multimeter (keithley 2700) and probing needles the bond-pads have been measured. Both the devices with and without the adhesion layers showed results comparable with the intermediate resistance measurements as shown in Chapter 4. The resistance measurements showed that all AlCu interconnects were conducting and no short-circuits between the interconnects have been observed. No interconnects were measured with a resistance with a significant deviation ($< 3\sigma$) compared to the results in section 4.

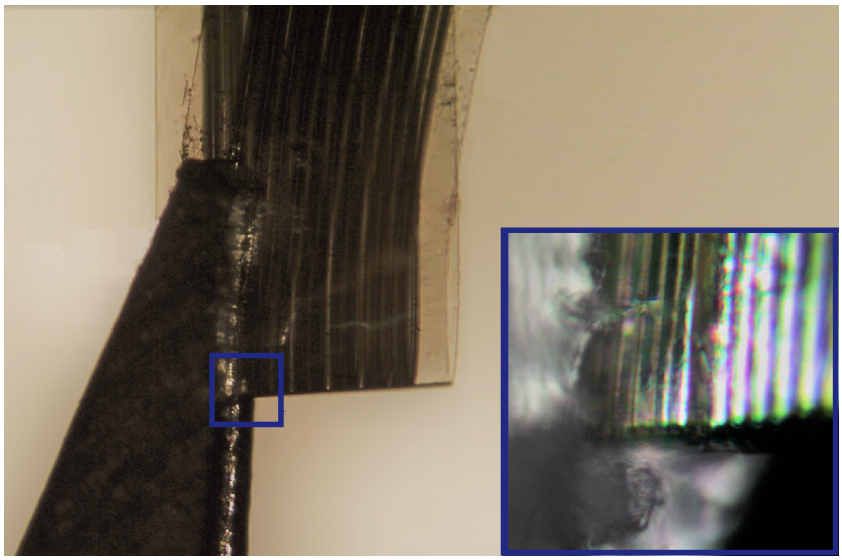
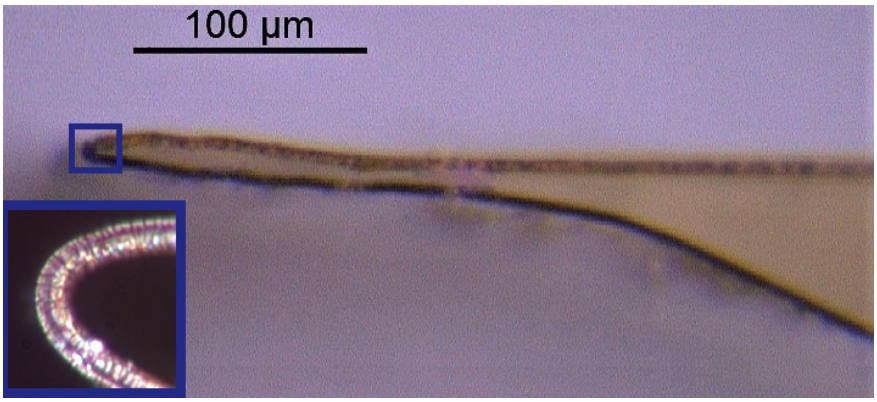


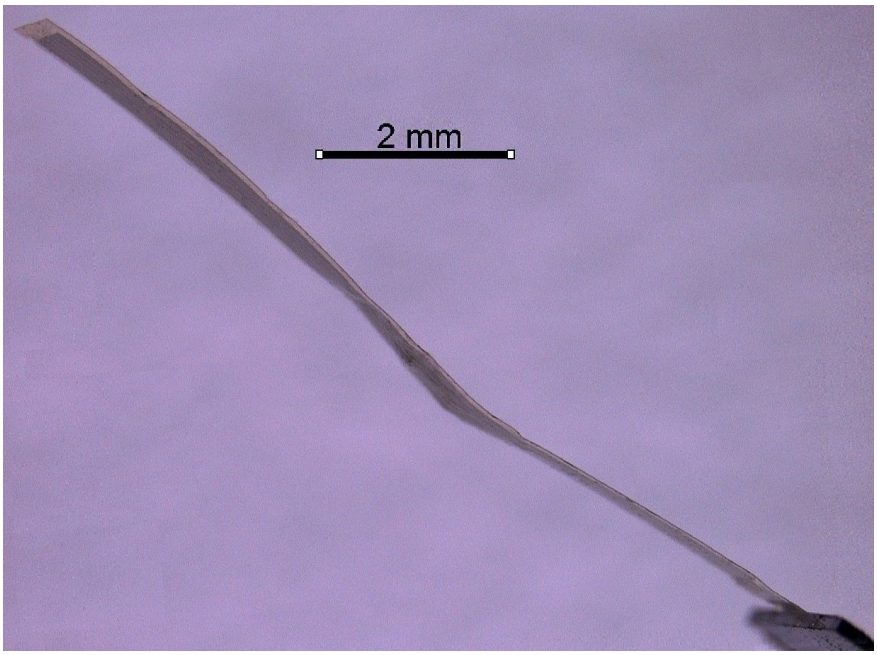
Figure 8.1: The flex with the flexible interconnects are folded using tweezers to apply local pressure.

8.3. Bending test

In order to test the flexibility of the flexible foil an accurate method is to bend the interconnects around a small radius wire as presented in [4]. However, from a mechanical point of view it is very challenging to go to very small radii using this approach because it is difficult to force the flexible foil to bend around such a small diameter wire. Another method is to bend or even fold the flexible interconnects between an object such as tweezers or a book. First using tweezers the flexible interconnect was bent. When not a lot of force is applied, the flexible interconnect comes back to its original shape. This is not the case when more pressure is applied. When the interconnect is folded, the bending radius at the fold is very small and approaches thickness of the PI layer (5 µm). The folded foil with interconnects between tweezers is shown in Figure 8.1. With tweezers local pressure was applied and the bending radius approached 5 µm. A microscope inspection indicated that no failures such a breaking, tearing of delamination of the interconnect were observed.



(a)



(b)

Figure 8.2: A side view of (a) a folded interconnect and (b) the interconnect folded back afterwards.

After pressure was applied on different places on the fold, the flexible foil stayed in this folded shape. A microscope image of the side view of a folded flexible interconnect is shown in Figure 8.2a. The image shows that the bending radius at the tip of the flexible interconnects is <10 µm. While folded, an electrical measurement showed that the resistance of the metal interconnects did not significantly

change due to the folding.

Next, this flexible interconnect was folded back, first with tweezers and then with a sheet to apply pressure evenly. The flexible interconnect came back to the original shape, this is shown in Figure 8.2b. Again, optical inspection and electrical measurements did not show failures. This tweezers bending test and measurement was repeated with several devices both with and without adhesion layers, giving similar results.

The flexible interconnects were also tested using a book to apply pressure on a folded interconnect, this is depicted in Figure 8.3. After 5 minutes between the book a sharp fold was created in the interconnects. Nevertheless no electrical failures were found. The flexible interconnect was folded back, however the fold remained visible. A microscope image of the interconnect after folding back is shown in Figure 8.4.

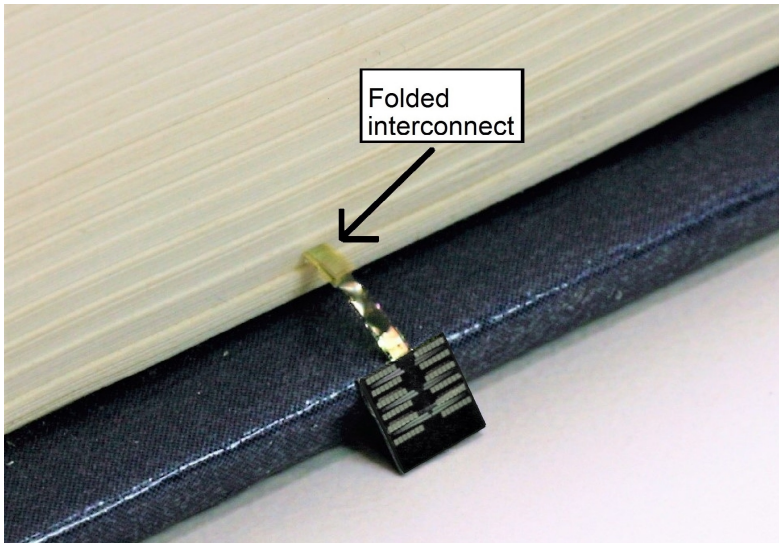


Figure 8.3: The flexible interconnects can be bent 180 degrees (folded) and remain fully functional. In this photograph the test structure was folded and squeezed between the pages of a book to apply pressure evenly. The interconnects remain fully intact after this treatment.

8.4. Discussion

The bending test showed that the flexible foil can be bent to radii smaller than 10 µm, without observing any failures. No significant change in electrical measurement is observed when the interconnects are bent or folded. However, the dynamic behaviour during bending of the interconnect is not measured. During the bending the metal interconnects are deformed, which can cause a change in electrical behaviour. To accurately measure this, a more advanced and accurate measurement setup is required. Furthermore, a fatigue measurement would also be interesting. In such a measurement an interconnect would be repeatedly bent around a small radius to measure after how many cycles failures are observed.

No significant change in electrical behaviour has been observed during the test. However, the amount of measured interconnects was limited. Therefore it is difficult to compare the measurement results between different interconnects or devices. For example a small change in resistance could not be measured.

8.5. Conclusion

In this chapter it is shown that the flexible interconnect test devices are working as expected, all interconnects meet the expected resistance values. The interconnects can be bent or even folded to very

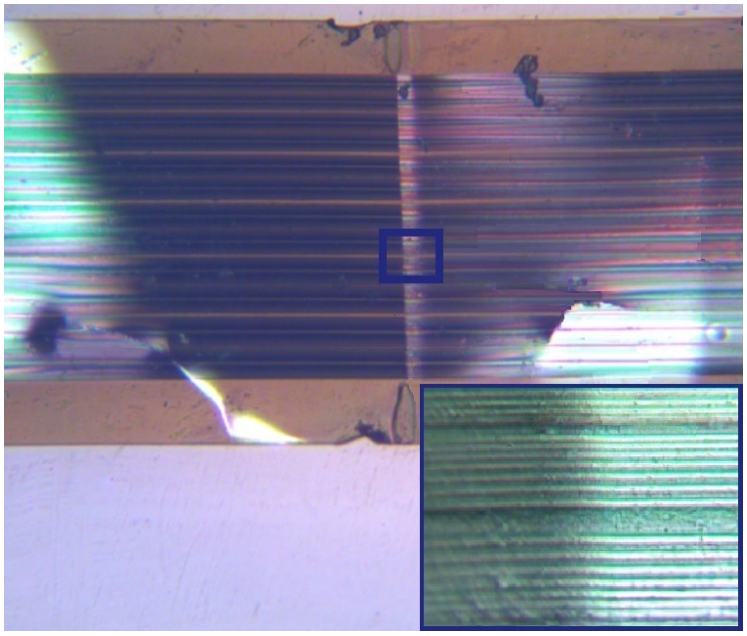


Figure 8.4: A interconnect folded back after being folded between a book.

small diameters of less than 20 µm without failures being observed. In most cases the interconnect can be folded back without permanent damage. Before, during and after the interconnects are bent no significant difference in the electrical behaviour is measured.

9 Conclusion

In this thesis challenges related to the development the next generation F2R technology platform have been adressesd. Novel techniques, improvements in the process flow and analysis of the technology are presented. These challenges are mainly related to increasing the density of the flexible interconnects and miniaturization of the F2R technology.

High density flexible interconnects have been fabricated by means of anisotropical chlorine based dry etching instead of isotropic wet etching. Using this technique the fabrication of flexible interconnects with 0.8 µm width and a total pitch of 1.6 µm is shown. The problem of post-etch corrosion of the AlCu interconnects was solved by taking anti-corrosion measures. These anti-corrosion measures are need to adequately remove the Cl(-containing) residues after the dry etch. Inadequate removal of these residues can cause the formation of HCl, which is very corrosive to AlCu. Furthermore, it was found that with an underlying layer of polyimide, the over-etch should be at-least 30 %.

Small-pitch vias have been fabricated by etching a small tapered hole in the polyimide layer and filling it with metal by means of sputtering. With lithography a resist mask with small holes has been patterned. Tapering in these holes was obtained by a post-exposure bake. This temperature step acts as a reflow for the resist. Next, the holes in the resist mask have been transferred to the polyimide layer by means of dry etching. In this work the fabrication of tapered contact holes with a pitch of 3 µm in a 2.5 µm thick layer of polyimide is demonstrated.

In this work a novel approach is shown were a combination of a very thin adhesion layer of SiC and SiO_2 creates a chemical bonding between two polyimide layers. With these adhesion layers perfect adhesion was obtained, even in a wet environment. Furthermore, the integration of these adhesion layers in the F2R process flow have been investigated and demonstrated.

The new techniques and improvements have also been integrated in the F2R process flow. The successful fabrication flexible interconnect test devices has been shown. These devices consist of a silicon island with bond-pads and test structures such as vias and daisy chains, and a flexible part with meandering flexible interconnects. Additionally, on some devices adhesion layers between the polyimides have been integrated. It is demonstrated that the patterning of these adhesion layers is possible, however the etching needs to be optimized.

Furthermore, an analysis has been done on the miniaturization of a F2R IVUS system wrapped around a guidewire. A relation was found between the geometry of the silicon islands and the flexible interconnects, and the radius of such the ultra-sound catheter. It was found that an IVUS catheter can be scaled to a smaller diameter using the same technology (amount of tiles, thickness of the tiles, etching angle, trench-ratio and flexibly of the interconnects) while only scaling the width of the islands. The analysis shows that this would require a greater flexibility then was achieved earlier work [4]. However, in this work bending radii of <10 µm are achieved with the fabricated test devices. Before, during and after the bending of the flexible foil all interconnects are functioning as expected. For both the devices with and without the adhesion layers no failures such as delamination or tearing of the polyimides were observed.

The improvements and new techniques showed in this work are expected to play an import role in the development of a next generation F2R technology platform. Using the newly developed techniques the density of the F2R-based devices can be increased, allowing for miniaturization and increased functionally. Furthermore, these new developments in combination with the analysis of the bending of the interconnects and F2R based IVUS systems, the design space is defined better.

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A

Derivation of a relation for the bending radius

In this appendix a relation between t, s, n, β and r_{out} is derived from the equation direct in Section 2.3. A relation for the inner radius was found in Section 2.3,

$$\tan\left(\frac{\theta}{2}\right) = \frac{{}^{1}/_{2}W}{r_{in}+t}. \tag{A.1}$$

With the substitution of equation 2.8 this can be rewritten to,

$$r_{in} = \frac{\tan\left(\sin^{-1}\left(\frac{W}{2\cdot r_{out}}\right)\right)}{{}^{1}/_{2}W} - t. \tag{A.2}$$

This equals equation 2.6 and can be rewritten as, (note: $\tan(\sin^{-1}x) = \frac{x}{\sqrt{1-x^2}}$)

$$\frac{\frac{W}{r_{out}}}{W\sqrt{1-\left(\frac{W}{2\cdot r_{out}}\right)^2}} - t = \frac{\frac{W}{2} - t\cdot\tan\beta}{\tan\left(\sin^{-1}\frac{s\cdot\cos\beta}{2t}+\beta\right)}, \tag{A.3}$$

with,

$$W = 2\cdot r_{out}\cdot\sin\left({}^{\pi}/_{n} - sin^{-1}\left(\frac{s}{2\cdot r_{out}}\right)\right). \tag{A.4}$$

Thus,

$$\frac{1}{r_{out}\cdot\sqrt{1-\sin^2\left({}^{\pi}/_{n} - sin^{-1}\left(\frac{s}{2\cdot r_{out}}\right)\right)}} - t = \frac{r_{out}\cdot\sin\left({}^{\pi}/_{n} - \sin^{-1}\frac{s}{2\cdot r_{out}}\right) - t\cdot\tan\beta}{\tan\left(\sin^{-1}\frac{s\cdot\cos\beta}{2t}+\beta\right)}. \tag{A.5}$$

The left hand side can be simplified (assuming ${}^{\pi}/_{n} + sin^{-1}\left(\frac{s}{2\cdot r_{out}}\right)$ is always positive),

$$\frac{1}{\sqrt{1-\sin^2\left({}^{\pi}/_{n} - sin^{-1}\left(\frac{s}{2\cdot r_{out}}\right)\right)}} = \frac{1}{\sqrt{\sin^2\left({}^{\pi}/_{n} + sin^{-1}\left(\frac{s}{2\cdot r_{out}}\right)\right)}} = \frac{1}{\sin\left({}^{\pi}/_{n} + sin^{-1}\left(\frac{s}{2\cdot r_{out}}\right)\right)}. \tag{A.6}$$

This results in the simplified implicit relation between t, s, n, β and r_{out},

$$\frac{1}{r_{out}\cdot\sin\left({}^{\pi}/_{n} + sin^{-1}\left(\frac{s}{2\cdot r_{out}}\right)\right)} - t = \frac{r_{out}\cdot\sin\left({}^{\pi}/_{n} - \sin^{-1}\frac{s}{2\cdot r_{out}}\right) - t\cdot\tan\beta}{\tan\left(\sin^{-1}\frac{s\cdot\cos\beta}{2t}+\beta\right)}. \tag{A.7}$$

B

Flowcharts

B.1. Polyimide adhesion improvement layers flowchart

Process flow polyimide adhesion improvement layers			
Stage	**No.**	**Step**	**Remark**
1st Polyimide	1	Start	Starting with 4x 1um PEVCD oxide wafers 150mm
	2	Semsysco	4 min HF Ozone cleaning
	3	VM651	apply VM651
	4	Spinning	2000rmp 45s dry spinning
	5	PI spinning	Dispensing PI, 8s500rmp,45s2000rmp,2s3000rmp
	6	Bake	PI softbake 5min at 125C
	7	Cure	Koyo oven N2 cure, 2h at 275C
Deposition	8	PECVD	50nm SiC deposition 250C
	9	PECVD	50nm Sio2 deposition 250C
	10	Sputter	100nm Pt sputter with shadow mask
2nd Polyimide	11	Descum	O2 descum 600W 2min 110C
	12	VM651	apply VM651
	13	Spinning	2000rmp 45s dry spinning
	14	Bake	2 min at 120C baking the adhesion promotor
	15	PI spinning	Dispensing PI, 8s500rmp,45s2000rmp,2s3000rmp
	16	Bake	PI softbake 5min at 125C
	17	Cure	Koyo oven N2 cure, 2h at 275C

B.2. Polyimide adhesion process variations flowchart

Process flow polyimide adhesion process variations				Wafers							
Stage	**No.**	**Step**	**Remark**	1	2	3	4	5	6	7	8
1st PI	1	Start	Starting with 8x 150mm	*	*	*	*	*	*	*	*
	2	Semsysco	4 min HF Ozone cleaning	*	*	*	*	*	*	*	*
	3	PECVD	1um low stress oxide	*	*	*	*	*	*	*	*
	4	VM651	apply VM651	*	*	*	*	*	*	*	*
	5	Spinning	2000rmp 45s dry spinning	*	*	*	*	*	*	*	*
	6	PI dispense	Dispensing PI (at RT)	*	*	*	*	*	*	*	*
	7	Spinning	Spin 8s500rmp,45s2000rmp,2s3000rmp	*	*	*	*	*	*	*	*
	8	Bake	PI softbake 5min at 125C	*	*	*	*	*	*	*	*
	9	Cure	Koyo oven N2 cure, 2h at 275C	*	*	*	*	*	*	*	*
Dep.	10	Sputter	1um 1.3kW Al sputtering	*	*	*	*				
	11	Etch	Al dry etch EPD+22s	*	*		*				
	12	Descum	O2 descum 600W 2min 110C	*	*			*	*		
	13	PECVD	50nm SiC deposition 250C	*	*	*	*	*	*	*	*
	14	PECVD	50nm Sio2 deposition 250C	*	*		*	*	*	*	*
	15	Sputter	100nm Pt sputter with shadow mask	*	*	*	*	*	*	*	*
2nd PI	16	Descum	O2 descum 600W 2min 110C	*	*	*	*	*	*	*	*
	17	Etch	10nm sputter etch	*	*	*	*	*	*	*	*
	18	VM651	apply VM651	*	*	*	*	*	*	*	*
	19	Spinning	2000rmp 45s dry spinning	*	*	*	*	*	*	*	*
	20	PI dispense	Dispensing PI (at RT)	*	*	*	*	*	*	*	*
	21	Spinning	Spin 8s500rmp,45s2000rmp,2s3000rmp	*	*	*	*	*	*	*	*
	22	Bake	PI softbake 5min at 125C	*	*	*	*	*	*	*	*
	23	Cure	Koyo oven N2 cure, 2h at 275C	*	*	*	*	*	*	*	*

B.3. Process flow dry etching Al interconnects on oxide

Process flow dry etching Al interconnects on oxide				Wafers				
Stage	**No.**	**Step**	**Remark**	1	2	3	4	5
Marks	1	Start	Starting with 8x 150mm DSP 400um	*	*	*	*	*
	2	Scribing	Laser scribing the wafer number	*	*	*	*	*
	3	Semsysco	4 min HF Ozone cleaning	*	*	*	*	*
	4	PR coating	Coating 1.3um HPR504 resist	*	*	*	*	*
	5	Exposure	Stepper ex. job:3d alignment, E=150, f=0	*	*	*	*	*
	6	Development	HPR development	*	*	*	*	*
	7	Etch	Marker etch 35s Si etch	*	*	*	*	*
	8	Strip	Hz plus 36 min strip	*	*	*	*	*
	9	Cleaning	4 min HF Ozone cleaning	*	*	*	*	*
	10	PECVD	1um low-stress SiO2 PECVD	*	*	*	*	*
Al patterning	11	Sputtering	700nm AlCu 1kW (5nm sputter etch)	*	*	*	*	*
	12	Coating	SPR660 1.3um PR coating	*	*	*	*	*
	13	Exposure	Stepper ex. job:M2, E=250, f=0	*	*	*	*	*
	14	Development	SPR development	*	*	*	*	*
	15	Bake	Resist bake (oven) T=125,t=30mim	*	*	*	*	*
	16	Etch	Al001 dry etch EPD+22s	*	*	*	*	*
	17	Passivation	7 min H2N2 treatment (anti-corrosion)	*	*	*	*	*
	18	Water	After etch directly in DI water bath	*	*	*	*	*
	19	Rinse	Std. rinse/dry	*	*	*	*	*
	20	Strip	Microstrip 10+5 min strip	*	*	*	*	*
	21	Rinse	Std. rinse/dry	*	*	*	*	*

B.4. Process flow dry etching Al interconnects 2-step

Process flow dry etching Al interconnects 2-step			
Stage	**No.**	**Step**	**Remark**
Marks	1	Start	Starting with 8x 150mm DSP 400um
	2	Scribing	Laser scribing the wafer number
	3	Semsysco	4 min HF Ozone cleaning
	4	PR coating	Coating 1.3um HPR504 resist
	5	Exposure	Stepper ex. job:3d alignment, E=150, f=0
	6	Development	HPR development
	7	Etch	Marker etch 35s Si etch
	8	Strip	Hz plus 36 min strip
	9	Cleaning	4 min HF Ozone cleaning
	10	PECVD	1um low-stress SiO2 PECVD
Aluminum patterning	11	Sputtering	1400nm AlCu 1kW (5nm sputter etch)
	12	Coating	SPR660 1.3um PR coating
	13	Exposure	Stepper ex. job:M2, E=250, f=0
	14	Development	SPR development
	15	Bake	Resist bake (oven) T=125,t=30mim
	16	Etch	Al001 dry etch 80s
	17	Etch	PA001 EPD+20s
	18	Etch	Descum 2min
	19	Etch	Al001 dry etch EPD+22s
	20	Passivation	7 min H2N2 treatment (anti-corrosion)
	21	Water	After etch directly in DI water bath
	22	Rinse	Std. rinse/dry

B.5. Process flow dry etching Al interconnects on polyimide

Process flow dry etching Al interconnects on oxide			
Stage	**No.**	**Step**	**Remark**
Marks	1	Start	Starting with 8x 150mm DSP 400um
	2	Scribing	Laser scribing the wafer number
	3	Semsysco	4 min HF Ozone cleaning
	4	PR coating	Coating 1.3um HPR504 resist
	5	Exposure	Stepper ex. job:3d alignment, E=150, f=0
	6	Development	HPR development
	7	Etch	Marker etch 35s Si etch
	8	Strip	Hz plus 36 min strip
	9	Cleaning	4 min HF Ozone cleaning
	10	PECVD	1um low-stress SiO2 PECVD
PI	11	Descum	O2 descum 600W 2min 110C
	12	Rinse	Std. rinse/dry
	13	VM651	Apply VM651
	14	Spinning	2000rmp 45s dry spinning
	15	PI dispense	Dispensing PI (at RT)
	16	Spinning	Spin 8s500rmp,45s2000rmp,2s3000rmp
	17	Bake	PI softbake 5min at 125C
	18	Cure	Koyo oven N2 cure, 2h at 275C
Rerouting	19	Start	Frontside processing
	20	Bake	Dehydration bake in oven T=125,t=30
	21	Sputtering	700nm AlCu 1kW (5nm sputter etch)
	22	Coating	SPR660 1.3um PR coating
	23	Exposure	Stepper ex. job:M2, E=250, f=0
	24	Development	SPR development
	25	Bake	Resist bake (oven) T=125,t=30mim
	26	Etch	Al001 dry etch EPD+22s
	27	Passivation	7 min H2N2 treatment (anti-corrosion)
	28	Water	After etch directly in DI water bath
	29	Rinse	Std. rinse/dry
	30	Strip	Microstrip 10+5 min strip
	31	Rinse	Std. rinse/dry

B.6. Process flow small pitch contact holes

Process flow small pitch contact holes			
Stage	**No.**	**Step**	**Remark**
Marks	1	Start	Starting with 150mm Si wafers
	2	Scribing	Laser scribing the wafer number
	3	Semsysco	4 min HF Ozone cleaning
	4	PR coating	Coating 1.3um HPR504 resist
	5	Exposure	Stepper ex. job:3d alignment, E=150, f=0
	6	Development	HPR development
	7	Etch	Marker etch 35s Si etch
	8	Strip	Hz plus 36 min strip
	9	Cleaning	4 min HF Ozone cleaning
	10	PECVD	1um low-stress SiO2 PECVD
	11	Sputtering	1um Al 1.3kW (6nm sputter etch)
PI patterning	12	Descum	O2 descum 600W 2min 110C
	13	VM651	Apply VM651
	14	Spinning	2000rmp 45s dry spinning
	15	PI dispense	Dispensing PI (at RT)
	16	Spinning	Spin 8s500rmp,45s2000rmp,2s3000rmp
	17	Bake	PI softbake 5min at 125C
	18	Cure	Koyo oven N2 cure, 2h at 275C
	19	PR coating	Coating 3.9um AZ4533 resist
	20	Exposure	Stepper exposure job:B2, E=200, f=0
	21	Development	AZ thick development
	22	Etch	ICP PAR02 O2 aniso etch 185s
	23	Strip	Microstrip 10+5 min strip
	24	Rinse	Std. rinse/dry

B.7. Full process flexible interconnects

Process flow flexible interconnects				Wafers				
Stage	**No.**	**Step**	**Remark**	1	2	3	4	5
Marks	1	Start	Starting with 8x 150mm DSP 400um	*	*	*	*	*
	2	Scribing	Laser scribing the wafer number	*	*	*	*	*
	3	Semsysco	4 min HF Ozone cleaning	*	*	*	*	*
	4	PR coating	Coating 1.3um HPR504 resist	*	*	*	*	*
	5	Exposure	Stepper ex. job:3d alignment, E=150, f=0	*	*	*	*	*
	6	Development	HPR development	*	*	*	*	*
	7	Etch	Marker etch 35s Si etch	*	*	*	*	*
	8	Strip	Hz plus 36 min strip	*	*	*	*	*
	9	Cleaning	4 min HF Ozone cleaning	*	*	*	*	*
	10	PECVD	1um low-stress SiO2 PECVD	*	*	*	*	*
Back mask	11	Start	Rotate wafer (backside processing)	*	*	*	*	*
	12	PECVD	5.5um backside zero-stress SiO2 PECVD	*	*	*	*	*
	13	PR coating	Coating 1.3um HPR504 resist	*	*	*	*	*
	14	Exposure	Stepper ex. job:B1, E=150, f=0	*	*	*	*	*
	15	Development	HPR development	*	*	*	*	*
	16	Etch	DRIE APS SiO01 5min,1200nm	*	*	*	*	*
	17	Strip	3min O2 strip Trymax	*	*	*	*	*
	18	PR coating	Coating 4.5um AZ4533 resist	*	*	*	*	*
	19	Exposure	Stepper exposure job:B2, E=200, f=0	*	*	*	*	*
	20	Development	AZ thick development	*	*	*	*	*
	21	Etch	DRIE APS SiO01 EPD(20min),4300nm	*	*	*	*	*
	22	Strip	5min O2 strip Trymax	*	*	*	*	*
Bondpads	23	Start	Rotate wafer (frontside)	*	*	*	*	*
	24	Sputtering	1um Al 1.3kW (6nm sputter etch)	*	*	*	*	*
	25	PR coating	Coating 1.3um HPR504 resist	*	*	*	*	*
	26	Exposure	Stepper ex. job:M1, E=150, f=0	*	*	*	*	*
	27	Development	HPR development	*	*	*	*	*
	28	Bake	Post-bake T=125,t=30min	*	*	*	*	*
	29	Etch	PES etch 10-12min EPD+10% (triton dip)	*	*	*	*	*
	30	Rinse	Std. rinse/dry	*	*	*	*	*
	31	Strip	5min O2 strip Trymax	*	*	*	*	*
1st PI	32	Start	Frontside processing	*	*	*	*	*
	33	Descum	O2 descum 600W 2min 110C	*	*	*	*	*
	34	Rinse		*	*	*	*	*
	35	VM651	Apply VM651	*	*	*	*	*
	36	Spinning	2000rmp 45s dry spinning	*	*	*	*	*

Flowchart continues on next page

Flowchart continued from last page								
1st PI	37	Bake	2 min at 120C baking the adhesion promoter	*	*	*	*	*
	38	PI dispense	Dispensing PI (at RT)	*	*	*	*	*
	39	Spinning	Spin 8s500rmp,45s2000rmp,2s3000rmp	*	*	*	*	*
	40	Bake	PI softbake 5min at 125C	*	*	*	*	*
	41	Cure	Koyo oven N2 cure, 2h at 275C	*	*	*	*	*
	42	PR coating	Coating 3.9um AZ4533 resist	*	*	*	*	*
	43	Exposure	Stepper exposure job:B2, E=200, f=0	*	*	*	*	*
	44	Development	AZ thick development	*	*	*	*	*
	45	Etch	ICP PAR02 O2 aniso etch 185s	*	*	*	*	*
	46	Strip	Microstrip 10+5 min strip	*	*	*	*	*
	47	Rinse	Std. rinse/dry	*	*	*	*	*
Rerouting	48	Start	Frontside processing	*	*	*	*	*
	49	Bake	Dehydration bake	*	*	*	*	*
	50	Sputtering	700nm AlCu 1kW (5nm sputter etch)	*	*	*	*	*
	51	Coating	SPR660 1.3um PR coating	*	*	*	*	*
	52	Exposure	Stepper ex. job:M2, E=250, f=0	*	*	*	*	*
	53	Development	SPR development	*	*	*	*	*
	54	Bake	Resist bake (oven) T=125,t=30mim	*	*	*	*	*
	55	Etch	Al001 dry etch EPD+22s	*	*	*	*	*
	56	Passivation	7 min H2N2 treatment (anti-corrosion)	*	*	*	*	*
	57	Water	After etch directly in DI water bath	*	*	*	*	*
	58	Rinse	Std. rinse/dry	*	*	*	*	*
	59	Strip	Microstrip 10+5 min strip	*	*	*	*	*
	60	Rinse	Std. rinse/dry	*	*	*	*	*
2nd PI	60	Dehydration	30min at 125C dehydration bake	*	*			
	61	Descum	O2 descum 600W 2min 110C	*	*			
	63	PECVD	50nm SiC deposition 250C	*	*			
	64	PECVD	50nm Sio2 deposition 250C	*	*			
	65	VM651	Apply VM651	*	*			
	66	Spinning	2000rmp 45s dry spinning	*	*			
	67	Bake	2 min 120C adhesion promoter bake	*	*			
	68	PI dispense	Dispensing PI (at RT)	*	*	*	*	*
	69	Spinning	Spin 8s500rmp,45s2000rmp,2s3000rmp	*	*	*	*	*
	70	Bake	PI softbake 5min at 125C	*	*	*	*	*
	71	Cure	Koyo oven N2 cure, 2h at 275C	*	*	*	*	*
Flowchart continues on next page								

Flowchart continued from last page								
Al mask	72	Sputtering	200 nm Al	*	*	*	*	*
	73	PR coating	Coating 1.3um HPR504 resist	*	*	*	*	*
	74	Exposure	Stepper ex. job:M1, E=150, f=0	*	*	*	*	*
	75	Development	HPR development	*	*	*	*	*
	76	Etch	PES etch 2min, EP+10% (trition dip)	*	*			
	77	Rinse	Std. rinse/dry	*	*	*	*	*
	78	Strip	Microstrip 10+5 min strip	*	*	*	*	*
	79	Rinse	Std. rinse/dry	*	*	*	*	*
DRIE	80	Start	Rotate wafers (backside processing)	*	*	*	*	*
	80	Etch	Deep Si aniso 60min	*	*	*	*	*
	81	Etch	SiO2 aniso 1200nm EP+10% OE	*	*	*	*	*
	82	Etch	Deep Si aniso 95min (330um)	*	*	*	*	*
	83	Etch	CHF3 high pressure 1min	*	*	*	*	*
PI etch	84	Start	Rotate wafers (frontside processing)	*	*	*	*	*
	85	Etch	PI etch PAR002 EP+20s	*	*	*	*	*
	86	Etch	SiO2 etch EP+10s	*	*			
	87	Etch	SiC ethc Ep+10s	*	*			
	88	Etch	PI etch PAR002 EP+20s	*	*	*	*	*
	89	Etch	PES etch 2min Ep+10%	*	*	*	*	*