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Nanoribbon Logic Gates & Circuits

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Dedicated to

my supervisors, family and country

Abstract

As CMOS feature size is reaching atomic dimensions, unjustifiable static power, reliability, and economic implications are exacerbating, thus prompting for research on new materials, devices, and/or computation paradigms. Within this context, Graphene Nanoribbons (GNRs), owing to graphene's excellent electronic properties, may serve as basic structures for carbon-based nanoelectronics. However, the graphene intrinsic energy bandgap absence hinders GNR-based devices and circuits implementation. As a result, en route to graphene-based logic circuits, finding a way to open a sizable energy bandgap, externally control GNR's conduction, and construct reliable high-performance graphene-based gates are the main desideratum. To this end, first, we propose a GNR-based structure (building block) by extending it with additional top gates and back gate while considering five GNR shapes with zigzag edges in order to open a sizeable bandgap, and further investigate GNR geometry and contact topology influence on its conductance and current characteristics. Second, we present a methodology of encoding the desired Boolean logic transfer function into the GNR electrical characteristics, i.e., conduction maps, and then evaluate the effect of V_{DD} variation on GNR conductance. Moreover, we find a proper external electric mean (e.g., top gates and back gates) to control the GNR behavior. Third, we develop a parameterized Verilog-A SPICE-compatible GNR model based on Non-Equilibrium Green's Function (NEGF)-Landauer formalism that builds upon an accurate physics formalization, which enables to symbiotically exploit accurate physics results from Matlab Simulink and optimized SPICE circuit solvers (e.g., Spectre, HSPICE). Subsequently, we construct graphene-based Boolean gates by means of two complementary GNRs, and design a GNR-based 1-bit Full Adder and a SRAM cell. Finally, we extend the NEGF-Landauer simulation framework with the self-consistent Born approximation while taking into account the temperature-induced phenomena in GNR electron transport, i.e., electron-phonon interactions for both optical and acoustic phonons, and further explore the graphene-based gates performance robustness under temperature variations.

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List of Acronyms and Symbols

HOPG	Highly Ordered Pyrolytic Graphite
CVD	Chemical Vapor Deposition
STT	Spin-Transfer Torque
SOT	Spin-Orbit Torque
GNR	Graphene Nanoribbon
GQD	Graphene Quantum Dot
MOSFET	Metal Oxide Semiconductor FET
FET	Field Effect Transistor
G-FET	Graphene based Field-effect Transistor
G-TFET	Graphene Tunnel Field-effect Transistor
DSE	Design Space Exploration
QPC	Quantum Point Contact
FA	Full Adder
NEGF	Non-Equilibrium Green Function
R-GNR	Rectangular Graphene Nanoribbon
B-GNR	Butterfly Graphene Nanoribbon
C-GNR	Camel Graphene Nanoribbon
W-GNR	Waterfall Graphene Nanoribbon
DB-GNR	Double Butterfly Graphene Nanoribbon
Z-GNR	Zigzag Graphene Nanoribbon
A-GNR	Armchair Graphene Nanoribbon
TB	Tight Binding
DOS	Density of State
GNRFET	Graphene Nanoribbon Field-Effect Transistor
SB-GNRFET	Schottky-Barrier-Type GNRFET
GNR-TFET	Graphene Nanoribbon Tunnel Field-Effect Transistor
SRAM	Static Random-Access Memory
ECC	Error Correcting Code
LDPC	Low Density Parity Code
RCA	Ripple Carry Adder
SNM	Static Noise Margin
3D	Three-dimensional
TSV	Through Silicon Via
MRAM	Magnetic Random Access Memory
MTJ	Magnetic Tunnel Junction
TMR	Tunnel Magnetoresistance

1 Introduction

As CMOS scaling is approaching atomic feature size, the high power density and leakage, low reliability and yield, and increasing IC production costs are exacerbating, thus prompting for research and development on new materials, devices, architectures, and computation paradigms. One of the post Silicon front runners is graphene, which is a two-dimensional carbon allotrope where carbon atoms occupy the hexagon vertices and are arranged in a honeycomb lattice, as illustrated in Figure 1.1. The carbon atom forms a very strong σ bond

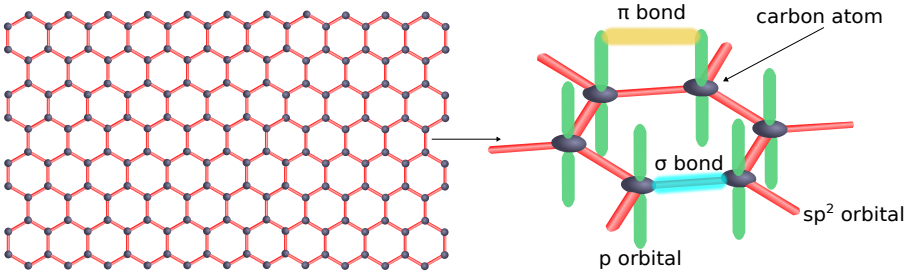

Figure 1.1: Graphene Crystal and its Chemical Bonds.

with its three neighbors via sp^2 hybridization, and the remaining p orbital constructs a π bond with adjacent carbon atoms [2], [3]. As a result, on one hand, the formed extended π-electron system in the honeycomb lattice dominates graphene's electronic conduction, and determines its electrical properties, e.g., (i) very high electron mobility at room temperature (2×10^5 $\mathrm{cm^2V^{-1}s^{-1}}$, $200\times$ higher than Si) [4], (ii) high thermal conductivity (5.30×10^3 $\mathrm{W/mK}$, $10\times$ larger than copper) [5], (iii) high electron velocity near the K (Dirac) points (1.1×10^6 $\mathrm{m/s}$) [6], (iv) high current density ($10^8\mathrm{A/cm^2}$, 5 orders of magnitude larger than copper interconnects) [7], (v) ballistic carrier transport ($> 1\,\mu\mathrm{m}$ mean free paths) [8], (vi) good electrical conductivity, (vii)

tunable electronic properties, which makes it attractive for high-speed electronic circuit applications [9], [10], [11]. On the other hand, the strength of graphene sp^2 bonds determine its chemical stability and mechanical properties, e.g., (i) thinness ($< 10\,\mathrm{nm}$) [12], (ii) stiffness, strength, and toughness (a high Young's Modulus (or Elastic Modulus) of 1 Tpa [13], [14], $2\times$ larger than silicon carbide), (iii) zero effective mass, (iv) stackable, (v) impermeable to gases [15], (vi) flexible [16], (vii) optically transparent [17], which make it a strong candidate for, e.g., electromechanical systems, strain sensors, supercapacitors, hydrogen storage, and flexible devices. These unique and outstanding electrical and mechanical properties of graphene have attracted tremendous academia and industry attention, and investigations on graphene fabrication methods and graphene-based applications have exponentially increased [18], [19], [20], [21], [22].

1.1 Graphene Synthesis and Applications

Since graphene was first unambiguously produced, identified, and reported in the celebrated paper by K. S. Novoselov and A. K. Geim [23], its fabrication enjoyed a research popularity surge as mass high-quality graphene production techniques are crucial for graphene potential exploitation. Several methods have been developed to synthesize graphene, and generally speaking, there are three main monolayer graphene fabrication approaches. (i) Thermal decomposition of SiC wafers, also called this way epitaxial growth that can deliver large-area epitaxial graphene via Si sublimation and C atoms segregation on graphitic layers [24]. The advantage of epitaxially grown graphene for nanoscale electronic applications resides in its planar two-dimensional structure, which allows for traditional top-down lithography and processing technologies [25]. However, this method is complicated, time-consuming, and expensive, due to SiC processing difficulty. (ii) Mechanical exfoliation from, e.g., Highly Ordered Pyrolytic Graphite (HOPG), and transfer onto substrates, such as $SiO2$ [26]. Mechanical exfoliation generates high-quality pristine graphene via a repetitive stick and peel process, which avoids the long processing time, high temperature, and metal catalyst required the epitaxial growth method [27]. However, mechanical exfoliation is labor intensive and limited into small (micro-scale) areas, which makes it rather inappropriate for large-scale fabrication and processing. (iii) Chemical exfoliation, e.g., Chemical Vapor Deposition (CVD) of polycrystalline graphene [28], chemical reduction of few-layered graphene oxide [29], [30], and wet-chemistry synthesis methods, e.g.,

electrochemical, graphite oxide, and liquid-phase exfoliation [31], [32], [33]. CVD and chemical reduction method offer high-quality graphene sheets in large quantity, and wet-chemistry has the advantage to produce graphene with excellent solubility that is fundamental for solution process device applications. In addition, liquid-phase exfoliation method makes graphene attractive for specific applications like printed and flexible electronics, supercapacitors, and electromagnetic shielding. However, the chemical exfoliation causes a permanent sp^2 structural damage in graphene [34], which changes pristine graphene's electrochemical behavior and degrades graphene electrical properties [35], [36]. Although current graphene manufacturing methods have their own limitations, they laid manufacturing foundations of future graphene-based devices and applications and fundamental breakthrough are still expected due to graphene research community expected endeavours.

Due to its remarkable properties and vast carbon availability, a wide range of graphene-based applications, e.g., spintronics, photonics and optoelectronics, sensors, energy storage and conversion, biomedical applications, electronics, are starting to get momentum. Owing to its room-temperature spin transport property (long spin-diffusion lengths of $\mu\mathrm{m}$ scale), adjastable carrier concentration, and high electronic mobility, graphene has very good potential of serving as spin channel material of spintronic devices [37], [38]. Graphene spintronics attempts take advantage of the large electron spin freedom degree in order to create a novel form of information storage and associated logic gates for high-speed and low-power operations. While new graphene based spin-based memories, e.g., Spin-Transfer Torque (STT) and Spin-Orbit Torque (SOT) MRAMs, are appealing [39] further experimental and theoretical exploration of, e.g., spin injection and transport, spin orbit coupling and relaxation, defect-induced magnetic moments, in order to enable the practical ralization of graphene-based spin logic devices.

Moreover, its optical transparency, flexibility, and environmental stability, encouraged graphene-based photonics and optoelectronics application research, ranging from solar cells and light emitting devices, to photo-detectors, ultrafast lasers and touch screens [40], [41]. Specifically, an organic solar cell with solution-processed graphene transparent electrodes has been proposed with a film thickness smaller than $20\,\mathrm{nm}$ and optical transmittance bigger than 80% [42]. A graphene-based broadband optical modulator with high modulation speed, small area, and big optical bandwidth has been developed at Berkeley to provide support for on-chip optical communication [43]. A chip-integrated graphene-based photodetector with ultra-fast response and broad spectral bandwidth has been introduced, which achieves a photo-responsivity

of $> 0.1\,\mathrm{AW}^{-1}$ and a response rate of 20GHz [44].

Graphene is also quite attractive for the fabrication of various sensor types, e.g., chemical and electrochemical, mass and strain, optical, electric field [45], [46], and for the detection of toxic, explosive, and flammable gases, and oxygen depletion in industry and fire-fighting. A high-performance low-power carbon dioxide (CO_2) gas sensor has been reported [47], with high-sensitivity, fast response, and short recovery time. The sensing mechanism relies on the fact that graphene conductance linearly increases with the concentration of the CO_2 adsorbed on the graphene surface. A real-time multi-channel graphene biosensor has been proposed [48], which enables reliable measurement of concentration-dependent DNA hybridization kinetics and affinity, and exhibits low cost and high throughput when compared to biosensors based on nanowire field-effect transistors. However, despite of its great promise, the road towards achieving commercial graphene-based sensors is still hindered by the limited availability of high quality and wafer-scale graphene.

Due to its ease of synthesis and functionalization graphene is also exhibiting promising potential in energy storage and conversion applications, e.g., lithium ion batteries, fuel cells, and supercapacitors. Specifically, [49] reported a novel graphene aerogel assisted method for the preparation of metal oxide nanoparticles with excellent capacitance and rate capability for supercapacitor implementations and [50] an advanced energy-storage system, "all-graphene battery", which can deliver a power density of $6450\,\mathrm{W/kg}$ while retaining an energy density of $225\,\mathrm{Wh/kg}$. Again, several key issues, e.g., effectively increasing electrode conductivity and enlarging specific surface area, remain to be addressed en route to the realization of practical graphene-based devices able to outperform conventional counterparts.

Graphene has also captured an increasing interest for biomedical applications, including biosensing and tissue engineering through graphene-quenched fluorescence, gene and drug delivery, graphene-enhanced cell differentiation and cell growth control, cancer therapy, biological imaging, and graphene-assisted laser desorption/ionization for mass spectrometry [51], [52], [53]. A nano-graphene oxide for cellular imaging and drug delivery has been developed [54], owning promising properties of large specific surface area, low cost and non-covalent interactions with aromatic drug molecules. Moreover, [55] proposed an enhanced stem cell growth and differentiation method based on graphene and graphene oxide, which provides accelerated stem cell growing due to graphene's strong non-covalent binding abilities. Those initial but very significant contributions on graphene-based biomedical and biological devices

suggest a promising future for graphene utlization in clinical assays and advanced clinical tools.

Apart of the previously mentioned applications, graphene electronics is most likely the most attractive one due to graphene's unique and remarkable electrical properties, e.g., ballistic electron transport, which make it a strong Si challenger for digital logic implementations. Its excellent electrical properties make it a promising material for high-performance, low-power, nano-scale carbon-based circuits, which are expected to play an important role in the advancement of semiconductor technology [56], [57], [58], [59], [60].

Nevertheless, the road towards graphene based nanoelectronics development is not that straightforward, mostly due to its zero bandgap and semi-metallic behavior [61]. One way to alleviate this problem is to process graphene into Graphene Nanoribbons (GNRs) [62], or Graphene Quantum Dots (GQDs) [63] and to this end GNRs have been utilized as conduction channels into graphene based Metal Oxide Semiconductor FET (MOSFET) equivalents, e.g., Graphene based Field-effect Transistor (G-FET) [64], [65], Graphene Tunnel Field-effect Transistor (G-TFET) [66], [67]. The availability of graphene MOSFETs and interconnects (graphene can exhibit metallic behavior) potentially opens the avenue towards designing and implementing all-graphene integrated circuits based on the current CMOS Boolean algebra based paradigm. However, graphene-based electronic devices based on the traditional MOSFET operation principle suffer from fundamental issues, e.g., low ON/OFF current ratio, high off-state current, high contact resistance, graphene rough edges (defects). Therefore, the development of commercial graphene-based devices and circuits requires breakthroughs for: (i) opening a distinct and well-defined graphene bandgap without degrading its electronic properties, (ii) enlarging device ON/OFF current ratios, and (iii) fabricating graphene ribbons with well-defined widths and clean edges.

1.2 Graphene Nanoribbon Logic Circuit Challenges

Graphene Nanoribbons (GNRs) are narrow graphene strips exhibiting semiconducting behavior through quantum confinement. Moreover, if produced into quasi-one-dimensional structures with sub-10 nm narrow widths and well-defiend (atomically smooth) edges, they are predicted to present a nanoribbon width and edge structure adjustable band gap, which is essential for the design of graphene-based transistors operating at room-temperature with high electron mobility, outstanding switching speed, and ballistic transport [68], [69].

However, there are a number of design and manufacturing related issues that need to be addressed, en route to GNR-based logic circuits.

From manufacturing perspective the main hurdle is the unavailability of a cost-effective, reliable large-scale (wafer-scale) GNR fabrication method to allow the mass-production of graphene structures with well-defined edges and highly reproducible features. Over the past few years, graphene researchers focused on GNR fabrication and several approaches have been developed, such as top-down lithographic patterning [70], [71], chemical procedures [72], and high quality grown carbon nanotubes longitudinally unzipping [73], [74]. Specifically, a fast and inexpensive approach to fabricate GNRs as narrow as $9\,\mathrm{nm}$ with an ON/OFF current ratio of 70 at room temperature and carrier mobility of $300\ \mathrm{cm^2V^{-1}s^{-1}}$ is presented in [75] and a surface-assisted synthesis method to produce atomically precise, low-edge-defect GNRs, e.g., 3-Armchair GNRs (1 hexagon width) and 6-Zigzag GNRs (6 hexagon width) is described in [76]. Such developments clearly indicate that GNR structures with well-defined dimensions and geometries and clean defect free edges can be potentially fabricated in the close future.

From the design standpoint, there are several graphene specific problems, which solutions are essential for the realization of competitive graphene based circuits and systems as follows:

- Identify the appropriate external means (e.g., voltage, magnetic field) to enable GNR conductance/behaviour control.
- Obtain distinguishable "ON" and "OFF" states, by means of GNR's conductivity manipulation while not degrading the intrinsic highly advantageous properties of graphene (e.g., extremely high charge-carrier mobility).
- Open a sizeable GNR energy bandgap and achieve an I_{ON}/I_{OFF} current ratio suitable for robust operation.
- Investigate alternative design styles able to take full advantage of GNR's conductance nonlinearities.
- Ensure GNR based logic structures' input output compatibility such that they can be straightforwardly connected to form larger circuits.

This thesis aims to address and provide solutions to the previously GNR-based logic circuits design related issues.

1.3 Research Questions

In this section, we formulate the research question addressed by this thesis, which in its most general form can be stated as:

- **Can graphene open alternative beyond CMOS avenues towards energy effective computing despite its band-gap opening lack?**

To provide an answer to this fundamental question we pursue a rather complex investigation by addressing 6 related questions, which are essential with regard to the general one.

The first issue one is facing when considering graphene based computing is the fact that it is a semimetal with "zero" energy bandgap ($E_g = 0$) in the Fermi level (E_F) proximity, as illustrated in Figure 1.2, which, essentially speaking, prohibits the OFF switching of graphene conduction channels in devices, such as Field Effect Transistors (FETs). Thus, a distinct bandgap ($E_g > 0$)

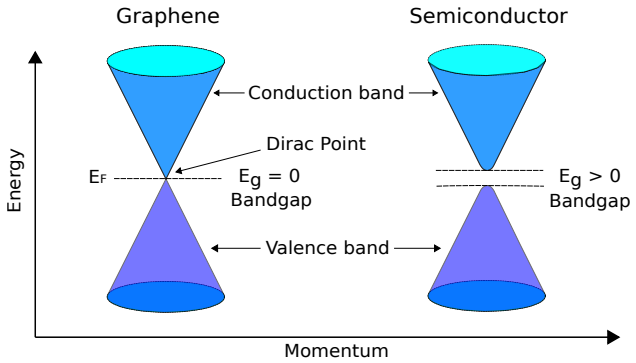

Figure 1.2: Graphene Zero Bandgap vs. Semiconductor Bandgap.

is crucial for graphene-based devices conduction control. Generally speaking, three main avenues have been undertaken to induce graphene non-zero energy bandgap: (i) internal structure chemical modification via patterned hydrogenation [77], [78] or chemical doping [79], [80], (ii) exposure to external electro-magnetic fields by means of applying perpendicular electrical field via top gate electrodes [81], [82], and (iii) topology modifications by use of, e.g., straining [83], [84], patterning [85], [86], [24], [87], and topological imperfections [88], [89].

Nevertheless, while being able to provide an energy bandgap increase these methods negatively impact graphene charge-carrier mobility and by implication limit the achievable graphene device operation speed. Thus, on one

hand, graphene high carrier mobility that potentially benefit device switching speed comes at the cost of diminished OFF switch capabilities, which results in high static power consumption, while on the other hand state-of-the-art bandgap opening methods have detrimental impact on carrier mobility. This clearly indicates that in order to make graphene a strong CMOS contender in implementing Boolean algebra based digital logic (e.g., processors and computing platforms, which, to be competitive need to build upon fast and energy effective switches), further investigations on graphene electron transport and electrical properties are required. In this context, the first to be investigated question can be formulated as:

- **Can we find a way to open GNR energy bandgap without compromising graphene excellent intrinsic properties, such as high carrier mobility?**

Such a method ought to induce a sizeable bandgap of at least $0.4\,\mathrm{eV}$ without degrading graphene intrinsic properties, and in the same time enable GNR conductance/behaviour control, in order to yield distinguishable "ON" and "OFF" states and an I_{ON}/I_{OFF} current ratio (in the order of 10^6, which is typical for low power sub-10 nm CMOS) suitable for robust operation on GNR-based devices.

While graphene based FETs able to exhibit a certain switching behaviour have been proposed [90], [91], and can potentially be utilized to construct CMOS alike logic gates and circuits such an approach is not able to take full advantage of graphene conduction nonlinearity [92], [1]. Thus our next investigation step is focused on the investigation of GNRs' potential to provide more complex than simple switching behaviours. Thus, this gives shape to the following research question:

- **Given a certain basic Boolean function can we identify a GNR topology, which conductance accurately mirrors its true table?**

The basic idea behind such an approach is to embed more computation power, e.g., 2-input (N)AND, (N)OR, X(N)OR, in one single graphene device, which potentially benefits circuit area, delay, and power consumption.

One essential element for our investigations towards energy effective graphene gates and circuits is the availability of GNR circuit-level models and simulations tools able to accurately capture graphene related physical phenomena. Therefore, in order to bring graphene specific phenomena from the physics to the circuit-level and allow for graphene-based circuit design and optimizations, a fast and parameterized model appropriate for electrical, e.g., SPICE, simulations is required. Moreover, since GNRs behavior and potential benefit

in circuits are not fully comprehended, such a model should preserve the high accuracy of low-evel physical simulation methods. In view of the previous argument, the next research question formulates as:

- **Can we devise a model able to bring GNR specific phenomena from physics to circuit level, in such a way that accurate physics formalization and fast SPICE circuit solvers can be symbiotically exploited?**

Such a model ought to build upon an accurate physical formalization and be able to symbiotically exploit accurate physics results and optimized SPICE circuit solvers (e.g., Spectre, HSPICE). Moreover, to allow for GNR gate and circuit design exploration it should be generic and has the ability to accommodate a wide range of GNR shapes and topologies as input parameters.

Equipped with bandgap opening, function mapping, and simulation methods the next investigation step focusses on the construction of energy effective GNR-based logic gates and circuits. Generally speaking, en route to such gates/circuits, there are multiple aspects which need to be taken into consideration, e.g., (i) how GNRs interact with each other when interconnected, (ii) how to combine GNRs and construct GNR-based gates/circuits which is able to perform fast and energy effective operations, (iii) how to make sure that digital GNR gates/circuits can be cascaded, i.e., achieve clean and compatible/-matching gate inputs and outputs electric levels. Thus, the next to be addressed research question is:

- **Can GNRs be combined in order to construct fast and energy effective gates and circuits, e.g., Boolean gates, full adders, and memory cells?**

The main goal inhere is to go beyond simple switching behaviour and seek gate and circuit structures able to take full advantage of the GNR potential (e.g., high electron mobility, and ballistic carrier transport) while being able to perform robust, fast, and energy effective computation.

As CMOS device dimensions are down-scaling into the sub-10nm range, temperature variations have a significant impact on devices and circuits reliability and performance, e.g., output signal integrity, propagation delay, and power consumption [93]. While for CMOS gates temperature effects have been largely investigated [94], for gates implemented with atomic-level GNRs, such effects have not been explored. Furthermore, the temperature-related electron-phonon scattering mechanisms have a significant impact on graphene electron transport behaviour and carrier mobility [95]. Moreover, even though new graphene fabrication technologies (e.g., scalable bottom-up approaches that

produce graphene by means of Chemical Vapour Deposition (CVD) [96], and on-surface synthesis methods [76]) are exceeding the precision limit of modern lithographic approach, and can manufacture atomically precise GNRs with well-defined width, e.g., 3-Armchair GNRs (1 hexagon width) and 6-Zigzag GNRs (6 hexagon width), GNR edge defects caused by non-ideal graphene fabrication process cannot be completely eliminated and may have a negative influence on GNR-based gates. In this context, we raise the following research question:

- **Can we devise performance-wise, when subjected to reliability compromising conditions commonly affecting circuit operation, e.g., temperature variation and defects, GNR Boolean gates?**

In answering the above research questions, this thesis explores and provides evidence related to graphene's potential in opening alternative beyond CMOS roads towards energy effective computing. Specifically, as presented in the next section, we investigate, propose, and evaluate techniques for GNR energy bandgap creation, GNR conductance modulation, GNR circuit-level modeling and simulation, and design of robust, fast, energy effective GNR-based gates and circuits.

1.4 Thesis Contributions

Subsequently, we summarize the contributions we made in this thesis towards the topology-induced GNR electron transport, conductance modulation, simulation model, the design of the proposed complementary GNR-based gates and computing circuits, and investigations of GNR-based gates performance robustness under temperature variations and GNR edge defects, as follows.

- We propose a graphene structure (building block) which employs a GNR as the conducting channel, and extends it with source/drain contacts and additional top/back gates as means to modulate its conduction. Further, we explore the graphene structure's ability to open the GNR energy bandgap via GNR geometry change. The simulation results show that by means of GNR geometry carving, we are able to derive a sizeable energy bandgap, e.g., butterfly GNR and waterfall GNR obtain wider energy bandgap values of $0.4\,\mathrm{eV}$ and $0.7\,\mathrm{eV}$, when compared to other methods such as periodic modulation of the graphene lattice via patterned adsorption of atomic hydrogen (i.e., an obtained bandgap is $0.4\,\mathrm{eV}$) and molecular doping (i.e., this approach results in a bandgap from $0.19\,\mathrm{eV}$

to $0.54\,\mathrm{eV}$). Thus, to some extent, we address the issue of GNR energy bandgap lack, which suggests GNR's potential as a basic building block for future carbon-based electronic circuits and applications.

- We investigate various GNR geometries and contact topologies influence on the GNR-based structure's conductance and current characteristics by means of the NEGF-Landauer formalism. The simulation results exhibit that the GNR width has a remarkable impact on GNR conductance, while length has little effect on conductance. For butterfly GNR configuration, the narrow and short constriction channel is more efficient to obtain a high current ratio, up to 2.1×10^4. To account for angle between constriction channel and Drain/Source contact for butterfly GNR, the bigger angle can achieve better current ratio. In addition, longer and wider bump structure provides better current ratio, up to 1.5×10^4 for Camel GNRs, and the bump configurations improve the current related characteristics for Double butterfly GNRs, e.g., the current ratio is up to 2.4×10^4. Last, we explore the ability of gate bias, top gate V_{g} and back gate V_{back} to control GNR conduction. The simulation results suggest the top/back gate contacts are good enough ways to modulate the GNR-based device conduction, e.g., gate contact improves current ratio up to 2.3×10^7 for Waterfall GNRs. Thus, we can derive higher current ratio for Non-rectangular GNR, up to 10^7, when compared to 10^2 of rectangular GNRs and 10^6 of traditional low-power sub-$10\,\mathrm{nm}$ Si process.
- We present a methodology of encoding the desired Boolean logic transfer function into the graphene electrical characteristics, e.g., conduction maps, by performing a Design Space Exploration (DSE) with regard to GNR topologies and geometries. In particular, we introduce a butterfly GNR structure by augmenting the trapezoidal Quantum Point Contact (QPC) topology with two top gates such that we can modulate its conductance via external voltages. Subsequently, we take into account the basic set of Boolean functions (INV, BUF, AND, NAND, OR, NOR, XOR, XNOR), and for each function we identify a GNR topology capable providing a conductance map (conductance G as output vs. two top gate voltages as inputs) mirroring the relative Boolean function truth table in which high G stands for logic output "1" and low G represents logic output "0". The simulation results indicate that the proposed 2-input butterfly GNR-based structures operating at $V_{\mathrm{DD}} = 0.2\,\mathrm{V}$ surpass $7\,\mathrm{nm}$ FinFET CMOS counterparts running at $V_{\mathrm{DD}} = 0.7\,\mathrm{V}$ by up to 2, 2 and 4 orders of magnitude in terms of propagation delay, power consumption, and power-delay product, respectively, while requiring 2

orders of magnitude less active area. Particularly, for 3-input Boolean function, the proposed GNR-based approach proves to be even more effective, i.e., up to 3, 2, and 4 orders of magnitude in terms of propagation delay, power consumption, and power-delay product, respectively. Furthermore, the proposed method is less sensitive to gate fan-in scaling, as when incrementing it from 2 to 3, the GNR structures obtain 26% and 42% variation for area and delay, respectively, while CMOS area footprint and delay increase by up to 100% and 51%, respectively. Thus, this suggests that the GNR-based sructure's excellent potential of serving as a potent candidate to replace CMOS in the future high-performance energy-effective post-Si nanoelectronics.

- We evaluate the effect of V_{DD} variation on the GNR-based structure's conductance and delay, and further to determine V_{DD} lower bound for proper operation. The experiments indicate the proposed GNR-based structures have a strong robustness with respect to V_{DD} variation, e.g., the GNR conductance and delay for butterfly GNR structure that reflects NOR function, change by no more than 2% and 6%, respectively. In addition, to account for V_{DD} lower bound value, the NOR GNR structure is able to operate even at $10\,\mathrm{mV}$. Further, we explore GNR edge defects influence on butterfly GNR conductance. The simulation results reveal that rather substantial even due to one missing atom in the constriction edge, and despite the performance degradation, the GNR-based structure is still able to deliver the expected Boolean functionality. This suggests the proposed GNR-based structure potential of performing robust operations related to V_{DD} variation and GNR edge defects.

- We develop a parameterized Verilog-A SPICE-compatible generic model based on NEGF-Landauer formalism which builds upon an accurate physics formalization, by computing GNR specific variables, e.g., conductance, current, via internally called Simulink code. In this way, the proposed GNR model symbiotically exploits accurate physics results from Matlab Simulink and optimized SPICE circuit solvers (e.g., Spectre, HSPICE). This model enables parameterized electrical simulations for GNR-based structures, and preserves the physical simulation accuracy degree. In addition, the parameterized model allows for graphene-based circuit design and optimizations, which suggests the model potential of bringing GNR specific phenomena from the physics to the circuit-level by fully comprehending the GNRs behavior and potential benefit in the circuit context. In order to validate and evaluate the proposed model applicability, we take into account a simple test case circuit and

the GNR-based 2-input XOR gate, and simulate the afferent I-V characteristic via Cadence Spectre and Matlab Simulink. The simulation results indicate that our proposed Verilog-A GNR model is accurate and enables the accurate evaluation of graphene-based circuits potential performance.

- We propose a methodology of constructing graphene-based Boolean gates and circuits. To this end, we make use of two complementary GNRs, i.e., a pull-up GNR performing the targeted Boolean function and a pull-down GNR operating its inverse Boolean function. Each GNR structure has a conduction channel made of a GNR with zigzag edges, which is situated between the drain and source contacts. The gate primary inputs voltages are applied via top gates. Subsequently, we conduct a special Design Space Exploration with regard to GNR dimensions (geometries) and gate contact topologies, while abiding to particular constraints: (i) gate output voltage values which are compatible with gate input voltage values, and (ii) high ratio between the high and low GNR conductance values, in order to identify the specific GNRs with desired functionalities. The proposed 1-, 2-, and 3-input complementary GNR gates are validated in Cadence by means of SPICE simulation which employs a Verilog-A model that calls internally a Simulink model. we obtain up to 2 orders of magnitude smaller propagation delay, 3 orders of magnitude lower power, and 2 orders of magnitude smaller active area footprint, when compared to 7nm FinFET CMOS counterparts. In addition, we prove that contrary to CMOS designs, the proposed GNR-based gates can yield effective power-delay trade-offs, at approximately the same area. We observe that this is because the graphene conductance main contributor is the nanoribbon geometry and its overall topology, rather than the effective area, thus the required active area is not proportional with gate's function complexity and fan-in. In particular, the proposed GNR gates provide clean and compatible/-matching gate inputs and outputs electric levels. Therefore, the obtained results suggests the graphene-based gates surpass the CMOS counterparts in terms of delay, power and area, and have a promising potential of serving as the basic building blocks for future fast, energy-effective, high-dense carbon-based integrated circuits.
- We present a GNR-based 1-bit Full Adder (FA) and a SRAM cell, as they currently constitute the foundation for the construction of any computation system. In particular, we design a 3-input MAJORITY gate which apart of being able to directly compute FA's Carry-Out, which

surpasses the CMOS equivalent Carry-Out calculation circuit by up to 2 orders of magnitude smaller delay and 3 orders of magnitude lower power consumption, while requiring 2 orders of magnitude less area. The proposed FA design provides $6\times$ smaller delay, 3 orders of magnitude less power consumption, while requiring 2 orders of magnitude less area, when compared to 7nm FinFET CMOS counterpart. By consequence, a GNR-based n-bit Ripple Carry Adder, which performance is linear in the Carry-Out path, will be $108\times$ faster than a CMOS implementation. Particularly, the proposed GNR-based SRAM cell achieves a better resilience to DC noise characteristics than the CMOS equivalent, while obtaining $3.6\times$ smaller delay, 2 orders of magnitude less power, and 1 order of magnitude less area. The proposed GNR FA and SRAM cell clearly reveal that GNR-based implementations can potentially outperform CMOS counterparts and that the proposed approach is opening a promising avenue towards future energy-effective carbon-based nanoelectronics.

- We extend a NEGF-Landauer simulation framework with the self-consistent Born approximation, while taking into account the temperature-induced phenomena, i.e., electron-phonon interactions for both optical and acoustic phonons, where NEGF calculations describe the electron-electron interaction and the Landauer formula provides the GNR device current and conductance. Subsequently, we evaluate the considered complementary graphene-based Boolean gates behavior under a set of temperatures from $-55°C$ to $125°C$ which covers the commercial, industrial and military ranges, and further investigate the temperature variation impact on GNR-based gates reliability and performance in terms of output signal integrity, input-to-output propagation delay, and power consumption by means of SPICE simulation in Cadence. We observe that the proposed GNR-based complementary gates are robust with respect to temperature variation, and even in the worst temperature condition (at $125°C$) outperform 7nm CMOS FinFET counterparts operating at room temperature, which suggesting the GNR-based gates' potential as basic building cells for future reliable, low-power, nanoscale carbon-based electronics and applications.

1.5 Thesis Organization

The remainder of the thesis is structured in 6 chapters, as follows:

In **Chapter 2**, we present a graphene structure and explore its ability to open a sizeable energy bandgap via GNR geometry carving and applied top/back gate voltages. Moreover, we design five different GNR shapes with zig-zag edges, and investigate the GNR geometry influence on its conductance and current characteristics. Last, we explore the ability of gate bias (e.g., top gates and back gate) to control GNR conduction.

In **Chapter 3**, we consider a basic set of Boolean functions (e.g., INV, BUF, AND, NAND, OR, NOR, XOR, XNOR) and perform DSE with regard to GNR dimensions and topologies, such that for each function we find out a GNR structure which is able to provide a conductance density map reflecting the relative Boolean function truth table (e.g., high G for logic output 1, low G for logic output 0). Subsequently, we investigate the effect of V_{DD} variation, and determine V_{DD} lower bound value. Last, we discuss GNR fabrication status, difficulties and challenges, and investigate GNR edge defects influence on GNR conductance and performance figures of merit.

In **Chapter 4**, we develop a fast, accurate and parameterizable Verilog-A SPICE-compatible generic model for the GNR-based structure simulations, which computes the GNR conductance by means of NEGF-Landauer formalism called from within the Verilog-A code. We validate the model accuracy and versatility by utilizing Simulink assisted Cadence Spectre simulation of a simple test case GNR-based circuit and a GNR-based 2-input XOR gate.

In **Chapter 5**, we introduce a methodology of designing GNR Boolean gates by means of two complementary GNRs in which a pull-up GNR performs the targeted Boolean function and a pull-down GNR implements its inverse. Subsequently, we propose and evaluate the 1-, 2- and 3-input GNR gates via the proposed SPICE simulation. Further, we present GNR-based designs of 1-bit Full Adder (FA) and SRAM cell, as they currently constitute the foundation for the construction of any computation system.

In **Chapter 6**, we extend the NEGF-Landauer simulation framework with the self-consistent Born approximation in order to taking into account the temperature-induced phenomena, i.e., electron-phonon interactions for both optical and acoustic phonons. Next, we evaluate the graphene-based complementary Boolean gates behavior under a set of temperatures by means of SPICE simulation in Cadence, and further explore the temperature variation impact on their reliability and performance (e.g., output signal integrity, prop-

agation delay, and power consumption).

Chapter 7 summarizes the thesis, and provides possible directions for future work.

2

Topology Induced Graphene Nanoribbon Electron Transport

Graphene Nanoribbons (GNRs) owing to graphene's remarkable electronic properties may serve as basic blocks for post-Si nanoelectronics. En route to GNR-based logic circuits, finding a way to open GNR energy bandgap and to externally control GNR's conduction with a high current ratio $I_{\text{on}}/I_{\text{off}}$ is the main desideratum. To this purpose, we design five different GNR shapes with zigzag edges (Rectangular, Butterfly, Double Butterfly, Camel, Waterfall GNRs) and build upon a GNR-based building block by extending it with additional top gate and back gate, and then investigate GNR geometry and contact topology influence on its conductance and current characteristics by means of the Non-Equilibrium Green Function (NEGF)-Landauer formalism with a 3D Poisson solver. The simulation results show that by means of GNR geometry carving, we are able to open GNR energy bandgap (e.g., Butterfly GNR and Waterfall GNR obtain wide energy bandgap $0.4\,\text{eV}$ and $0.7\,\text{eV}$, respectively). For Butterfly GNR, the narrow and short constriction channel (small W_{c} and L_{c}) is more helpful to obtain a high $I_{\text{on}}/I_{\text{off}}$ (up to 2.1×10^4). For Double Butterfly GNR and Camel GNR, the bump structures help improve $I_{\text{on}}/I_{\text{off}}$ (up to 2.4×10^4 and 1.5×10^4, respectively). Furthermore, our experiments suggest that top/back gates have a big influence on the GNR conductance and $I_{\text{on}}/I_{\text{off}}$ (e.g., provide a high $I_{\text{on}}/I_{\text{off}} = 2.3 \times 10^7$ for Waterfall GNR), which suggests the applied top/back gate contacts are good methods for controlling the GNR-based device conduction, establishing GNR's potential as basic building block for future GNR-based logic circuits.

2.1 Introduction

Graphene Nanoribbons(GNRs) are strong candidates for device conduction channel implementations with one caveat characteristic to pristine graphene, i.e., the absence of an intrinsic energy bandgap in the proximity of the Fermi level [97], [90], [98]. Such a bandgap is fundamental for conductivity control via electronic means (e.g., applied gate voltages), in order to create distinguishable "ON" and "OFF" states in digital electronics [99], [100], [101].

To induce a graphene energy bandgap, three main avenues have been typically undertaken: (i) chemical modification of graphene's internal structure by means of, e.g, patterned hydrogenation [77], [78], chemical doping [79], [80], (ii) multilayer graphene exposure to external electro-magnetic fields, e.g., applying perpendicular electrical field via top gate electrodes [81], [82], and (iii) topology modifications, e.g., straining [83], [84], patterning [86], [24], [87], generating topological imperfections, such as stone-wale defects [88], [89]. For example, it was demonstrated that: (i) periodic modulation of the graphene lattice via patterned adsorption of atomic hydrogen opens a bandgap of ≈ 0.4 eV [102], (ii) molecular doping results in a bandgap magnitude ranging from 0.19 eV to 0.54 eV [103], [104], [105] and (iii) bilayer graphene exhibits a non-zero bandgap, modulated by an external electric field applied perpendicularly to the graphene layers, while multilayer (≥ 3 layers) graphene under electric field lacks any appreciable induced energy bandgap [106], [107].

All the above approaches with the exception of chemical modification have been proved unable to open an energy bandgap wider than $0.4\,\mathrm{eV}$, which means that graphene based switches can have at most a current ratio $I_{\text{on}}/I_{\text{off}}$ in the order of 10^3, as opposed to $10^6 - 10^7$ which is the typical ratio for low power nano-level Si process. Moreover, with the energy bandgap increase these methods negatively impact the charge carrier mobility. Thus, the high carrier mobility exhibited by graphene (which can greatly benefit the devices switching speed) comes at the expense of diminished ability to switch off the devices, which further results in high static power consumption figures (uncompetitive with low-power CMOS). This suggests that in order to make graphene a strong CMOS contender in implementing Boolean algebra based digital logic (e.g., processors and computing platforms, which to be competitive need to build upon fast and energy effective switches), further investigations are required. While finding a better way to open GNR's energy bandgap and to achieve a high $I_{\text{on}}/I_{\text{off}}$ is the main desideratum, achieving it requires a better understanding of the relation between GNR's conduction and its shape (dimensions and geometries), which is the focus of the investigation presented

in this chaper.

In order to address the GNR zero energy bandgap and low current ratio problem, we build upon a graphene building block by extending it with source/drain contact and additional top/back gates as means to modulate its conduction. First, we explore the ability to open the GNR energy bandgap via GNR geometry change or through applied top/back gate voltages. The experimental results show that the method by GNR geometry change can make the GNR energy bandgap wider open (e.g., Butterfly GNR gets a wide bandgap $0.4\,\mathrm{eV}$ and Waterfall GNR obtains a wider band gap $0.7\,\mathrm{eV}$).

Second, we design five different GNR shapes with zig-zag edges Rectangular GNR (R-GNR), Butterfly GNR (B-GNR), Camel GNR (C-GNR), Waterfall GNR (W-GNR) and Double Butterfly GNR (DB-GNR) and investigate the GNR geometry influence on its conductance and current characteristics. To this end, we consider various GNR configurations by carving GNR geometries W, L, W_{c}, L_{c}, W_{b}, L_{b}, and derive GNR conductance and current by means of the NEGF-Landauer formalism. The experimental results suggest that W has a remarkable impact on GNR conductance G, while L has little effect on G. Normally, for B-GNR configuration, the narrow and short constriction channel (smaller W_{c} and L_{c}) is more helpful to obtain a higher $I_{\mathrm{on}}/I_{\mathrm{off}}$ (up to 2.1×10^4). With respect to angle between constriction channel and Drain/Source contact for B-GNR, the bigger angle can achieve better $I_{\mathrm{on}}/I_{\mathrm{off}}$ (e.g., GNR with 60° has $92\times$ bigger $I_{\mathrm{on}}/I_{\mathrm{off}}$ than GNR with 22°). However, for C-GNR case, longer and wider bump yields better $I_{\mathrm{on}}/I_{\mathrm{off}}$ (up to 1.5×10^4). Furthermore, for DB-GNR case, the bump configurations can help improve the current related characteristics (e.g., $I_{\mathrm{on}}/I_{\mathrm{off}}$ is up to 2.4×10^4).

Last, we explore the ability of gate bias (e.g., top gate V_{g} and back gate V_{back}) to control GNR conduction. The results show that V_{back} modulates the Fermi level for the energy at the Dirac point, thus the back-gated GNR can enable a higher $I_{\mathrm{on}}/I_{\mathrm{off}}$ ($10\times$ bigger when compared to top-gate controlled GNR). In addition, V_{g} has also a big impact on $I_{\mathrm{on}}/I_{\mathrm{off}}$. The experimental results suggest the top/back gate contacts are good methods to control the GNR-based device conduction (e.g., gate contact improves $I_{\mathrm{on}}/I_{\mathrm{off}}$ up to 2.3×10^7 for W-GNR).

The remaining of this chapter is structured as follows: Section 2.2 presents the theoretical formalism to compute the GNR electronic ballistic transport. Section 2.3 entails an overview of the GNR geometries and topologies in our experiments. Section 2.4 illustrates the means to open the energy bandgap: via GNR geometry change or through applied gate voltages. The simulation results are shown in Section 2.5. Finally, some concluding remarks are given

in Section 2.6.

2.2 Graphene Nanoribbon Modelling & Simulation

Like the mythological Janus, graphene nanoribbons have two personae determined by the lattice orientation: (i) Zig-Zag graphene nanoribbon (Z-GNR), which is always metallic due to its near the Fermi level localized state and (ii) Armchair graphene nanoribbon (A-GNR), which is metallic or semiconducting depending on its ribbon width [108]. For the purpose of our investigation only Z-GNRs are relevant and as such in the sequel we study carrier transport properties inside single layer Z-GNRs, as the one depicted in Figure 2.1.

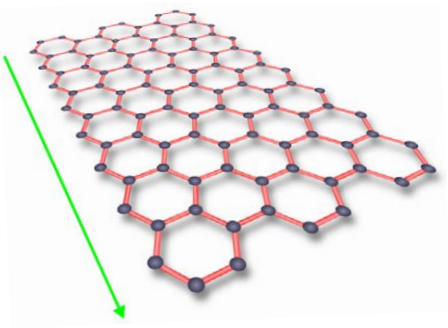

Figure 2.1: Zig-Zag GNR Configuration.

To capture the GNR specific electronic ballistic transport we make use of the Non-Equilibrium Green Function (NEGF) – Landauer formalism, which builds upon the NEGF quantum transport methodology, the tight-binding Hamiltonian model and the Landauer formula to compute GNR's conductance and current-voltage characteristics. In addition, we utilize a 3D Poisson solver to self-consistently calculate the GNR potential by means of finite difference method [109], [110]. As discussion vehicle we make use of a conduction channel formed by a GNR placed between two electrodes as depicted in Figure 2.2, which is described by a Hamiltonian matrix H incorporating all internal and external potentials. In our simulations, we construct H by using semi-empirical tight-binding model computations, as follows:

$$H = \sum_{i,j} t_{i,j} \left|i\right\rangle \left\langle j\right|, \tag{2.1}$$

where $t_{i,j}$ is computed as:

$$t_{i,j} = \begin{cases} \tau, & \text{if } i \text{ and } j \text{ atoms are adjacent,} \\ 0, & \text{otherwise.} \end{cases} \tag{2.2}$$

In general, $\tau = -2.7\,\text{eV}$ [110]. On the channel sides the two contacts with different electrochemical potentials u_1 and u_2, sustain the channel conduction and their interaction with the channel is modelled via the left and right contact self-energy matrices Σ_1 and Σ_2, respectively.

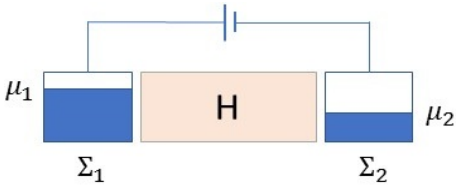

Figure 2.2: General Simulation Model.

After H, Σ_1 and Σ_2 are derived, $T(E)$ which models the probability of one electron being transmitted between the two end contacts is computed as a function of energy E via:

$$T(E) = trace(\Gamma_1 G_R \Gamma_2 G_R^\dagger). \tag{2.3}$$

where $G_R(E)$ is the retarded Green's function with energy E and $G_R^\dagger$ is the transpose of G_R. $\Gamma_{1,2}$ are the left and right contact broadening factors, which are numerically computed via:

$$G_R(E) = [EI - H - \Sigma_1 - \Sigma_2]^{-1}, \tag{2.4}$$

$$\Gamma_{1,2} = i \cdot [\Sigma_{1,2} - \Sigma_{1,2}^\dagger], \tag{2.5}$$

respectively, where I is the identity matrix and H GNR's tight-binding Hamiltonian matrix.

The current to flow along the GNR is then derived based on the Landauer formula, as follows:

$$I = \frac{q}{h} \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E - \mu_1) - f_0(E - \mu_2))\ \mathrm{d}E, \tag{2.6}$$

where q and h are the electron charge and Planck's constant, respectively. Moreover, $f_{1,2}(E)$ are the Fermi functions corresponding to the left and right contacts, respectively, computed via:

$$f_{1,2}(E) = \frac{1}{1 + \exp((E - u_{1,2})/(K_B T))}, \tag{2.7}$$

where K_B and T are the Boltzmann constant and the experimental temperature.

Assuming that the end contacts are biased by V_d and V_s, the channel conductance is derived according to Ohm's law as follows:

$$G = \frac{I}{V_\mathrm{d} - V_\mathrm{s}}. \tag{2.8}$$

2.3 Graphene Nanoribbon Topologies

Figure 2.3 depicts on its left side a Rectangular GNR (R-GNR) with zig-zag edges, and on its right side the basic unit of the graphene lattice (a carbon atoms hexagon with $a = 0.142\,\mathrm{nm}$ side). The length and the width of one

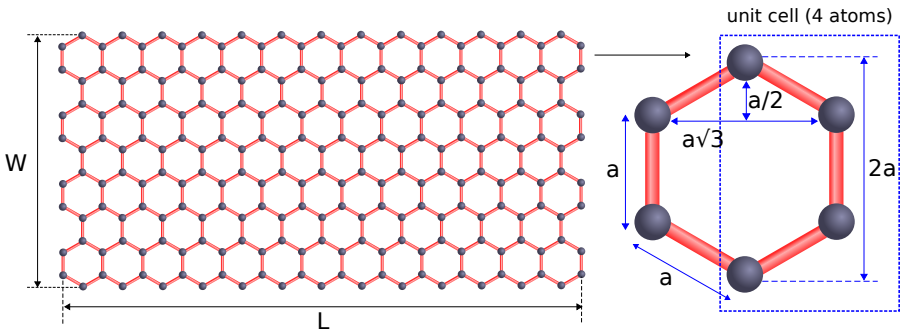

Figure 2.3: Rectangular GNR and Unit Cell.

carbon hexagon are $a\sqrt{3}$ nm and $2a$ nm. In our experiments, we define the right 4 atoms of a hexagon as a Unit Cell (UC). To express GNR's width/length we make use of Row/Column UC (RUC, CUC) as basic units, thus the GNR in Figure 2.3, has $W = 4$ RUC and $L = 13$ CUC.

The actual length or width of a GNR (unit is [nm]), is calculated as:

$$Length = L \cdot \sqrt{3} \cdot a \tag{2.9}$$

and

$$Width = (3 \cdot W - 1) \cdot a. \tag{2.10}$$

As nanoribbons can be patterned we consider in our investigation, besides rectangular GNR, we design and investigate four GNR shapes: Butterfly GNR (B-GNR), Camel GNR (C-GNR), Double Butterfly GNR (DB-GNR) and Waterfall GNR (W-GNR), as depicted in Figure 2.4, in order to address the zero bandgap and poor current ratio associated with the rectangular structure. As

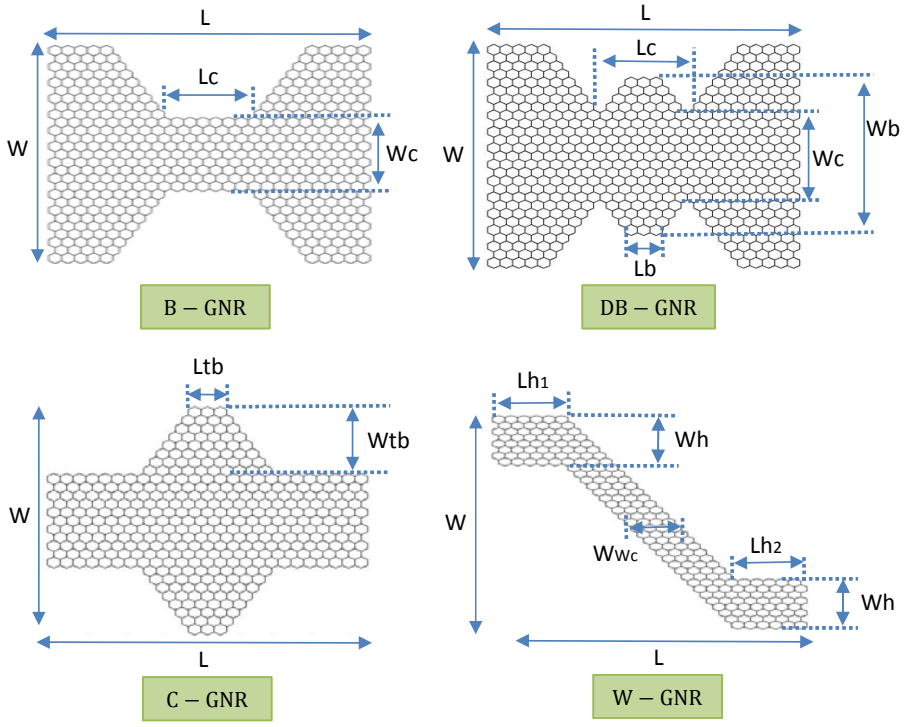

Figure 2.4: Non-rectangular GNRs.

indicated in the Figure, each geometry is described by global Width W and Length L, and, when applicable, by Constriction Width W_{c} and Length L_{c}, Bump Width W_{b} and Length L_{b}, Top Bump Width W_{tb} and Length L_{tb}, or outer and inner boundary Head Length L_{h1} and L_{h2}, Head Width W_{h} and Channel Width W_{wc}.

Apart of biasing the GNR by applying V_{s} and V_{d} on the source and drain contacts its conductance can be also modulated by means of electrostatic interaction (e.g., a top gate voltage V_{g}). As illustrated in Figure 2.5, we design

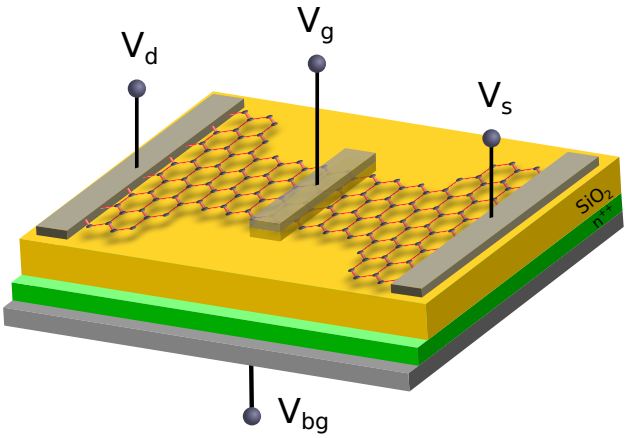

Figure 2.5: 3D GNR Structure [1].

a GNR-based building block and employ the butterfly GNR as its conduction channel, through which the current flow is induced by applying a bias voltage ($V_{\mathrm{d}} - V_{\mathrm{s}}$) between the two end-point contacts, and is modulated by the top gate. In our experiment we set the width of action of each of these voltages to $3\sqrt{3}a$ (3 unit cell width). In addition, a back bias voltage V_{back} is applied beneath the GNR, which in manufactured devices is typically a small fraction of the back gate potential, i.e., V_{bg} (because of the significant potential drop on the dielectric layer - usually SiO_2 - residing underneath the graphene ribbon). For all the other shapes we use the same approach to apply the voltages on the GNRs.

In the next section we used the Non-Equilibrium Green Function - Landauer formalism described in Section 2.2, to simulate the previously described GNRs to investigate how their geometry influences their electronic transport properties (conductance and current), and demonstrate that geometry has a crucial role in shaping GNR's conduction and energy bandgap opening.

2.4 Energy Bandgap Opening

As Z-GNRs are always metallic, due to energy bandgap absence, one needs to find a way to create bandgap in order to design GNR-based devices/switches. In this section we investigate the potential effect of Z-GNR geometry change and/or external bias on bandgap formation and width.

2.4.1 Via GNR Geometry Change

To observe the bandgap existence we set all bias voltages (V_s, V_d, V_g, V_back) to $0\,\mathrm{V}$ for the considered GNR shapes (R-GNR, B-GNR, C-GNR, W-GNR and DB-GNR) and use the NEGF - Landauer formalism to compute their conductance as a function of energy E. Figure 2.6, depicts the conductance G plot for an R-GNR with $W = 12$ and $L = 25$, where E_F is the Fermi level, τ atom hopping energy ($\tau = -2.7\,\mathrm{eV}$ in our case), h Planck's constant, and q the electron charge. The Figure presents zero energy bandgap as there is no energy level for which the conductance curve touches Y axis ($G = 0$).

However, Figure 2.7 indicates that B-GNR, C-GNR, DB-GNR and W-GNR (dimensions are mentioned in the figure) exhibit a bandgap of $0.4\,\mathrm{eV}$, $0.25\,\mathrm{eV}$, $0.12\,\mathrm{eV}$, and $0.7\,\mathrm{eV}$, respectively. While this suggests W-GNR as the best option, one has to consider also the high conductance capability for which C-GNR is in leading position. Thus, we can conclude that a reasonably large bandgap can be opened at zero external energy cost by GNR shaping and a tradeoff exists between high conductance value and energy bandgap width.

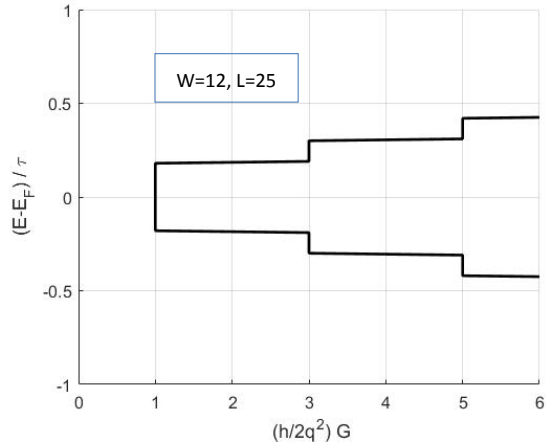

Figure 2.6: R-GNR Conductance G vs. Energy E.

2.4.2 Via Applied Gate Voltages

Bandgap can be also opened by means of electrostatic interaction and to demonstrate this we consider an R-GNR with $W = 12$ and $L = 25$, set V_s, V_d, V_back $0\,\mathrm{V}$, and vary V_g from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$. Figure 2.8(a) depicts G function of E for a $3\sqrt{3}$ a gate width at $V_\mathrm{g} = 1\,\mathrm{V}$ and indicates the presence of a very

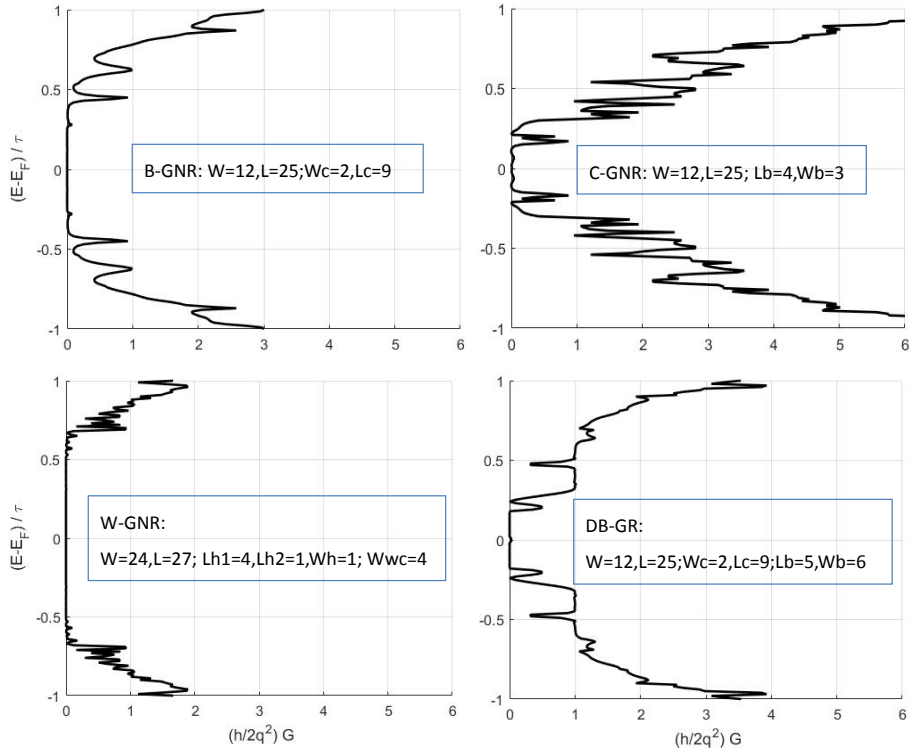

Figure 2.7: GNR Conductance vs. Energy.

small energy bandgap, which means that top gate voltage has little influence on energy bandgap formation. Intuitively speaking increasing gate width might enforce a better but Figure 2.8(b), which presents the conductance curve for a gate width of $7\sqrt{3}$ a is not providing evidence to sustain this. Back bias can also be utilized but as indicated in Figure 2.9 it shifts the Fermi Energy up or down for the positive or negative V_{back} values, respectively, without changing the G vs E curve shape.

Thus far we addressed the bandgap creation issue and demonstrated that GNR shape plays a crucial role in this matter while external electrostatic interaction is not an effective solution. In the sequel we focus on the influence of GNRs dimensions of their conduction capabilities.

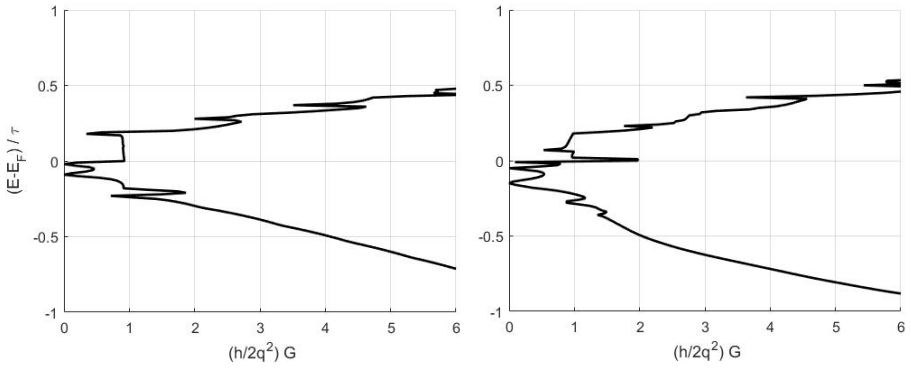

Figure 2.8: Conductance vs. Energy for R-GNR with Geometry $W = 12$, $L = 25$, $V_{\mathrm{g}} = 1\,\mathrm{V}$, $V_{\mathrm{back}} = 0\,\mathrm{V}$ and Different Gate Widthes.

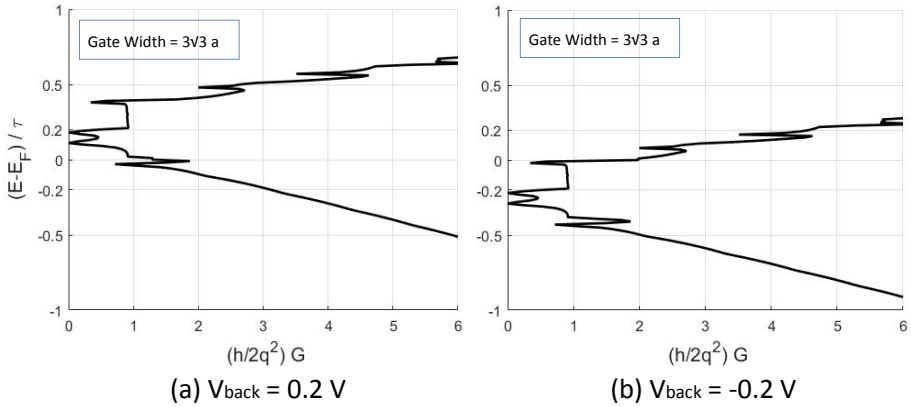

Figure 2.9: Conductance with Energy for R-GNR with Geometry $W = 12$, $L = 25$ and $V_{\mathrm{g}} = 1\,\mathrm{V}$, $V_{\mathrm{back}} = \pm 0.2\,\mathrm{V}$.

2.5 GNR Conductance Dependence on Dimensions

In this section we instantiate R-GNR, B-GNR, C-GNR, DB-GNR and W-GNR shapes with various geometries and evaluate their conduction under different bias conditions. The goal inhere is to identify the key geometrical parameters for each shape and create the foundation of a design exploration strategy that can potentially help us to identify the most appropriate topology for certain design constraints in terms of, e.g., bandgap width, maximum conductance, high current ratio. We rely again on the Non-Equilibrium Green Function -

Landauer formalism to derive GNR's conductance and current.

2.5.1 Conductance vs. W vs. L for Rectangular GNRs

In this section, we evaluate the electronic transport properties of several R-GNR configurations with $W = 8, 10, ..., 26$ and $L = 13, 15, ..., 25$. Figure

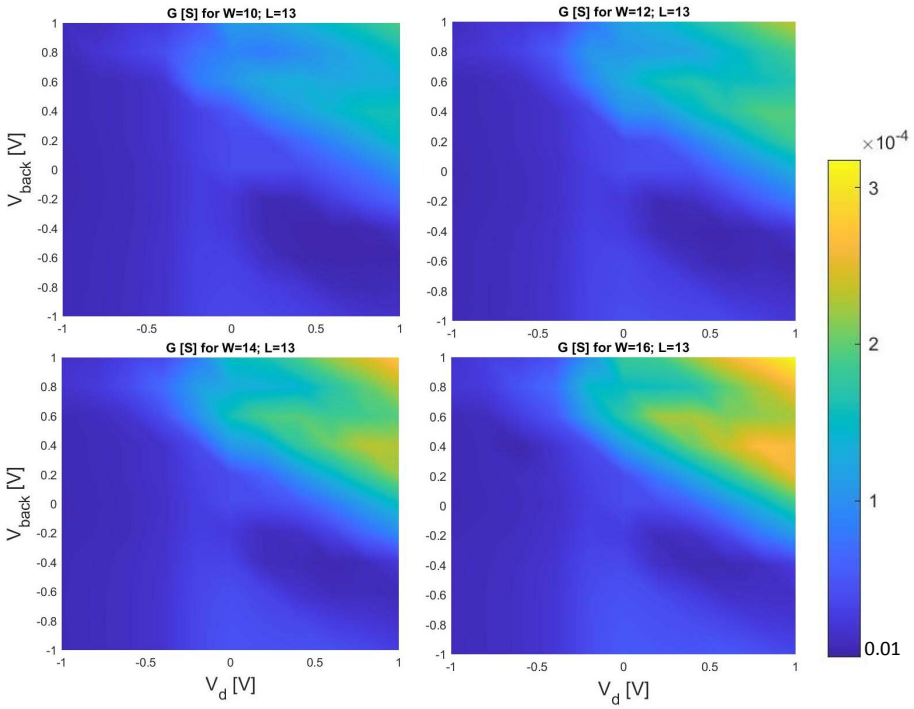

Figure 2.10: G vs. V_{back} vs. V_{d} for $W = 10, 12, 14, 16$.

2.10 presents conductance maps (G versus V_{d} and V_{back}) for R-GNRs with fixed $L = 13$, variable $W = 10, 12, 14, 16$, respectively, and $V_{\text{g}} = V_{\text{s}} = 0\,\text{V}$. One can observe that conductance increases with W (much obviously in the region V_{back}=[0V, 1V] and V_{d}=[0V, 1V]). The highest conductance value is $3.2 \times 10^{-4}\,\text{S}$ for GNR topology ($W = 16$, $L = 13$, $V_{\text{d}} = 1\,\text{V}$ and $V_{\text{back}} = 1\,\text{V}$), and its lowest conductance is $2.5 \times 10^{-6}\,\text{S}$ for GNR ($W = 10, L = 13$, $V_{\text{d}} = 0.6\,\text{V}$ and $V_{\text{back}} = -0.6\,\text{V}$). Furthermore, we also derive the conductance maps for other R-GNR configurations with fixed $W = 10$, but variable $L = 15, 17, 19, 21, 23, 25$. we observe 6 similar plots with the one (which has topology with $W = 10, L = 13$) in top left corner of Figure 2.10, indicating

that when increasing L from 13 to 25 and keeping $W = 10$, the conductance remains almost unchanged. Based on this we can conclude that W significantly influences G while L has very little effect on it. Subsequently, in order

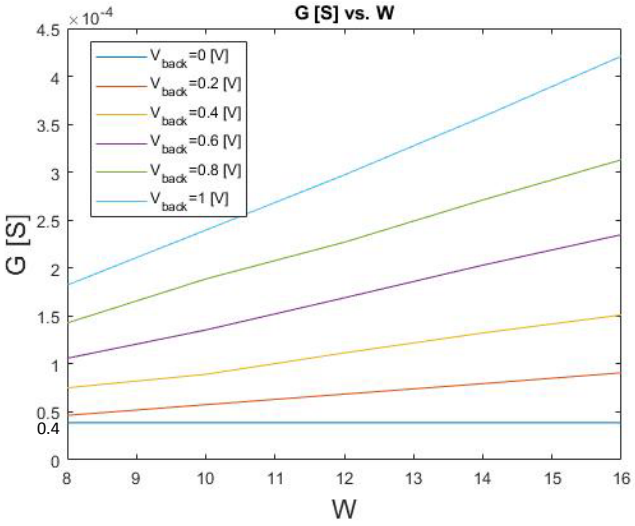

Figure 2.11: G vs. W with Variable V_{back}.

to validate such conclusion we obtain the conductance with variable W (from 8 to 16) for fixed $L = 25$, $V_{\text{d}} = 0.2\,\text{V}$, $V_{\text{g}} = 0\,\text{V}$, $V_{\text{s}} = 0\,\text{V}$ and variable $V_{\text{back}} = 0, 0.2, 0.4, 0.6, 0.8, 1\,\text{V}$, as plotted in Figure 2.11. It indicates linearly G increase with W for fixed V_{back} value, and the larger V_{back} the higher the conductance. Specially, the conductance remains almost the same value for $V_{\text{back}} = 0$ and the conductance variation is less than 0.1%, while for $V_{\text{back}} = 1$ the conductance variation is 130.9%. In addition, we derive the conductance G with variable L (from 13 to 25) for fixed $W = 16$, and the same applied external voltages as the setting in Figure 2.11. The results indicates that G is practically independent on L.

Further, we obtained similar results for the other four GNR shapes (B-GNR, C-GNR, W-GNR and DB-GNR), thus one can conclude that the W and V_{back} have major impact on GNR conductance while for given W and V_{back} values, G is practically constant with respect to L.

2.5.2 Conductance vs. W_c vs. L_c for Butterfly GNRs

In this section we assume as discussion vehicle the B-GNRs with topology $L = 25$, $W = 14$ or 18, constriction width W_c (from 3 to 15) and constriction length L_c (from 1 to 9), and simulate these GNRs under different bias conditions (V_d, V_s and V_{back}) to explore variable GNR structures with different constriction parameters (W_c and L_c) influence on B-GNR's conductance G.

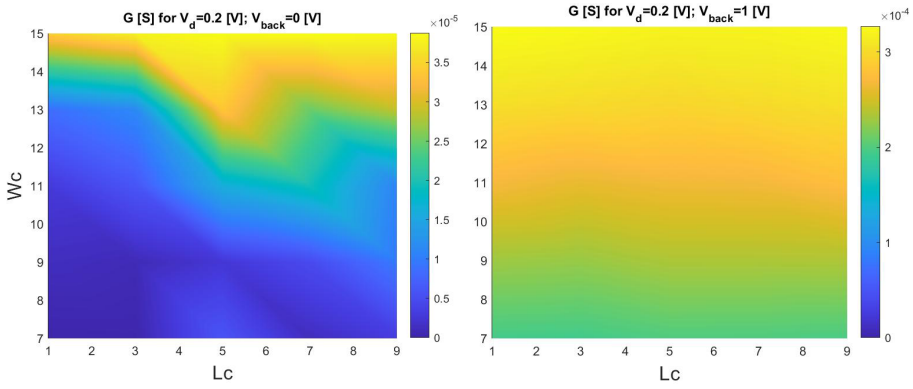

Figure 2.12: G vs. L_c and W_c for $V_d = 0.2\,\text{V}$, $W = 18$ at $V_{back} = 0\,\text{V}$ and $1\,\text{V}$.

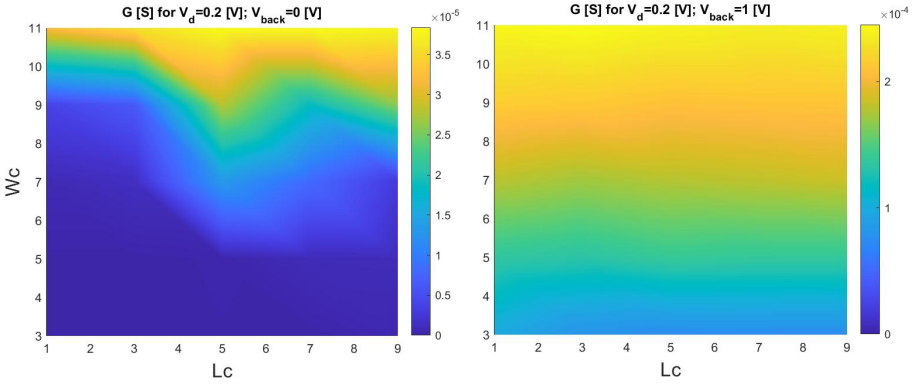

Figure 2.13: G vs. L_c and W_c for $V_d = 0.2\,\text{V}$, $W = 14$ at $V_{back} = 0\,\text{V}$ and $1\,\text{V}$.

Figure 2.12 and 2.13 display GNR conductance G dependence on L_c and W_c for $V_d = 0.2\,\text{V}$, $L = 25$, $W = 18$ or 14 and $V_{back} = 0\,\text{V}$ or $1\,\text{V}$, respectively. One can observe that when $V_{back} = 0\,\text{V}$, W_c and L_c have significant influence on the conductance value, (i.e., G substantially increases with W_c increase, while G increases in a lower ration with L_c increase). When $V_{back} = 1\,\text{V}$, W_c

still has an impact on G but L_c ceases to do so. Thus, the constriction parameter W_c plays a more important role than L_c in GNR conductance modulation. Further, in order to gain more insight into the constriction parameters W_c and L_c influence on current related characteristics, we depict current ratio I_{on}/I_{off} map as a function of L_c and W_c, as illustrated in Figure 2.14. The experimental results show that smaller W_c and L_c are able to obtain a higher I_{on}/I_{off}. Specifically, in our B-GNR case, the highest I_{on}/I_{off} are 1.3×10^4 (at $W_c = 7$ and $L_c = 1$) and 1.7×10^4 (at $W_c = 3$ and $L_c = 1$) for GNR geometries with $W = 18$ and $W = 14$, respectively.

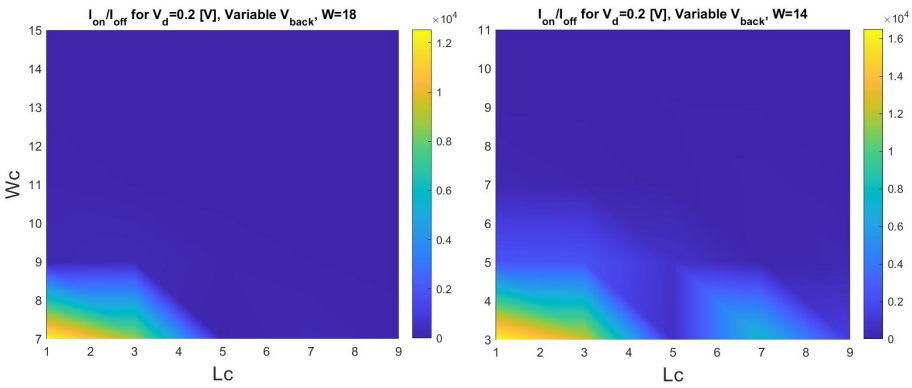

Figure 2.14: I_{on}/I_{off} vs. L_c and W_c for $V_d = 0.2\,\mathrm{V}$, Variable V_{back}.

2.5.3 Conductance vs. Butterfly GNR Constriction Angle

The constriction angle is also influencing B-GNR carrier transport and to study its impact on conductance we assume a B-GNR with $W = 14, L = 35, W_c = 7$ and $L_c = 3$. As the oblique line is actually a staircase following the lattice structure to characterize it we define two variables, step hight SH and step length SL, as depicted in Figure 2.15. Due to lattice structure an oblique line can be realized with more than one stair shape configurations, e.g., for 30°, there are $(SH, SL) = (1, 2)$, $(SH, SL) = (2, 3)$ and $(SH, SL) = (3, 4)$, resulting in different roughness and by implication G and I_{on}/I_{off} values. Moreover the number of realizable angles is also limited, e.g., Table 2.1 summarizes the feasible angles when $SH \in \{1, 2, 3\}$ and $SL \in \{1, ..., 6\}$, in which the $SH = 1$ with two angles (60°and 30°) are written in the pink box, the $SH = 2$ with four angles (60°, 40.9°, 30°and 23.4°) are collected in the green box, and the $SH = 3$ with six angles (60°, 46.1°, 36.6°, 30.0°, 25.3°and 21.8°,) are summarized in the blue box.

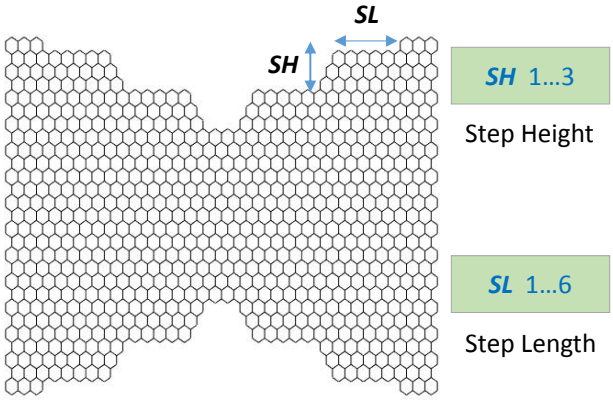

Figure 2.15: B-GNR Oblique Line Realization

Table 2.1: Feasible Constriction Angles.

Angle[°]	SH	SL	Angle[°]	SH	SL
60.0	1	1	60.0	3	1
30.0	1	2	46.1	3	2
60.0	2	1	36.6	3	3
40.9	2	2	30.0	3	4
30.0	2	3	25.3	3	5
23.4	2	4	21.8	3	6

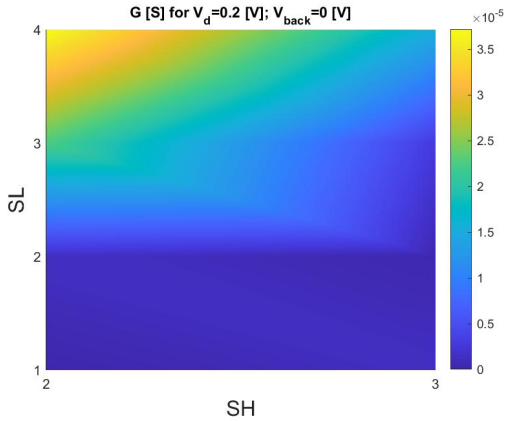

Figure 2.16: G vs. SH and SL for $V_{\mathrm{d}} = 0.2\,\mathrm{V}$, $V_{\mathrm{back}} = 0\,\mathrm{V}$.

Figure 2.16 depicts G map for the considered B-GNRs with different con-

striction configurations ($SH \in \{2,3\}$ and $SL \in \{1,...,4\}$), under the bias ($V_{\text{d}} = 0.2\,\text{V}$, $V_{\text{back}} = 0\,\text{V}$). The figure indicates that when $V_{\text{back}} = 0\,\text{V}$: (i) for fixed SL the conductance decreases (from 36.6% to $5.1\times$) with each SH increase (constriction angle increases) and (ii) for fixed SH the conductance increases (from $2.6\times$ to $10.6\times$) with each SL increase (constriction angle decreases), which implies that the GNR conductance for $V_{\text{back}} = 0\,\text{V}$ substantially increases with angle decrease. On the other hand for $V_{\text{back}} = 1\,\text{V}$, conductance is almost insensitive to SH and SL variations, in which conductance change is 1.2%.

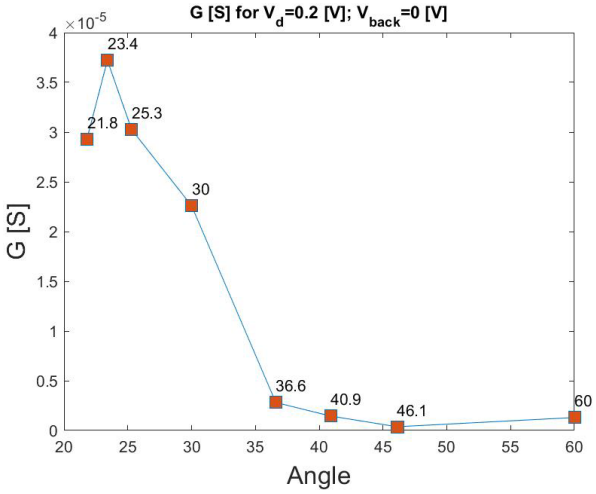

Figure 2.17: G vs. Constriction Angle for $V_{\text{d}} = 0.2\,\text{V}$, $V_{\text{back}} = 0\,\text{V}$.

As shown Figure 2.17, we demonstrate G with different angles from Table 2.1. For the same angle in Table 2.1, we choose one of them as example in our experiment. From the plot in Figure 2.17, one can notice that for $V_{\text{back}} = 0\,\text{V}$, conductance decreases (95.6% in total for all steps) with angle increase. Thus, the constriction angle has a significantly impact on GNR conductance.

Further, we derive current ratio $I_{\text{on}}/I_{\text{off}}$ for B-GNR geometries with different constriction parameters. Figure 2.18 plots $I_{\text{on}}/I_{\text{off}}$ with the constriction angle, in which one can observe that $I_{\text{on}}/I_{\text{off}}$ increases with angle increase (GNR with $60°$ has $92\times$ bigger $I_{\text{on}}/I_{\text{off}}$ than GNR with $21.8°$) and its highest current ratio is 6.4×10^2. Thus, we can conclude that in general the biggest constriction angle ($60°$) is the best angle for getting the highest $I_{\text{on}}/I_{\text{off}}$.

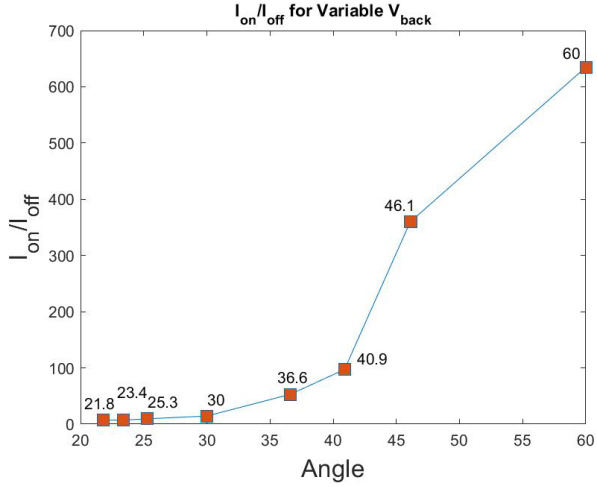

Figure 2.18: $I_{\text{on}}/I_{\text{off}}$ vs. Angle for $V_{\text{d}} = 0.2\,\text{V}$ and Variable V_{back}.

2.5.4 Conductance vs. W_{tb} vs. L_{tb} for Camel GNRs

In this section, we investigate Camel GNR (C-GNR) and its W_{tb} and L_{tb} influence on C-GNR conductance and current characteristics. Specifically, we start from a rectangular GNR with $L = 25$ and $W = 18$ as initial configuration. On the top and bottom edges, a bump is present whose width W_{tb} and length L_{tb}, defined as illustrated in Figure 2.19, are varied as follows: (i) W_{tb} is varied from 2 to 6, and (ii) L_{tb} is varied from 1 to 7. The voltages applied on top of C-GNR are the same with R-GNR in above Section.

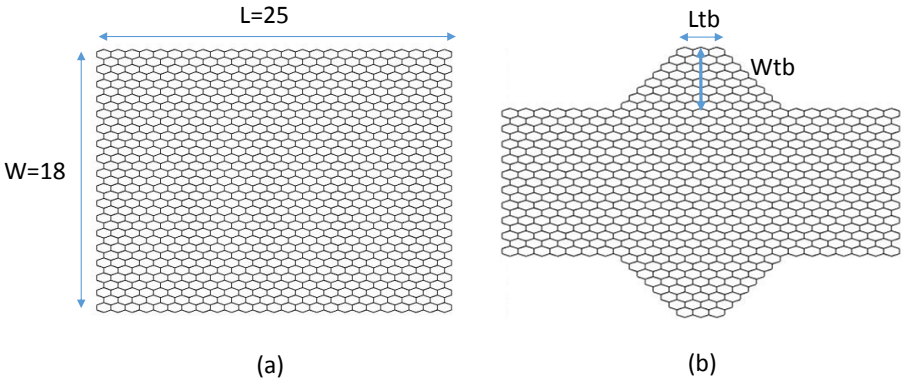

Figure 2.19: Initial Nanoribbon Configuration and Bump Dimensions.

We derive the conductance G map versus the bump width W_{tb} and length L_{tb}, for variable V_{back} from 0 to 0.8, as shown in Figure 2.20. As a general trend, we

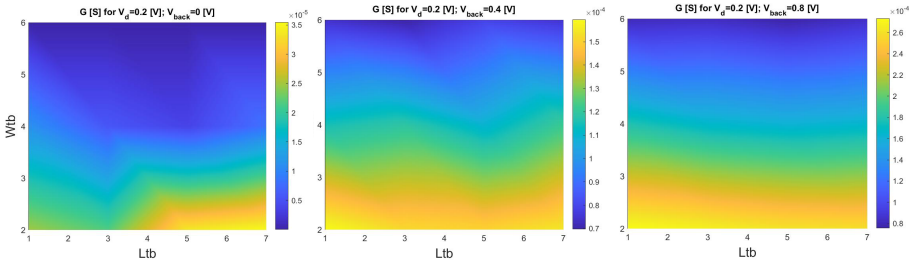

Figure 2.20: G vs. Bump Dimensions for Different V_{back}.

can observe: (i) we identify in Figure 2.20 the bigger L_{tb} and smaller W_{tb} as the bump dimensions which yield the highest GNR G for $V_{\text{back}} = 0\,\text{V}$, while for $V_{\text{back}} = 0.4\,\text{V}$ or $0.8\,\text{V}$ the smaller W_{tb} can obtain the highest GNR G, and (ii) the smaller L_{tb} and bigger W_{tb} can derive the lowest GNR G. Subsequently, we investigate C-GNR geometry influence on current ratio $I_{\text{on}}/I_{\text{off}}$. Figure 2.21 depicts $I_{\text{on}}/I_{\text{off}}$ for $V_{\text{d}} = 0.2\,\text{V}$ and variable V_{back}. One can observe

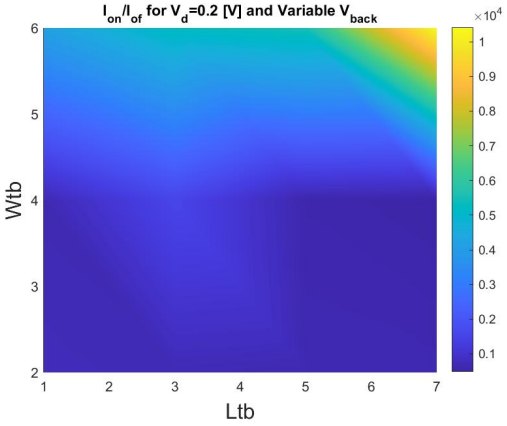

Figure 2.21: $I_{\text{on}}/I_{\text{off}}$ vs. Bump Dimensions for $V_{\text{d}} = 0.2\,\text{V}$.

that $I_{\text{on}}/I_{\text{off}}$ increases with W_{tb} and L_{tb} increase, and its maximum achievable current ratio is 1.0×10^4 (at $W_{\text{tb}} = 6$ and $L_{\text{tb}} = 7$) which implys the bump width and length have a big impact on the GNR conductance and the current-related characteristics (e.g., $I_{\text{on}}/I_{\text{off}}$).

2.5.5 Conductance vs. W_b vs. L_b for Double Butterfly GNRs

In this section, we focus on the carrier transport properties of Double Butterfly GNR (DB-GNR), which exhibits a bump on the narrow constriction on Butterfly GNR (B-GNR). As illustrated in Figure 2.22, we consider the dimensions of 2 initial B-GNR structures: (a) B-GNR with width $W = 14$, length $L = 25$, narrow constriction width $W_c = 5$ and constriction length $L_c = 7$, and (b) GNR with $W = 18$, $L = 25$, $W_c = 9$ and $L_c = 7$. Specifically, for each of

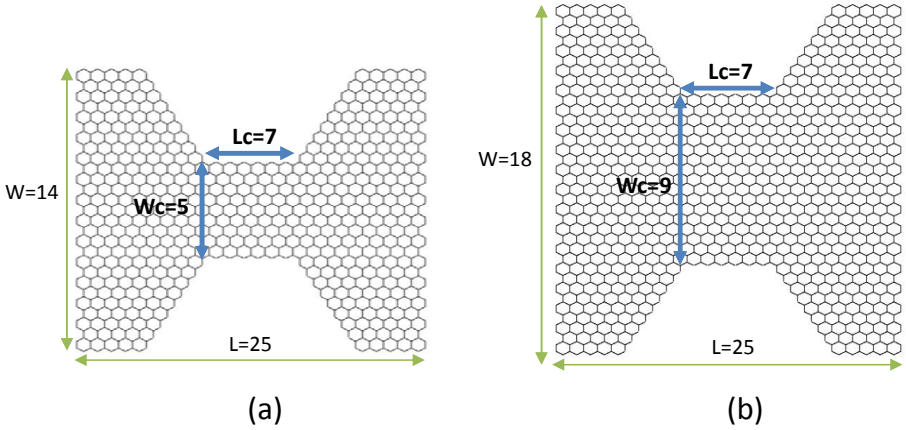

Figure 2.22: Initial Butterfly GNR Configurations.

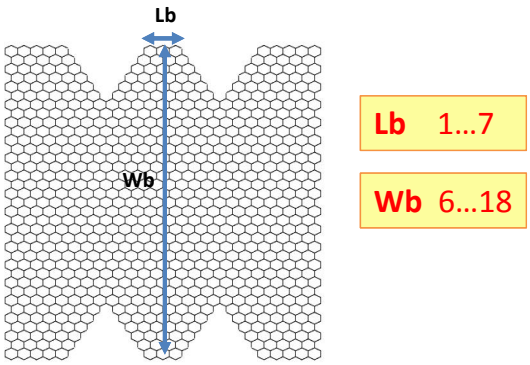

Figure 2.23: DB-GNR Dimensions.

the 2 initial B-GNR configurations, we define the bump length (L_b) and bump width (W_b) as shown in Figure 2.23 and vary them as follows: (i) L_b from 1 which corresponds to a triangular bump to 7 which is related to a trapezoidal

bump, and (ii) W_b from 6 to 18. The voltages we apply on top of the nanoribbon are: $V_d = 0.2\,V$, $V_s = 0\,V$ and the top gate voltage $V_g = 0\,V$. A global back bias voltage V_{back} varying from 0 V to 1 V (in increments of 0.2 V) is also applied.

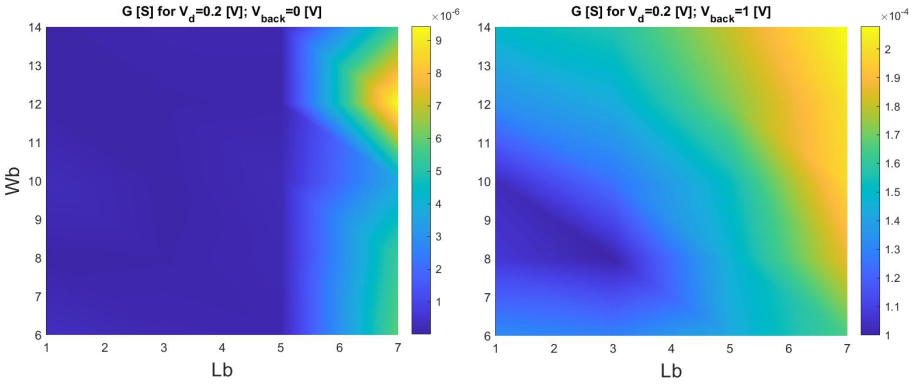

Figure 2.24: G vs. W_b vs. L_b for $W = 14$, $V_d = 0.2\,V$ and $V_{back} = 0\,V$ or $1\,V$.

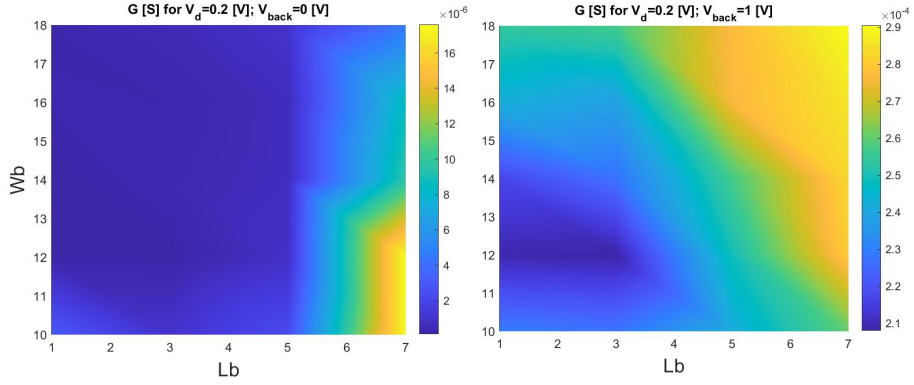

Figure 2.25: G vs. W_b vs. L_b for $W = 18$, $V_d = 0.2\,V$ and $V_{back} = 0\,V$ or $1\,V$.

Subsequently we investigate the influence of W_b and L_b on the conductance G. In Figure 2.24, 2.25 we show the bump dimensions influence on G (at $V_d = 0.2\,V$, $V_{back} = 0\,V$ or $1\,V$) for the 2 GNR configurations, respectively. As a general trend, for a fixed bump width W_b the GNR conductance increases with L_b increase ($1510\times$ increase for GNR with dimension $W = 14$, and $1508\times$ increase for GNR with $W = 18$), while for a fixed L_b (from 1 to 5) the conductance remains almost a constant value with W_b increase. Particularly, for a fixed L_b (from 5 to 7), the GNR G increases with W_b increase (26%

increase for dimension $W = 14$ and 15% increase for $W = 18$). Thus, we can identify the region $L_{\mathrm{b}} \in [1, 5]$ and $W_{\mathrm{b}} \in [6, 12]$ as the bump dimensions which provides a low value of G, while the region $L_{\mathrm{b}} \in [5, 7]$ and $W_{\mathrm{b}} \in [14, 18]$ which exhibits a high G. Further, we explore bump structures influence

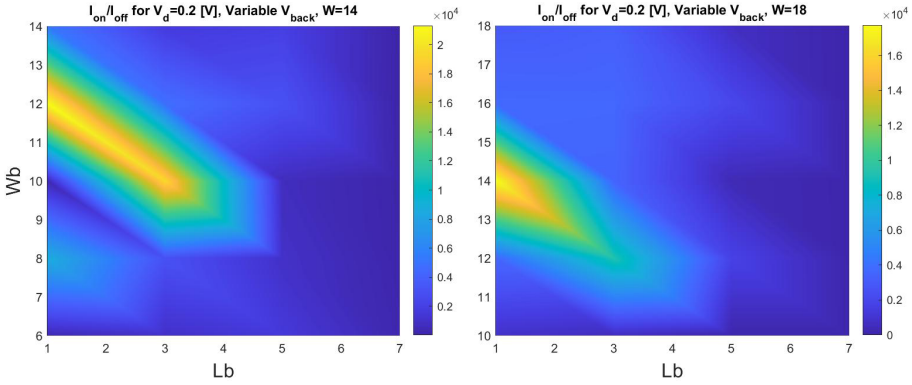

Figure 2.26: $I_{\mathrm{on}}/I_{\mathrm{off}}$ vs. W_{b} vs. L_{b} for $V_{\mathrm{d}} = 0.2\,\mathrm{V}$ and Variable V_{back}.

on current ratios $I_{\mathrm{on}}/I_{\mathrm{off}}$. Figure 2.26 shows bump parameters (W_{b} and L_{b}) influence on $I_{\mathrm{on}}/I_{\mathrm{off}}$, in which the highest $I_{\mathrm{on}}/I_{\mathrm{off}}$ are 2.1×10^4 (at $W_{\mathrm{b}} = 12$ and $L_{\mathrm{b}} = 1$) and 1.8×10^4 (at $W_{\mathrm{b}} = 14$ and $L_{\mathrm{b}} = 1$) for variable V_{back} and for dimension $W = 14$ and $W = 18$, respectively. Therefore, the bump structure plays a significate role in GNR electron transport and is helpful to improve the current related characteristics (e.g., $I_{\mathrm{on}}/I_{\mathrm{off}}$) for DB-GNRs.

2.5.6 Ability to Control GNR Conduction Using Gate Bias

In this section, we investigate the ability of gate bias (e.g., top gate and back gate) to control GNR conduction.

Back Gate Control Ability

On the back of the graphene we apply a back-gate-bias V_{back}, which in manufactured devices is typically a small fraction of the back gate potential (because of a significant potential drop on the dielectric layer - usually SiO_2 - residing underneath the graphene ribbon). Normally, the back-gate-bias V_{back} modulates the electrostatic tunability of the Fermi level for the energy at the Dirac point and the back-gate controlled GNRs can enable a much higher $I_{\mathrm{on}}/I_{\mathrm{off}}$

(e.g., $10\times$ bigger when compared to the top-gate controlled GNRs in our experiments).

Top Gate Control Ability

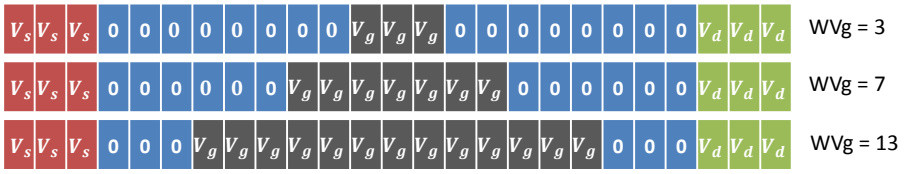

Figure 2.27: Examples of Top Gate Contact Width.

For top gate contact control ability, we consider GNR with a single top gate V_{g} with varying contact width and investigate its contact width influence on the GNR conductance and current characteristics. In particular, we consider 4 GNR configurations: (i) B-GNR ($W = 14, L = 25, W_{\mathrm{c}} = 3, L_{\mathrm{c}} = 1$), (ii) DB-GNR ($W = 14, L = 25, W_{\mathrm{c}} = 5, L_{\mathrm{c}} = 7, W_{\mathrm{b}} = 12, L_{\mathrm{b}} = 1$), (iii) C-GNR ($W = 14, L = 25, W_{\mathrm{tb}} = 6, L_{\mathrm{tb}} = 7$), and (iv) W-GNR ($W = 18, L = 25, W_{\mathrm{h}} = 1, W_{\mathrm{wc}} = 4, L_{\mathrm{h1}} = 6, L_{\mathrm{h2}} = 3$). We selected these GNR configurations for B-GNR, DB-GNR and C-GNR, as they render the best conductance G and $I_{\mathrm{on}}/I_{\mathrm{off}}$ among the analyzed GNR shapes presented in above Section. The voltages applied on top of GNR are as follows: $V_{\mathrm{s}} = 0\,\mathrm{V}$, $V_{\mathrm{d}} = 0.2\,\mathrm{V}$ and V_{g} varied from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$. Beneath the back of GNR, we apply V_{back} varied from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$. We denote by WV_{g} the top gate contact width and vary it from 1 to 19 in increments of 2, as illustrated in Figure 2.27.

In order to explore the V_{g} influence on the GNR conductance, we present the conductance maps w.r.t. V_{g} and V_{back} for the B-GNR case with $WV_{\mathrm{g}} = 7$ and 13 as an example, as shown in Figure 2.28. We observe a similar G vs. V_{g} vs. V_{back} behavior for the DB-GNR, C-GNR and W-GNR cases. As a general trend, for a fixed V_{g} the conductance significantly changes (up to 1.57×10^4 for $WV_{\mathrm{g}} = 7$ and 1.63×10^4 for $WV_{\mathrm{g}} = 13$) with V_{back} variation, while for a fixed V_{back} the conductance varies (up to 3.99×10^3 for $WV_{\mathrm{g}} = 7$ and 4.01×10^3 for $WV_{\mathrm{g}} = 13$) with V_{g} variation. Thus, the V_{back} ability to control the GNR conductance is much stronger (1 order of magnitude) than V_{g}. One possible reason for this situation is that V_{back} is connected to all carbon atoms in GNR sheet, while V_{g} covers less carbon atoms such that V_{g} has less impact on the GNR electron transport than V_{back}.

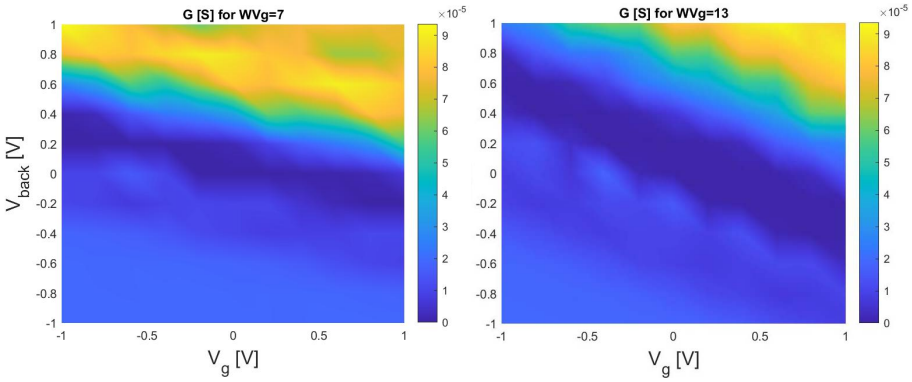

Figure 2.28: Conductance vs. Top Gate and Back Gate Voltages for B-GNR with $WV_g = 7$ and 13.

Further, we investigate the gate contact width WV_g influence on the current characteristics. Figure 2.29 shows I_{on}/I_{off} variation w.r.t. the top gate width WV_g for B-GNR, DB-GNR, C-GNR and W-GNR. One can observe that for the B-GNR case, normally, I_{on}/I_{off} increases with WV_g increase until $WV_g = 15$ in which B-GNR provides a highest $I_{on}/I_{off} = 2.1 \times 10^4$, while for DB-GNR, C-GNR and W-GNR case, as a general trend, the conductance decreases with WV_g increase. In particular, for these 4 cases, the current ratios change in different way, which suggests that GNR current characteristic is rather GNR geometry dependent. In addition, the I_{on}/I_{off} variations with WV_g change are 27.8%, 13.0%, 39.5% and $3\times$ for B-GNR, DB-GNR, C-GNR and W-GNR, respectively, which implys WV_g has a remarkable impact on GNR I_{on}/I_{off} (especially for W-GNR).

Table 2.2: Top Gate Voltage Contact Dimensions for the Best Current Characteristics at $V_d = 0.2\,\mathrm{V}$.

	I_{on}/I_{off}	I_{on}	I_{off}	WV_g
B-GNR	2.1×10^4	9.1×10^{-5}	4.3×10^{-9}	15
DB-GNR	2.4×10^4	1.5×10^{-4}	6.1×10^{-9}	1
C-GNR	1.5×10^4	1.0×10^{-4}	6.9×10^{-9}	3
W-GNR	2.3×10^7	2.7×10^{-5}	1.2×10^{-12}	1

Furthermore, as shown in Table 2.2 we summarise the highest I_{on}/I_{off}, their corresponding ON-state current I_{off}, OFF-state current I_{on} and WV_g configurations for these 4 GNR shapes. The B-GNR exhibits $I_{on}/I_{off} = 2.1 \times 10^4$ for $WV_g = 15$ and the DB-GNR has an I_{on}/I_{off} of 2.4×10^4 for $WV_g = 1$.

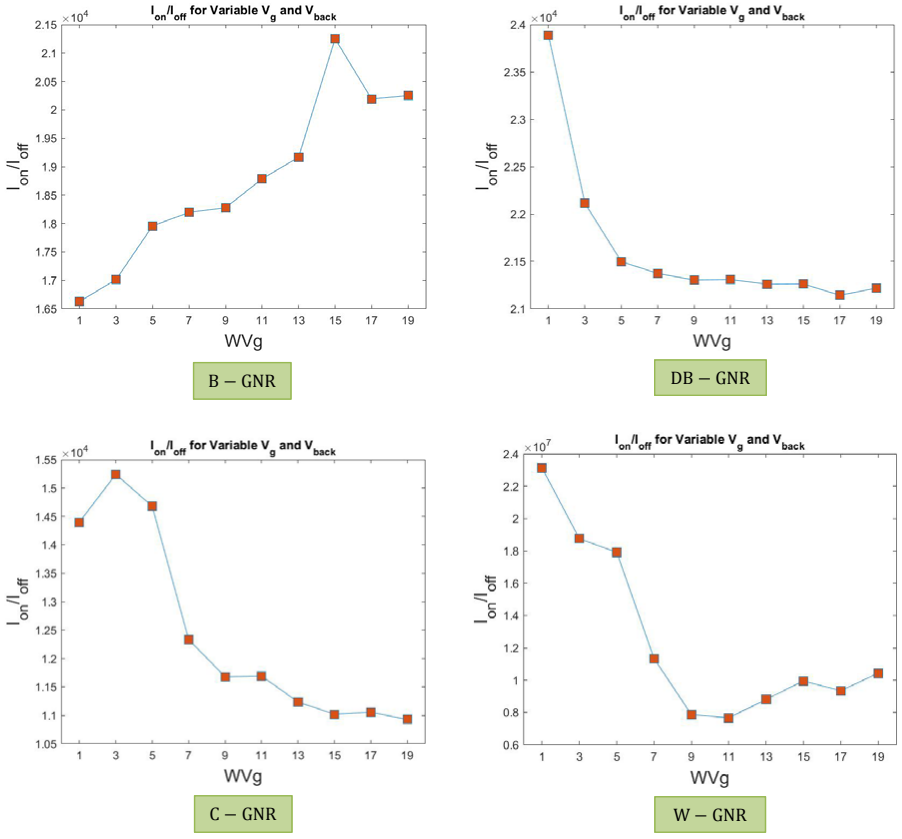

Figure 2.29: $I_{\text{on}}/I_{\text{off}}$ vs. Top Gate Contact Width WV_{g}.

The C-GNR obtains an $I_{\text{on}}/I_{\text{off}}$ of 1.5×10^4 for $WV_{\text{g}} = 3$, while the W-GNR provides the biggest $I_{\text{on}}/I_{\text{off}} = 2.3 \times 10^7$ for $WV_{\text{g}} = 1$ among 4 GNR shapes, because W-GNR's special geometry makes it obtain a very low OFF-stage current (e.g., 1.2×10^{-12}A).

As a result, the top and back gate voltagse have a big impact on the GNR conductance and $I_{\text{on}}/I_{\text{off}}$. The experiment result suggests that the top/back gate contacts are good methods to control the GNR-based device conduction (e.g., gate contact improves $I_{\text{on}}/I_{\text{off}}$ up to 2.3×10^7 for W-GNR and 2.1×10^4 for B-GNR).

2.6 Conclusion

In this chapter, we explored and investigated five different GNR shapes (R-GNR, B-GNR, DB-GNR, C-GNR, W-GNR) influence on the conductance and current characteristics. To this end, we built upon a GNR-based building block by extending it with a additional top gate and a back gate. In particular, we explored the ability to open the GNR energy bandgap through GNR geometry change or via applied top/back gate voltages. Further, we investigated the GNR geometry influence on its G and $I_{\text{on}}/I_{\text{off}}$ by varying GNR geometries W, L, W_{c}, L_{c}, W_{b}, L_{b}, W_{tb} and L_{tb}. The experimental result suggests that W has a remarkable impact on G, while G is practically independent on L. For B-GNR case, the configuration with small W_{c} and L_{c} is more helpful to obtain a higher $I_{\text{on}}/I_{\text{off}}$. In addition, for the angle between constriction channel and Drain/Source contact for B-GNR, the experiment suggests that the bigger angle can achieve better $I_{\text{on}}/I_{\text{off}}$. Furthermore, for DB-GNR and C-GNR case, bump structure (W_{b} and L_{b}) can help improve the current related characteristics. Last, we explored the ability of gate bias (e.g., top gate and back gate) to control GNR conduction. The result suggests that V_{back} voltage modulates the Fermi level for the energy at the Dirac point, thus the back-gated GNRs can enable a much higher $I_{\text{on}}/I_{\text{off}}$. The top gate voltage has also a remarkable impact on the $I_{\text{on}}/I_{\text{off}}$. Our experiment suggests that the top/back gate contacts are good external methods for controlling the GNR-based device conduction (e.g., gate contact improves the $I_{\text{on}}/I_{\text{off}}$ up to 2.3×10^7 for W-GNR and 2.1×10^4 for B-GNR), establishing GNR's potential as basic building block for future carbon-based logic circuits.

3

Graphene Nanoribbon Conductance Modulation

In this chapter we augment a trapezoidal Quantum Point Contact (QPC) topology with top gates to form a butterfly Graphene Nanoribbon (GNR) structure and demonstrate that, by adjusting its topology, its conductance map can mirror basic Boolean functions, thus one can use such structures instead of transistors to build carbon-based gates and circuits. We first identify by means of Design Space Exploration (DSE) specific GNR topologies for 2- and 3-input $\{\text{AND}, \text{NAND}, \text{OR}, \text{NOR}, \text{XOR}, \text{XNOR}\}$ and demonstrate by means of Non-Equilibrium Green Function - Landauer based simulations that butterfly GNR-based structures operating at $V_{DD} = 0.2\,\text{V}$ outperform $7\,\text{nm}$ @$V_{DD} = 0.7\,\text{V}$ CMOS counterparts by 2 to 3, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively, while requiring 2 orders of magnitude less active area. Subsequently, we investigate the effect of V_{DD} variations and the V_{DD} value lower bound. We demonstrate that NOR butterfly GNR structures are quite robust as their conductance and delay are changing by no more than 2% and 6%, respectively, and that AND and NOR GNR geometries can operate even at $10\,\text{mV}$. Finally, we consider aspects related to the practical realization of the proposed structures and conclude that even if there are still hurdles on the road ahead the latest graphene fabrication technology developments, e.g., surface-assisted synthesis, our proposal opens an alternative towards effective carbon-based nanoelectronic circuits and applications.

3.1 Introduction

Generally speaking, the main impediments to graphene-based Boolean logic can be divided into design and manufacturing related [20], [21], [111], [112], [113]. From the manufacturing point of view, finding a cost-effective, scalable and reliable manufacturing process, which enables mass-production with minimum defects density and highly reproducible features, is the main desideratum. From the design perspective, several aspects have to be considered: (i) ability to control conductivity and yield distinguishable "on" and "off" states, while (a) not compromising any of the graphene intrinsic highly advantageous properties (e.g., high carrier mobility), and (b) providing an $I_{\text{ON}}/I_{\text{OFF}}$ ratio in the order of 10^6 to 10^7 (i.e., the typical ratio for low power $<20\,\text{nm}$ Si logic process), (ii) encoding the desired Boolean logic transfer function into the graphene electrical characteristics (e.g., conduction maps), (iii) finding proper external electric means (e.g., top gates, back gates) to control the graphene behavior and induce the desired logic functionality, and (iv) ensuring the conditions for cascading digital circuits (i.e., clean and compatible/matching electric levels, e.g., voltage, current, for the gates inputs and outputs).

In this chapter, we address (ii) and (iii) related issues and demonstrate that by augmenting the trapezoidal Quantum Point Contact (QPC) topology in [114] with top gates to form a butterfly GNR we can modulate its conductance by means of external voltages, such that it mirrors the behavior of basic Boolean functions. In particular, we consider the basic set of Boolean functions $\{\text{AND}, \text{NAND}, \text{OR}, \text{NOR}, \text{XOR}, \text{XNOR}\}$ and perform a Design Space Exploration (DSE) with regard to GNR topology and dimensions, such that for each function we identify a GNR structure able to provide the conductance map (conductance G vs. top gate voltages) reflecting its truth table (high G for logic $''1''$, low G for logic $''0''$). For modelling GNRs' electronic transport properties we employ the NEGF-Landauer formalism [114], [110].

Our simulations indicate that the obtained 2-input butterfly GNR-based structures operating at $V_{DD} = 0.2\,\text{V}$ outperform $7\,\text{nm}$ $@V_{DD} = 0.7\,\text{V}$ CMOS counterparts by 2, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively, while requiring 2 orders of magnitude less active area. For 3-input function the butterfly GNR based approach proved to be even more effective, i.e., 2 to 3, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively. Moreover our approach is less sensitive to gate fan-in scaling as when incrementing it from 2 to 3 CMOS area footprint (delay) increases by up to 100% (51%) while for the GNR structures area (delay)

changes are up to 26% (42%). We also compared with state of the art graphene based 2-input gates and obtained: (i) 1 order of magnitude smaller delay for all 2-input structures, when compared to [115], and (ii) 3, 1, 1, and 2 orders of magnitude smaller area, delay, power consumption, and power-delay product, respectively, when compared to the NAND in [116].

We subsequently concentrate on the effect of V_{DD} variations and on determining V_{DD} lower bound value. To this end we simulate NOR butterfly GNR structures while changing V_{DD} with $\pm 10\%$ in increments of 2% with respect to the nominal voltage $V_{DD} = 0.2\,\mathrm{V}$. These experiments reveal that GNR conductance and delay are changing by no more than 2% and 6%, respectively. Concerning V_{DD} lower bound we present AND and NOR GNR geometry able to operate even at $10\,\mathrm{mV}$ and demonstrate that it is rather GNR geometry and contact topology dependent, $20\,\mathrm{mV}$ for the considered structures.

Finally, we discuss GNR fabrication status, difficulties and challenges, and explore edge defects influence on butterfly GNR conductance. Our results indicate that GNR's conductance variation is rather substantial, even due to one missing atom in the constriction edge, conductance ratio is decreasing but is also experiencing substantial increase, which is quite interesting as it suggests that defects might be helpful rather than harmful, and despite the performance degradation the GNR can still deliver the expected Boolean functionality. This together with the fact that surface-assisted synthesis approach was utilized to fabricate atomically precise, low-edge-defect GNRs, e.g., 3-Armchair GNRs (1 hexagon width) and 6-Zigzag GNRs (6 hexagon width) [76], indicates that our proposal opens an alternative towards effective carbon-based nanoelectronic circuits and applications.

The remaining of this chapter is structured as follows: Section 3.2 presents an overview of the utilized simulation framework. Section 3.3 entails DSE results in terms of GNR topologies and their afferent conductance maps mirroring the basic set of 2- and 3-input Boolean functions. Section 3.4 presents simulation results (i.e., area, delay, robustness to V_{DD} variation, V_{DD} lower bound), comments on the potential of GNR-based Boolean logic design, discusses GNR fabrication status, difficulties and challenges, and analysis of the potential impact of GNR edge defects. Finally, concluding remarks are given in Section 3.5.

3.2 Simulation Framework

In this chapter, we explore the potential of using GNRs as basic building blocks (other than transistors) for future GNR-based logic gates and mainly deal with the following problem: Given an initial GNR shape and a basic Boolean function, determine the GNR topology, geometry, and means to modulate its conductance (via, e.g., external gate voltages), such that it mirrors the desired logic functionality while providing good conduction properties, e.g., I_{ON}/I_{OFF} ratio. In relation with this, we subsequently describe: (i) the underlying GNR-based structure, (ii) the utilised simulation model, which is able to capture graphene electronic ballistic transport properties, and (iii) the design space exploration methodology we employ in order to identify a GNR geometry, which conductance best reflects a given Boolean function.

As GNR research vehicle, we build upon the trapezoidal Quantum Point Contact with zig-zag edge alignment, described in [114]. We characterise its geometry and topology as graphically defined in Figure 3.1 and further denote it as butterfly GNR. we make use of the 3D GNR-based structure (GNR building

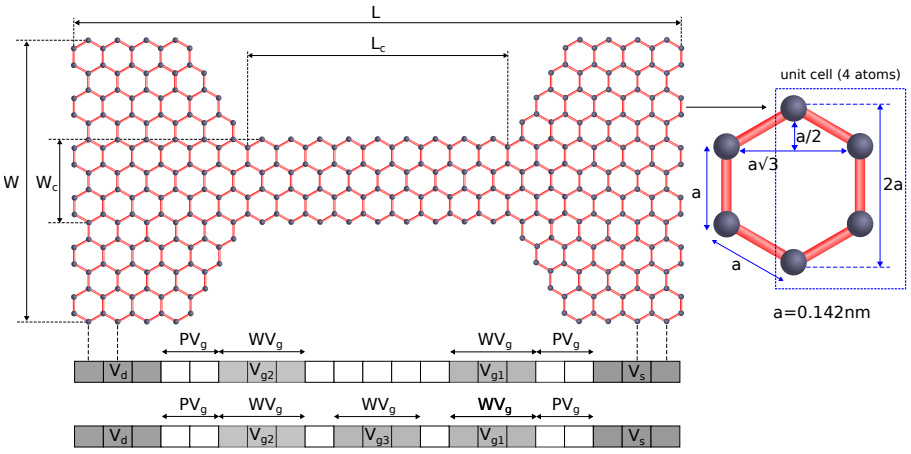

Figure 3.1: Butterfly Graphene Nanoribbon (GNR)

block) as illustrated in Figure 2.5 in Chapter 2, in which we employ a butterfly GNR as a conduction channel, through which the current flow (i) is induced via a bias voltage (i.e., $V_d - V_s$) applied between the drain and source contacts of the graphene sheet, (ii) is modulated by input voltages (i.e., V_{g1} and V_{g2}), which are applied via the two (in this case) top gates, and (iii) is biased by V_{back} applied beneath the GNR.

Based on this GNR structure, we vary the nanoribbon geometry and the gate contacts topology, until a conduction map reflecting the desired Boolean functionality, is obtained. We initially consider the set of 2-input Boolean functions $\{\text{AND}, \text{NAND}, \text{OR}, \text{NOR}, \text{XOR}, \text{XNOR}\}$, and apply voltage levels via the two top gates, as illustrated in Figure 2.5. We convene to use $0\,\text{V}$ and $1\,\text{V}$ as the voltage levels afferent to logic $''0''$ and logic $''1''$. We note that this choice is solely for explanatory purpose and is not restrictive in any way; one can also choose other voltage levels (e.g., $10\times$ smaller), and for a certain Pareto butterfly GNR geometry, obtain a conduction map that complies with the desired Boolean logic. We set the left contact (drain) and the right contact (source) voltage to $0.2\,\text{V}$ and $0\,\text{V}$, respectively. For each Boolean logic function, we perform a Design Space Exploration (DSE) by varying the following: (i) the butterfly GNR dimensions defined in terms of the distance between adjacent carbon atoms, a ($1.42\,\text{Å}$), as depicted in Figure 3.1 (i.e., the nanoribbon total width, W, and length, L, from $41\,\text{a}$ to $47\,\text{a}$ and from $25\sqrt{3}$ a to $27\sqrt{3}$ a, respectively; and the constriction width, W_c and length, L_c, from $2\,\text{a}$ to $35\,\text{a}$ and from $3\sqrt{3}$ a to $12\sqrt{3}$ a, respectively), (ii) the top gate contacts topology (i.e., the distance between the two top gate contacts and the source/drain contacts, P_Vg, from $2\sqrt{3}$ a to $6\sqrt{3}$ a, and the contact width, W_Vg from $3\sqrt{3}$ a to $7\sqrt{3}$ a), and (iii) V_back from $-1\,\text{V}$ to $1\,\text{V}$ (in increments of $0.2\,\text{V}$).

For each design point, we derive the conductance map with respect to the 2-input top gate voltages. To this end, we make use of previously mentioned GNR modelling and simulation methodology in Section 2.2. More precisely, for modelling the electronic ballistic transport in GNRs, we employ the Non-Equilibrium Green Function (NEGF) quantum transport model, the semi-empirical Tight Binding (TB) computations to obtain the system Hamiltonian, and the Landauer formalism to derive GNR's current and conductance [114], [110], [117].

The convergence criteria that we employed for the Pareto conduction maps are threefold: (i) for each $(V_\text{g1}, V_\text{g2})$ pair of inputs ($(0,0)$, $(0,1)$, $(1,0)$ and $(1,1)$), the conductance magnitude should mirror the desired Boolean output logical value, (ii) the standard deviation of all conductance values corresponding to logic $''0''$ (logic $''1''$) should be smaller than a certain imposed percentage, e.g., 10%, and (iii) given that no optimization with respect to the I_ON/I_OFF ratio is targeted, the worst ratio between the logic $''1''$ and logic $''0''$ conductance should be ≥ 10. Note that for 3-input Boolean functions the same DSE methodology applies.

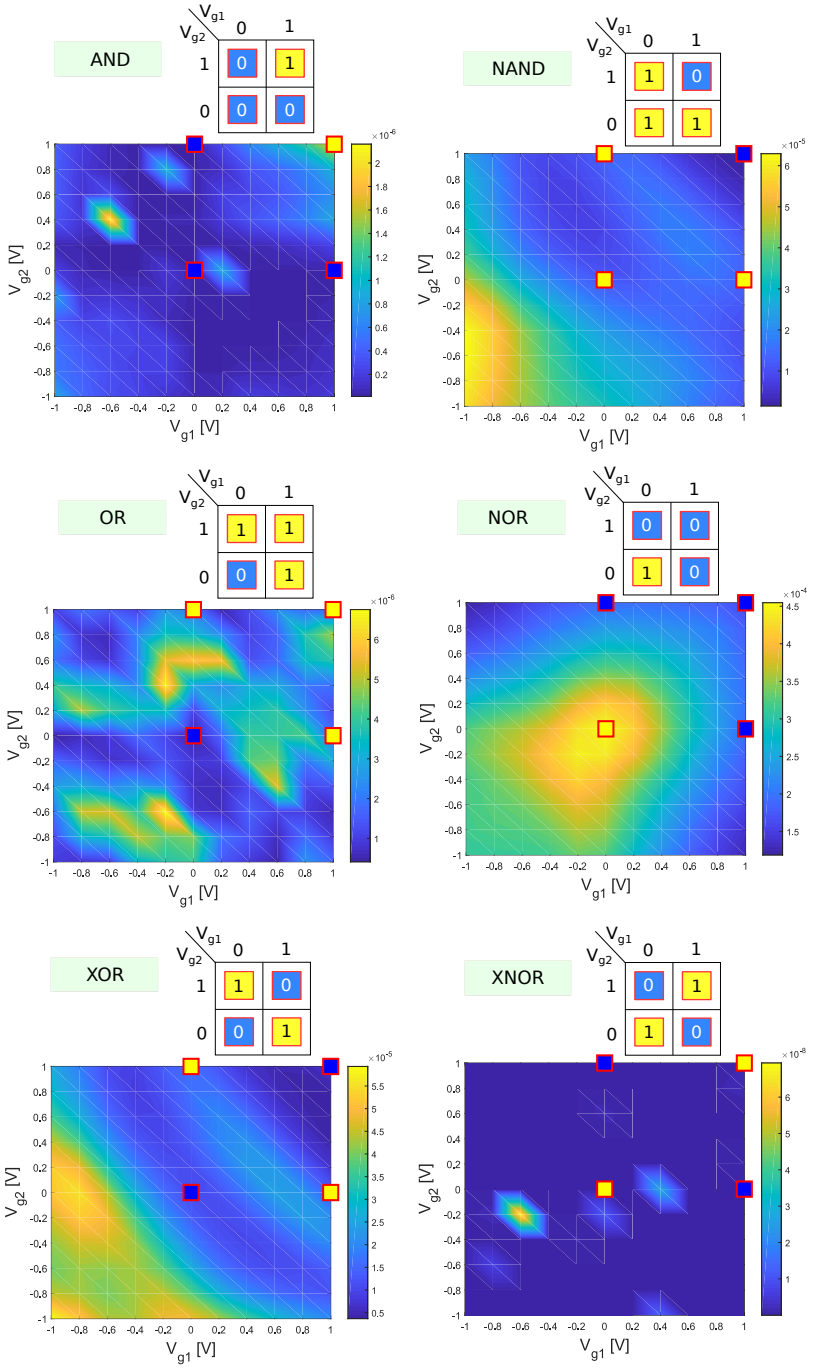

Figure 3.2: 2-input Boolean Functions Conduction Maps.

Table 3.1: 2-input Butterfly GNR Topologies.

		AND	NAND	OR	NOR	XOR	XNOR
W	[a]	41	41	41	41	41	41
L	[a]	$25\sqrt{3}$	$27\sqrt{3}$	$27\sqrt{3}$	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$
W_{c}	[a]	8	8	14	20	8	14
L_{c}	[a]	$5\sqrt{3}$	$5\sqrt{3}$	$11\sqrt{3}$	$9\sqrt{3}$	$5\sqrt{3}$	$10\sqrt{3}$
$P_{V_{\mathrm{g}}}$	[a]	$2\sqrt{3}$	$6\sqrt{3}$	$4\sqrt{3}$	$6\sqrt{3}$	$6\sqrt{3}$	$3\sqrt{3}$
$W_{V_{\mathrm{g}}}$	[a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back}	$[V]$	0	0.4	0	0.4	0.4	0.2

3.3 GNR Conduction Carving

This section present DSE results for 2- and 3-input $\{\mathrm{AND}, \mathrm{NAND}, \mathrm{OR}, \mathrm{NOR}, \mathrm{XOR}, \mathrm{XNOR}\}$ Boolean functions and some comments on the potential applicability of our results for graphene-based Boolean logic gate implementations.

3.3.1 2-input Boolean Functions

Table 3.1 summarizes the optimal butterfly GNR dimensions and back bias voltages, which resulted from the DSE, afferent to each considered 2-input Boolean logic function. All 6 butterfly GNR shapes have the same total width and similar length, but different constriction width and length. The constriction width has a bigger impact on conductance (when compared to the constriction length influence), and thus, its value significantly varies between GNRs corresponding to different Boolean functions. One can also observe in the Table that the distance between the top gate contacts and the source/drain contacts is larger for $\{\mathrm{NAND}, \mathrm{NOR}, \mathrm{XOR}\}$ and smaller for $\{\mathrm{AND}, \mathrm{OR}, \mathrm{XNOR}\}$, while the contact width remains the same for all 6 Boolean functions. As for the V_{back} value, $0\,\mathrm{V}$ or a low value ($\leq 0.4\,\mathrm{V}$) is enough to enable the most appropriate top gate control on the conductance. The conduction density maps (conductance G vs. input voltages V_{g1}, and V_{g2} between $-1\,\mathrm{V}$ and $1\,\mathrm{V}$) exhibited by the 6 butterfly GNR structures described in Table 3.1 are presented in Figure 3.2. The 4 red outlined squares emphasized in each density plot are denoting the high or low GNR conductance values corresponding to the 4 possible input voltages $(V_{\mathrm{g1}}, V_{\mathrm{g2}})$ combinations $(0,0)$, $(0,1)$, $(1,0)$, and $(1,1)$. As color convention we utilize yellow for logic $''1''$ conductance (high con-

ductance) and blue for logic $''0''$ conductance (low conductance). For each density plot, the corresponding Karnaugh map mirrored in the conductance magnitude is also displayed. Let us consider for instance the 2-input XNOR GNR structure. The two yellow points correspond to high conductance values (9.23×10^{-10} S and 1.03×10^{-9} S), while the two blue points correspond to low conductance values (1.90×10^{-11} S and 1.78×10^{-11} S). We note that the blue and yellow colors that we utilised for the 4 conductance square points have no significance in relation with the density map color legend, they just denote a low and a high point conductance, respectively. The best and worst high/low conductance ratios for XNOR are 58 and 49, respectively, and logic $''1''$ ($''0''$) conductance values dispersion is 6% (under 10% for all the mapped functions), which enables robust operation.

3.3.2 3-input Boolean Functions

To explore butterfly GNR structure scalability with respect to the number of inputs, we added a third top gate (equidistant top gates) to enable the possibility to mirror 3-input Boolean gate functionality. The 3-input butterfly GNR structures are similar with the 2-input counterparts geometry-wise, as summarized in Table 3.2, which demonstrates its capability to accommodate multiple top gate inputs.

The obtained conductance maps (conductance G vs. input voltages V_{g1}, V_{g2} and V_{g3} between -1 V and 1 V) corresponding to the 6 butterfly GNR structures described in Table 3.2, are depiced in Figure 3.3 in a double layered manner. The top layer corresponds to $V_{g3} = 1$ V, and all possible combinations of the other two inputs (V_{g1}, V_{g2}), while the bottom layer corresponds to $V_{g3} = 0$ V. The 8 red outlined squares on the two conductance density plot layers reflect the Boolean output logic value ($''0''$ or $''1''$) corresponding to the 8 possible input combinations: $(0,0,0)$, $(0,0,1)$, $(0,1,0)$, $(0,1,1)$, $(1,0,0)$, $(1,0,1)$, $(1,1,0)$, $(1,1,1)$. One can observe that the conductance values are in good agreement with $\{\text{AND}, \text{NAND}, \text{OR}, \text{NOR}, \text{XOR}, \text{XNOR}\}$ true tables, which proves the ability of the butterfly GNR (or GNR in general for that matter) to reflect more complex Boolean functions.

3.3.3 Discussion

Some remarks are at hand in relation with the structures introduced above.

While we demonstrated that one single GNR can deliver a Boolean gate be-

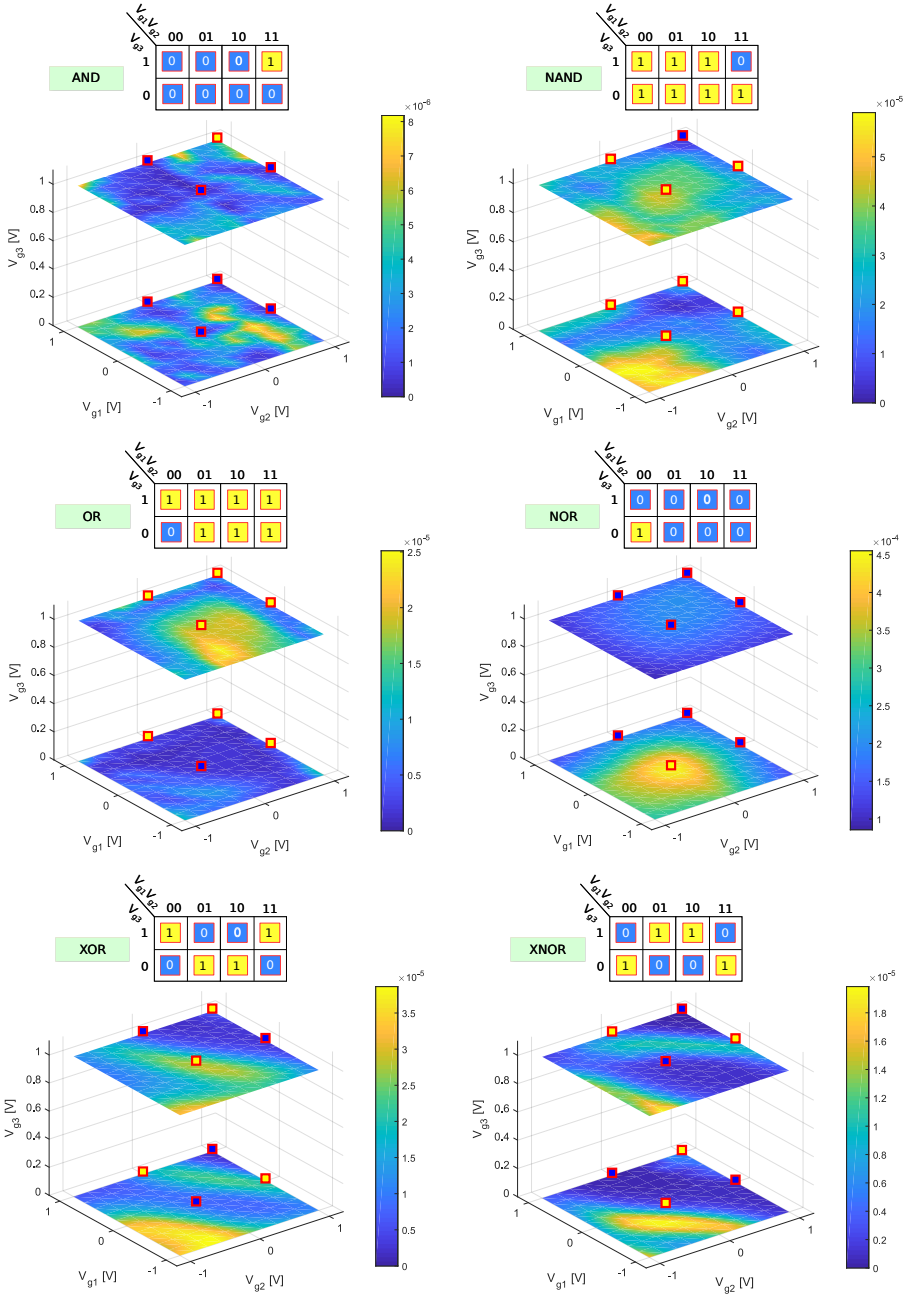

Figure 3.3: 3-input Boolean Functions Conduction Maps.

Table 3.2: 3-input Butterfly GNR Topologies.

		AND	NAND	OR	NOR	XOR	XNOR
W	[a]	47	47	41	41	41	41
L	[a]	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$	$29\sqrt{3}$	$29\sqrt{3}$	$29\sqrt{3}$
W_{c}	[a]	17	17	8	20	2	2
L_{c}	[a]	$5\sqrt{3}$	$5\sqrt{3}$	$5\sqrt{3}$	$13\sqrt{3}$	$7\sqrt{3}$	$7\sqrt{3}$
$P_{V_{\mathrm{g}}}$	[a]	$5\sqrt{3}$	$6\sqrt{3}$	$5\sqrt{3}$	$4\sqrt{3}$	$5\sqrt{3}$	$5\sqrt{3}$
$W_{V_{\mathrm{g}}}$	[a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back}	$[V]$	0	0.2	0.2	1	0.8	0.6

haviour the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio it is rather low (e.g., 38 for the AND function, 49 for the XNOR function for 2-input butterfly GNR structures). However, this can be enhanced by doping [80], or by using per se sawtooth shaped gate contacts instead of rectangular shaped ones [118], or by any other band gap engineering method reported in the literature. Improving $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is future work part of the actual gate design and is beyond the scope of this chapter. The GNR shape determines the carrier confinement properties, and as a consequence, in our case, it can open an energy bandgap of, e.g., up to $0.65\,\mathrm{eV}$ for the butterfly GNR which mirrors the XNOR function. A bandgap of this magnitude was deemed sufficient to effectively switch off a manufactured graphene based device [62].

One can also rely on a butterfly GNR topology, which makes use of one top gate and one back gate in order to apply two Boolean inputs. In this case, V_{back} modulates the energy Fermi level at the Dirac point and thus the back-gated GNR can deliver a much higher $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio ($10^4\times$ bigger ratio) when compared to the top gate applied inputs case. However, as the graphene sheet and the back gate contact is generally separated by a thick dielectric layer (e.g., $\approx 300\,\mathrm{nm}$ SiO_2), back-gated GNR topologies were proven to suffer from very large parasitic capacitances [114], [23], rendering them, at least in the current development state, rather impractical when compared to top-gated GNR structures.

3.4 Performance Evaluation

In this section we are concerned with the evaluation of the potential performance of the proposed structures. Given that they are able to deliver basic

Table 3.3: 2-input GNRs and 7 nm CMOS Gates Propagation Delay, Area, and Power.

	$\tau_p[ps]$		Active Area $[nm^2]$	
	GNR	CMOS	GNR	CMOS
AND	$2.790 \cdot 10^{-2}$	9.618	$2.428 \cdot 10^{1}$	$1.452 \cdot 10^{3}$
NAND	$1.931 \cdot 10^{-2}$	7.556	$2.719 \cdot 10^{1}$	$0.968 \cdot 10^{3}$
OR	$1.271 \cdot 10^{-2}$	8.309	$2.453 \cdot 10^{1}$	$1.452 \cdot 10^{3}$
NOR	$1.948 \cdot 10^{-2}$	9.175	$2.698 \cdot 10^{1}$	$0.968 \cdot 10^{3}$
XOR	$1.086 \cdot 10^{-2}$	9.168	$2.428 \cdot 10^{1}$	$2.420 \cdot 10^{3}$
XNOR	$1.602 \cdot 10^{-2}$	10.870	$2.452 \cdot 10^{1}$	$2.904 \cdot 10^{3}$
	Power $[nW]$		Power-delay Product $[ps\text{-}nW]$	
	GNR	CMOS	GNR	CMOS
AND	$4.135 \cdot 10^{1}$	$6.242 \cdot 10^{2}$	1.1560	$6.003 \cdot 10^{3}$
NAND	$7.218 \cdot 10^{1}$	$5.247 \cdot 10^{2}$	1.3940	$3.965 \cdot 10^{3}$
OR	$3.505 \cdot 10^{1}$	$5.535 \cdot 10^{2}$	0.4453	$4.599 \cdot 10^{3}$
NOR	$9.884 \cdot 10^{1}$	$4.528 \cdot 10^{2}$	1.9250	$4.155 \cdot 10^{3}$
XOR	$8.165 \cdot 10^{1}$	$1.049 \cdot 10^{3}$	0.8864	$9.616 \cdot 10^{3}$
XNOR	$6.005 \cdot 10^{1}$	$1.229 \cdot 10^{3}$	0.9617	$1.336 \cdot 10^{4}$

Boolean gate behaviours the number we report are giving an indication about the expected performance of fully designed butterfly GNR based gates. Apart of the usual area, delay, and power consumption figures of merit we also investigate the sensitivity of the proposed structures to V_{DD} variations and edge defects and attempt to determine the V_{DD}'s lower bound for proper operation.

3.4.1 Propagation Delay, Area, and Power

While the butterfly GNR-based structure, graphically depicted in Figure 2.5, is not a fully design gate it can be regarded as the main building block of

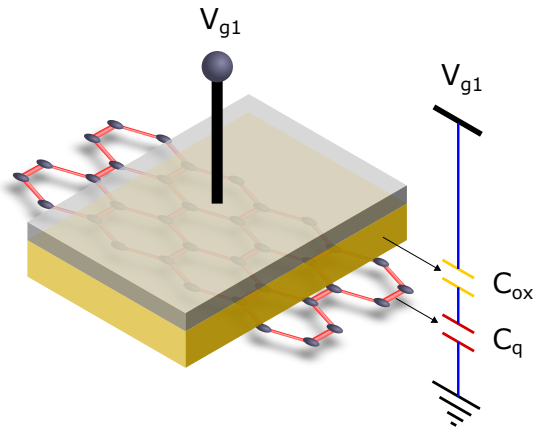

Figure 3.4: Top Gate Capacitance.

a GNR-based Boolean gate. Thus, by analyzing the performance of its 2- and 3-input instances we can gain some insight - even though speculatively - into the potential merit of our approach when compared with CMOS and other Graphene based state of the art designs. To this end, we first evaluate the butterfly GNRs mapping the basic set of 2- and 3-input Boolean functions $@V_{\mathrm{DD}} = 0.2\,\mathrm{V}$ and the Boolean logic gate counterparts implemented in a commercial $7\,\mathrm{nm}$ ($V_{\mathrm{DD}} = 0.7\,\mathrm{V}$) CMOS technology. We are interested in the worst case input to output propagation delay, the active area footprint (the conduction channels area), and power consumptions. The CMOS gates figures were measured in Cadence RTL Compiler [119].

For deriving the GNR propagation delay, we assume that a $12\,\mathrm{nm}$ Al_2O_3 layer is utilized as insulator underneath the top gate contacts [120], and compute the delay τ_p by using Elmore RC delay, as $\tau_p = (R_{\mathrm{gnr}}+2R_{\mathrm{C}})\cdot C_{\mathrm{g}}$, where R_{gnr} is the GNR resistance between the drain and source contacts derived by the NEGF model, R_{C} is the ohmic resistance between graphene and metal contacts, and C_{g} is the top gate capacitance (depicted in Figure 3.4 as a function of the quantum capacitance, C_{q}, and the oxide capacitance, C_{ox} in series) [116], [121]. As metal-graphene contact resistance R'_{C} reported in the literature vary from $100\,\Omega\cdot\mu\mathrm{m}$ to $1\,\mathrm{k}\Omega\cdot\mu\mathrm{m}$ [122] we set $R'_{\mathrm{C}} = 200\,\Omega\cdot\mu\mathrm{m}$ in our evaluations. Furthermore, in order to compute the quantum capacitance C_{q} we followed the approach in [110], [123], and expressed it as a function of the density of states $DOS(E)$, the thermal broadening function $F_{\mathrm{T}}(E)$, and the energy E,

Table 3.4: 3-input GNRs and 7 nm CMOS Gates Propagation Delay, Area, and Power.

	$\tau_p[ps]$		Active Area $[nm^2]$	
	GNR	CMOS	GNR	CMOS
AND	$3.860 \cdot 10^{-2}$	$1.116 \cdot 10^{1}$	$3.056 \cdot 10^{1}$	$1.936 \cdot 10^{3}$
NAND	$2.339 \cdot 10^{-2}$	7.635	$3.056 \cdot 10^{1}$	$1.452 \cdot 10^{3}$
OR	$1.804 \cdot 10^{-2}$	8.547	$2.707 \cdot 10^{1}$	$1.936 \cdot 10^{3}$
NOR	$2.472 \cdot 10^{-2}$	$1.092 \cdot 10^{1}$	$2.973 \cdot 10^{1}$	$1.452 \cdot 10^{3}$
XOR	$1.479 \cdot 10^{-2}$	$1.373 \cdot 10^{1}$	$2.667 \cdot 10^{1}$	$4.840 \cdot 10^{3}$
XNOR	$2.262 \cdot 10^{-2}$	$1.637 \cdot 10^{1}$	$2.667 \cdot 10^{1}$	$5.808 \cdot 10^{3}$
	Power $[nW]$		Power-delay Product $[ps\text{-}nW]$	
	GNR	CMOS	GNR	CMOS
AND	$2.326 \cdot 10^{1}$	$3.998 \cdot 10^{2}$	0.898	$4.461 \cdot 10^{3}$
NAND	$8.701 \cdot 10^{1}$	$3.433 \cdot 10^{2}$	2.035	$2.621 \cdot 10^{3}$
OR	$6.472 \cdot 10^{1}$	$3.473 \cdot 10^{2}$	1.167	$2.968 \cdot 10^{3}$
NOR	$9.868 \cdot 10^{1}$	$2.983 \cdot 10^{2}$	2.439	$3.257 \cdot 10^{3}$
XOR	$7.167 \cdot 10^{1}$	$1.768 \cdot 10^{3}$	1.060	$2.427 \cdot 10^{4}$
XNOR	$4.090 \cdot 10^{1}$	$2.529 \cdot 10^{3}$	0.925	$4.140 \cdot 10^{4}$

as:

$$C_{\mathrm{q}} = \mathrm{q}^2 \cdot \int_{-\infty}^{+\infty} DOS(E) \cdot F_{\mathrm{T}}(E - (\mu_1 - \mu_2))\, \mathrm{d}E. \tag{3.1}$$

Table 3.3 presents the input to output propagation delay, the active area, and the power consumption corresponding to 2-input butterfly GNR structures dimensionally defined in Table 3.1 and 7 nm 2-input CMOS gate counterparts. In a nutshell the Table reveals that when compared with CMOS the GNR structures provide input to output propagation delay, power consumption, and power-delay product reductions of 2, 1 to 2, and 3 to 4 orders of magnitude, respectively.

We observe that while for the CMOS case, the propagation delay has similar values for all gates (44% maximum variation with respect to the NAND gate minimum delay of $7.556\,\mathrm{ps}$), for the GNR case delay disparities between various gates can go to up to about $2.6\times$. The high delay variation among GNR structures is related to I_{ON} current dependence on GNR structures geometry and gate contacts topology and it can be dealt with by incorporating delay constraints into the GNR geometries design space exploration. A similar phenomenon can be observed in terms of power consumption, as faster gates consume more power, and to a limited extend in the power-delay product case. When compared in terms of active area the GNR structures require a 2 orders of magnitude smaller footprint. We note that GNR structures have similar areas (which benefit the layout) but somehow different delay and power consumption. This implies that by keeping roughly the same area while changing the GNR geometry we can obtain very different conduction behaviour and performance figures, which is not the case for CMOS based designs.

Table 3.4 summarizes delay, area, and power consumption for 3-input GNR structures and CMOS counterparts. We observe a similar trend as for the 2-input case from Table 3.3, i.e., GNR structures provide input to output propagation delay, power consumption, and power-delay product reductions of 2 to 3, 1 to 2, and 3 to 4 orders of magnitude, respectively, and about 2 orders of magnitude smaller active area. We note that GNR structures advantage over CMOS is even more substantial as their area and delay are only slightly increasing when compared with the 2-input case. By comparing the data in Tables 3.3 and 3.4, we observe that CMOS 3-input gates area footprint (delay) increases by 33% to 100% (up to 51%) relative to the 2-input gates area (delay) while for the GNR structures area (delay) changes are from 9% to 26% (21% to 42%). Thus, we can conclude that while complex CMOS logic gates require larger area and are slower this is not the case for the proposed GNR structures.

To get inside on the way our work positions against state of the art graphene based gates we also compare with 2-input pn-junctions-based gates proposed in [115] and [116]. Table 3.5 indicates that our structures outperform the pn-junctions-based Boolean gates introduced in [115] by 1 order of magnitude in terms of delay. Moreover, when comparing with the 2-input NAND in [116] ($0.105\,\mathrm{um}^2$ area, $0.177\,\mathrm{ps}$ delay, $3.15\,\mu\mathrm{W}$ power consumption and $0.557\,\mathrm{ps}\cdot\mu\mathrm{W}$ power-delay product), our 2-input NAND mirroring GNR structure requires 3 orders of magnitude smaller area, is 1 order of magnitude faster, consumes $44\times$ less power, and exhibits a 2 orders of magnitude lower power-delay product. The better performance provided by our structures is mainly induced by the fact that we make use of graphene properties to directly eval-

Table 3.5: 2-input GNR and pn-Junctions Gate Delays.

	$\tau_p[ps]$	
	GNR	[115]
AND	$3.860 \cdot 10^{-2}$	0.486
NAND	$2.339 \cdot 10^{-2}$	0.567
OR	$1.804 \cdot 10^{-2}$	0.486
NOR	$2.472 \cdot 10^{-2}$	0.567
XOR	$1.479 \cdot 10^{-2}$	0.486
XNOR	$2.262 \cdot 10^{-2}$	0.486

uate the function instead of relying of the traditional switch (transistor) based approach.

All these results suggest that, potentially speaking, GNR-based logic gates built with the proposed structures can substantially outperform advanced CMOS counterparts and can open a novel avenue towards future post-Si nanoelectronics. To get further inside into our approach potential, in the remainder of the section, we investigate operation robustness aspects related to V_{DD} variation and scaling and non-ideal graphene fabrication process and patterning.

3.4.2 V_{DD} Variation Robustness

To investigate the effect of V_{DD} variations on GNR's stable operation, we consider the butterfly GNR structures with 2 and 3 inputs that mirror the NOR Boolean functionality, vary V_{DD} with $\pm 10\%$ in increments of 2% with respect to the nominal voltage $V_{\text{DD}} = 0.2\,\text{V}$, and measure the GNR conductance corresponding to each of the 4 primary 2-input combinations: $(V_{\text{g1}}, V_{\text{g2}}) = (0,0); (0,1); (1,0); (1,1)$ V (or 8 input combinations for the 3-input case). Figure 3.5 and Figure 3.6 graphically present G as a function of V_{DD} for the 2-input and 3-input, respectively, NOR butterfly GNR structures.

One can observe that G experiences very little variations (maximum 1.13% for the 2-input case and 1.94% for the 3-input case), with respect to the nominal $V_{DD} = 0.2\,\text{V}$ values. Our experiments also reveal that the V_{DD} variation effect on the timing characteristics is relatively small, i.e., the input to output propagation delay varies on average with 6.0% and 5.6% for the 2-input and 3-input case, respectively.

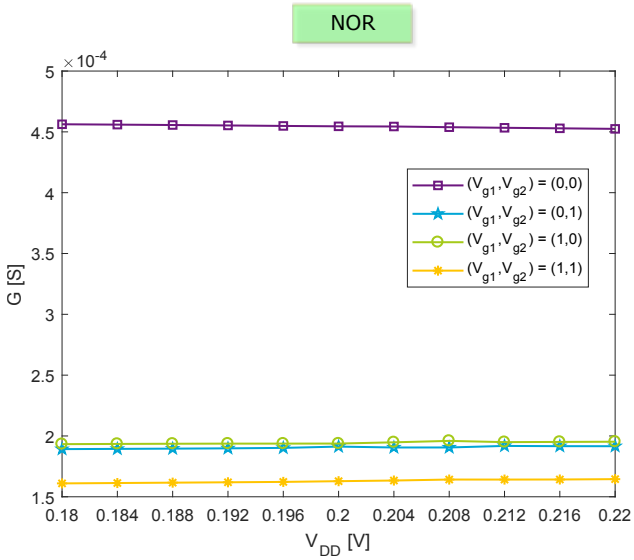

Figure 3.5: 2-input NOR GNR G Stability to V_{DD} Variations.

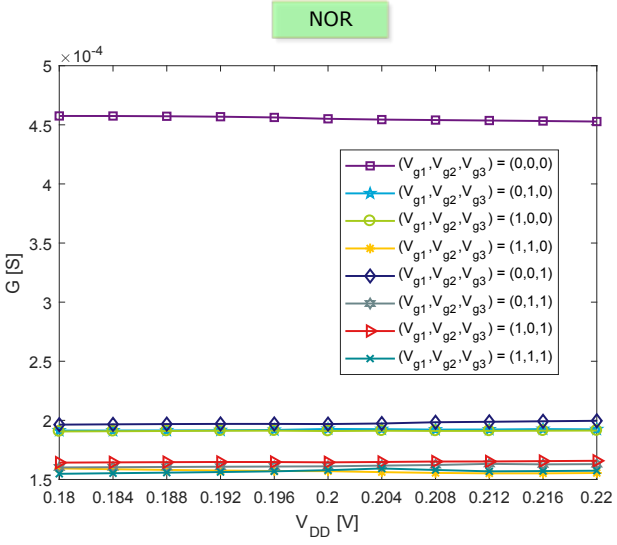

Figure 3.6: 3-input NOR GNR G Stability to V_{DD} Variations.

3.4.3 V_{DD} Lower Bound

In this section, we attempt to asses the lowest V_{DD} value for which we can still obtain butterfly GNR structures able to mirror basic Boolean functionality while being able to provide an I_{ON}/I_{OFF} current ratio bigger than a certain threshold (i.e., big enough to allow the differentiation between logic low and logic high voltage levels). To this end, we consider 4 different V_{DD} values (i.e., $0.1\,\text{V}$, $0.05\,\text{V}$, $0.02\,\text{V}$, and $0.01\,\text{V}$). For each V_{DD} value, we perform a DSE in order to obtain butterfly GNR structures which mirror 2-input AND and 2-input NOR functionality.

The obtained GNR geometries and contacts topologies for each V_{DD} value are summarized in Table 3.6 and Table 3.7, for AND and NOR, respectively. We observe that, while in general both the geometry and contacts topology need to change with either V_{DD} or Boolean functionality change, in some cases, it suffices to modify the contacts topology only. For example, the NOR geometries for $V_{DD} = 0.01\,\text{V}$ and $V_{DD} = 0.02\,\text{V}$ are identical, the only difference being P_{V_g} (the top gate contacts position with respect to the source and drain contacts), $4\sqrt{3}$ versus $2\sqrt{3}$. Another example is for the AND and NOR geometries when $V_{DD} = 0.01\,\text{V}$, in which case, the only difference is the applied V_{back} voltage value ($0.2\,\text{V}$ versus $0\,\text{V}$).

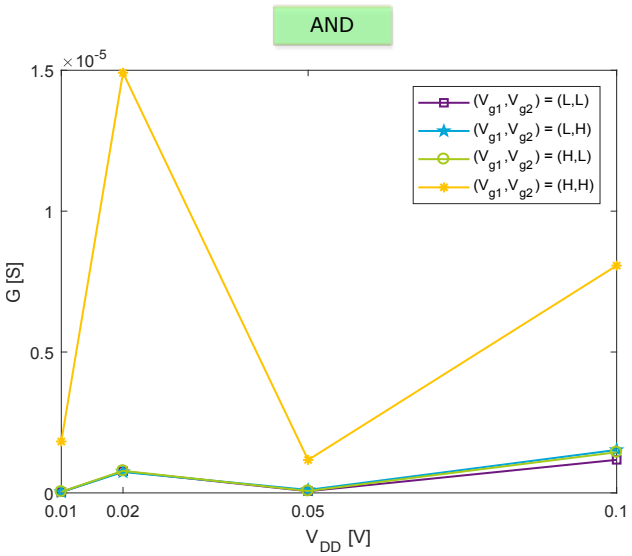

Figure 3.7: 2-input AND GNR Conductance vs V_{DD}.

Figure 3.7 (3.8) presents the conduction of the four AND (NOR)

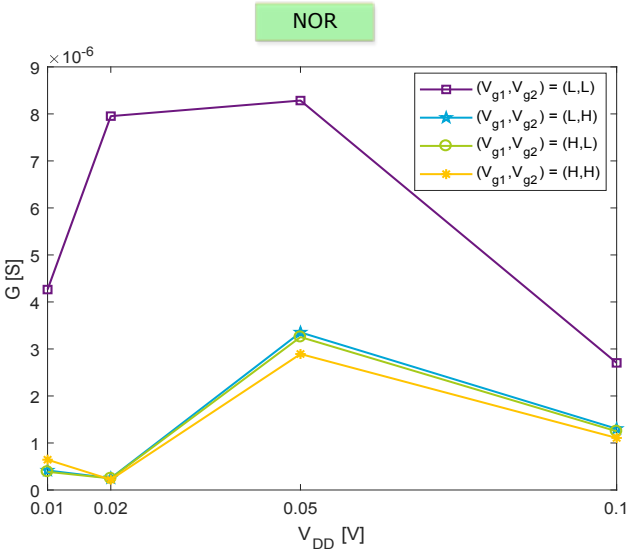

Figure 3.8: 2-input NOR GNR Conductance vs V_{DD}.

GNRs corresponding to all possible input combinations $(V_{\mathrm{g1}}, V_{\mathrm{g2}}) = (L, L); (L, H); (H, L); (H, H)$, where L and H denote logic low input voltage level and logic high input voltage level, respectively. we note that while L is always $0\,\mathrm{V}$, H is equal to the GNR specific V_{DD} value. In Figure 3.7, the lines colored in (purple, blue, and green) and orange reflect conductance values for logic low and hight output value, respectively. The Figure suggests that the structure tailored to $V_{\mathrm{DD}} = 0.02\,\mathrm{V}$ operation provides the best "on" to "off" conductance ratio and by implication the most robust operation. The same observation holds true for the NOR case in Figure 3.8, which suggest that nonintuitive design optimization avenues are potentially available for the design of butterfly GNR based Boolean gates and circuits.

We further investigate V_{DD} limitations from a different angle by considering the $V_{\mathrm{DD}} = 0.1\,\mathrm{V}$ specific GNR AND (NOR) geometry in Tables 3.6 (3.7) and varying V_{DD} from 100 to $1\mathrm{mV}$ while adjusting V_{g1} and V_{g2} logic high voltage values accordingly. Figure 3.9 (3.10) presents AND (NOR) GNR conductance evolution while V_{DD} decreases from $100\,\mathrm{mV}$ to $1\,\mathrm{mV}$ while using the same legend as in Figure 3.7. One can observe the best performance corresponds to the nominal V_{DD} values for which the structures were designed and that the high to low conductance ratio decreases when V_{DD} is diminished. The desired functionality is maintained until a certain V_{DD} threshold when the G values (which reflect the Boolean function output), become indistinguishable

Table 3.6: 2-input AND GNR Topology vs V_{DD}.

V_{DD} $[V]$	0.01	0.02	0.05	0.1
W [a]	47	41	47	41
L [a]	$25\sqrt{3}$	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$
W_{c} [a]	11	14	11	8
L_{c} [a]	$3\sqrt{3}$	$7\sqrt{3}$	$3\sqrt{3}$	$9\sqrt{3}$
$P_{V_{\text{g}}}$ [a]	$3\sqrt{3}$	$3\sqrt{3}$	0	$3\sqrt{3}$
$W_{V_{\text{g}}}$ [a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back} $[V]$	0	0	0	0

Table 3.7: 2-input NOR GNR Topology vs V_{DD}.

V_{DD} $[V]$	0.01	0.02	0.05	0.1
W [a]	47	47	41	41
L [a]	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$	$27\sqrt{3}$
W_{c} [a]	17	17	14	8
L_{c} [a]	$5\sqrt{3}$	$5\sqrt{3}$	$11\sqrt{3}$	$9\sqrt{3}$
$P_{V_{\text{g}}}$ [a]	$4\sqrt{3}$	$2\sqrt{3}$	$4\sqrt{3}$	$3\sqrt{3}$
$W_{V_{\text{g}}}$ [a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back} $[V]$	0	0	0.2	0.2

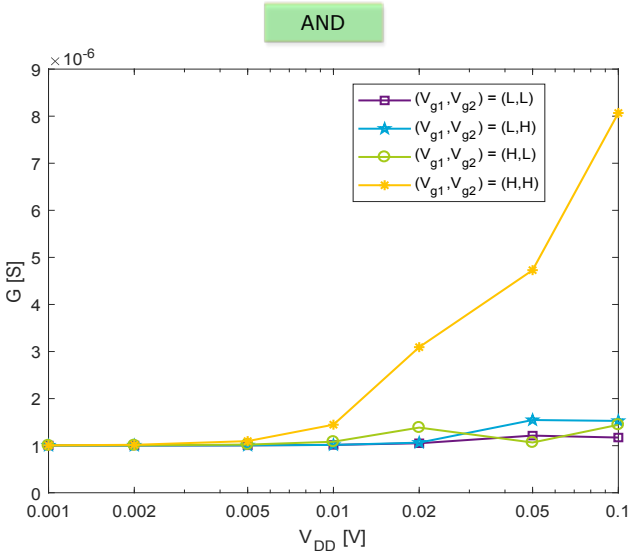

Figure 3.9: 0.1 V 2-input AND GNR Conductance vs V_{DD}.

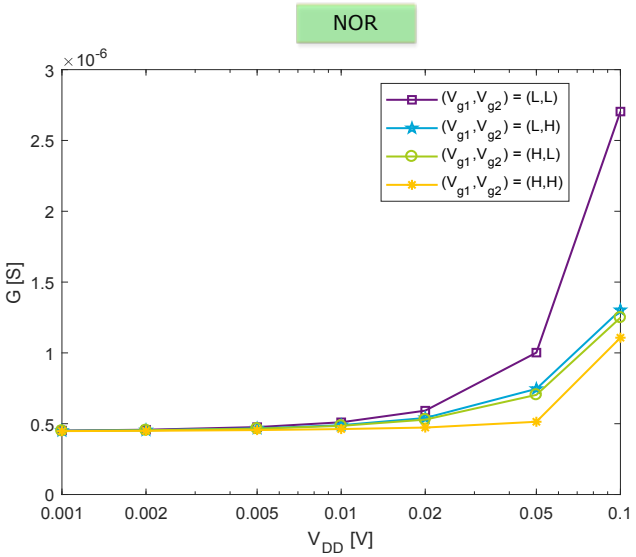

Figure 3.10: 0.1 V 2-input NOR GNR Conductance vs V_{DD}.

between logic high and logic low, or the Boolean logic is not correctly reflected any longer, which is 20 mV for AND and about 10 mV for NOR. This suggests that any GNR structure has its own V_{DD} lower operation value, which is highly dependent on the GNR geometry and contacts topology.

3.4.4 Fabrication Challenges and Edge Defects

In this section, we first briefly discuss GNR fabrication status, difficulties, and challenges, and subsequently investigate the GNR edge defects potential impact on the proposed structures.

Fabrication Status and Challenges

Up to date, several fabrication methods have been utilized to produce GNRs, such as top-down lithographic patterning [70], [71], chemical procedures [72], and longitudinally unzipping of high quality grown carbon nanotubes [73], [74]. While top-down lithographic patterning is very promising for the fabrication of well-arranged $12 - 20$ nm GNRs for large-scale integration, carbon nanotubes "unzipping" or "unrolling" can successfully produce sub-20 nm GNR [124]. Other GNR fabrication strategies include nanowire mask lithog-

raphy [125] and block copolymer lithography, which both can produce sub-10 nm GNRs [126].

Despite their fast development, all GNR fabrication approaches are still confronting some major difficulties and challenges, e.g., (i) lack of scalability and designable densely alignment, (ii) GNR damage, edge defects, and electronic properties degradation due to conventional plasma etching, (iii) time-consuming and expensive. Over the last few years, researchers focused on the development of GNR fabrication, and tried to address these issues. [96] provided one approach to scalable graphene, which obtains graphene by means of Chemical Vapour Deposition (CVD) followed by a transfer from the original Ni substrate to a Si/SiO_2 substrate. [127] introduced a facile route for fabricating densely packed aligned sub-20 nm GNRs array by making use of symmetric block copolymer lithography. In [128], the authors obtained low edge-defects GNRs with 30 nm width by means of electron beam lithography followed by O_2 neutral beam etching on large-scale CVD-grown graphene. [75] proposed a fast and inexpensive approach to fabricate GNRs as narrow as 9 nm with an $I_{\text{ON}}/I_{\text{OFF}}$ current ratio of 70 at room temperature and carrier mobility of $300\ \mathrm{cm^2v^{-1}s^{-1}}$. [76] made use of the surface-assisted synthesis approach to fabricate atomically precise, low-edge-defect GNRs, e.g., 3-Armchair GNRs (1 hexagon width) and 6-Zigzag GNRs (6 hexagon width), which indicates that the structures we introduced in this chapter can be potentially fabricated in the close future. However, there are still hurdles and challenges ahead on the road towards all-graphene electronics, e.g., (i) enable GNR bandgap modulation to the useful value range of $0.5 - 1.5$ eV [76], (ii) increase GNR fabrication process time and cost efficiency, (iii) avoid high Schottky barriers for nerrow metal-GNRs contacts [76], (iv) scale GNR-based prototype devices to high integration densities [129], and (v) fabrication of GNRs interconnects.

Even though new fabrication technologies (e.g., scalable bottom-up approaches and on-surface synthesis methods) are exceeding the precision limit of modern lithographic approach and can produce atomically precise GNRs with well-defined width, edge defects cannot be completely eliminated, at least not for the time being and in view of this we evaluate their impact on GNR's electrical properties and by implication on the behavior of the proposed butterfly structures.

Edge Defects

As a thorough analysis of random edge defects influence on GNR electrical characteristics is out of the scope of the current chapter we restrict our investi-

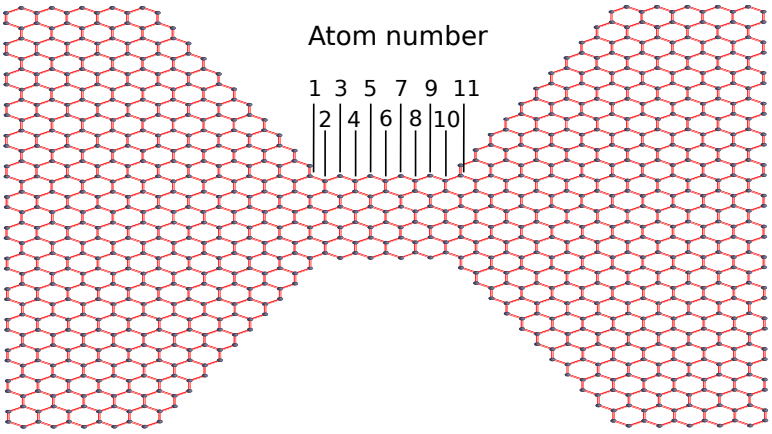

Figure 3.11: Missing Atoms on the Constriction Upper Edge.

gation to the case when one or two defects are present in the GNR constriction edge and make use of the NEGF-Landauer formalism while neglecting the phonon and electron scattering.

To this purpose we choose a 2-input AND GNR with $W = 41, L = 25\sqrt{3}, W_{\text{c}} = 8, L_{\text{c}} = 4\sqrt{3}, P_{V_{\text{g}}} = 2\sqrt{3}, W_{V_{\text{g}}} = 6\sqrt{3}, V_{\text{back}} = 0\,\text{V}, V_{\text{d}} = 0.2\,\text{V}$, $V_{\text{s}} = 0\,\text{V}$, $V_{\text{g1}} = 0$ or $0.2\,\text{V}, V_{\text{g2}} = 0$ or $0.2\,\text{V}$ and derive its conductance corresponding to the four input combinations for GNR with perfect edges and for 11 defected GNRs, each one missing one of the atoms indicated in Figure 3.11. Table 3.8 summarizes the obtained conductance values and high/low ratios for all considered cases. Note that G_{00} corresponds to $V_{\text{g1}} = 0\,\text{V}, V_{\text{g2}} = 0\,\text{V}$, G_{01} corresponds to $V_{\text{g1}} = 0\,\text{V}, V_{\text{g2}} = 0.2\,\text{V}$, etc. One can observe that the conductance variations are large, i.e., up to $28.6\times$, $37.8\times$, $52.4\times$ and $6.1\times$ for G_{00}, G_{01}, G_{10}, and G_{11}, respectively. Additionally, defect presence induces G_{11}/G_{01} and G_{11}/G_{10} ratios decrease and in most of the cases a G_{11}/G_{00} substantial increase, which is quite interesting as it suggest that defects might be helpful rather than harmful. While from the perspective of high/low conductance ratio edge defects deteriorate GNR's electronic properties one can notice that GNRs with edge defects can still reflect the expected Boolean functionality.

Table 3.8: Conductance of Ideal and Incomplete 2-input AND GNR.

	Conductance [S]				Ratio		
	G_{00}	G_{01}	G_{10}	G_{11}	G_{11}/G_{00}	G_{11}/G_{01}	G_{11}/G_{10}
Without defects	$3.829 \cdot 10^{-8}$	$5.668 \cdot 10^{-8}$	$4.138 \cdot 10^{-8}$	$3.012 \cdot 10^{-6}$	79	53	73
Atom 1 defect	$2.010 \cdot 10^{-8}$	$7.068 \cdot 10^{-8}$	$4.761 \cdot 10^{-8}$	$2.462 \cdot 10^{-6}$	122	35	52
Atom 2 defect	$1.115 \cdot 10^{-8}$	$1.982 \cdot 10^{-7}$	$2.763 \cdot 10^{-7}$	$6.936 \cdot 10^{-6}$	622	35	25
Atom 3 defect	$1.654 \cdot 10^{-7}$	$2.198 \cdot 10^{-6}$	$7.446 \cdot 10^{-7}$	$1.073 \cdot 10^{-5}$	65	5	14
Atom 4 defect	$3.541 \cdot 10^{-8}$	$7.741 \cdot 10^{-7}$	$1.082 \cdot 10^{-6}$	$1.338 \cdot 10^{-5}$	378	17	12
Atom 5 defect	$1.479 \cdot 10^{-7}$	$1.373 \cdot 10^{-6}$	$1.304 \cdot 10^{-6}$	$2.036 \cdot 10^{-5}$	138	15	16
Atom 6 defect	$1.611 \cdot 10^{-7}$	$7.553 \cdot 10^{-7}$	$2.210 \cdot 10^{-6}$	$1.679 \cdot 10^{-5}$	104	22	8
Atom 7 defect	$1.132 \cdot 10^{-6}$	$8.786 \cdot 10^{-7}$	$1.676 \cdot 10^{-6}$	$2.148 \cdot 10^{-5}$	19	24	13
Atom 8 defect	$6.791 \cdot 10^{-8}$	$3.360 \cdot 10^{-7}$	$2.133 \cdot 10^{-6}$	$1.251 \cdot 10^{-5}$	184	37	6
Atom 9 defect	$7.262 \cdot 10^{-8}$	$3.872 \cdot 10^{-7}$	$1.559 \cdot 10^{-6}$	$1.345 \cdot 10^{-5}$	185	35	9
Atom 10 defect	$1.679 \cdot 10^{-8}$	$1.470 \cdot 10^{-7}$	$5.185 \cdot 10^{-7}$	$7.223 \cdot 10^{-6}$	430	49	14
Atom 11 defect	$3.078 \cdot 10^{-8}$	$1.050 \cdot 10^{-7}$	$1.116 \cdot 10^{-6}$	$3.615 \cdot 10^{-6}$	117	34	3

3.5 Conclusion

In this chapter, we investigated graphene nanoribbons potential as fundamental building blocks for carbon-based implementation of Boolean logic gates and circuits. We augmented a trapezoidal Quantum Point Contact (QPC) topology with top gates to obtain a butterfly Graphene Nanoribbon (GNR) structure and demonstrated that by adjusting its topology its conductance map can mirror basic Boolean functions, thus one can use such structures instead of transistors to build carbon-based gates and circuits. We identified by means of Design Space Exploration (DSE) specific GNR topologies for 2- and 3-input $\{\text{AND}, \text{NAND}, \text{OR}, \text{NOR}, \text{XOR}, \text{XNOR}\}$ and demonstrated by means of Non-Equilibrium Green Function - Landauer based simulations that butterfly GNR-based structures operating at $V_{DD} = 0.2\,\text{V}$ outperform $7\,\text{nm}$ @$V_{DD} = 0.7\,\text{V}$ CMOS counterparts by 2 to 3, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively, while requiring 2 orders of magnitude less active area. We also investigated the effect of V_{DD} variations and V_{DD} proper operation lower bound. To this end we demonstrated that (i) NOR butterfly GNR structures are quite robust as their conductance and delay are changing by no more than 2% and 6%, respectively, (ii) V_{DD} lower bound is GNR geometry and contact topology dependent and AND and NOR GNR geometries can operate even at $10\,\text{mV}$. Finally, we considered aspects related to the practical realization of the proposed structures and concluded that even if there are still hurdles on the road ahead the latest graphene fabrication technology developments, e.g., surface-assisted synthesis, our proposal opens an alternative towards effective carbon-based nanoelectronic circuits and applications.

Note. The content of this chapter is based on the following papers:

Y. Jiang, N. Cucu Laurenciu, and S.D. Cotofana, **On Basic Boolean Function Graphene Nanoribbon Conductance Mapping**, *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, vol. 66(5), p. 1948-1959, 2018.

Y. Jiang, N. Cucu Laurenciu, and S.D. Cotofana, **On Carving Basic Boolean Functions on Graphene Nanoribbons Conduction Maps**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2018.

4

Parameterized Verilog-A SPICE-compatible Graphene Nanoribbon Model

To enable the exploration and evaluation of potential graphene-based circuit designs, we propose a fast and accurate Verilog-A physics-based model of a 5-terminal trapezoidal Quantum Point Contact (QPC) Graphene Nano-Ribbon (GNR) structure with parameterizable geometry. The proposed model computes the GNR conductance based on the Non-Equilibrium Green's Function (NEGF)-Landauer formalism, via a Simulink model called from within the Verilog-A model. Furthermore, model accuracy and versatility are demonstrated by means of Simulink assisted Cadence Spectre simulation of a simple test case GNR-based circuit and a GNR-based 2-input XOR gate.

4.1 Introduction

Since fabrication technology of graphene-based logic and circuits is still in an early stage, modeling and simulation have been playing an important role for providing a physical insight into futuristic graphene-based circuits, and a proper evaluation on its potential performance. Numerical simulations for Graphene Nano-Ribbon Field-Effect Transistors (GNRFETs), based on non-equilibrium Green's function (NEGF) formalism have been published [130], which are accurate, but are too complex. Another simulator for GNRFETs tries to take the advantage of a look-up-table to speed up the simulation process, but with the design parameters increase and change, the simulator needs to rebuild the model, such that its complexity increases [131]. Analytical models that simulate Schottky-Barrier-Type graphene nanoribbon field-effect

transistor (SB-GNRFETs) and graphene nanoribbon tunnel field effect transistors (GNR-TFETs) are published in [132], [133], respectively. The simulator presented in [134], [135] provide a SPICE-compatible model for GNRFETs simulation, also enabling circuit-level delay and power analysis under process variation.

In order to bring Graphene Nano-Ribbon specific phenomena from the physics to the circuit-level, to allow for graphene-based circuit design and optimizations, a fast and parameterized model that enables electrical simulation is required. However, since GNRs behavior and potential benefit in the circuit context are not fully comprehended, such a model should preserve the physical simulation accuracy degree. To this end, in this chapter we focus on the graphene nanoribbon simulation and introduce a Verilog-A SPICE-compatible generic model based on NEGF formalism, which builds upon an accurate physics formalization, by computing GNR specific variables, e.g., conductance, via internally called Simulink code. In this way, the proposed GNR model symbiotically exploits accurate (in perfect agreement with physics results) Simulink results and optimized SPICE circuit solvers (e.g., Spectre, HSPICE). As discussion vehicle, we consider a 5-terminal trapezoidal Quantum Point Contact (QPC) GNR topology, whose conductance map can mirror basic Boolean functions [1], and develop a generic 8-parameter Verilog-A model able to capture the behavior of any QPC topology instance. To illustrate the proposed model applicability, we consider a simple test case circuit and the GNR-based 2-input XOR gate introduced in [136], and simulate the afferent I-V characteristic, via Cadence Spectre and Matlab Simulink. The simulation results indicate that our proposed physics-based Verilog-A GNR model is accurate and enables the proper evaluation of graphene-based circuits potential performance.

The remaining of this chapter is structured as follows: Section 4.2 entails an overview of the physics-based Verilog-A GNR model. Section 4.3 presents the simulation results and comments on the practical applicability of our proposed Verilog-A GNR model. Finally, some concluding remarks are given in Section 4.4.

4.2 Verilog-A GNR model

In this section, we present the GNR model SPICE interface and its parameters, and describe the mathematical formalism underlying the GNR behavior. Further, in Section 4.2.2, we outline the simulation flow for a transient nodal

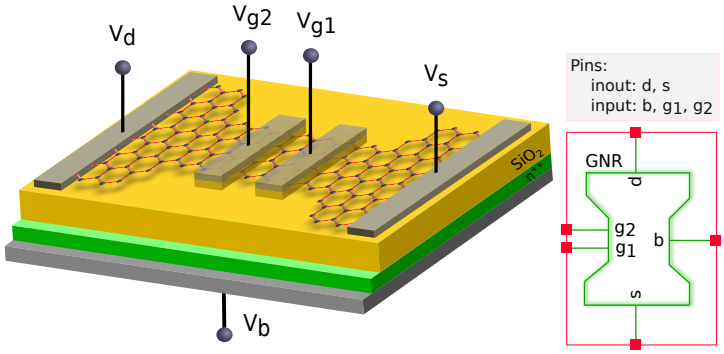

Figure 4.1: Trapezoidal QPC Topology and Associated SPICE Symbol.

analysis.

4.2.1 GNR model specification and formalism

The proposed Verilog-A model captures the behavior of a generic trapezoidal QPC (with zig-zag atomic edge alignment) structure [114], as depicted in Fig. 4.1, in which we make use of the GNR as a conduction channel. The Verilog-A model has 5 pins and 8 parameters (presented in Fig. 3.1 in Section 3.2) capturing: (i) the nanoribbon geometry, i.e., width W, length L, constriction width W_c, and constriction length L_c, and (ii) the top gates topology, i.e., position PV_{g1}, PV_{g2} (the distance between the two top gate contacts and the source/drain contacts, respectively) and width WV_{g1}, WV_{g2} (the top gate contacts width). We note that all values are expressed in terms of a ($0.142\,\mathrm{nm}$), the distance between two graphene lattice adjacent carbon atoms. In this way, the model is generic and can accommodate a wide range of GNR shapes and topologies.

For modelling the GNR electronic transport, we employ previously mentioned the Non-Equilibrium Green Function quantum transport model as shown in Section 2.2, in which the semi-empirical Tight Binding (TB) computations to obtain the system Hamiltonian, and the Landauer-Buttiker formalism to derive the GNR current and conductance.

4.2.2 Simulation flow

Let us assume a SPICE circuit description which also contains one or more GNR components, for which a transient nodal analysis is desired. At time

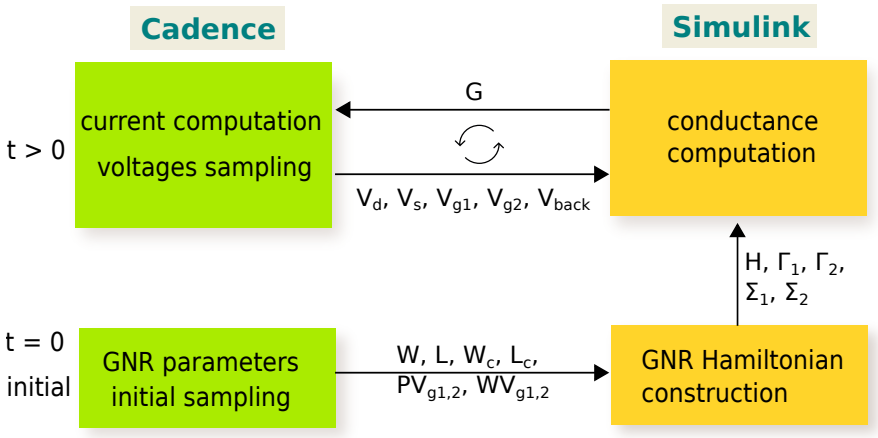

Figure 4.2: Cadence-Simulink-Based Verilog-A GNR Simulation Framework.

steps automatically chosen by the SPICE solver (e.g., Cadence Spectre; Synopsys HSPICE), the Verilog-A GNR model samples the 5 voltages (afferent to the 5 pins depicted in Fig. 4.1). The simulation flow we utilize in the proposed Verilog-A GNR model is presented in Fig. 4.2. In order to compute the conductance G, the Simulink code makes use of the GNR Hamiltonian, which is geometry dependent. Thus the Hamiltonian matrix H, and matrices $\Gamma_{1,2}$, $\Sigma_{1,2}$ are computed only once during the first-time step ($t = 0$, initial step) of the transient simulation, and saved for latter uilization in subsequent simulation steps.

Further, throughout the subsequent simulation iteration process, every time a voltage variation larger than a certain value is detected, the Verilog-A GNR model triggers the Simulink module that receives as input the GNR 5 voltages and 8 parameters (W, L, W_c, L_c, $PV_{g1,2}$, $WV_{g1,2}$). Subsequently, based on these voltages and parameters the Simulink module computes the actual and accurate GNR conductance G. Once the Simulink evaluated conductance value G is known to the Verilog-A model, the current through the GNR is updated via:

$$I(\mathrm{d},\mathrm{s}) = V(\mathrm{d},\mathrm{s}) \cdot G. \tag{4.1}$$

4.3 Simulation Results

To exemplify and evaluate the Verilog-A GNR model practical applicability, we consider a test case circuit depicted in Fig. 4.3, composed of a capacitor

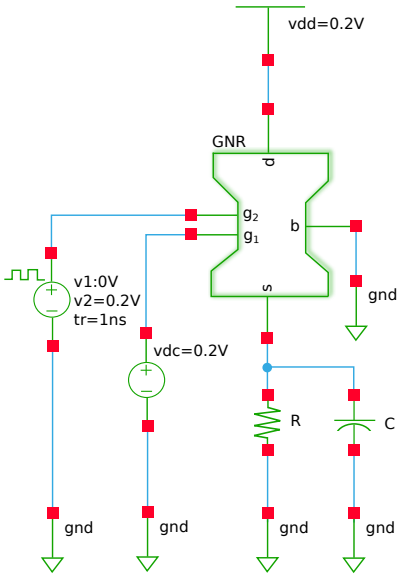

Figure 4.3: One GNR-based Circuit Simulation Setup.

of $C = 1\,\text{fF}$, a resistor R, and a GNR with geometry specified by $W = 29\,\text{a}$; $L = 19\sqrt{3}\,\text{a}$; $W_\text{c} = 17\,\text{a}$; and $L_\text{c} = 10\sqrt{3}\,\text{a}$. In addition, the gate topology is given by $PV_\text{g1} = PV_\text{g2} = 2\sqrt{3}\,\text{a}$, and $WV_\text{g1} = WV_\text{g2} = 3\sqrt{3}\,\text{a}$. The GNR structure thus defined is subjected to the following voltages: $V_\text{d} = 0.2\,\text{V}$; $V_\text{b} = 0\,\text{V}$; $V_\text{g1} = 0.2\,\text{V}$; and V_g2 which is varied from $0\,\text{V}$ to $0.2\,\text{V}$. The circuit is simulated with Cadence Spectre [119] and Matlab Simulink [137]. As example of simulated characteristics, we present in Fig. 4.4, the curves for the input voltage V_g2, and the resulted voltage V_s at the GNR's terminal, as well as the current through the GNR, I_ds, for 2 simulation scenarios: $R = 10\,\text{k}\Omega$ (case 1), and $R = 30\,\text{k}\Omega$ (case 2). The simulation results correctly capture the expected V_s and I_ds modifications induced by V_g2 changes. Furthermore, we also observe the fact that the R value has a clear impact on the maximum I_ds value. We note that based on the obtained simulation results, one could easily measure the input-to-output propagation delay, and/or the power consumed by the circuit.

Further, we take as another test case circuit the GNR-based 2-input XOR gate

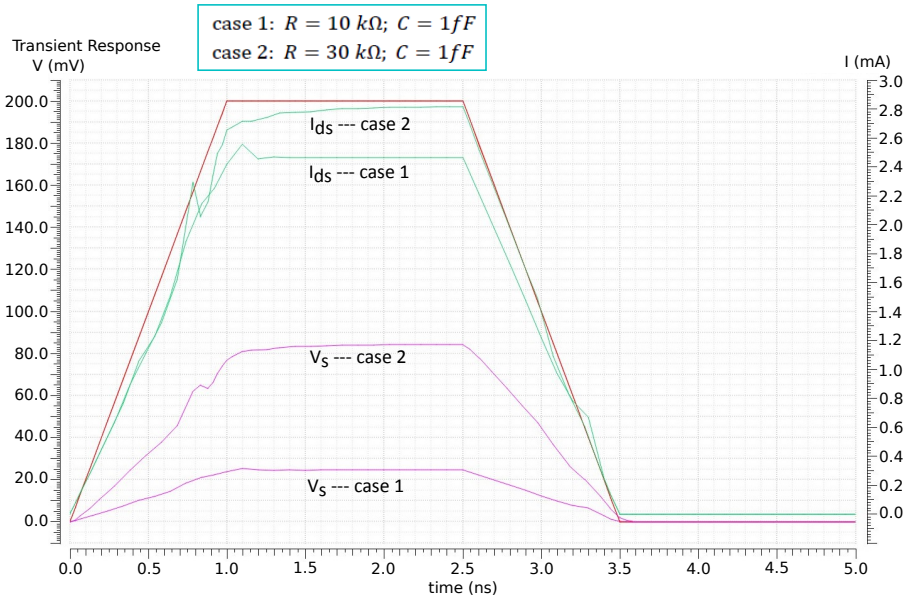

Figure 4.4: One GNR-based Circuit Simulation Results.

introduced in [136], as depicted in Fig. 4.5. The XOR gate is constructed in a complementary way with a pull-up GNR (GNR_{up}) and a pull-down GNR (GNR_{dn}). The two GNRs perform complementary functions, i.e., they are designed in such a way that GNR_{up} maps the XOR functionality onto its conductance, while GNR_{dn} conductance reflects the XNOR functionality. The XOR gate GNR_{up} geometry and contacts topology are specified by $W = 41\,\mathrm{a}$; $L = 25\sqrt{3}\ \mathrm{a}$; $W_c = 8\,\mathrm{a}$; $L_c = 4\sqrt{3}\ \mathrm{a}$, $PV_{g1} = PV_{g2} = 1\sqrt{3}\ \mathrm{a}$, and $WV_{g1} = WV_{g2} = 3\sqrt{3}\ \mathrm{a}$. The XOR gate GNR_{dn} dimensions and contacts topology are specified by $W = 29\,\mathrm{a}$; $L = 25\sqrt{3}\ \mathrm{a}$; $W_c = 5\,\mathrm{a}$; $L_c = 7\sqrt{3}\ \mathrm{a}$, $PV_{g1} = PV_{g2} = 6\sqrt{3}\ \mathrm{a}$, and $WV_{g1} = WV_{g2} = 3\sqrt{3}\ \mathrm{a}$. In order to simulate this test case circuit, we apply two gate inputs (V_{g1}, V_{g2}), and start with $V_{g1} = V_{g2} = 0\,\mathrm{V}$ followed by $(V_{g1}, V_{g2}) = (0.2\,\mathrm{V}, 0.2\,\mathrm{V}) \rightarrow (0\,\mathrm{V}, 0.2\,\mathrm{V}) \rightarrow (0.2\,\mathrm{V}, 0\,\mathrm{V}) \rightarrow (0\,\mathrm{V}, 0\,\mathrm{V})$, as depicted in the right plot of Fig. 4.6, where the simulation duration is $800\,\mathrm{ps}$.

The left plot in Fig. 4.6 captures the GNR-based XOR circuit output voltage response. We observe that the GNR-based XOR circuit exhibits the expected functionality and, based on this simulation, we derive the input to output propagation delay and power consumption of this GNR-based XOR gate as: (i) $7.48\,\mathrm{ps}$ delay, i.e., 18.4% smaller than that of CMOS XOR gate in $7\,\mathrm{nm}$

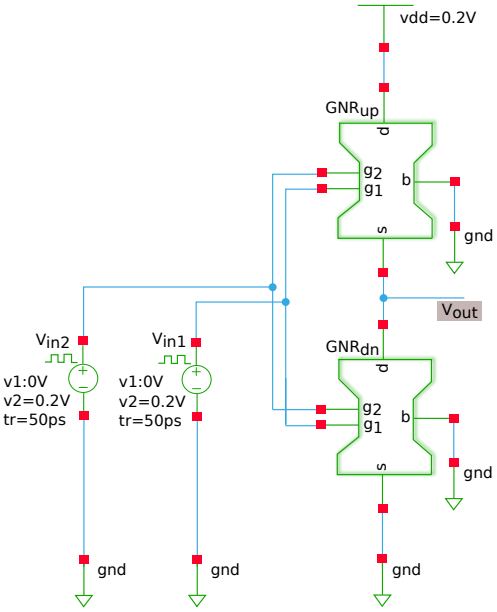

Figure 4.5: GNR-based XOR Gate Simulation Setup.

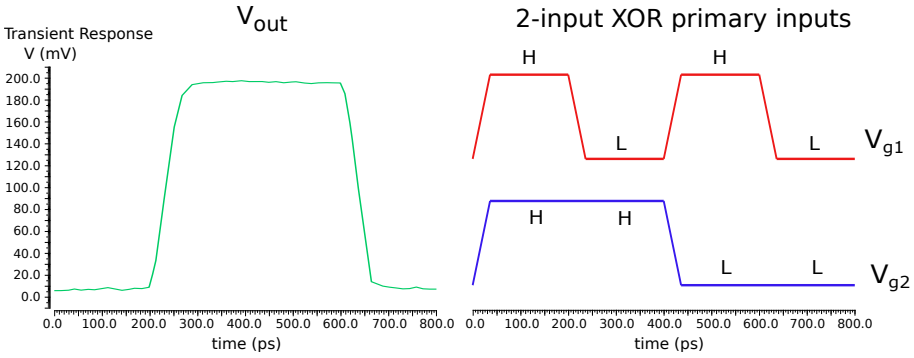

Figure 4.6: GNR-based XOR Gate Simulation Results.

technology ($9.168\,\mathrm{ps}$); and (ii) $1.734\,\mathrm{nW}$ power consumption, i.e., 2 orders of magnitude smaller than that of $7\,\mathrm{nm}$ CMOS XOR gate ($5.923\times10^{2}\,\mathrm{nW}$) [138].

As final remarks, we note that: (i) by computing the GNR conductance in Matlab Simulink, we benefit of accurate, physics-based results, which allows for a closer to reality assessment of the GNR-based circuits potential performance, when compared to, e.g., CMOS-based counterparts; (ii) a compact Verilog-A only model which directly embeds the NEGF-Landauer formalism would

be prohibitively complex and most likely slower as it requires complex numbers matrices multiplication and inverse operations, and last but not least (iii) our proposal can be easily extended to reflect the behaviour of other multi-gate GNR-based structures and/or to capture more GNRs into one Verilog-A model.

4.4 Conclusion

In this chapter we proposed an accurate physics-based Verilog-A GNR model, which enables the proper evaluation of graphene-based circuits potential performance. Our simulation results confirm its accuracy and capability to capture the behaviour of GNR based circuits, i.e., XOR gate, and to allow for performance comparison with CMOS counterparts. The development of compact Verilog-A only models, which trade accuracy for faster simulation, may constitute future work, once GNR behavior is properly understood and characterized from the circuit prospective.

Note. The content of this chapter is based on the following paper:

Y. Jiang, N. Cucu Laurenciu, and S.D. Cotofana, **Non-Equilibrium Green Function-Based Verilog-A Graphene Nanoribbon Model**, *IEEE 18th International Conference on Nanotechnology (IEEE-NANO)*, pp. 1-4, 2018.

5

GNR-based Complementary Gates

In this chapter we make use of the fact that GNR behaviour can be modulated, via top/back gate contacts, to mimic a given functionality and combine complementary GNRs for constructing Boolean gates. We first introduce a generic gate structure composed of a pull-up GNR performing the gate Boolean function and a pull-down GNR performing its complement. Then, we seek GNR dimensions and gate topologies required for the design of 1-, 2-, and 3-input graphene-based Boolean gates, validate the proposed gates by means of SPICE simulation, which makes use of a Non-Equilibrium Green's Function (NEGF)-Landauer formalism based Verilog-A model to calculate GNR conductance, and evaluate their performance with respect to propagation delay, power consumption, and active area footprint. Simulation results indicate that, when compared with $7\,\mathrm{nm}$ FinFET CMOS counterparts, the proposed gates exhibit $6\times$ to 2 orders of magnitude smaller propagation delay, 2 to 3 orders of magnitude lower power consumption, and necessitate 2 orders of magnitude smaller active area footprint. We further present Full Adder (FA) and SRAM cell GNR designs, as they are currently fundamental components for the construction of any computation system. For an effective FA implementation we introduce a 3-input MAJORITY gate, which apart of being able to directly compute FA's Carry-Out is an essential element in the implementation of Error Correcting Codes (ECC) codecs, that outperforms the CMOS equivalent Carry-Out calculation circuit by 2 and 3 orders of magnitude in terms of delay and power consumption, respectively, while requiring 2 orders of magnitude less area. The proposed FA exhibits $6.2\times$ smaller delay, 3 orders of magnitude less power consumption, while requiring 2 orders of magnitude less area, when compared with the $7\,\mathrm{nm}$ FinFET CMOS counterpart. However, due to the effective Carry-Out circuitry, a GNR-based n-bit Ripple Carry Adder, which performance is linear in the Carry-Out path, will be $108\times$ faster than an equivalent CMOS implementation. The GNR based SRAM cell provides a slightly

better resilience to DC noise characteristics, while performance-wise has a $3.6\times$ smaller delay, consumes 2 orders of magnitude less power, and requires 1 order of magnitude less area than the CMOS equivalent. These results clearly indicate that the proposed GNR-based approach is opening a promising avenue towards future competitive carbon-based nanoelectronics.

5.1 Introduction

From the design standpoint, there are several impediments to graphene-based Boolean logic that need consideration: (i) how to control the conductivity in order to obtain "on" and "off" states that are distinguishable, while not compromising the intrinsic highly advantageous properties of graphene (e.g., high carrier mobility), (ii) how to encode a specific Boolean logic transfer function onto electrical properties of graphene (e.g., conduction maps), (iii) how to find the appropriate external electrical means (e.g., top gates, back gate) that enable the graphene behaviour control and that can induce a specific logic functionality, (iv) how to make sure that digital circuits can be cascaded, i.e., clean and compatible/matching gate inputs and outputs electric levels, (v) understanding how the GNRs interact with each other when they are interconnected, and (vi) how to combine GNRs and construct graphene-based gates/circuits.

Past work in [1] proved that when a trapezoidal Quantum Point Contact (QPC) topology [114] is being augmented with top gates, and when its GNR geometry is changed, the GNR conductance can be modulated via external voltages such as top gate and back gate voltages, so that Boolean logic functions behaviour is being mirrored. This structure addresses the issue outlined in (i)-(iii), and constitutes a basic ingredient for Boolean gates construction. However, multiple aspects still need to be taken into consideration, chiefly, the manner to obtain Boolean gates which have clean and compatible primary inputs and outputs voltage levels by shaping and combining various GNRs.

In this chapter, we address the (iv)-(vi) issues resulted from the electrical interaction of GNRs, which will enable the construction of graphene-based Boolean gates and circuits. For this purpose, we make use of the methodology for designing Boolean gates by means of two complementary GNRs, i.e., a pull-up GNR performing the targeted Boolean function and a pull-down GNR performing its inverse, introduced in [136]. The GNR structures have a conduction channel made of a graphene zigzag ribbon, which is situated between the drain and source contacts. The gate primary inputs voltages are applied via one/two top gate/s. Since each gate necessitates GNRs with a desired be-

haviour (e.g., conductance) which corresponds to the Boolean function that they mimic, we identify topologies which are able to yield the behaviour of each basic function, i.e., AND, NAND, OR, NOR, XOR, XNOR, INV, and BUFF. For this purpose, we conduct a design space exploration with regard to the GNR shape and its dimensions, and the top gates contacts topology, while abiding to particular constraints (e.g., gate output voltage values which are compatible with gate input voltage values, high ratio between the high and low conductance values of the GNR).

The proposed 1-, 2-, and 3-input GNR gates are validated in Cadence by means of SPICE simulation which employs a Verilog-A model, that calls internally a Simulink model in order to compute the GNR conductance using the Non-Equilibrium Green's Function (NEGF)-Landauer formalism [114], [110], [117]. To gain insight into the potential of our proposal, we evaluate the GNR gates with respect to delay, active area footprint, and power consumption, relative to the $7\,\mathrm{nm}$ FinFET CMOS [138] counterparts. Our results indicate that proposed 1-, 2- and 3-input graphene gates outperform $7\,\mathrm{nm}$ FinFET CMOS counterparts as follows: (i) they provide up to $6\times$ and 2 orders of magnitude smaller propagation delay, (ii) they consumes 2 and 3 orders of magnitude lower power, and (iii) they require 2 orders of magnitude smaller active area footprint, respectively. We observe that, contrary to CMOS designs, the proposed GNR-based gates can yield effective power-delay trade-offs, at approximately the same area. This is because the graphene conductance main contributor is the nanoribbon geometry and its overall topology, rather than the effective area. Furthermore, the required active area is not proportional with gate's function complexity and fan-in, e.g., XOR and INV have similar footprints, which results in more compact circuit layout.

We further present GNR based designs of 1-bit Full Adder (FA) and SRAM cell, as they currently constitute the foundation for the construction of any computation system. For an effective FA implementation we design a 3-input MAJORITY gate, which apart of being able to directly compute FA's Carry-Out is an essential element in the implementation of Error Correcting Codes (ECC) decoders, that outperforms the CMOS equivalent Carry-Out calculation circuit by 2 and 3 orders of magnitude in terms of delay ($0.109\,\mathrm{ps}$ vs $11.863\,\mathrm{ps}$) and power consumption, respectively, while requiring 2 orders of magnitude less area. The proposed FA design exhibits $6.2\times$ smaller delay, 3 orders of magnitude less power consumption, while requiring 2 orders of magnitude less area, when compared with the $7\,\mathrm{nm}$ FinFET CMOS counterpart. By consequence, a GNR-based n-bit Ripple Carry Adder, which performance is linear in the Carry-Out path, will be $108\times$ faster than a CMOS implemen-

tation. The GNR based SRAM cell provides a slightly better resilience to DC noise characteristics, while performance-wise has a $3.6\times$ smaller delay, consumes 2 orders of magnitude less power, and requires 1 order of magnitude less area than the CMOS equivalent.

The rest of this chapter has the followig structure: Section 5.2 presents the proposed 1-, 2-, and 3-input GNR-based Boolean gates and their correspondant design methodology. Section 5.3 describes the simulation framework. Section 5.4 and 5.5 presents, evaluates, and compares the proposed designs with state of the art CMOS equivalents. Finally, the chapter ends with some concluding remarks in Section 5.6.

5.2 Complementary GNR Pair-based Boolean Gates

Subsequently we describe the design methodology we employed for the proposed GNR-based Boolean gates and we present the rationale behind the gates complementary construction.

We begin by noticing that there are 2 fundamental elements towards graphene-based circuits: (i) opening the graphene energy bandgap in order to switch off effectively the current, and (ii) finding how to control GNR conductance and how to enact the appropriate electrical response corresponding to a particular Boolean function. For this purpose, as GNR research vehicle to be build upon, we use a trapezoidal graphene Quantum Point Contact (QPC) which has zigzag shaped edges [114]. The GNR can be utilized as conduction channel between the source and drain contacts, which are biased by a voltage $V_d - V_s$. The bandgap opening problem can be solved to a certain extent, by carving the GNR geometry. When carving the GNR gometry and adding top and back gates with various topologies, we can modulate the graphene conductance (via voltages externally applied on the GNR top gates), such that it mirrors a particular intended Boolean function. In Figure 2.5 in Section 2.3 is illustrated the main ingredient employed for the construction of GNR-based Boolean gates, i.e., a GNR structure which is augmented with 1 back gate and 2 top gates contacts.

Figure 5.1 shows for example, the conductance map that we obtained for a GNR whose geometry was optimized in such a way that it is able to reflect the functionality of the Boolean XOR operator, with $0\,\mathrm{V}$ and $1\,\mathrm{V}$ associated to logic low and logic high voltage levels, respectively.

Subsequently, building upon the structure presented in Figure 2.5, we propose

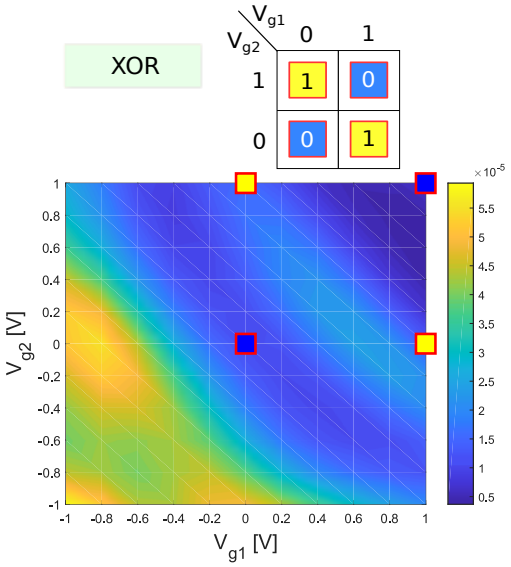

Figure 5.1: 2-input XOR Conductance Map.

GNR-based complementary Boolean gates. For this purpose, we construct each gate using 2 GNR basic building structures, as depicted in Figure 5.2: a pull-down GNR, denoted as GNR_{dn}, which has its source terminal connected to the ground V_{SS}, and a pull-up GNR, denoted subsequently as GNR_{up}, which has its drain contact connected to the supply voltage V_{DD}. The pull-up and the pull-down GNRs perform complementary functions, e.g., a NAND gate is composed of a GNR_{up} which mirrors onto its conductance the NAND logical functionality, and of a GNR_{dn} whose conductance maps the AND logical functionality.

In order to obtain the suitable GNRs for every gate, we conduct a design space exploration, by changing a set of parameters, as defined in Figure 3.1 in Section 3.2: (i) nanoribbon geometry (i.e., width W and length L, constriction width W_c and length L_c, and extrusion top length L_b and width W_b), and (ii) the topology of the top gate contacts (i.e., contacts width W_{V_g} and their position relative to the drain and source contacts P_{V_g}).

The primary output voltage level of the gate illustrated in Figure 5.2, can be approximated as:

$$V_{out} = V_{DD} \cdot \frac{G_{up}}{G_{dn} + G_{up}}, \tag{5.1}$$

where G_{dn} and G_{up} are the conductances of the pull-down and pull-up GNR,

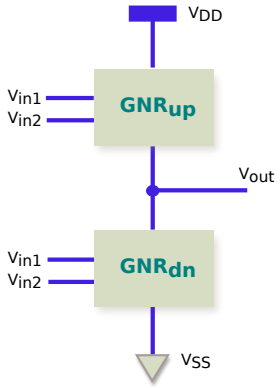

Figure 5.2: GNR Boolean Gate with Complementary GNRs.

respectively. Therefore, multiple aspects require to be taken into consideration as part of the design space exploration process, among which:

- A high ratio between the conductances of the pull-up and pull-down GNRs is the main contributor for achieving gate output voltages which are closer to the power supply and ground rails, as well as low leakage power. In particular, when the gate output voltage ought to pull-up to V_{DD}, the ratio G_{up}/G_{dn} ought to be at least > 10, for obtaining $V_{out} \geq 91\% \cdot V_{DD}$. Conversely, when the gate voltage ought to pull-down to V_{SS}, the ratio G_{up}/G_{dn} ought to be less than $1/10$, for obtaining $V_{out} \leq 9.1\% \cdot V_{DD}$.
- To avoid spurious transients in the gate output voltage, the conductance which is modulated via the gate input voltages shouldn't manifest non-linearities.
- Conductance values which can enable a reasonable input to output propagation delay and power trade-off are preferable.
- Balanced output switching delay (i.e., "0" $\rightarrow$ "1" delay which resembles "1" $\rightarrow$ "0" delay).

By means of the design space exploration, we exposed 3 types of GNR shapes, which are depicted in Figure 5.3 and found to be the most suitable for the construction of GNR Boolean gates construction. Further, in Section 5.4 we prove that by appropriately changing the dimensions of the GNR shapes, they deliver the necessary functionalities for constructing all the desired Boolean gates.

We observe that the GNR gates can be directly cascaded to construct networks of GNR gate to enable GNR-based circuit design, since the GNRs input

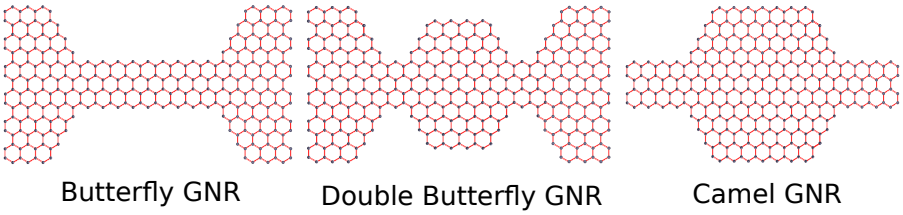

Figure 5.3: GNR Shapes for Boolean Gates.

voltages are compatible with their output voltages. Nevertheless, akin to the CMOS case, certain circuit topologies may result in signal integrity degradations, and in these situations, buffers, such as the one from Section 5.4, are necessary for restoring the logic high and logic low voltage levels.

5.3 Simulation Setup

In this section, we describe the formalism for deriving the electrical properties of GNRs and present the SPICE simulation setup of proposed GNR-based Boolean gates.

5.3.1 GNR Conduction Computation

To derive GNR conduction under certain bias condition we model graphene electronic ballistic transport by means of the Non-Equilibrium Green's Function (NEGF)-Landauer formalism as shown in Section 2.2. The GNR channel is described by a Hamiltonian matrix $H = H_0 + U$, which models the interactions between neighbor carbon atoms (via H_0), and incorporates all the external as well as the internal potentials (e.g., top gates voltages, and back gate voltage) via U. H_0 is constructed by using semi-empirical (tight-binding) calculations. In our simulation we account for first nearest-neighbor (1NN) interactions, and the potential distribution matrix U is determined self-consistently as the solution of the 2D Poisson equation

$$\nabla \cdot [\epsilon(\mathbf{r})\ \nabla U(\mathbf{r})] = -\frac{\rho(\mathbf{r})}{\epsilon_0}, \tag{5.2}$$

where $\mathbf{r} = x\hat{\mathbf{x}} + y\hat{\mathbf{y}}$ is a position vector in space, ϵ_0 denotes the vacuum permittivity, $\epsilon(\mathbf{r})$ is the dielectric permittivity of the materials at position $\mathbf{r}$, and ρ represents the net charge density distribution. The Poisson equation is numerically solved by making use of the finite difference method.

5.3.2 Mixed SPICE-Simulink Simulation

In order to validate the correct operation and evaluate the proposed GNR-based Boolean gates, we utilize SPICE simulation in Cadence [119]. The GNR of each gate is modeled using a Verilog-A model which has 5 pins (out of which 2 inout pins: source and drain, and 3 input pins: 2 top gates and 1 back gate) [139]. In order to permit multiple GNR shapes and gate topologies, we developed a parametric Verilog-A model which is able to take into account: the nanoribbon length L and width W, the constriction length L_c and width W_c, the extrusion top length L_b and width W_b, the position of the top gate contacts relative to the source/drain contacts $P_{V_{g1,2}}$, and the top gate contact widths $W_{V_{g1,2}}$, as defined in Figure 3.1. The Verilog-A model triggers internally a Simulink model which computes the GNR conductance as described in Section 5.3.1. In this way, we benefit of pysics level, accurate results. The inter-communication between Simulink [137] and Cadence is illustrated schematically in Figure 4.2. Based on the GNR geometry (described using the 10 parameters), at the initial time step $t = 0$, Simulink computes the Hamiltonian matrix H, the source and drain contacts self-energy, Σ_1 and Σ_2, and their energy broadening factors, Γ_1 and Γ_2. Then, for every remaining transient simulation time step, Simulink receives from Cadence 5 inputs (V_d, V_s, V_{g1}, V_{g2}, and V_b voltages), and based on the matrices computed during the initial time step $t = 0$, it derives the afferent GNR conductance G and then passes this value back to Cadence. Once the conductance value is known to the Verilog-A model, the current through the GNR is updated via the relation: $I(d, s) = V(d, s) \cdot G$.

5.3.3 GNR Gates Simulation

Individual GNR gates are simulated in Cadence using a generic setup which is illustrated in Figure 4.5 in Section 4.3 for 2-input gates with the back gate voltage set to 0 V. For each gate, there are two GNRs which are connected in series. We employ 0 V as logic low voltage level, and 0.2 V as logic high voltage level. For 1-input gates, i.e., inverter and buffer, the $g2$ pin is absent, while for 3-input gates a third pin denoted as $g3$ is added. The gate primary input voltages are periodic pulse signals with 50 ps rise time and fall time and 50% duty cycle. The primary input signals period is set to 400 ps for 1-input gates, 400 ps and 800 ps for 2-input gates, and 400 ps, 800 ps, and 1600 ps for 3-input gates.

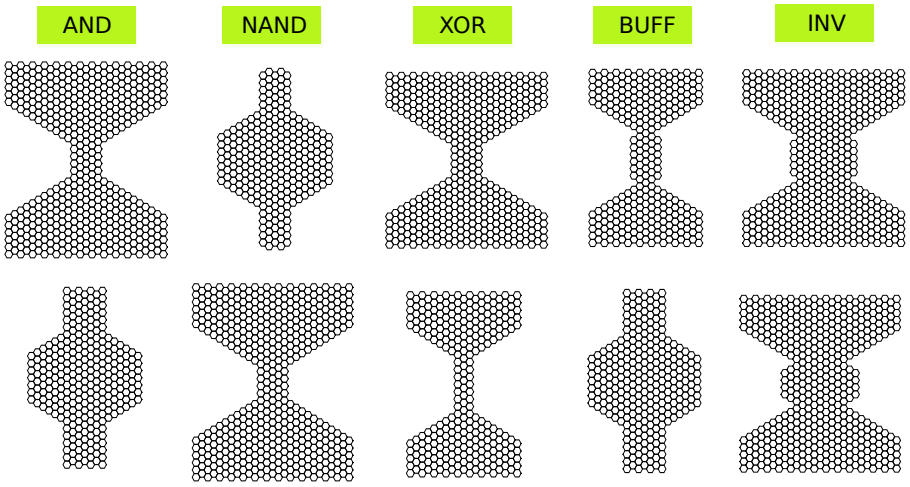

Figure 5.4: GNR_{up} (top row) and GNR_{dn} (bottom row).

5.4 GNR Boolean Gates

In this section we propose and investigate the performance of 1-, 2-, and 3-input GNR basic Boolean gates.

5.4.1 1- and 2-input GNR Gates

We present in the following for every proposed GNR gate, its topology, and we validate in SPICE the gates correct operation. Further we evaluate them with respect to propagation delay, area, and power consumption, against 7 nm FinFET CMOS counterparts.

Figure 5.4 graphically illustrates the GNR shapes utilized in the proposed 1- and 2-input gates. We observe that, intuitively speaking, GNR_{up} and GNR_{dn} can be interchanged as part of two gates which perform inverse Boolean functions, i.e., we can use the same 2 GNRs for both AND gate and NAND gate per se. Nevertheless, as the pull-up GNR is connected to V_{DD} and V_{out}, when connecting it as pull-down GNR to V_{out} and V_{SS} for the inverse gate, its conductance map might deviate from expected behaviour (might not properly mirror the same Boolean function). Therefore, for gates which perform complementary functions, it is necessary to use different GNRs even if they execute the same Boolean function. The geometry and contacts topology of the proposed GNR gates, which are optimized for an operating voltage of 0.2 V, are sum-

Table 5.1: Complementary Boolean Gate GNR Dimensions.

		(W, L)	(W_c, L_c)	(W_b, L_b)	(P_{V_g}, W_{V_g})
AND	GNR_{up}	$(41, 27\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(2\sqrt{3}, 6\sqrt{3})$
	GNR_{dn}	$(29, 25\sqrt{3})$	$(0, 0)$	$(9, 7\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$
NAND	GNR_{up}	$(29, 25\sqrt{3})$	$(0, 0)$	$(11, 7\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(2\sqrt{3}, 6\sqrt{3})$
XOR	GNR_{up}	$(41, 25\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(1\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(29, 25\sqrt{3})$	$(5, 7\sqrt{3})$	$(0, 0)$	$(6\sqrt{3}, 3\sqrt{3})$
BUFF	GNR_{up}	$(29, 25\sqrt{3})$	$(5, 7\sqrt{3})$	$(2, 6\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(29, 25\sqrt{3})$	$(0, 0)$	$(9, 7\sqrt{3})$	$(0, 6\sqrt{3})$
INV	GNR_{up}	$(41, 25\sqrt{3})$	$(14, 6\sqrt{3})$	$(2, 5\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 25\sqrt{3})$	$(14, 6\sqrt{3})$	$(3, 4\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$

marized in Table 5.1. We note that all dimensions in the table are expressed in terms of $a = 0.142\,\mathrm{nm}$, the distance between adjacent carbon atoms, which holds true for all the other reporting GNR geometries tables included in the chapter. GNR gate designs which operate on other power supply voltage values (e.g., varying from mV to V) are feasible and lead to varying delay-power-area tradeoffs, but they require identifying GNR topologies which are capable of delivering the intended functionality under the new biasing setup. In general, the delay and robustness requirements constrain the power supply voltage, but our choice for $0.2\,\mathrm{V}$ is motivated primarily by the fact that we wanted to probe the delay and power potential of graphene logic while maintaining the GNR dimensions within a feasible range.

The GNRs of all gates have similar total width and length, but they have different extrusion and constriction dimensions. The extrusion and constriction width impact on the conductance is big, which is not true for the influence of their length dimension. Therefore, as it can be inferred from Table 5.1, the extrusion and constriction width parameters can vary significantly among GNRs which correspond to different Boolean functions. Also, it can be observed that the top gates contacts are situated closer to the source/drain contacts for the GNRs which map {AND, XOR, BUFF} Boolean operations, and further for {NAND, INV}. The width of the top gate contacts remains the same for all GNRs with 2 exceptions - the GNRs which map {AND, INV}.

For illustrating the complementary operation of proposed GNR-based Boolean

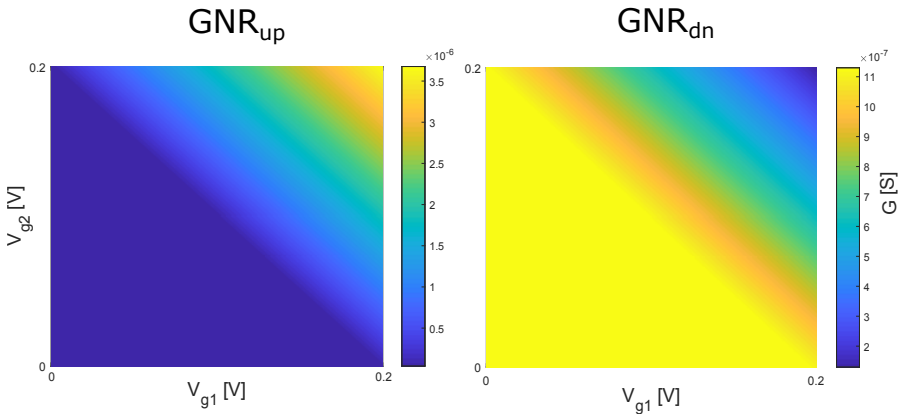

Figure 5.5: AND Gate GNR Conductance Maps.

gates, we consider the AND gate, and present the 2 conductance maps in Figure 5.5 which correspond to the gate pull-up and pull-down GNRs. As we can notice, the 4 corner conductance points are mirroring the logical AND functionality for GNR_{up}, and the inverted function (NAND) for GNR_{dn}. The 2 density plots are also pointing out the proposed gate robustness to voltage variations of the gate input. For example, $\approx 5\%$ variation of the input voltages results in $\approx 4.9\%$ and $\approx 4.4\%$ variation of GNR_{up} and GNR_{dn} conductance, respectively.

Figure 5.6 shows the {INV, BUFF, AND, NAND, XOR} GNR gates input voltages and their response. We observe that all gates exhibit correct operation in line with the corresponding Boolean function. The presence of small spikes can be observed on the output voltage evolution. We attribute these spurious transients on one hand to the feedback currents of the input voltage sources, and on the other hand to non-linearities which are present in the dependence of the GNR conductance on the voltages to which the GNR is subjected.

Table 5.2 summarizes the input to output propagation delay, the active area requirements, and the power consumption for the proposed gates and for 7 nm FinFET CMOS [138] (V_{DD} =0.7 V) counterparts. For a fair area-wise comparison, we only consider the conduction channels area of the encompassed devices, instead of the total standard cell footprint (which is not available for GNR gates). As far as the power is concerned, we measure in SPICE the total power for all 4 clock cycles. The tabulated results show a propagation delay reduction for the GNR gates, relative to the CMOS counterparts, which varies from 23% for the XOR gate, up to 6× for the AND gate, and 2 orders of

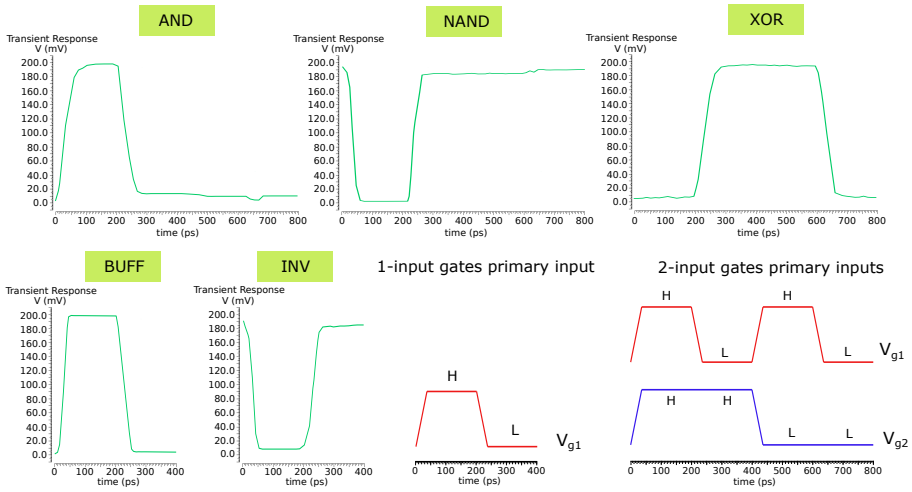

Figure 5.6: GNR Gate SPICE Simulation Results.

Table 5.2: 1- and 2-input Gates Delay, Area, and Power.

	$\tau_p[ps]$		Active Area $[nm^2]$		Total Power $[nW]$	
	GNR	CMOS	GNR	CMOS	GNR	CMOS
AND	1.38	9.618	$4.272 \cdot 10^1$	$1.452 \cdot 10^3$	4.628	$5.886 \cdot 10^2$
NAND	2.15	7.556	$4.146 \cdot 10^1$	$9.680 \cdot 10^2$	2.370	$5.415 \cdot 10^2$
XOR	7.48	9.168	$4.038 \cdot 10^1$	$2.420 \cdot 10^3$	1.734	$5.923 \cdot 10^2$
BUFF	0.42	2.040	$3.283 \cdot 10^1$	$9.680 \cdot 10^2$	0.937	$4.704 \cdot 10^2$
INV	0.27	1.110	$5.431 \cdot 10^1$	$4.840 \cdot 10^2$	0.947	$4.621 \cdot 10^2$

magnitude lower power consumption in all cases. Moreover, the GNR gates necessitate 1 to 2 orders of magnitude smaller active area footprint than the most advanced CMOS technology node [140] counterparts.

While for the {AND, NAND, XOR} CMOS gates, the propagation delay and power figures are similar, we observe that this is not the case for the GNR gates. For instance, the GNR AND delay is $4.4\times$ smaller than the GNR XOR gate delay. However, the GNR AND power consumption is $1.6\times$ higher than that of the one of the GNR XOR. This is a direct consequence of our design choice towards a fast AND gate at the expense of increased power consumption. However, when designing the GNR gates one may opt for other trade-offs.

In Table 5.2 it can be noticed that the active area of different CMOS gates can vary by up to $4\times$, while in the case of the GNR gates the variation resides within 65%. Therefore, we can arrive at the conclusion that while, generally speaking, complex Boolean logic translates into a larger CMOS circuit area realization, this is not the case for GNR, where a complex Boolean functionality can be achieved with very little area implications. For example, if we consider the XOR gate relative to the NAND gate, the occupied area for the CMOS case increases by $1.5\times$, while the area is similar (2.7% reduction) for the GNR case.

5.4.2 3-input GNR Gates

As higher than 2 gate fan-in might be of interest in practical implementations, in this section, we seek GNR topologies appropriate for the implementation of 3-input gates, namely $\{\text{AND3}, \text{NAND3}, \text{OR3}, \text{NOR3}\}$ and investigate the characteristics of the obtained GNR gates. Note that besides those we also propose 3-input XOR and MAJORITY gates but we discuss them in the more relevant context of the Full Adder implementation presented in Section 5.5.1.

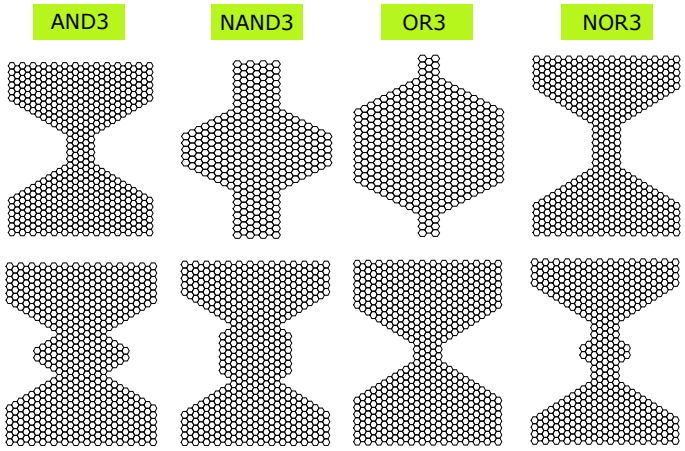

Figure 5.7: 3-input Gate GNR Shapes.

The identified GNR gates dimensions and shapes are presented in Table 5.3 and Figure 5.7, respectively. For the 3-input gates, P_{Vg} defines the position of the first and third top gates with respect to the drain and source contacts, respectively. The second top gate is situated in the middle in-between the other two top gates. We note that for all the gates introduced in Section 5.4.1, topologies able to operate under the same $0\,\text{V}$ back gate voltage bias have been sought.

To implement 3-input gates, we extended the Design Space Exploration (DSE) by letting the back gate voltage also vary as other back gate voltage values can facilitate a more appropriate top gate control on the conductance, and induce a higher ON/OFF current ratio by modulating the Fermi energy level at the Dirac point. The applied back gate voltages for each identified GNR topology are presented in Table 5.4.

As a result of this DSE extension we are also able to identify 1- and 2-input gate designs with slightly better performance than the ones proposed in Section 5.4.1, which is the case for the XOR and INV gates (with geometries presented in Table 5.7 and Table 5.10, respectively) that we employ for the Full Adder and SRAM cell designs in Section 5.5. Table 5.6 reflects the due to non-zero back bias ($V_b = 0$ DSE ($\_v1$) vs $V_b \neq 0$ extended DSE ($\_v2$)) performance improvement for these 2 gates and indicates $7\times$ and 11% delay reduction, 19% and 23% lower power consumption, for the XOR and INV gate, respectively, while requiring roughly the same active area. We note that the 1- and 2-input gates proposed in Section 5.4.1 were optimized for low power thus by setting a high performance focus for the design space exploration, we can potentially obtain GNR topologies that reduce the gate delay by at least one order of magnitude.

Table 5.3: 3-input GNR Gate Dimensions.

		(W, L)	(W_c, L_c)	(W_b, L_b)	(P_{V_g}, W_{V_g})
AND3	GNR_{up}	$(41, 27\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(5\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(14, 6\sqrt{3})$	$(5, 2\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$
NAND3	GNR_{up}	$(35, 27\sqrt{3})$	$(0, 0)$	$(11, 5\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(2, 6\sqrt{3})$	$(5\sqrt{3}, 3\sqrt{3})$
OR3	GNR_{up}	$(35, 27\sqrt{3})$	$(0, 0)$	$(14, 11\sqrt{3})$	$(5\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(2, 2\sqrt{3})$	$(0, 0)$	$(3\sqrt{3}, 3\sqrt{3})$
NOR3	GNR_{up}	$(41, 27\sqrt{3})$	$(8, 6\sqrt{3})$	$(0, 0)$	$(5\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(2, 2\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$

All dimensions are expressed in terms of $a = 0.142\,\mathrm{nm}$, the distance between adjacent carbon atoms.

We performed SPICE simulation and validated the 3-input gates correct functionality as indicated by the plots in Figure 5.8.

Table 5.5 summarizes the delay, area, and power consumption for 3-input GNR

Table 5.4: 3-input GNR Back Gate Bias.

	V_b $[V]$			
	AND3	NAND3	OR3	NOR3
GNR_{up}	0	-0.4	0.2	-0.4
GNR_{dn}	-0.1	0	-0.1	0

Table 5.5: 3-input GNR Gates Propagation Delay, Area, and Power vs $7\,\text{nm}$ FinFET CMOS.

	$\tau_p[ps]$		Active Area $[nm^2]$	
	GNR	CMOS	GNR	CMOS
AND3	2.538	$1.116 \cdot 10^1$	$5.665 \cdot 10^1$	$1.936 \cdot 10^3$
NAND3	3.195	7.635	$4.387 \cdot 10^1$	$1.452 \cdot 10^3$
OR3	2.273	8.547	$5.092 \cdot 10^1$	$1.936 \cdot 10^3$
NOR3	2.132	$1.092 \cdot 10^1$	$4.771 \cdot 10^1$	$1.452 \cdot 10^3$
XOR3	1.583	$1.373 \cdot 10^1$	$5.179 \cdot 10^1$	$4.840 \cdot 10^3$
MAJ3	0.109	$1.099 \cdot 10^1$	$5.078 \cdot 10^1$	$2.180 \cdot 10^4$
	Power $[nW]$		Power-Delay Product $[ps\text{-}nW]$	
	GNR	CMOS	GNR	CMOS
AND3	6.234	$2.326 \cdot 10^2$	15.82	$4.461 \cdot 10^3$
NAND3	2.777	$8.701 \cdot 10^2$	8.871	$2.621 \cdot 10^3$
OR3	0.836	$6.472 \cdot 10^2$	1.900	$2.968 \cdot 10^3$
NOR3	1.035	$9.868 \cdot 10^2$	2.207	$3.257 \cdot 10^3$
XOR3	1.654	$1.768 \cdot 10^3$	2.618	$2.427 \cdot 10^4$
MAJ3	3.388	$3.482 \cdot 10^3$	0.371	$3.826 \cdot 10^4$

gates (we also included the MAJORITY gate MAJ3 introduced in Section 5.5 for sake of completeness) and CMOS counterparts. We observe that the 3-input

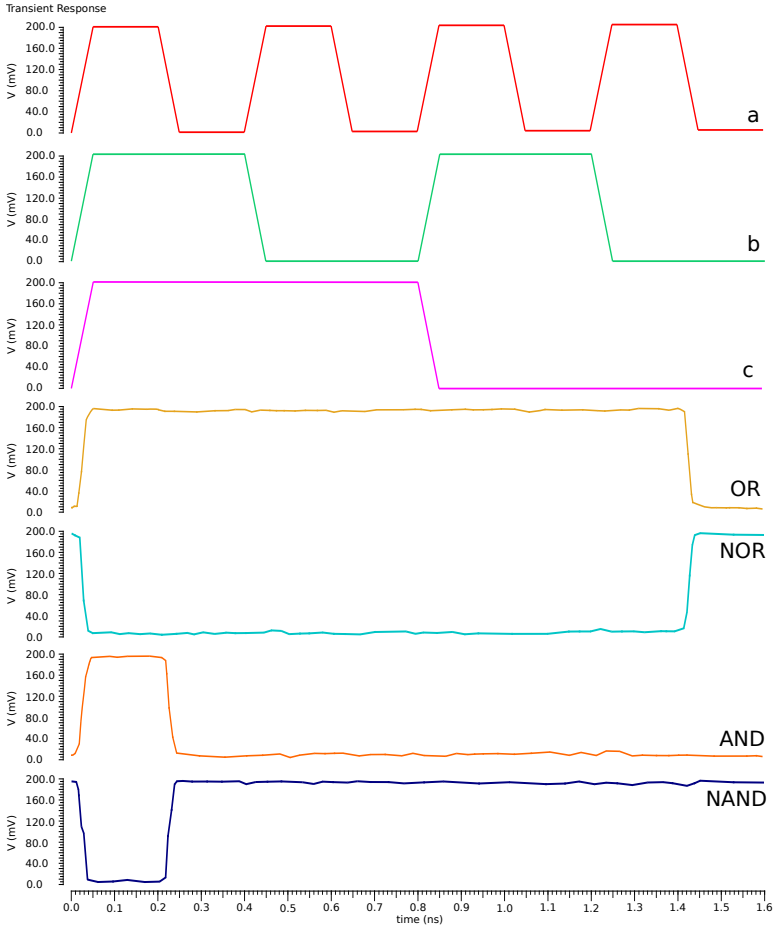

Figure 5.8: 3-input Gate SPICE Simulation Results.

Table 5.6: Extended DSE Delay, Area, and Power.

	$\tau_p[ps]$		Active Area $[nm^2]$		Total Power $[nW]$	
	GNR_$v1$	GNR_$v2$	GNR_$v1$	GNR_$v2$	GNR_$v1$	GNR_$v2$
XOR	7.48	0.96	40.38	51.51	1.73	1.40
INV	0.27	0.24	54.31	45.23	0.95	0.73

GNR gates provide propagation delay, power consumption, and power-delay product reductions of $2\times$ and 2 orders of magnitude, 2 and 3 orders of magnitude, and 2 and 5 orders of magnitude, respectively, for NAND3 and MAJ3,

respectively, while requiring about 1 to 2 orders of magnitude smaller active area. We observe that both 2-input and 3-input GNR gates occupy roughly the same area. This implies that we can increase the gate fan-in and the gate functional complexity with little to no impact on the active area footprint. The same cannot be said about CMOS where the area generally increases with the gate complexity increase. Also, the fact that we can implement a 3-input MAJORITY gate with 2 GNRs is quite significant and has positive implications on other implementations, e.g., Error Correcting Codes (ECC) codecs, LDPC [141], [142], [143], [144], which performance heavily depends on the effectiveness of the utilized MAJORITY gate implementations.

All these results suggest that, potentially speaking, GNR-based logic gates can substantially outperform advanced CMOS counterparts and can open a novel avenue towards future post-Si nanoelectronics. To get a glimpse on the possible implications of our proposal on potential carbon based computing platform performance we propose in the next section GNR based implementations of two fundamental computing and storage circuit elements.

5.5 Basic GNR Circuits

In this Section, we make use of proposed GNR gates to design the most frequently utilised computation and storage elements, i.e., the Full Adder and the SRAM cell.

5.5.1 1-bit Full Adder

As adders are the most ubiquitous basic building blocks of any computing system, we consider a 1-bit Full Adder, with 3 1-bit inputs (a, b, Carry-In), and 2 1-bit outputs (Sum, Carry-Out) and evaluate and compare different GNR and 7 nm FinFET CMOS implementations. For the CMOS case we use the optimized 28 transistors standard cell. For the GNR case, as illustrated in Figure 5.9, we make use of a single 3-input MAJORITY gate, realised with 2 GNRs only, for computing the Carry-Out output since it is faster, smaller, and consumes less power than any counterpart designs relying on multiple 2-input gates (e.g., 6 NAND gates). As an adder critical path typically resides in the carry propagation path, and since for GNR-based implementations 2-input gates and 3-input gates may yield similar performance, we consider two designs for computing the Sum output (i.e., using 2 2-input XOR gates and using 1 3-input XOR gate).

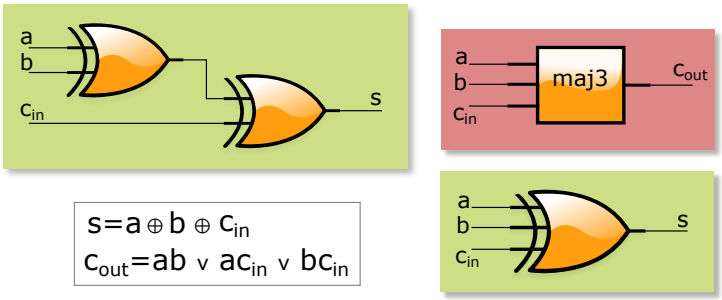

Figure 5.9: 1-bit Full Adder.

Table 5.7: Dimensions of GNR 1-bit Full Adder Gates.

		(W, L)	(W_c, L_c)	(W_b, L_b)	(P_{V_g}, W_{V_g})
XOR	GNR_{up}	$(41, 27\sqrt{3})$	$(14, 6\sqrt{3})$	$(2, 2\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(2, 2\sqrt{3})$	$(7\sqrt{3}, 3\sqrt{3})$
XOR3	GNR_{up}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(8, 2\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(2, 2\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$
MAJ3	GNR_{up}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(2, 4\sqrt{3})$	$(5\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(2, 2\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$

Table 5.8: FA Gates GNR Back Gate Bias.

	XOR		XOR3		MAJ3	
	GNR_{up}	GNR_{dn}	GNR_{up}	GNR_{dn}	GNR_{up}	GNR_{dn}
V_b [V]	0	-0.1	0.1	0	0	-0.1

We summarize in Table 5.7 the topology and dimensions of the GNR gates relevant for the Full Adder implementation and graphically illustrate in Figure 5.10 the employed GNR shapes. The back gate voltages applied to the adder gates comprising GNRs are included in Table 5.8.

Figure 5.11 presents SPICE simulation results for the GNR based Full Adder implementation and one can observe that the Sum and Carry-Out outputs exhibit the correct functionality. When using a single 3-input GNR XOR gate for computing the Sum, we obtain a delay of 2.878 ps, while when using 2 cascaded 2-input GNR XOR gates, we measure a delay of 1.910 ps. Thus, we opted for the latter logic implementation of the Full Adder Sum output

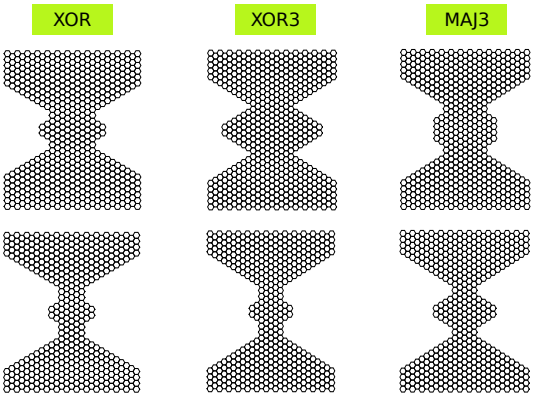

Figure 5.10: FA GNR_{up} (top row) and GNR_{dn} (bottom row).

Table 5.9: FA Delay, Area and Power Consumption.

	$\tau_p[ps]$		Active Area $[nm^2]$		Total Power $[nW]$	
	GNR	CMOS	GNR	CMOS	GNR	CMOS
FA	1.910	11.863	$1.538 \cdot 10^2$	$3.004 \cdot 10^4$	6.188	$7.915 \cdot 10^3$

bit. The Carry-Out delay is determined by the 3-input GNR MAJORITY gate with a measured value of $0.109\,\mathrm{ps}$. Table 5.9 summarizes the propagation delay, area, and power consumption measured figures for the 1-bit GNR-based and CMOS-based Full Adders, and indicate that the GNR FA has $6.2\times$ smaller delay, requires 2 orders of magnitude smaller area, and consumes 3 orders of magnitude less power than the CMOS counterpart. We note however that for implementations of Ripple Carry Adders (RCA), which are the quite common, the Carry-Out delay is the one determining the overall adder performance. Thus, as the Carry-Out delay is $0.109\,\mathrm{ps}$ and $11.863\,\mathrm{ps}$, for the GNR and CMOS FA, respectively, an n-bit GNR RCA will be $108\times$ faster than the CMOS counterpart.

5.5.2 SRAM Cell

Further, we consider an SRAM cell, illustrated in Figure 5.12, which is widely utilized for data storage, and investigate its performance when designed using GNRs relative to the 6T $7\,\mathrm{nm}$ FinFET CMOS counterpart. The dimensions and shapes of the two left/right access GNRs and of the GNRs belonging to

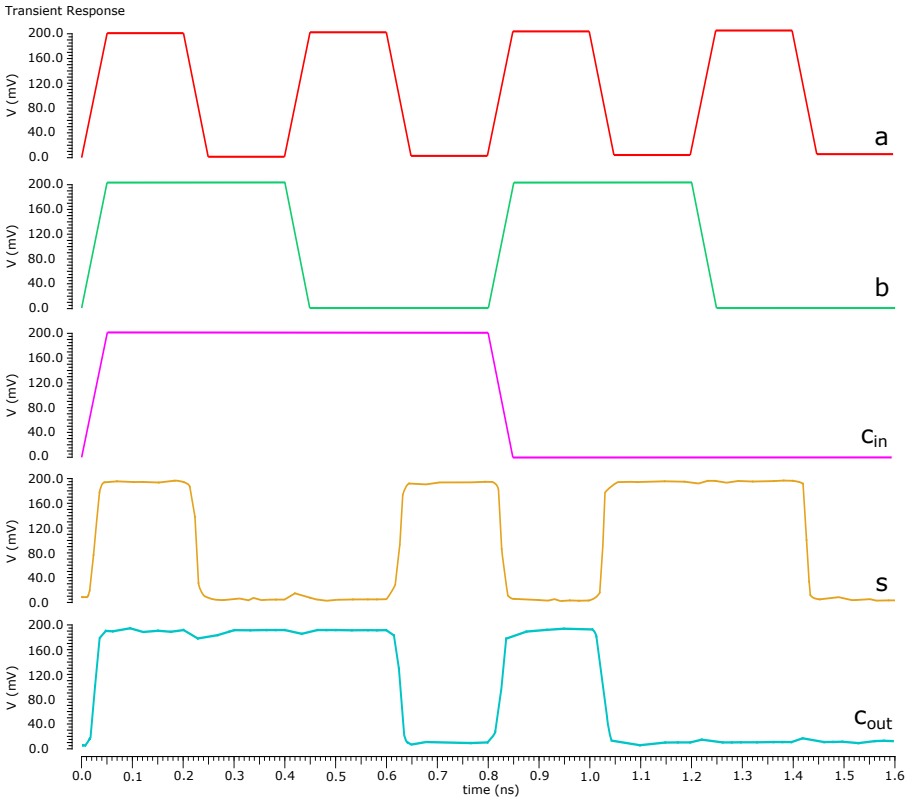

Figure 5.11: GNR FA SPICE Simulation Results.

the inverter gate are presented in Table 5.10 and Figure 5.13, respectively. As back gate voltages, we use -0.1 V and 0 V for the inverter GNR_{up} and GNR_{dn}, respectively, and 0 V for the left/right access GNR.

We analyze cell robustness to variability during the information retention state for both CMOS and GNR configurations, which is characterized by the Static Noise Margin (SNM) defined as the minimum amount of DC noise required in order to flip the SRAM cell state. The SNM value is given by the side of the biggest square embeddedable between the two DC characteristics of the cross-coupled inverters, illustrated in Figure 5.14 and Figure 5.15 for CMOS and GNR cells, respectively. Simulation results indicate an SNM value of 0.25 V ($\approx 35.7\%$ from V_{DD} =0.7 V) for the 7 nm FinFET CMOS configuration and of 0.072 V ($\approx 36\%$ from V_{DD} =0.2 V) for the GNR counterpart, thus we can conclude that the two memory cells exhibit similar DC noise voltage tolerance. Performance-wise, as presented in Table 5.11, the GNR SRAM cell

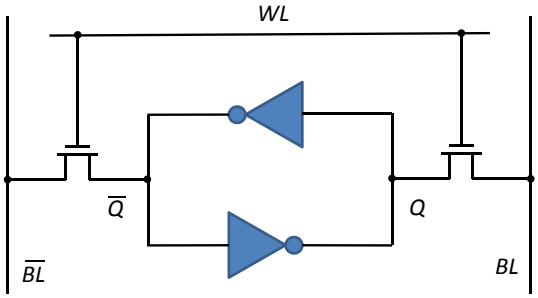

Figure 5.12: SRAM Cell.

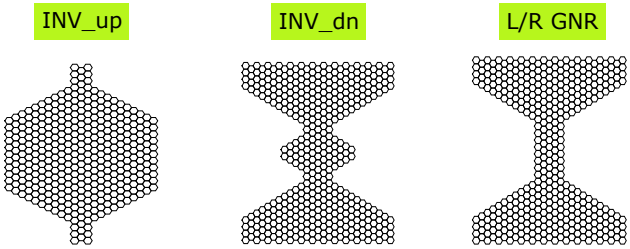

Figure 5.13: SRAM Cell GNR Topologies.

provides $3.6\times$ smaller delay, consumes 2 orders of magnitude smaller power, and requires 1 order of magnitude less active area than the CMOS SRAM cell. We conclude, based on the simulation results presented in Section 5.5.1 and Section 5.5.2, that GNR-based implementations can potentially outperform CMOS counterparts and that the proposed approach is opening a promising avenue towards future carbon-based nanoelectronics.

5.6 Conclusion

In this chapter, we proposed $1-$, 2-, and 3-input GNR Boolean gates and investigated their potential as building structures for post-CMOS circuits. For this purpose, we introduced a generic GNR Boolean gate which is constructed using two GNRs arranged in a complementary manner (one GNR executes the gate Boolean function, and the other GNR executes the inverted Boolean function). Then, we identified a set of suitable GNR geometries and gate topologies, while taking into account the gate output switching behaviour, and presented 1-input $\{$BUFF, INV$\}$, 2-input $\{$AND, NAND, XOR$\}$, and 3-input

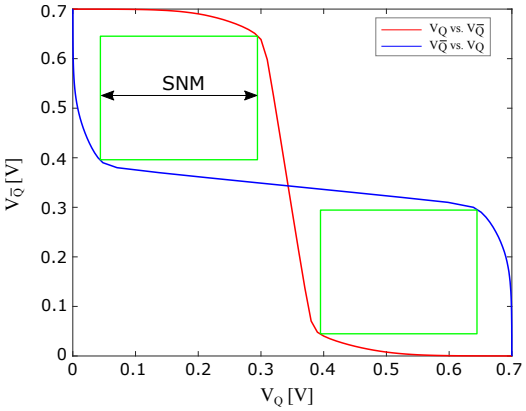

Figure 5.14: 6T SRAM SNM Diagram.

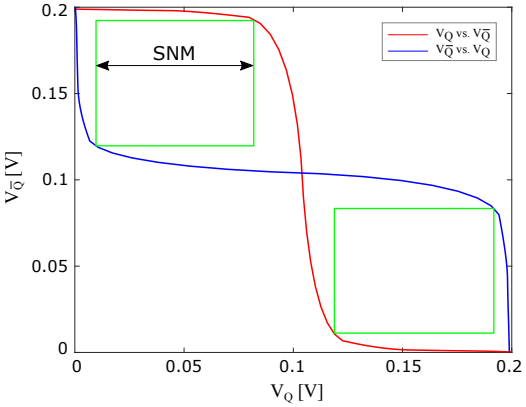

Figure 5.15: GNR SRAM SNM Diagram.

{AND, NAND, XOR, MAJORITY} gate designs. We validated the correct operation and evaluated the proposed gates in Cadence. We modelled the GNR conductance using a Verilog-A model which relies on the NEGF-Landauer formalism via an internally triggered Simulink model. Simulation results indicated that, when compared against 7 nm FinFET CMOS counterparts, the proposed gates exhibit $6\times$ to 2 orders of magnitude smaller propagation delay, 2 to 3 orders of magnitude lower power consumption, and require 2 orders of magnitude less active area footprint. We further presented Full Adder (FA) and SRAM cell GNR designs, as they are currently fundamental components for the construction of any computation system. For an effective FA implementation we introduced a 3-input MAJORITY gate, which apart of being able to

Table 5.10: GNR SRAM Component Dimensions.

		(W, L)	(W_c, L_c)	(W_b, L_b)	(P_{V_g}, W_{V_g})
INV	GNR_{up}	$(35, 27\sqrt{3})$	$(0, 0)$	$(14, 11\sqrt{3})$	$(5\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(5, 2\sqrt{3})$	$(5\sqrt{3}, 3\sqrt{3})$
	$GNR_{L/R}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(5\sqrt{3}, 3\sqrt{3})$

Table 5.11: SRAM Delay, Area and Power Consumption.

	$\tau_p[ps]$		Active Area $[nm^2]$		Total Power $[nW]$	
	GNR	CMOS	GNR	CMOS	GNR	CMOS
SRAM	0.763	2.729	$6.776 \cdot 10^1$	$9.68 \cdot 10^2$	4.429	$2.622 \cdot 10^2$

directly compute FA's Carry-Out, is an essential element in the implementation of Error Correcting Codes (ECC) decoders, that outperforms the CMOS equivalent Carry-Out calculation circuit by 2 and 3 orders of magnitude in terms of delay and power consumption, respectively, while requiring 2 orders of magnitude less area. The proposed GNR FA exhibits $6.2\times$ smaller delay, 3 orders of magnitude less power consumption, while requiring 2 orders of magnitude less area, when compared with the $7\,\mathrm{nm}$ FinFET CMOS counterpart, and that a GNR-based n-bit Ripple Carry Adder is potentially $108\times$ faster than an equivalent CMOS implementation. The GNR based SRAM cell provides a slightly better resilience to DC noise characteristics, while performance-wise has a $3.6\times$ smaller delay, consumes 2 orders of magnitude less power, and requires 1 order of magnitude less area than the CMOS equivalent. Our investigations clearly suggest that GNR-based implementations can potentially outperform CMOS counterparts and that the proposed approach is opening a promising avenue towards future carbon-based nanoelectronics.

Note. The content of this chapter is based on the following papers:

Y. Jiang, N. Cucu Laurenciu, H. Wang, and S.D. Cotofana, **Graphene Nanoribbon Based Complementary Logic Gates and Circuits**, *IEEE Transactions on Nanotechnology (TNANO)*, vol. 18, p. 287-298, 2019.

Y. Jiang, N. Cucu Laurenciu, and S.D. Cotofana, **Complementary Arranged Graphene Nanoribbon-Based Boolean Gates**, *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 1-7, 2018.

6

GNR Gates Performance Robustness under Temperature Variations

As CMOS scaling is reaching its limits, high power density and leakage, low reliability, and increasing IC production costs are prompting for developing new materials, devices, architectures, and computation paradigms. Additionally, temperature variations have a significant impact on devices and circuits reliability and performance. Graphene's remarkable properties make it a promising post Silicon front-runner for carbon-based nanoelectronics. While for CMOS gates temperature effects have been largely investigated, for gates implemented with atomic-level Graphene Nanoribbons (GNRs), such effects have not been explored. This chapter presents the results of such an analysis performed on a set of GNR-based Boolean gates by varying the operation temperature within the military range, i.e., $-55°C$ to $125°C$, and evaluating by means of SPICE simulations gate output signal integrity, propagation delay, and power consumption. Our simulation results reveal that GNR-based gates are robust with respect to temperature variation, e.g., 5.2% and 5.3% maximum variations of NAND output logic "1" (V_{OH}) and logic "0" (V_{OL}) voltage levels, respectively. Moreover, even in the worst condition GNR-based gates outperform CMOS FinFET 7nm counterparts, e.g., $1.6\times$ smaller delay and $185\times$ less power consumption for the INV case, which is strengthening their great potential as basic building blocks for future reliable, low-power, nanoscale carbon-based electronics.

6.1 Introduction

Due to its excellent properties, graphene has been used for transistor-based logic, which follows the traditional CMOS design style, e.g., in [91, 145],

while alternative approaches towards gate realizations departing from the switch-based mainstream have been introduced in, e.g., [146, 147].

As CMOS dimensions are down-scaling to sub-$10\,\mathrm{nm}$ range, temperature variations have a significant impact on device and circuits reliability and performance [93]. While for CMOS gates temperature effects have been largely investigated [94], for gates implemented with atomic-level Graphene Nanoribbon (GNR), such effects have not been explored. In this chapter, we present the results of such an analysis performed on a set of 1- and 2-input GNR-based Boolean gates, i.e., {INV, BUF, AND2, NAND2, OR2, NOR2, XOR2} . We vary the operation temperature within the military range, i.e., $-55°C$ to $125°C$, and evaluate by means of SPICE simulations gate's output signal integrity, propagation delay, and power consumption. The obtained results suggest that the GNR-based gates are robust with respect to temperature variation, e.g., 5.2% and 5.3% maximum variations for NAND for logic "1" (V_{OH}) and logic "0" (V_{OL}) output voltage level, respectively. Additionally, even in the worst case condition they outperform CMOS FinFET 7nm counterparts, e.g., $1.6\times$ smaler delay and $185\times$ less power consumption for the INV case, suggesting that the GNR-based gates have great potential as basic building blocks for future reliable, low-power, carbon-based nanoelectronics.

The remaining of this chapter is structured as follows: Section 6.2 entails an overview of the simulation framework. Section 6.3 presents the simulation results and comments on the gates robustness with respect to temperature variation. Finally, some concluding remarks are given in Section 6.4.

6.2 Simulation Framework

In this section, we present a phonon limited GNR transport computation model based on Non-Equilibrium Green's Function (NEGF) approach which takes into account electron-phonon interaction, for deriving GNR's electrical properties (e.g., current and conductance). Further, we describe the GNR-based complementary Boolean gates SPICE simulation under temperature variations.

6.2.1 Phonon Limited GNR Transport Computation Model

In order to model the electronic carrier transport, we make use of the NEGF-Landauer formalism, where NEGF calculations describe the electron-electron interaction and the Landauer formula gives the GNR current and conductance [110]. To account for the temperature-induced phenomena, i.e., electron-

phonon interactions for both optical and acoustic phonons, we extended the NEGF-Landauer simulation framework with the self-consistent Born approximation [148].

The evaluated gates are constructed from basic structures as the one depicted in Figure 2.5 in Section 2.3, which includes a trapezoidal graphene Quantum Point Contact (QPC) with zigzag edges carved into a butterfly GNR shape in order to meet the desired gate functionality [1]. This GNR is utilized as conduction channel between the source and drain contacts, which are biased by a potential $V_d - V_s$. Top gates (V_{g1}, V_{g2}) and one back gate (V_{bg}) are utilized to modulate the GNR device conductance and current.

The simulation flow Depicted in Figure 6.1 consists of 4 steps, as follows.

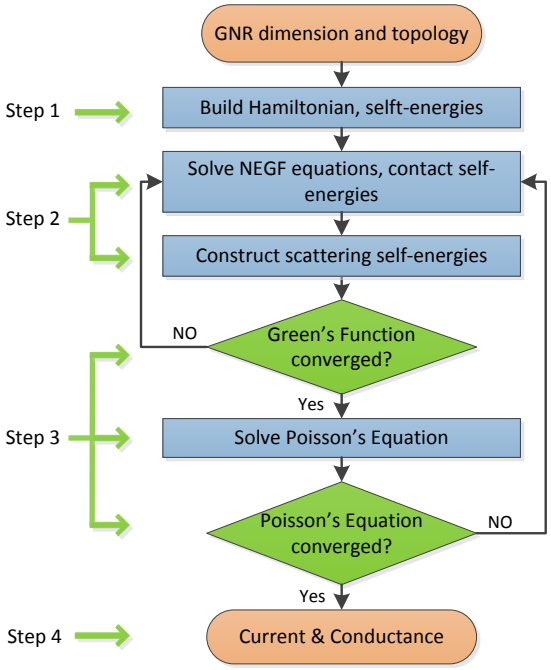

Figure 6.1: GNR Simulation Flow based on NEGF-Landauer Formalism with Phonon Scattering.

In **Step 1**, we use semi-empirical Tight Binding (TB) computations to construct the GNR Hamiltonian matrix H with respect to GNR's dimension and gate contact topology, which incorporates all internal and external potentials such as top gate voltages and back gate voltage, and the H is constructed as shown in Equation 2.1 in Section 2.2.

The drain and source contacts are applied on GNR's end sides with different electrochemical potentials, and the drain and source contact-channel interactions are modelled by the contact self-energy functions Σ_D and Σ_S, respectively.

In **Step 2**, after deriving H, Σ_D, and Σ_S, we proceed to solve NEGF equations in order to obtain the electrical properties. The most important equations to be solved are the energy dependent retarded Green's function (G^r) and the electron and hole correlation functions (G^n and G^p), [110], denoted as:

$$G^r(E) = [(E + i\eta^+)I - H - \Sigma_S - \Sigma_D - \Sigma_{el-ph}]^{-1}, \tag{6.1}$$

$$G^n(E) = G^r * (\Sigma_S^{in} + \Sigma_D^{in} + \Sigma_{el-ph}^{in}) * G^a, \tag{6.2}$$

$$G^p(E) = G^r * (\Sigma_S^{out} + \Sigma_D^{out} + \Sigma_{el-ph}^{out}) * G^a, \tag{6.3}$$

where I is the identity matrix, η^+ is an infinitesimal positive value, and Σ_{el-ph} denotes the scattering function, which corresponds to electron-phonon interactions. $G^a = [G^r]^\dagger$ is the advanced Green's function, Σ_{el-ph}^{in} and Σ_{el-ph}^{out} are in-scattering and out-scattering functions corresponding to electron-phonon interactions. $\Sigma_{S(D)}^{in}$ and $\Sigma_{S(D)}^{out}$ are the source (drain) lesser (in) self-energies function and advanced (out) self-energies function, respectively, computed as:

$$\Sigma_{S(D)}^{in}(E) = \Gamma_{S(D)}(E) * f_{S(D)}(E), \tag{6.4}$$

$$\Sigma_{S(D)}^{out}(E) = \Gamma_{S(D)}(E) * [1 - f_{S(D)}(E)], \tag{6.5}$$

where $f(E)$ denotes the Fermi-Dirac distribution function at temperature T and $\Gamma_{S(D)}$ the broadening function computed as:

$$\Gamma_{S(D)}(E) = i[\Sigma_{S(D)}(E) - \Sigma_{S(D)}^\dagger(E)]. \tag{6.6}$$

The electron-phonon scattering function Σ_{el-ph} incorporates all scattering mechanism self-energies related to Acoustic Phonon (AP) and Optical Phonon (OP) [148] (Σ_{el-ph}^{in} and Σ_{el-ph}^{out} are constructed in a similar way), denoted as:

$$\Sigma_{el-ph} = \Sigma_{AP} + \Sigma_{OP}, \tag{6.7}$$

where Σ_{AP} and Σ_{OP} are the AP and OP self-energies, respectively, which can be computed as:

$$\Sigma_{AP}^{in}(i, i, E) = D_{AP} * G^n(i, i, E), \tag{6.8}$$

$$\Sigma^{out}_{AP}(i,i,E) = D_{AP} * G^{p}(i,i,E), \tag{6.9}$$

$$\Sigma_{AP}(i,i,E) = D_{AP} * G(i,i,E), \tag{6.10}$$

$$\begin{aligned}\Sigma^{in}_{OP}(i,i,E) =& D_{OP} * [(n_{\omega}+1) * G^{n}(i,i,E+\hbar\omega) \\ &+ n_{\omega} * G^{n}(i,i,E-\hbar\omega)],\end{aligned} \tag{6.11}$$

$$\begin{aligned}\Sigma^{out}_{OP}(i,i,E) =& D_{OP} * [(n_{\omega}+1) * G^{p}(i,i,E+\hbar\omega) \\ &+ n_{\omega} * G^{p}(i,i,E-\hbar\omega)].\end{aligned} \tag{6.12}$$

For AP scattering and OP scattering, in this study, the two coupling constant are set as $D_{AP} = 0.01\,\mathrm{eV}^2$ and $D_{OP} = 0.07\,\mathrm{eV}^2$. The phonon energy is set as $\hbar\omega = 180\,\mathrm{meV}$. The Bose-Einstein distribution function is defined as:

$$n_{\omega} = 1/\exp\left(\frac{\hbar\omega}{K_B T} - 1\right), \tag{6.13}$$

where $\hbar$ is the reduced Planck constant and ω the mode frequency.

In order to simplify the OP scattering self-energy computations, the real part of OP scattering self-energy is neglected ([149] suggests that it has a small impact on phonon scattering) and its imaginary part is computed as:

$$\Sigma_{OP}(E) = -\frac{i}{2}\left(\Sigma^{in}_{OP}(E) + \Sigma^{out}_{OP}(E)\right). \tag{6.14}$$

In **Step 3**, after building the phonon scattering self-energies, the GNR transport computation model checks G^r change between current iteration and previous iteration. If the variation is bigger than 1%, then go back to Step 2, otherwise, the Poisson's equation is solved (by a 3D Poisson solver) to compute the graphene potential self-consistently [150], [109].

In **Step 4**, after the Poisson's solver has converged, the transmission function T(E), which models the probability of one electron being transmitted from the source contact to the drain contact, is computed as a function of energy as:

$$T(E) = \mathrm{Trace}\left[\Gamma_S(E)\; G^r(E)\; \Gamma_D(E)\; G^a(E)\right]. \tag{6.15}$$

Finally, the Landauer-Büttiker formalism is utilized to derive GNR's current and conductance as shown in Equations 2.6 and 2.8 in Section 2.2:

6.2.2 GNR Gate SPICE Simulation

To evaluate the considered GNR-based Boolean gates behavior under temperature variations, we make use of SPICE simulation in Cadence, with a simulation setup exemplified in Figure 6.2 for a graphene NAND gate. Two GNR devices are employed to construct a complementary style GNR-based Boolean gate, e.g., for a NAND gate, the GNR_{up} device captures the NAND Boolean function, while the GNR_{dn} device reflects the AND function [136]. We denote by V_{in1} and V_{in2} the gate inputs and by V_{out} the gate output. The back gate is connected to ground ($0\,V$) and V_d is set to $0.2\,V$, which means that in terms of gate output voltage $0.2\,V$ means logic "1" and $0\,V$ logic "0". Gate inputs rise and fall times are set to $10\,ps$. We vary the temperature from $-55°C$ to $125°C$, which covers commercial, industrial, and military ranges, and measure for each considered gate , i.e., INV, BUFF, AND2, NAND2, OR2, NOR2 and XOR2, output signal integrity, propagation delay, and power consumption.

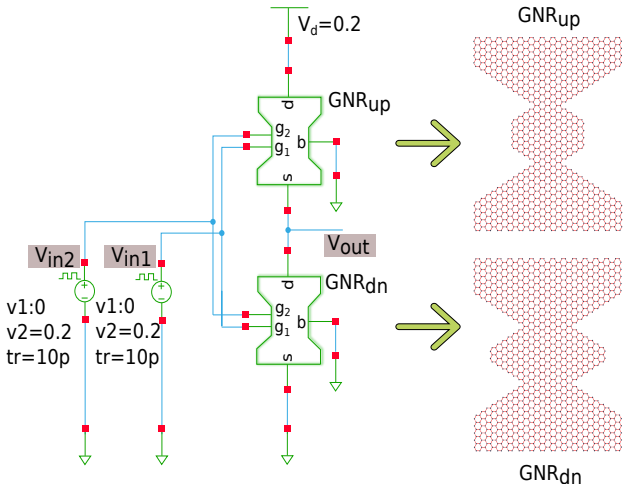

Figure 6.2: Generic GNR Gate SPICE Circuit (left) and NAND2 GNRs Dimensions (right).

6.3 Simulation Results

In this section, we present the GNR dimensions and topologies of the GNR-based gates, and evaluate their output signal integrity, propagation delay and power consumption under temperature variations by means of the proposed

SPICE simulation.

6.3.1 GNR Dimensions and Topologies of Boolean Gates

Table 6.1 summarizes the complementary Boolean gates' GNR dimensions and topologies expressed in terms of the unit value a ($0.142\,\mathrm{nm}$). The generic GNR's topology parameters in the Table 6.1 are illustrated in Figure 3.1 in Section 3.2: (i) nanoribbon geometry (i.e., width W and length L, constriction width W_{c} and length L_{c}), bump width W_{b} and length L_{b}, (ii) top gate contacts topology (i.e., contact width $W_{V_{\mathrm{g}}}$ and position relative to the drain and source contacts $P_{V_{\mathrm{g}}}$)..

Table 6.1: Complementary Boolean gate GNR dimensions and topologies.

		(W, L)	$(W_{\mathrm{c}}, L_{\mathrm{c}})$	$(W_{\mathrm{b}}, L_{\mathrm{b}})$	$(P_{V_{\mathrm{g}}}, W_{V_{\mathrm{g}}})$
INV	$\mathrm{GNR_{up}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(10\sqrt{3}, 3\sqrt{3})$
	$\mathrm{GNR_{dn}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(6\sqrt{3}, 6\sqrt{3})$
BUFF	$\mathrm{GNR_{up}}$	$(47, 25\sqrt{3})$	$(11, 4\sqrt{3})$	$(0, 0)$	$(12\sqrt{3}, 6\sqrt{3})$
	$\mathrm{GNR_{dn}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(12\sqrt{3}, 6\sqrt{3})$
AND2	$\mathrm{GNR_{up}}$	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(2, 2\sqrt{3})$	$(2\sqrt{3}, 3\sqrt{3})$
	$\mathrm{GNR_{dn}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(4\sqrt{3}, 6\sqrt{3})$
NAND2	$\mathrm{GNR_{up}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(8, 2\sqrt{3})$	$(3\sqrt{3}, 6\sqrt{3})$
	$\mathrm{GNR_{dn}}$	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(8, 2\sqrt{3})$	$(3\sqrt{3}, 6\sqrt{3})$
OR2	$\mathrm{GNR_{up}}$	$(47, 25\sqrt{3})$	$(11, 4\sqrt{3})$	$(0, 0)$	$(1\sqrt{3}, 3\sqrt{3})$
	$\mathrm{GNR_{dn}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(5, 4\sqrt{3})$	$(4\sqrt{3}, 3\sqrt{3})$
NOR2	$\mathrm{GNR_{up}}$	$(41, 27\sqrt{3})$	$(14, 6\sqrt{3})$	$(2, 2\sqrt{3})$	$(2\sqrt{3}, 6\sqrt{3})$
	$\mathrm{GNR_{dn}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(4\sqrt{3}, 3\sqrt{3})$
XOR2	$\mathrm{GNR_{up}}$	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(5, 4\sqrt{3})$	$(3\sqrt{3}, 6\sqrt{3})$
	$\mathrm{GNR_{dn}}$	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(8, 2\sqrt{3})$	$(4\sqrt{3}, 6\sqrt{3})$

6.3.2 GNR Gates Performance Robustness under Temperature Variations

Table 6.2 summarizes our simulation results in terms of percentage variation of gate output level for logic "1" (V_{OH}) and logic "0" (V_{OL}), propagation delay

Table 6.2: GNR gates output voltage levels, delay, and power consumption variation (%) vs. temperature.

	$T[^\circ C]$	$V_{OH}[\%]$	$V_{OL}[\%]$	$\tau_{pd}[\%]$	$P[\%]$		$T[^\circ C]$	$V_{OH}[\%]$	$V_{OL}[\%]$	$\tau_{pd}[\%]$	$P[\%]$
	-55	-1.56%	-1.54%	147.1%	-85.1%		-55	-2.27%	-1.94%	22.1%	-81.3%
	-25	-1.04%	-0.94%	69.2%	-65.3%		-25	-1.66%	-1.51%	14.4%	-58.3%
INV	0	-0.80%	-0.56%	39.0%	-42.7%	BUF	0	-0.95%	-1.10%	7.8%	-43.4%
	60	2.18%	1.68%	-12.5%	112.9%		60	1.73%	1.13%	-17.3%	52.1%
	125	5.32%	4.18%	-14.2%	275.2%		125	3.52%	2.61%	-24.1%	83.7%
	-55	-2.29%	-1.72%	139.2%	-73.8%		-55	-1.54%	-1.07%	63.8%	-73.2%
	-25	-1.63%	-1.16%	57.0%	-52.4%		-25	-1.08%	-0.67%	30.2%	-34.3%
AND2	0	-1.07%	-0.52%	32.1%	-29.8%	NAND2	0	-0.48%	-0.34%	3.2%	-22.8%
	60	1.47%	1.11%	-15.8%	59.3%		60	1.37%	2.07%	-3.3%	87.9%
	125	2.57%	3.27%	-39.3%	188.0%		125	3.67%	4.21%	-44.4%	374.2%
	-55	-1.47%	-1.55%	33.1%	-74.1%		-55	-1.43%	-1.55%	119.5%	-73.6%
	-25	-0.91%	-0.96%	23.1%	-57.1%		-25	-1.08%	-1.13%	39.0%	-54.4%
OR2	0	-0.55%	-0.51%	11.0%	-33.3%	NOR2	0	-0.66%	-0.60%	5.7%	-27.9%
	60	1.67%	1.48%	-38.8%	149.5%		60	1.11%	1.85%	-37.2%	105.8%
	125	3.78%	4.26%	-58.4%	397.4%		125	2.73%	3.48%	-48.9%	250.3%
	-55	-1.52%	-1.73%	59.3%	-72.2%						
	-25	-1.04%	-1.21%	30.2%	-53.8%						
XOR2	0	-0.51%	-0.72%	13.7%	-28.0%						
	60	2.13%	1.92%	-32.1%	168.8%						
	125	4.44%	3.96%	-47.2%	367.6%						

$T = 27^\circ C$ Reference	$V_{OH}[mV]$	$V_{OL}[mV]$	$\tau_{pd}[ps]$	$P[nW]$
INV	194.27	5.34	0.28	0.670
BUF	193.60	5.90	0.48	0.459
AND2	193.34	5.61	0.62	0.357
NAND2	195.16	3.60	0.67	0.263
OR2	195.26	4.95	0.77	0.291
NOR2	195.25	4.96	0.64	0.316
XOR2	195.23	5.00	0.67	0.280

(τ_{pd}), and power consumption (P). All reported percentages are relative to the values obtained at room temperature $27^\circ C$ (listed in Table 6.2 right bottom inset). One can observe that, for all gates, starting from a certain threshold temperature (inbetween $0^\circ C$ and $27^\circ C$), with temperature decrease the following trends are in place: (i) output signal levels get closer to the supply rails voltages - for logic "1" (from -0.48% to -2.29% closer) and for logic "0" (from -0.34% to -1.94% closer), (ii) power consumption decreases (from -22.8% to -85.1%), while (iii) propagation delay gets worse (from 3.2% to 147.1% increase). When increasing T above the temperature threshold, the trend reverses: (i) output signal levels deteriorate from 1.11% to 5.32% for logic "1" and from 1.11% to 4.26% for logic "0", (ii) power consumption increases from 52.1% to 397.4%, while (iii) propagation delay decreases from 3.3% to 58.4%. Overall, across the considered temperature range ($-55^\circ C$ to $125^\circ C$) the following observations are in place: (i) V_{OH} and V_{OL} worst degradation is 5.32% for INV and 4.26% for OR2, respectively, which suggests robustness of GNR-based gates with respect to temperature variation, (ii) gates switch up to $2.47\times$ slower for INV (but still $1.61\times$ faster than CMOS FinFET 7nm at $27^\circ C$), and (iii) gates consume up to $5\times$ more power for OR2 (but still $395\times$ less power than CMOS FinFET 7nm counterpart at $27^\circ C$).

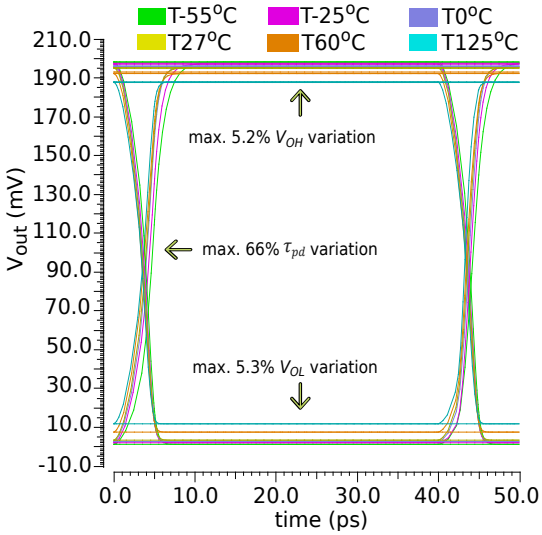

Figure 6.3: GNR NAND2 Gate Eye Diagram (% variations are between min and max values).

The eye diagram for the 2-input GNR NAND gate output voltages depicted in Figure 6.3, reveals that the maximum variations for V_{OH} and V_{OL} are 5.2% and 5.3%, respectively, while the maximum propagation delay variation is 66%. Table 6.3 summarizes the worst case delay (at $-55°C$) and power consumption (at $125°C$) for all GNR gates vs. CMOS FinFET 7nm counterparts at room temperature $27°C$, and indicates that even in the worst case temperature conditions GNR gates can still outperform CMOS equivalent counterparts operating at room temperature, e.g., $8.7\times$ smaler delay for XOR2 and $185\times$ less power consumption for INV. These results clearly indicate that GNR-based gates exhibit performance robustness with respect to temperature variations.

Table 6.3: GNR gates worst case propagation delay and power consumption vs. room temperature CMOS FinFET $7\,\text{nm}$ counterparts.

		INV	BUF	AND2	NAND2	OR2	NOR2	XOR2
τ_{pd} $[ps]$	GNR	0.69	0.58	1.48	1.09	1.02	1.40	1.06
	CMOS	1.11	2.04	9.62	7.56	8.31	9.18	9.17
P $[nW]$	GNR	2.5	0.8	1.0	1.2	1.4	1.1	1.3
	CMOS	462.1	470.4	588.6	541.5	553.5	452.8	592.3

6.4 Conclusion

In this chapter, we performed an evaluation of temperature variations impact on the reliability and performance (output signal integrity, propagation delay, and power consumption) of GNR-based complementary Boolean gates, while taking into account phonon scattering effects on carrier transport. Our results suggest that GNR-based gates are robust with respect to temperature variations and even in the worst case condition potentially outperform room temperature operating CMOS FinFET 7nm counterparts. Our results are suggesting that GNR-based complementary gates have potential as basic building blocks for future reliable, low-power, nanoscale carbon-based electronics.

Note. The content of this chapter is based on the following paper:

Y. Jiang, N. Cucu Laurenciu, H. Wang, and S.D. Cotofana,, **A Study of Graphene Nanoribbon-based Gates Performance Robustness under Temperature Variations**, *IEEE* 20^{th} *International Conference on Nanotechnology (IEEE-NANO)*, 2020.

7

Conclusions and Future Work

In this thesis, we first presented a GNR-based structure (building block) and pursued 4 main investigation avenues: (i) exploring the building block's ability to open the GNR energy bandgap via GNR geometry change, (ii) investigating various GNR geometries and contact topologies influence on the GNR building block's conductance and current characteristics, (iii) encoding the desired Boolean logic transfer function into the GNR electrical characteristics, e.g., conduction maps, (iv) evaluating the impact of V_{DD} variation and edge defects on the GNR building block conductance. Second, we developed a parameterized Verilog-A SPICE-compatible generic model based on Non-Equilibrium Green's Function (NEGF)-Landauer formalism for simulations of the GNR-based building block, and gates. Subsequently, we proposed a construction method of GNR-based Boolean gates and circuits, and presented a GNR-based 1-bit Full Adder and a SRAM cell. Finally, we extended the NEGF-Landauer simulation framework with the self-consistent Born approximation in order to taking into account the temperature-induced phenomena, and explored the temperature variation impact on the GNR-based gates' reliability and performance, e.g., output signal integrity, propagation delay, and power consumption.

7.1 Summary

The thesis contents can be summarized as follows:

Chapter 1 - We discussed graphene crystal and its chemical bonds, and introduced graphene electrical and mechanical properties. Subsequently, we presented 3 current graphene synthesis methods, i.e., epitaxial growth, mechanical exfoliation and chemical exfoliation, and then summarized the main graphene-based applications, ranging from spintronics, photonics and optoelectronics,

sensors, energy storage and conversion, to biomedical applications, and digital electronics. Next, we argued the main challenges to GNR logic circuits, which are design and manufacturing related. Last, we formulated the corresponding research questions addressed in the thesis, highlighted the proposed approaches, and summarized the contributions we made in this thesis.

Chapter 2 - We proposed a graphene building block which employed a carved GNR as conducting channel, and extended it with source/drain contacts and additional top/back gates as means to modulate its conduction. First, we explored the building block's ability to open the GNR energy bandgap via GNR geometry change. To this end, we designed 5 different GNR shapes with zigzag edges, e.g., Rectangular GNR, Butterfly GNR, Camel GNR, Waterfall GNR and Double Butterfly GNR, and our simulation results exhibited that we were able to widely open GNR energy bandgap by means of GNR geometry carving, e.g., Butterfly GNR and Waterfall GNR derived energy bandgap values of $0.4\,\mathrm{eV}$ and $0.7\,\mathrm{eV}$, respectively. Subsequently, we investigated the GNR geometry influence on its conductance and current characteristics. The obtained results indicated that for Butterfly GNR configuration, the narrow and short constriction channel was efficient to obtain a high current ratio, up to 2.1×10^4, and the bigger angle (between constriction channel and Drain/Source contact) could achieve better current ratio. Longer and wider bump structure provided better current ratio (up to 1.5×10^4) for Camel GNRs, and the bump configurations improved the current related characteristics for Double Butterfly GNRs. Last, we explored the ability of gate bias (e.g., top gate V_{g} and back gate V_{back}) to control GNR conduction, and the experimental results suggested the top/back gate contacts are good enough ways to modulate the GNR-based device conduction.

Chapter 3 - We introduced an approach of encoding the desired Boolean logic transfer function into the graphene electrical characteristics, e.g., conduction density maps (conductance G vs. top gate voltages), by performing a Design Space Exploration (DSE) with respect to GNR topologies and geometries. To this end, we considered a basic set of Boolean functions (e.g., INV, BUF, AND, NAND, OR, NOR, XOR, XNOR), and for each function we identified a GNR geometry which enabled a conduction density map reflecting the corresponding Boolean function truth table, e.g., high G referred to logic output "1", low G represented logic output "0". The simulation results indicated that the proposed 2-input GNR-based building blocks operating at $V_{\mathrm{DD}}=0.2\,\mathrm{V}$ outperformed $7\,\mathrm{nm}$ FinFET CMOS counterparts, up to 2, 2 and 4 orders of magnitude in terms of propagation delay, power consumption, and power-delay product, respectively, while requiring 2 orders of magnitude less

active area. Particularly, for 3-input Boolean function, the 3-input GNR-based building blocks proved to be even more effective. Further, we investigated the proposed GNR-based building block sensitivity to gate fan-in scaling, as when incrementing it from 2 to 3, and our results revealed that the GNR-based building block was less sensitive to gate fan-in scaling, and obtained 26% and 42% variation for area and delay, respectively, while CMOS area footprint and delay increased, up to 100% and 51%, respectively. Subsequently, we evaluated the effect of V_{DD} variation and edge defects on the GNR-based building blocks' conductance and delay, and further determined V_{DD} lower bound for proper operation. The experimental results suggested the proposed GNR-based building blocks have a strong robustness with respect to V_{DD} variation and edge defects, e.g., the conductance and delay for the GNR-based building block which mirrored NOR functionality changed by no more than 2% and 6%, respectively. For V_{DD} lower bound value, the NOR GNR-based building block was able to operate even at $10\,\mathrm{mV}$. The obtained results suggested our proposal opens an alternative towards effective carbon-based nanoelectronic circuits and applications.

Chapter 4 - We developed a fast and accurate Verilog-A SPICE-compatible generic model which enabled parameterized electrical simulations of the GNR-based building blocks with various dimensions and geometries, while preserving the physical simulation accuracy degree. The model computed the GNR conductance and current based on the NEGF-Landauer formalism, via a Simulink model which was called within the Verilog-A code. We validated the model accuracy and versatility by means of Simulink assisted Cadence Spectre simulation of a simple test case GNR-based circuit and a GNR-based 2-input XOR gate, and the simulation results indicated the GNR model was accurate, enabled the accurate evaluation of graphene-based circuits potential performance, and allowed for graphene-based circuit design and optimizations, which suggested the model potential of bringing GNR specific phenomena from the physics to the circuit-level by fully comprehending the GNRs behavior and potential benefit in the circuit context.

Chapter 5 - We presented a construction method of GNR-based Boolean gates, in which two GNRs are arranged in a complementary way, i.e., a pull-up GNR performed the targeted Boolean function and a pull-down GNR operated its inverse Boolean function, and the gate primary inputs voltages were applied via top gates. Subsequently, we proposed and evaluated the 1-, 2- and 3-input GNR gates in Cadence via the SPICE simulation which employed the proposed Verilog-A model. we obtained up to 2, 3, 2 orders of magnitude smaller propagation delay, lower power, and smaller active area footprint, respectively, when

compared to 7nm FinFET CMOS counterparts. In particular, the proposed GNR gates provided clean and compatible/matching gate inputs and outputs electric levels. Furthermore, we also proved that contrary to CMOS designs, the proposed GNR-based gates could yield effective power-delay trade-offs, at approximately the same area. Next, we presented a GNR-based 1-bit Full Adder (FA) and a SRAM cell, as they constituted the foundation for the construction of any computation system. More precisely, we design a 3-input MAJORITY gate to directly compute FA's Carry-Out. The simulation results revealed that the proposed FA design provided $6\times$ smaller delay, 3 orders of magnitude less power consumption, while requiring 2 orders of magnitude less area, when compared to 7nm FinFET CMOS counterpart. The proposed GNR-based SRAM cell achieved a better resilience to DC noise characteristics than the CMOS equivalent, while achieved $3.6\times$ smaller delay, 2 orders of magnitude less power, and 1 order of magnitude less area. The proposed GNR gates, FA and SRAM cell clearly indicated that GNR-based implementations can potentially surpass CMOS counterparts and that the proposed method is opening a promising avenue towards future high-speed, low-power, carbon-based digital circuits.

Chapter 6 - We extended the NEGF-Landauer simulation framework with the self-consistent Born approximation, while taking into account the temperature-induced phenomena, i.e., electronphonon interactions for both optical and acoustic phonons. Further, we evaluated the proposed complementary graphene-based Boolean gates behavior under a set of temperatures from $-55°C$ to $125°C$ which covered the commercial, industrial and military ranges, and investigated the impact of the temperature variation on GNR-based gates reliability and performance in terms of output signal integrity, input-to-output propagation delay, and power consumption by using SPICE simulation in Cadence. The obtained results indicated that the proposed GNR-based gates showed robustness with respect to temperature variation, and even in the worst temperature condition (at $125°C$) surpassed 7nm CMOS FinFET counterparts, which suggesting the GNR-based gates' potential of serving as basic building cells for future reliable, energy-effective, nano-scale graphene-based electronic circuit applications.

7.2 Future Research Directions

Subsequently, we discuss future research work suggested as a continuation of the research avenues undertaken in this thesis.

- **Reliability Studies of Ionizing Radiation Effects on GNR-based Boolean Gates**
  One interesting application field resides in developing radiation hardened and resilient devices utilized in high flux ionizing radiation fields, such as outer space. However, the experimental investigations suggest significant effects of irradiation on graphene, and potential radiation corresponding defects induced in graphene. Besides the edges defects, V_{DD} variation and temperature variation impact on the proposed GNR-based Boolean gates, the ionizing radiation (e.g., Ion, Gamma-ray, Alpha particle and Beta particles radiations) effects on the proposed gates performance also attract our interest. A study of ionizing radiation effects on the GNR-based gates performance (i.e., transport properties, charge carrier density, mobility, thermal properties, propagation delay, power consumption, and output signal integrity) is desired in this context.

- **Graphene-based Monolithic-3D Integrated Circuits**
  Three dimensional (3D) integration technology provides an effective platform for improving circuits performance by fabricating multiple layers of active devices (e.g., transistors or building blocks) on a single 3D chip. Graphene, due to its unique properties, is a promising 2D material for realizing ultra-high-density monolithic-3D integrated circuits of ultimate thinness for next-generation electronics, in which multiple stacked tiers (i.e., active layer, back-end-of-line layer and inter-layer dielectric layer) are grown sequentially on the same substrate, which has the potential of higher inter-layer dielectric density with respect to the traditional Through Silicon Via (TSV), higher routability and design flexibility. By means of monolithic-3D integration technology, the proposed GNR-based gates in the thesis are expected to be integrated into monolithic 3D circuits.

- **Graphene-based Reconfigurable Logic Circuits, Nonvolatile Magnetic Random Access Memories (MRAMs) Enabled by Spin-orbit Feature of Graphene**
  Graphene's low spin-orbit coupling and high carrier mobility make it very attractive for graphene-based spintronic devices (e.g., spin transistor and all-spin-logic devices), in which graphene functions as a spin-current transport channel with long spin-diffusion length (micrometers level) at room temperature. Graphene-based Magnetic Tunnel Junction (MTJ) which composes of an insulating barrier between two ferromagnetic materials, via Tunnel Magnetoresistance (TMR) effect for reading operation, and Spin Transfer Torque (STT) switching mechanism for

writing operation, are crucial components for reconfigurable logic circuits and nonvolatile MRAMs. The spin current-induced graphen-based reconfigurable logic circuits and nonvolatile MRAMs are desired in this context by using graphene-based MTJs as basic building blocks.

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Samenvatting

Terwijl de dimensies van CMOS-componenten de atoomschaal bereiken en het verspild statische vermogen, de betrouwbaarheid, en de economische implicaties verergeren, is er steeds meer vraag naar onderzoek naar nieuwe materialen, apparaten, en/of computatieprincipes. In die context kunnen grafeen nanolinten (*Graphene Nanoribbons*, GNR's) de basisstructuren vormen voor koolstofgebaseerde nanoelektronica dankzij de uitstekende elektronische eigenschappen van grafeen. Echter, het gebrek van grafeen aan een intrinsieke energiebandkloof is beperkend in de implementatie van GNR-componenten en -schakelingen. Als gevolg hiervan zijn de belangrijkste doelstellingen op het pad naar grafeengebaseerde logische schakelingen het vinden van een manier om een significante energiebandkloof te openen, het extern aansturen van de geleiding van GNR's, en het samenstellen van betrouwbare, hoogwaardige grafeengebaseerde poorten. Om dit te bereiken, stellen we ten eerste een GNR-gebaseerde structuur op als bouwsteen door die uit te breiden met zogeheten *top gates* en *back gates*, terwijl we vijf GNR-vormen beschouwen met zigzagranden om een significante bandkloof te openen, en verder onderzoeken we hoe de geometrie en contacttopologie van GNR's hun geleiding en stroomkarakteristieken beïnvloeden. Ten tweede presenteren we een methodologie om de gewenste booleaanse logische overdrachtsfunctie ter versleutelen in de elektrische karakteristieken van een GNR zoals de geleidingsfunctie, en evalueren dan het effect van V_{DD} op de geleiding van een GNR. Bovendien vinden we een goede externe manier (zoals de *top gates* en *back gates*) om het gedrag van de GNR aan te sturen. Ten derde ontwikkelen we een geparametriseerd, Verilog-A SPICE-geschikt GNR model gebaseerd op het *Non-Equilibrium Green's Function* (NEGF)-Landauer formalisme dat gebaseerd is op een nauwkeurige fysische formalisatie, wat in staat stelt om symbiotisch gebruik te maken van naurkeurige fysische resultaten van MATLAB Simulink en geöptimaliseerde SPICE schakelingsoplossers (zoals Spectre of HSPICE). Vervolgens stellen we grafeengebaseerde booleaanse poorten samen door middel van twee complementaire GNR's samen en ontwerpen we een GNR-gebaseerde 1-bit Full Adder en een SRAM-cel. Ten slotte breiden we het NEGF-Laundauer simulatieprincipe uit met de zelfconsistente Bornbenadering waarbij we temperatuurgerelateerde effecten, zoals interactie tussen elektronen en zowel akoestische als optische fononen, in acht nemen en onderzoeken we de robuustheid van de eigenschappen van de grafeengebaseerde poorten onder temperatuurvariaties.

List of Publications

Publications related to the thesis

International Journal Papers

1. **Y. Jiang**, N. Cucu Laurenciu, H. Wang, and S.D. Cotofana, Graphene Nanoribbon Based Complementary Logic Gates and Circuits, *IEEE Transactions on Nanotechnology (TNANO)*, vol. 18, p. 287-298, 2019.

2. **Y. Jiang**, N. Cucu Laurenciu, and S.D. Cotofana, On Basic Boolean Function Graphene Nanoribbon Conductance Mapping, *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, vol. 66(5), p. 1948-1959, 2018.

International Conference Proceedings

1. **Y. Jiang**, N. Cucu Laurenciu, H. Wang, and S.D. Cotofana, A Study of Graphene Nanoribbon-based Gate Performance Robustness under Temperature Variations, *IEEE 20th International Conference on Nanotechnology (IEEE-NANO)*, pp. 62-66, 2020.

2. **Y. Jiang**, N. Cucu Laurenciu, and S.D. Cotofana, On Carving Basic Boolean Functions on Graphene Nanoribbons Conduction Maps, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2018.

3. **Y. Jiang**, N. Cucu Laurenciu, and S.D. Cotofana, Complementary Arranged Graphene Nanoribbon-Based Boolean Gates, *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 1-7, 2018.

4. **Y. Jiang**, N. Cucu Laurenciu, and S.D. Cotofana, Non-Equilibrium Green Function-Based Verilog-A Graphene Nanoribbon Model, *IEEE 18th International Conference on Nanotechnology (IEEE-NANO)*, pp. 1-4, 2018.

Other publications

International Journal Papers

1. H. Wang, N. Cucu Laurenciu, **Y. Jiang**, and S.D. Cotofana, Graphene-based Artificial Synapses with Tunable Plasticity, *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 2020. (submitted)

International Conference Proceedings

1. H. Wang, N. Cucu Laurenciu, **Y. Jiang**, and S.D. Cotofana, Ultra-compact, Entirely Graphene-based Nonlinear Leaky Integrate-and-Fire Spiking Neuron, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2020.

2. H. Wang, N. Cucu Laurenciu, **Y. Jiang**, and S.D. Cotofana, Graphene Nanoribbon-Based Synapses with Versatile Plasticity, *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 1-6, 2019.

3. H. Wang, N. Cucu Laurenciu, **Y. Jiang**, and S.D. Cotofana, Atomistic-level Hysteresis-aware Graphene Structures Electron Transport Model, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2019.

Curriculum Vitae

Yande JIANG was born on August 4^{th}, 1990 in Guilin, Guangxi Province, China. In 2006, he started his high-school study at Guilin High School, Guilin, China. During this period, he developed his interest in computer.

He entered the College of Computer at National University of Defense Technology (NUDT), Hunan, China in 2009, and got his B.Sc. degree in Computer Science and Technology in 2013, and M.Sc. degree in Electronic Science and Technology in 2015, under the supervision of Prof. Yang Guo. This period of study gave him a comprehensive understanding of computer architecture and microelectronics, and it became clear that he wants to have a career in scientific research.

In 2016, he was awarded a 4-year scholarship from the China Scholarship Council (CSC) to pursue his Ph.D. at the Department of Quantum and Computer Engineering, the Faculty of Electrical Engineering, Mathematics, Computer Science at Delft University of Technology (TU Delft). Driven by his interest, he continued to study nanotechnology and nanocomputing, and received the supervision from Prof. dr. S. D. Cotofana. His Ph.D. studies focus on graphene-based computing: e.g., modeling and simulation of nano-device, reliability study on nano-logic and gates, graphene-based circuits design. The results of the work are presented in the current dissertation.

He will continue research in graphene-based computing and nanotechnology after his Ph.D. graduation.