Flexible parylene-platinum based electrodes and interconnects

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Challenge the future

FLEXIBLE PARYLENE-PLATINUM BASED ELECTRODES AND INTERCONNECTS

by

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ABSTRACT

F2R is a generic IC fabrication based platform that allows for the fabrication of miniature and flexible sensing functionalities for minimally invasive medical instruments. Examples of these minimally invasive medical instruments are catheters and guidewires. By introducing more materials to the F2R technology, it can be extended to more applications. An example of such an application is neural brain probes.

This thesis focuses on the introduction of parylene and platinum to the F2R technology. This is a challinging tasks, as many different technologies have to be introduced and modified. Therefore, the main objective of this thesis was to develop a fabrication process that allows for the electrical and mechanical evaluation of flexible parylene-platinum based electrodes and interconnects.

In order to electrically and mechanically evaluate the devices, test structures were designed. These test structures make the electrical and mechanical evaluation possible and can be used for further evaluation of future developments. Furthermore, several fabrication technology modules have been developed. The effect of particles on the stability of the device has been reduced by investigating their origin. The step coverage of platinum was improved by optimizing the dry etching of parylene. This was done by introducing CF_4 to the etching process, which resulted in a desired 45° slope of sidewall of the parylene structures. Also, the patterning of platinum was improved by separating the etching process into two steps. This resulted in fenceless and clean metallization.

Since the adhesion of the layers is of major importance for in-body applications, the adhesion of parylene and platinum was investigated. By exploring several adhesion promoting techniques, the overall adhesion of the devices was found to be good, and therefore sufficient for electrochemical characterization.

All the previous technology modules were integrated where possible, and have led to the fabrication of flexible parylene-platinum based devices. These test devices consist of a silicon island with bond pads and flexible part with electrodes and a comb-meander structure. Rolling tests have shown that the devices can be rolled to an inner diameter of <1 mm without damaging the interconnects. This flexibility is required for the assembling of a 3D brain probe using a flexible microelectrode array.

PREFACE

This thesis concludes my Biomedical Engineering master program. I would like thank my supervisor Ronald Dekker for giving me the oppurtunity to do this thesis and his support during this project. I would also like to thank my mentor Marta for guiding me in this project. Without their knowledge and patience this work would not be possible.

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A.I. Kanhai
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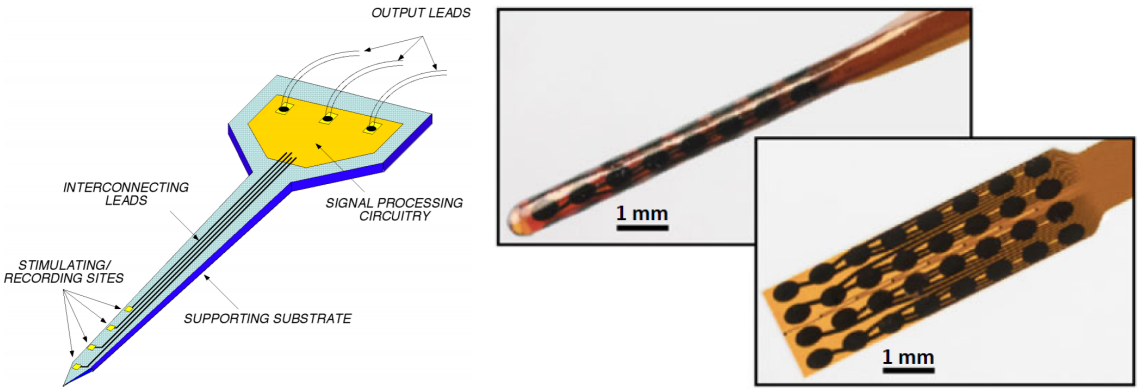
CONTENTS

1

INTRODUCTION

Deep brain stimulation (DBS) is an effective treatment for neurological and psychiatric disorders. Examples of medical conditions that have been succesfully treated with DBS are: Parkinson's Disease, obsessive compulsive disorders (OCD), dystonia and depression [1][2]. The neural stimulation to the brain is provided by a neural probe, which contains an array of microelectrodes. These microelectrodes are implanted in the brain at a specific target site, depending on the condition and symptoms of the patient. The development of micro-electromechanical systems (MEMS) technology over the years has led to different designs and fabrication processes of microelectrodes for neural recording and stimulation. Initially, most of these designs consisted of microelectrodes that where positioned in 1D or 2D arrays (Figure 1.1(a)). However, most of the state-of-the-art neural probes now consist of a 3D microelectrodes array configuration that is realized by cylindrically wrapping a flexible thin film with electrodes and interconnects (Figure 1.1(b)). These 3D designs improve the DBS lead's capability to stimulate brain tissue by providing more refined spatial stimulation to the surrounding tissue [3][4][5]. Furthermore, these probes can provide higher density electrodes, and thus promote miniaturization of neural probes. This will reduce the foreign body response, which is a major cause of implant failure [6].



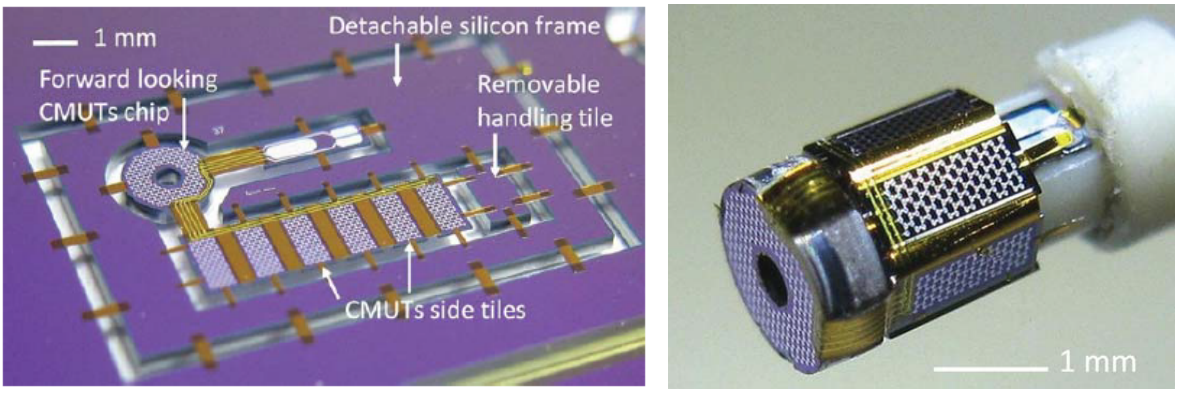
(a) (b)

Figure 1.1: Examples of different probe designs: (a) schematic design of a basic 2D neural probe; (b) 3D design of a flexible thin film based probe before and after wrapping [7]

1.1. FLEX-TO-RIGID PLATFORM

The previously mentioned 3D probe designs require more advanced fabrication and assembly methods. This can be achieved by using the flex-to-rigid (F2R) platform [8][9]. F2R is a generic IC fabrication based platform that allows for the fabrication of miniature and flexible sensing functionalities for minimally invasive medical instruments such as catheters and guidewires. It utilizes, flexible high-density interconnects consisting of polyimide and aluminum (Figure 1.2). This makes wrapping- and folding-based assembly methods possi-

ble, and enables, for example, the integration of devices on the tip of the instrument. Furthermore, devices of arbitrary shape and thickness can be realized through a backside silicon deep reactive ion etching (DRIE) process.
If F2R technology would be applied to neural brain probes, it will make novel designs possible, such as the integration of active electronics into the tip of DBS devices. This will make the implant less invasive, since less electronics have to be implanted to process and provide the proper signal to the brain. Also, less lead have to be used, making the device more robust. Moreover, since it is fully based on the standard IC fabrication, higher density flexible thin film electrode arrays can be fabricated. This will result in more accurate stimulation of the tissue, which in the end will lead to better treatment of DBS and improvements in the previously mentioned applications of neural recording and stimulation.
In order to extend the F2R technology to neural brain probes, the materials used in the platform have to be adjusted to the different biological environment, which is brain tissue. As previously mentioned, polyimide and aluminum are being used for the flexible interconnects. Both of these are not the most suitable materials for brain implants (biocompatibilty of polyimide not sufficient and aluminum is not a noble metal). A good alternative for flexible interconnect and the encapsulation is parylene, and for the metallization platinum is preferred.



(a) (b)

Figure 1.2: Example of a F2R based device that can be integrated at the tip of a $2mm$ diameter catheter [8].

1.2. PARYLENE C

A material that is commonly employed in implantable devices for flexible interconnects and encapsulation is Parylene C (from now on referred to as parylene). This is due to its many desirable properties [10][11][12]. Parylene has a lower Young's Modulus ($E \approx 4GPa$) than other polymers such as polyimide, which reduces the mechanical mismatch between the device and the tissue. Furthermore, it has the highest degree of biocompatibility (USP Class IV) and good insulating properties. It also has a low water vapor transmission rate of $0.2\frac{g \cdot mm}{m^2 \cdot day}$ [13]. Finally, parylene can be processed using standard microfabrication techniques. Parylene is deposited in a conformal chemical vapor deposition process, and the etching can be done using oxygen plasma based processes.

1.2.1. CHEMICAL VAPOR DEPOSITION

The chemical vapor deposition process (CVD) allows thin conformal deposition, which also enables the parylene to cover sharp edges and fill slits under components [14] [15]. The CVD of parylene consists of three main steps, which are sublimation, pyrolysis and polymerization. Dimer, or paracyclophane, is the source material of parylene (solid white granular powder). This is loaded into the vaporizer, where the sublimation occurs at around $175°C$. The dimer is converted into gas, and flowing into the pyrolysis furnace. Due to the conversion to the gaseous phase, the pressure rises. This change is used to control the deposition rate. The next step is pyrolysis, which is executed at $690°C$. This high temperature process transforms the molecule structure in the dimer gas into monomer vapor. The final step is the bonding of the monomers, where they form long molecular chains to grow the parylene layer directly on the ambient temperature surfaces. Molecules are deposited and no byproducts are present from the polymerization process.

1.2.2. SILANE A-174

Parylene, due to its chemical structure, is hydrophobic and it will therefore prefer to bond with a clean hydrophobic surface. This introduces problems when depositing parylene on a hydrophilic surfaces like SiO_2, which is a commonly used insulator in microfabrication. To increase the adhesion of parylene to SiO_2 and other hydrophilic substrates, a commonly used adhesion promoter is methacryloxypropyltrimethoxysilane or Silane A-174 [10]. The molecules of this adhesion promotor create a monolayer, with a hydrophilic silane head adhering to oxide on one end, and a carbohydrate tail that bonds with parylene on the other end. Silane A-174 has shown to provide sufficient adhesion for parylene on SiO_2. Since platinum is more hydrophilic, Silane A-174 has also been tested as an adhesion promoter before depositing parylene on platinum [10]. This showed to increase the bonding strength in peel tests from $\sim 5\ mN/cm$ (no treatment) to $\sim 1000\ mN/cm$ (with Silane A-174).

1.3. PLATINUM

Platinum and its alloys have many valuable uses in different types of implantables, e.g. pacemakers, cochlear implants, retinal implants and brain implants. This is mainly due to its high nobility, which causes no reaction when surrounded by human tissue and body fluids. This noble metal is also highly biologically inert and has low corrosivity [16].

1.3.1. PHYSICAL VAPOR DEPOSITION

Physical vapor deposition (PVD) is the process in which a layer of atoms or molecules are deposited from the vapor phase onto a solid substrate in vacuum chamber. The most common types of PVD of platinum are sputtering and evaporation [17]. Sputtering involves ejecting a material from a target source onto a substrate. This is realized by bombarding the target by an ionized gas (often an inert gas such as argon). It is used commonly to deposit thin films of various materials IC processing. In evaporation, the target material is bombarded with an electron beam given off by a filament. The atoms from the target material are evaporated and converted into the gaseous phase. These atoms are then undergoing precipitation, which results in a thin layer on the substrate.
Sputtering is used in this thesis to deposit platinum for several reasons. First of all, it provides better step coverage since the atoms have high energy when arriving on the parylene surface. For the same reason, sputtering also provides better adhesion to the parylene compared to evaporation. Furthermore, evaporation is very slow compared to sputtering. In this fabrication process 600nm of platinum was used. This thickness would result in a very time consuming deposition and would practically not be feasible.

1.3.2. ION MILLING

The etching of platinum in this fabrication process will be done by ion milling. Ion milling is a physical etching technique where ions of an inert gas (argon) are accelerated from a wide beam ion source towards the surface of a substrate in vacuum. This continuous bombardment of the substrate by ions removes the surface materials. The incident beam angle of the ions is usually between 30° and 60°, which is controlled by the angle of the substrate table. This incident angle increases the etch rate significantly (up to 50%) compared to a 90° incident angle [18].
Lift-off is another method to pattern platinum. However, it has shown to be very inconsistent, especially when the platinum is sputter deposited [19]. This is mainly due to the platinum particles that remain or redeposit on the wafer after the lift-off process. Furthermore, since parylene is already present on the wafer during the patterning, the photoresist stripping methods are limited. This introduces problems when the photoresist below the parts that should have been lifted off did not dissolve properly.

1.4. AIM OF THIS THESIS

Introducing parylene and platinum to F2R technology is a major change. Therefore, the main objective of this thesis is to develop a fabrication process that allows for the electrical and mechanical evaluation of flexible parylene-platinum based electrodes and interconnects. This thesis will make a step in the development of integrating parylene and platinum in the F2R technology in the future.

To fabricate reliable biomedical devices for implantation, contamination with particles needs to be minimized. Therefore during the fabrication process, the major particle contamination causes are detected and

investigated.
To develop a fabrication process for parylene-platinum based electrodes, different process steps have to be investigated. To enable this, a device has to be designed that allows for simple evaluation of properties such as electrode impedance, delamination and minimum bending radius.
Since adhesion is of major importance in this process to minimize delamination, this is discussed and elaborated on from results from previously conducted research. The goal of research was to evaluate adhesion promoting treatments by doing cross cut tests before and after soaking in a saline solution.
The patterning of parylene has to be investigated (primarily the slope of the etched profile) in order to make the platinum metallization fully and uniformly covering the parylene.
The patterning of platinum using also has to be investigated in order to obtain clean (no photoresist residues) and fenceless metallization.
These technology modules have to be integrated, and the final DRIE process and releasing has to be investigated to make the device (partly) flexible. At last, wrapping of the flexible part of the device has to be evaluated , with the main goal of rolling the device with a diameter ≥1 mm. Commercially available DBS probes have diameters between ~ 1 mm and ~ 1.5 mm [20].

1.5. ORGANIZATION OF THIS THESIS

Chapter 2 discusses the mask design, used materials and the initial simplified process flow. Chapter 3 discusses the particle contamination due to processing on both sides of the wafer. In Chapter 4, the adhesion of parylene and platinum is investigated. Chapter 5 discusses the dry etching of parylene. The patterning of platinum is discussed in Chapter 6. Chapter 7 describes the integration of the technology modules, followed by the final device release steps in the process flow. The results of the electrical measurements and mechanical test of the devices are also included in this chapter. Finally, the thesis is concluded in Chapter 8, also including recommendations for future work.

2

DESIGN OF THE TEST DEVICES

2.1. INTRODUCTION

In order to allow for the characterization of the electrodes and evaluation of the mechanical stability of flexible parylene-platinum based electrodes and interconnects, test structures are required. This chapter discusses the mask design, the function of the test structure on the test devices, and the initial simplified fabrication process.

2.2. MASK DESIGN

The design consists of three main parts: bond pads, electrodes and a comb-meander structure. Figure 2.1 shows the complete design. Area 1 and 3 are non-flexible, area 2 is flexible. The area around the bond pads is not flexible to make the electrical measurements more practical. The device is supported by a frame to allow for easier handling when the silicon and oxide are etched from the back to make it partly flexible.
In total there a four masks required for this design. The first mask is used for the backside DRIE to etch make the device partly flexible. The second mask is used for the vias in the first parylene layer that results in a connection between the platinum and the oxide. The third mask is used to pattern the platinum on the first parylene layer, which is an inverted image. The fourth mask is used to reopen the bond pads, electrodes and etch through parylene between the device and the outer frame. This leaves the device suspended in the silicon frame. The devices can then be cut out of the frame, for example for electrode characterization.
The masks that are being used in EKL have a usable area of 20 x 20 mm^2 when used for one image. To be cost-effective, the four masks were placed on one mask plate by dividing it into four rectangles. This resulted in a die size of 20 x 5 mm^2. These dimensions were expected to be enough to place the previously mentioned test structures on the devices.

2.2.1. BOND PADS

The bond pads are connected to the electrodes and the comb-meander structure. In total there are six bond pads. Three of them are used for stimulation of the three electrodes, the other three are used for the comb-meander structure. The bond pads used for the electrodes are 3000 x 1000 μm^2, whereas the bond pads used for the comb-meander structure are 900 x 900 μm^2. The bigger size for three of the bond pads is chosen to make the electrical setup more practical, since these bond pads are designed to be clamped to provide continuous stimulation to the electrodes during characterization. The other three bond pads were designed smaller, since only impedance measurements need to be done on these (one measurement before and one measurement after soaking). The vias of the big bond pads are 2960 x 960 μm^2 and of the small bond pads are 860 x 860 μm^2.

2.2.2. ELECTRODES

The electrodes are used to provide electrical stimulation to the surrounding medium, which in this case is a saline solution. All three of them are connected to different bond pads so they can be characterized independently. The radii are 185 μm, 370 μm and 740 μm. The radius of 370 μm has shown to be a good size for brain stimulation electrodes, taking the trade-off between charge injection rate and impedance into account [7].

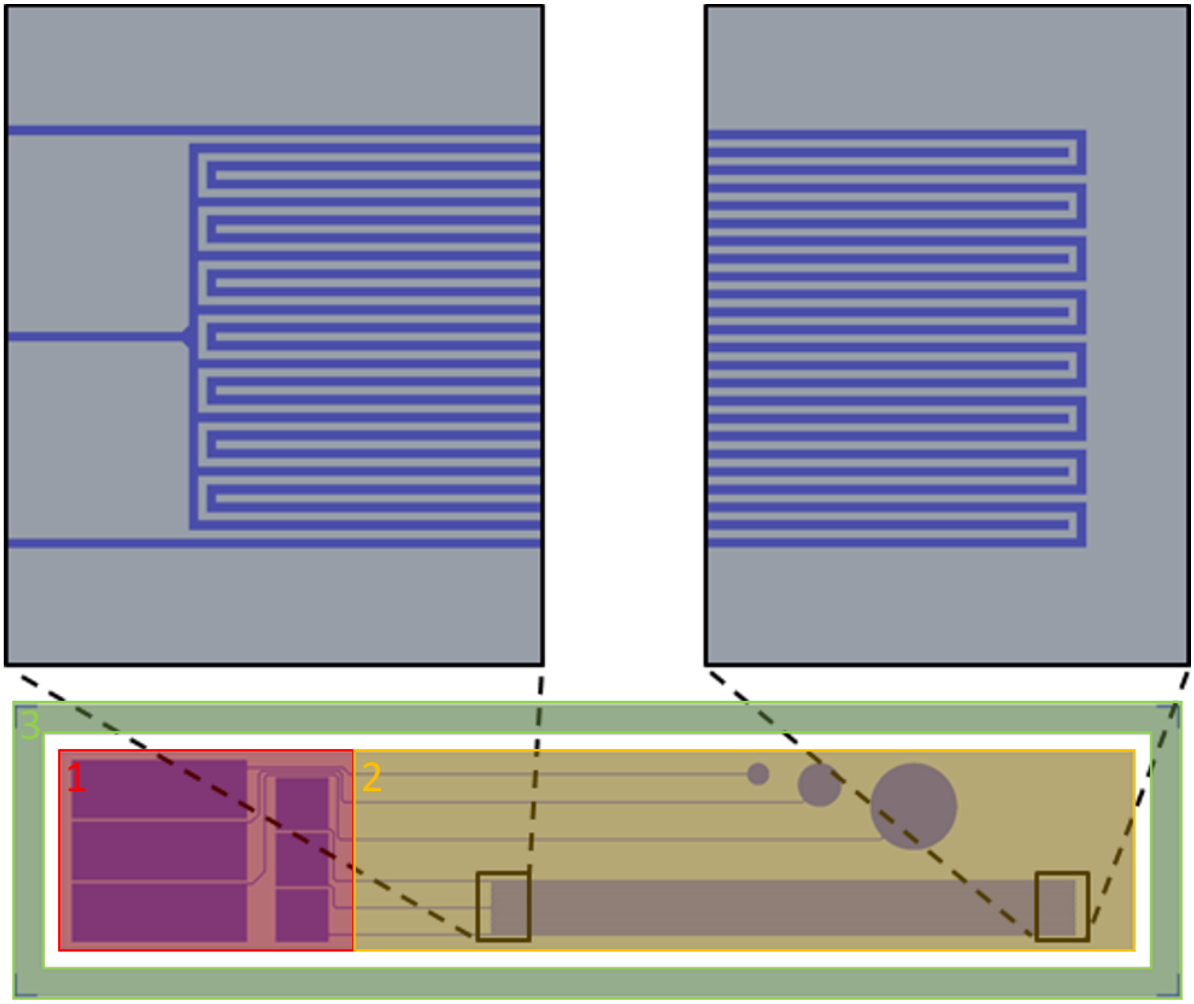


Figure 2.1: The mask design showing the 6 bond pads, 3 electrodes and the comb-meander structure on a substrate in the frame. Area 1 (6 bond pads on the silicon island) and area 3 (silicon frame) are non-flexible. Area 2 (3 electrodes and comb-meander structure) is flexible.

The size of the other two electrodes were based on this size, having twice this size and half this size. This was chosen to check its behavior when the sizes are changed for different applications (and because there was unused space on the die).

2.2.3. COMB-MEANDER STRUCTURE

In order to evaluate the structural stability of parylene-platinum based devices in a physiological environment, a comb-meander structures was designed to measure impedance changes, and to perform mechanical tests. The comb-meander structure consists of one meandering interconnect, and a comb structure in between this interconnect. The meandering interconnect allows for simple mechanical evaluation by measuring the resistance between the small outer bond pads. The width of all interconnects in the device is 20 μm (exceptions are the 90° corners in the IDE, which are slightly thicker).

2.3. PROCESS FLOW

As mentioned in Chapter 1, parylene and platinum are the two new materials introduced in the F2R fabrication flow, with the future goal to fully integrated them in the F2R process. In the F2R process, both sides of the wafer are processed, therefore double-sided polished silicon wafers are used. Figure 6.7 shows a simplified version of the schematic process flow. The following subsections discuss these steps in more details.

2.3.1. STEP 1 & 2: FRONTSIDE SILICON DIOXIDE AND BACKSIDE SILICON DIOXIDE HARDMASK

The process started with 2 μm of SiO_2 was deposited (PECVD) on the frontside, followed by deposition and patterning of 6 μm of SiO_2 on the backside. The backside SiO_2 was patterned to function as the hardmask for the DRIE release step later in the process. Although these steps are very simple, they already gave some problems, which are is discussed in Chapter 3. The frontside SiO_2 has multiple functions in this process. Firstly, it acts as an insulating layer for the bond pads (between the silicon and the platinum). Furthermore, it also makes the probe clamping less likely to damage the flexible device and makes handling more practical.

2.3.2. STEP 3: FIRST PARYLENE DEPOSITION AND PATTERNING

The next step was the deposition of 2.5 μm of parylene (CVD). The parylene on the frontside was patterned with the vias. This will be further elaborated in the Chapter 5. Once parylene is present on the wafer, no more high power oxygen plasma treatment or chemicals like HNO_3 are allowed.

2.3.3. STEP 4: PLATINUM DEPOSITION AND PATTERNING

Before 600 nm of platinum was sputtered, and titanium adhesive layer of 20 nm was sputtered. This is commonly used as an adhesion layer before platinum deposition. 600 nm platinum is used because it has shown to be necessary for flip chip purposes of these devices (unpublished). After platinum sputtering, the platinum was patterned, which is further described in Chapter 6.

2.3.4. STEP 5: SECOND PARYLENE DEPOSITION

After the platinum is patterned, the second 2.5 μm parylene deposition with Silane A-174 is performed. This thickness positions the metallization of the flexible membrane in the neutral axis.

2.3.5. STEP 6: TITANIUM DEPOSITION AND PATTERNING

The patterning of the second parylene layer (opening of the electrodes and bond pads) is done by using a titanium hardmask. A hardmask is necessary for the later patterning step since the devices are released from the back (DRIE). The titanium deposition (200 nm) was done at low temperature (25 $^{\circ}C$) due to the presence of parylene. This is further discussed in Chapter 7.

2.3.6. STEP 7: BACKSIDE SILICON ETCH

The 6μm oxide hardmask that was deposited and patterned in the first two step was used to etch 400μm of silicon (DRIE) from the backside. This etching process introduced some unexpected problems which will be discussed in Chapter 7.

2.3.7. STEP 8: PARYLENE ETCHING

The reopening of the electrodes and the bond pads was done with O_2 based plasma. Furthermore, this etching step also etches parylene around the device to make it suspend in the frame. This is further discussed in Chapter 7.

2.3.8. STEP 9: WET ETCHING OF OXIDE AND TITANIUM

The step in the process was to fully released the devices by stripping the titanium hardmask and the oxide on the backside. Like step 6, 7 and 8, this is further discussed in Chapter 7

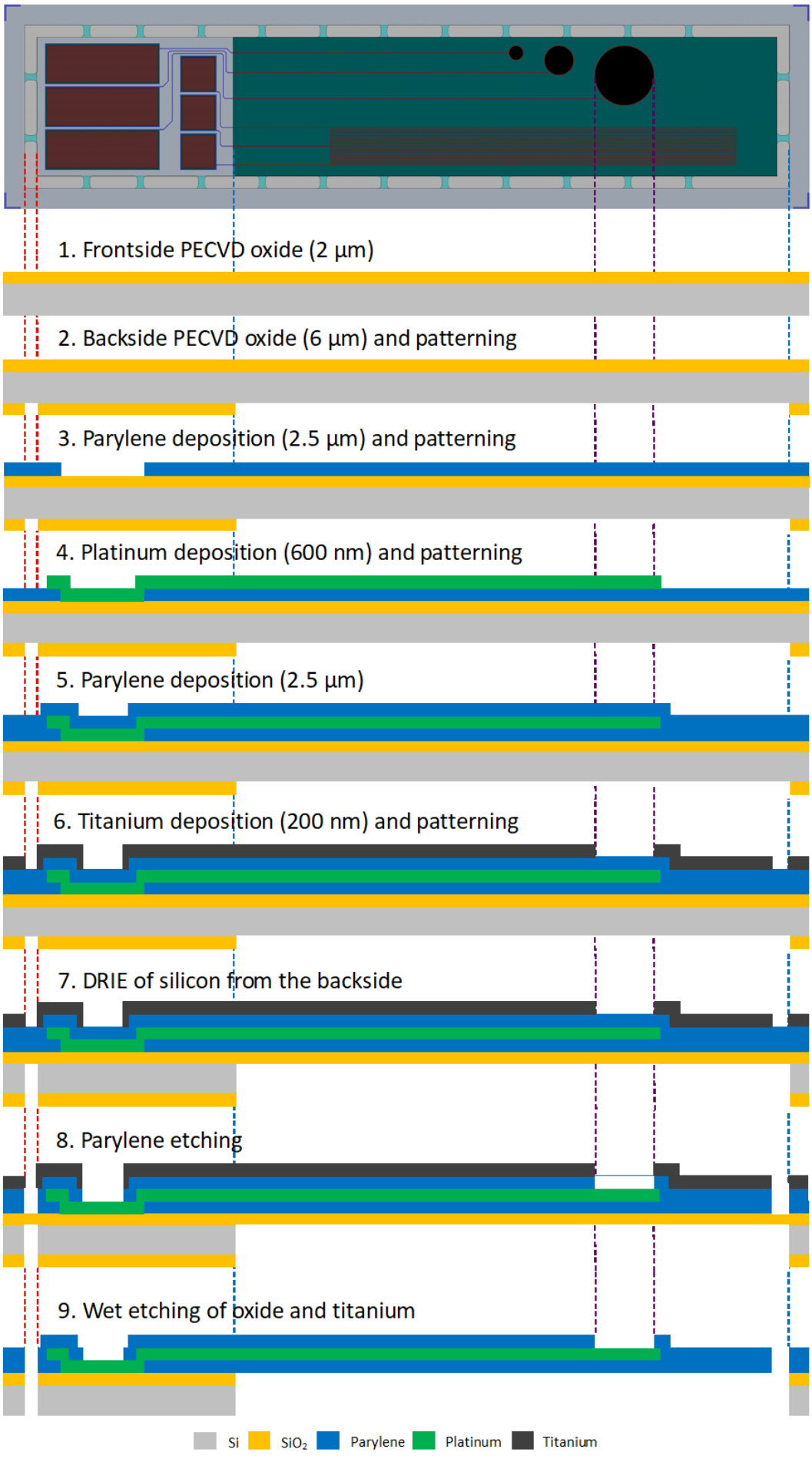


Figure 2.2: A simplified schematic flow of the full process

3

REDUCING PARTICLE CONTAMINATION

3.1. INTRODUCTION

Since this fabrication process is intended to produce parylene-platinum based flexible interconnects for implantables, contamination with any kind of particle has to be minimized. This chapter discusses the detection and possible reduction of particles that appeared due to processing the wafer on both sides.

3.2. PARTICLE CONTAMINATION AFTER FRONTSIDE OXIDE DEPOSITION

The process starts with the alignment markers lithography and etching on the frontside, followed by 2 μm oxide deposition on the frontside. A standard cleaning procedure was done by emerging the wafer in HNO_3 99% and HNO_3 69% for both 10 minutes. HNO_3 99% is used to clean the wafer from organics and HNO_3 69% is used to clean the wafer from metal traces. The next step is the 6 μm oxide deposition on the backside. This deposition revealed the presence of particles on the backside under the oxide originating from the handling fork. After this 6 μm backside oxide was patterned by dry etching, the resulting hardmask on the backside is used in the DRIE process to etch 400 μm of silicon on test wafers. This revealed that the particles were also masking during this etching process (see Figure 3.1).

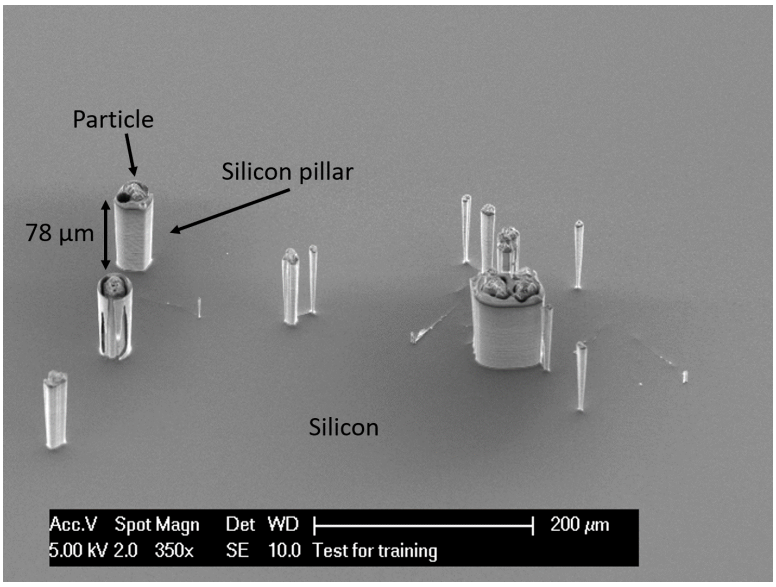


Figure 3.1: The backside silicon of the wafer after etching (DRIE) of 78 μm of silicon using the 6 μm oxide backside hardmask

To further investigate increase in particles after contact with the handling fork, an experiment was performed. This was done by measuring the amount of particles (Reflex 300 Particle Measurement) in between the process steps. Measurements were done on the backside of the wafer before processing, after deposition of 2 μm

of oxide on the frontside and after the previously mentioned cleaning procedure. The results of these measurements are presented in Figure 3.2. It is clearly visible in Figure 3.2(b) that the handling fork of the tool (Novellus) left particles residues on the backside, increasing the particle count from 3 to 1338. Furthermore, after the cleaning procedure, this even increased the particle count to 5852. Since cleaning in HNO_3 99% and HNO_3 69% did not reduce the amount of particles, indicates that the particles are not organic or metal traces.

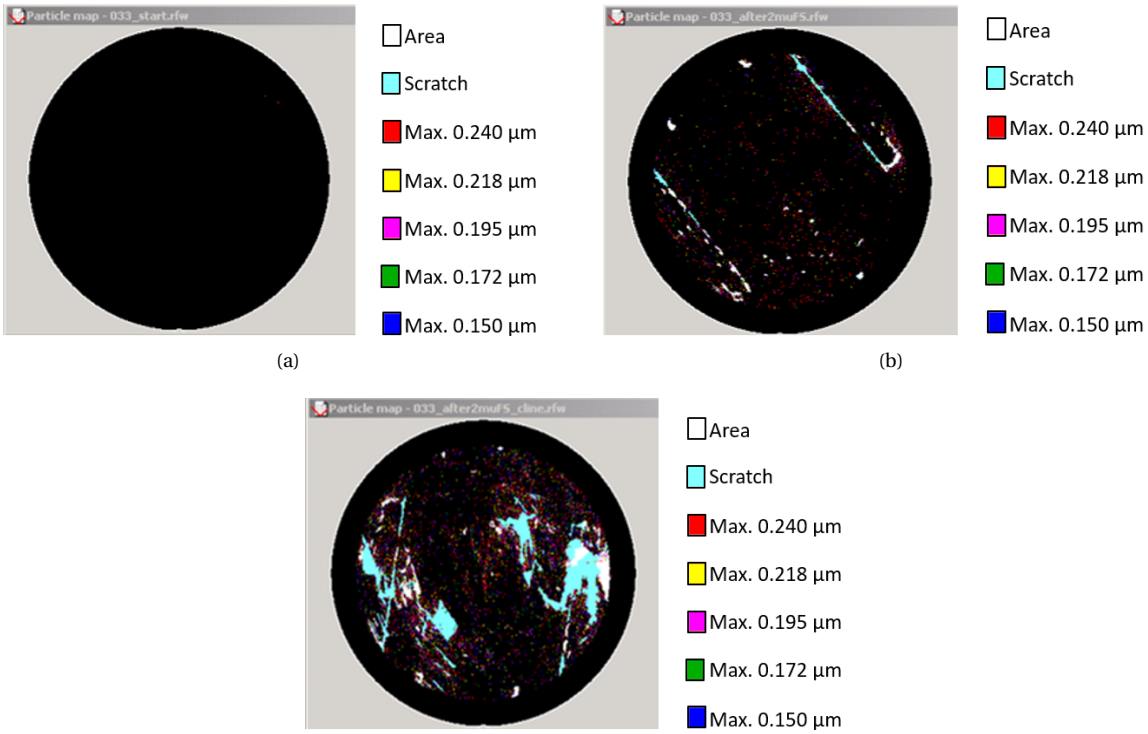


Figure 3.2: Results of the particle measurement on the backside: (a) before processing (particle count: 3); (b) after deposition of $2\mu m$ PECVD of oxide on the frontside (particle count: 1338); (c) after cleaning in HNO_3 99% and HNO_3 69% for both 10 minutes (particle count: 5852).

3.3. THERMAL OXIDE PROTECTION LAYER

Since the wafer is processed on both sides in this process, it would always make contact with the handling fork of the tool (Novellus) on both sides. A possible solution to reduce the amount of particles caused by this is to etch a thin layer of oxide away along with the particles caused by the handling fork. This was tested by growing 200 nm thermal oxide (on both sides of the wafer) as a protection layer before the process started. After oxide deposition on the frontside, the wafer was dipped in BHF 1:7 for 4 minutes to fully remove the thermal oxide on the backside. This short process flow is illustrated in Figure Figure 3.3. Figure 3.4 shows that the amount of particles is still similar to the previous situation (particle count: 1758), and therefore shows that the particles are not etched away along with the oxide. However, the pattern originating from the handling fork has been reduced.

Since the amount of particles could not be significantly improved, it was decided to change the order of the first few steps in the process. The goal of this different processing order was to avoid contact between the backside silicon of the wafer and the handling fork to avoid the previous masking. This was done by starting the fabrication process with the backside oxide deposition (6 μm). The wafer was then flipped for the frontside alignment markers lithography and etching, follow by the standard cleaning procedure. Next, the wafer was flipped and the backside lithography and etching was done. Lastly, the wafer was flipped again and 2 μm of oxide was deposited on the frontside. This change of the processing order results in the particles being present on top of the backside mask (instead of on the backside silicon) and in between the frontside oxide and the frontside silicon (instead of in between frontside oxide and the first parylene layer). Particles being present on top of the backside mask does not influence the DRIE process of the backside silicon. Fur-

thermore, particles being present in between the frontside oxide and the frontside silicon does not introduce a problem since oxide and silicon have good adhesion (and therefore the influence on the adhesion of the full stack is minimal).

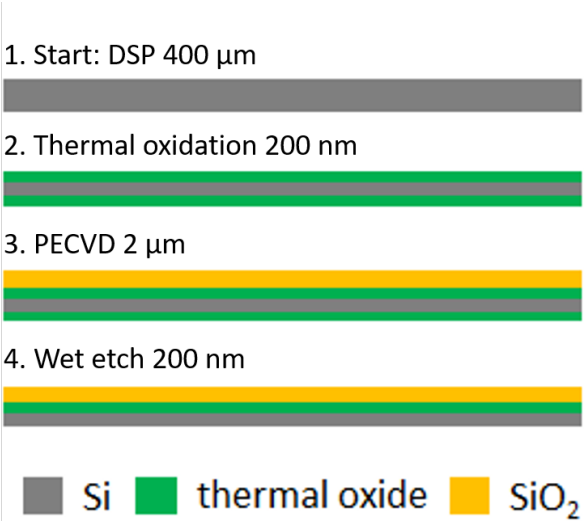


Figure 3.3: Schematic process flow of the experiment.

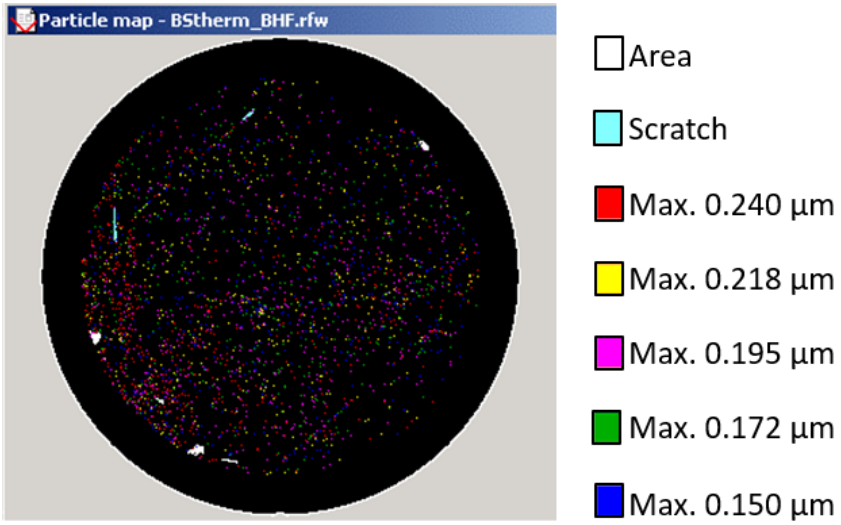


Figure 3.4: The backside of the wafer after wet etching the thermal oxide away with BHF 1:7 (particle count: 1758).

3.4. CONCLUSION

The PECVD oxide deposition on both sides of the double sided polished wafers results in a significant increase in the amount of particles. Cleaning with HNO_3 99% and HNO_3 69% for 10 minutes worsens this issue. Furthermore these particles cannot be etched away using BHF 1:7. Therefore, rather than reducing the amount of particles, they were repositioned on and in between layers that have minimal influence on the fabrication and the reliability of the device.

4

ADHESION OF PARYLENE AND PLATINUM

4.1. INTRODUCTION

In microfabrication of implantable electronic devices, a good adhesion between the layers of device is important. Poor adhesion between the layers will result in device failure. However, achieving perfect adhesion in the internal biochemical environment of the human body is challenging. For the device fabricated in this thesis, the main interfaces that require good adhesion are platinum on parylene, parylene on platinum, and parylene on parylene. This chapter will discuss the adhesion of these interfaces by testing different adhesion promoting techniques. Another interface that requires good adhesion (which is also present in the fabricated device) is parylene on oxide. However, these layers have sufficient adhesion when using the Silane A-174 primer, which will be explained later in this chapter. Therefore, the adhesion of parylene on oxide will be assumed to be good in the experiments.
The experiments in this chapter were performed during an internship. However, since the same deposition methods, materials and thicknesses were used, the obtained results are important for the further development of parylene-platinum based interconnects and electrodes for F2R applications inside the body. Furthermore, most findings in literature regarding the adhesion of parylene and platinum are based on different thicknesses and evaluation methods. This makes comparing results complex. Also, most methods to improve the adhesion are not possible due to the requirement of certain tools and setups. Therefore, the goal of these experiments was to test the most practical adhesion promoting techniques to get an initial idea of the adhesion that can in theory be achieved with the parylene-platinum based electrodes and interconnects fabricated in this thesis.

4.2. ADHESION OF PLATINUM TO PARYLENE

A method to increase the adhesion of platinum to common substrates such as oxide is by using a thin titanium layer (<100 nm). This is due to the higher binding strength that titanium has with oxide compared to other metals such as platinum [21]. As a result, it has become very common to use titanium as an adhesive layer between platinum and the used substrate. Increasing the surface roughness of parylene has shown to promote the adhesion to the next deposited layer [22]. A simple method to increase the roughness of parylene is by sputter etching (with an argon plasma) [23]. Another adhesion promoting treatment found in literature is annealing at high temperatures (≥200 °C). The reason for the working principle of this annealing treatment is the reduction of the intrinsic stress of the sputtered platinum, by recrystallization [24].

4.3. ADHESION OF PARYLENE TO PLATINUM

Parylene is hydrophobic and therefore prefers to bond with a clean hydrophobic surface. This introduces problems when depositing parylene on hydrophilic surfaces like oxide. To increase the adhesion of parylene to oxide and other hydrophilic substrates, a commonly used adhesion promoter is Silane A-174. The molecules of this adhesion promotor create a monolayer, with a hydrophilic silane head adhering to oxide at one end, and a carbohydrate tail that bonds with parylene on the other end. Silane A-174 has shown to provide sufficient adhesion for parylene to oxide. Since platinum is also hydrophilic, Silane A-174 has also been tested as an adhesion promoter before depositing parylene on platinum. This showed an increase in the

bonding strength in peel tests from 5 mN/cm (no treatment) to 1000 mN/cm (with Silane A-174) [10]. Also, annealing at high temperatures (≥200 °C) can improve the adhesion of parylene to platinum [24].

4.4. ADHESION OF PARYLENE TO PARYLENE

Parylene on parylene has shown to have good adhesion with no primer, which is caused by the fact that it prefers to bond with a clean hydrophobic surface [24]. However, since Silane A-174 has shown to increase the adhesion of parylene to platinum, it should also be tested on parylene since this layer is also exposed to the primer during the fabrication of the device.

4.5. METHODS

Cross cut tests were performed to evaluate the adhesion of different samples. This test was originally not developed to quantify the adhesion of layers, but rather to establish whether the adhesion of a certain layer is at an adequate level. A 5 x 5 grid was cut into the substrate forming 1 mm x 1 mm squares, according to ASTM D3359 guidelines. A polyester tape (Tape 8705B) with an adhesive force of 4.3 N/cm and 7.6 N/cm was applied and removed from the grid at 180°. The adhesion was rated according to the scale presented in Figure 4.2.

As previously mentioned, the devices should be resistant to the biochemical environment of the human body. This means that the adhesion between the layers should be unaffected in a PBS solution, which is commonly used to simulate biochemical environment of human tissue. Therefore the samples were also evaluated with cross cut tests after submerging in a PBS solution. The emerging was done at 37 °C for 2 days to test the initial response to PBS, and 55 °C for 10 days to evaluate the adhesion after an accelerated aging test. 55 °C is a common temperature used when performing accelerated aging test in a PBS solution for medical microdevices [25], and also in accordance with ASTM F1980-16 [26].

4.6. PROCESS FLOW

In order to test the adhesion of the three interfaces, different configurations of layers were prepared. These are shown in Figure 4.1. All of the samples were fabricated on 500 μm single side polished (SSP) wafers. For each of the configurations, several samples were used to test different adhesion promoting techniques. An overview of all the process steps for every sample can be found in Appendix C.

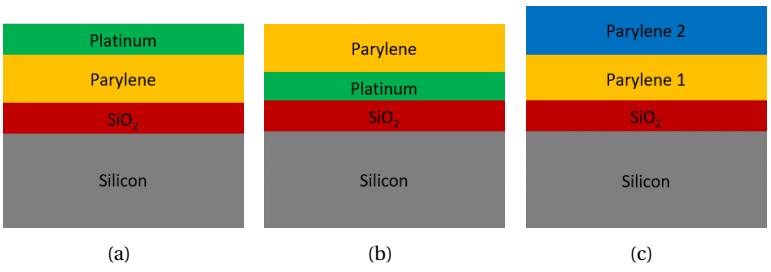


Figure 4.1: The different configurations that were used to evaluate the adhesion.

4.6.1. ADHESION OF PLATINUM TO PARYLENE

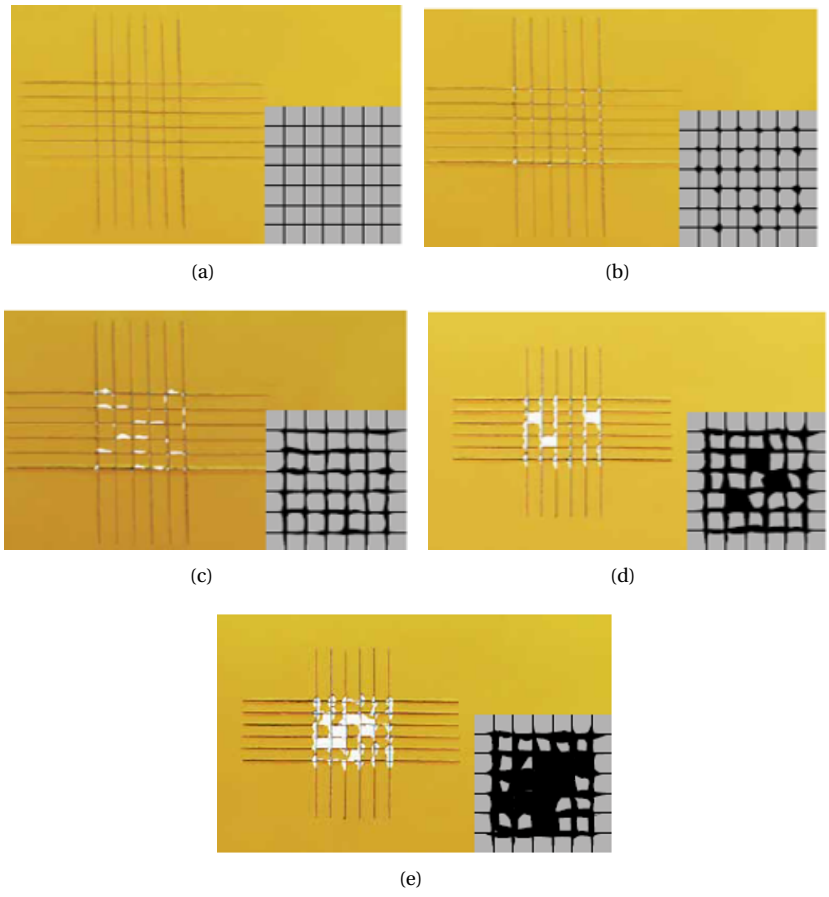
Three samples were used to study the adhesion of platinum to parylene (see Table 4.1). The process started with the deposition of 2 μm of PECVD oxide. Next, 2.5 μm of parylene was deposited using Silane A-174 as a primer to increase the adhesion between parylene and oxide. The samples were sputter etched with argon plasma (15 seconds) at 25 °C to increase the roughness. The increase in roughness was not measured. However, short sputter etching (100 seconds) with argon plasma has shown to increase the ten-point height from 3.9 nm to 25 nm on polyimide [27]. On two samples, 20 nm of titanium was sputtered. The titanium deposition was not performed on sample A2 to test its effect on the adhesion. Finally, the platinum was sputter deposited (600 nm). Sample A3 underwent an additional annealing step at 200 °C for 1 hour in nitrogen to evaluate the effect of annealing on this configuration.

4.6.2. ADHESION OF PARYLENE TO PLATINUM

Three samples were used to study the adhesion of parylene to platinum (see Table 4.2). The process started with the deposition of 2 μm of PECVD oxide. Next, 20 nm of titanium was sputter deposited, followed by 600 nm of platinum. On sample B1, 2.5 μm of parylene was deposited using Silane A-174 as a primer. The other two samples were annealed at 200 °C for 1 hour in nitrogen before the deposition of parylene. On sample B2, 2.5 μm of parylene was deposited with Silane A-174. On sample B3, 2.5 μm of parylene was deposited without Silane A-174.

4.6.3. ADHESION OF PARYLENE TO PARYLENE

Four samples were used to study the adhesion of parylene to parylene (see Table 4.3). The process started with the deposition of 2 μm of PECVD oxide. Next, 2.5 μm of parylene was deposited on sample C2 using Silane A-174 as a primer, and on sample C3 without using Silane A-174. Sample C1 and C4 underwent the same process steps as C2 and C3, respectively. However, the parylene deposition on C1 and C4 were preceded by a sputter etching step with argon plasma (15 seconds) at 25 °C to increase the roughness.



(a) (b) (c) (d) (e)

Figure 4.2: (a) ASTM Classification: 5B - The edges of the cuts are completely smooth; none of the squares of the lattice is detached; (b) ASTM Classification: 4B - Detachment of small flakes of the coating at the intersections of the cuts. A cross-cut area not significantly greater than 5 % is affected; (c) ASTM Classification: 3B - The coating has flaked along the edges and/or at the intersections of the cuts. A cross-cut area significantly greater than 5 %, but not significantly greater than 15 %, is affected; (d) ASTM Classification: 2B - The coating has flaked along the edges of the cuts partly or wholly in large ribbons, and/or it has flaked partly or wholly on different parts of the squares. A cross-cut area significantly greater than 15 %, but not significantly greater than 35 %, is affected; (e) ASTM Classification: 1B - The coating has flaked along the edges of the cuts in large ribbons and/or some squares have detached partly or wholly. A cross-cut area significantly greater than 35 %, but not significantly greater than 65 %, is affected [28].

4.7. RESULTS

The cuts were made by hand with a cross cutting tool (CC3000 by TQC) that contained six blades with 1 mm spacing in between them. The grids had to be evaluated before the peeling, because in some cases the

classification of the grid was not 5B before the peeling test. Table 4.1, Table 4.2 and Table 4.3 show the results of the cross cut tests. The arrows indicate how the classification of the cut changed before and after the peeling. Colors have been added to indicate either that the classification did not change after peeling (green), changed to the lowest classification (red), or changed to a classification in between 5B and 1B (orange). The images of all the cross cuts can be found in Appendix C.

4.7.1. ADHESION OF PLATINUM TO PARYLENE

The cuts went through both platinum (and titanium) and parylene, landing on the oxide. The results are displayed in Table 4.1. The cuts were already classification 4B before peeling. but no detachment was observed after peeling. This indicates very good adhesion of platinum to parylene. The fact that the classification was 4B before peeling is also a sign of very good adhesion, since the blades were not able to easily 'push' platinum and parylene layer away from oxide. Therefore, more manual force was required to make the cuts, which resulted in more delamination of the grid by only cutting (before peeling). Furthermore, no differences in adhesion were observed between the samples.

Table 4.1: The process flow and results of the cross cut tests of the platinum on parylene samples according to the ASTM D3359 guidelines.

	A1	A2	A3
PECVD oxide (2.0 µm)	✓	✓	✓
Silane A-174	✓	✓	✓
Parylene deposition (2.5 µm)	✓	✓	✓
Sputter etch (Argon)	✓	✓	✓
Titanium sputtering (20 nm)	✓		✓
Platinum sputtering (600 nm)	✓	✓	✓
Annealing at 200°C for 1h (N_2)			✓
No soaking *(4.3 N/cm)*	4B→4B	4B→4B	4B→4B
No soaking *(7.6 N/cm)*	4B→4B	4B→4B	4B→4B
2 days in PBS at 37 °C *(4.3 N/cm)*	4B→4B	4B→4B	4B→4B
2 days in PBS at 37 °C *(7.6 N/cm)*	4B→4B	4B→4B	4B→4B
10 days in PBS at 55 °C *(4.3 N/cm)*	4B→4B	4B→4B	4B→4B
10 days in PBS at 55 °C *(7.6 N/cm)*	4B→4B	4B→4B	4B→4B

4.7.2. ADHESION OF PARYLENE TO PLATINUM

The cuts applied to the samples went through the parylene layer and landed on platinum. The cuts were classification 5B before peeling. The results are displayed in Table 4.2. Using the same theory as before, in this case the cuts were easy to apply, indicating that the parylene was easily pushed away from platinum surface (so less adhesion then the platinum on parylene samples). This was confirmed with the soaking test in PBS for 10 days at 55 °C. In this test, the classification changed to 3B (on sample B1 and B3) and 2B (on sample B2) when using the 4.3 N/cm tape. When using the 7.6 N/cm tape, the classification changed to 1B (on sample B1 and B2) and 2B (on sample B2). This indicates that sample B3, which was annealed at 200 °C for 1 hour in nitrogen without Silane A-174, showed a better adhesion than the other samples.

4.7.3. ADHESION OF PARYLENE TO PARYLENE

The cuts applied to the samples went through both parylene layers and landed on the oxide. The cuts had different classifications before peeling. Significant differences in detachment after cutting (before peeling) were observed between the non-sputter etched (sample C1 and C4) and sputter etched samples (sample C2 and C3). The samples that underwent sputter etching showed more delamination after cutting (before peeling) of the bottom parylene layer from the oxide. However, after peeling no delamination was observed on the samples.

Table 4.2: The process flow and results of the cross cut tests of the parylene on platinum samples according to the ASTM D3359 guidelines.

		B1	B2	B3
PECVD oxide (2.0 µm)		✓	✓	✓
Titanium sputtering (20 nm)		✓	✓	✓
Platinum sputtering (600 nm)		✓	✓	✓
Annealing at 200°C for 1h (N_2)			✓	✓
Silane A-174		✓	✓	
Parylene deposition (2.5 µm)		✓	✓	✓
No soaking	*(4.3 N/cm)*	5B→5B	5B→5B	5B→5B
No soaking	*(7.6 N/cm)*	5B→5B	5B→5B	5B→5B
2 days PBS at 37 °C	*(4.3 N/cm)*	5B→5B	5B→5B	5B→5B
2 days PBS at 37 °C	*(7.6 N/cm)*	5B→5B	5B→5B	5B→5B
10 days PBS at 55 °C	*(4.3 N/cm)*	5B→3B	5B→2B	5B→3B
10 days PBS at 55 °C	*(7.6 N/cm)*	5B→1B	5B→1B	5B→2B

Table 4.3: The process flow and results of the cross cut tests of the parylene on parylene samples according to the ASTM D3359 guidelines.

		C1	C2	C3	C4
PECVD oxide (2.0 µm)		✓	✓	✓	✓
Silane A-174		✓	✓	✓	✓
Parylene deposition (2.5 µm)		✓	✓	✓	✓
Sputter etch (Argon)		✓			✓
Silane A-174		✓	✓		
Parylene deposition (2.5 µm)		✓	✓	✓	✓
No soaking	*(4.3 N/cm)*	4B→4B	5B→5B	4B→4B	3B→3B
No soaking	*(7.6 N/cm)*	4B→4B	5B→5B	4B→4B	3B→3B
2 days in PBS at 37 °C	*(4.3 N/cm)*	4B→4B	5B→5B	4B→4B	3B→3B
2 days in PBS at 37 °C	*(7.6 N/cm)*	4B→4B	5B→5B	4B→4B	3B→3B
10 days PBS at 55 °C	*(4.3 N/cm)*	4B→4B	5B→5B	4B→4B	3B→3B
10 days PBS at 55 °C	*(7.6 N/cm)*	4B→4B	5B→5B	4B→4B	3B→3B

4.8. CONCLUSION

Platinum on parylene showed very good adhesion, with no delamination when performing cross cut tests. No differences were observed when using a titanium adhesive layer or when performing an annealing step. Parylene on parylene also showed no delamination when performing the cross cut tests. Parylene on platinum has shown to be the most troublesome interface, with delamination occurring with cross cut tests after soaking PBS for 10 days at 55 °C. However, the adhesion is still sufficient for electrochemical characterization, which was the main goal of the adhesion evaluation. Furthermore, all the adhesion promoting techniques used can be integrated in the fabrication of the devices.

5

DRY ETCHING OF PARYLENE

5.1. INTRODUCTION

Parylene is resistant to dissolution by solvents below its melting point ($290^{\circ}C$) [29]. Although it is possible to dissolve parylene in certain chemicals such as chloronaphthelene and benzolyl benzoate at temperatures above $150^{\circ}C$, these chemical processes are not compatible with common lithography [29]. The only practical method to pattern parylene is by using plasma etching. This chapter discusses the optimization of a plasma based process to etch parylene semi-isotropically. This improves the step coverage of platinum in the next fabrication step. Like previously mentioned, sputtering is used to deposit platinum. This might result in not fully covered vias if the slope of the vias is too steep.

5.2. ANISOTROPIC ETCHING OF PARYLENE

Parylene etching processes usually only use O_2 plasma. It is known that O_2 plasma etches parylene anistropic. This is due to the fact that the degradation of parylene in an O_2 plasma primarily begins from their linear section. The etch rate of the aliphatic part of parylene molecules is higher than the etch rate of the aromatic rings [30]. Therefore, the etching process is anisotropic.

5.2.1. METHOD

The test wafers that were prepared for the anisotropic etching of parylene were DSP 400 μm. On the frontside 2 μm of oxide was deposited, followed by 2.5 μm of parylene. The parylene is always deposited on both sides on the wafer, and therefore the backside parylene of 2.5 μm was completely etched. The lithography on the frontside parylene was then performed, which was done with 6 μm of AZ9260. The parylene was etched using O_2 plasma (80 sccm). After landing on the oxide, the photoresist was stripped by performing an acetone spin clean.

5.2.2. RESULTS

Figure 5.1 shows the resulting slope after etching the first 2.5 μm of parylene with O_2 plasma. It can be seen that the slope is almost 90°. In order to avoid possible not fully covered parylene vias with platinum, a different etching recipe using CF_4 gas addition was investigated.

5.3. SEMI-ISOTROPIC ETCHING OF PARYLENE

It is known that introducing CF_4 gas to O_2 gas plasma will have an isotropic effect on the etching of parylene [31]. This is caused by the fact that the fluorine atoms enhance the opening of benzene rings in parylene. As a result, adding a small concentration CF_4 gas to O_2 gas will increase the ratio of linear to aromatic groups of the parylene, and will therefore make the etching process semi-isotropic. This effect was explored in this thesis to reduce the steepness of the parylene vias.
An example of the etch rate curve as a function of the CF_4 gas fraction in O_2/CF_4 based plasma is depicted in Figure 5.2. It was proposed in [32] that as the CF_4 gas concentration is increased, fluorocarbon polymer might be produced on the polymer surface by direct deposition from the CF_4 plasma. This fluorocarbon layer would function as a diffusion barrier for the reactive species, causing the polymer etch rate to decrease

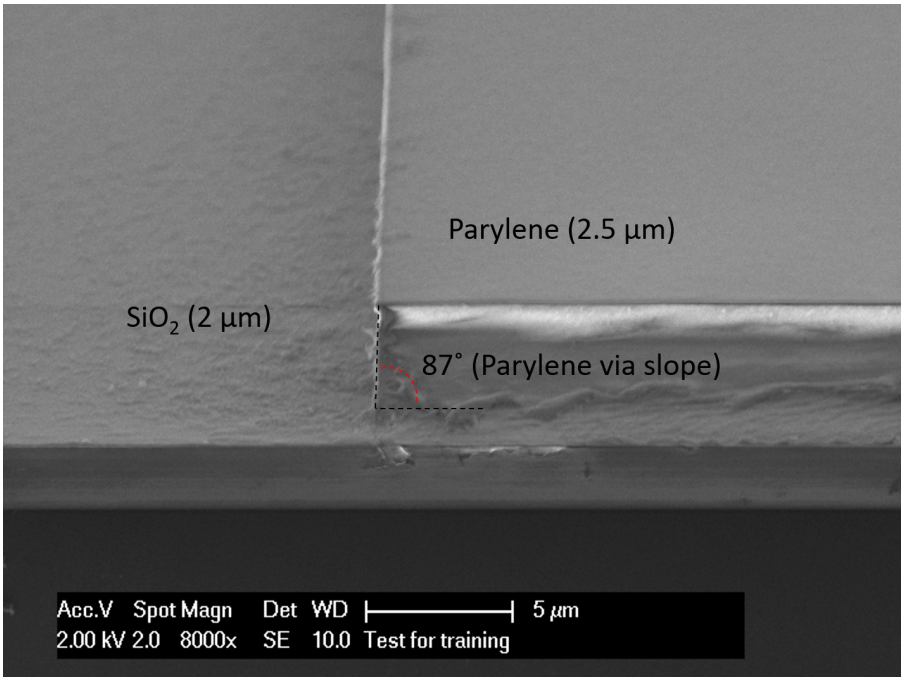


Figure 5.1: Resulting slope after etching 2.5 μm of parylene in 13 minutes (O_2 : 80 sccm, 500 W, 20 °C)

as the fluorinated gas concentration increases beyond a critical value. Figure 5.2 shows a maximum at a CF_4 gas fraction of 16%, however this maximum can vary based on process parameters (e.g. temperature, power, pressure) [33].

5.3.1. METHOD

Due to unavailability of the PECVD tool (Novellus), the same test wafers that were used for the anisotropic etching could not be prepared. Therefore, 500 μm wafers with 100 nm of thermal oxide on both sides were used (most practical solution at the time). This was followed by 2.5 μm of parylene, and backside parylene etching. The lithography on the parylene was the same as before (6 μm of AZ9260). Small gas flow rates of CF_4 (5 sccm and 10 sccm) were added to the O_2 plasma etch recipe. These smalls gas flows were chosen since only 2.5 μm of parylene had to be etched, and adding CF_4 gas increases the etch rate. Also, the fact that CF_4 etches oxide had to be taken into account when landing on oxide while overetching. Furthermore, the net gas flow was kept on 80 sccm in order to keep the total gas flow constant, resulting in CF_4 gas fractions of 6.67% and 14.30%. After etching parylene with these different gas flows the photoresist was stripped using an acetone spin clean.

5.3.2. RESULTS

The result of the etched structures with the two different O_2/CF_4 based plasmas recipes are displayed in Figure 5.4. These SEM images were obtained by manually breaking the wafer at the vias and looking at the cross-section. Different parameters of the resulting slopes were evaluated. Firstly, the vertical etch rate was calculated (Table 5.1). Since the etching was semi-isotropic, the lateral etch rate was determined to check the if the effect on the features size was within specifications, which can be a maximum increase of μm per side (the metallization that is patterned on the these vias is 20 μm bigger per side). The lateral etch rate was defined as follows:

$$R_{lateral} = \frac{(d_{before} - d_{after})/2}{t} \tag{5.1}$$

, where d_{before} is the distance between two vias in the photoresist mask before etching (90 μm), d_{after} is the shortest distance between two vias (at the top of the slope) after etching and t is the duration of the etch (3 minutes). A schematic cross-section after etching before the photoresist is stripped is depicted in Figure 5.3. An example of the vertical etching measurement between two vias is illustrated in Figure 5.5. The broken

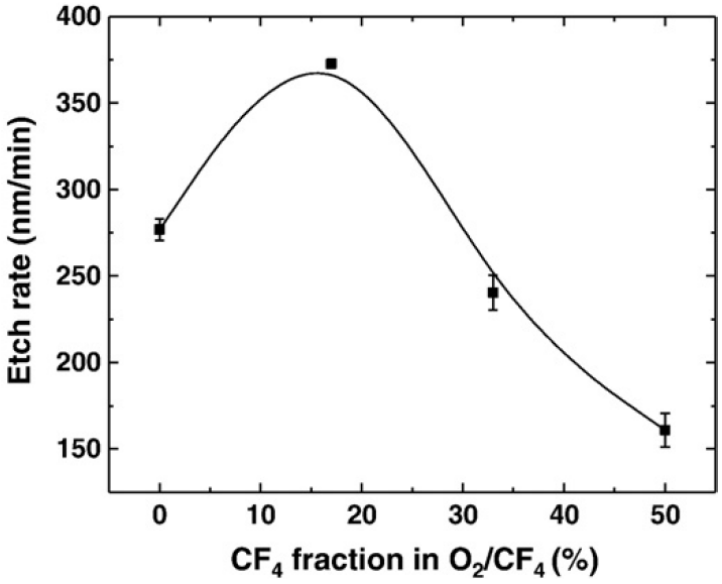


Figure 5.2: An example of the etch rate of parylene as a function of the CF_4 gas fraction in O_2/CF_4 based plasma (gas flow: 60 sccm, P=300 W) [31].

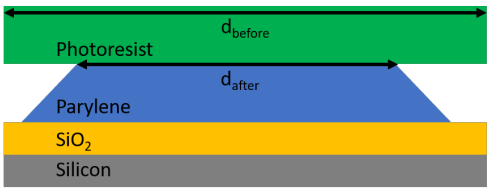


Figure 5.3: Schematic cross-section showing d_{before} and d_{after} after etching before the photoresist is stripped.

parylene layer in the middle is caused by the manual breaking. At last, the angle of the sidewall was calculated. Table 5.1 gives an overview of the parameters between the different etching recipes.
The vertical etch rate when only using O_2 : 80 sccm is the lowest as expected (~ 187 nm/min). When using O_2 : 75 sccm and CF_4 : 5 sccm the etch rate is significantly higher (~ 965 nm/min). However, when using O_2 : 70 sccm and CF_4 : 10 sccm, the etch rate is lower (~ 746 nm/min). By using the etch rate curve in Figure 5.2, the decrease in the etch rate indicates that a CF_4 gas fraction of 14.30% in this etching process is already above the CF_4 gas fraction that results in the maximum etch rate. The lateral etch rate did not show a significant difference when using CF_4 : 5 sccm compared to CF_4 : 10 sccm (~ 1553 nm/min and ~ 1356 nm/min). Consequently, the angles of the sidewalls were also similar (~ 45° and ~ 55°). However, the more desirable sidewall angle was achieved by using O_2 : 75 sccm and CF_4 : 5 sccm. The inlfuence on the thickness of the oxide when landing was very small. 11 nm of oxide was etched when using O_2 : 70 sccm and CF_4 : 10 sccm, and 23 nm of oxide was etched when using O_2 : 75 sccm and CF_4 : 5 sccm.

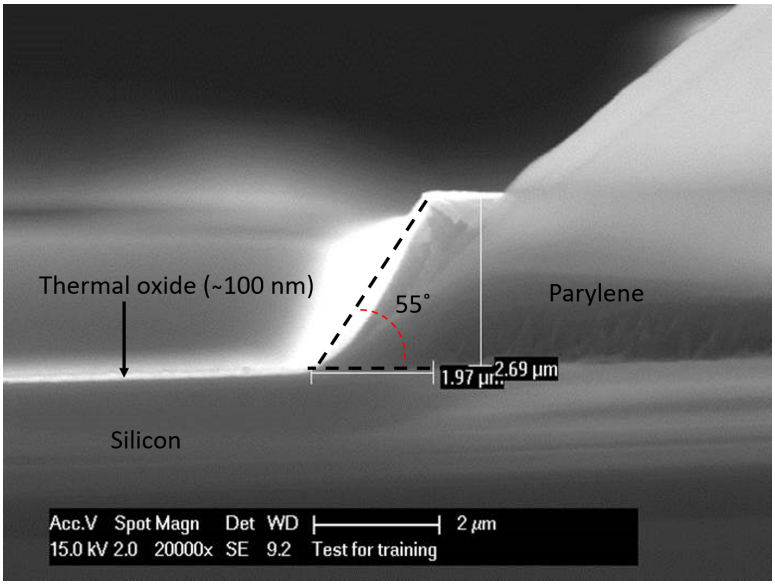
Table 5.1: Results of the parylene etching in plasma with different O_2 and CF_4 gas concentrations.

Gas flow rates	Vertical etch rate	Lateral etch rate	Sidewall angle
O_2 : 80 sccm; CF_4 : 0 sccm	~ 187 nm/min	~ 0 nm/min	~ 90°
O_2 : 75 sccm; CF_4 : 5 sccm	~ 965 nm/min	~ 1553 nm/min	~ 45°
O_2 : 70 sccm; CF_4 : 10 sccm	~ 746 nm/min	~ 1356 nm/min	~ 55°

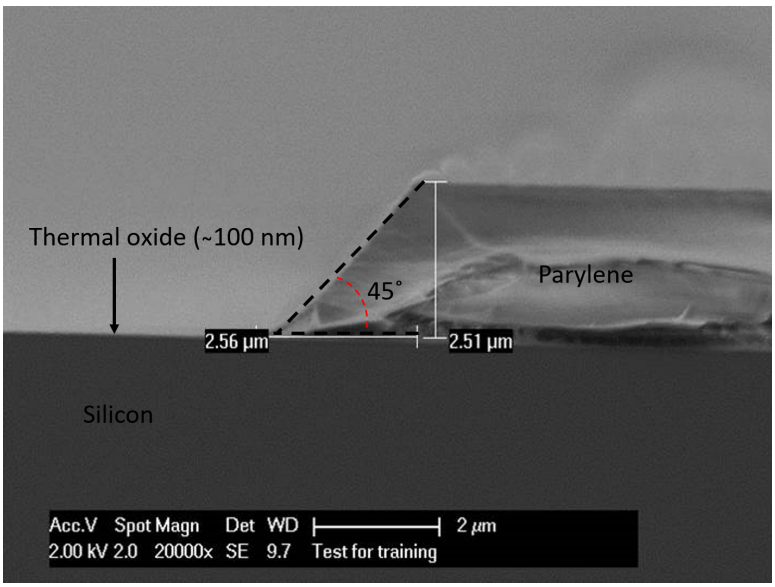
5.4. CONCLUSION

Etching of parylene with only O_2 based plasma results in ~ 90° sidewall angles. This can be changed to an angle closer to 45° by introducing CF_4 gas in the etching process, which improves the step coverage of platinum in the next fabrication step. The gas mixture that allowed to etch parylene with a sidewall angle of ~ 45°

contained 75 sccm O_2 and 5 sccm CF_4. Furthermore, an added advantage of introducing CF_4 gas was the increase of the vertical etch rate, which increased from ~ 187 nm/min to ~ 965 nm/min. This significantly speeds up the etching procudure. The isotropic effect when using O_2 : 75 sccm and CF_4 : 5 sccm resulted in a lateral etching of 4.7 μm per side when etching 2.5 μm of parylene. This is acceptable, since metallization patterned on these vias (bondpads) is 20 μm bigger per side, and thus will still fully cover the vias. The etching of the oxide when landing on oxide is negligible.



(a)



(b)

Figure 5.4: Side view of the slopes of the vias after etching with: (a) O_2 : 70 sccm and CF_4 : 10 sccm; (b) O_2 : 75 sccm and CF_4 : 5 sccm.

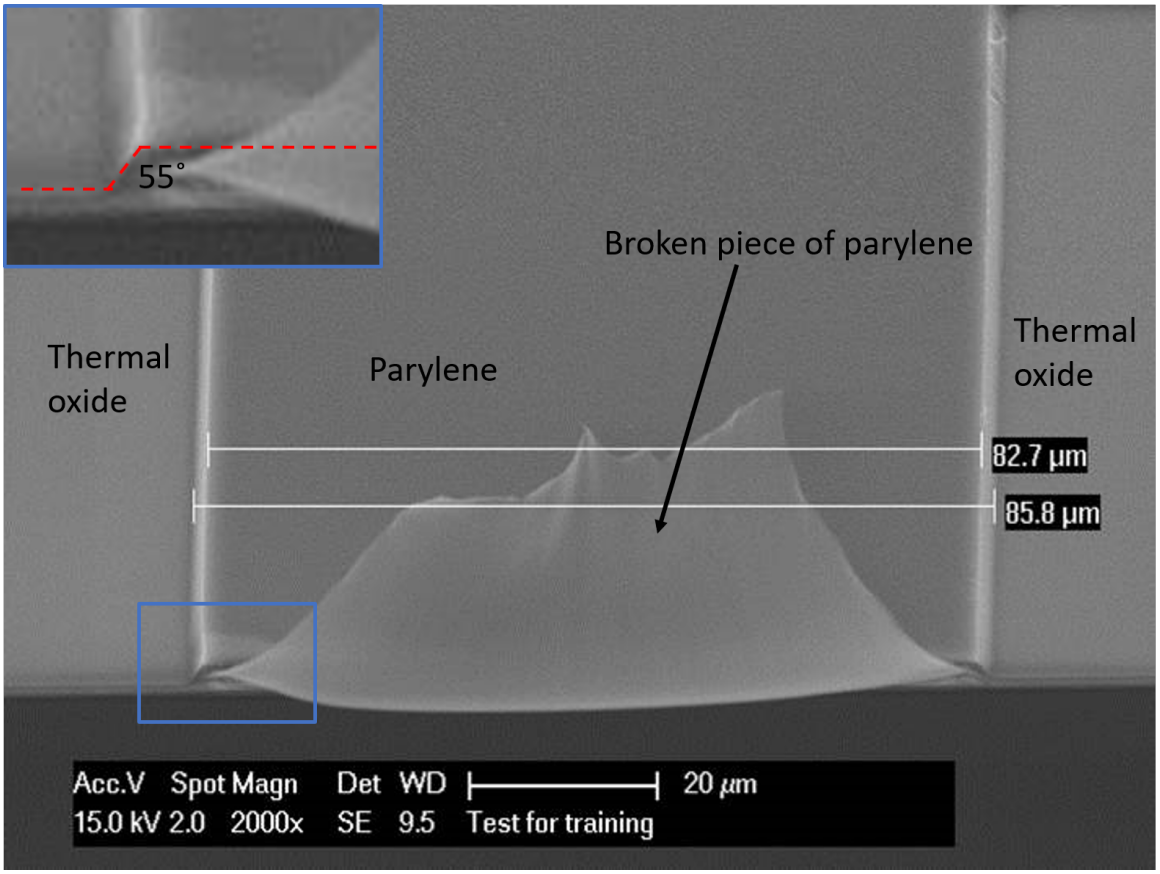


Figure 5.5: Resulting slope after etching 2.5 μm of parylene with O_2 : 70 sccm and CF_4 : 10 sccm.

6

DEPOSITION AND PATTERNING OF PLATINUM

6.1. INTRODUCTION

The deposition of platinum was done by sputtering and the patterning of platinum was done by ion milling. Ion milling has shown to have problems in obtaining the desired metallization. These problems are redeposition of platinum on the sidewall of the photoresist and the thermal effect on the photoresist. This chapter will discuss the deposition of platinum, the issues during the ion milling process, and the methods that were explored to solve these issues.

6.2. PLATINUM DEPOSITION

The platinum deposition by sputtering was done on a carrier wafer due to processing in a different cleanroom (tool that was used is only compatible with 6 inch wafers). The 4 inch process wafer was placed in a holder on the carrier wafer to prevent any contamination with platinum on the edge or the backside. This is important for further processing at EKL due to different contamination policies. However, the initial sputter depositions were not successful in preventing possible contamination due to movement in the holder. The solution to this problem is briefly discussed in Appendix A.
After 600 nm of platinum was deposited, a sheet resistance R_s of 0.264 Ω was measured. By using the sheet resistance R_s, the resistance R of the meandering interconnect can be calculated:

$$R = R_s \cdot \frac{L}{W} = 0.264 \cdot \frac{166478}{20} = 2.20\,k\Omega \tag{6.1}$$

, where L is the length of the meandering interconnect (166478 μm) and W is the width of the meandering interconnect (20 μm). In Chapter 7 the theoretical resistance of the meandering interconnect will be compared with the measured resistance before rolling and bending of the membrane.

6.3. ION MILLING

During the ion milling process, two problems can occur which have undesired consequences for the metallization. A known problem that ion milling introduces is the redeposition of platinum on the sidewalls of the photoresist [34]. After removing the photoresist, this results in fence-like structures. An example of platinum fence formation is shown in Figure 6.1. Since the fences are platinum based, they are hard to removed. If another metal was used and patterned by using ion milling, a short dip in a chemical etchant might improve the profile by etching away the fences. However, in the case of platinum this is not a practical solution due to the lack of a well-defined and controllable wet etching process of platinum on parylene [35].
Another problem with the ion milling process is the thermal effect (burned and/or crosslinking) on the photoresist. Furthermore, since this process also had to be done on a carrier wafer (ion milling tool that was used is only compatible with 6 inch wafers), this effect is even stronger due to less cooling. This thermally modified photoresist is hard to remove, since the burning and/or crosslinking of the photoresist reduces its solubility. Due to the parylene, oxygen plasma can not be used to strip the photoresist. The main photoresist stripping

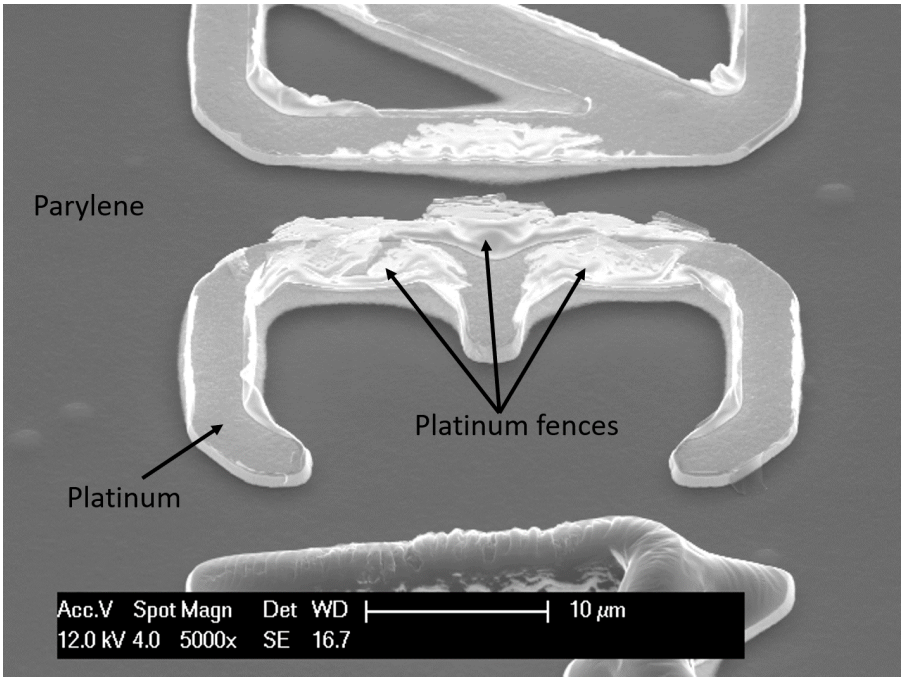


Figure 6.1: An example of platinum fence formation after stripping the photoresist after ion milling.

method that is used (and preferred) in this process is an acetone spin clean. Acetone is commonly used to strip photoresist when parylene is exposed [24].

6.3.1. METHOD

In order to avoid to the redeposition of platinum on the sidewalls and reduce the thermal modification of the photoresist, several adjustments were made to the lithography process on platinum. In theory, thicker photoresist, is less likely to burn due to more volume. Therefore, the photoresist thickness was increased to 6 μm (AZ9260) as a first test.

To address the formation of fences at the sidewalls of the photoresist, reflow was performed. Reflow is a post lithography bake to round off the corners of the photoresist and reduces the steepness of the slope. This will cause more of the platinum to be redeposited on top of the photoresist instead of on the sidewalls, which reduces fence formation.

The test wafers used were 400 μm DSP. 2 μm of oxide was deposited, followed by 2.5 μm of parylene. Next, 200 nm of titanium was deposited. Titanium was chosen over platinum for more practical and time efficient processing (no processing in Eindhoven required). Lithography on the titanium was done with 6 μm (AZ9260).

In order to check the slopes of the different profiles of the photoresist resulting from different reflows, cross-sections were analysed before ion milling. The cross-sections were obtained by manually breaking the samples after reflow. The breaking line was chosen perpendicular to the interconnects of the IDEs since these contain the smallest structures (20 μm width). They also contain the smallest distance between two structures (20 μm spacing). Therefore, this area will see the most fence formation if redeposition on the sidewall of the photoresist is occurring.

Figure 6.2 shows the cross sections of the IDE interconnects after different reflows. Figure 6.2(a), Figure 6.2(b), and Figure 6.2(c) all show similar shapes after reflow. However, the peak of the profile of Figure 6.2(a) compared to Figure 6.2(b) and Figure 6.2(c) show a ~0.9 μm and a ~0.8 μm difference in height, respectively. The effect when performing reflow in a convection furnace was also tested to evaluate if a more desired slope can be achieved. The result is displayed in Figure 6.2(d). The corner of the profile is still visible and the slope is not fully rounded. Since parylene is already present on the wafer, the reflow time and temperature should be minimized. Therefore, reflow at 110 °C for 30 seconds was chosen to perform ion milling (Figure 6.2(a)). Taking the minimal differences into account between Figure 6.2(b) and Figure 6.2(c), reflow at 110 °C for one minute was also tested to perform ion milling. The ion milling result using reflow at 110 °C for one minute was used to compare to the reflow at 110 °C for 30 seconds to check if the difference in the profile have an

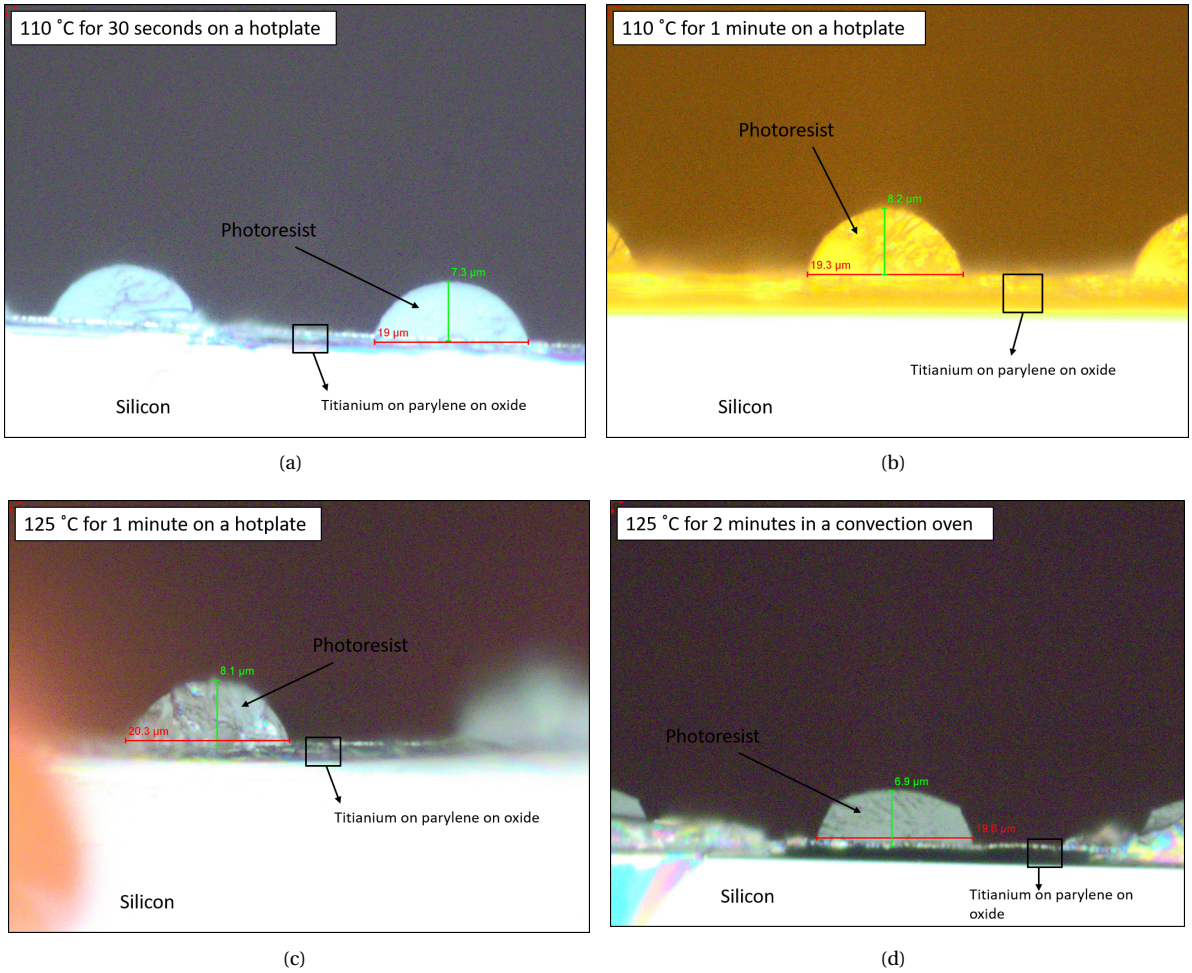


Figure 6.2: Different reflow profiles of 6 μm of AZ9260 on titanium: (a) at 110 °C for 30 seconds on a hotplate; (b) at 110 °C for 1 minute on a hotplate; (c) at 125 °C for 1 minute on a hotplate; and (d) at 125 °C for 2 minutes in a convection oven. The blurring on certain areas of the images is caused by the manual breaking, which is not perfectly straight.

influence on the fence formation.

6.3.2. RESULTS

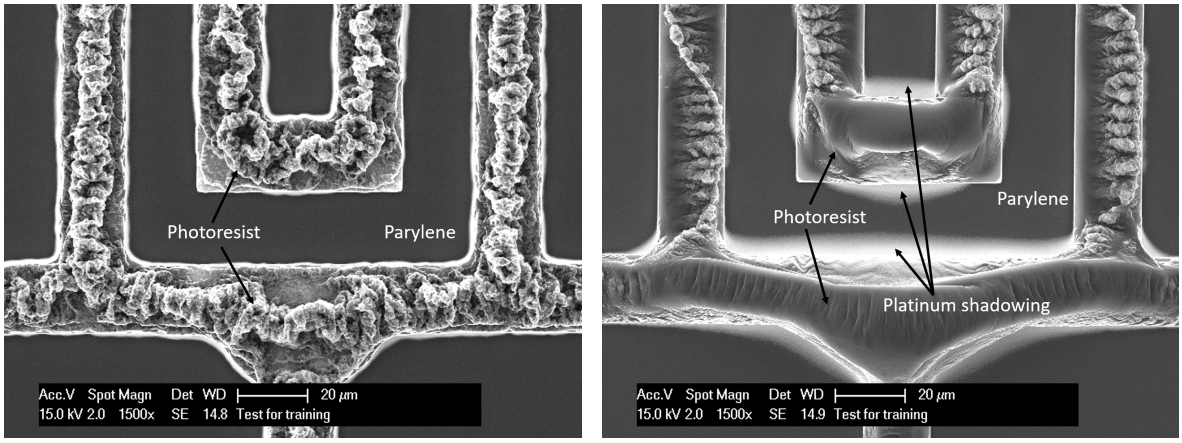
As described in Chapter 2, 600 nm of platinum followed by 20 nm of titanium was etched by ion milling. The results after ion milling at the IDE splitting are displayed in Figure 6.3. The peak height of the photoresist that was reflow at 110 °C for 30 seconds is ~ 0.9 μm higher. This difference leads to significant differences after ion milling. Figure 6.3(a) (peak height 7.3 μm) shows that the structure of the photoresist is very different compared to Figure 6.3(b) (peak height 8.2 μm) . Secondly and more importantly, Figure 6.3(b) shows platinum residues in certain areas at and around corners. This platinum 'shadowing' is caused by the incident angle of the ions during the ion milling process and the peak height of the photoresist. This can lead to failure of the IDE measurements since these platinum residues can cause short circuits (see Figure 6.4(a)).

6.3.3. PHOTORESIST REMOVAL

In order to remove the photoresist after ion milling, several resist stripping methods were explored.

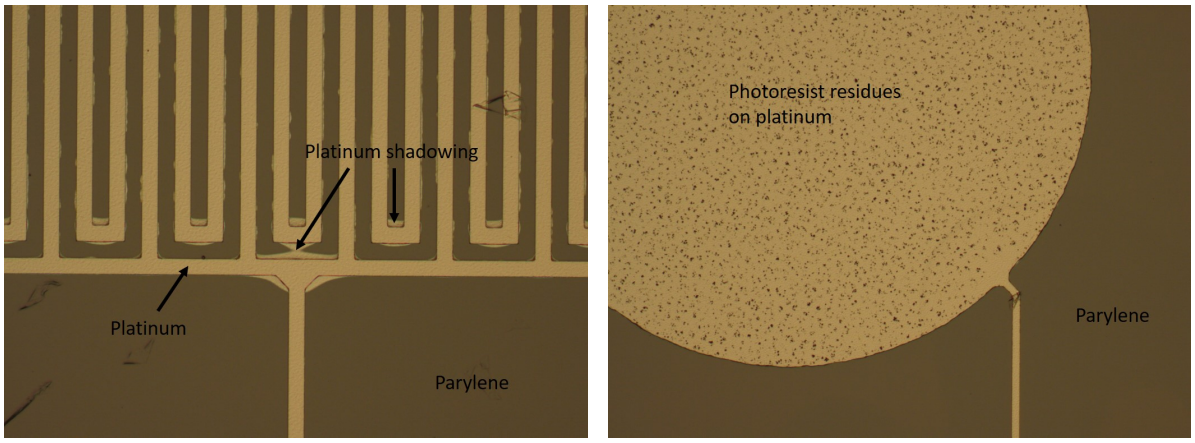
ACETONE SPIN CLEAN AND ULTRSONIC BATH

In this fabrication process, the preferred method to removed photoresist is with acetone. However, several acetone spin treatments had no visible effect on the photoresist. Therefore, the devices where soaked in an acetone ultrasonic bath at 40 °C for ~ 3 hours. This also had no visible effect on the photoresist.



(a) (b)

Figure 6.3: Results directly after ion milling using 6 μm of AZ9260: (a) after the reflow at 110 °C for 30 seconds on a hotplate; (b) after the reflow at 110 °C for one minute on a hotplate.



(a) (b)

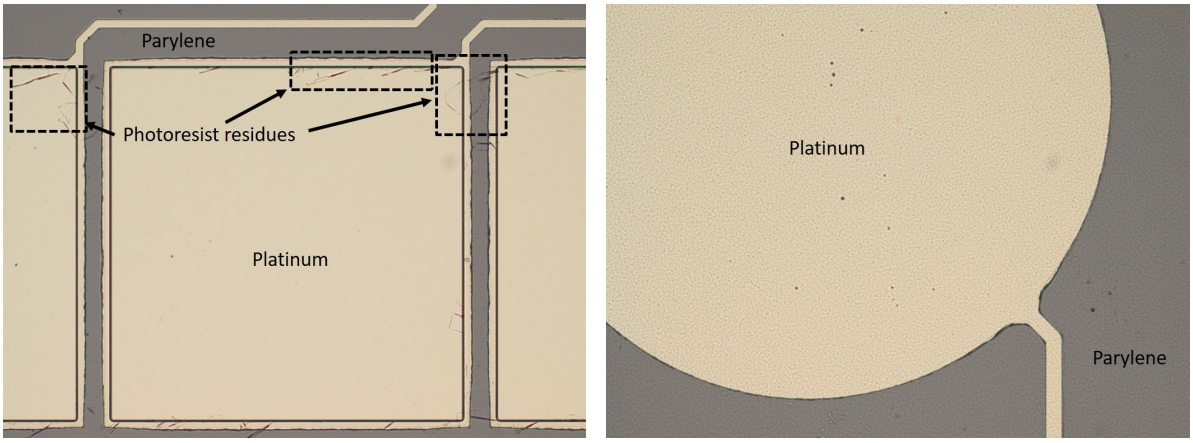
Figure 6.4: Results of photoresist removal with NMP at 70 ° C in an ultrasonic bath for ~ 3 hours: (a) at the IDEs; (b) at an electrode.

NMP AND ULTRASONIC BATH

Based on these results, a more aggressive photoresist stripping method had to be used. Since parylene limits methods such as high power O_2 plasma treatment and HNO_3, other options had to be explored. This led to soaking in NMP at 70 °C for ~ 2 hours. Some photoresist at the side was partially removed, however the metallization was still completely covered with photoresist. The wafers where then soaked in NMP at 70 °C in an ultrasonic bath for ~ 3 hours. This removed the majority of the photoresist on the interconnects (Figure 6.4(a)), but still left residues on the bigger structures such as the electrodes and bondpads (Figure 6.4(b)).

OXYGEN PLASMA TREATMENT

The remaining photoresist residues were primarily on the electrodes and bondpads. Since these would be reopened later in the process, they would be etched away. However, there would be residues at the edge of the electrodes and bondpads (under the second parylene layer). In order to minimized these residues, an additional directional oxygen plasma treatment was performed (O_2: 70 sccm, 60 W) for 2 minutes. This removed the big residues from the bondpads and electrodes (see Figure 6.5), however it also etched ~ 400 nm of parylene. This etching made the NMP delamination visible under the microscope, since the parylene was thinner. This is displayed in Figure 6.6. Furthermore, after exposing to NMP, a color change was visually observed. It is visible that the delamination is around the electrode, but also under the electrode. Therefore, the observed delamination was most likely between the first parylene layer and the oxide.



(a) (b)

Figure 6.5: Results of photoresist removal with NMP at 70 °C in an ultrasonic bath for ~ 3 hours and 2 minutes of oxygen plasma etching (O_2: 70 sccm, 60 W): (a) at a bondpad; (b) at an electrode.

6.3.4. CONCLUSION

Increasing the thickness of the photoresist from 4 μm to 6 μm did not improve the stripping of the photoresist. Reflow causes an increase of the peak height on small structures, which can result in platinum residues if the peak height is more than ~ 7.3 μm. This is caused by the incident angle of the ions during the ion milling process. Furthermore, reflow of 30 seconds and 60 seconds at 110 °C did still lead to fence formation. The thermally modified resist after patterning can be partially removed from the bondpads and electrodes by soaking in NMP at 70 ° C for ~ 3 hours. Directional oxygen plasma (O_2: 70 sccm, 60W) was used for 2 minutes to further reduce these residues, while also sacrificing 400 nm of parylene. Exposure to NMP also causes delamination. As a result, a different approach without NMP treatment was investigated.

6.4. TWO-STEP ION MILLING PROCESS

The previous approach one-step did not result in completely residue and fence free patterned platinum metallization and parylene delamination from oxide was observed. Therefore a different method was proposed where the ion milling is done in two steps. This process is displayed in Figure 6.7. During the first ion milling step, ~ 550 μm of platinum is etched, leaving ~ 50 nm of platinum and ~ 20 nm of titanium. At that point, the parylene is still covered with platinum.Therefore, more resist stripping method are allowed, such as high power oxygen plasma treatment at low temperature. After stripping the photoresist with high power oxygen plasma, the remaining ~ 50 nm of platinum and ~ 20 of titanium can be etched.

6.4.1. METHOD

For more time efficient processing, the test wafers that were used to evualate the two-step ion milling process were prepared in a different cleanroom (where the ion milling is performed). 6-inch silicon wafers with 600 nm of platinum on 20 nm of titanium on parylene were prepared. The platinum was coated with 1 μm of HPR504. A different mask was used with similar feature sizes (~ 20 μm). During the first ion milling step, the etch rate was overestimated, resulting in only etching of 364 nm of platinum. However, this would only result in thinner platinum and not influence the result of the process. After the first ion milling step, the resist was stripped using high power O_2 plasma with temperature control (T<100 °C). Lastly, the remaining platinum and titanium was etched.

6.4.2. RESULTS

The results of the two-step ion milling process are displayed in Figure 6.8. Figure 6.8(a) shows no residues after oxygen plasma barrel strip. Figure 6.8(b) shows patterned platinum on parylene with no photoresist residues or platinum fences. A difference between the patterned platinum resulting from the two step ion milling process compared to using one the step ion milling process is that the surface roughness of the platinum might be rougher. However, a rougher surface will only be beneficial for the structural stability of the device [36]. Additionally, since the photoresist was completely removed, thinner photoresist could be used

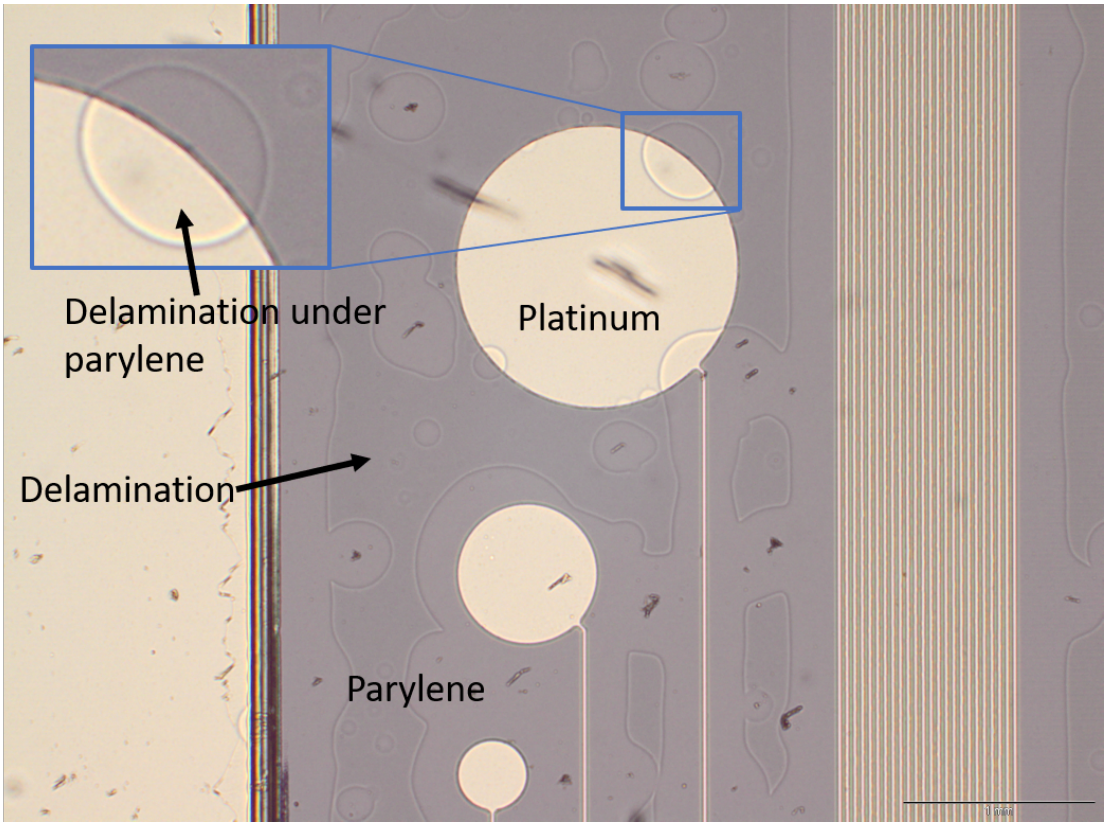


Figure 6.6: Delamination under parylene caused by NMP visible after 2 minutes of oxygen plasma etching (O_2: 70 sccm, 60 W).

(1 μm). This avoided the previously mentioned platinum shadowing and any fence formation caused by redeposition of platinum on the sidewall.

6.4.3. CONCLUSION

The two step ion milling solves the issues of platinum patterning on parylene. After the first ion milling step, the photoresist was stripped using O_2 plasma. This did not have any undesired consequences for the parylene layer. After the second ion milling step, a clean and fenceless metallization was observed. A disadvantage of this method compared to the one step ion milling process is the processing time.

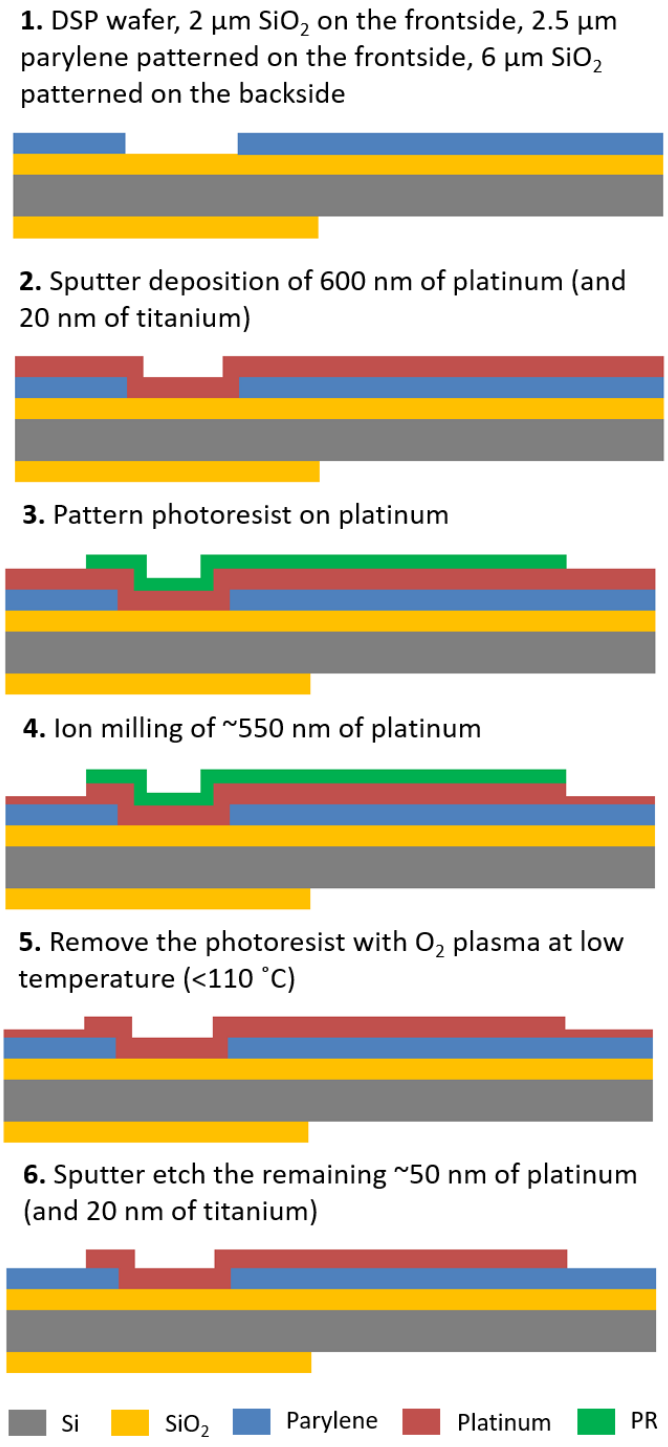
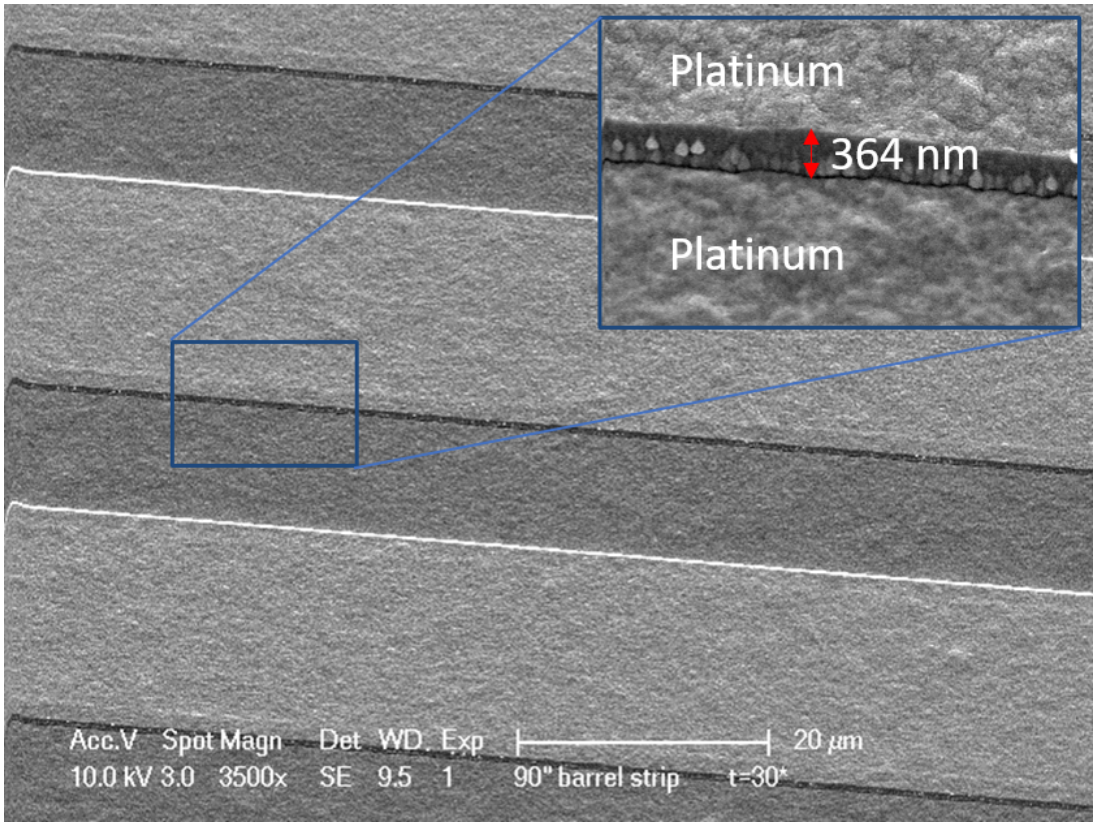
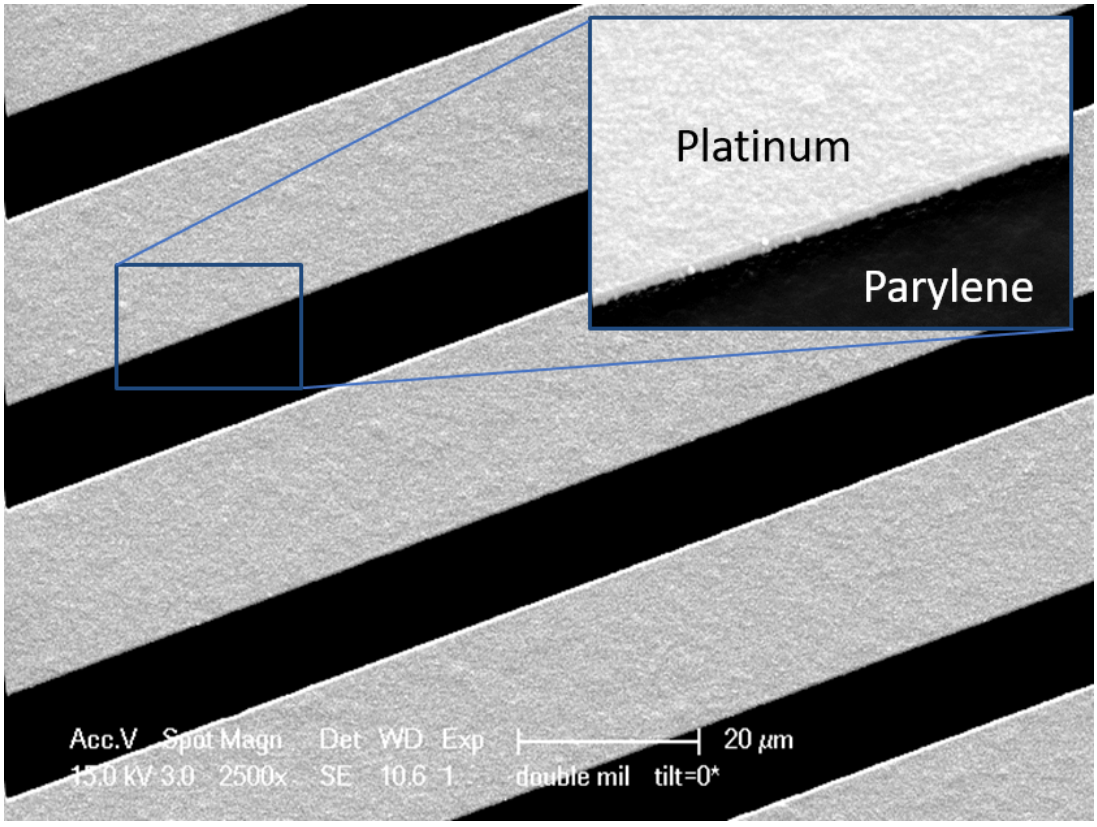


Figure 6.7: The two step ion milling process.



(a)



(b)

Figure 6.8: Results of the two step platinum ion milling process: (a) after the first ion milling step and stripping of the photoresist with oxygen plasma; (b) after the second ion milling step.

7

INTEGRATION AND RESULTS

7.1. INTRODUCTION

This chapter discusses the integration of the technology modules from the previous chapters with step 1 to step 6 of the initial process flow, along with important details of these process steps. Next, the final process steps are be discussed. These consist of the DRIE of the silicon from the backside, the frontside parylene etching and the final wet etching step to remove the oxide and the titanium hardmask to make the device partly flexible. Finally, the results of the electrical measurements before rolling, after rolling and after bending of the flexible interconnects are discussed.

7.2. PROCESS INTEGRATION INTO STEP 1 TO STEP 6

The technology modules from Chapter 3, Chapter 4, Chapter 5 and Chapter 6 were integrated into the initial process flow from Chapter 2 where possible. The next sections describe the integration into step 1 to 6 of the initial process flow, as well as the additional details for these process steps. The full process flow can be found in Appendix B.

7.2.1. STEP 1 & 2: FRONTSIDE SILICON DIOXIDE AND BACKSIDE SILICON DIOXIDE HARDMASK

Using the results from Chapter 3, the process started with the deposition of 6 μm of oxide on the backside of the wafer. The wafer was then flipped and alignment marker lithography and etching was performed on the frontside. Next, an oxygen plasma strip (400 sccm, 1000 W) and a cleaning procedure (HNO_3 99% and HNO_3 69% for 10 minutes) were performed.
The wafer was then flipped and backside lithography and oxide plasma etching were done for the DRIE mask. The thickness of backside SiO_2 could have been less than $6\mu m$. However, this backside lithography process was successful in past processes and was therefore not changed. The same oxygen plasma strip and cleaning procedure were repeated.
Finally, 2 μm of oxide was deposited on the frontside. As previously mentioned, this processing order avoids any direct contact of the backside silicon with the handling fork of the PECVD tool (Novellus), and therefore solves the masking problem during the DRIE step later in the process.

7.2.2. STEP 3: FIRST PARYLENE DEPOSITION AND PATTERNING

The next step was the deposition of parylene (CVD), in which 2.5 μm of parylene is deposited on both sides of the wafer (using Silane A-174 as a primer). After deposition, the wafer was flipped and the parylene on the backside was completely removed by etching using an oxygen plasma (80 sccm, 500 W, 20 °C). The frontside was cleaned with an acetone spin clean and the parylene on the frontside was coated with 6 μm of AZ9260. After exposure and developing, the vias were etched using the optimized recipe (O_2: 75 sccm, CF_4: 5 sccm) from Chapter 5 to achieve a 45° slope. After the etching, the resist was stripped with an acetone spin clean.

7.2.3. STEP 4: PLATINUM DEPOSITION AND PATTERNING

The new holder at Philips (Appendix A) was used to deposit 20 nm of titanium, followed by 600 nm of platinum. This resulted in no platinum (and titanium) deposition at edges (and backside) of the wafer. This

solves contamination issues when further processing the wafers in EKL.
Chapter 6 discussed the two-step ion milling process, which results in clean and fenceless platinum metallization. However, it was not possible to incorporate the two-step ion milling process into the final fabrication flow due to the unavailability of the ion milling tool. Therefore, the wafer which was processed using the initial ion milling process (which used NMP in an ultrasonic bath at 70 °C to remove the photoresist) was used. As a result, it was decided not to perform any reliability tests in a saline solution. Also, no further adhesion promoting techniques from Chapter 4 such as annealing at 200 °C for 1 hour in nitrogen or sputter etch were performed. The only process modification was the addition of an extra exposure step in the lithography to reopen the alignment markers. This was done to prevent any alignment issues that can occur during the final exposure.

7.2.4. STEP 5: SECOND PARYLENE DEPOSITION

After the platinum is patterned, the second parylene layer of 2.5 μm (using Silane A-174 as a primer) is deposited. This deposition was followed by the same process steps as the first parylene deposition, which are the parylene backside etching and the frontside acetone spin cleaning.

7.2.5. STEP 6: TITANIUM DEPOSITION AND PATTERNING

The patterning of the second parylene layer (opening of the electrodes, bond pads and frame) was done by using a titanium hardmask. Aluminum could also have been used as a hardmask instead of titanium, however, using an aluminum mask to etch parylene left aluminum residues on the parylene in past processes. Therefore, titanium was used in this process as a hardmask to pattern the parylene. The titanium deposition (200 nm) was done at low temperature (25 °C) due to the presence of parylene. After lithography, the titanium was dry etched (Trikon Omega 201). To make sure there were no residues, the wafer was dipped in Triton X-100 to reduce the surface tension and wet etched in a titanium etchant. This etchant consisted of 1 part H_2O, 1 part H_2O_2 31% and 1 part NH_4OH 28%. After this, the resist was stripped with an acetone spin clean. This left residues at the edge of the structures that were removed by a short low power oxygen plasma (60 seconds, 70 sccm, 60 W).

7.3. FINAL FABRICATION STEPS

The final process steps after partly integrating the technology modules into the initial process flow included the backside silicon DRIE process, opening of the bond pads, electrodes and bridges to the frame by etching parylene on the frontside of the wafer, and the removal of the titanium hardmask and oxide on the backside.

7.3.1. STEP 7: BACKSIDE SILICON ETCH

DRIE was used to etch 400 μm of silicon from the backside of the wafer. This etching process was first performed on a test wafer. This test wafer contained 2.5 μm of parylene on 2 μm of oxide on the frontside, and 6 μm of patterned oxide (hardmask) on the backside of the wafer. After this etching procedure, several membranes were broken. This was an issue, since in the actual device platinum interconnects would break and be exposed in the chamber of the tool, which is not allowed. Therefore, the etching was performed on a transport wafer. However, in order to obtain similar cooling conditions as for the process wafer, a temporary adhesive was used (Crystalbond^{TM} 555) between the transport wafer and the process wafer. This conductive wax was softened and applied on the transport wafer at ~ 50 °C (on a hotplate). When the wax was softened, the process wafer was flipped and applied on the transport wafer. The process and the transport wafer where then cooled down to increase the bonding strength of the wax. Furthermore, four pieces of tape were applied on the edge of the wafer to avoid any shifting and misalignment during the DRIE process.
The DRIE process only resulted in several broken membranes. However, separating the wafers was not possible with the softening on a hotplate and soaking in the recommended solvents (water or acetone). Furthermore, the softening on a hotplate caused cracking of the oxide (Figure 7.1). Therefore, the wafers were separated by manually applying external force. This caused many of the membranes to break. On certain dies the titanium mask was also peeled off with the wax. And example of such a die is depicted in Figure 7.2. It does however show that the DRIE process was successful.

7.3.2. STEP 8: PARYLENE ETCHING

The next step was to etch the parylene to reopen the bond pads and electrodes using the titanium hardmask. This mask also contained the bridges around the device, which suspends it in the frame. 5 μm of parylene

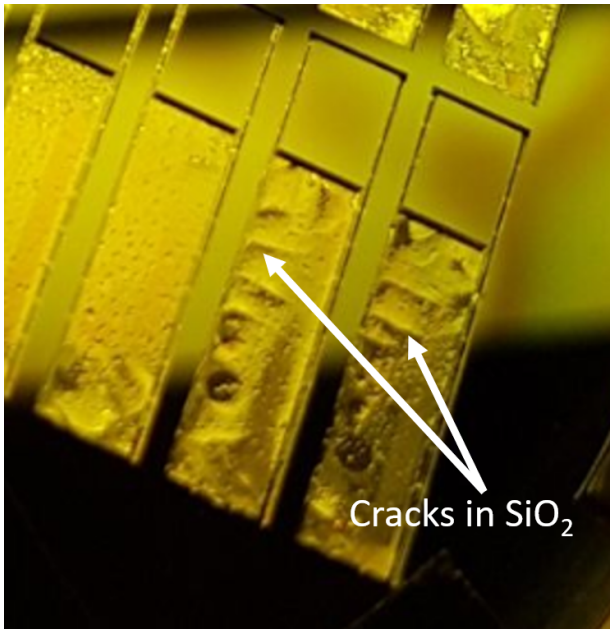


Figure 7.1: The backside of the wafer after the DRIE process and resoftening on a hotplate.

was etched using an oxygen plasma (70 sccm, 60 W, Alcatel GIR300 F etcher). Since this tool lacks a proper cooling system, a cooldown was performed after the etching to prevent any further breaking of the oxide due to abrupt temperature changes. This cooldown consisted of a 30 minutes cool down in the etch chamber with no gasses, followed by a few minutes with helium gas flow (10 sccm). The results after the etching of the parylene can be seen in Figure 7.3. The opened platinum does not contain any photoresist residues due to the overetching. However, it is clearly visible that there are still photoresist residues around the edges of the bond pads and electrodes. These residues were already visible after the second parylene deposition.

7.3.3. STEP 9: WET ETCHING OF OXIDE AND TITANIUM

The final step in the process was to remove the titanium hardmask and the oxide etch stop layer. The oxide could also have been removed before step 7. An advantage of this processing order would be less stress during the reopening of the bond pads and electrodes. However, since the oxide already contained cracks during the separation process of the transport wafer and the process, the stress was already relieved. Furthermore, the etching of the oxide before the reopening could not have been performed wet (BHF 1:7), since the titanium would also be etched away. Additionally, wet etching the titanium and the oxide simultaneously reduces the processing time.

Before the wet etching process, the wafer was emerged in Triton X-100 to reduce the surface tension. The wafer was then emerged in BHF 1:7. The 200 nm of titanium was removed after ~ 60 seconds. The oxide was removed after ~ 7.5 minutes. The wafer was left under a fume hood for over 12 hours to dry.

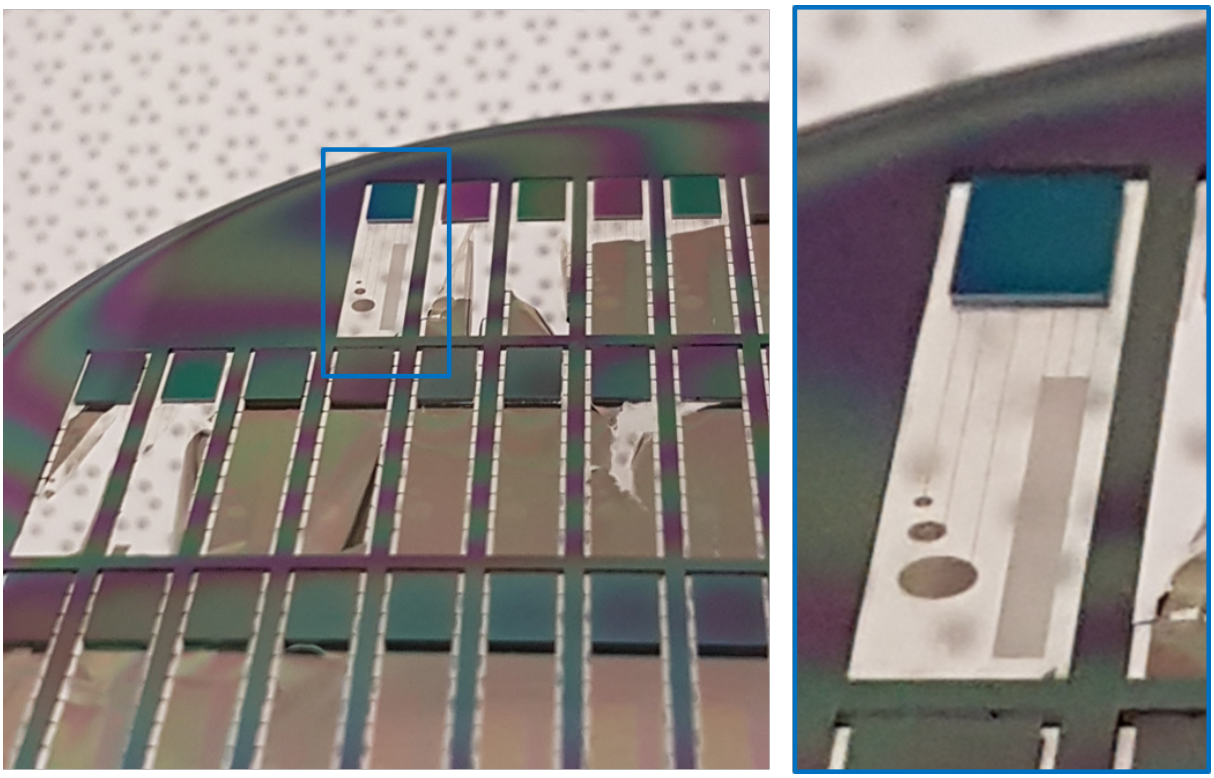
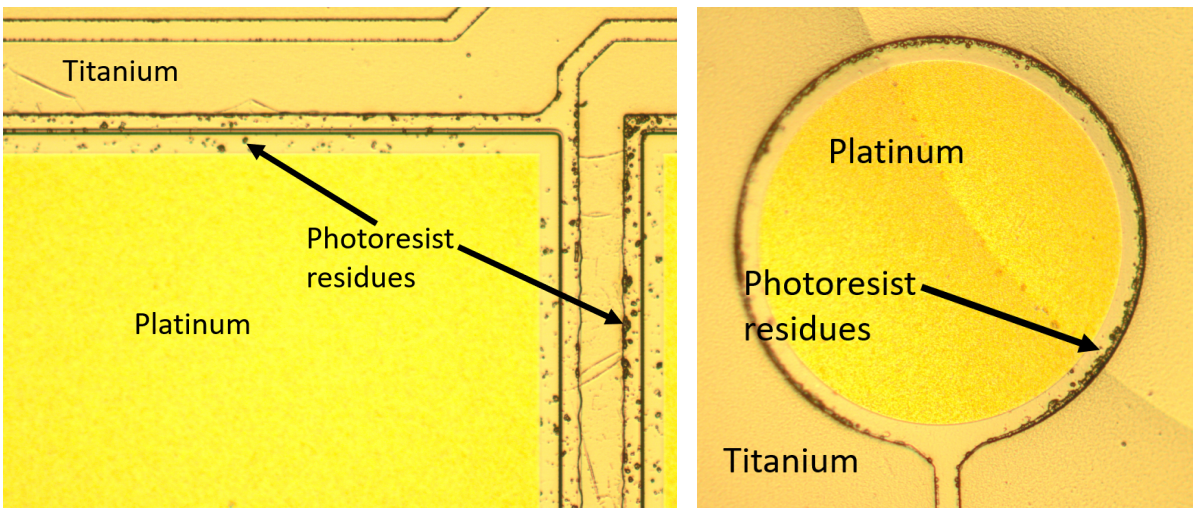


Figure 7.2: The backside of the wafer after the DRIE process and separation of the process wafer from the transport wafer.



(a) (b)

Figure 7.3: Results after 28 minutes of oxygen plasma etching (O_2: 70 sccm, 60W): (a) at a bondpad; (b) at an electrode

7.4. RESULTS

After the fabrication of the test devices, the flexible meandering interconnect was tested both electrically and mechanically. One of the main objectives, as mentioned in Chapter 1, is to roll the flexible interconnects to an inner diameter < 1 mm while measuring the correct resistance. Also, bending tests were performed to evaluate the minimum bending radius.

7.4.1. ELECTRICAL MEASUREMENTS

In Chapter 6, the resistance of the meandering interconnect was calculated to be 2.20 $k\Omega$. Before performing rolling or bending tests, the resistance of the meandering interconnect was measured with a mechanical probe station (Cascade Microtech). This measurement tool was preferred over a multimeter to avoid any failures due to handling. Table 7.1 shows the resistance measurements of the devices before rolling the flexible interconnects. This resistance measurement (2152.8 Ω, $\sigma = 8.3$) showed that the meandering interconnect of the comb-meander structure was conducting and no short circuits were present.

Table 7.1: The resistance measurements (n=28) of the meandering interconnect before rolling, after rolling and after bending.

	Before rolling	**After rolling**	**After bending**
R (Ω)	2152.8 ($\sigma = 8.3$)	2151.8 ($\sigma = 8.2$)	2160.9 ($\sigma = 14.1$)

7.4.2. ROLLING AND BENDING TESTS

In order to accurately test the flexibility of the thin film flexible interconnects, a precise evaluating method is required to bend the flexible interconnects around a small radius (of e.g. a rod or wire). However, this is a challenging task since it is difficult to bend the flexible interconnects accurately due to their size and thickness. Therefore, a more practical method that provides information about the mechanical performance of the device is to roll the flexible interconnects (in this case with an inner diameter of <1 mm) without a supporting structure (rod or wire). Furthermore, the flexible interconnects can also be bend with a tweezer, approaching a bending radius close the thickness of the flexible film (~6 μm).
The device was rolled (with tweezers on both sides of the flexible film) to an inner diameter of <1 mm, while still being suspended in the frame. When released, the outer part of the flexible film slightly unrolled. This is displayed in Figure 7.4. However, the inner diameter was still within specifications. The resistance measurement after rolling is shown in Table 7.1. This resistance measurement (2151.8 Ω, $\sigma = 8.2$) indicates no failures in the flexible interconnect after rolling.
Next, while in this rolled state, pressure was applied with a tweezer on the rolled flexible interconnects. The resulting flexible interconnect (after releasing the tweezer) is displayed in Figure 7.5. After releasing the tweezer, the membrane went slightly back to its rolled stated, but the fold was still visible. Table 7.1 shows the resistance measurement after bending with a tweezer (2160.9 Ω, $\sigma = 14.1$). This measurement again indicates no failures in the flexible interconnect. To further inspect the result of the fold, the flexible interconnects were folded back to their original state of before the mechanical tests. The result of the fold on the flexible interconnects remained visible (see Figure 7.6).

7.4.3. DISCUSSION

Although the device survived the rolling test and bending test, it was observed that the flexible film was still prone to tearing. This was especially noticeable when handling the devices with lateral movement (manual handling with tweezers). Furthermore, the tearing mainly occurred at the border of the silicon part of the device (containing the bond pads) and the flexible film. It appears that the edge of this silicon island is too 'sharp' for the flexible part of the device, making handling outside the frame difficult. Possible solutions this reduce this problem will be discussed in Chapter 8.

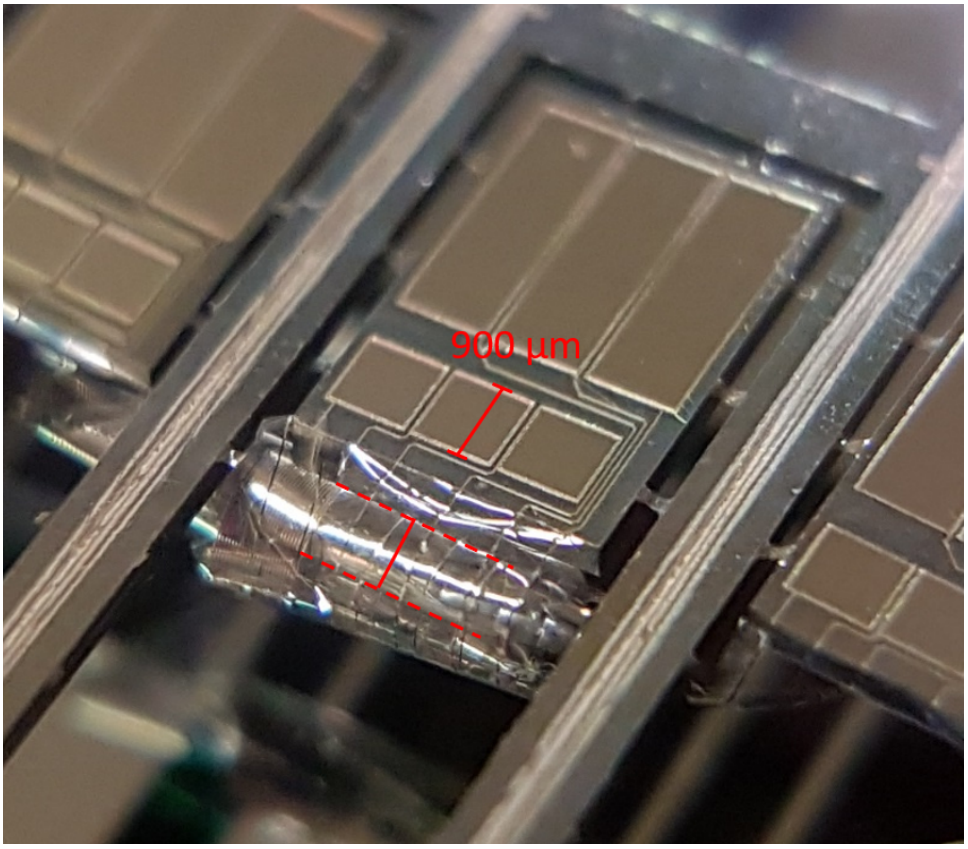


Figure 7.4: The rolled state of the flexible film (inner diameter <1 mm) while the device is still suspended inside the frame.

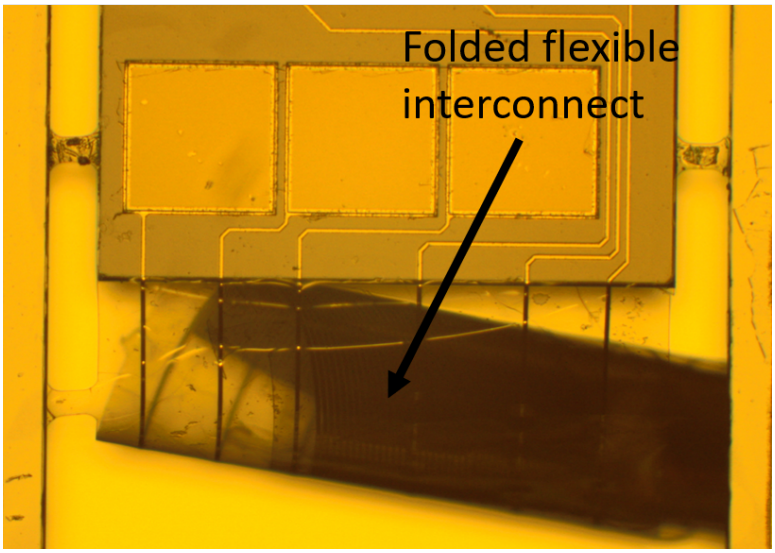


Figure 7.5: The bended state of the device after applying pressure with a tweezer.

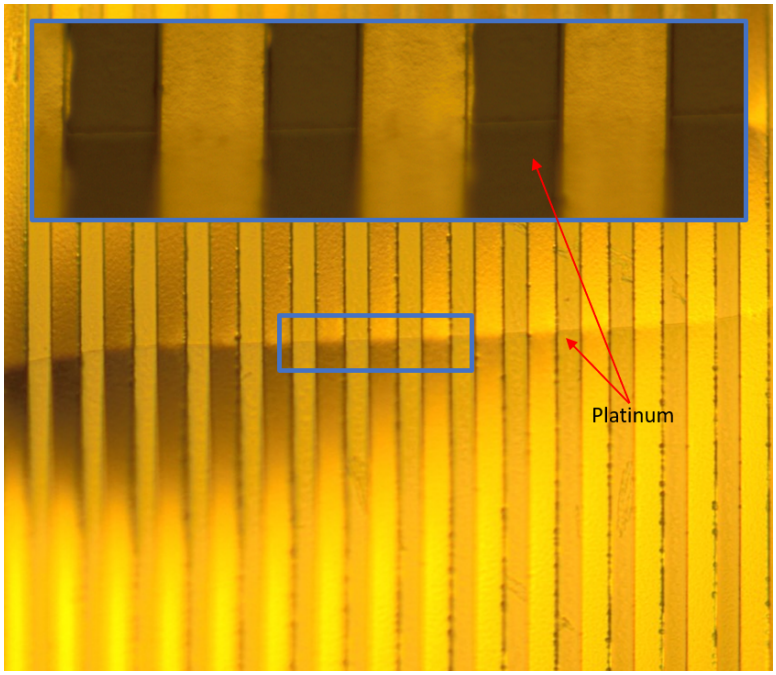


Figure 7.6: The resulting fold mark on the platinum after unrolling the flexible film.

7.5. CONCLUSION

Although all technology modules from the previous chapter could theoretically be integrated in the initial process flow, due to practical issues it was not possible to use the two-step ion milling process. Although the DRIE process was successful, separating the process wafer from the transport wafer was not possible without breaking membranes and partly cracking the oxide etch stop. The remaining fabrication steps did not introduce any further issues. The flexible meandering interconnects survived the rolling and bending test. After rolling and after bending, no significant differences in the electrical resistance was measured.

8

CONCLUSION

In this thesis, a fabrication process was developed that allows for the fabrication of flexible parylene-platinum based interconnects and electrodes. Novel methods, improvements and evaluation of the technology are presented.

The particle contamination at critical interfaces was controlled. This was done by identifying the origin of the particles, and a process step rearrangement to avoid the masking issues that they introduce. Furthermore, rearrangement of the process steps also repositioned the particles from in between the bottom parylene layer and the oxide on the front, to in between the oxide and the silicon on the front. This interface is more stable, and therefore will minimally affect the stability of the device.

The adhesion of parylene and platinum was investigated. This was done with a practical evaluation method that did not require a complex setup. The most critical interface was identified, which was the parylene on platinum interface. This interface requires additional adhesion promoting improvements, but so far the annealing at high temperatures (>200 °C) has shown the best results. However, overall the adhesion is sufficient to perform electrochemical characterization, which was the main objective of the adhesion evaluation. Furthermore, the results of the adhesion tests can be used as a reference for adhesion promoting treatments of parylene and platinum in the future.

The parylene etching for the vias was improved to obtain a slope of 45°. This was done for a parylene layer of 2.5 μm thickness using 6 μm of AZ9260. This improved the platinum step coverage, resulting in a more uniform metallization. The obtained slope was achieved by investigating the effect of CF_4 on the isotropy of the etching process. The improved etching recipe consisted of O_2: 75 sccm and CF_4: 5 sccm.

A new method to pattern platinum on parylene that results in clean and fenceless metallization has been demonstrated. This method separates the ion milling into two steps. The first ion milling step etches the majority of the platinum, leaving a thin layer behind (~50 nm). This thin layer still covers the parylene, which allows for photoresist removal methods such as high power oxygen plasma treatment (controlled at low temperature due to the parylene). This results in clean metallization. Furthermore, since the photoresist can be fully stripped, thin resist (1 μm) can be used. This avoids fence formation due to reduced redeposition of platinum on the sidewall.

After the fabrication of the devices, the flexible interconnects passed the rolling and bending tests. Before rolling, after rolling (inner diameter < 1 mm), and after bending by applying pressure with a tweezer, the same resistance values were measured.

The improvements and results presented in this work are important for future development of the integration of parylene and platinum in the F2R technology platform. The developed fabrication technology modules allow for consistent reproducibility. Furthermore, the devices can be electrically and mechanically characterized. This facilitates the evaluation of future improvements of the fabrication of flexible parylene-platinum based interconnects and electrodes.

RECOMMENDATIONS AND FUTURE WORK

As previously mentioned, the flexible devices were prone to tearing during manual handling, which was mainly due to the sharp silicon island. A design change that might reduce this problem is to round the silicon island at the corners, since it was observed that tears were originating from these corners.

Another design improvement that can be made is the addition of a second silicon island on the other end of the flexible film. This allows for more practical handling, since it reduces handling contact with the flexible film. Furthermore, depending on the length of this second silicon island, it can also facilitate the rolling of the flexible film by functioning as a supporting structure.

A fabrication related issue that lowered the yield significantly was the separation of the process wafer from the transport wafer. The reason for the transport wafer was to prevent the exposure of platinum in the chamber of the tool (not allowed) due to broken membranes. The conductive adhesive that was used did not dissolve in the recommended solvents after the DRIE process. During the DRIE process, the adhesive might have been chemically altered, since it was very easy to separate the process wafer from the transport wafer in the solvents before the DRIE process. This requires more research and experiments with different conductive adhesives.

Another way to tackle this problem is to separate the DRIE process in 2 steps (similar to the two-step ion milling process presented in this thesis). In the first etching step, the majority of the silicon should be etched, leaving a thin layer of silicon behind. This can be done without a transport wafer. In the next second etching step, a transport wafer can be used without, or with minimal conductive wax. Since this etch can be very short, the poor cooling properties of the device wafer on the handle wafer, which will affect the selectivity of the oxide hardmask, might be acceptable.

The adhesion of parylene and platinum was investigated. However, the stability of the full configuration (parylene-platinum-parylene) was not evaluated. This can provide more information regarding the effectiveness of adhesion promoting techniques, since the full configuration can behave differently. For example, annealing the full configuration at high temperatures (>200 °C) will reduce the intrinsic stress of the platinum, but can also increase bonding of the parylene-parylene interface by the entanglement of the linear chains of the parylene at the interface [24].

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A

PLATINUM CONTAMINATION PREVENTION

As mentioned in Chapter 6, the initial platinum sputter deposition was not successfull. This appendix will briefly explain this issue and how it was solved.

The sputtering of platinum (and the titanium adhesive layer) is done at Philips, where 6 inch wafers are used instead of 4 inch wafers. The sputtering of platinum is done by placing the 4 inch process wafer on several 4 inch dummy wafers. These are then all mounted on a 6 inch carrier wafer in holder with a protection ring on top. The dummy wafers are needed to match the correct height in the holder. This is important, since it allows the protection ring to fit perfect on the holder, which prevents platinum deposition on the edge and side of the wafer. During the first deposition, the ring was bending, causing platinum contamination at the edge. This was solved in the new holder, by improving the mechanical support (Figure A.1). Figure A.2 shows the results of the deposition in the old holder and the new holder. The improvement in the edge exclusion is clearly visible.

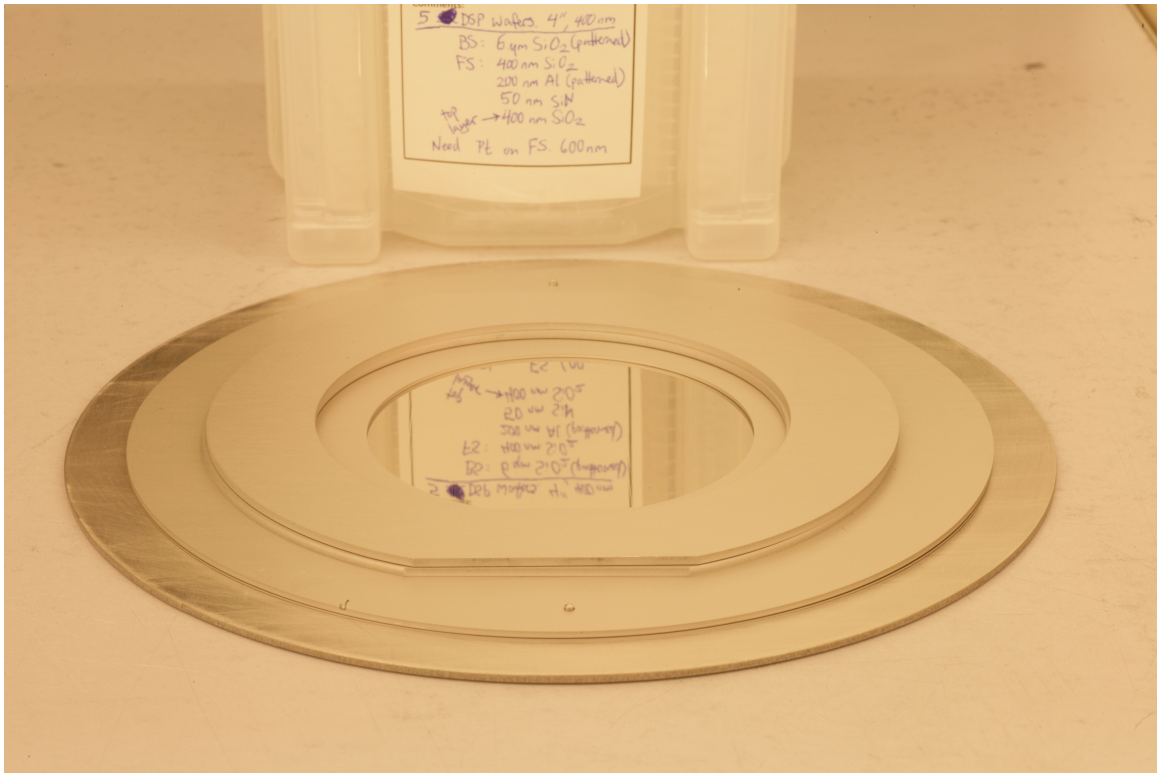
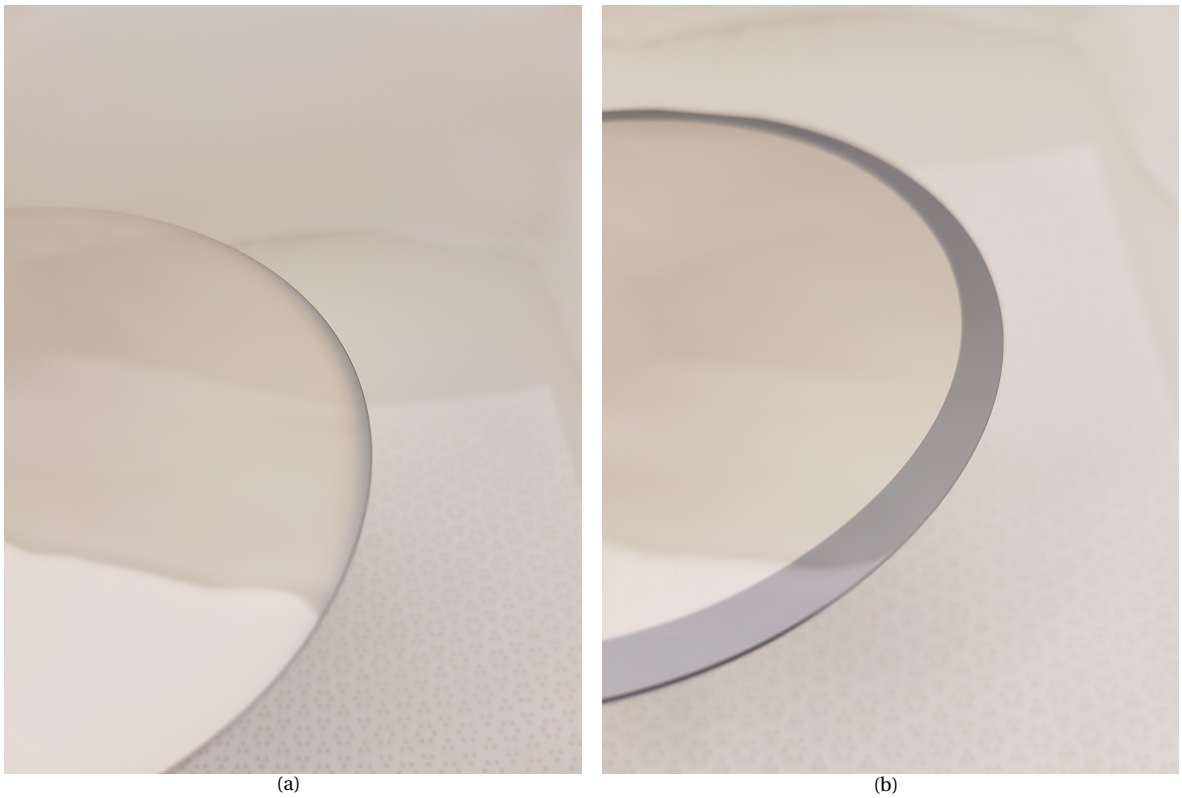


Figure A.1: The wafer mounted in the new holder.



(a) (b)

Figure A.2: The edge of the wafer after platinum sputter deposition at Philips: (a) using the old holder; (b) using the new holder.

B

FABRICATION FLOWCHART

1. PLASMA ENHANCED SiO_2 DEPOSITION (6.0 μm) (BS)

Use the Novellus PECVD reactor to deposit a 6.0 μm thick SiO_2 layer.
Follow the operating instructions from the manual when using this machine.
The process conditions of the deposition program may not be changed !

Use **ZeroStressOxide**
Check logbook for time

2. COATING AND BAKING (FS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95 °C for 1.5 minute. Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co-3012-zerolayer** (resist thickness: 1.400 μm).

3. ALIGNMENT AND EXPOSURE (FS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper. Follow the operating instructions from the manual when using this machine.

Mask: COMURK
Reticle ID: COMURK
Job: LITHO/epi0.0
Energy: 140 mJ/cm^2

4. DEVELOPMENT (FS)

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 1.5 minute. Always check the temperature of the hotplates first.

Use development program: **Dev - SP**.

5. INSPECTION: LINEWIDTH AND OVERLAY (FS)

Visually inspect the wafers through a microscope, and check the linewidth. No resist residues are allowed

on the backside.

6. PLASMA ETCHING OF ALIGNMENT MARKS (FS)

Use the Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed!
Use sequence URK-NPD for and set the platen temperature to 20 °C to etch ASML URK's into the silicon. Check if etched properly, check Si depth in Dektak, should be 140 nm. Only then continue with next cleaning step.

7. CLEANING PROCEDURE: TEPLA + HNO3 100% and 69% for Si

Plasma strip: Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 4.

Cleaning: 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the white dot.

QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning: 10 minutes in concentrated nitric acid (Merck: HNO3 65% selectipur) at 110 °C. Use wet bench "HNO3 (65%)" and the carrier with the white dot.

QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying: Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

8. COATING AND BAKING (BS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3027M positive photoresist, and a soft bake at 95°C for 1.5 minute. Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co-3027-4.0μm-NO EBR** resist thickness: 4.0 μm

9. ALIGNMENT AND EXPOSURE (BS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2209
Layer ID: RELEASE
Job: special/001project/EC2209/EC2209
Energy: 500 mJ/cm^2

Use backside alignment: P -> M, GLOBAL -> BACKSIDE4

10. DEVELOPMENT (BS)

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 1.5 minute. Always check the temperature of the hotplates first.

Use development program: **Dev - DP**.

11. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check development results.

12. WINDOW ETCHING 6 μm OXIDE (BS)

Use Drytek 384T plasma etcher with program stdoxide.
Change the time to 14 minutes (TEST ON ONE WAFER FIRST).
Follow the instructions when using this machine.

13. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check size. Oxide should be completely etched.

14. CLEANING PROCEDURE: TEPLA + HNO3 100% and 69% for Si

Plasma strip: Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 4.

Cleaning: 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the white dot.

QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning: 10 minutes in concentrated nitric acid (Merck: HNO3 65% selectipur) at 110 °C. Use wet bench "HNO3 (65%)" and the carrier with the white dot.

QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying: Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

15. PLASMA ENHANCED SiO2 DEPOSITION (2.0 μm) (FS)

Use the Novellus PECVD reactor to deposit a 2.0 m thick SiO2 layer.
Follow the operating instructions from the manual when using this machine.
The process conditions of the deposition program may not be changed!

Use **ZeroStressOxide**
Check logbook for time

16. TEPLA O2 PLASMA TREATMENT

Use Tepla plasma system recipe number 2 to promote adhesion for the first Parylene deposition. Next step (Parylene deposition) has to be done within half an hour.

17. PARYLENE DEPOSITION 2.5 μm (MEMS)

Use Parylene deposition chamber in MEMS lab.
Use: 2g/1μm-> 5g with A-174 Silane adhesion promoter. Always 5 wafers in chamber.

18. MEASURE THICKNESS PARYLENE/ OPTICAL INSPECTION

Use LEITZ to measure the thickness of the par. Use Par on Si, then substract oxide (also calculated with Par on Si) to estimate parylene thickness. Also inspect the surface for bubbles and uniformity.

19. PLASMA ETCH PARYLENE 2.5 μm (BS)

Use the Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
Preconditioning necessary with par dummy wafer, check etch rate.
Use sequence **Par1** for and set the platen temperature to 20 °C to etch parylene from the backside.

20. OPTICAL INSPECTION/HOTPLATE

Check for bubble formation/other defects. Optional heating on hotplate to observe possible degassing.

21. SPIN CLEANING AND BAKE TO DRY/EVAPORATE SOLVENT RESIDUES (FS)

Clean the frontside with the spray coater (use edge chuck) with 5s of Acetone, and remaining time drying.
Use program **acetone-spin-mapper**.
Anneal for 2min at 90 °C.

22. COATING AND BAKING (SEMI-MANUAL) (FS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
Spin coating with AZ9260 positive photoresist, and a soft bake at 100°C for 2.5 minute.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use pre bake program: **Only-SB on coater** Use coating program: **x-Marta-Syr-9260-6μm-sb-95deg-5mi30s-noHMDS-noEBR**

23. WAIT 15 MINUTES

24. ALIGMENT AND EXPOSURE (FS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2209
Layer ID: PARVIA1
Job: special/001project/EC2209/EC2209
Energy: 675 mJ/cm^2
Focus: -3μm

25. WAIT 15 MINUTES

26. DEVELOPMENT (MANUAL)

Develop: Use AZ400K: Water (1:4) developer and develop for ca 120sec.
Rinse and dry: Rinse immediately and use the manual dryer.

27. INSPECT LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check linewidth.

28. PLASMA ETCH PARYLENE 2.5 μm (FS)

Use the Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.

Preconditioning necessary with par dummy wafer, check etch rate.
Use sequence Par3 with O2: 75 sccm, CF4: 5 sccm and set the platen temperature to 20 °C to etch parylene from the frontside. Test on 1 wafer first , previously 3 min for 2.5 μm with PARVIA1 mask.

29. RESIST STRIP AND DRY

Use the Spray Coater with 5s of Acetone, and remaining time drying.
Use program **acetone-spin-mapper**.

30. INSPECTION: LINEWIDTH

Visually inspect the wafers through a microscope, and check linewidth and slope.

31. PLATINUM SPUTTER DEPOSITION (600nm) (PlnS)

Preceded by 2 min bake at 90 °C on hotplate, sputter etch and 20 nm titanium adhesive layer. Use clean 6 inch carrier wafers, clean tweezers and clean shield ring. PROVIDE 4 INCH DUMMY WAFERS FOR HEIGHT ADJUSTMENT at PInS.

32. BACKSIDE INSPECTION

From now on extra careful with further processing in EKL. Check possible contamination on the backside. Wafer edge 4mm exclusion from the edge.

33. MANUAL COATING AND BAKING (FS)

Use the Brewer Science Manual Spinner to coat the wafers with resist, and follow the instructions specified for this equipment.

Use coating program: **x-arshaad-HPR-504-1μm**
Bake at 90 °C for 2 min

34. ALIGNMENT AND EXPOSURE (FS) (RED CASSETTE)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2209
Layer ID: METAL
Job: special/001project/EC2209/EC2209
Energy: 120 mJ/cm^2
Focus: -0.3 μm

Alignment markers need to be re-opened as well:

Mask: COMURK
Layer ID: 1
Job: litho/clearurk
Energy: 180 mJ/cm^2
Focus: -0.3μm

35. DEVELOPMENT (MANUAL)

Develop: Using AZ developer: Water (4:3) and develop for ca 60 sec.
Rinse and dry: Rinse immediately and use the manual dryer.

36. REFLOW RESIST TO FURTHER REDUCE FENCE FORMATION

Bake in a convection furnace at 125 °C for 30 min.

37. TWO STEP PLATINUM ETCH (600nm) (PlnS) (FS)

Platinum etch at PlnS on 6 inch carrier wafer, use clean tweezers.
Etch 550 nm of platinum, then high oxygen plasma strip (T< 110 °C) to strip the resist, and etch remain 50 nm of platinum and 20 nm of titanium.

38. PARYLENE DEPOSITION 2.5 μm (MEMS)

Use Parylene deposition chamber in MEMS lab.
Use: 2g/1μm-> 5g with A-174 Silane adhesion promoter. Always 5 wafers in chamber.

39. TITANIUM DEPOSITION (200 nm) (FS) (ON CLEAN CARRIER)

Use Sigma recipe **Ti-200nm-25C** to deposit titanium at low temperature (25°C).

40. MANUAL COATING AND BAKING (FS)

Use the Brewer Science Manual Spinner to coat the wafers with resist, and follow the instructions specified for this equipment.

Bake at 90 °C for 3 min
Use coating 3.1 μm of AZ3027
Bake at 90 °C for 2 min

41. ALIGNMENT AND EXPOSURE (FS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2209
Layer ID: PAROPEN
Job: special/001project/EC2209/EC2209
Energy: 420 mJ/cm^2
Focus: 0 μm

Bake at 95 °C for 3 min

42. DEVELOPMENT (MANUAL)

Develop: Using Shipley MF322 and develop for ca 60 sec.
Bake at 100 °C for 1.5 min
Rinse and dry: Rinse immediately and use the manual dryer.

43. PLASMA ETCH TITANIUM 200 NM (FS)(LAND ON PARYLENE)

Use the Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed!

Use sequence **Tintisvo**

44. PLASMA ETCH PARYLENE 2.5 μm (BS)

Use the Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
Preconditioning necessary with par dummy wafer, check etch rate.
Use sequence **Par1** for and set the platen temperature to 20 ^{o}C to etch parylene from the backside.

45. RESIST STRIP AND DRY

Use the Spray Coater with 5s of Acetone, and remaining time drying.
Use program **acetone-spin-mapper**.

46. ETCH SILICON USING OX HM (BS) (LAND ON OXIDE)
Use Rapier to etch 400 μm of silicon. RECIPE: EKL-smooth-20 (previously: 260 cycles to etch 78 um with RELEASE mask)

47. PLASMA ETCH PARYLENE 2.5 μm (FS) (LAND ON PT)

Use Alcatel to etch 5.0 μm of Parylene (O2 plasma: 70 sccm, P= 60W)(previously 220nm/min).

48. WET ETCH OXIDE (BS) AND TITANIUM (FS) (LAND ON PARYLENE) (SAL)

Triton for 15min, remove oxide (7.5 min) and titanium (1 min) with wet etching in SAL with BHF.

C

CROSS CUT TESTS

Table C.1: The complete process flow of all the samples used for the cross cuts tests.

	Pt on Par			Par on Pt			Par on Par			
	A1	A2	A3	B1	B2	B3	C1	C2	C3	C4
PECVD oxide (2.0 µm)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Silane A-174	✓	✓	✓				✓	✓	✓	✓
Parylene deposition (2.5 µm)	✓	✓	✓				✓	✓	✓	✓
Parylene frontside cleaning with acetone							✓			✓
Sputter etch Argon (15 s)	✓	✓	✓	✓	✓	✓	✓			✓
Titanium sputtering (20 nm)	✓		✓	✓	✓	✓				
Platinum sputtering (600 nm)	✓	✓	✓	✓	✓	✓				
Annealing at 200°C for 1h (N_2)			✓		✓	✓				
Acetone and IPA cleaning							✓			✓
Hotplate at 100°C (2 min)							✓			✓
Silane A-174				✓	✓		✓	✓		
Parylene deposition (2.5 µm)				✓	✓	✓	✓	✓	✓	✓

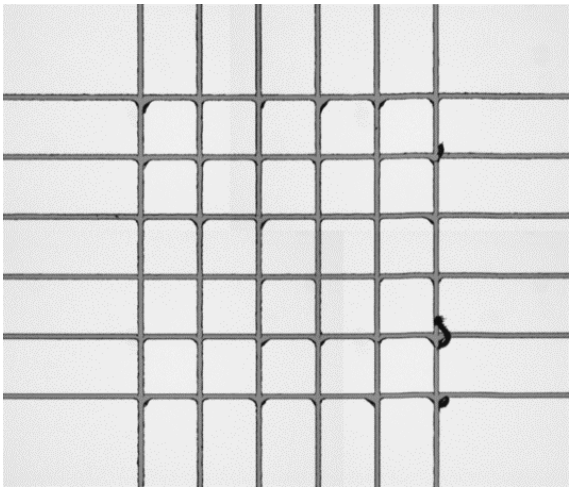


Figure C.1: Sample A1 (platinum to parylene) before peeling (after cutting).

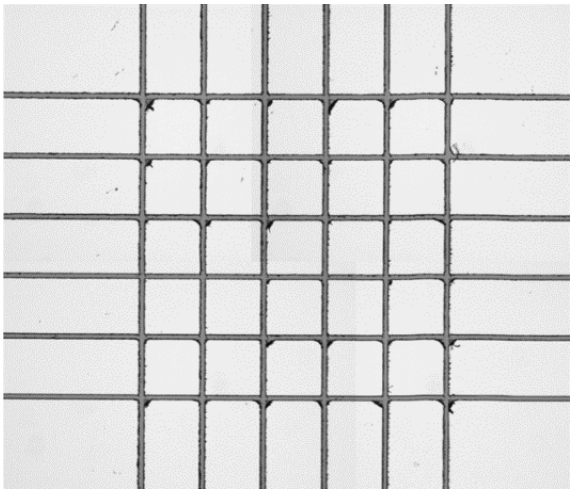


Figure C.2: Sample A1 (platinum to parylene) after peeling with 4.3 N/cm.

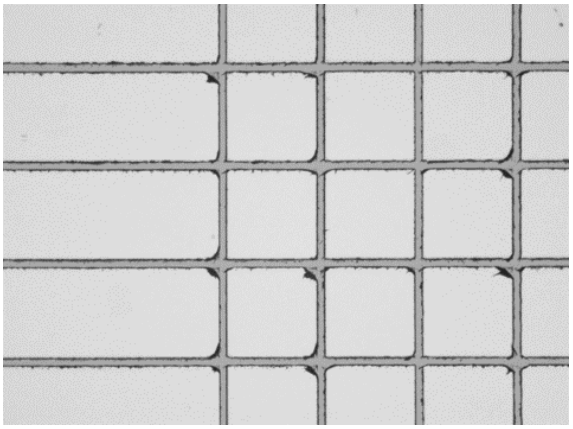


Figure C.3: Sample A1 (platinum to parylene) after peeling with 4.3 N/cm after 2 days in PBS at 37 °C.

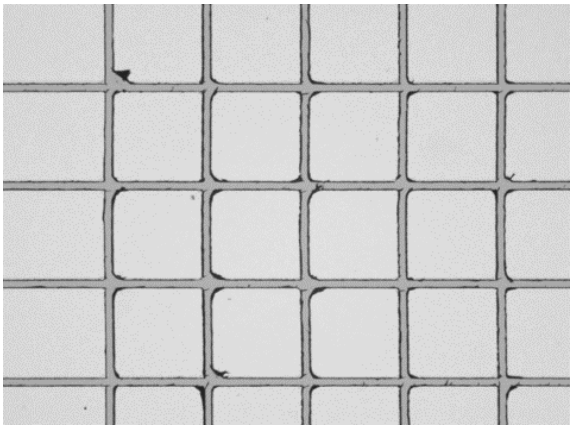


Figure C.4: Sample A1 (platinum to parylene) after peeling with 7.6 N/cm after 2 days in PBS at 37 °C.

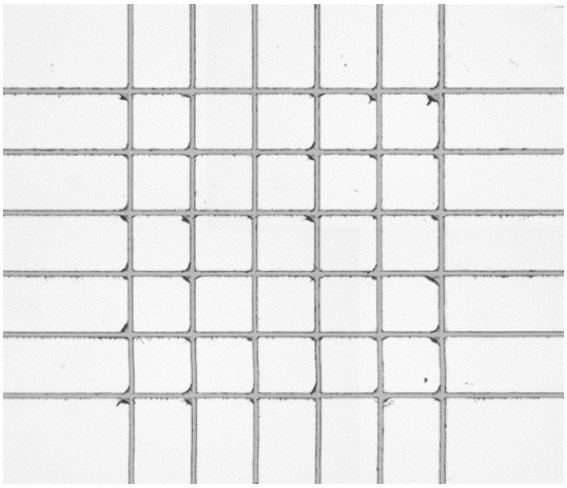


Figure C.5: Sample A1 (platinum to parylene) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

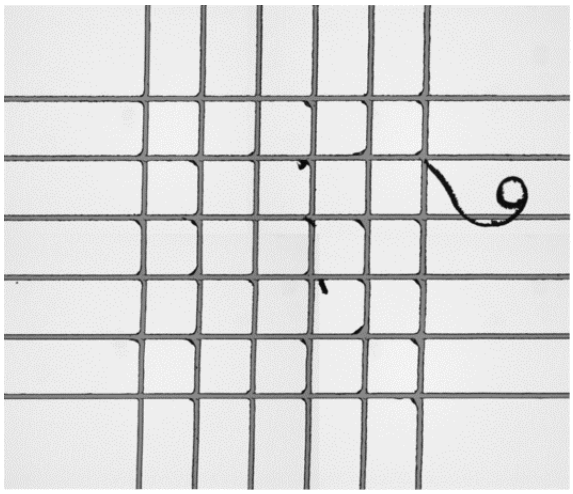


Figure C.6: Sample A2 (platinum to parylene) before peeling (after cutting).

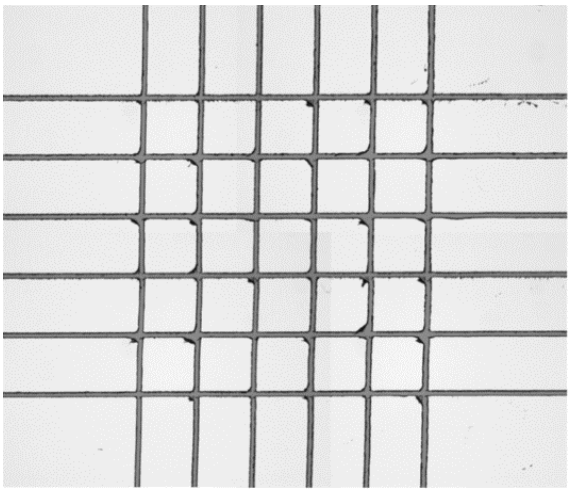


Figure C.7: Sample A2 (platinum to parylene) after peeling with 4.3 N/cm.

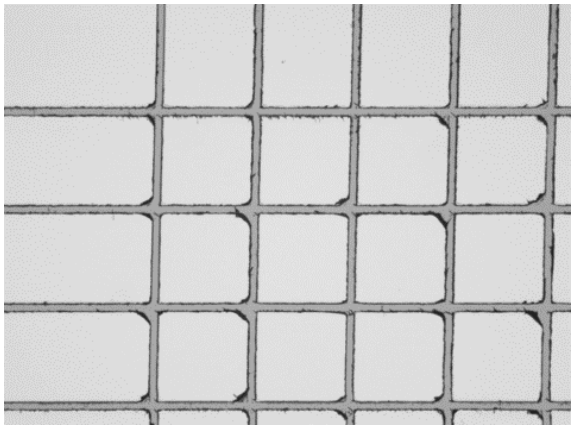


Figure C.8: Sample A2 (platinum to parylene) after peeling with 4.3 N/cm after 2 days in PBS at 37 °C.

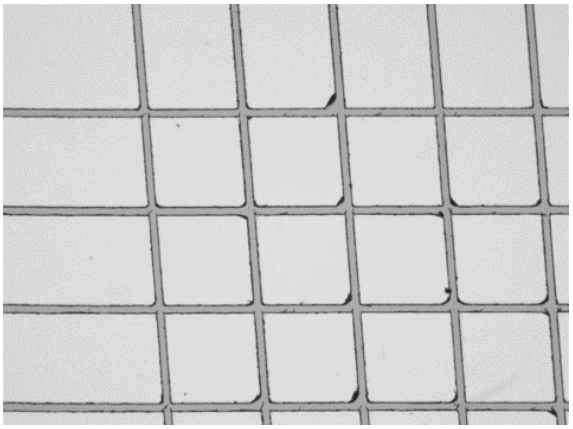


Figure C.9: Sample A2 (platinum to parylene) after peeling with 7.6 N/cm after 2 days in PBS at 37 °C.

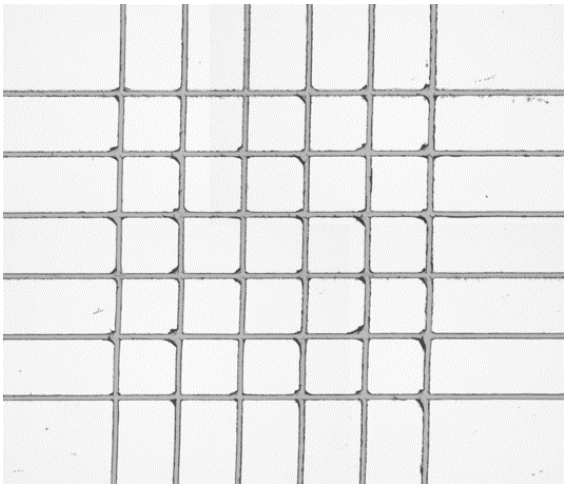


Figure C.10: Sample A2 (platinum to parylene) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

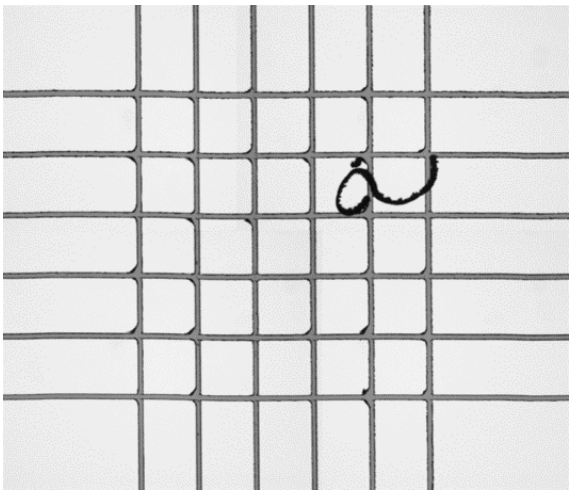


Figure C.11: Sample A3 (platinum to parylene) before peeling (after cutting).

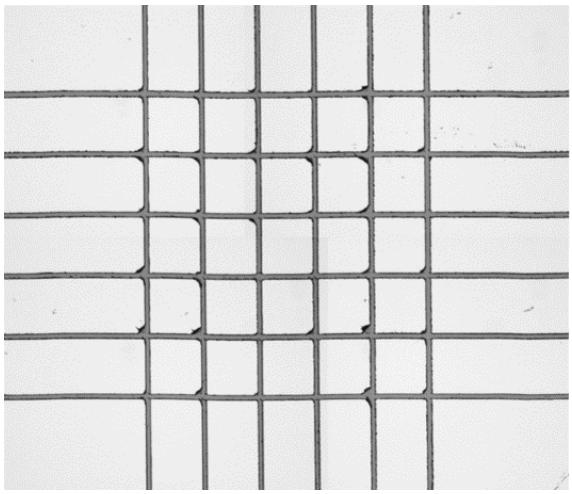


Figure C.12: Sample A3 (platinum to parylene) after peeling with 4.3 N/cm.

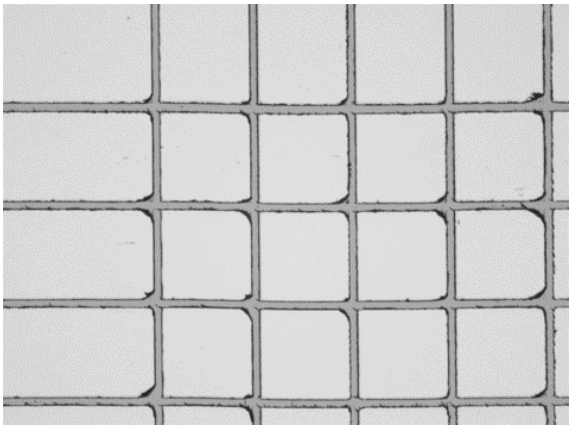


Figure C.13: Sample A3 (platinum to parylene) after peeling with 4.3 N/cm after 2 days in PBS at 37 °C.

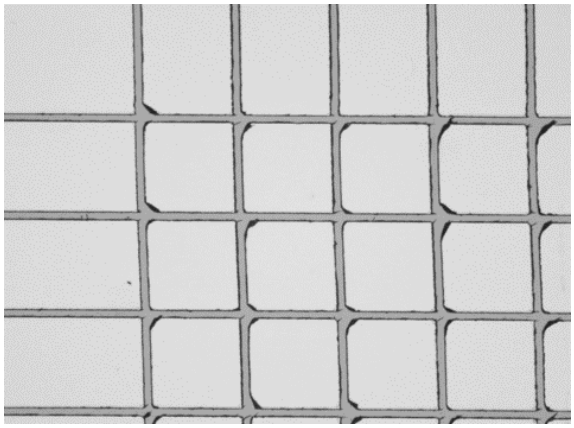


Figure C.14: Sample A3 (platinum to parylene) after peeling with 7.6 N/cm after 2 days in PBS at 37 °C.

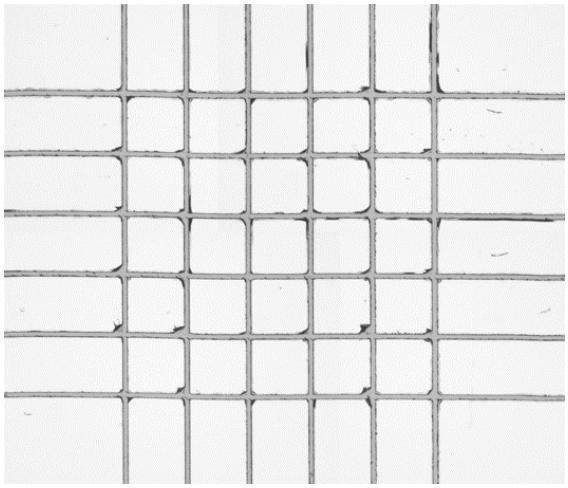


Figure C.15: Sample A3 (platinum to parylene) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

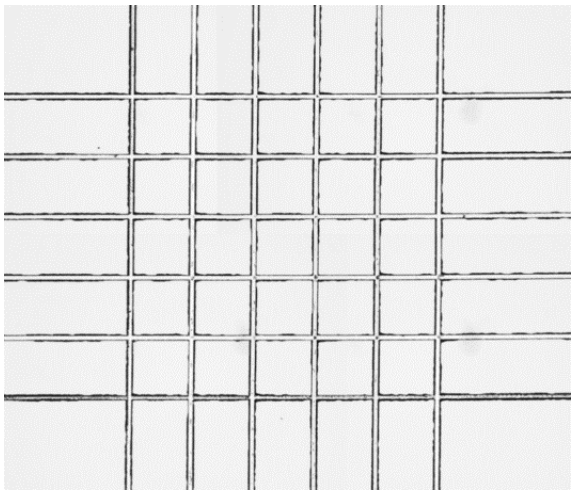


Figure C.16: Sample B1 (parylene on platinum) before peeling (after cutting).

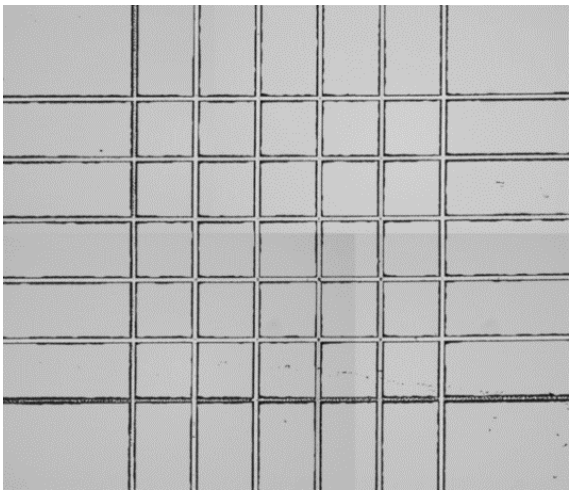


Figure C.17: Sample B1 (parylene on platinum) after peeling with 4.3 N/cm.

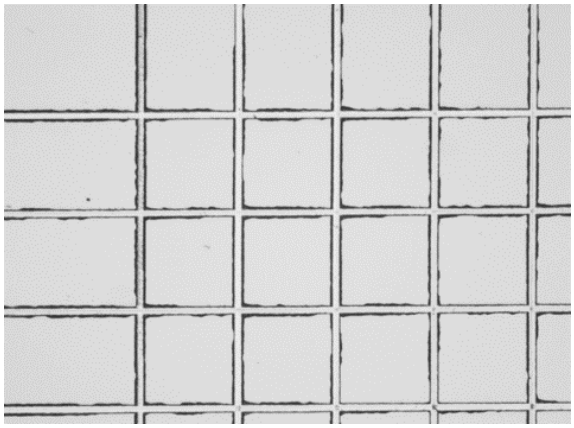


Figure C.18: Sample B1 (parylene on platinum) after peeling with 4.3 N/cm after 2 days in PBS at 37 °C.

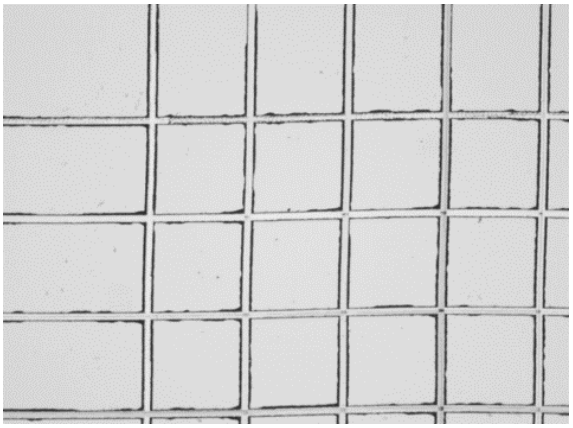


Figure C.19: Sample B1 (parylene on platinum) after peeling with 7.6 N/cm after 2 days in PBS at 37 °C.

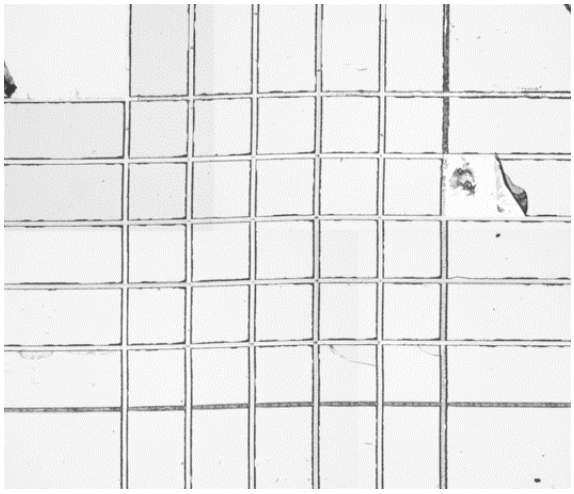


Figure C.20: Sample B1 (parylene on platinum) after peeling with 4.3 N/cm after 10 days in PBS at 55 °C.

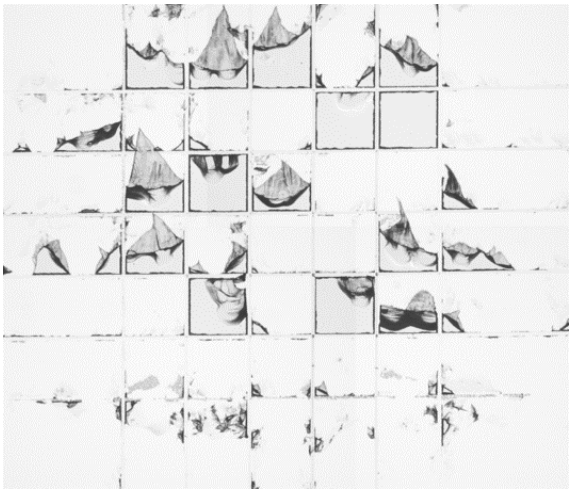


Figure C.21: Sample B1 (parylene on platinum) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

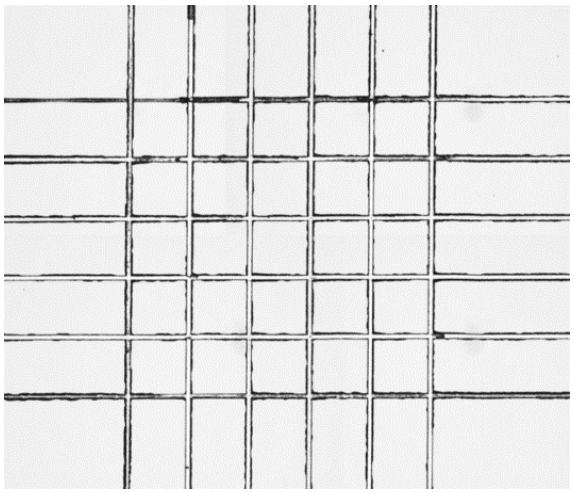


Figure C.22: Sample B2 (parylene on platinum) before peeling (after cutting).

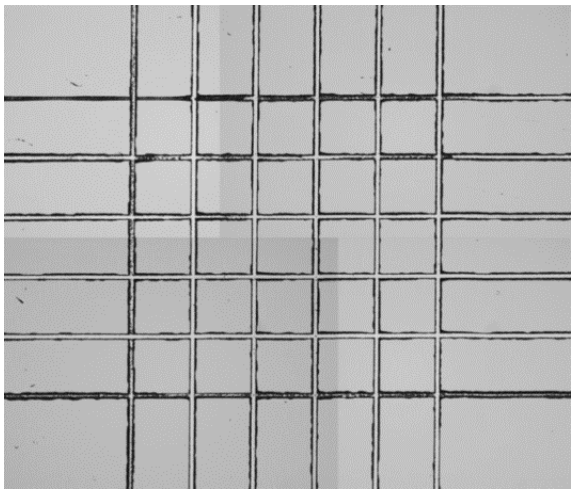


Figure C.23: Sample B2 (parylene on platinum) after peeling with 4.3 N/cm.

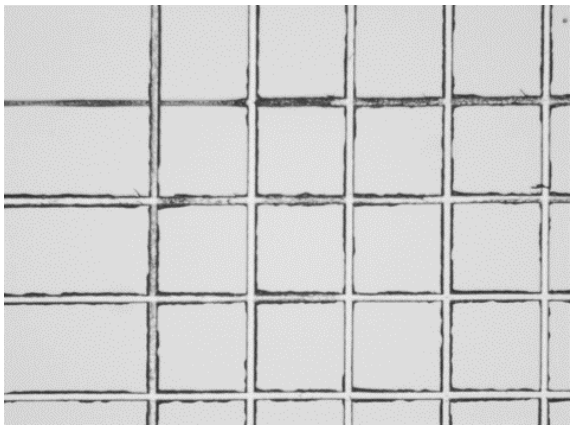


Figure C.24: Sample B2 (parylene on platinum) after peeling with 4.3 N/cm after 2 days in PBS at 37 °C.

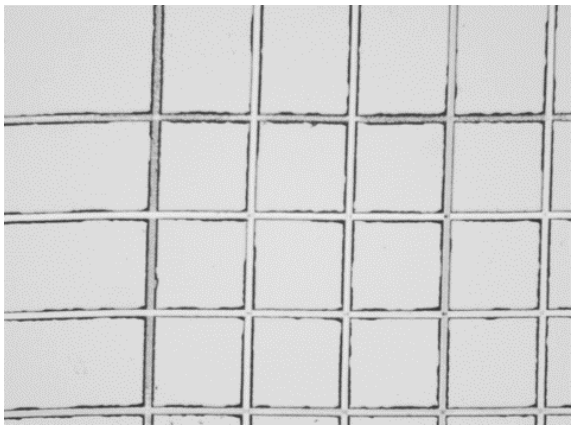


Figure C.25: Sample B2 (parylene on platinum) after peeling with 7.6 N/cm after 2 days in PBS at 37 °C.

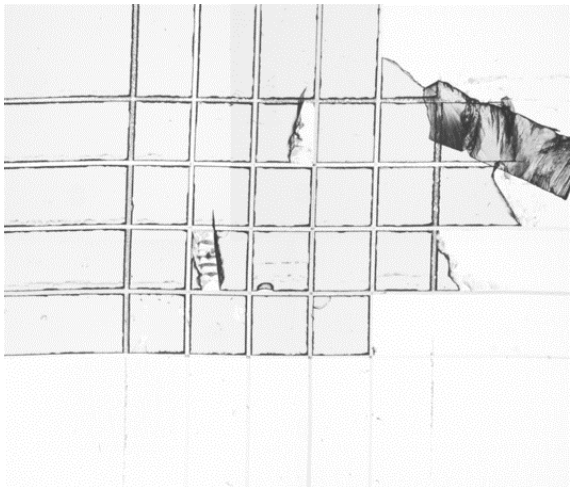


Figure C.26: Sample B2 (parylene on platinum) after peeling with 4.3 N/cm after 10 days in PBS at 55 °C.

Figure C.27: Sample B2 (parylene on platinum) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

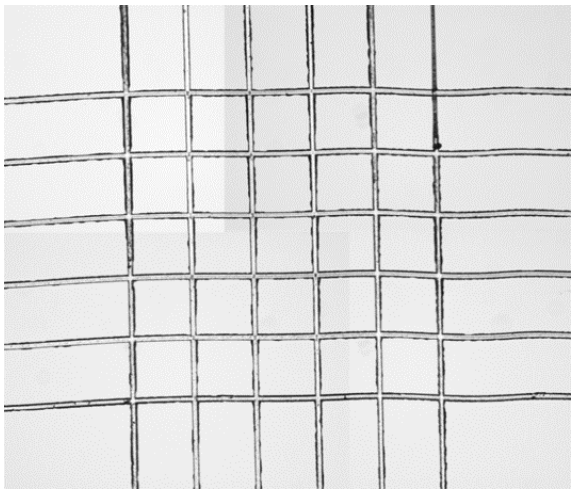


Figure C.28: Sample B3 (parylene on platinum) before peeling (after cutting).

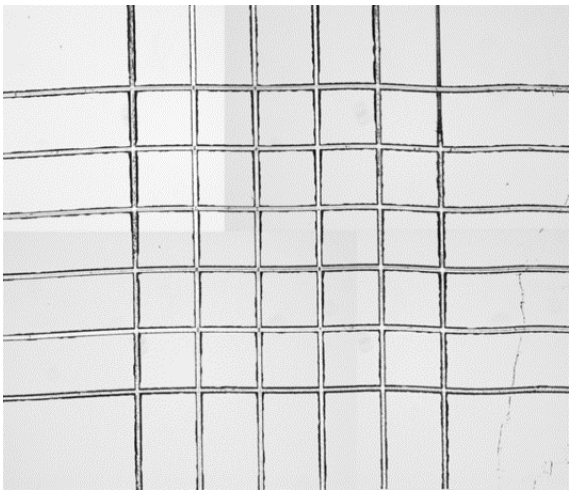


Figure C.29: Sample B3 (parylene on platinum) after peeling with 4.3 N/cm.

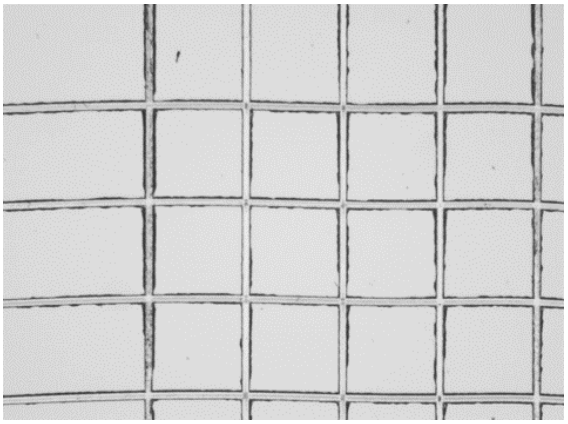


Figure C.30: Sample B3 (parylene on platinum) after peeling with 7.6 N/cm after 2 days in PBS at 37 °C.

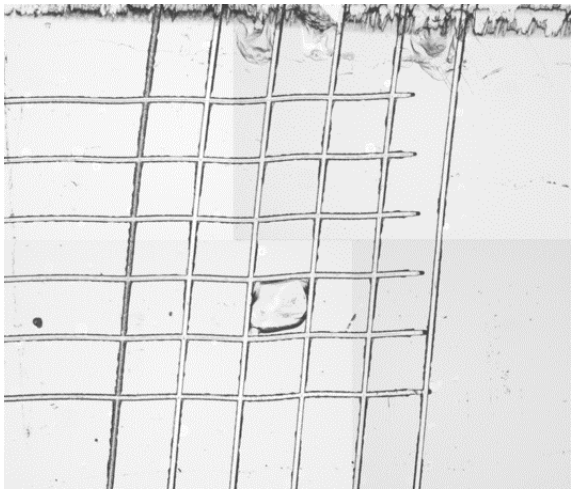


Figure C.31: Sample B3 (parylene on platinum) after peeling with 4.3 N/cm after 10 days in PBS at 55 °C.

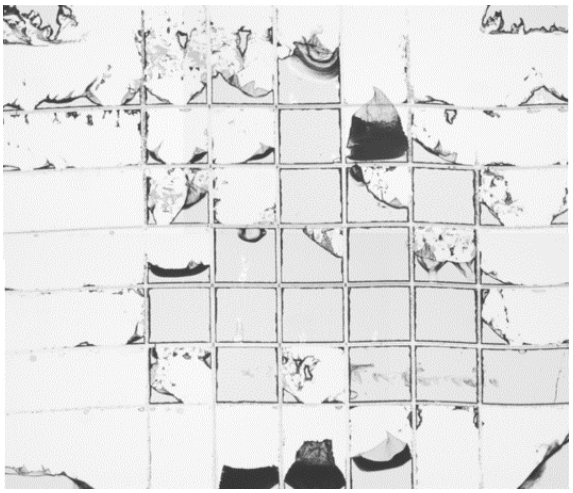


Figure C.32: Sample B3 (parylene on platinum) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

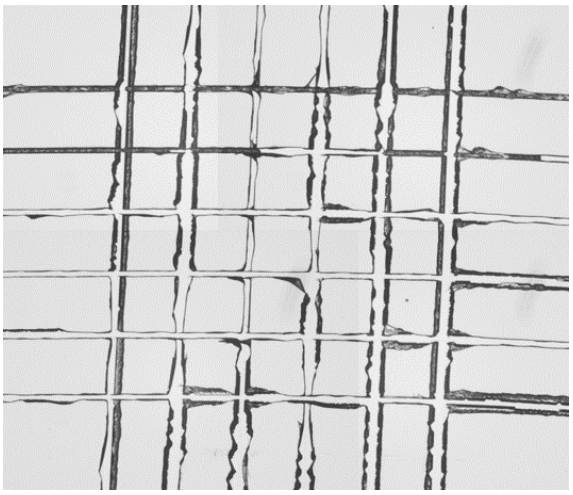


Figure C.33: Sample C1 (parylene on parylene) after peeling with 4.3 N/cm

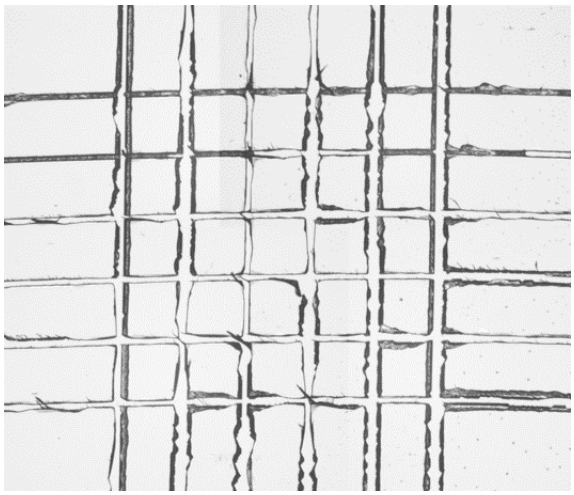


Figure C.34: Sample C1 (parylene on parylene) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

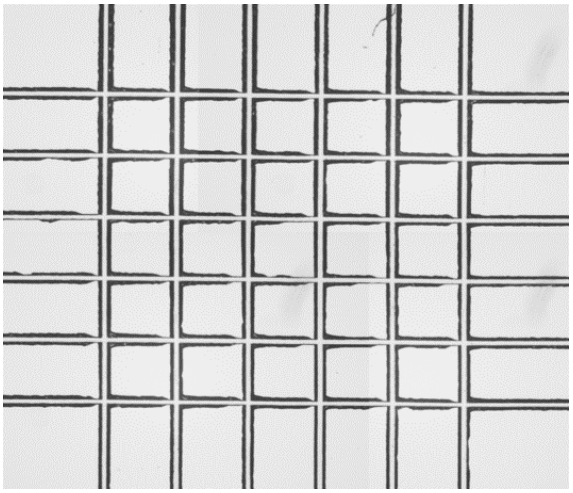


Figure C.35: Sample C2 (parylene on parylene) after peeling with 4.3 N/cm

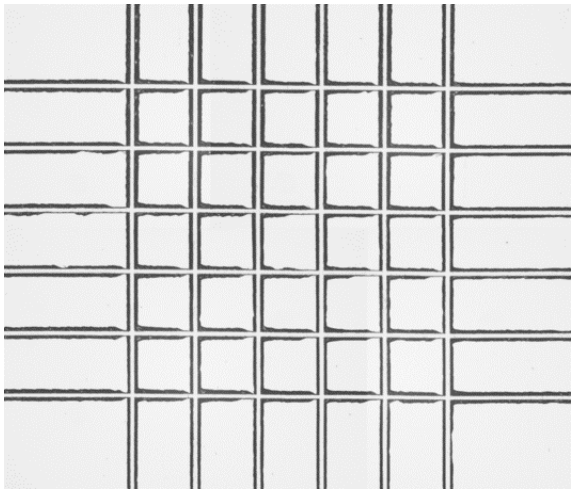


Figure C.36: Sample C2 (parylene on parylene) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

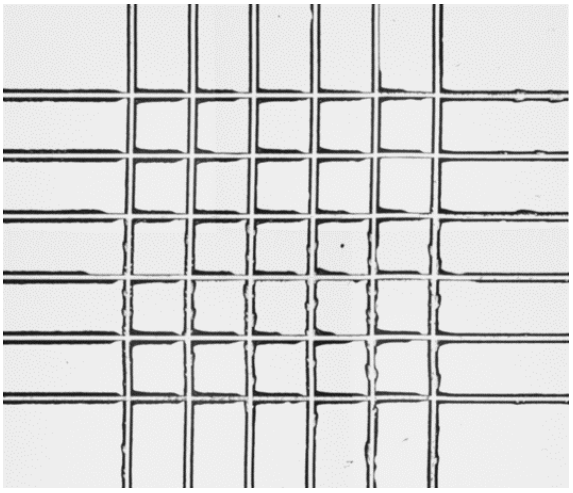


Figure C.37: Sample C3 (parylene on parylene) after peeling with 4.3 N/cm

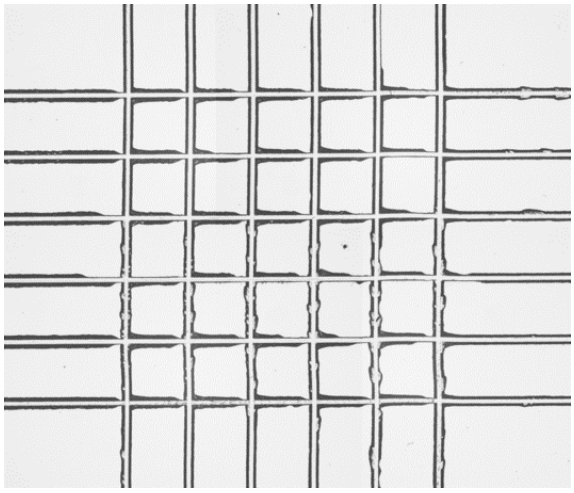


Figure C.38: Sample C3 (parylene on parylene) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.

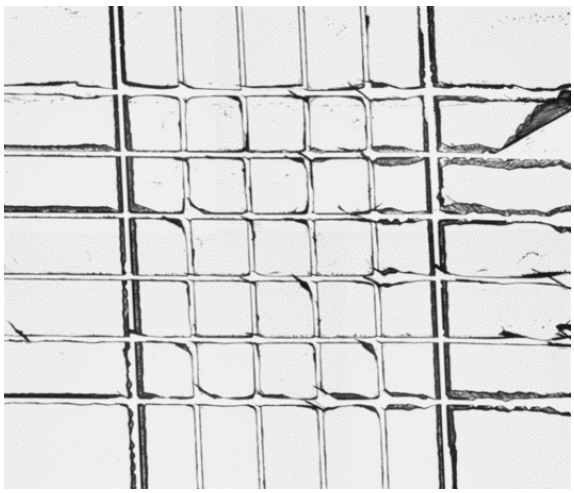


Figure C.39: Sample C4 (parylene on parylene) after peeling with 4.3 N/cm

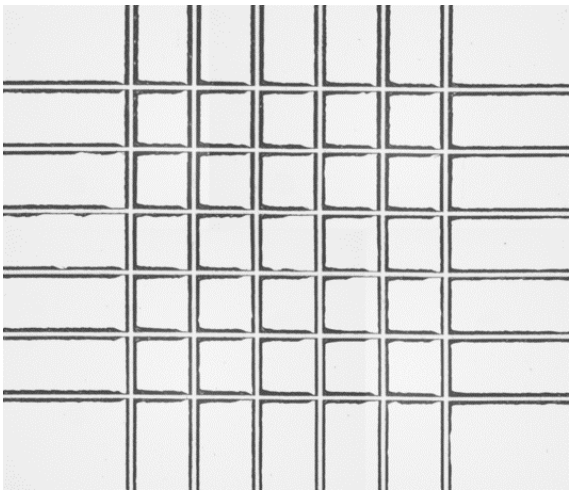


Figure C.40: Sample C4 (parylene on parylene) after peeling with 7.6 N/cm after 10 days in PBS at 55 °C.