# A MONOLITHIC PHOTOPLETHYSMOGRAM (PPG) SENSOR

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# ABSTRACT

A photoplethysmogram (PPG) is an important optically-obtained bio-sginal that enables convenient daily monitoring of heart rate and oxygen saturation (SpO2). Most state-of-the-art PPG sensing systems require an off-chip photodiode, and the photodiode's output parasitic capacitance limits the power-noise trade offs. The objective of this project is to implement a monolithic low-power PPG sensor for heart-rate detection. A novel sensing system has been developed, which has arrays of photogate imagers as front-ends and a compact successive approximation register analog-to-digital converter serving as the readout circuit. The readout power consumption is 0.64 $\mu$W at a sampling rate of 40 Hz. The minimum required LED power consumption is predicted to be 3 $\mu$W according to the post-layout simulation. The die area is 6.05 $mm^2$ including the pads. Compared with the prior art, the readout power consumption is reduced by four times and the die area is reduced by 3 times. The chip was submitted for fabrication in June in TSMC180nm.

# 1

# INTRODUCTION

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## 1.1. DAILY HEART-RATE MONITORING

Nowadays, the number of people with suboptimal health conditions is gradually increasing. A recent study [1] revealed a substantial prevalence of 69.46% of adults who were in sub-optimal health conditions in 2020. Moreover, the COVID pandemic deteriorates this situation both for the COVID survivors and for other healthy people. [2] discovered that 68% survivors were still showing at least one symptom after 6 months, while the possibility decreased slightly to 49% at 12 months, which was still twice the percentage of the COVID-negative control group. For most other healthy adults, the recurring government suggestions on the working/studying from home have dramatically decreased their outdoor activities, which substantially increases concerns of sub-optimal health conditions. Therefore, a reliable and durable health monitoring system is needed.

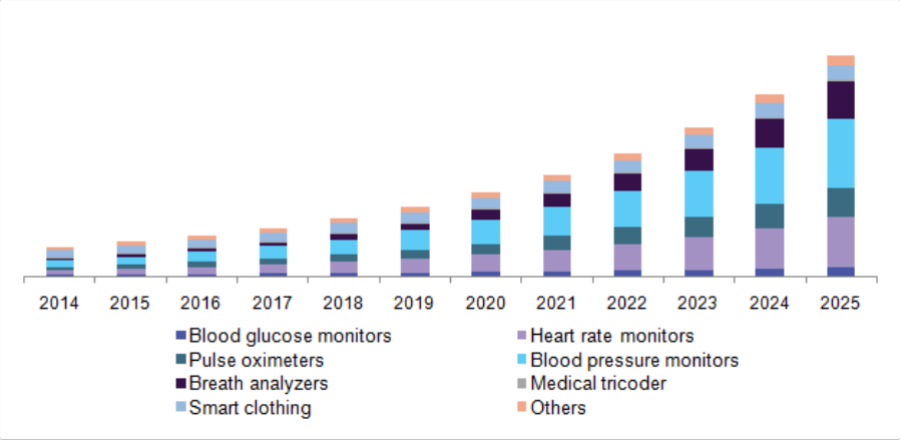


Figure 1.1: US smart medical device market by product, 2014-2025 (predicted) [3]

Figure 1.1 shows that a doubling of the overall market for smart medical devices in the United States is expected between 2021 and 2025. Among all categories, heart-rate monitoring devices (heart-rate monitors and pulse oximeters) will occupy one third of the market in 2025, as most pulse oximeters can also be used only as heart-rate monitors. However, conventional heart-rate monitors, based on electrocardiography (ECG), require electrodes placed directly on the body [4], which is not suitable for daily wearable monitoring purposes due to the bulky readout machine. Though state-of-the-art work have demonstrated lightweight wearable wrist ECG measuring solutions [5] [6]. However a watch-size box can still be cumbersome for daily use if it has an only function of ECG recording.

Optical heart-rate monitoring techniques stand out recently because they feature small size, easy integration with other devices, and low cost. The photoplethysmogram (PPG) sensing system has established its prevalence and success in pulse oximeters since 1974

[7]. However, even though most commercial pulse oximeters are portable, they are still not convenient for continuous mobile daily monitoring. Smartwatches and smart rings overcome this issue by integrating a photodiode and a light emitting diode (LED) at the back side, thus enabling everyday heart-rate measurement based on PPG signal.

However, the bottleneck for the wearable PPG sensing systems is that the power consumption of LEDs (the most power hungry component in the system) is high, resulting in a quick drain of the battery of the wearable device. To reduce LED power consumption, it is promising to investigate an optical receiver with a co-integrated photodiode and readout circuit capable to detecting smaller-amplitude PPG signals. A 4-Transistor pinned photodiode (4TPPD) fully integrated PPG-sensing system has been experimentally proven to work to obtain the heart rate [8]. However, it is not an ideal option considering its complexity and cost of manufacture.

## 1.2. MOTIVATION AND OBJECTIVES

The previously stated high LED power consumption is related to the significant parasitic capacitance between the input of the readout chip and the off-chip photodiode in conventional implementations of PPG sensors. This large capacitance effectively attenuates the signal, deteriorating the signal-to-noise ratio (SNR). The attenuated signal often requires higher LED power to compensate, which is often the dominant power component in the whole system, causing the total power consumption to increase almost linearly with the increase in LED power. To tackle this, several monolithic solutions (sensor front-ends and readout on the same chip) have been adopted in [8–10]

The state-of-the-art monolithic PPG sensors require expensive CMOS image sensor (CIS) process, particularly for a shallow, highly doped p+ thin layer. The fabrication cost can be three times higher than that of the fabrication under standard CMOS technology, given the same die area and the same circuit complexity. In this project, photogate (PG) image sensors are deployed, which share a working principle similar to the ones that uses CIS, but can be fabricated with standard CMOS technology.

The objective of this study is to develop a novel energy-efficient monolithic PPG sensing system with photogate imager sensors as front-ends. The whole chip will be fabricated in standard TSMC180nm technology.

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## 1.3. THESIS ORGANIZATION

Chapter 2 focuses on the state-of-the-art PPG readout chain design. Basic background information on the skin-light-signal (physiological-optical-electronic) interaction chain will also be presented. Three pieces of state-of-the-art monolithic PPG sensing literature are reviewed.

Chapter 3 presents the sensor front end, PG imager. It starts with the working principle and concludes with comprehensive noise analysis.

Chapter 4 is the main chapter that proposes the architecture and analyses key design aspects. Energy consumption, signal to noise ratio, the number of pixels are justified, and a compromised decision is achieved. Other design aspects, namely ADC resolution, capacitor sizing, settling accuracy and settling speed, are also analysed.

Chapter 5 presents a transistor-level design of key blocks. The transistor design choices are explained, and the block level simulation result is shown.

Chapter 6 provides the layout design and system-level postlayout simulation result. An energy distribution chart concludes this chapter.

Chapter 7 concludes this work by benchmarking state-of-the-art work, summarizing this work and proposing improvements for future work.

# 2

# STATE-OF-THE-ART PPG READOUT APPROACHES

In this chapter, a short introduction to the photoplethysmogram sensor will be presented, including its brief history, working principle, and applications. Moreover, a small section will also provide the related physiological knowledge required to understand this application. Finally, a literature review of state-of-the-art work on PPG readout circuits will be presented.



## 2.1. HISTORY

The PPG was first introduced in the last century. In the 1930's, an analogue measurement of the blood volume change was first demonstrated in the United states [11]. The term PPG was then coined in 1937, when Alrick Hertzman first introduced the use of reflective PPG to measure the change in blood volume [12]. In the last 30 years, the compact, cheap, reliable, and power-efficient design of PPG sensing systems have attracted more attention. Thanks to the wide application of non-invasive monitoring methods, the development of PPG sensors has experienced a major revolution since the 1970s [7].

## 2.2. WORKING PRINCIPLE

The basic principle behind a PPG sensor is to collect transmitted or reflected optical light from body tissue emitted by a visible or near-infrared LED and then translate it into signals in the electronic domain, i.e. current. In modern systems, the signal will then be digitised, followed by the corresponding algorithms to extract the desired information, such as the peak finding algorithm for heart-rate measurement. The body tissue under test can vary greatly from the tip of the finger to the ear, wrist, ankle, and even cheek.

As mentioned above, there are two main types of PPG sensors, transmission type and reflection type. The transmission PPG sensors are usually placed on the fingertip, where the pulse oximeter is a typical example. The photodiode (PD) directly receives the light signal after its penetrating the finger tip. The light loss due to scattering is very limited as long as the light transmitter and receiver are positioned properly. It is also possible to place it on the earlobe, tongue, and nasal septum [13], where the cross section of the tissue is thin enough for light to penetrate. Indeed, because of its tricky and limited location for measuring, the transmission PPG is more often deployed for clinical monitoring rather than for daily monitoring purpose.

Unlike the transmission one, the reflection PPG relies on light propagation inside the tissue as the left section of Figure 2.1 shows. However, it also shows that more light scatters away during reflection, which leads to a potentially high demand for LED power. Nevertheless, the advantage is that it can be deployed for testing a wider range of tissues, due to its relaxed requirement on the tissue-under-detection to be as thin as the finger tip. This leads to its extensive application in smart bands and smart watches.

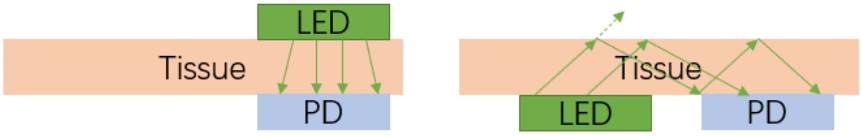


Figure 2.1: Working principle of two conventional types of PPG sensors, transmission (left) and reflection (right)

### 2.2.1. OPTICAL PHYSICS, BEER-LAMBERT LAW

To investigate PPG's working principle from a more micro-perspective, it is important to introduce the Beer-Lambert law, or the Beer-Lambert-Bourguer law. It defines the relationship between the attenuation of the light, preferably monochromatic light, through a physical material with a single absorbing element.

Mathematically, it can be simply formulated as:

$$A = \varepsilon \ell c, \tag{2.1}$$

where $A$ is absorbance, defined as the logarithm of the ratio of impinging to the radiant power received through a sample [14].
$\varepsilon$ is the molar absorption coefficient, in the SI unit of $m^2/mol$
$\ell$ is the length of the optical path, in the SI unit of m
$c$ is the molar concentration (molarity) of the absorbing elements, in the SI unit of $mol \cdot m^{-3}$

To put it simply, the Beer-Lambert law quantifies the amount of light attenuation when it propagates in a certain medium. It is worth noticing that light scattering loss and reflection loss are not considered by that law.

### 2.2.2. PPG SIGNAL GENERATION

Section 2.2.1 has explained a linear relationship of light attenuation. This theory can be applied to the generation of PPG signals. Figure 2.2 illustrates two paths through which impinging light can travel, the change of which is modulated by heart beat. Assume a very short time period, static LED and constant thickness and absorption coefficients for the tissue, venous blood, and non-pulsating arterial blood. In other words, the light attenuation in first three layers is the same in adjacent samples (when the LED turns on). When light reaches the pulsating arterial blood, its path changes with respect to different cardiac activities. For example, when it travels through a systole (the right of Figure 2.2), its path shortens, resulting in less light attenuation and hence a higher intensity

to be received by light collecting devices (e.g. a photodiode), either after reflection or transmission. This process repeats and eventually translates into the PPG signal, as illustrated at the bottom of this figure. As only the pulsating arterial blood contributes to the PPG signal generation, this part is called the AC component, while the other three are referred to as DC components as a whole in later text. Meanwhile, the perfusion index (PI) is known as the AC/DC ratio, whose typical values range from 0.2% to 20% [15].

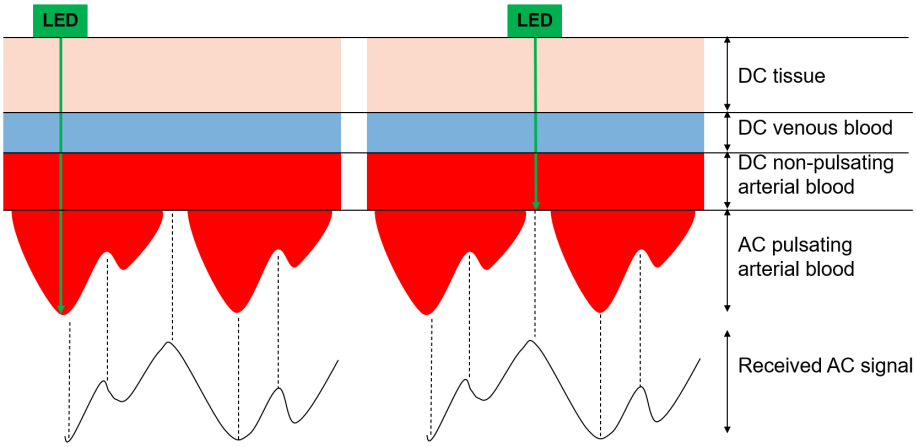


Figure 2.2: PPG signal generation in two paths, diastole (top left) and systole (top right) and an example of PPG signal (bottom) . (The LED is static. Displacement in this drawing is relative, due to blood flow)

## 2.3. PHYSIOLOGICAL-OPTICAL-ELECTRONIC INTERACTION

The way PPG signal is produced has been explained, which is the optical-electronic interaction. This section serves as an intermezzo to supplement the physiological knowledge required to understand the physiological-optical interaction and eventually the whole three-way interaction will be clear.

### 2.3.1. SKIN PHYSIOLOGY

Figure 2.3 is a classic but complex presentation of three layers of skin, namely the epidermis, the dermis, and the subcutaneous fat tissue. The epidermis is the outermost and shallowest layer, consisting of viable keratinocytes and without blood vessels. The middle layer is the dermis, composed of hair follicles, different glands, and various types of blood vessels. The subcutaneous fat tissue lies the deepest, where fibroblasts, adipose cells, and macrophages are found mainly with more sizeable blood vessels than those in the dermis layer.

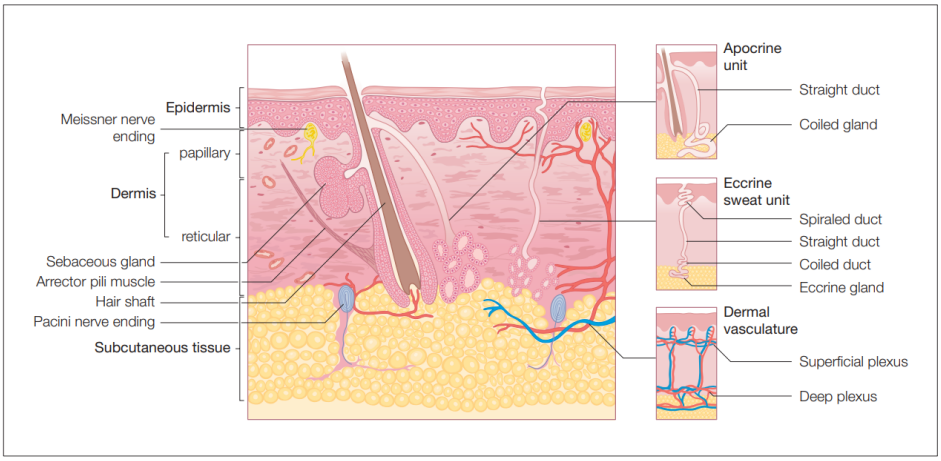


Figure 2.3: Diagrammatic cross section of the skin and panniculus [16]

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### 2.3.2. SKIN-LIGHT-SIGNAL INTERACTION

Indeed, these different layers will contribute differently to the light transmission path, considering various compositions and their locations. Firstly, melanin in the epidermis layer has a high absorption coefficient, especially at low wavelengths [17]. Secondly, when exposed sufficiently, the dermis will be penetrated and dominate the overall light absorbance, since it is typically in the order of 10 times thicker than the epidermis. Various blood vessels in it can lead to different absorbance levels, and their effective light path is subject to the change of time, or rather to cardiac activity. The change in light path of the blood vessels in the dermis layer is a major variance of interest for reflective PPG sensing. Finally, when light penetrates the subcutis, more change in terms of light path could be found. However, penetrating so deep to the subcutis risks additional random walk (scattering) of photons inside the skin, which can result in inaccurate reception of photons after reflection.

When light penetrates through the skin, the depth it can travel largely depends on the incident light wavelength. According to the study in [17], a higher wavelength leads to a deeper path that light can travel, given the same location on the skin and the same incident energy density. For example, in the visible light spectrum range, red light (700 $\mu$m wavelength) can travel 7.5 times deeper than violet light (400 $\mu$m wavelength).

As described, PI of the skin effectively translates into the ratio of the pulsating AC signal of interest to the non-pulsating DC components, through the change of received light intensity. In order to implement a PPG heart-rate monitor, an LED with a single wavelength must be chosen. The near-infrared (NIR) wavelength (780 nm – 2500 nm) has been popular for years, because of its long penetrating path. However, such deep-penetrating results in extra unwanted information, including random walks of photons

during reflection and stronger involvement of DC components. Recently, to obtain a higher effective PI, green wavelengths (around 510 nm) have been widely deployed [8, 18, 19], since they have a short but sufficient penetrating depth and absorption coefficient of the oxygenated hemoglobin (HbO2) around that wavelength is higher than it at NIR wavelengths [20]. Moreover, an application note from Analog Devices by [21] also demonstrates that a higher amplitude of the effective PPG signal (AC) can be obtained by using a green LED compared to red, blue and infra-red LEDs with the same power consumption.

Having said this, the green LED is deployed in this project that has a proper penetrating depth sufficient for heart-rate extraction.

## 2.4. LITERATURE REVIEW

As said, an off-chip PD has a high parasitic capacitance to the input of the read-out circuit, which limits the read-out chain's power and noise performance. Power consumption and noise would be reduced if the PD was integrated on the same silicon as the front-end. This section reviews three state-of-the-art monolithic ppg readout approaches. A comparison table follows.

### 2.4.1. DISTRIBUTED ARRAY MONOLITHIC CMOS PPG SENSOR

The work [9] in 2017 presents a monolithic CMOS PPG sensor (Figure 2.4). To be more elaborate, it deploys a distributed array of 1-bit sigma delta converters. Each converter has a PD as a front-end that operates in reverse mode, converting its anode voltage to a modulated 1-bit stream. There are 128 units (128 converters and 128 PDs), and their outputs are added and averaged. An external digital filter (CIC+FIR) is deployed to reconstruct the output. The proposed monolithic and distributed architecture increases the dynamic range of the sensor and reduces the impact of noise. The proposed architecture has a readout power consumption of 13 - 25 $\mu$W, which is subject to the change of photon-generated DC levels that depends on LED's power-on duty. Unfortunately, the LED power consumption is not reported, while it can be expected to be a high value due to the very high sampling rate (160 kHz). The chip area is 1.792 mm$^2$.

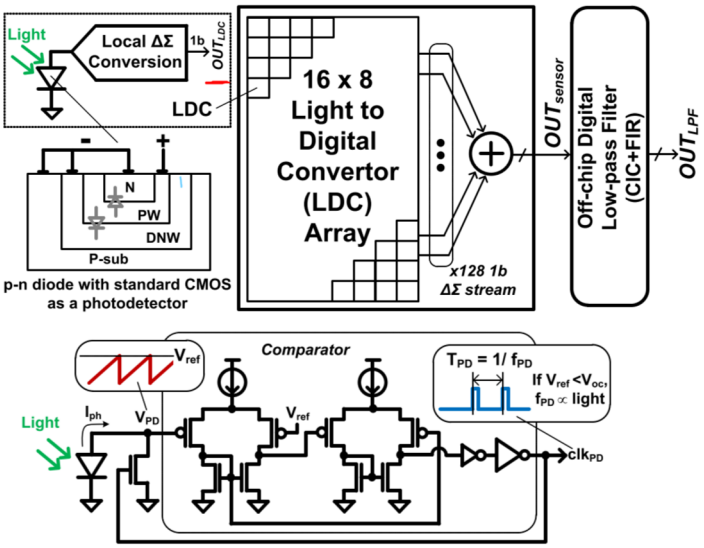


Figure 2.4: Proposed distributed array light to digital converter as in [9]

### 2.4.2. MONOLITHIC PINNED PHOTODIODE (PPD) PPG SENSOR

Figure 2.5 shows an architecture that incorporates a state-of-the-art CMOS image sensor (CIS) readout chain together with PPD pixels proposed by [8] in 2019. The front-end on-chip PPD features a special conversion method to passively integrate the photocurrent and a voltage can be generated at the output. Then, a variable gain voltage amplifier is deployed to handle different swings of the input signal. An incremental ADC follows to digitize the voltage. The ADC has a variable resolution that is implemented by changing the counting time. It achieves an LED power consumption of 1.97 $\mu$W and a readout power consumption of 2.63 $\mu$W with a sampling frequency of 40 Hz. The main readout power consumption is burnt during the ADC phase, when the main amplifier statically turns on during counting, which is worth optimising. The chip size is 20 mm$^2$.

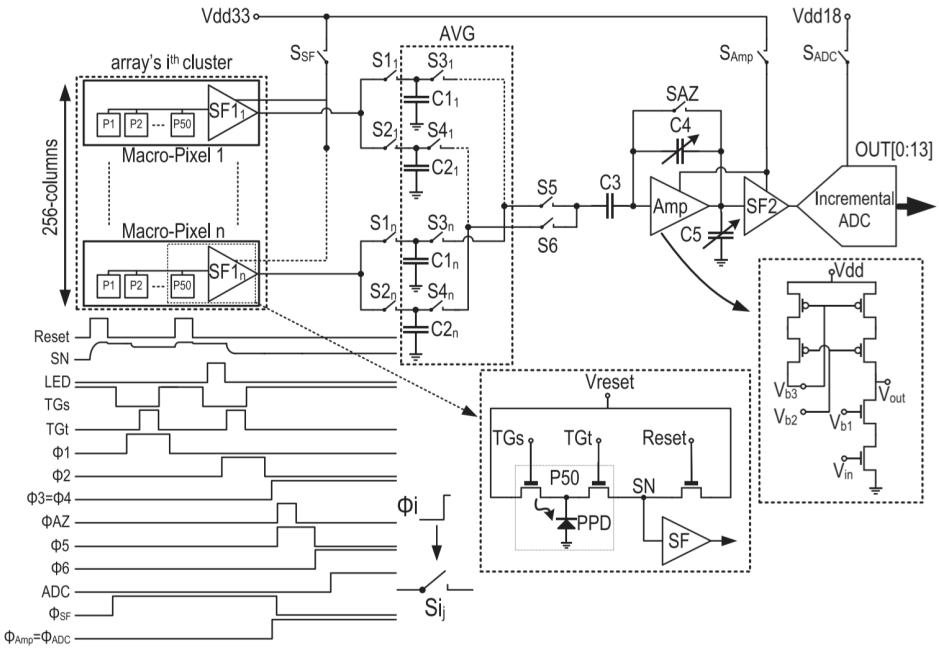


Figure 2.5: Proposed pinned photodiode PPG sensing chain as in [8]

### 2.4.3. MONOLITHIC RESPONSIVITY ENHANCED PHOTODIODE PPG SENSOR

The work [10] in 2021 presents a monolithic PPG solution that incorporates quantum-efficiency-enhanced PDs and its readout circuit (Figure 2.6). The photodiodes are specially enhanced using thicker Si, thicker anti-reflection layer and back-side scattering structure. The responsitivity at infra-red improves by 4.6 times compared with conventional image sensors. Hence, they are sensitive to green, red and infra-red and can serve for more test requirements than heart-rate monitoring.

The readout chain has a transimpedance amplifier, a programmable gain amplifier (PGA) and a sigma delta modulator. The intermediate PGA stage helps ambient light cancellation, low frequency noise reduction and dynamic range extension. However, it needs static current during the observation window and inevitably increase readout power consumption. This work reports a readout power consumption of 24 $\mu$W with a sample rate of 20 Hz. It does not report the power consumption of LED, which can be deduced from its measurement setup and the reported LED duty cycle to be around 7 $\mu$W. The die area is 5.5 mm$^2$.

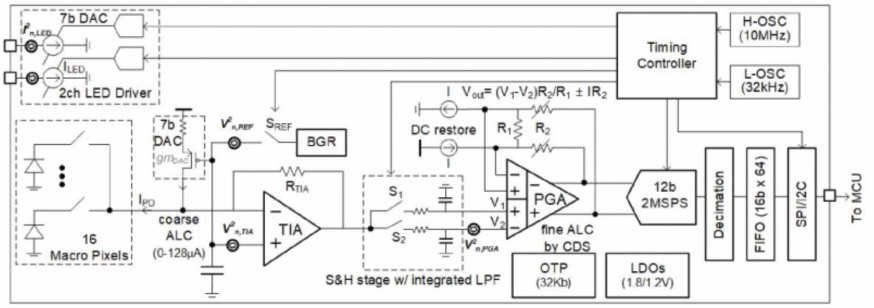


Figure 2.6: Proposed responsitivity-enhanced photodiode PPG sensing chain as in [10]

### 2.4.4. SUMMARY OF STATE-OF-THE-ART WORK

Table 2.1: Summary of state-of-the-art work

| Parameters | Unit | ISSCC'21 | TBioCAS'19 | ESSCIRC'17 |
|---|---|---|---|---|
| **Technology** | nm | 65 | 180 | 180 |
| **Sampling frequency** | Hz | 20 | 40 | 160000 |
| **Readout SNR**[a] | dB | 90 | 75 | 72 |
| **LED duty cycle** | % | 0.04 | 0.07 | 10 |
| **LED power consumption** | $\mu$W | 6[b] | 1.97 | N/A |
| **Readout power consumption** | $\mu$W | 24 | 2.63 | 13-25 |
| **Chip area** | $mm^2$ | 5.5 | 20 | 1.792 |

[a] At a sinusoidal input 1dB below full scale to avoid overrange, excluding the sensor front end noise, e.g. photon shot noise.
[b] Approximated from its measurement setup and the reported LED duty cycle.

The table above summarises the prior academic art that has implemented a monolithic PPG sensing system. Since the primary motivation for this project is power-efficiency, the PPD CMOS image sensor configuration is promising. However, as stated, a PPD device requires additional processing on top of standard CMOS technology, which is not a cost-effective choice. Since the company supporting this project aims to explore CMOS imager, photogate imager sensors are deployed as front-ends that can be fully integrated with standard CMOS.

# 3

# A SENSOR FRONT END - A PHOTOGATE IMAGE SENSOR

In this chapter, a detailed introduction to the sensor front ends, the photogate image sensor will be presented. The chapter starts with the working mechanism. Then, a parametric noise analysis based on a classic readout structure is presented. The noise analysis part incorporates parametric analysis of thermal noise, flicker noise, shot noise and quantisation noise.

## 3.1. THE PHOTOGATE IMAGE SENSOR



The active-pixel sensor has been developed to serve as an alternative to the traditional charge-coupled device (CCD) for image capture. It has advantages in terms of cheap and easy integration with image sensing circuits, low power consumption, and higher immunity to photo-charge leakage from/to adjacent pixels [22] [23].

### 3.1.1. WORKING PRINCIPLE

The photoage image sensor is a typical application of active pixel sensors, and can be completely fabricated in standard CMOS technology. For a better understanding of its working principle [24], Figure 3.1 illustrates the cross section of a photogate imager and its corresponding operating timing diagram.

(1) The photogate covered by polysilicon is first biased at a certain high potential, say $0.9 \times V_{dd}$.

(2) The reset switch (RST) turns on, removing any residue charge in the floating diffusion (FD) node from the previous sample. This resets the potential of FD to one $V_{TH}$ below $V_{dd}$, with a certain noisy reset thermal noise voltage level also sampled.

(3) LED turns on. Photogenerated carriers are collected under the gate oxide and then stored in the "PD" diffusion node. Received optical photons generate electric charges in a fixed ratio that known as quantum efficiency.

(4) PG pulls down and the transfer gate (TX) turns on. The channel beneath TX is created and there is a potential difference between PG and FD. Therefore, photogenerated carriers (charges) start to flow from the PD area towards the FD.

(5) The FD node senses a voltage difference, according to the equation: $\Delta V_{FD} = \frac{Q}{C_{FD}}$

(6) To allow the signal to be sampled by the readout backend, $V_{FD}$ is first buffered by a source follower (SF, blue dotted area). Meanwhile, $S_1$ turns on after RST to sample the reset level and low frequency flicker noise from SF to $C_1$ and $S_2$ turns on after TX to sample the reset noise, flicker noise and signal level to $C_2$. These two signals stored in $C_1$ and $C_2$ will be subtracted in the readout circuit. The mechanism is called correlated double sampling (CDS). Therefore, by using this active pixel sensor CDS operating scheme, the reset noise and flicker noise from the SF can be effectively cancelled, improving the overall signal to noise ratio (SNR).

The floating diffusion node is also referred to as the sensor node (SN), simply because it provides sensing.

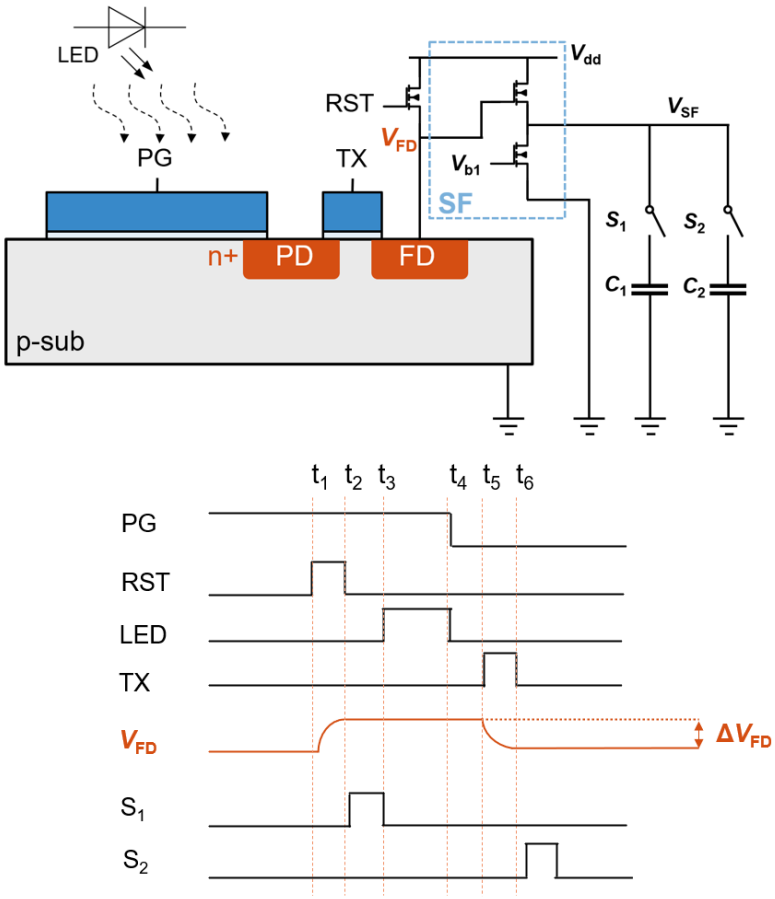


Figure 3.1: CMOS photogate sensor cross-section architecture with operating timing diagram per frame

## 3.2. PIXEL DESIGN

The company that supports this project has a design for a photogate sensor [25]. Each photoage sensor size is 10 $\mu m$ × 12 $\mu m$ and its FD node's full well capacity (FWC, $N_{sat}$) is $4.8 \cdot 10^4$, with sufficient charge transfer and low dark current. The potential change at the FD node is 0.39 V, if FWC is reached. The quantum efficiency, referred to as the ratio of the number of electrons generated beneath PG to the number of incident photons, at the wavelength of interest (530 nm) is 0.4. The fill factor (FF), referred to as the ratio of the light sensitive area to the full pixel unit area, is 0.7.

## 3.3. LED EXPOSURE TIME

The LED will be populated offchip but on PCB. A typical choice of the off-the-shelf LED is SFH7060 by Opto Semiconductors [26]. The required LED exposure time to fully charge FD of one single pixel can be derived from:

$$t = \frac{N_{sat} \times \frac{hc}{\lambda}}{QE \times FF \times Area_{unit} \times I_e}, \tag{3.1}$$

where $QE$ stands for quantum efficiency of the light sensitive area,
$FF$ stands for fill factor $\frac{Area_{lightsensitive}}{Area_{unit}}$,
$Area$ is the area of pixel, i.e., 120 $\mu m^2$
$I_e$ refers to the radiant intensity, 0.5 $mW/cm^2$ for this LED.
$\frac{hc}{\lambda}$ is photon energy.

Solving this gives $t = 0.173\ ns$. This also means that for every $4.8 \cdot 10^4$ number of electrons that is wanted to be collected at the FD node, the LED needs to be turned on for 0.173 ns.

## 3.4. PARAMETRIC PHOTOGATE IMAGER NOISE ANALYSIS

In this section, noise analysis for a typical readout chain for photogate pixels will be presented. Figure 3.2 shows a top level block diagram for the conventional source follower (common drain stage) based PG imager readout chain, with different kinds of noise sources indicated. The basic signal chain includes a pixel, a source follower, a column level amplifier, and an analog-to-digital converter. The noise contributors are pixel's shot noise, source follower's thermal and flicker noise, amplifier's thermal and flicker noise and quantisation noise.



All noise sources inside the pixel and outside the pixel (i.e., from the readout chain) will be analysed separately. All noise sources will eventually be referred to the input side, i.e., the FD node. For simplicity, sampling noise will be temporarily ignored, because the impact of different CDS techniques on it differs.

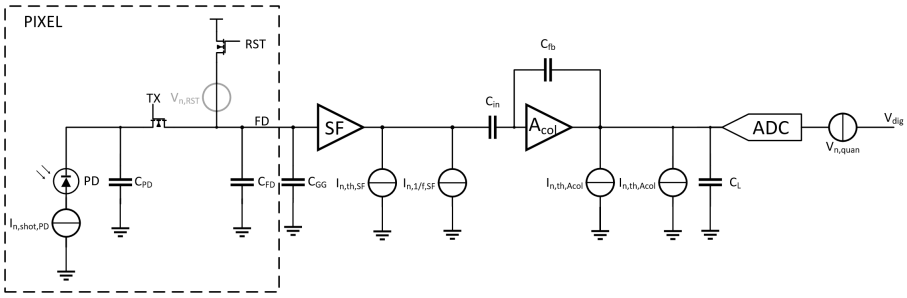


Figure 3.2: Top level block diagram of the photogate pixel readout chain with different noise sources

### 3.4.1. ANALYSIS METHOD

A systematic way of analysing noise is by deriving its output-referred noise and then referring it back to the input side with proper conversion parameters. Therefore, it is important to obtain the overall conversion gain and the transfer functions of each noise sources to the output.

For the overall conversion gain, it is simple by assuming the column level amplifier has a gain of $A_{col} = \frac{C_{in}}{C_f}$. In terms of pixel conversion gain, that is, from the charge received at the FD node to the voltage generated at the same node, it can be approximated to:

$$A_{CG} \approx \frac{1}{C_{FD} + C_{GG}}, \tag{3.2}$$

where $C_{FD}$ is the capacitance of the floating diffusion node and $C_{GG}$ is all parasitic capacitors referring to ground at that node, which includes the reset switch's gate to

source capacitor, the source follower's gate to drain and the source follower's gate to source capacitor. Other parasitic capacitances, such as those originating from metal routing, are ignored for now.

For the transfer functions of each noise source to the output, Figure 3.3 presents a small signal diagram, which helps in deriving the transfer functions. Compared with Figure 3.2, it ignores the shot noise from the pixel, since it is already referred to input.



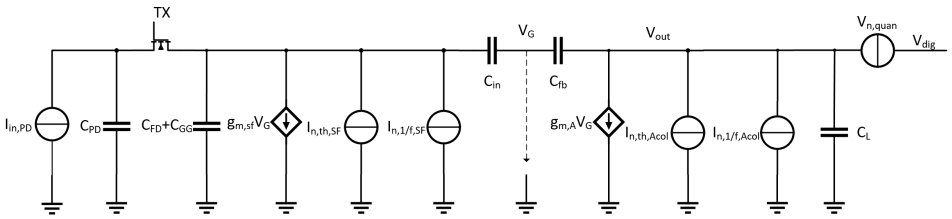


Figure 3.3: Small signal diagram of the photogate pixel sensor and its classical readout chain, showing flicker and thermal noise

The pixel's photodiode is basically a charge-transfer device modelled as a current source. In order to transfer the source follower's two noise sources, two transfer functions are needed: one for the noise transfer function of the source follower and the other for the signal transfer function of the column level amplifier. Similarly, in order to transfer the amplifier's thermal noise, an amplifier noise transfer function is required.

The noise transfer function is calculated at the output of the corresponding signal path. From the small signal diagram in Figure 3.3, the noise transfer function for the noise generated by the source follower referred to its output (i.e. the input of the column-level amplifier) is calculated by:

$$H_{n,pix}(f) = \frac{\frac{1}{g_{m,SF}} \cdot A_{CG} \cdot (C_{GG} + C_{FD})}{1 + j\frac{f}{f_{c,pix}}}, \tag{3.3}$$

where $f_{c,pix}$ is the cutoff frequency of the in-pixel SF, given by $f_{c,pix} = \frac{1}{2\pi} \cdot \frac{g_{m,SF}}{A_{CG} \cdot C_{in} \cdot (C_{GG} + C_{FD})}$.

The transfer function of the amplifier can be obtained as:

$$H_A(f) = -\frac{A_{col}}{1 + j\frac{f}{f_{c,A}}}, \tag{3.4}$$

where $f_{c,A}$ is the cutoff frequency of the column-level amplifier, given by $f_{c,A} = \frac{1}{2\pi} \cdot \frac{g_{m,A}}{(A_{col}+1) \cdot C_L + C_{fb}}$. $C_L$ is the load capacitor and $C_{in}$ the input integrating capacitor for the amplifier.

Similarly, the noise transfer function required to refer noise originating from the column-level amplifier to its output can be obtained by:

$$H_{n,A}(f) = \frac{\frac{1}{g_{m,SF}} \cdot (A_{col} + 1)}{1 + j\frac{f}{f_{c,A}}} \tag{3.5}$$

## 3.5. SHOT NOISE



In this section, the shot noise or Poisson noise in the system will be discussed in detail. It can be seen in Figure 3.2, that the transistor's shot noise due to leakage current is not presented. The reason is that the shot noise in the photodiode introduced by the impinging light photons has a dominant role. The noise variance of the photodiode's shot noise is simply equal to the mean value of incident photons [27]. After converting it to the charge domain, it can be given by:

$$Q_{shot}^2 = N \cdot q^2, \tag{3.6}$$

where $N$ is the number of incident photons per pixel and $q$ is the elementary charge in the unit of Coulomb.

Equation 3.6 shows the shot noise is originated from and dominated by the significant high value of the incident number of photons, up to a few thousands per pixel area (1 $\mu m$), based on the different pixel design. Therefore, it is reasonable to neglect the leakage current shot noise due to tunnelling resulting from barrier control processes.

## 3.6. THERMAL NOISE

In this section, the thermal noise in the system will be analysed. The most significant thermal noise originates from the channel in the transistors. In this case, only thermal noise from the source follower and the column level amplifier is considered. The reason is that the column-level amplifier has a sufficient gain to suppress the noise contribution of the next stages. Also, the thermal noise due to the reset switch is neglected, since it can be cancelled by correlated double sampling as described in Section 3.1.1.

The current noise PSD of the column-level amplifier is well known as [28]:

$$S_{I,th,Acol} = 4kT \cdot \gamma_A g_{m,A} \tag{3.7}$$

Similarly, the current noise PSD of the source follower is:

$$S_{I,th,SF} = 4kT \cdot \gamma_{SF} g_{m,SF} \tag{3.8}$$

The thermal noise contribution of the column-level amplifier in the charge domain, referred to the FD node, can be calculated by combining 3.5 and 3.7 using:

$$\bar{Q}^2_{th,A} = \frac{1}{A^2_{col} \cdot A^2_{CG}} \int_0^\infty S^2_{I,th,Acol} \times |H_{n,A}(f)|^2 df \tag{3.9}$$

Solving this gives:

$$\bar{Q}^2_{th,A} = \frac{kT \cdot \gamma_A}{((A_{col}+1) \cdot C_L + C_{fb}) \cdot A^2_{CG}} \tag{3.10}$$

Similarly, the thermal noise contribution from the source follower, referred to the same FD node, can be calculated by combining 3.3,3.4, and 3.14:

$$\bar{Q}^2_{th,SF} = \frac{1}{A^2_{col} \cdot A^2_{CG}} \int_0^\infty S_{I,th,SF} \times |H_A(f)|^2 \times |H_{n,pix}(f)|^2 df \tag{3.11}$$

Hence:

$$\bar{Q}^2_{th,SF} = \frac{kT \cdot \gamma_{SF}}{C_{in} \cdot A^2_{CG}} \tag{3.12}$$

Since the amplifier and source follower's thermal noise are uncorrelated, the total input referred thermal noise can be obtained by:

$$\bar{Q}^2_{th,tot} = \frac{kT}{A^2_{CG}} \cdot \left(\frac{\gamma_{SF}}{C_{in}} + \frac{\gamma_A}{((A_{col}+1) \cdot C_L + C_{fb})}\right) \tag{3.13}$$

## 3.7. FLICKER NOISE

The MOSFET's gate oxide and silicon substrate interface is where the flicker noise is generated. When the silicon crystal reaches an end at this interface, "dangling" bonds develop, generating new energy states. These energy states randomly trap charge carriers when they move at the interface. THus, a noisy flicker current is introduced into the gate current. This is a typical mechanism, although some other mechanisms are still under discussion for the formation of flicker noise [28].

The flicker noise PSD is widely known to be inversely related to transistor area, as roughly modelled by [28]. This section only analyse the source follower's flicker noise. Applying similar analysis to the amplifier's flicker noise is straightforward.

The current noise PSD of the source follower's flicker noise can be expressed as:

$$S_{I,flicker,SF} = \frac{K_F \cdot g_{m,SF}^2}{C_{ox} \cdot W \cdot L \cdot f}, \tag{3.14}$$

where $K_F$ is in the flicker noise coefficient, in the unit of $[J]$, usually in the order of $10^{-25}$

Similarly as source follower's thermal noise, the input referred noise variance in the charge domain can be calculated using 3.3, 3.4, and 3.14:

$$\bar{Q}_{flicker,SF}^2 = \frac{1}{A_{col}^2 \cdot A_{CG}^2} \int_0^\infty S_{I,flicker,SF} \times |H_A(f)|^2 \times |H_{n,pix}(f)|^2 df \tag{3.15}$$

It is tricky to solve equation 3.15 above by hand, due to the divergence at 0 Hz. A different approach can be taken by assuming the interest band for flicker noise is from 100 Hz to the corner frequency of flicker noise. For now, the starting frequency 100 Hz is chosen as the reciprocal of a very generous conversion time, 10 ms. The corner frequency can be obtained by equalising the flicker noise and thermal noise:

$$\frac{K_F \cdot g_{m,SF}^2}{C_{ox} \cdot W \cdot L \cdot f_c} = 4 \cdot kT \cdot g_{m,SF} \cdot \gamma_{SF} \tag{3.16}$$

Hence:

$$f_c = \frac{K_F \cdot g_{m,SF}}{4 \cdot kT \cdot \gamma_{SF} \cdot C_{ox} \cdot W \cdot L} \tag{3.17}$$

Then similarly find the integral and divide by the transfer gain:

$$\bar{Q}_{flicker,SF}^2 = \frac{1}{A_{col}^2 \cdot A_{CG}^2} \int_{100}^{f_c} S_{V,flicker,SF} = \int_{100}^{f_c} \frac{K_F}{C_{ox} \cdot W \cdot L \cdot f} df \tag{3.18}$$

## 3.8. QUANTIZATION NOISE

The quantization noise due to analog to digital conversion can be easily derived in the charge domain as:

$$\bar{Q}_{quantization}^2 = \frac{(\frac{V_{ref}}{N_{bit}})^2}{12 \cdot A_{col}^2 \cdot A_{CG}^2} \tag{3.19}$$

Up to this point, all related noise sources that are worth analysis have been discussed and calculated for a photogate imager and its classical readout chain.

# 4

# SYSTEM LEVEL DESIGN AND ANALYSIS

In this chapter, the readout architecture used in this project will be presented, followed by a numerical analysis of key design aspects, such as noise, power consumption, and speed. Moreover, the final decision on these design aspects will be traded off and then summarised.

## 4.1. PROPOSED ARCHITECTURE

This section proposes the readout architecture. The key of the readout chain is an analog-to-digital converter (ADC). According to [29], three typical types of ADC are used for biomedical low-frequency sensing systems, namely the incremental sigma delta ADC (IADC), the (dual) slope ADC and the successive approximation register (SAR) ADC. Given the same resolution and clock period, the IADC and slope ADC require significantly longer conversion times, indicating more static energy consumption. Moreover, sigma-delta modulators require oversampling, which means that the LED must be turned on multiple times to extract multiple $\Delta V_{SF}$ but these multiple $\Delta V_{SF}$ serve only for one sample. This is additional energy consumption that should be avoided. Therefore, from the energy-efficient perspective, the SAR ADC is chosen.



In this section, a compact design will be introduced that mainly includes two phases, the charge transfer and the charge-redistribution SAR ADC. Moreover, several auxiliary blocks, such as a comparator and digital control units, will be presented briefly at the building-block level, and details of them will be explained in the next chapter. The working principle will be described first stage by stage and then as a whole.

### 4.1.1. PHASE-1, INVERTING VOLTAGE AMPLIFICATION

Figure 4.1 shows a charge amplifier and two capacitors that form a feedback network for inverting voltage amplification. As described in Figure 3.1, the output of the source follower or the input of $C_{in}$ (i.e., node $V_{SF}$ in the figure) experiences a voltage change, $\Delta V_{SF}$. While $V_{in1}$ is taken as a steady virtual ground voltage equals to $V_{cm1}$, since the amplifier $A_1$ is usually taken as having a very large gain. The moment when the left plate of $C_{in}$ experiences a voltage change, the charge in it has no where to go but distribute to $C_{fb}$, which effectively brings node $V_{out}$ up, and hence $\Delta V_{out} = \Delta V_{SF} \frac{C_{in}}{C_{fb}}$.

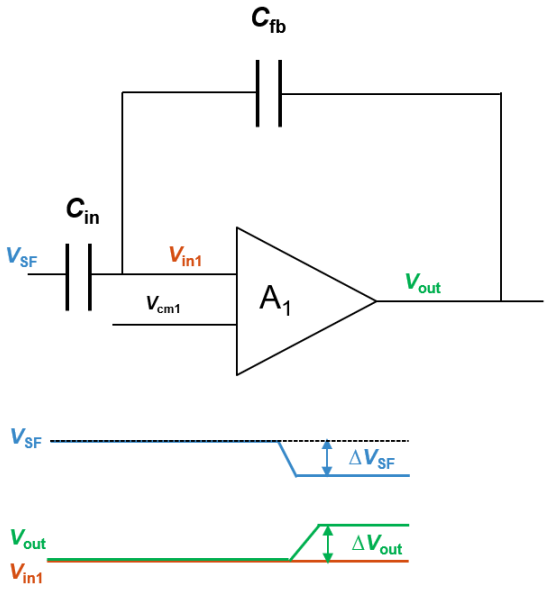


Figure 4.1: Phase-1, charge transfer, with node voltage annotated

### 4.1.2. PHASE-2, SAR ANALOGUE TO DIGITAL CONVERSION

In the second phase, a compact SAR conversion is performed. The feedback capacitors are actually in the binary capacitive-digital-to-analog-conversion (CDAC) format, which was connected in parallel to node C to form a closed loop in the previous phase. Then $C_{fb}$ is disconnected from the closed loop, and their right plates are immediately charged by $V_{ref+}$. Meanwhile, $C_{in}$ is disconnected from node $V_{in1}$ to prevent any charge from flowing into or out of it. Since it is now an open loop, node B is no longer a virtual ground and it will see a immediate voltage increase. After this, the same amplifier $A_1$ now serves as a pre-amplifier for the comparator stage, which means that node C swings from rail to rail. Finally, a classical SAR search pattern follows to redistribute the charge in the CDAC-$C_{fb}$ , using the comparator and the SAR control unit. The unit capacitors are neutralised one by one.

The comparator's offset and noise often leads to comparison error. Nevertheless, the pre-amplifier can effectively attenuate these nonidealities, if referring them to the input node $V_{in1}$. Designing a new preamplifier results in complex circuit design and requires an additional nonlinearity control mechanism. Therefore, the amplifier $A_1$ serves as a pre-amplifier for a fast and reliable comparison result in a compact architecture.

The comparator has a clocked dynamic architecture, which consumes no static current and has better synchronisation with SAR conversion.

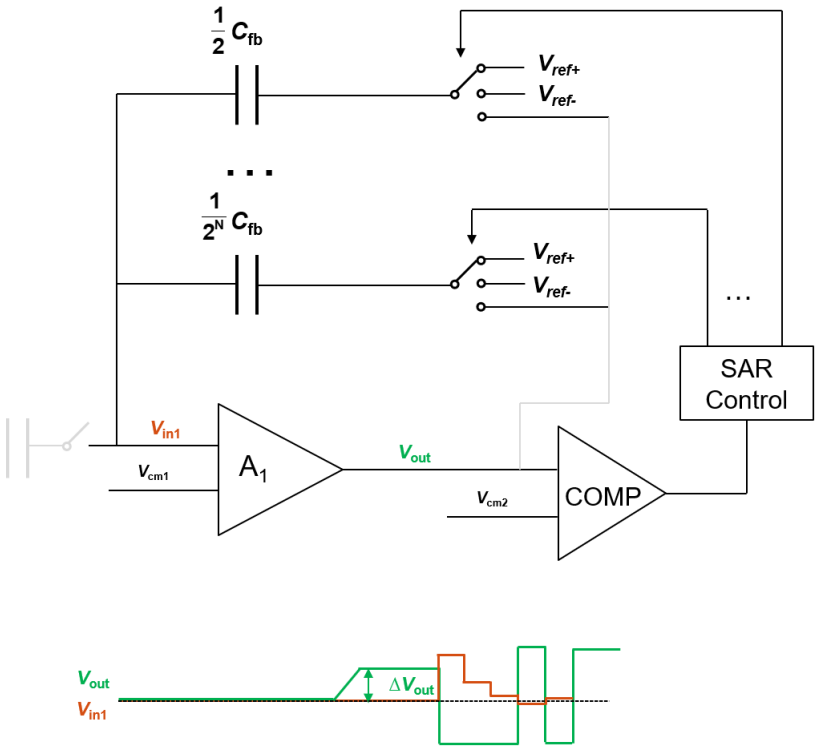


Figure 4.2: Phase-2, SAR ADC, with node voltage annotated

### 4.1.3. ARCHITECTURE WITH TIMING DIAGRAM

Figure 4.3 and 4.4 below illustrate the proposed architecture and its timing diagram. The overall working mechanism per time period explains as follows:

$t_1 - t_2$ In order to reduce amplifier's flicker noise, an autozeroing technique is deployed. The basic working principle is: First turn on $S_1$, $S_2$ and $S_3$ and hence amplifier's low-frequency nonidealities are effectively stored in $C_{AZ}$ by shortening the inputs to the common mode; Then, $S_1$ is off and the pair of auxiliary AZ transistors is continuously injecting mismatched current, which cancels the nonidealities existed in the time periods of interest, i.e., as of $t_2$.



$t_4 - t_5$ To clear any residue charge in the feedback CDAC from previous sample, a reset period is employed by turning on $S_4$. Equally important, the single pole three throw (SP3T) switches now connect the right plate of capacitors to the feedback network, i.e., node $V_{out}$.

$t_6 - t_7$ This is phase-1 for charge transfer as described in Section 4.1.1.

$t_8 - t_9$ This is phase-2 for SAR conversion as described in section 4.1.2. In this period, $C_{in}$ is disconnected from the loop and is placed at the common-mode voltage by turning off $S_2$ and turning on $S_3$ until the next sample arrives.

As of $t_9$ The whole system stays idle before going into the next power-up cycle.

The rest of periods ($t_2 - t_4$, $t_5 - t_6$ and $t_7 - t_8$) are dedicated non-overlapping periods, which in reality does not have such comparable lengths as drawn in the figure.

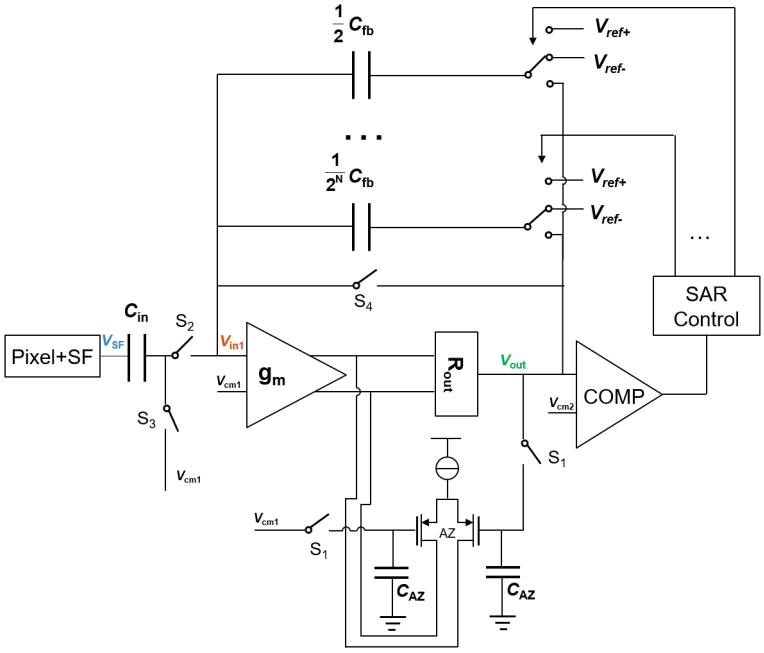


Figure 4.3: Proposed architecture (main amplifier drawn in $g_m - R_{out}$ way)

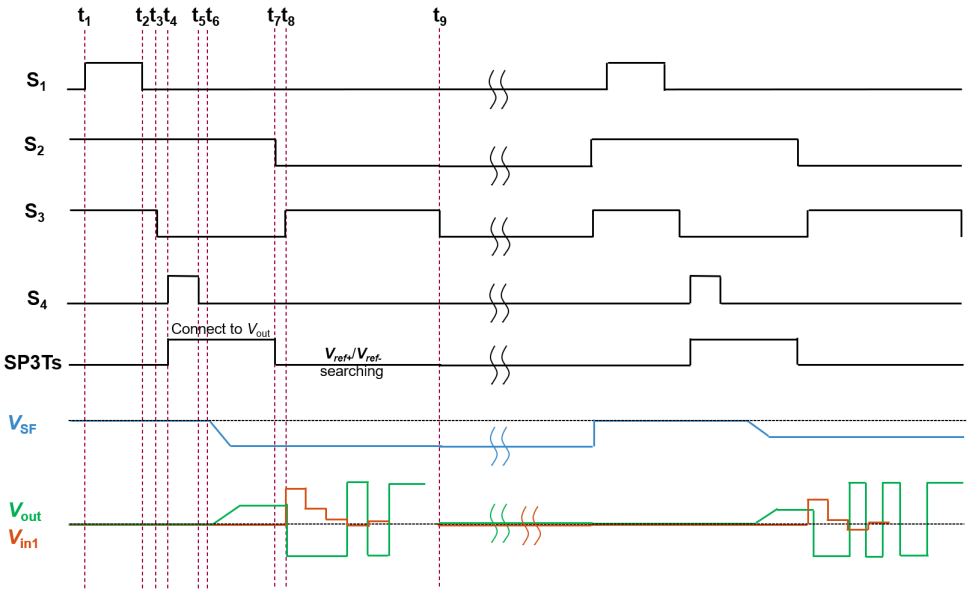


Figure 4.4: Timing Diagram. (not drawn to the scale)

## 4.2. SYSTEM LEVEL ANALYSIS

This section presents a system-level analysis. The system includes the LED, the pixel sensors and the readout circuit introduced in Section 4.1. This section analyses key design aspects, signal-to-noise ratio (SNR), power, ADC resolution, capacitor sizing and required number of pixels. These subsections of the analysis conclude with the proposal of design parameters that would be used in transistor-level design.

### 4.2.1. ENERGY CONSUMPTION PER SAMPLE



The work in [8] reports a total of 4.6 $\mu W$ of total power consumption to monitor the minimum detectable PPG signal (i.e., SNR = 30 dB), where 1.97 $\mu W$ is burnt in LED and the rest 2.63 $\mu W$ is consumed by readout circuits (AFE + ADC) with a sampling rate of 40 Hz. Nevertheless, the LED power consumption is a complex benchmark, where wavelength, PI of the test location, sensor quantum efficiency, LED's viewing angle, and even the algorithm used in signal processing can bring difference. The readout energy consumption per sample is 66 nJ/sample. In this work, we propose that readout energy consumption < 20 nJ/sample and LED energy consumption as low as possible.

The dynamic comparator does not consume static power and the digital circuit's power consumption is fairly low and can be temporarily ignored. A rough division can be that half of the energy is burnt in the source follower, whereas the rest half consumed in the main amplifier.

### 4.2.2. CAPACITOR RATIO

In order to find the capacitor ratio, the signal swing should be considered. The pixel designer reports a typical full well $V_{FD,pp}$ of 0.4 V according to his simulation as said. Assume that a typical operational amplifier(op-amp) swings 1 V with $V_{dd}$ = 1.8 V. An intuitive choice for the feedback gain can be 2x so that signal swings within the op-amp's allowable swing range. However, since this is a brand new pixel without any previous measurement result, a safe margin should be reserved to prevent it swings out of the rail. Therefore, 1x feedback gain is chosen, that is, $\frac{C_{in}}{C_{fb}} = 1$.

### 4.2.3. SIGNAL TO NOISE RATIO

The whole system is designed to monitor heart rate, and hence its accuracy is important. A maximum average heart-rate error of 1% should be guaranteed. For simplicity, we assume the detection error mainly comes from the system's noise.

To find the relationship between SNR and accuracy, a MATLAB model was created:

(1) Extract a noiseless PPG signal from the database in [30] that was obtained from a real body and normalize it. This normalized signal is actually AC signal of interest $S_{AC}$.

(2) Find the number of local maxima in both signals in (1) and using the MATLAB function called *"findpeaks"*, with a parameter *"MinPeakProminence"* being half of $V_{pp,AC}$. The number of local maxima in this noiseless plot is regarded as the accurate heart-beat count.

(3) To make a noisy PPG signal, uniformly distributed random noise level with a certain standard deviation ($\sigma$) was added to every sample of the signal in (1). And then normalise it.

(4) Count the number of peaks in the noisy signal and find the relative error of the heart-beat counts. SNR can be calculated from $SNR = 20\log 10(\frac{V_{pp,AC}}{\sigma})$

(5) Repeat step (1) - (4) by injecting noise with different standard deviation.

(6) Plot the curve about relative heartbeat error versus SNR and fit it exponentially.

Figure 4.5 presents the fact that in order to achieve as little as 1% heart-rate error, an SNR of 20 dB should be guaranteed. Nevertheless, other non-idealities, such as signal drift due to temperature and body motion, can distort the signal and make the algorithm less sensitive. This though can be solved by sophisticated algorithm design, but a more sensible choice in analogue domain is to reserve margin in the SNR target. Therefore, 25 dB SNR is targeted.

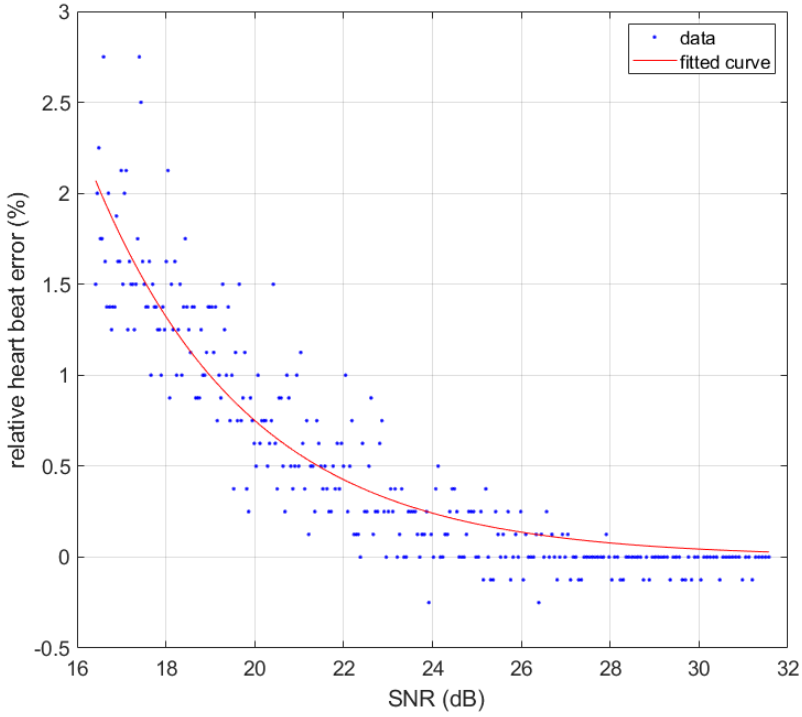


Figure 4.5: Heart-rate error versus SNR, raw data (blue) and exponential-fitted curve (red)

### 4.2.4. NUMBER OF PIXELS

The required number of pixels (n) directly relates to system's SNR requirement, 25 dB as said in the previous section.

$$SNR = 20log_{10}(\frac{N_{AC}}{\sqrt{\sigma^2_{shot} + N^2_{n,rms,readout}}}) = 20log_{10}(\frac{PI \times n \times N_{sat}}{\sqrt{n \times N_{sat} + (\frac{V_{n,read} \times n \times C_{FD}}{q})^2}}) \tag{4.1}$$

The system noise contains pixel's shot noise and readout noise, it is quite tricky at this stage to predict the readout noise. To find the required number of pixel, if we consider shot noise only, a safe way is to round the SNR requirement from 25 dB up to 30 dB to accommodate the uncertain readout noise:

$$SNR = 20log_{10}(\frac{N_{AC}}{\sigma_{shot}}) = 20log_{10}(\frac{PI \times n \times N_{sat}}{\sqrt{n \times N_{sat}}}) \tag{4.2}$$

Substitute $N_{sat} = 4.8 \times 10^4$, and worst PI=0.2% in equation 4.2 and solve for n = 5100. Round it to 5000.

Connecting all 5000 pixels simultaneously leads to a large $C_{FD}$. When it works below the FWC of $5000 \times 4.8 \times 10^4$, this capacitance does not decrease. However, because the readout noise does not change with operating in FWC or not, these capacitance provides a large constant noise multiplier to the readout noise, means a degrading to the overall SNR. Therefore, these pixels will be divided into two clusters, each of which has 2500 pixels. Only one cluster is turned on to handle most measurement conditions, and both are turned on to handle worst or close to worst conditions. These pixels in a cluster end up in distributing as parallel pixel arrays, more information about the exact division will be provided in Section 4.3 and 5.5.

### 4.2.5. NOISE-POWER TRADE OFFS



The shot noise in the system changes with the input photons, whereas the readout noise (mainly thermal and quantisation noise) is constant for a fixed noise bandwidth that depends on the transistor design. Section 3.3 shows that LED power consumption is linearly proportional to the collected number of electrons, and Equation 4.1 shows that low readout noise is beneficial for reducing the number of electrons to achieve the same SNR. Therefore, low readout noise can help reduce the power consumption of the LED.

In order to find how much LED power reduction can be achieved, a quantitative sweep model has been implemented. It is under the condition that all 5000 pixels are switched in with 10 % PI. The number of impinging photons increases and the SNR can be calculated based on Equation 4.1. The SNR can then be plotted versus the incident photons. Three readout noise rms scenarios, 10 $\mu V$, 50 $\mu V$ and 100 $\mu V$ were swept. The result is as Figure 4.6 below shows:

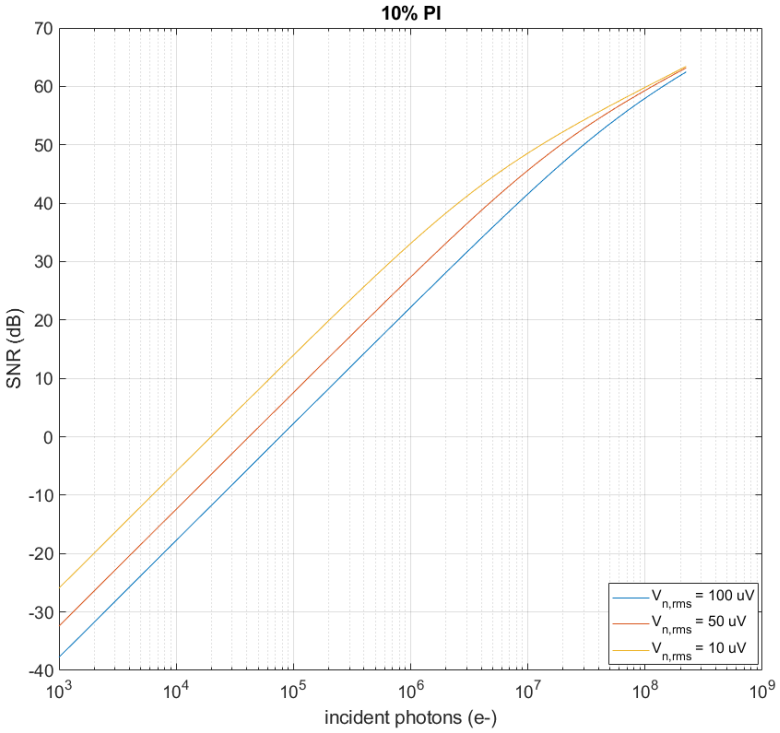


Figure 4.6: Whole system's SNR versus the number of input photons, when readout noise rms value varies from 10 $\mu V$, 50 $\mu V$ to 100 $\mu V$ for 10% PI

Figure 4.6 presents the results that when PI is 10 %, shot noise is dominant when 5000 pixels operate close to the overall FWC, $2.4 \times 10^8$. When operating with a lower number of incident photons, say around $10^6$, readout noise dominates. Given the number of incident photons is linearly proportional to LED power consumption, one fact is that the system with low readout noise can consume a lower amount of LED power to achieve the same minimum SNR of 25 dB. A 4x reduction in LED power can be predicted, compared $V_{n,rms}$ = 10 $\mu V$ with $V_{n,rms}$ = 100 $\mu V$. Nevertheless, this does not indicate that the readout noise should be suppressed as low as possible in order to achieve low LED power consumption, because low readout noise effectively translates to high readout power consumption.

In order to find a good trade-off between LED power and readout power, a model that simulates the total energy consumption required per sample to monitor the lowest detectable signal (SNR = 25 dB) versus readout noise is built as follows:

(1) Sweep the SNR versus the number of incident photons in different combinations of PI and $V_{n,rms}$, using the model deployed for Figure 4.6. It investigated 4 PI

scenarios, including the strongest 20 % , the weakest 0.2 % and two intermediate values, 1 % and 5 %. And the $V_{n,rms}$ was swept in the range of 1 $\mu V$ - 500 $\mu V$, which was chosen based on a rough estimation of the readout noise.

(2) Find the number of incident photons required for SNR to reach 25 dB.

(3) Convert the number of photons and readout noise to LED energy consumption and readout energy consumption, respectively.

i. The number of received/incident photons N can be translated into the exposure time of LED as discussed in Section 3.3. Knowing the LED exposure time, the LED energy consumption is fairly straight forward.

ii. To link the readout noise with readout energy consumption, following steps are required:

a. Assume flicker noise is fully cancelled.

b. $C_{fb}$ can be obtained by solving:

$$V_{n,rms}^2 = V_{n,th}^2 + V_{n,sample}^2 = 2 \times \alpha \frac{kT\gamma}{C_{fb}} + \frac{kT}{C_{in}}, \tag{4.3}$$

where $V_{n,th}$ is the thermal noise in the voltage domain referred at the output of the amplifier, which can be derived from Equation 3.13. $V_{n,sample}$ denotes sampling noise, which is $\frac{KT}{C_{in}}$. $\alpha$ denotes noise excess factor, taking 4 as a worst case according to [31].

c. Assume a simplified single-pole (first-order) system, and hence the settling behaviour is exponential. And the settling slope is 8.6 dB/$\tau$. This $\tau$ is often referred to as $\tau_{8.6dB}$. The first phase needs to settle within the noise rms value. Hence, the required settling accuracy is given by $20 \times \log(0.4/V_{n,rms})$. Settling time is chosen as 5 $\mu$s as the pixel settling speed. Therefore:

$$\tau_{8.6dB} = \frac{\frac{C_{fb}}{1+1/Gain}}{g_m} = 5\ \mu \div \frac{20 \times \log(0.4/V_{n,rms})}{8.6} \tag{4.4}$$

d. Combine equation 4.3 and 4.4, $g_m$ can be solved to be only related to the change of $V_{n,rms}$.

e. The minimum corner frequency of flicker noise limited by this technology is about 500 Hz to avoid unrealistically large size of transistors that contribute flicker noise. Therefore, the longest power-up time for the static amplifier is around 2 ms to ensure that the autozeroing can store and cancel the flicker noise. 2 ms power-on time is a worst case, which in reality

f. Having specified the power-up time, we can find the readout energy consumption that is linearly proportional to $g_m$ obtained in step d.

(4) Add LED energy consumption and readout energy consumption, and plot the total energy consumption against $V_{n,rms}$ for different PI values as Figure 4.7.

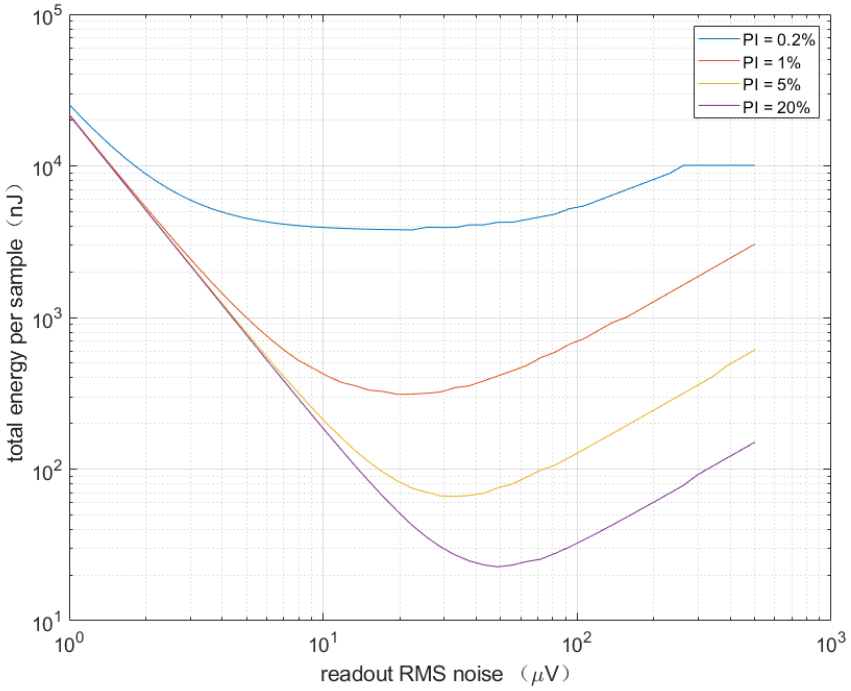


Figure 4.7: Whole system's energy consumption versus the average readout noise, under different PI conditions (0.2%, 1%, 5% and 20%)

Figure 4.7 shows that squeezing the readout noise to a minimum does not bring any system-level energy saving, since the readout energy consumption dominates. On the other hand, higher readout noise means lower readout energy dissipation, but at the cost of burning more LED energy to reach 25 dB. This figure shows that when the average readout noise is within the range of 20 $\mu V$ – 60 $\mu V$, an energy consumption close to the minimum value could be obtained, regardless of the perfusion index. The minimum LED turn-on time is 130 ns when the readout noise is 20 $\mu V$ under 20 % PI, which is possible as long as the duty frequency of the LED is high enough, as the datasheet provides that the rise time of the radiant intensity is 32 ns.

The flat segment when $PI = 0.5\%$ is because in the readout noise dominant area, if the signal of interest is too low, SNR fails to reach 25 dB even when pixels operate in FWC. In FWC, the LED power stops increasing while the readout power is negligible in this scenario and hence it clips. This implies that a higher number of pixels is required as a backup solution to prevent the case when the signal-of-interest is too low.

The desired range of readout noise also gives a clear prediction of required $g_{m,A}$ that should falls in the range of 7.1 $\mu S$ to 72 $\mu S$. Moreover, another important design parameter, $C_{fb}$ falls in the range of 8 pF to 72 pF.

### 4.2.6. ADC RESOLUTION

The quantisation noise should be lower than the thermal noise sampled in the CDAC.

$$V_{n,quan}^2 < V_{n,thermal}^2 \tag{4.5}$$

$$\frac{V_{LSB}^2}{12} < V_{n,thermal}^2 \tag{4.6}$$

$V_{n,thermal}$ has been optimized in the previous section to be in the range of 20 $\mu$V to 60 $\mu$V. Substitute it to the inequality 4.6, and maximum $V_{LSB}$ can be solved varying from 70 $\mu$V to 210 $\mu$V. The full scale of the ADC is chosen as 0.9 V. Divide 0.9 by $V_{LSB}$ and take base-2 logarithm of the result. The resolution can be solved to vary from 12.07-bit to 13.65-bit. However, because decimal places can not exist in ADC resolution and a safe margin should be reserved, the ADC resolution is chosen to be 14-bit.

The capacitor mismatch is at least 0.1 % in this technology, a purely linear 14 bits charge-redistributed SAR ADC is quite tricky according to the model created by [32]. Advanced techniques, such as trimming, noise-shaping, hybrid with Sigma Delta Modulator (zoom-in), can increase resolution. However, the majority of the signal is DC with a small varying AC component, because of PI, and hence we do not need the full 14 bits to be linear. Due to the primary location for the deployment of this sensor is the finger tip and wrist of healthy people, whose typical PI is around 1 % - 3 %. Therefore $V_{pp}$ of the AC signal when operating in FWC is 12 mV. This means 6.23-bit linearity is required, while decimal is not allowed and again 1-bit margin requires. Therefore, good linearity for 8 bits is required and possible in this technology, meaning the mentioned enhancement techniques are not necessary. In this project, a classic configuration, series-split array (6-bit MSB+8-bit LSB) can help differentiate the AC signal and hence maintain good linearity on the LSB side. More details will be elaborated in Section 5.3.1.

### 4.2.7. SOURCE FOLLOWER DRIVING CAPABILITY

Theoretically, the source follower and the amplifier should settle equally quickly in phase-1. Because the effective load of the source follower is $C_{in}$, which is twice the effective load of the amplifier, the source follower must have a double of $g_{m,A}$. Based on the conclusion in Section 4.2.5 that $g_{mA}$ should stays 7 $\mu$S to 72 $\mu$S, $g_{mSF}$ can be concluded to be 15 $\mu$S to 150 $\mu$S, where small up-rounding is made to ensure that the source follower settles before the amplifier.

## 4.3. PIXEL ARRANGEMENT

As mentioned, nominal 5000 pixels are required to handle the worst-case measurement condition when PI is only 0.2%. However, only half of them are practically required to handle most measurement scenarios and the reduced $C_{FD}$ helps the noise-power tradeoff. This is because when being referred to the charge domain at the input of

SF(node FD in Figure 3.2), the fixed amount of read-out voltage noise must be multiplied by $C_{FD}$. Moreover, Figure 4.7 indicates backup pixels are required to handle even worse scenarios when the readout noise rms value is too high. Therefore, in this project, 2500×4 pixels will be placed on the chip.

Take a closer look at a 2500-pixel cluster. In state-of-the-art CMOS imaging system, to minimize the $C_{FD}$ caused by routing and coupling that can choke noise performance, the source follower is placed right adjacent to the pixel's FD node. Moreover, the imaging system demands accurate capture and readout of each pixel's voltage. However, in our application, only the relative change in charges collected in $C_{FD}$ is required to be captured. The individual pixel's $V_{FD}$ is not our concern, but the pixel cluster's global relative change in a short time window (e.g., a few seconds to extract heart rate) matters.



To justify the division of pixels or rather the number of macro-pixels or source followers, first a practical perspective is considered. As presented in the previous subsection, $g_{m,SF}$ shall remain in the range of 15 $\mu$S to 150 $\mu$S. However, if 2500 source followers are deployed per cluster, the drain current per SF is 0.4 – 4 nA, which is apparently not possible in this technology to obtain such a low biasing current.

Then from the system SNR perspective, in this project, enough SNR design margin has been reserved as extensively discussed and hence routing capacitance may not be a big concern as long as it is reasonably low. The interference resulting from coupling capacitance in routing does play a first-order role as only global change is of interest. A way to prevent paying more power in SF to compensate for its noise contribution is to connect pixels in an array (a macro-pixel), which therefore can average the noise at the output of the source follower. A decent division can be 50×50, that is, 50 macro-pixels, and each macro-pixel has 50 pixels and a source follower. In this way, the current per SF is 20 – 200 nA. Again, 20 nA is not possible, and hence $g_{mSF}$ is chosen to be 150 $\mu$S (an equivalent of $I_D$ = 200 nA for each SF). Moreover, additional noise averaging is enabled at the output of the source follower, where thermal noise of SF is averaged for 50x.

## 4.4. SUMMARY OF DESIGN PARAMETERS

Table 4.1 summarises the design parameters that are important in the transistor design, based on the previous justification.

Table 4.1: Design parameters

| Design parameter | Requirement (unit) |
|---|---|
| Technology | TSMC180nm |
| Supply | 1.8($V$) for Readout<br>3.3($V$) for Pixel+SF |
| $g_{m,A}$ | 70 ($\mu S$) |
| $g_{m,SF}$ | 150 ($\mu S$) |
| $C_{in}$,$C_{fb}$ | 60 ($pF$) |
| Resolution | 14 (bit) |
| Number of Pixels | 2500×4 |

# 5

# CIRCUIT DESIGN

This chapter presents the circuit implementation of the main building blocks, including the main amplifier, the dynamic comparator, the capacitor DAC, the SAR logic unit and the source followers. Key simulation results are also presented.

## 5.1. MAIN AMPLIFIER

This section presents the design of the main amplifier, including an auxiliary pair used for autozeroing. The design choices and the simulation results are also shown.

The primary requirement for the amplifier is low power consumption, because its static current is constantly required over the observation window (phase-1 and phase-2) and is the main power consumer in the readout chain. The gain of the amplifier is moderate, and 84 dB should be enough to make sure it settles within the LSB of the ADC. A slight lose of DC gain translates to a gain error and is not a big issue. The output swing requirement is moderate – high, around 1 V. The speed requirement is moderate – high and the bandwidth is around 1 MHz, derived from the reciprocal of the settling constant ($\tau_{8.6}$) mentioned in Section 4.2.5. Therefore, according to *Table 9.1 Comparison of performance of various op-amp topologies* in [28], the folded cascode is chosen.



Figure 5.1 shows the schematic of the main amplifier. It is a single-ended folded-cascode amplifier with an auxiliary pair illustrated in the middle (MAZ1 and MAZ2). As said, the auxiliary pair serves for the autozeroing, which can suppress offset and flicker noise. However, differential charge injection error voltage introduced by turning off two possibly-mismatched switches SAZ can not be corrected by AZ and will appear as equivalent input-referred offset voltage. In order to reduce its effect, the transconductance $g_m$ of the auxiliary pair is chosen to be 1/10 as that of the main input pair.

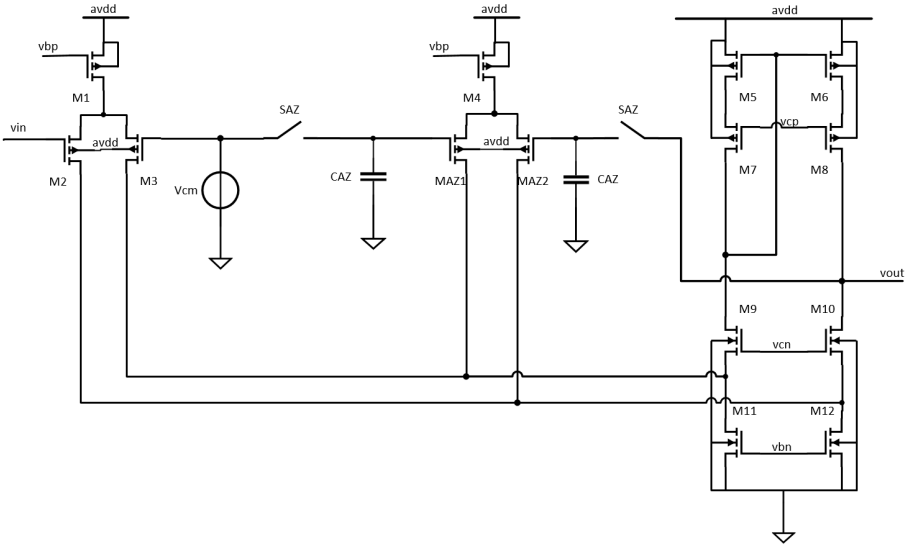


Figure 5.1: Main amplifier, folded cascode with an auxiliary pair resident in the middle

Regarding the sizing of each transistor and transistor pair, the biasing condition should be justified, which is as follows:

(1) Current source - M1, M4, M5, M6, M11 and M12: These transistors serve as current sources that mirror current from the biasing network. The primary reason is that they need a large $V_{dsat}$ to have high independence of output current change against the small variation of $V_{GS}$. Moreover, M5, M6, M11 and M12 only contribute to $r_{out}$ in the voltage gain expression in [28], which means a longer device helps. Therefore, they are biased in strong inversion, with a gmoverid of around 7 S·A$^{-1}$.

(2) Input pair - M2, M3, MAZ1 and MAZ2: These transistors are input pairs, while M2 and M3 are the main input pair. This is not a high speed application, hence high $V_{d,sat}$ is not necessary [33]. Considering $g_m$ efficiency, they are biased in weak inversion, which have a low $V_{d,sat}$ and a high gmoverid, 24 S·A$^{-1}$.

(3) Cascode pair - M7, M8, M9 and M10: They are cascodes to boost the gain. Their $g_m$ and $r_{out}$ are both important in the voltage gain. They also have a direct influence on the headroom or footroom of the output swing. Therefore, for a decent compromise among design requirements, they are biased in moderate inversion. The gmoverid is around 15 S·A$^{-1}$.

Since the amplifier's flicker noise needs to be stored and cancelled by the autozeroing mechanism, the corner frequency of the flicker noise should be lower than the switching

frequency. In this case, the effective switching frequency is the reciprocal of the time from the start of the AZ phase to the start of the SAR conversion. The charge transfer needs 5 $\mu$s as stated before, and a generous assumption can be made that the time required for the AZ pair to store the flicker noise is 200 $\mu$s, taking into account of the extra margin reserved for settling under different process corners. This 200 $\mu$ s translates into an effective switching frequency of 5 kHz. The op-amp's area is not a big concern since the area-hungry component on this die is the pixel sensor. Therefore, to ensure that the flicker corner is lower than that, the input pairs and tail current source pairs need to have a properly large size, which is the most common and easy approach.

Therefore, the sizing and the current that goes through each transistor are:

Table 5.1: Sizing of the main amplifier

| Transistor number | Size ($\mu$m × M / $\mu$m) | Current ($\mu$A) |
|---|---|---|
| M1 | 1×40/10 | 8 |
| M2,M3 | 3×40/1 | 4, 4 |
| M4 | 1×4/10 | 0.8 |
| MAZ1, MAZ2 | 3×4/1 | 0.4, 0.4 |
| M5, M6 | 1×20/10 | 4, 4 |
| M7, M8 | 0.5×20/1 | 4, 4 |
| M9, M10 | 0.22×20/1 | 8.4, 8.4 |
| M11, M12 | 0.22×84/10 | 8.4, 8.4 |

Figure 5.2 is the bode plot of the op-amp in open loop, with a 30 pF capacitance to model its effective output load. It is a stable op-amp, as the second pole is far away enough from the 3dB bandwidth at 700 kHz.

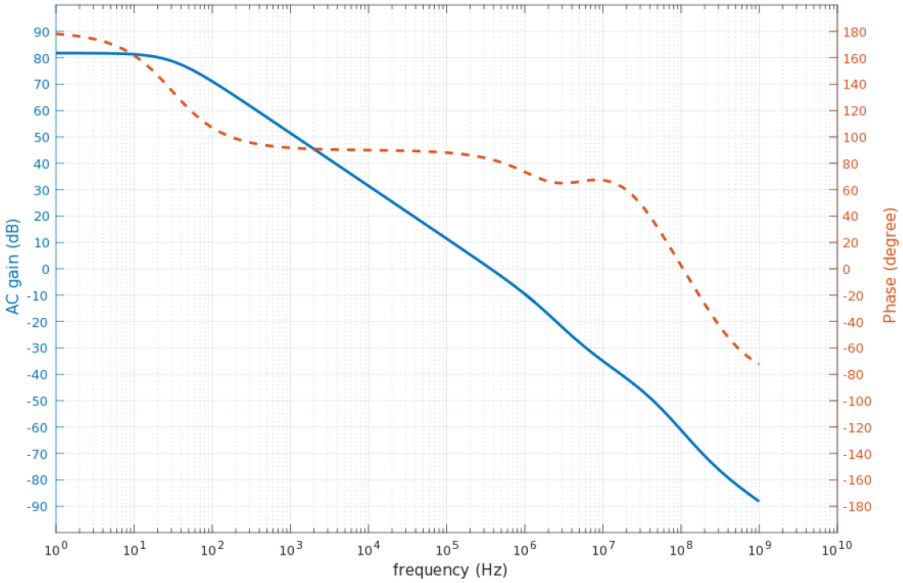


Figure 5.2: Bode plot of the op-amp in open loop, with an effective load capacitance of 35 pF

Figure 5.3 shows the input-referred noise amplitude spectral density. It can be interpolated that the flicker noise corner is around 3 kHz, by finding the intersection of the floor noise and the flicker noise. 3 kHz corner frequency is sufficient for AZ to hold and cancel the flicker noise within the switching period as discussed before.

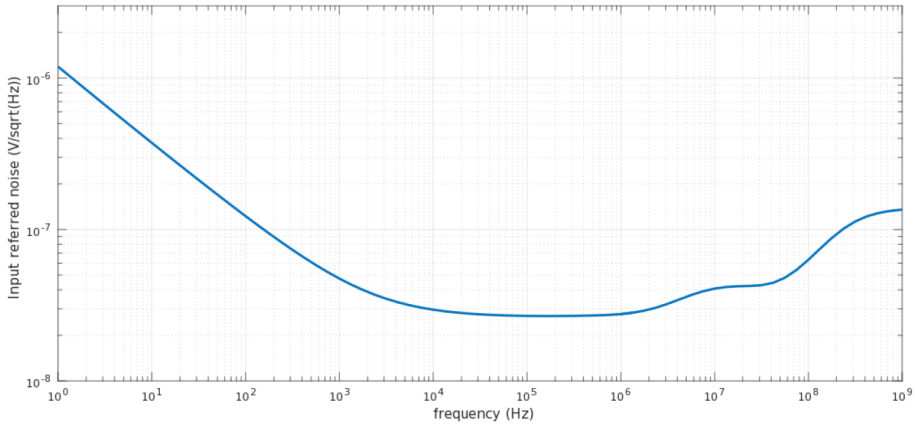


Figure 5.3: Input referred AC noise of the op-amp

A constant finite DC gain leads to settling error voltage that translates to a constant gain error. However, during phase-1, the output node swings to different output voltages. The amplifier's open-loop DC gain tends to change with that swing. The variation of open-loop DC gain leads to non-linearity of the signal that samples in $C_{fb}$, which eventually leads to non-linearity of of the system.

An open-loop testbench was created to investigate its effect by injecting a very small AC magnitude into the input (vin) on top of its common mode. Then the DC gain and DC operating point of the output node (vout) are recorded. Figure 5.4 shows the plot of DC gains versus output DC operating points. The common mode is 0.45 V and the desired ADC full range is 0.9 V. Therefore, the annotated points indicate the desired output swing range (0.45 V – 1.35 V).

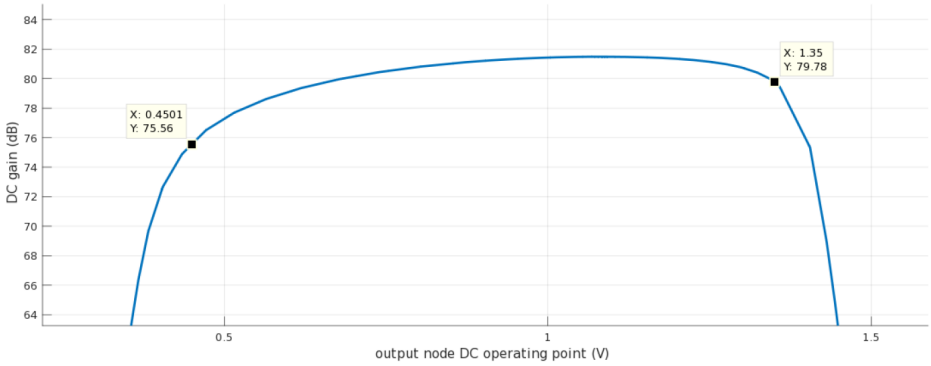


Figure 5.4: DC gain versus output swing

An interesting observation is that the decrease of DC gain is not balanced, due to the not fully balanced headroom and footroom of the amplifier. However, this is not an issue because our AC signal is also changing. Given a fixed PI, when the DC signal is low, the AC is also low. Only good linearity over an AC signal range is required. A numerical analysis of this large signal behaviour is as follows:

(1) Assume PI = 10%, which means the worst case when AC amplitude is large.

(2) Start with a $\Delta V_{SF}$ = 1 mV. 450 mV is the common mode voltage. In other words, node vin is 451 mV. The AC is now 450.95 mV – 451.05 mV, which is also the swing of vout.

(3) Look up in Figure 5.4 to find the DC gain when the output node swings to $V_1$ 450.95 mV and $V_2$ 451.05 mV, which is 75.54 dB and 75.59 dB respectively.

(4) The typical transfer function of a finite-gain inverting amplifier is as below:

$$\frac{\Delta V_{out}}{\Delta V_{SF}} = -Gain \times \frac{A\beta}{(1+A\beta)}, \tag{5.1}$$

where A is the finite gain, $\beta$ is the feedback factor that equals to $\frac{1}{1+1/gain}$ and in this case $\beta$ is 0.5.

(5) The settling error voltage can be found by solving:

$$\epsilon_V = |\Delta V_{SF}| - |\Delta V_{out}| = \frac{1/\beta}{A+1/\beta} \times vin = \frac{2}{2+A} \times vin \tag{5.2}$$

Substitute two combinations of vin and DC gain into it. $\epsilon_{V1}$ is 0.315 $\mu$V and $\epsilon_{V2}$ is 0.348 $\mu$V.

(6) Find the absolute difference between the settling error voltages. In this case, it is 33 nV.

(7) Repeat steps (2) - (6) with different input $\Delta V_{SF}$. Plot the difference in the settling error voltages versus the input DC values.



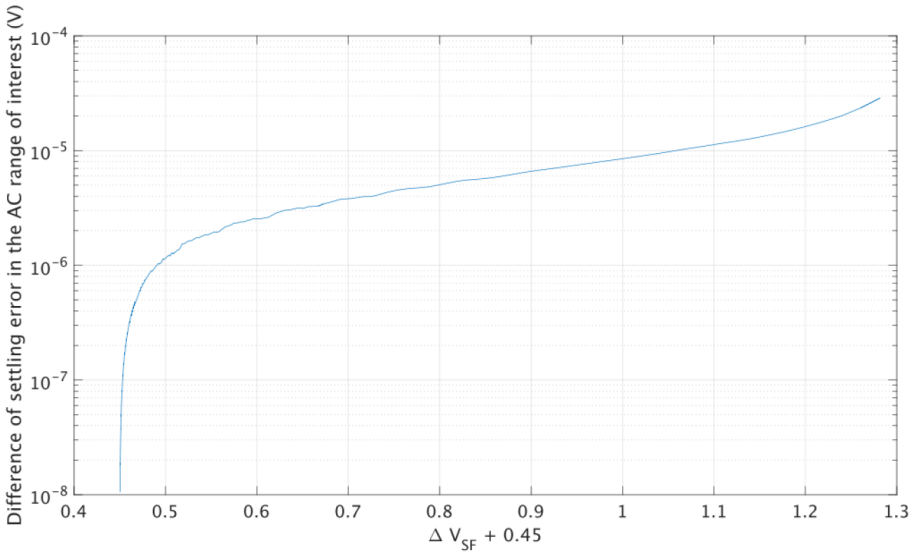


Figure 5.5: Difference of settling error voltage in the AC range of interest, in 10% PI

Figure 5.5 shows that the maximum settling error voltage is 28 $\mu$V when the DC input voltage is large. It is smaller than half of the LSB step of ADC and hence is not an issue. The message here is that even though the signal transfer phase (phase-1) experiences a non-linear gain error, the difference of settling error voltages in the AC signal of interest range is small enough to avoid distortion of the signal that samples in $C_{fb}$.

## 5.2. COMPARATOR

In this project, a double-tail latch-type voltage sense amplifier is deployed [34], as per Figure 5.6. In order to make a fully balanced comparator that works properly under different process corners and temperatures, matching its differential output impedance is necessary. Therefore, each of its differential output nodes is followed by an identical buffer that available from TSMC's standard digital cell library, which is not illustrated in the figure.

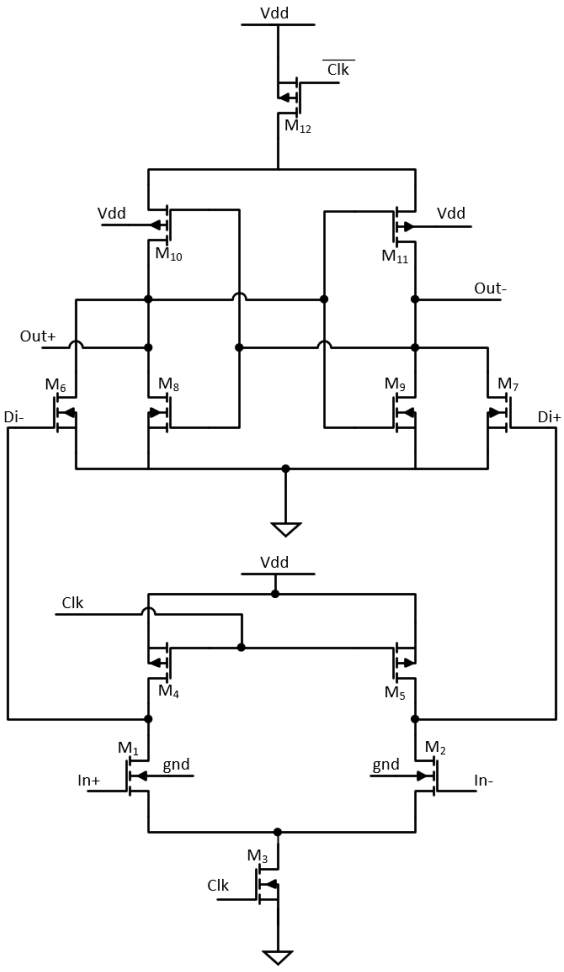


Figure 5.6: Dynamic comparator: Double-tail latch-type voltage sense amplifier [34]

The basic signal behaviour is as follows:

(1) Precharge (reset) phase: When Clk = 0 V, M4 and M5 turn on, nodes Di+ and Di- are precharged to Vdd. This results in M6 and M7 turning on and the output nodes out+ and out- being reset to 0.

(2) Evaluation phase: When Clk = Vdd, tail transistors M3 and M12 turns on, providing current. M3 and M4 are now off and have a negligible impact on this phase. Di nodes start to drop, the rate of which depends on the input. The moment one of the Di nodes fails to clamp its respective output node to ground, the cross-coupled inverters (M8–M11) begin to reproduce the input voltage difference and latch the output nodes to rail-to-rail, Vdd or ground.

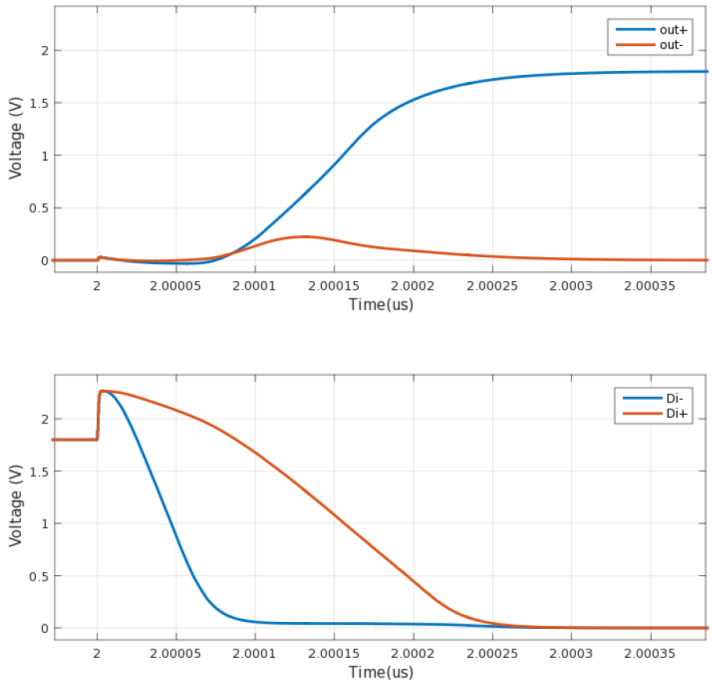


Figure 5.7: Comparator signal behaviour when In+ > In-, clock rising edge at 2 $\mu s$

Compared to the conventional latched type comparator in [35], this architecture operates faster and has lower offset and kickback noise, due to the additional shielding between input and output provided by M6 and M7. Figure 5.7 shows the signal behaviour of four nodes of interest, when the clock signal changes from low to high at 2 $\mu$s. The total time used for the output nodes to settle is less than 300 $ps$, in other words the delay is 300 ps. In this project, 300 ps delay is not a concern, as the clock period during the SAR search phase is 8 $\mu$s. Moreover, the design specifications regarding offset and noise of the comparator are also relaxed, because they are effectively suppressed by the high-gain pre-amplifier.

## 5.3. CAPACITOR-DAC (CDAC)

### 5.3.1. CDAC ARRAY

The system requires a 14-bit CDAC and an equivalent feedback capacitance of 60 pF. The CDAC has a crucial responsibility in the SAR conversion phase, meaning its parasitic capacitances and matching are important. There are two main-stream options to fabricate the capacitors, Metal-insulator-metal (MIM) and Metal-Oxide-Metal (MOM). In this process (TSMC180nm), the mismatch ratio is close for both types. However, MIM capacitors have significantly lower parasitic capacitances to the substrate, compared to MOM capacitors with the same nominal capacitance value. To be more specific, MIM capacitors have 10x less parasitic capacitance on the bottom plate than MOM, and also MIM capacitors do not have parasitic capacitance on their top plate whereas MOM capcitors have, based on the Parasitic Extraction result by Calibre/2014. Therefore, MIM capacitors were deployed for this project.



In this process, the minimum value for an MIM capacitor is 35 fF. If the CDAC is a fully binary array, its total capacitance must be at least 573 pF ($35f \times 2^{14}$). This is doable, but is at the cost of 9x more driving capability required for the op-amp in the charge transfer phase, compared with the nominal 60 pF specified before. A higher $g_m$ does not result in an ultimate power-efficient solution, as discussed in Section 4.2.5. Things can be even worse, because a higher unit capacitor is necessary to reduce its mismatch effect. As mentioned, the signal of interest occupies only a small proportion of the overall $V_{pp}$ in this particular application. A 6 bit MSB + 8 bit LSB series-split configuration motivated in Section 4.2.6 has been implemented as in Figure 5.8.

The sizing of the bridging capacitor($C_b$), LSB side capacitors (unit capacitor $C_L$) and MSB side capacitors (unit capacitor $C_M$) are calculated motivated as follows:

(1) If $C_M$ switches, the voltage change $\Delta V_1$ seen at the input of the amplifier is:

$$\Delta V_1 = \frac{C_M}{C_M + \frac{C_b \times 255 C_L}{C_b + 255 C_L}} \tag{5.3}$$

(2) If $C_L$ switches, the voltage change $\Delta V_2$ seen at the input of the amplifier is:

$$\Delta V_2 = \frac{C_b}{C_b + 63 C_M} \frac{C_L}{255 C_L + \frac{C_b \times 63 C_M}{C_b + 63 C_M}} \tag{5.4}$$

(3) To achieve a simple layout that minimises routing capacitance and a balanced layout that minimises device-to-device mismatch, $C_L$ is chosen the same as $C_M$.

(4) We would like $\Delta V_2$ to be equal to $\frac{V_1}{2^8}$. Substitute it with Equation 5.3 and 5.4, and $C_b$ can be solved to be equal to $C_L$ (and $C_M$).

(5) The feedback capacitance is 60 pF, hence:

$$63C_M + \frac{C_b \times 255C_L}{C_b + 255C_L} = 60pF \tag{5.5}$$

$C_M = C_b = C_L$ can be solved to be 937.557 fF.

Therefore, a 6 bit MSB + 8 bit LSB allocation in this case leads to two main advantages:

1) The equivalent capacitance is now dominated by the MSB side, and hence the unit capacitance is 937.557 fF. The total nominal capacitance is $C_u \times (2^6 - 1 + 2^8 - 1 + 1)$ = 299 pF, half of the value of deploying a pure binary array (537 pF). Moreover, the capacitor array with a larger unit capacitor has a better matching.

2) A 6 bit MSB + 8 bit LSB allocation in this case leads to the MSB side remaining unchanged in adjacent samples, since the DC component is expected to be captured fully or mainly in the MSB side. This large DC component originates from body tissue and does not vary significantly or suddenly during a certain monitoring period. Therefore, the linearity requirement lies on the LSB side.



Though this configuration relaxes the overall linearity requirement, it comes with two downsides. First, the mid-point INL transition is typically the largest (equals to the maximum INL error). Second, the array partitioning leads to an irregularly centroid or partially uniform layout, which can lead to mismatch effect that is hard to predict analytically [32]. Nevertheless, the first defect can be easily tackled by burning more or less LED power to bring the signal out of the dangerous zone and the second can be mitigated by careful layout and dummy capacitor enclosure.

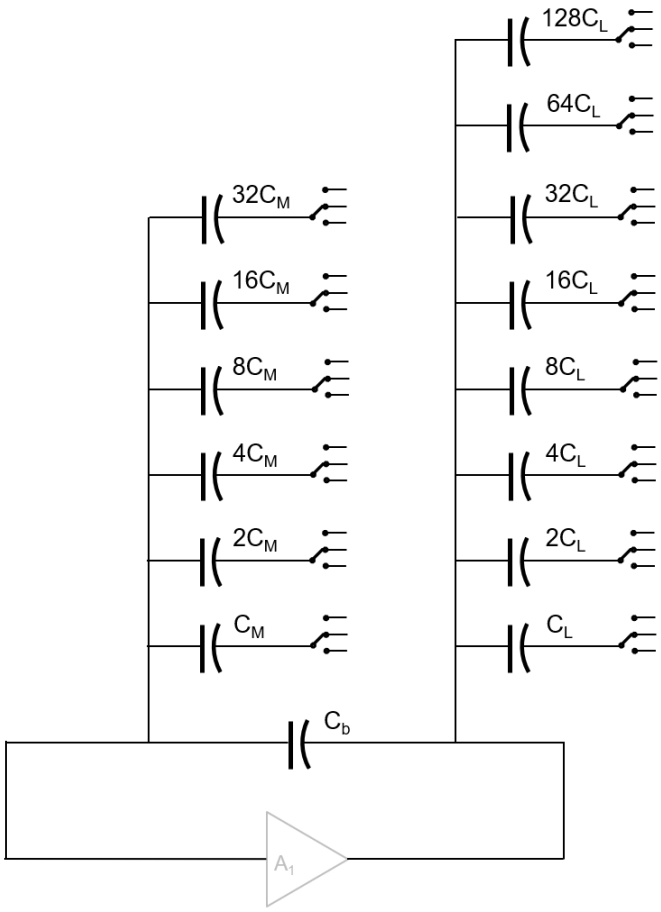


Figure 5.8: CDAC array

### 5.3.2. SINGLE POLE THREE THROW SWITCH (SP3T)

Figure 5.9 illustrates the SP3T switch used in the CDAC. It has three pairs of complementary switches. The basic control logic is as follows: In phase-1 (charge transfer), the bottom pair turns on while the other two switch off; In phase-2 (SAR), the bottom pair turns off and the other two switch on or off depending on the output of SAR control unit (only one turns on). Therefore, it needs two control signals, one coming from off-chip signal to force it to connect to the output of the amplifier, and the other one coming from SAR logic. Dedicated digital gate driver circuitry is employed for each SP3T.

The DAC also needs to settle quickly in every approximation window, meaning that its RC constant ($R_{on}C$) needs to be kept reasonable. Therefore, the size of the switch scales up as the capacitance of the capacitor in that particular branch increments binarily, by

increasing the number of parallel devices. To avoid crazy number of parallel transistor per switch, it is not necessary to increase the M-factor exactly in the binary pattern as per the capacitance. The decision here made for the top two pairs of transistors is: $M_{C\&2C} = 1, M_{4C\&8C} = 2, M_{16C\&32C} = 4, M_{64C\&128C} = 8$. The bottom pair remains in its small unit size to minimise charge injection and clock feed-through in the first phase.

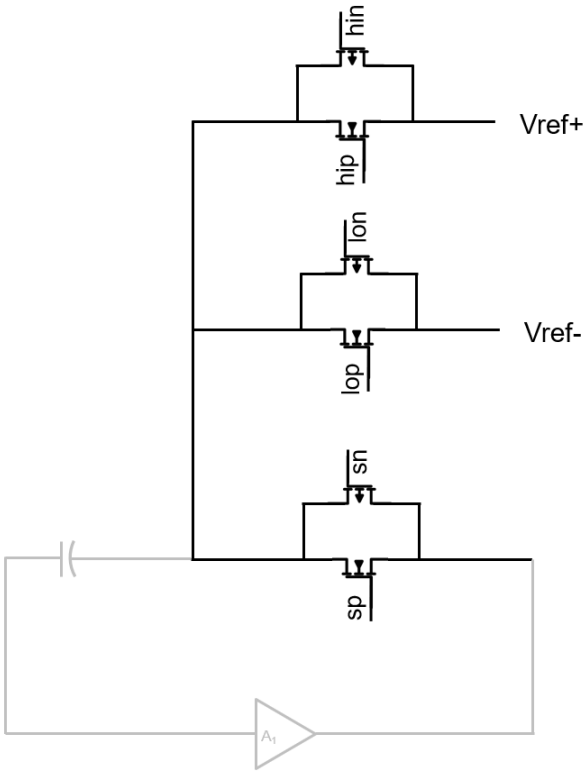


Figure 5.9: A single-pole-three-throw switch

## 5.4. SAR LOGIC

There are two typical implementations of the SAR control logic, synchronous and asynchronous. The synchronous logic is conventional, which requires a high-frequency clock $f_{clock,SAR} > N \times f_s$. However, due to the fact that power consumption in CMOS increases linearly with respect to frequency, asynchronous control logic is deployed in SAR ADCs that have high sampling rate. As stated in [36], asynchronous control logic circuit spreads its interference power widely over the bandwidth, while the synchronous one only shows 97% of interference power at the multiple of the clock frequency. Therefore, due to the low sampling rate and less concern about the high frequency interference, synchronous control logic is deployed.

Figure 5.10 shows the synchronous control logic used in this project, invented by [37]. The top row is a sequencer that gets reset first and shifts "1" from left to right. The bottom row, which serves as a code register, receives the output from the sequencer and is set one by one. The output of each D-FF in the bottom row is used as a clock for conditional reset of the previous D-FF. The input D connects to the comparator output. The clock frequency here is 125 kHz and the current consumption is 0.5 $\mu A$ during SAR approximation.

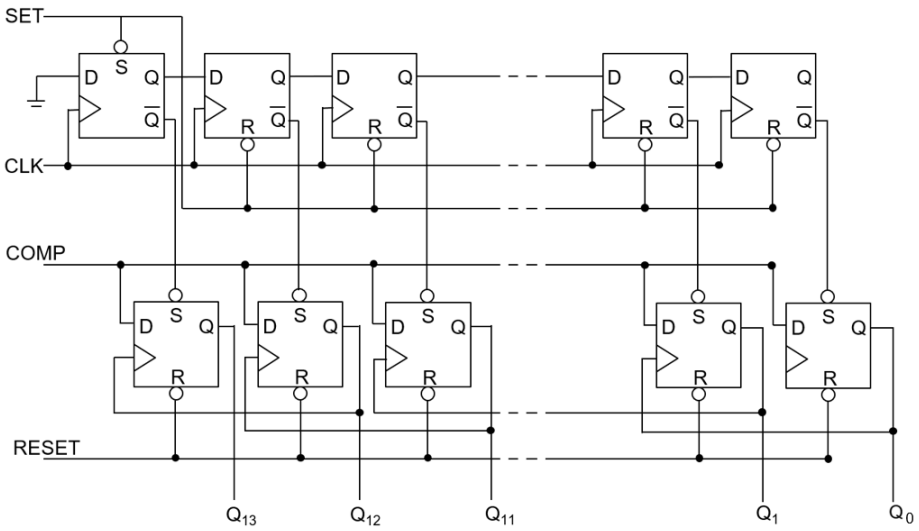


Figure 5.10: SAR control logic

## 5.5. SENSOR FRONT-ENDS

As mentioned in Section 4.3, four 2500-pixel clusters are required on the chip and each cluster has 50 macro-pixels. Each macro-pixel has 50 pixels and these 50 pixels share a source follower. This section presents the way in which sensor front-ends are constructed together with source followers.

### 5.5.1. SOURCE FOLLOWER

In Section 4.3, a 50 × 50 arrangement is proposed. It is based on two reasons. Firstly, a reasonable noise averaging can be achieved at the output of the source follower. Secondly, the drain current for each source follower is practically possible (not too low).

Basically, each cluster consists of 50 macro-pixels (MP) and each MP consists of 50 pixels. Each MP is followed by a source follower, meaning that the current in each source follower is 200 nA. Now, $C_{in}$ also needs to be divided into small segments that can be connected to each MP. We mentioned that $C_{in}$ has to be effective 60 pF and hence each MP has a load of $C_{in,MP}$ = 1.2 pF.



Figure 5.11 shows the schematic of the source follower. It is supplied with 3.3 V in accordance with the supply of the pixel itself. The main input is NMOS with a deep N well that enables its bulk and source to be connected. In this way, its body effect is minimised, and the best linearity is achieved. Meanwhile, it is biased in moderate inversion for better linearity.

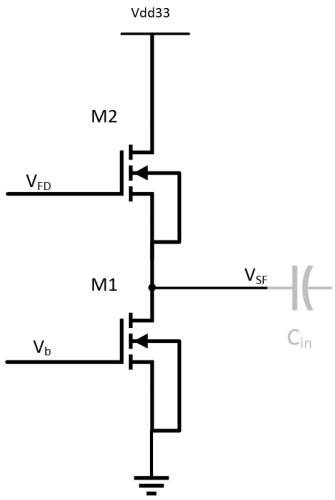


Figure 5.11: A source follower

Table 5.2 shows the design choice for the source follower:

Table 5.2: Source follower design

| Item | Value | Unit |
|---|---|---|
| Size of $M_1$ (W×M/L) | 0.25×2/8 | $\mu$m × M / $\mu$m |
| Size of $M_2$ (W×M/L) | 0.5×4/1 | $\mu$m × M / $\mu$m |
| $V_b$ | 0.88 | V |

### 5.5.2. PIXEL CLUSTER

As mentioned, each cluster has 50 MPs and each MP has 50 pixels nominally. In real design, the source follower resides in the middle of the MP for a balanced routing parasitic capacitance management. Each source follower occupies an area of 8 $\mu$m × 25 $\mu$m in layout and replaces three pixels in the middle. Therefore, every MP has 46 pixels, and 49 MPs make up a pixel cluster.

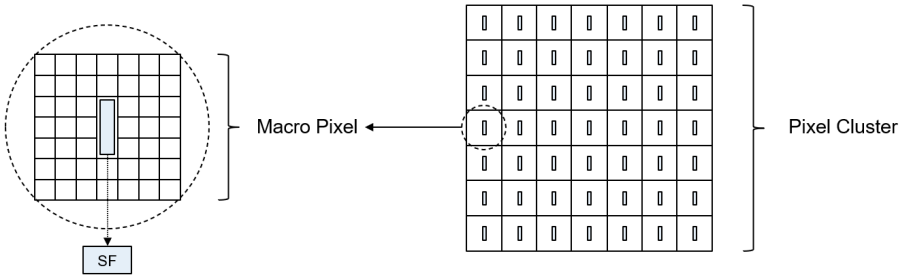


Figure 5.12: A macro pixel and a pixel cluster (blue square denotes a source follower)

# 6

# LAYOUT AND POST-LAYOUT SIMULATION RESULT

This chapter presents the layout design of the pixel array and the readout circuit with design considerations and the readout post-layout simulation results. As the chip has been submitted for fabrication but has not yet returned at the time of writing of this thesis, a detection and counting process was simulated in MATLAB, taking into account of non-idealities, which will be presented. A chart of energy dissipation per sample of this work concludes this chapter.

## 6.1. LAYOUT DESIGN

### 6.1.1. PIXEL ARRAY

As said, each pixel array has 46 individual pixels. Their output nodes need to be connected in parallel. The primary objective of the layout is to minimize any capacitance to ground seen at the floating diffusion node that is the main noise choker, which includes routing parasitic capacitance and coupling capacitance to adjacent grounded metal. Certainly, the routing parasitic capacitance is basically the coupling capacitance to the p-type substrate.

In order to align with the company's intellectual property embargo, the actual pixel layout will not be presented. However, to justify the metal routing decisions of the layout, Figure 3.1 was redrawn and annotated:

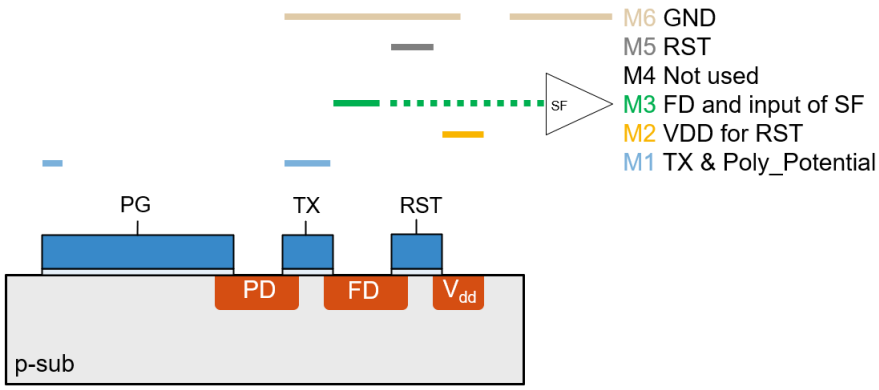


Figure 6.1: Cross section of individual photogate imager's metal routing, light yellow (M6), grey (M5), green (M3), gold (M2), blue (M1)

In order to block out light impinging onto the light sensitive areas other than the desired polysilicon, M6 is grounded and serves as a shielding on top of those areas (FD and SF). For the same area, M1 has the largest parasitic capacitance, since it is closest to substrate. M5 gives the lowest coupling to the substrate though only a shallow decrease in parasitic capacitance is observed from M2 to M5. However, M5 is too close to the top grounded shielding M6 and the coupling to it can be significant and take over the dominance. In

order to make a good compromise to minimise the FD node's capacitance to ground, FD must be routed using middle layers. In this case, M3 is deployed to connect pixels' FD inside an array.

The moment TX turns on, TX couples the clock transition to the FD node, by the TX – FD overlapping capacitance, leading to the clock feedthrough. Therefore, it is also important to minimise the TX-FD coupling capacitance. TX is connected by M1 that is far away enough from M3 used for FD.

The PG is a light-sensitive area, so it needs to be connected for potential and a minimum width of M1 is used. $V_{dd}$ and RST are less likely to deteriorate the system performance and hence they are connected using the spare layers that has minimum interference to adjacent nodes.

The total $C_{FD}$ for a pixel array is 91 fF. According to Parasitic Extraction (PEX), in a pixel array, the parasitics to ground is 26.7 fF in total and the coupling capacitance TX-FD is 16 fF. Therefore, the layout-related parasitic and coupling capacitance only degrades SNR by 1.5 dB roughly, which can be easily compensated by injecting 1.2 times the incident photons according to Figure 4.6, which is equivalent of burning 1.2 times the LED power.

### 6.1.2. READOUT

Figure 6.2 shows the layout of the readout circuit. The amplifier resides in the top right of the figure. SAR logic and SP3Ts stays top left. The comparator is in top middle. The rest of the area is occupied by the feedback CDAC.

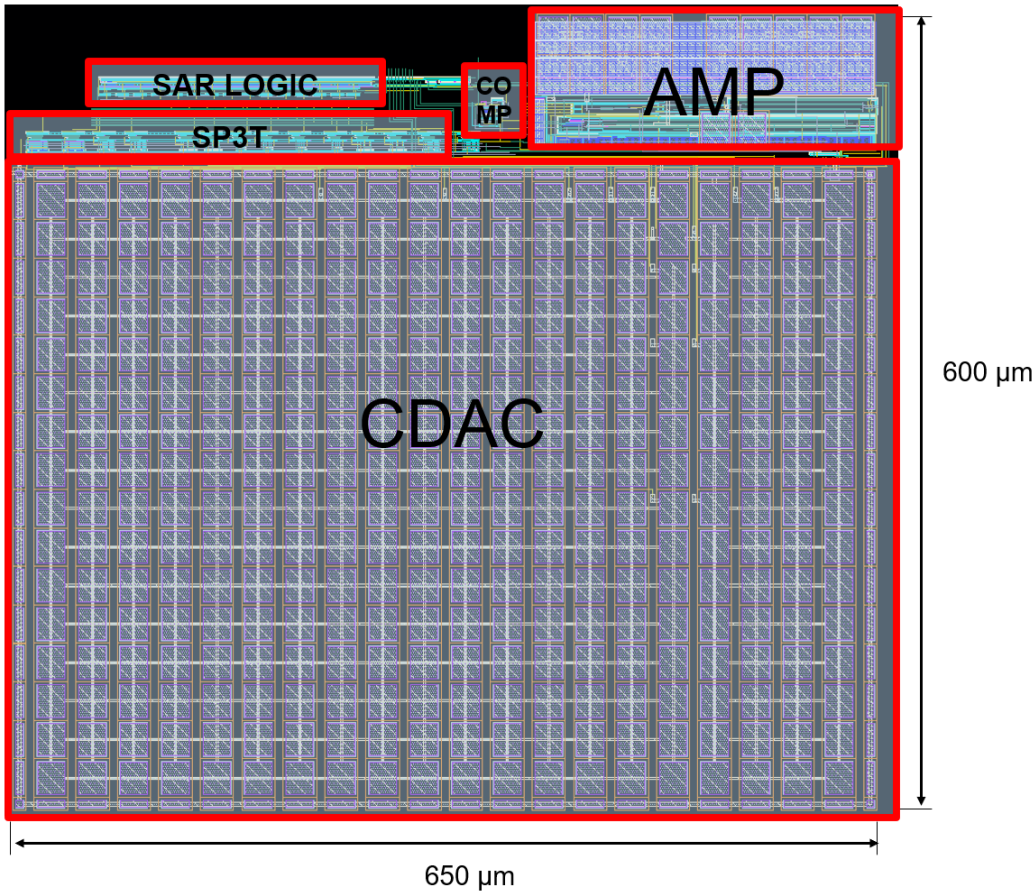


Figure 6.2: Readout layout

### 6.1.3. FULL CHIP

Figure 6.3 presents the layout of the full chip. Four clusters of pixel sensors reside at the top of the chip. The readout circuit is at the bottom right. The rest of the chip area is covered by decoupling capacitors. The filler of the padring is there, but it disappears from showing after zooming out, and hence the screenshot of the padring looks discontinued.

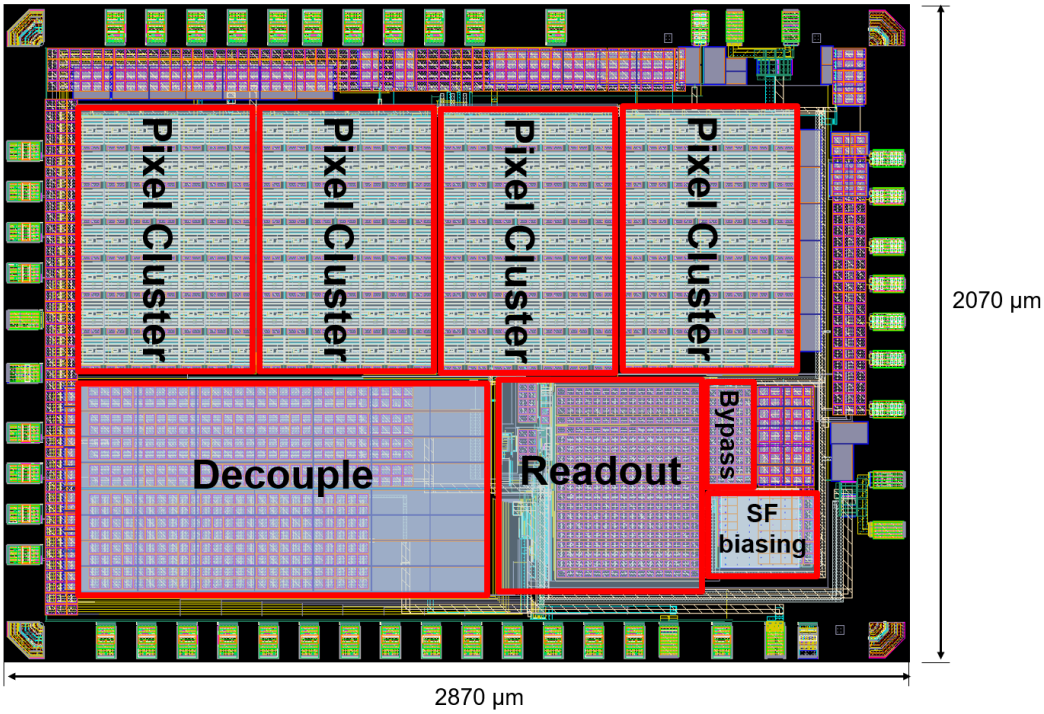


Figure 6.3: Full chip layout

## 6.2. POST LAYOUT SIMULATION

Unfortunately, it is not possible to simulate the pixel's performance in Cadence ADE. In this section, the readout circuit (phase-1 and phase-2) and the combination of source followers and the readout circuit are individually simulated and verified.

### 6.2.1. READOUT

Figure 6.4 shows a dummy structure on the chip that can fully bypass the pixel clusters including pixel, SF and $C_{in}$. A single-pole-two-throw switch and a large input capacitor (60 pF) $C_{in,by}$ can simply mimic $\Delta V_{SF}$ that samples on $C_{in}$. To verify the readout, especially the linearity of the ADC, it is wise to use the dedicated bypass structure with minimal interference.

The basic working mechanism is as follows: $V_{bypass\_1}$ is fixed at 0.9 V to mimic the reset level of the pixel. $V_{bypass\_2}$ is swept from 0 to 0.9 V, which is the nominal full range. Thus, the left plate of $C_{in\_by}$ sees a $\Delta V_{in}$ that is equivalent to $\Delta V_{SF}$ in the real system.



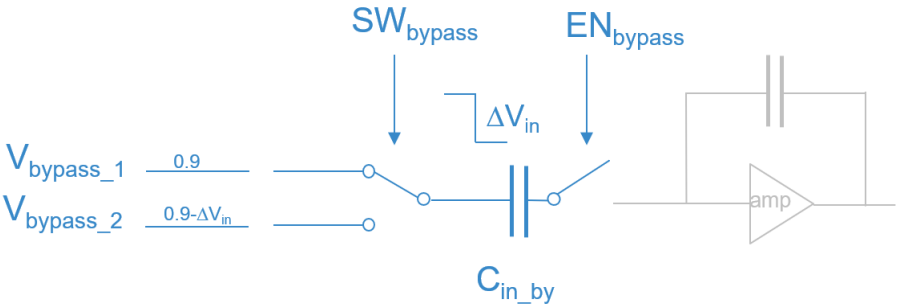


Figure 6.4: Bypass structure

Figure 6.5 below shows the INL of the system for a small input range. The x-axis is input $\Delta V_{in}$. And the y-axis is INL, expressed as $\frac{(Q_{13}\times 2^{13}+Q_{12}\times 2^{12}+...+Q_0\times 2^0)-\Delta V_{out}}{V_{LSB}}$. The result presents three segments, each of which spreads 14 mV. 14 mV is $\frac{900}{2^6}$, which indicates that the transition happens at every 14 mV when MSB changes. The 14 mV is where AC signal of interest typically stays. The nonlinear transition between every 14 mV segment is because of the parasitic capacitors that exist on both sides of the bridging capacitor. This parasitic capacitance comes from routing between the unit capacitors and it is quite difficult to mitigate. Additionally, the transitions do not happen exactly at the multiples of 14 mV, but at 28.5 mV, 43 mV and 57 mV approximately. This is because the real feedback gain is not exactly 1 due to imbalanced routing and coupling capacitance for $C_{in\_by}$ and $C_{fb}$, which leads to a small gain error. Within the 14 mV segment, it is linear to ±1 LSB, but with quantisation error that looks like spikes in the figure. It is because the simulation uses fine input steps of 1/3 of the $V_{LSB}$ and any analogue value ranging from

± 0.5 LSB may be interpreted to the closest digitized LSB value. However, from a system point of view, these types of non-linearities and the gain error are not a big concern. A more detailed demonstration will be presented in Section 6.2.2.

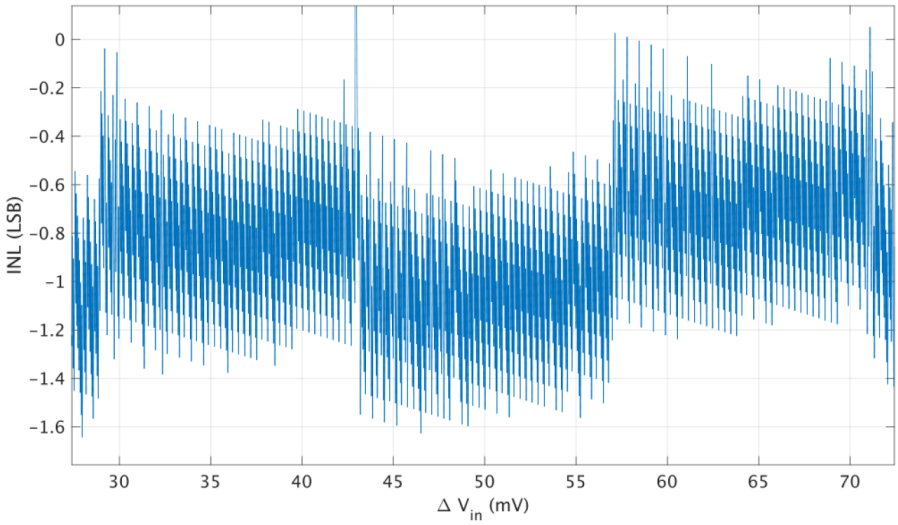


Figure 6.5: INL of the ADC using bypass structure

### 6.2.2. SOURCE FOLLOWER AND READOUT

This section presents results of the whole system excluding pixels that takes a PPG signal as input. The simulation procedure is as follows:

(1) A real PPG signal is again taken from the dataset collected by [30].

(2) Normalise the signal to the desired range that can represent a certain DC component and PI.

(3) For every sample, generate a piecewise linear (pwl) waveform that contains the corresponding PPG information. The waveform starts at a fixed reset voltage level and decreases to different levels that change with the PPG signal.

(4) Switch in only one cluster and use the generated pwl as the input of the source followers. In this way, the input of the source followers sees a voltage down step that mimics the PG pixel's operation.

(5) Decode the output of every sample in MATLAB using $D_{out} = Q_{13} \times 2^{13} + Q_{12} \times 2^{12} + ... + Q_0 \times 2^0$ and plot the stairstep graph of the digitised output using the "*stairs*" function in MATLAB.

(6) Normalise the waveforms in step (2) and (5) to the range of 0 – 1 V and plot them together.

(7) Count the digitised peaks and the peaks of the original waveform using the same "*findpeaks*" algorithm as in Section 4.2.3.

(8) Repeat steps (2) to (7) for different combinations of PI and DC.

Three combinations are verified. They are: Combination-1, DC = 390 mV and PI = 10% to mimic a typical FWC operation; Combination-2 DC = 450 mV and PI = 0.2 % to mimic a worst case when signal experiences a large mid-point INL transition while the AC signal is smallest; Combination-3, DC = 2 mV and PI = 10% to mimic the lowest detectable signal according to Figure 4.6.

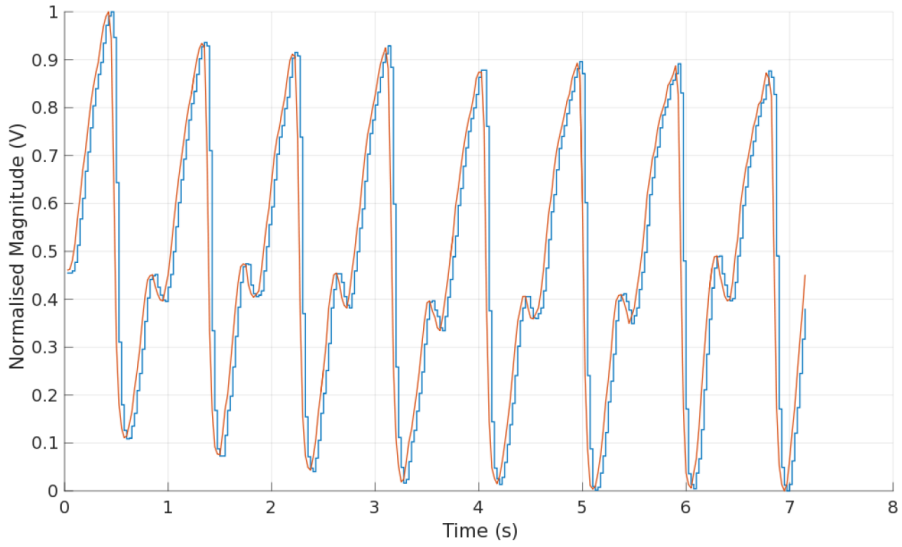


Figure 6.6: Normalised input (yellow) and output (blue) for combination-1



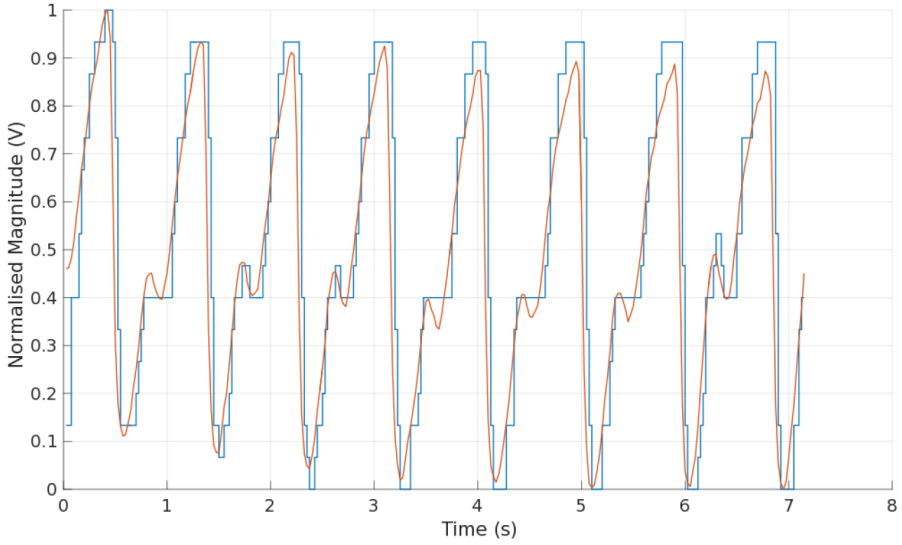


Figure 6.7: Normalised input (yellow) and output (blue) for combination-2

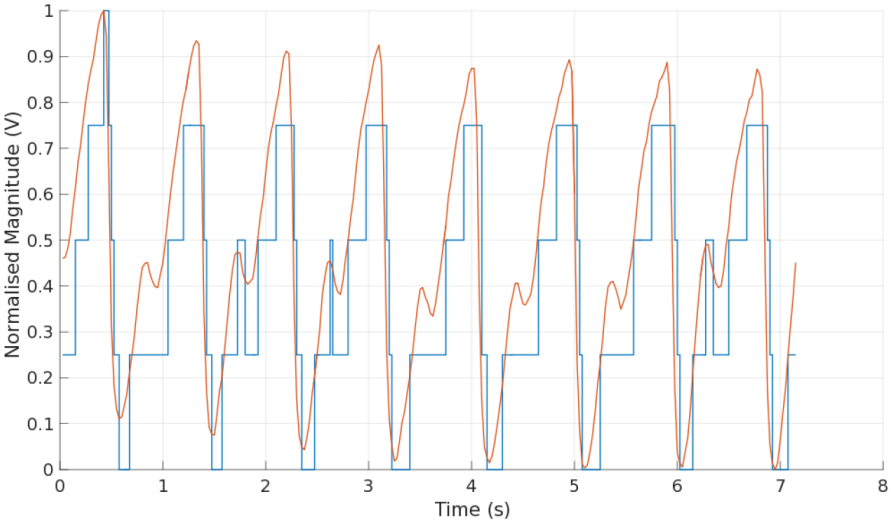


Figure 6.8: Normalised input (yellow) and output (blue) for combination-3



The same algorithm works for all three combinations, and there are no detection errors. For combination-1, the AC range is large enough (39 mV) and there are no large transitions in that range. Small quantisation errors that go up and down by $0.5V_{LSB}$ (55 $\mu$V), as Figure 6.5 shows, do not distort the waveform much. For combination-2, the AC range is 900 $\mu$V. Even if the mid transition is large, say $2V_{LSB}$ (110 $\mu$V), the waveform still keeps its shape for peak detection. It is slightly tricky for the third combination. The AC range is only 200 $\mu$V, which is equivalent of about 4 $V_{LSB}$ steps. The linearity of the ADC can distort the waveform. Luckily, in this case, since *"MinPeakProminence"* is 0.5 as per step (3) in Section 4.2.3, the dicrotic notches visually look like small peaks but are not counted in.

It is worth mentioning that the model above does not include noise, and hence the waveform can be further distorted. The simulation shows a transient noise of 80 $\mu$V at a bandwidth of 1 – 10 MHz. For combination-3, it is very likely to disrupt the peak finding algorithm. The easiest way to fix this is by burning more LED power, which effectively increases the AC range. The signal with a larger AC can tolerate more noise and more non-linearities of the ADC. However, it is difficult and is also not necessary now to predict how much additional power needs to be burnt on the LED. The measurement setup, measurement environment (ambient light), and even the human body under test can make a difference.

## 6.3. ENERGY DISTRIBUTION

In this project, the energy was mainly dissipated in the amplifier and the source followers. The comparator does not consume static current and the digital logic only consumes very little since it operates in low frequencies. The energy dissipation per sample is reported in Figure 6.9 below. This is obtained by starting up the biasing networks for 200 $\mu$s, powering up the main amplifier for 200 $\mu$s and powering up the source followers for 50 $\mu$s. The reported total energy for source follower is when only one cluster turns on. Since the SF's start-up and biasing currents are small, it can be approximated that turning more clusters on simultaneously increases the SF's total energy consumption linearly.

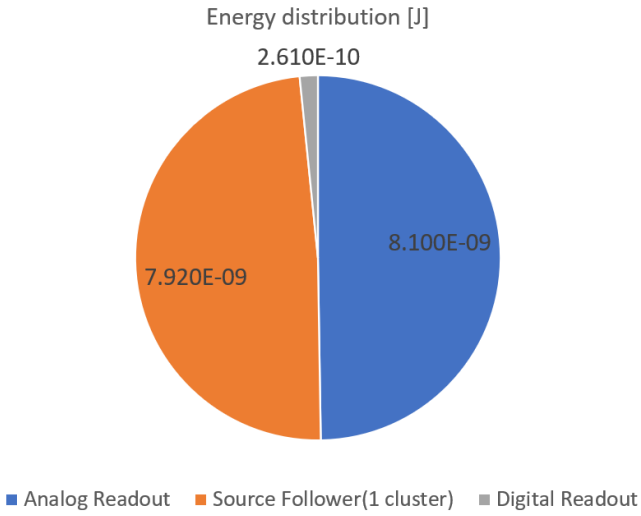


Figure 6.9: Pie chart of energy consumption per sample [J]

# 7

# CONCLUSION

## 7.1. THESIS CONTRIBUTION

In this thesis, the design of a monolithic power-efficient PPG readout system has been presented. This work deploys an energy-efficient SAR ADC instead of the sigma-delta modulator and incremental sigma-delta modulator used in prior work [8–10], which substantially reduces read-out power consumption. The system level simulation and modelling demonstrate the targeted detection accuracy is achieved, which though is subject to the change of measurement conditions. Similarly, the reported LED power consumption is also an estimated value, which has a large variation that depends mainly on body location.

Table 7.1 below compares this work with three state-of-the-art monolithic approaches mentioned before. This work is best to benchmark with the work in TBioCAS'19 [8], since both deploy a CMOS imager related device (4TPPD and PG). The sampling rate of this work is 40 Hz, which is sufficient to recover the PPG signal for further processing and is comparable to the sampling rate reported in [8]. The readout power is reduced by four times due to the short observation window per sample that dominated by the SAR ADC searching phase. The power of the LED is hard to estimate accurately by simulation, but a comparable result has been predicted. The die area is three times smaller than [8], due to the larger fill factor of PG than 4TPPD.

Table 7.1: Performance comparison – monolithic PPG sensing systems

| Parameters | Unit | ISSCC'21 [10] | TBioCAS'19 [8] | ESSCIRC'17 [9] | This work |
|---|---|---|---|---|---|
| **Technology** | nm | 65 | 180 | 180 | 180 |
| **Sampling frequency** | Hz | 20 | 40 | 160000 | 40[c] |
| **Readout SNR**[a] | dB | 90 | 75 | 72 | 84 |
| **LED duty cycle** | % | 0.04 | 0.07 | 10 | 0.03[d] |
| **LED power** | $\mu W$ | 6[b] | 1.97 | N/A | 3[d] |
| **Readout power** | $\mu W$ | 24 | 2.63 | 13-25 | 0.65 |
| **Chip area** | $mm^2$ | 5.5 | 20 | 1.792 | 6.05 |

[a] At a sinusoidal input 1dB below full scale, similar to [10] to avoid overrange, excluding the sensor front end noise, e.g. photon shot noise.
[b] Approximated from its measurement setup and the reported LED duty cycle.
[c] To benchmark with the work reported in TBioCAS'19.
[d] Estimated by assuming PI = 3% as in finger, subject to the change of measurement setup and LED type.

## 7.2. FUTURE WORK

This thesis has presented a energy-efficient monolithic PPG sensing system that can find heart rate. Future work can explore the following directions:

(1) Optimize the sensor using special technology to enhance its sensitivity at red and IR wavelengths. With good sensitivity at multiple wavelengths and the waveform

reproduced by ADC, this system can also monitor other physiological parameters that other PPG sensors are capable of, such as $SpO_2$ and blood pressure.

(2) Deal with motion artefacts (MA). Motion artefacts are signal corruption resulting from motion, which can be sensor-skin displacement and body movement. A sophisticated algorithm that can eliminate MA could be developed. Circuit-level implementation can also be explored, such as using a reference sensor for detecting and storing MA.

(3) Integrate the prevalent use of artificial intelligence (AI). This ultra-low power design also indicates feasibility of continuous PPG monitoring. The large amount of sample data collected by continuous monitoring can lead to good integration with AI, either in digital domain or in the circuit domain. This AI-assisted result can be fed back to calibrate or reconfigure the circuit, and hence a better system performance will be achieved.

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