Evaluation of a Matrix Modular Multilevel Converter based on a Series-Parallel Converter

1st Pablo Burgos and 2nd Ricardo Lizana F.
Centro de Energia
Universidad Catolica de la Santisima Concepcion
Concepcion, Chile
pburgos@ucsc.cl ; ricardolizana@ucsc.cl

3rd Abraham M. Alcaide
Dept. of Electrical Engineerin
Universidad de Sevilla
Sevilla, Spain
amarquez@ieee.org

4th Sebastian Rivera
Electrical Sustainable Energy - DCE&S,
Delft University of Technology
Delft 2628 CD, Netherlands
s.rivera.i@ieee.org

2025 IEEE 34th International Symposium on Industrial Electronics (ISIE) | 979-8-3503-7479-7/25/$31.00 ©2025 IEEE | DOI: 10.1109/ISIE62713.2025.11124757

***Abstract*—The Matrix Modular Multilevel Converter (M3C) is a promising solution for medium-to-high voltage AC/AC conversion, due to its small size by not requiring an intermediate DC-link and its reduced arms compared to a back-to-back scheme. This paper introduces an M3C based on Modular Multilevel Series-Pararell Converter (MMSPC) modules, enabling sensorless voltage balancing between modules to simplify the control scheme needed in the converter. This module, however, introduces overcurrent risk due to the sensorless balancing operation, to solve this, port inductances are incorporated while the commutation frequency is increased. This paper shows a simulation of an M3C based on MMSPC modules, interconnecting two AC systems with a top port inductance configuration and a commutation frequency of 2000 Hz. The results show that an M3C based on MMSPC reduces the control complexity while the top port inductance with the increased frequency reduces the overcurrent risk and improves the converter performance, making it a promising configuration for an optimized M3C for industrial uses.**

***Index Terms*—MMC, M3C, MMSPC, Port inductance**

I. Introduction

The matrix converter is an AC/AC converter composed of nine arms of bidirectional switches without a DC-link, making it more compact than the back-to-back scheme. However, it was known for having a high failure rate, a complex control scheme and being suitable only for low-voltage applications [1]. The Matrix Modular Multilevel Converter (M3C) introduced in [2] replaced the bidirectional switches by series connected power modules, improving robustness and making it suitable for medium-to-high voltage while conserving the compactness of the original topology. The converter is attractive for low-frequency transmission and high-power variable-speed drive applications such as semi-autogenous grinding and wind energy conversion. Despite the advantages, the M3C has an increased control complexity, leading to research to find new strategies to simplify. I.E [3] presents a simplified voltage space vector control avoiding large arm inductance, however, it is designed mainly for low frequency operation. In [4] a decoupled MMC-based control scheme is introduced which uses only five control loops. In [5] a decoupling algorithm is presented, this overcome the tight coupling between the circulating currents of two different frequencies, however, multiple control loops are used on the control scheme, increasing the implementation difficulty. Recent studies improved some aspects of the M3C control scheme. In [6], a control strategy with reduced switching frequency is used for module voltage balancing to minimize commutation losses. In [7] an MMC arbitrary arm energy control concept is extended to the M3C, aiming for a simpler control scheme.

On the other hand, [8] introduce the modular multilevel series-parallel converter (MMSPC), its main feature is an inherent voltage balancing between modules by a capacitor parallelization, reducing the control scheme requirements due to the intrinsic voltage balancing among the modules of the converter. However, this feature introduces a overcurrent risk and requires strategies to limit the current peaks reached.

In this research, an M3C based on MMSPC will be evaluated with the aim of optimizing topology control. For this, the intrinsic module voltage balancing of the MMSPC will be used to eliminate the necessity of voltage balancing control, thereby reducing control complexity and communication requirements. The modules will be improved by using two strategies to reduce the current peaks during the parallelization, one based on the commutation frequency and the other on interconnection inductance between modules [9]. The model and control will be based on the decoupled control of [4] since it is derived from the optimized HVDC MMC control shown in [10] simplifying control complexity and its understanding, however, only 4 control loops will be used since the voltage balancing will be performed by the MMSPC.

II. Topology and modules of the M3C proposed

A. M3C topology

The M3C topology is illustrated in Fig.1 and its based on the one shown in [4], where two AC asynchronous systems are interconnected. The topology consists of 9 arms, each containing "N" MMSPCs arranged in series along with a coupling inductance $\boldsymbol{L}$. Each module has a capacitor that carry the power from one system to another, so instead of having

This work was supported by the following projects from the Agencia Nacional de Investigación y Desarrollo (ANID): FONDECYT-R Grant No. 1230306, Ministerio de Ciencia e Innovación under the project TED2021-130613B-I00 and PID2023-152292OB-I00 as well as "UE - Ministerio de Hacienda y Función Publica - Fondos Europeos - Junta de Andalucía – Consejería de Universidad, Investigación e Innovación project 2024-31824 - 1828102303" and ANID/FONDAP/1523A0006 SERC Chile, Centro de Energía UCSC, Proyecto Institucional de Ingeniería 2030 (ING222010004) and AC3E (ANID/Basal/FB0008).

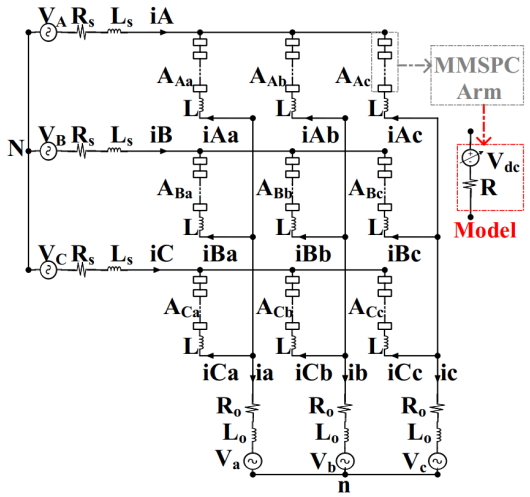

Fig. 1. M3C Topology (based on [4])

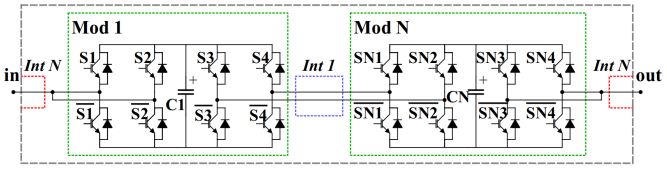

Fig. 2. MMSPC arm with N=2.

one DC-link with a large capacitor, it is distributed among the $9 \cdot N$ modules with smaller capacitors.

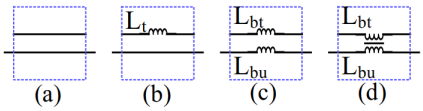

Fig. 3. Interconnection inductances configurations
(a) No Port inductances, (b) Top Port inductance, (c) Dual Port inductances , (d) Differential Port inductances.

B. MMSPC states and over current mitigation

The possible states of the MMSPC used on each arm remain on the interconnections between modules, these are shown in [9]. The interconnection between modules differ between ports [*Int* 1, *Int* 2, ..., *Int* $N-1$] and the "terminal" [*Int* N]. To explain these states, Fig.2 shows an MMSPC arm with $N=2$, and Table I shows the possible states on *Int 1* and *Int N*.

The series (+/-) states from both types of interconnection are used to carry the power from one system to another through the capacitors, the parallel (+/-) states on the other hand are only for the ports, this state perform a parallelization between the capacitors (**C1** and **CN** in Fig.2 case) allowing a sensorless voltage balancing between them, however, depending on the instantaneous voltages of each module, high current peaks may be generated if they are not effectively compensated. The bypass (+/-) states are only for the terminal, theses states bypass the voltage from one module to another without passing through the capacitors. Only one type of parallel and bypass

TABLE I
MMSPC POSSIBLE STATES (BASED ON [9])

Int 1				
State	**S3**	**S4**	**SN1**	**SN2**
Series +	Off	Off	On	On
Series -	On	On	Off	Off
Parallel +	On	Off	Off	On
Parallel -	Off	On	On	Off
Int N				
State	**S1**	**S2**	**SN1**	**SN2**
Series +	On	On	Off	Off
Series -	Off	Off	On	On
Bypass +	On	On	On	On
Bypass -	Off	Off	Off	Off

states is necessary since both (+/-) does the same, however, it is convenient to intercalate both to reduce commutation losses.

To compensate the current peaks during the parallel state, two strategies are used. The first is to increase the switching frequency to reduce the duration of the parallel state, thus reducing the current peaks generated by the balancing current.

The second strategy is adding inductances between modules, this strategy proposed in [9] introduces three configurations of shown in Fig.3 (b), (c) and (d). These inductances are used on ports like *Int 1* shown in Fig.2, the terminal has no inductance since it has the coupling inductance.

III. MODEL FOR THE M3C

For the model, a decoupled one based on [4] is performed. For this, the arm modules are replaced with variable voltage sources and a resistor that represents the internal losses of the arm (see Fig.1). The arm voltages $\mathbf{V_{So}}$ are represented by (1).

$$\mathbf{V_{So}} = \begin{bmatrix} V_{Aa} & V_{Ab} & V_{Ac} \\ V_{Ba} & V_{Bb} & V_{Bc} \\ V_{Ca} & V_{Cb} & V_{Cc} \end{bmatrix} = \underbrace{\begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix}}_{\mathbf{S_{So}}} V_{dc} \quad (1)$$

By a Kirchoff's voltage law (KVL) on the converter between nodes **N** and **n**, (2) is obtained.

$$\underbrace{\begin{bmatrix} V_A & V_B & V_C \\ V_A & V_B & V_C \\ V_A & V_B & V_C \end{bmatrix}}_{\mathbf{V_S}} + (R_s + L_s\frac{d}{dt}) \underbrace{\begin{bmatrix} i_A & i_B & i_C \\ i_A & i_B & i_C \\ i_A & i_B & i_C \end{bmatrix}}_{\mathbf{I_S}}$$
$$+ \underbrace{\begin{bmatrix} V_{Aa} & V_{Ba} & V_{Ca} \\ V_{Ab} & V_{Bb} & V_{Cb} \\ V_{Ac} & V_{Bc} & V_{Cc} \end{bmatrix}}_{\mathbf{V_{So}}} + (R + L\frac{d}{dt}) \underbrace{\begin{bmatrix} i_{Aa} & i_{Ba} & i_{Ca} \\ i_{Ab} & i_{Bb} & i_{Cb} \\ i_{Ac} & i_{Bc} & i_{Cc} \end{bmatrix}}_{\mathbf{i_{So}}} +$$
$$(R_o + L_o\frac{d}{dt}) \underbrace{\begin{bmatrix} i_a & i_a & i_a \\ i_b & i_b & i_b \\ i_c & i_c & i_c \end{bmatrix}}_{\mathbf{I_o}} + \begin{bmatrix} V_{Nn} & V_{Nn} & V_{Nn} \\ V_{Nn} & V_{Nn} & V_{Nn} \\ V_{Nn} & V_{Nn} & V_{Nn} \end{bmatrix} \quad (2)$$
$$+ \underbrace{\begin{bmatrix} V_a & V_a & V_a \\ V_b & V_b & V_b \\ V_c & V_c & V_c \end{bmatrix}}_{\mathbf{V_o}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Where the matrices and parameters with "S" subscript are input values, the parameters with "o" subscript are output values and the parameters with "So" subscript and without subscript are arm values.

To reduce the complexity of obtaining the dynamic equations of the converter, the decoupling is performed with the matrices **"P"** and **"Q"**, shown in (3) and (4), respectively.

$$\mathbf{P} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \quad (3)$$

$$\mathbf{Q} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \quad (4)$$

These matrices acts as filters, $\mathbf{P}$ only allows the DC component while $\mathbf{Q}$ allows only the AC component to pass through. Using these matrices in the KVL, the representation of the arm current equation ($\mathbf{I_{So}}$) is obtained in (5):

$$\begin{aligned} \frac{d\mathbf{I_{So}}}{dt} = &- \mathbf{P}\left(\frac{(R+3R_S)\mathbf{I_{So}} + \mathbf{V_{So}} - \mathbf{V_S}}{L+3L_S}\right)\mathbf{Q} \Big\}\frac{d\mathbf{I_S}}{dt} \\ &- \mathbf{Q}\left(\frac{(R+3R_o)\mathbf{I_{So}} + \mathbf{V_{So}} - \mathbf{V_o}}{L+3L_o}\right)\mathbf{P} \Big\}\frac{d\mathbf{I_o}}{dt} \\ &- \mathbf{Q}\left(\frac{R\mathbf{I_{So}} + \mathbf{V_{So}}}{L}\right)\mathbf{Q} \Big\}\frac{d\mathbf{I_c}}{dt} \\ &- \mathbf{P}\left(\frac{(R_S+R_o)I_{So} + \frac{1}{3}(\mathbf{V_o} - \mathbf{V_S})}{L_S+L_o}\right)\mathbf{P}\Big\}0 \end{aligned} \quad (5)$$

A. Input and output current model.

The first and the second component in (5) are the input and output currents respectively. These currents are decoupled as follows, where both are analogous.

$$\frac{d\mathbf{I_S}}{dt} = -\mathbf{P}\left(\frac{(R+3R_S)\mathbf{I_S} + \mathbf{V_{So}} - \mathbf{V_S}}{L+3L_S}\right)\mathbf{Q} \quad (6)$$

$$\frac{d\mathbf{I_o}}{dt} = -\mathbf{Q}\left(\frac{(R+3R_o)\mathbf{I_o} + \mathbf{V_{So}} - \mathbf{V_o}}{L+3L_o}\right)\mathbf{P} \quad (7)$$

After some algebraic manipulations on (6) and (7), the following equations are obtained.

$$\frac{d\mathbf{I_S}}{dt}(L+3L_S) + (R+3R_S)\mathbf{I_S} = -\mathbf{P}(\mathbf{V_{So}})\mathbf{Q} + \mathbf{V_S} \quad (8)$$

$$\frac{d\mathbf{I_o}}{dt}(L+3L_o) + (R+3R_o)\mathbf{I_o} = -\mathbf{Q}(\mathbf{V_{So}})\mathbf{P} + \mathbf{V_o} \quad (9)$$

The voltages $\mathbf{Vs}$ and $\mathbf{Vo}$ are neglected to make the expression lineal. By using (1) in (8) and (9), then using Laplace transform and some algebraics manipulations to simplify, it is possible to obtain the transfer functions (10) and (11).

$$\frac{\mathbf{I_S}}{\mathbf{M_S}} = \frac{-Vc_{dc}}{(L+3L_S)s + (R+3R_S)} \quad (10)$$

$$\frac{\mathbf{I_o}}{\mathbf{M_o}} = \frac{-Vc_{dc}}{(L+3L_o)s + (R+3R_o)} \quad (11)$$

B. Circulating current model.

The third term in (5) corresponds to the circulating current $\mathbf{I_c}$, which circulates within the converter arms. The decoupled control allow to control the circulating current in an independent way, and for achieve this, the model presented in (12) is proposed.

$$\frac{d\mathbf{I_c}}{dt} = -\mathbf{Q}\left(\frac{R\mathbf{I_c} + \mathbf{V_{So}}}{L}\right)\mathbf{Q} \quad (12)$$

By realigning the voltage is possible to obtain (13).

$$\frac{d\mathbf{I_c}}{dt}L + R\cdot\mathbf{I_c} = -\mathbf{Q}(\mathbf{V_{So}})\mathbf{Q} \quad (13)$$

Using (1) in (13) and using Laplace transformation and then some algebraic manipulations to simplify, is possible to obtain a transfer function to control the circulating current $\mathbf{I_c}$ by the decoupled modulation index $\mathbf{M_c}$ showed in (14).

$$\frac{\mathbf{I_c}}{\mathbf{M_c}} = \frac{-Vc_{dc}}{Ls + R} \quad (14)$$

C. Average capacitor voltage model.

To coordinate power transfer between input and output, a reference for average DC voltage is settled and $\mathbf{I_S}$ is adjusted to reach it. The model begins by using the power formula for the capacitors considering the $9\cdot N$ modules, this equals the input power, output power and losses.

$$Pc_{tot} = 9\cdot N\left(\frac{C_{dc}}{2}\cdot\frac{dVc_{dc}^2}{dt}\right) = \mathbf{P_S} - \mathbf{P_o} - \mathbf{P_{loss}} \quad (15)$$

The average DC voltage in the capacitors will depend only on input, so the output power and losses are neglected. The instantaneous input power in (15) can be defined as follows.

$$\mathbf{P_S} = \frac{3}{2} \cdot \mathbf{V_S} \cdot \mathbf{I_{S\ ref}} \tag{16}$$

Using (16) on (15), (17) is obtained.

$$9 \cdot N \left(\frac{C_{dc}}{2} \cdot \frac{dVc_{dc}^2}{dt} \right) = \frac{3}{2} \cdot \mathbf{V_S} \cdot \mathbf{I_{S\ ref}} \tag{17}$$

Using Laplace transformation on (17) and realigning it, the following transfer function is obtained.

$$\frac{Vc_{dc}^2}{\mathbf{I_{S\ ref}}} = \frac{\mathbf{V_S}}{3 \cdot N \cdot C_{dc} \cdot s} \tag{18}$$

The fourth term in (5) is related with the module voltage balancing. However, since the modulation strategy of the Modular Multilevel Series-Parallel Converter (MMSPC) cells inherently enables internal voltage balancing among the cells within the same arm, the use of this component is not required.

IV. Control Schemes of the M3C

A. Input and output control schemes.

The control scheme for input and output are analogue. These schemes are based on abc-dq stationary reference frame transformation. The d and q components obtained are controlled with a proportional-integrative controller (PI) tuned with the models shown in (10) for input and (11) for output. The reference current $i_{od\ ref}$ determines the power of the output system (master), while the reference current $i_{sd\ ref}$ adapts the power of the input (slave) to achieve a power balance between both systems. The q components are settled to zero to optimize the power factor of the systems.

B. Circulating current control schemes.

In order to obtain the circulating current, it is possible to use the next expression:

$$\mathbf{I_c} = -\mathbf{Q} \cdot I_{So} \cdot \mathbf{Q} \tag{19}$$

These currents are minimized by settling a reference in zero with a PI tuned by the transfer function on (14).

C. Average capacitor voltage control scheme.

For this control scheme, the average DC voltage on the capacitors $\overline{Vc}_{dc}$ tracks a settled reference value $\overline{Vc}_{dc\ ref}$ with a PI controller tuned with the transfer function on (18), and thus, the $i_{sd\ ref}$ is obtained.

All control schemes are illustrated in Fig.4, where the modulation indices are sum into a general modulation index for each module $\mathbf{M_{T\ So}}$.

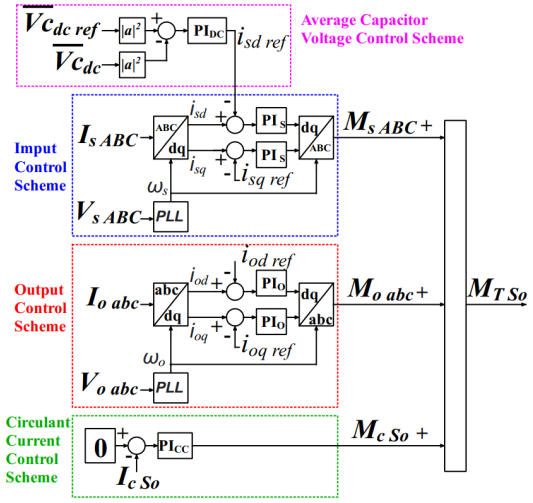

Fig. 4. General Control Scheme.

V. MMSPC Modulation Scheme

The modulation strategy compares the sum of the modulation index $\mathbf{M_{T\ So}}$ of each module with two carriers **Tri** and $-$**Tri**, following the next logic [9].

$$\begin{aligned} &\textbf{Serie +}: \quad \mathbf{M_{T\ So}} \geq \mathbf{Tri} \wedge \mathbf{M_{T\ So}} \geq -\mathbf{Tri}, \\ &\textbf{Serie -}: \quad \mathbf{M_{T\ So}} \leq \mathbf{Tri} \wedge \mathbf{M_{T\ So}} \leq -\mathbf{Tri}, \\ &\textbf{Parallel/Bypass (+/-)}: \quad -\mathbf{Tri} < \mathbf{M_{T\ So}} < \mathbf{Tri} \\ &\qquad\qquad\qquad\qquad \wedge -\mathbf{Tri} > \mathbf{M_{T\ So}} > \mathbf{Tri}. \end{aligned} \tag{20}$$

For each module, the carriers have a phase shift obtained by the next expression where k is the referenced module and N is the total number of modules.

$$\phi_{Tri,-Tri} = \frac{2\pi}{N}(k-1), \qquad \text{with k} = 1, 2, 3, ..., N. \tag{21}$$

VI. Simulation Results

Two asynchronous systems are simulated in Matlab Simulink, with a reference change $i_{od\ ref}$ at 2 s changing the power from 1000 W to -1000 W at the output system (master).

The top inductance configuration is used and its behavior is compared with the configuration with no port inductance. The top port inductance is accompanied by a series resistor R_{top} to simulate the losses.

The simulation parameters are indicated in Table II while the tuned PI parameters are shown in Table III.

A. Average DC voltage and capacitor voltage

The capacitors voltages are shown in Fig.5, these remains around 167 V, settling an approx. of 500 V per arm. It can be seen that adding a port inductance increase the capacitor voltage ripple in $\pm$ 2 V approx. After an i_d reference settling, the voltage ripple increases, however, it decreases over time. This shows that the self-voltage balancing of the MMSPC works properly, even with a i_d reference change and a higher

TABLE II
SIMULATION PARAMETERS

Parameter	Value
Input voltage $\mathbf{V_S}$	220 V-rms
Input frequency $\mathbf{f_S}$	50 Hz
Input inductance $\mathbf{L_S}$	15 mH
Input resistance $\mathbf{R_S}$	0.1 Ω
Output voltage $\mathbf{V_o}$	110 V-rms
Output frequency $\mathbf{f_o}$	60 Hz
Output inductance $\mathbf{L_o}$	15 mH
Output resistance $\mathbf{R_o}$	0.1 Ω
Output i_d reference before 2 s I_{od}	4.285 A-peak
Output i_d reference after 2 s I_{od}	-4.285 A-peak
Input i_q reference I_{sq}	0 A-peak
Output i_q reference I_{oq}	0 A-peak
Coupling Inductance L	5 mH
Arm Resistance R	10 mΩ
Number of modules per arm N	3 Modules
Port inductance L_t, for $N = 3$	2.5 mH
Series port resistor R_{top}, for $N = 3$	10 mH
Average capacitor voltage reference Vc_{dc}	167 Vdc
Module capacitance C_{dc}	2 mF
Carriers frequencies f_{Tri} and $f_{\text{-Tri}}$	2000 Hz

TABLE III
PI CONTROLLERS PARAMETERS

PI	Kp	Ti	Saturation	Cutoff Frequency	Damping Ratio
Is Currents	-0.091197	906.62 μs	±0.7	150 Hz	0.707
Io Currents	-0.26056	906.62 μs	±0.4	275 Hz	0.447
Ic Currents	-0.064671	917.43 μs	±0.25	500 Hz	0.707
Average Vc_{dc}	0.012631	9.48 ms	±42.85	50 Hz	0.718

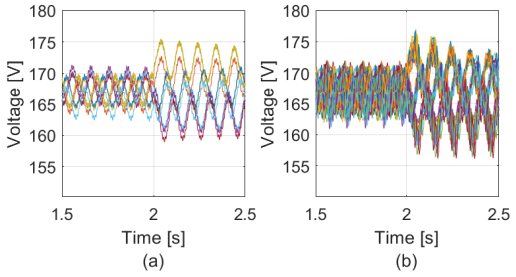

Fig. 5. Capacitor voltages: (a) Without port inductance, (b) With port inductance.

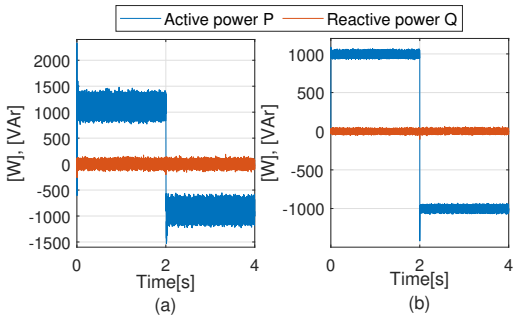

Fig. 6. Active and reactive power.(a) Input powers, (b) Output powers.

voltage ripple, keeping the capacitor voltages balanced without

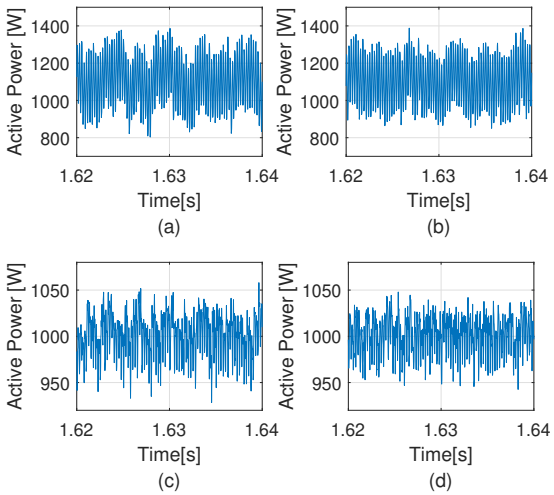

Fig. 7. Active power:(a) Input power without port inductance, (b) Input powers with top port inductance, (c) Output power without port inductance, (d) Output power with top port inductance.

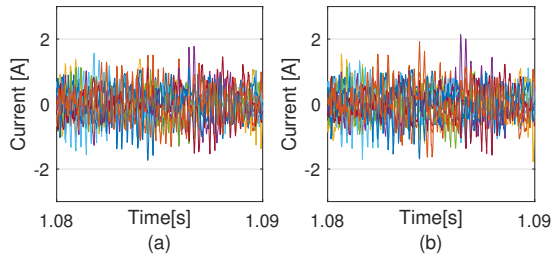

Fig. 8. Circulant currents: (a) Without port inductance, (b) With top port inductance.

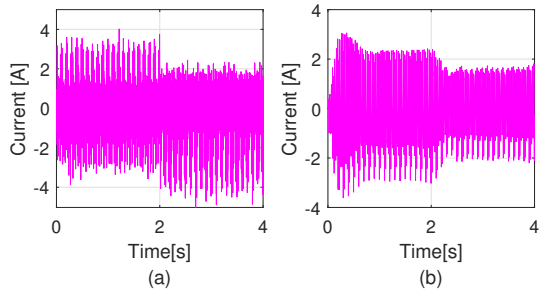

Fig. 9. Current between modules 1 and 2 in arm Aa: (a) Without port inductance, (b) With top port inductance.

a control scheme dedicated exclusively to this task.

B. Active and reactive power

The active and reactive power from both AC sides are shown in Fig.6. The active power is changed from 1000 W to -1000 W, maintaining the reactive power on 0 VAr. The active output power shown in Fig.6 (b) is around the 1000 W intended, with a variability of ± 50 W approx., increasing after the reference change, the output reactive power keeps

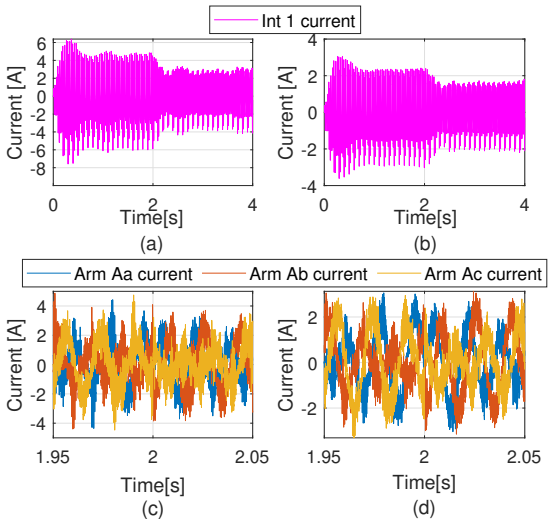

Fig. 10. Current between module 1 and 2 and currents from Arms Aa, Ab and Ac with top inductance configuration and different commutation frequency. (a) Current between module 1 and 2 using 1000 Hz commutation, (b) Current between module 1 and 2 using 2000 Hz commutation, (c) Arm currents using 1000 Hz commutation, (d) Arm currents using 2000 Hz commutation.

suppressed around the 0 VAr with $\pm$ 43 VAr approx. On the other hand, the active and reactive input powers shown in Fig.6 (a) show that the output powers exhibit a considerable ripple due to the capacitor ripple, preventing optimal system balancing. However, since the mean voltages track their reference value, the internal balance of the system is maintained.

The active power between 0 s and 2 s is compared with and without the top port inductance in Fig.7. The top port inductance slightly reduces the peaks of the active input and output power.

C. Circulant Currents

In Fig.8 the circulant currents are shown. These currents are balanced on every arm, being reduced around 0 A, proving that this control is working properly. The circulant current peaks increase slightly with the top port inductance configuration.

D. Interconnections currents and Arm currents

In Fig. 9, a comparison of the current between the modules 1 and 2 (Interconnection Current) of the arm Aa without port inductance and with top port inductance is presented. The current peaks reached without port inductance shown in Fig. 9 (a) are reduced with the top port inductance configuration shown in Fig. 9 (b), this proves that the introduced port inductance effectively reduce the current peaks reached.

On the other hand, Fig.10 shows the current between the modules 1 and 2 in the arm Aa and the iAx currents with a carrier frequency of 1000 Hz and 2000 Hz using the top port inductance, it can be observed that increasing the commutation frequency reduces the current peaks in the interconnections and the ripple on the arm currents.

The comparison shows that the configuration with the top port inductance is more recommendable than the configuration without port inductance. Although the capacitor ripple and the peaks in circulating current increase, the risk caused by current peaks during parallel states is reduced while the quality of the power transferred between the AC systems is improved.

VII. Conclusions

This paper presents a matrix modular multilevel converter (M3C) based on modular multilevel series-parallel converters (MMSPCs) with improvements in performance while reducing control complexity. The MMSPC is well suited for M3C, as it eliminates the need for capacitor voltage balancing control schemes. The sensorless voltage balancing works properly, reducing the control needed which, in practice, enables faster balancing by avoiding communication delays.

The proposed top port inductance configuration and the higher switching frequency effectively reduce current peaks between modules, reducing the risk of overcurrent of the MMSPC while the performance is improved by achieving slightly less ripple amplitude for power and significally less ripple for the arm currents. The top port inductance also slightly increases the circulant currents and the capacitor voltage ripple, however, it does not have a significant effect on the performance of the converter as is shown in this paper.

This M3C configuration offers a promising solution to the complex control challenges of this topology, making it more suitable for industrial applications.

References

[1] L. Empringham, J. W. Kolar, J. Rodriguez, P. W. Wheeler, and J. C. Clare, "Technological issues and industrial application of matrix converters: A review," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4260–4271, 2013.

[2] R. Erickson and O. Al-Naseem, "A new family of matrix converters," in *IECON'01. 27th Annual Conference of the IEEE Industrial Electronics Society (Cat. No.37243)*, vol. 2, 2001, pp. 1515–1520 vol.2.

[3] Y. Miura, T. Mizutani, M. Ito, and T. Ise, "Modular multilevel matrix converter for low frequency ac transmission," in *2013 IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS)*, 2013, pp. 1079–1084.

[4] D. Arancibia, M. A. Perez, and J. Rodriguez, "Decoupled control of a three-phase to three-phase modular multilevel matrix converter," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 404–408.

[5] S. Liu, X. Wang, Y. Meng, P. Sun, H. Luo, and B. Wang, "A decoupled control strategy of modular multilevel matrix converter for fractional frequency transmission system," *IEEE Transactions on Power Delivery*, vol. 32, no. 4, pp. 2111–2121, 2017.

[6] Z. Zhang, Y. Jin, and Z. Xu, "Modeling and control of modular multilevel matrix converter for low-frequency ac transmission," *Energies*, vol. 16, no. 8, 2023. [Online]. Available: https://www.mdpi.com/1996-1073/16/8/3474

[7] M. Utvić, P. Bontemps, and D. Dujić, "Direct arm energy control of the modular multilevel matrix converter," *IEEE Access*, vol. 11, pp. 1793–1805, 2023.

[8] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel module connectivity: Topology and control," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 203–215, 2015.

[9] Z. Li, R. Lizana F., S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module implementation and modulation strategy for sensorless balancing in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8405–8416, 2019.

[10] M. A. Pérez, R. Lizana F., and J. Rodríguez, "Decoupled current control of modular multilevel converter for hvdc applications," in *2012 IEEE International Symposium on Industrial Electronics*, 2012, pp. 1979–1984.