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Aging Characteristics of FR-4 at Different Frequencies

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***Abstract*- PCB transformers are emerging as a promising alternative to medium-frequency wire-wound transformers due to their numerous advantages. However, research on FR-4, the primary PCB insulation material, remains limited. This study investigates the dielectric performance of PCB electrodes through interlayer breakdown tests at 50 Hz, yielding an aging curve for this condition. Additionally, layer-to-layer breakdown tests were conducted at 50 Hz and 1 kHz, revealing a reduction in time to breakdown with increasing frequency. Notably, interlayer breakdown is significantly more likely, exhibiting a breakdown strength eight times lower than that of layer-to-layer breakdown.**

I. Introduction

Medium-frequency (MF) transformers have the potential to be replaced by PCB planar transformers in future applications [1] owing to their numerous advantages over traditional wire-wound transformers. PCB planar transformers exhibit higher power density, enhanced energy transfer efficiency through reduced copper and core losses, improved thermal management that facilitates heat sink application, increased reliability, and easy integration [2-3]. The planar design provides a larger surface area for heat dissipation, while the compact structure minimizes the winding lengths, leading to reduced magnetic flux leakage and lower electromagnetic interference.

Recent research has advanced the understanding and design of planar transformers. In [4], Spro conducted a comprehensive evaluation of the electrical performance of various planar transformer winding types, offering critical insights for optimizing winding designs. Also, Wang presented a detailed methodology for designing medium voltage (MV) PCB planar transformers, demonstrating that applying a semi-conductive coating to winding surfaces effectively mitigates electric field stress at winding edges. Furthermore, the treatment of winding terminals eliminated surface partial discharges, enhancing transformer reliability [5].

Within planar transformers, the winding turns are insulated by Flame Retardant 4 (FR-4), a cost-effective material known for its excellent mechanical strength and thermal conductivity, making it suitable for high-power (HP) applications. The FR-4 insulation is embedded within prepreg, similar to the PCB electrode samples illustrated in Fig. 1. Whereas, despite these advantages, the electrical properties of FR-4, remain inadequately explored.

In [6], Albert partially addressed this gap by investigating interlayer and layer-to-layer breakdown phenomena in PCB electrodes through short- and long-term breakdown tests at frequencies of 50 Hz, 130 kHz, and 190 kHz. However, the analysis lacked Weibull distribution modeling to assess failure probability, and the long-term tests failed to achieve effective accelerated aging results, as no breakdowns occurred during testing. These limitations highlight the requirement for further experimental studies to comprehensively evaluate dielectric aging behavior of FR-4 under various frequencies and stress conditions.

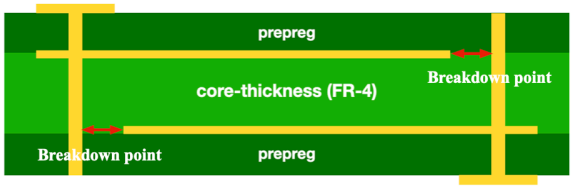

Fig. 1 Cross-section of the PCB electrodes used for breakdown tests.

II. Numerical Analysis and Experimental Procedure

A. Numerical Analysis

Numerical simulations were conducted to determine the field strength distribution of the PCB electrodes under MV conditions, with the results shown in Fig. 2. The simulations revealed that the field strength peaks at the electrode layer edges, commonly referred to as triple points. When the PCB core thickness is sufficiently large, the interlayer breakdown is more likely to occur along the interface between prepreg and core material. For the electrodes used for interlayer breakdown tests, the core material was selected with a standard thickness of 0.71 mm, balancing the technical performance and cost-effectiveness. The PCB electrode also adhered to a precise distance of 4.0 mm between electrode layer edge and via, as highlighted by red arrows in Fig. 1.

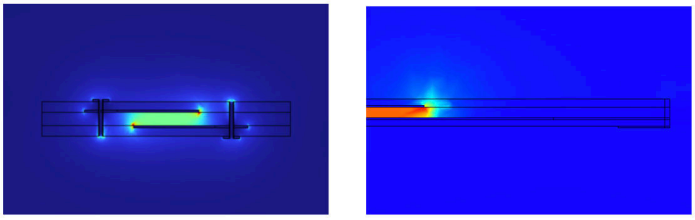

Fig. 2 Overall electric field strength distribution (color red symbolizes high field strength).

B. Experimental Set-up Performed at 50 Hz

Figure 3 and 4 depict the schematic and experimental setup used for high-voltage (HV) ramp sinusoidal breakdown tests and accelerated aging experiments at 50 Hz, respectively. To

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mitigate the impact of surge currents following a breakdown event, a current-limiting resistor with a resistance of 75 kΩ is incorporated into the circuit. This resistor not only limits the magnitude of the surge current but also increases the circuit's time constant τ, thereby enhancing the system's stability during breakdown events. To eliminate partial discharges and ensure accurate measurements, the PCB electrodes are fully immersed in the silicone oil. The use of silicone oil provides uniform insulation and prevents surface discharges, which can affect the reliability and consistency of the test results.

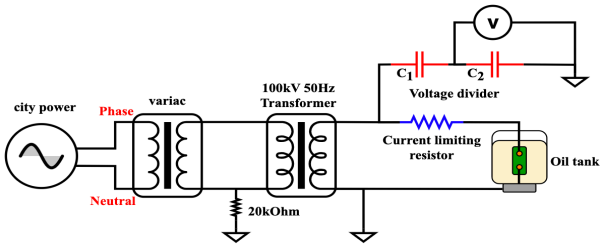

Fig. 3 Schematic of the experimental set-up at 50 Hz.

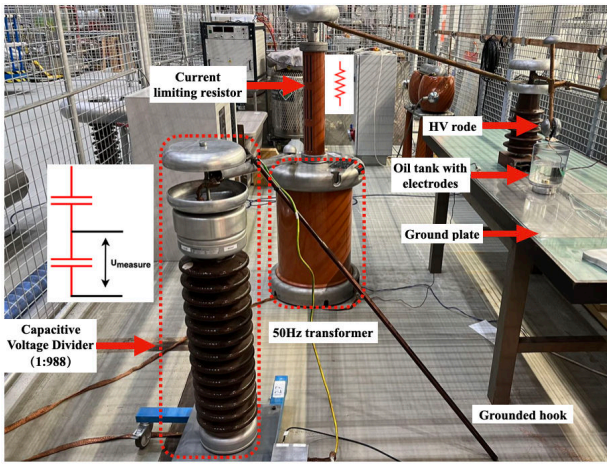

Fig. 4 Experimental set-up for PCB electrode breakdown tests at 50 Hz

C. Experimental Set-up Performed at 1 kHz

Fig. 5 illustrates the schematic of the experimental setup designed to evaluate the layer-to-layer breakdown of 0.36 mm PCB electrodes at a frequency of 1 kHz. The experimental process begins with the input signal, generated by a function generator, being directed to the Arduino A_0 pin for initial signal processing. The signal is then routed to the TREK amplifier, where it undergoes a substantial amplification by a factor of 3000. Additionally, the amplifier provides a feedback signal, scaled down by the same factor, which is sent to the Arduino A_1 pin for monitoring and analysis.

Prior to the electrode breakdown, the feedback signal from the TREK amplifier remains at a high amplitude, which prevents the Arduino from activating the relay control mechanism. When a breakdown occurs, the amplitude of the return signal at A_1 pin drops significantly. Once this return voltage falls below a predefined threshold, the Arduino's D_7 pin triggers a control signal to deactivate the relay. This process ensures that the duration of the short-circuited state in the test circuit is minimized, thereby protecting the experimental setup and preserving the integrity of the measurements.

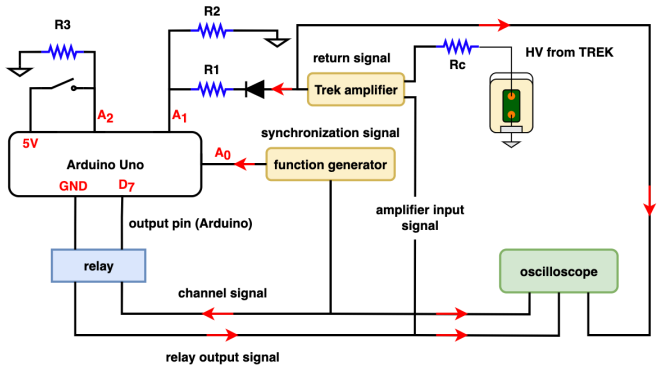

Fig. 5 Schematic of the HV accelerated layer-layer aging tests of the 0.36 mm thickness PCB electrodes at 1 kHz

III. Experimental results

A. Interlayer breakdown tests at 50 Hz

Based on the ramp sinusoidal breakdown data obtained from the experiments, the median interlayer breakdown voltage of the electrodes was determined as 28.6 kVrms, corresponding to an electric field strength of approximately 7.2 kV/mm, as illustrated in Fig. 6. This value could serve as a benchmark for evaluating the dielectric characteristics of FR-4 under high-voltage stress.

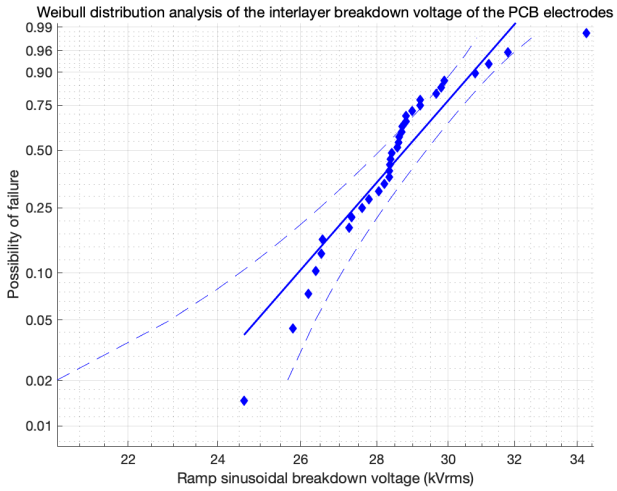

Fig. 6 Weibull distribution analysis of the PCB electrode interlayer ramp sinusoidal breakdown voltage at 50 Hz

The power law equation governing the HV accelerated aging experiments is given in formula (1). Also, the median time to

$$t = k\left(\frac{E}{E_0}\right)^{-n} \tag{1}$$

$$log(t) = -n \cdot log(E/E_0) + log k \tag{2}$$

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breakdown is utilized for constructing the aging curve, where t is the time to breakdown, k denotes the time to breakdown when the tested PCB sample is subjected to the reference field strength, E is the actual electric field strength in kilovolts per millimeter (kV/mm), and E_0 represents the reference field strength, which is 1.0 kV/mm. Formula (2) provides the logarithmic transformation of formula (1).

Fig. 7 indicates the HV accelerated interlayer aging curve of the PCB electrodes with a 4 mm gap, tested at 50 Hz. During the experiments, the inter-layer field strength was maintained at 5.5 kV/mm, 6 kV/mm, and 6.5 kV/mm. The corresponding time-to-breakdown values ($t_{5.5}$, t_6 and $t_{6.5}$) were recorded for each field strength. At a higher field strength of 7 kV/mm, the time-to-breakdown (t_7) was significantly reduced, making it unsuitable for inclusion in the aging curve due to the deviation from the overall trend. From the aging curve, the parameters n and k were determined as 17.14 and $10^{36.61}$, respectively. These values provide critical insights into the aging behavior and dielectric performance of the PCB electrodes under high-voltage stress.

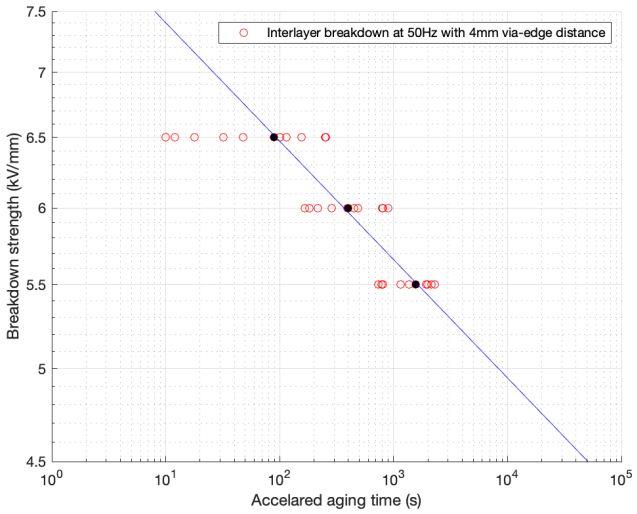

Fig. 7 The HV accelerated inter-layer aging curve of the PCB electrodes obtained at 50 Hz

B. Layer-to-layer breakdown tests at 50 Hz

Layer-to-layer ramp sinusoidal breakdown experiments were conducted using two types of electrodes: one with a narrow electrode width of 5 mm and the other with a wider width of 10 mm. All electrodes had a consistent thickness of 0.36 mm. The test results illustrate that the breakdown voltage for both PCB electrode types was nearly identical, approximately 21.5 kVrms, corresponding to a breakdown strength of 59 kV/mm, as shown in Fig. 8. In comparison, interlayer breakdown occurred more readily, exhibiting a breakdown strength that was 8 times lower than that of layer-to-layer breakdown.

$$F_1(U) = 1 - \exp\left[-\left(\frac{U}{\eta_1}\right)^{\beta}\right] \tag{3}$$

$$R_1(U) = 1 - F_1(U) = \exp\left[-\left(\frac{U}{\eta_1}\right)^{\beta}\right] \tag{4}$$

From Fig. 8, a comparative analysis of the ramp breakdown results for wider and narrow electrodes reveals the volume effect. Specifically, for the same probability of failure, the breakdown strength of the narrower PCB electrode samples is marginally higher than that of the wider electrode samples. This phenomenon is explained using the scaling laws (5-6).

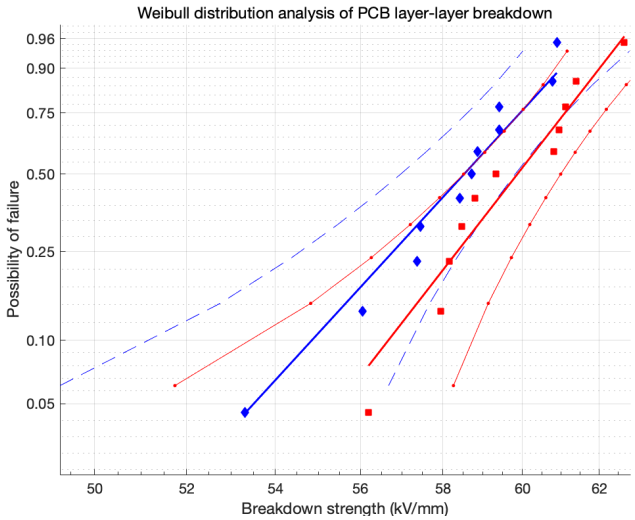

Fig. 8 Weibull analysis of the electrode layer-layer ramp breakdown strength at 50 Hz (blue for wider and red for narrow electrodes)

If the value of the applied voltage on the tested electrode is U, its possibility of breakdown $F_1(U)$ can be expressed by a two-parameter Weibull distribution formula (3). Furthermore, the reliability $R_1(U)$ of the electrodes under U can be derived using formula (4). Symbol η_1 denotes the scale parameter and β is the shape parameter. If the value of U equals to η_1, PCB sample's possibility of failure would become 63.2%.

$$F_n(U) = 1 - \exp\left[-n\left(\frac{U}{\eta_1}\right)^{\beta}\right] = 1 - \exp\left[-\left(\frac{U}{\eta_n}\right)^{\beta}\right] \tag{5}$$

$$\eta_n = \frac{\eta_1}{n^{\frac{1}{\beta}}};\quad \eta_2 = \frac{\eta_1}{2^{\frac{1}{\beta}}} \tag{6}$$

If the surface area of the copper layers in the PCB electrodes is increased by a factor of n, and the applied voltage remains constant at U, the possibility of PCB electrode breakdown $F_n(U)$ can be described by formula (5). The corresponding scale parameter, denoted as η_n, is given by (6). Consequently, to achieve a failure rate of 63.2%, the value of η_2 will be less than η_1.

During the PCB electrode aging tests at 50 Hz, the samples were tested at voltages of 17, 15, and 13 kV. For every set of experiments, the median time to breakdown was used as the representative value. The PCB samples were subjected to field strengths of 47.22, 41.67, and 36.11 kV/mm, respectively. The resulting aging curve is presented in Fig. 9 (red line). The obtained value of the parameter n_{50} is 11.5.

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C. Layer-to-layer breakdown tests at 1 kHz

Fig. 9 illustrates the HV accelerated layer-layer aging curves of the PCB electrodes at frequencies of 50 Hz and 1 kHz. The aging curves are presented with the median time to breakdown at a specified field strength. It is evident that, at the same field strength, the PCB electrodes subjected to the higher frequency of 1 kHz exhibit a shorter time to breakdown compared to those tested at 50 Hz. The value of the aging exponent n is 11.38 for 1 kHz and 11.5 for 50 Hz.

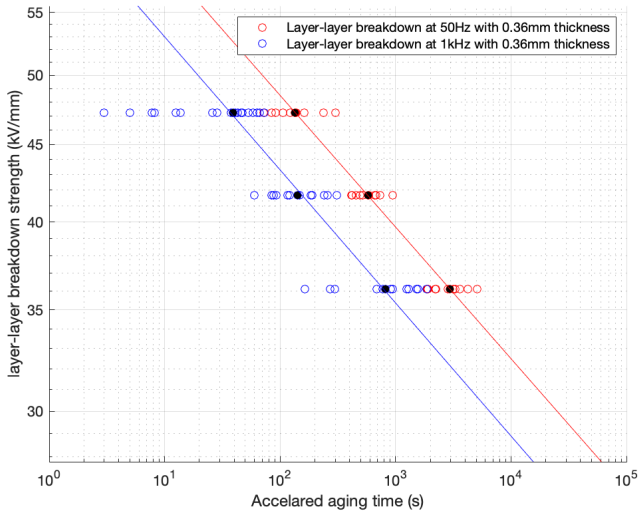

Fig.9 he HV accelerated layer-layer aging curve of the PCB samples obtained both at 50 Hz and 1 kHz

IV. Conclusion

The experimental results demonstrate that the layer-to-layer time to breakdown of FR-4 samples decreases with the growth of voltage frequency. Interlayer failure, particularly from PCB vias to copper edges, is critical owing to the relatively low breakdown strength of approximately 7.2 kV/mm at 50 Hz. At higher operating frequencies, the PCB interlayer breakdown strength is expected to decrease significantly. Further research is required to investigate high-frequency interlayer aging and breakdown behavior of the FR-4 samples. This will enable the design, construction, and validation of a planar transformer prototype as a potential alternative to wire-wound MF transformers.

Acknowledgment

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