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Microstructural Anisotropy-Governed Thermal Performance of Pressureless Sintered Silver in QFN Packaging

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***Abstract*—Pressureless sintered silver paste is widely used in SiC power electronic packaging for its superior thermal and electrical properties, enabling efficient heat dissipation and improved device reliability. Current thermal conductivity models frequently assume isotropic thermal behavior to simplify heat transfer calculations, yet these models neglect the inherent anisotropic porosity of sintered silver materials. This omission introduces errors in the characterization of these materials' thermal performance. This research investigates how the spatial anisotropic distribution of pressureless sintered silver's microstructure impacts QFN packaging's overall thermal conduction performance. This investigation is achieved by comparing lateral/vertical porosity differences between two materials and applying multidimensional thermal conductivity modeling. Two types of pressureless sintered silver were employed as die-attach materials to fabricate SiC MOSFET-based QFN packaging. The sintered microstructures' lateral and vertical cross-sections were characterized using scanning electron microscopy (SEM), enabling quantitative extraction of anisotropic porosity distributions. Subsequently, a numerical model was developed using the extracted porosity data to enhance the accuracy of heat transfer predictions in sintered silver layers while considering anisotropic thermal conductivity. Thermal resistance characterization was conducted on two QFN packages, and the accuracy of the proposed modeling methodology was validated by establishing the interrelation between experimental thermal resistance measurements and theoretical thermal conductivity predictions. This study demonstrates a refined approach to evaluating and optimizing sintered silver materials, providing a more accurate and application-driven thermal management strategy for SiC MOSFET power packaging.**

***Keywords*—Pressureless sintered silver, Anisotropic porosity, QFN package, Thermal conductivity model, Thermal resistance**

# Both authors contributed equally to this work.

I. Introduction

For wide bandgap semiconductor devices such as SiC and GaN used in high power density and high temperature power electronic systems, package thermal management has become a key factor affecting device reliability and service life[1]. Due to its excellent thermal conductivity, outstanding electrical properties, high-temperature stability, and mechanical reliability, pressureless sintered silver has become one of the most promising chip interconnect materials in the new generation of power electronic packaging [2].Thanks to advancements in sintered silver paste formulations, graded mixing of nanoparticles and micron particles, and the addition of volatile organic matter and reactive additives, sintered silver can be densified at temperatures below 180 °C without applying external pressure. The resulting silver joint has a shear strength exceeding 35 MPa and a thermal conductivity higher than 200 $W.m^{-1}.K^{-1}$ [3]. These advantages significantly reduce the risk of thermal stress and package deformation. This makes sintered silver an attractive option for high-power and high-temperature applications, such as electric vehicles, renewable energy systems, and industrial power modules.

Meanwhile, a large number of studies have explored the thermal modeling and reliability issues of sintered silver interconnects. Zhao *et al.* developed an analytical and numerical model based on the extension differential scheme (EDS) to predict the effective thermal conductivity of porous, sintered silver layers. Their results were consistent with those of finite element simulations [4]. Additionally, Youssef *et al.* correlated the overall porosity of the sintered nanosilver bonding layer with its thermal and mechanical properties [5].

However, to simplify the calculation, most of these methods assume that sintered silver has isotropic thermal

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properties, meaning its thermal conductivity is the same in all directions. In fact, the microstructure of pressureless sintered silver is direction-dependent. The inconsistency of particle stacking, solvent evaporation path and sintering shrinkage during the sintering process often leads to anisotropic pore distribution in the joint layer. The anisotropy of the pore structure has been reflected in cross-sectional SEM observations [6]. This structural anisotropy will change the heat flow path. If it is not taken into account, it will introduce significant errors in the thermal resistance prediction.

This study investigated how pressureless sintered silver microstructure anisotropy affects thermal performance. Two different pressureless sintered silver materials were selected for a comparative study. The cross-sectional pore structure of each material was characterized quantitatively in the horizontal and vertical directions. Porosity was processed using a binarization algorithm, and the results of the anisotropic pore characterization were converted into effective thermal conductivity using COMSOL finite element simulation. Finally, transient thermal resistance tests were performed on QFN package samples with the aforementioned sintered silver materials as chip interconnect layers to verify the modeling method. This study establishes a clear connection between microstructural anisotropy and package-level thermal performance, providing guidance for more accurate thermal design and material optimization in power electronic packaging.

II. Experimental Setup and Methods

A. Experimental and simulation overview

The impact of microstructural anisotropy of the sintered silver layer on thermal conduction was systematically assessed following the procedure in Fig. 1. Two commercial pressureless silver pastes were used as die-attach materials for a SiC MOSFET in a QFN package. Horizontal and vertical cross-sections were prepared for scanning electron microscopy (SEM) analysis to quantify pore distributions. The extracted porosity data were processed via binarization and used in COMSOL to build two-dimensional (2D) microstructure-based thermal models for directional conductivity simulation.

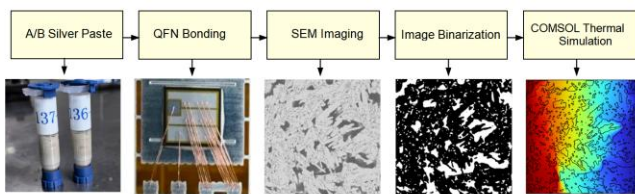

Fig. 1. Experimental and simulation flowchart

B. Sample preparation and experimental setup

For this study, two commercially available pressureless sintering silver paste materials (A and B) were selected. As shown in Fig. 2(a), the two pressureless sintered silvers were processed using the same temperature curve for sintering, with a three-stage heating process. The initial stage involved preheating for approximately 20 minutes to remove organic solvents and volatile components. During the second stage, the temperature steadily increased to approximately 130°C, which promoted sintering neck growth and the initial densification of the nanosilver particles. Then, the temperature was increased to a peak of 200°C and maintained for a period of time to achieve structural rearrangement and densification of the material. After sintering, the same packaging process was used for chip interconnection, bonding, and packaging. The materials were then assembled into a QFN-packaged device with the same structure. Fig. 2(b) shows the front and back of the sample.

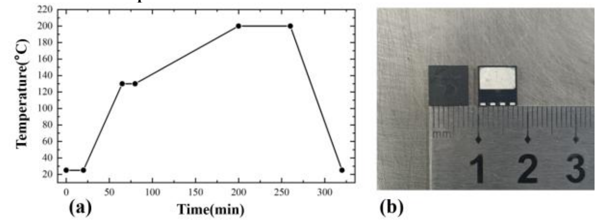

Fig. 2. (a) Sintering temperature curve (b) Front and back of QFN package sample.

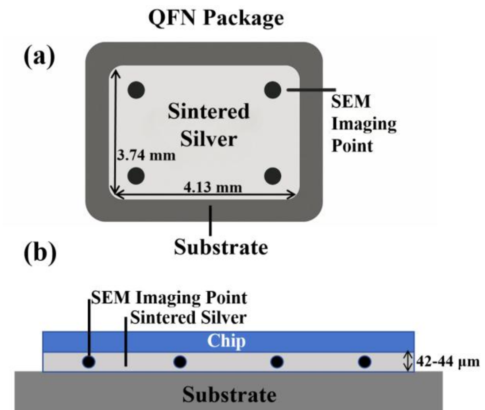

Fig. 3. SEM sections of sintered silver layer (a) horizontal (b) vertical.

To study the directional characteristics of the sintered silver microstructure, cross-sectional samples were prepared in the transverse and longitudinal directions for each material, forming four groups: A-horizontal (A-H), A-vertical (A-V), B-horizontal (B-H), and B-vertical (B-V). Each group contains three independently packaged samples. The samples were cut, mounted, and polished to expose the cross-sectional interface of the internal sintered silver layer. Four different areas were selected from each sample's sintered silver layer for scanning electron microscope (SEM) imaging. Fig. 3 shows the selected collection positions.

C. Porosity calculation method

An image processing program was written using MATLAB to quantitatively extract the pore structure from the SEM image. The program's processing flow includes converting the image to 8-bit grayscale, setting the threshold to 0.6, and binarizing the image. The pores are set to black and the pressureless sintered silver is set to white. Then, a median filter is applied to reduce noise. The calculation method for the binarization recognition result $B(x,y)$ is as follows:

$$B(x,y)=\begin{cases}0, & \text{if } I(x,y)<0.6\,(Porosity,\ Black)\\ 1, & \text{if } I(x,y)\geq 0.6\,(Sintered\ Silver,\ White)\end{cases} \quad (1)$$

To avoid interference from edge brightness in porosity calculations, 1% of the edge area of each image was excluded from analysis. Connected black areas in binary images were identified as pores, and their geometric parameters (e.g., area,

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equivalent diameter, eccentricity, direction, shape factor) were calculated using standard image analysis functions. The porosity of each image was calculated as the ratio of the pore area A_{pores} to the total image area A_{eff} . Pixel counts were converted to actual physical units (μm) based on the pixel size calibration value.

$$Porosity = \frac{A_{pores}}{A_{eff}} \times 100\% \quad (2)$$

III. MICROSTRUCTURE ANALYSIS

A. *Quantification of directional porosity*

A cross-sectional SEM image of each group with porosity closest to the group's average value was selected as a representative sample. The shooting magnification was 2K. The experimental SEM images and binarization results are shown in Fig. 4. Both pressureless sintered silver A and B show higher porosity in the vertical direction than in the horizontal direction. Unlike pressure-assisted sintering, the samples exhibit different porosities in the two directions because no external pressure is applied during sintering. Additionally, the pores of sample A are distributed in an ellipsoidal shape, while the pores of sample B are distributed in a lamellar shape. These differences in pore morphology lead to differences in the actual thermal properties of A and B.

Fig. 5 shows the statistical data of all scanning electron microscope (SEM) images of samples A and B in horizontal and vertical sections. The red marked points in the figure are the average values. For A, the porosity in the vertical and horizontal directions is 15.26% and 12.92%, respectively. The corresponding standard deviations are 5.10% and 4.51%, separately. For B, the porosity in the vertical and horizontal directions is 20.71% and 16.41%, respectively. The corresponding standard deviations are 1.86% and 3.96%, separately. These results show that the porosity of A and B is smaller in the horizontal direction than in the vertical direction. However, B shows a more significant porosity difference than A in both directions. Additionally, the pore distribution in the vertical direction is more uniform and stable. The vertical section of B has a highly porous structure, while its horizontal porosity is slightly lower and more volatile.

B. *Pore morphology evaluation*

In addition to porosity, this study evaluated other pore morphology parameters to determine microstructural anisotropy. Table 1 summarizes the key statistical values of the pore parameters in directions A and B. The mean diameter reflects the average pore size of the pores. The eccentricity reflects the degree to which the pore shape is elongated. The orientation of the pore main axis reflects the arrangement trend of the pore group in space. The compactness reflects the irregularity of the pore shape. Additionally, this study counted the number of pores in each image.

For A, the vertical direction shows larger average pore sizes, but fewer pores. This indicates stronger densification shrinkage during sintering, which merged the pores into a smaller number of higher-eccentricity, more compact pores. This points to a denser network of irregular, elongated pores in the vertical direction. While pore size remains consistent, the vertical section of B has a more interconnected and anisotropic pore structure than the horizontal section.

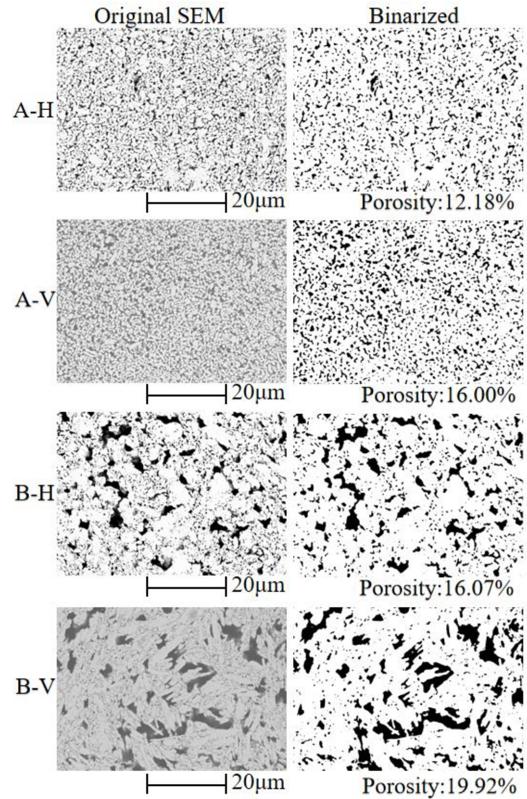

Fig. 4. Sample A and B's horizontal cross sections (left) and corresponding binarized images (right)

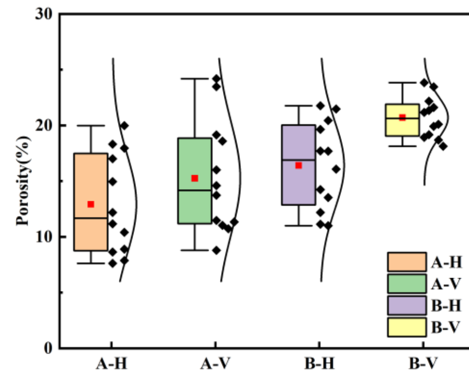

Fig. 5. A and B Porosity statistics in horizontal and vertical sections.

TABLE I. Morphological parameters of sintered silver samples

Parameters	A-H	A-V	B-H	B-V
Mean Diameter(μm)	0.341	0.462	0.367	0.376
Eccentricity	0.666	0.719	0.653	0.703
Orientation (°)	-8.08	-4.17	-5.48	-0.32
Compactness	1.95	1.63	2.10	2.19
Pore Count	3360	1481	2123	2219

These morphological observations suggest that vertical shrinkage during sintering influences the pore structure of both materials differently. Vertical shrinkage of material A causes pores to merge into fewer, larger voids vertically, while vertical shrinkage of B results in a uniform, dense pore

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network with irregular pore shapes in the vertical cross-section. Overall, both materials' microstructures are anisotropic in the horizontal and vertical directions. The surface-pressureless sintering of the silver paste exhibits directionality in pore formation during sintering. This anisotropic microstructure is expected to affect the heat conduction path within the material and must be considered in the subsequent thermal model.

IV. ANISOTROPIC THERMAL MODELING

A. Finite Element simulation setup

Finite element simulations were performed using COMSOL to quantitatively evaluate the effect of the observed microstructural anisotropy on thermal conduction. A two-dimensional model of the sintered silver layer was constructed using the above SEM binary images. The binary images of the selected samples were imported into COMSOL as a geometric model with a calibrated pixel ratio. The pores were filled with air, which acted as insulation. This model accurately captured the actual pore morphology and distribution of the cross-sectional sample. Table 2 lists the main simulation parameters and material properties used in the finite element model.

The two-dimensional model's boundary conditions were set to create a 1 K temperature difference in the sample's horizontal or vertical direction: the left boundary temperature was set to 300 K, the right boundary temperature to 299 K, and the other boundaries to adiabatic. A steady-state solution was used, considering only heat conduction and not convection or radiation, until the solution converged and the heat flow results stabilized.

B. Effective thermal conductivity results

The effective thermal conductivity k_{eff} of each sample orientation is calculated by the total heat flux obtained by simulation and the set temperature gradient. The effective thermal conductivity of A in the horizontal direction k_{eff_H} is 270.8 W.m^{-1}.K^{-1}; in the vertical direction k_{eff_V} is 247.4 W.m^{-1}.K^{-1}. The thermal conductivity ratio k_{eff_H} / k_{eff_V} is 1.095, indicating that the thermal conductivity along the horizontal direction is about 9.5% higher than that in the thickness direction. The horizontal direction k_{eff_H} of B is 228.5 W.m^{-1}.K^{-1}; k_{eff_V} is 203.9 W.m^{-1}.K^{-1}. The ratio k_{eff_H} / k_{eff_V} is 1.12, that is, the thermal conductivity in the horizontal is about 12% higher than that in the vertical direction. Consistent with the experimentally observed porosity differences, the results show a clear anisotropic trend.

The experimental results show that higher vertical porosity leads to a decrease in the thermal conductivity of the two materials in the vertical direction relative to the plane of the chip interconnect layer. The smaller porosity difference in the two directions for A than for B further emphasizes the importance of considering directional thermal properties in sintered silver layers. Assuming isotropy may overestimate the vertical heat dissipation capacity of these materials.

In actual QFN packages, heat diffuses horizontally and vertically. Thus, the thermal conductivity in these two directions can be combined to approximate the effective thermal conductivity of the sintered layer as a whole. We use a simple geometric mean model to estimate the overall effective thermal conductivity k_{avg} of each material [7]:

TABLE II. Key simulation parameters and material properties for thermal conductivity modeling.

Parameter	Value	Description
Domain size	lx × ly (μm)	Representative Volume Element
Matrix thermal conductivity (k_1)	429 W.m^{-1}.K^{-1}	Sintered Silver
Pore phase thermal conductivity (k_2)	0.001 W.m^{-1}.K^{-1}	Approximated Void
Boundary condition (T_{high})	300 K	Left Boundary
Boundary condition (T_{low})	299 K	Right Boundary

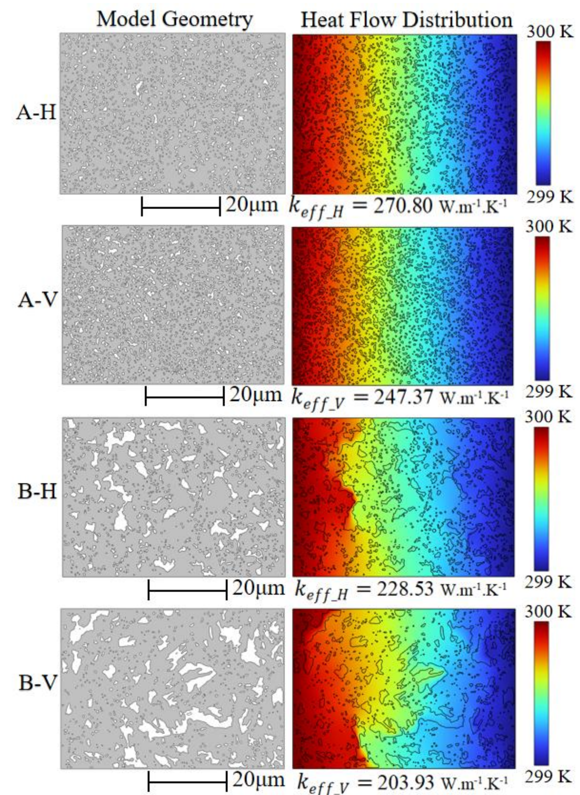

Fig. 6. Representative Model Geometry and Temperature Distribution

$$k_{avg} = \sqrt{k_{eff_H} \cdot k_{eff_V}} \quad (3)$$

This geometric mean model reflects the combined limiting effects of the heat transfer paths in both the plane and thickness directions of the chip interconnect layer. Considering the strong in-plane heat conduction that supports vertical heat dissipation brings this model closer to the overall thermal performance of the packaging layer than using only thermal conductivity in one direction. Furthermore, using the empirical formula of thermal conductivity to thermal resistance suggests that thermal conductivity and thermal resistance are inversely proportional when the process parameters are consistent. A transient thermal resistance test will be performed below to verify the accuracy of this evaluation model.

$$R_{th} \propto \frac{1}{k_{avg}} \quad (4)$$

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TABLE III. Thermal conductivity calculation results

Samples	k_{eff_H} ($W.m^{-1}.K^{-1}$)	k_{eff_V} ($W.m^{-1}.K^{-1}$)	k_{avg} ($W.m^{-1}.K^{-1}$)
A	270.8	247.4	258.8
B	228.5	203.9	215.9

V. EXPERIMENTAL THERMAL RESISTANCE VALIDATION

The difference in thermal conductivity between two pressureless sintered silver materials (A and B) in QFN packaging can be verified through transient thermal resistance measurements. The transient thermal impedance test is the most widely adopted method for analyzing the thermal characteristics of semiconductor device packaging. It provides detailed thermal performance data under various operating conditions. In this study, maintaining identical processing parameters and testing conditions for the QFN-packaged samples allowed the observed disparities in thermal characteristics to be attributed solely to the differences between the pressureless sintered silver materials. The transient thermal impedance testing conducted in this study comprises two principal components: (1) Verification of thermal resistance differences between materials A and B through dual-interface method measurement of junction-to-PCB thermal resistance (R_{th}); (2) Analysis of local thermal resistance function (local R_{th}) to validate the accuracy of the derived thermal conductivity model.

A. Dual-interface transient thermal resistance test

The dual-interface method for measuring R_{th} was conducted using SimuCAD Simcenter POWERTESTER 2400A, which is equipped with a tester and cooling plate. To facilitate testing, a PCB fixture was employed to establish interface connections for the QFN package pins. The definition of junction-to-PCB thermal resistance is as follows:

$$R_{\mathrm{th}}=\frac{T_J(t)\text{-}T_J(0)}{P_H} \tag{5}$$

where $T_J(t)$ represents the junction temperature at t , and $T_J(0)$ denotes the initial junction temperature, with P_H being the constant heating power. The dual-interface method determines total thermal resistance under steady-state conditions through two configurations of the interface: direct contact between the PCB fixture and cooling plate ("Dry ") and contact after applying thermal interface material ("TIM"). The specific junction-to-PCB thermal resistance is determined by identifying the separation point on the junction-to-PCB thermal resistance curve.

Calculating the junction temperature accurately requires calibrating the temperature-sensitive coefficient (K coefficient) corresponding to the voltage at specific temperatures. In this study, device channel heating was implemented to calibrate the K coefficient during the heating process. Junction temperatures were calculated from voltage measurements using the calibrated K coefficient. The calculation formula is expressed as follows:

$$\mathrm{T_J}(\mathrm{t})=\frac{V_{\mathrm{SD}}(t)\text{-}V_{\mathrm{SD}}(0)}{\mathrm{K}}+\mathrm{T_J}(0) \tag{6}$$

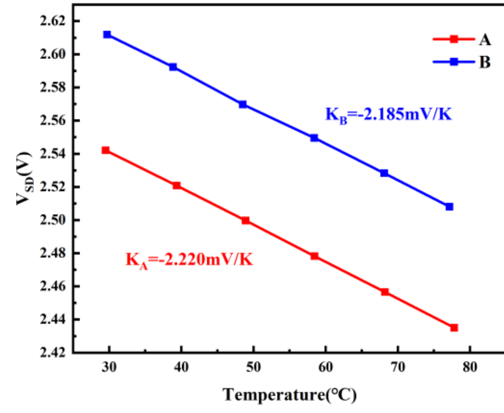

Fig. 7. Calibration of K coefficients for samples A and B.

Where $V_{\mathrm{SD}}(t)$ represents Source-Drain voltage of SiC MOSFET at t , $V_{\mathrm{SD}}(0)$ represents Source-Drain voltage at initial junction temperature. The K coefficient was determined through numerical fitting as illustrated in Fig. 7.

This study employed a heating test current of 10 A with a heating duration of 120 s and cooling period of 140 s, while maintaining the cooling plate temperature at 25 °C. Uniform clamping force was applied to ensure consistent contact between the device and cooling plate. The cumulative structure function results of R_{th} measured via the dual-interface method are presented in Fig. 8(a) and (b). Under controlled experimental conditions, the pressureless sintered silver samples A and B indeed induced distinct overall thermal resistance differences in QFN packaging.

As the heat source, the chip conducts thermal energy along a one-dimensional path through a series-connected thermal resistance-capacitance network comprising the chip, die attach, package, and cooling plate, as depicted in Fig. 8(d). The combined effects of the thermal and capacitance networks account for variations in the transient response curves. Further verification is required to quantify the thermal resistance differences between materials A and B at the die attach layer and elucidate their impact on the package's overall thermal resistance.

The differential structure function, which is derived from the integral structure function, reveals successive peaks that correspond to distinct structural layers. Interface positions between two materials are located between each peak and its adjacent trough. To mitigate errors induced by thermal interface materials, this study analyzed the differential structure functions of materials A and B under direct cooling plate contact configurations. As shown in Fig. 8(c), material A exhibits lower interfacial thermal resistance than material B between the chip and die-attach layer due to variations in porosity. These results conclusively demonstrate that differences in pore distribution directly influence interfacial thermal resistance and, consequently, overall package thermal resistance.

B. Analysis of local thermal resistance function

The thermal resistance values of A and B in the die-attach layer are critical to validating the accuracy of the thermal conductivity calculation model. This study used local structure functions to characterize the instantaneous thermal resistance from the chip heat source to specific cumulative thermal capacitance positions across layered structures. The

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peak positions in these functions correspond to the thermal resistance values in the die-attach layer. This reveals a difference of approximately 0.1 K/W in thermal resistance between A and B, as illustrated in Fig. 9. This result is consistent with the thermal conductivity model derived using anisotropic porosity parameters, confirming the validity of the methodology that calculates thermal resistance through porosity-dependent thermal conductivity derivation.

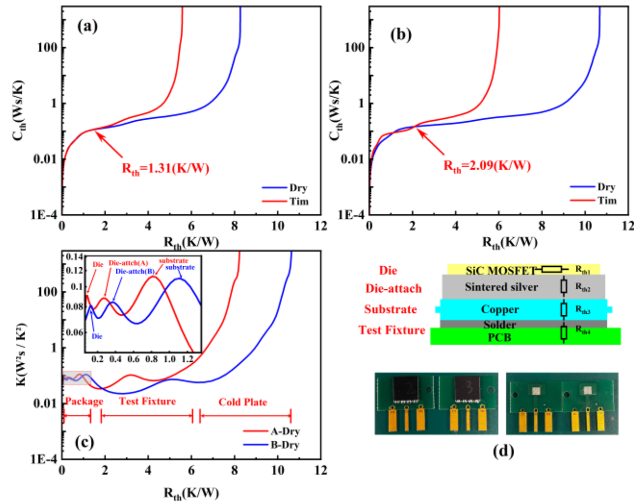

Fig. 8. Thermal resistance integral structure function of two samples. (a) sample A. (b) sample B. (c) thermal resistance differential structure function of two samples. (d) sample structure and QFN package.

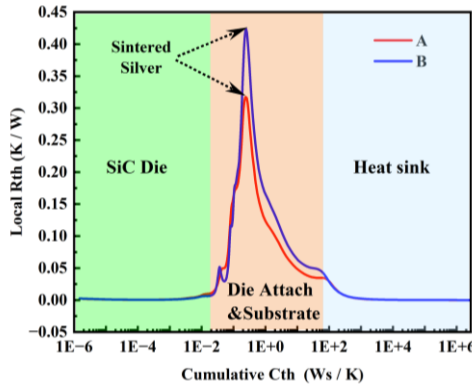

Fig. 9. The local thermal resistance functions of A and B

VI. Conclusion

This study systematically analyzed the effect of the microstructural anisotropy of two types of pressureless sintered silver in QFN packaging on thermal performance. By performing SEM characterization on the transverse and longitudinal sections and simulating the anisotropy of porosity with finite element technology, significant directional differences in porosity were revealed. The results show that the thermal conductivity is generally higher in the horizontal direction than in the vertical direction, which is consistent with the transient thermal resistance test results of the actual device, verifying the accuracy of the model. At the same time, the study found that differences in pore morphology also play an important role in regulating the heat conduction path. This study established an analytical framework for predicting thermal resistance performance based on the microscopic pore structure, which provides effective support for the selection and thermal design of high-power and high-temperature packaging materials.

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