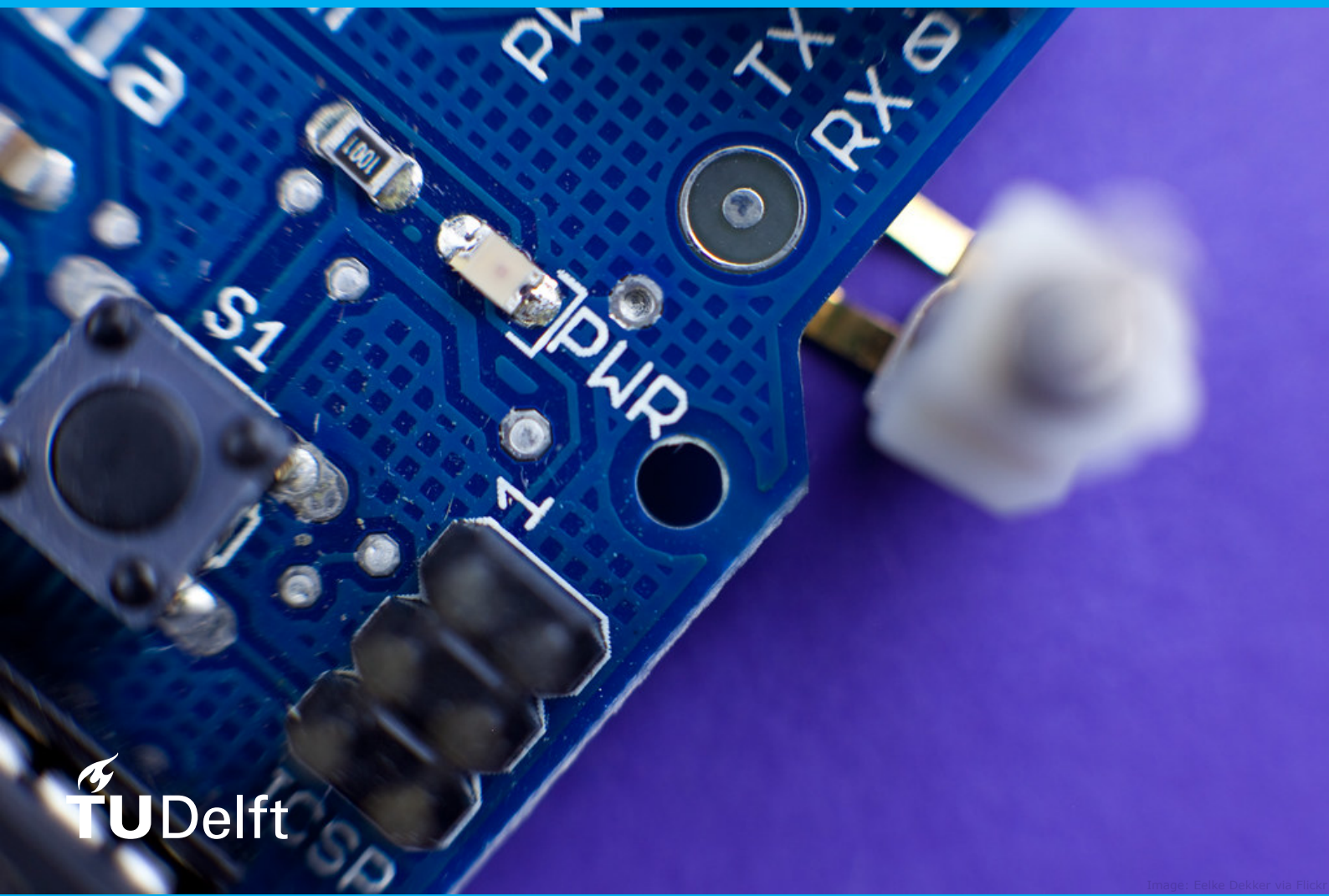
High frequency LLC resonant converter

Design and prototyping

Sagar Patel



TU Delft

Image: Eelke Dekker via Flickr

High frequency LLC resonant converter

Design and prototyping

by

Sagar Patel

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Friday September 20, 2019 at 10:00 AM.

Student number:	4747992	
Project duration:	November 21, 2018 – September 20, 2019	
Thesis committee:	Prof. dr. ir. P. Bauer,	TU Delft, supervisor
	Dr. ir. Z. Qin,	TU Delft, supervisor
	Dr. M. Cvetkovic,	TU Delft
	Ir. P. Degen,	NXP Semiconductors, supervisor

TU Delft

Preface

The purpose of this research is to design and prototype an LLC resonant converter operating at 500kHz. LLC resonant converters are becoming popular as power supplies for consumer electronics devices. There is always a push for reducing the size of power supplies. One of the way is going at higher switching frequencies. Theoretically higher switching frequency allows for smaller size of passive components such as capacitor and inductor. During this research by designing LLC converter at 500kHz various limitations of higher frequency operation is identified and volume reduction is compared with existing 87kHz design.

I would like thank my company supervisor from NXP Semiconductors, Peter Degen and my university supervisor Dr Zian Qin for their constant guidance and valuable insights throughout the course of this research. I would also like to thank Arjan van den Berg, Arjan Strijker,Frank van Rens,Ferdinand Sluijs and Jack Peeters from NXP semiconductors for their help during various stages of this research. I am also grateful to Prof Pavol Bauer and Dr Milos Cvetkovic for agreeing to be in my thesis committee.

This research would not have been possible without unconditional support from my parents. Their sacrifices throughout the life helped me reach here. My friends from Delft and Nijmegen also receive equal credit for being there for me throughout my masters.

Sagar Patel
Nijmegen, September 2019

Contents

List of Figures

List of Tables

1

Introduction

”Smaller is better” is the mantra of world of electronics. From a factory sized computers to laptops, from briefcase sized phones to smart phones miniaturization is everywhere. By going small, not only equipment becomes portable but the material cost and operating cost also reduces significantly. As a comparison, world’s first computer ENIAC was consuming 150kW of power whereas current top of the line processors consume about 60W while doing significantly more calculations. Power consumption of electronics devices reduced at such a level that it made poratable electronics feasible by incorporating a battery in it.

This portability lead to battery charging converters a must with the devices. The job of battery chargers is to convert AC power available from electricity grid to DC power level required for the device. Usually AC power is available at 120V/230V. The device requires DC power at 5-24V. Hence, apart from converting power from AC to DC, charger must also step down the voltage. For consumer devices other requirements also come into the picture for safety of consumer and better operating of grid.

One of the requirement is galvanic isolation of electronic device from electricity grid. This requirement is usually fulfilled by incorporating an isolation transformer. Transformer can also aid in step-down of voltage. Other requirement is having a near unity power factor when converter is rated for more than 75W. This necessitates a power factor correction stage in converter. Power factor correction can be done by using passive components only or with combination of active components along with passive components. Usually active power factor correction is preferred due to better correction and smaller size. The most used active power factor correction is using a boost converter.

As a result of using boost converter for power factor correction, output voltage is boosted to a higher level. A second converter(DC-DC) is necessary to bring down the higher DC voltage to consumer

device level DC voltage. This second converter can also incorporate galvanic isolation in it as using the galvanic isolation on supply side can lead to huge size of transformer due to lower frequency(i.e. 50/60Hz). Whereas power electronic converters usually operate in range of kHz which reduces size of transformer significantly.

As transformers can't work with constant DC voltage, converter has to create a pulsating DC which can be used by transformer. Converters achieve this by switching the voltage across transformer from power factor correction stage output voltage and ground rapidly. Semiconductor switches such as MOSFET and IGBT are used in the application. But this size reduction comes at a price of additional losses in semiconductor switches because of energy lost during switching ON and OFF and also while conducting. Efforts are always made to reduce these losses.

One of the DC-DC converter which is used in power supplies upto 300W is forward converter. Forward converter is relatively simple and easy to control. But it has higher switching losses and higher magnetic losses. Higher magnetic losses are due to presence of higher frequency components in magnetic flux inside the core as a result of square wave voltage across transformer.

To overcome the problems forward converter, resonant DC-DC converter are more and more being used. Resonant converters work on the principle of electrical resonance between inductor and capacitor. Some of the advantages of the resonant converters is lower losses in magnetic core as only fundamental frequency component is present in magnetic flux and possibility of reducing switching losses by making use of zero voltage switching.

Research Question

Current resonant converters work in the frequency range of 50-100kHz. The goal of the project is to push the operating frequency of resonant converter to 500kHz while utilizing NXP semiconductors resonant platform TEA2016. The LLC resonant converter has to be designed and hardware implemented to find out the limitations associated with higher frequency operation. As in the previous case when transformer has been moved from 50Hz to 50-100kHz range its size reduced significantly. It needs to be verified if this still holds true when going to 500kHz.

Chapter 2 gives in detail working of the resonant converter. It also gives explanation about why a particular topology is chosen.

Chapter 3 is about working of NXP semiconductors's resoanat platform IC TEA2016, its various features and how the features are used in control of the converter.

Chapter 4 discusses design of LLC resonant converter. In the design various parameters are chosen and how they affect the operation of converter is discussed. Further, design of integrated magnetic component is also discussed.

In chapter 5, converter is implemented on hardware as per design in chapter 4.

Chapter 6 discusses the results obtained from hardware implementation. This chapter discusses various problems that are found during operation of higher frequency is discussed and solutions to the problems are given.

2

Working of LLC converter

2.1. Introduction

Aim of this project is to investigate operation of LLC resonant converter at high frequency. In this chapter basics of LLC resonant converter is discussed.

2.2. Electrical resonance

The world of electrical engineering comprises of 3 basic passive elements: Resistance (R), Inductance (L) and Capacitance (C). Each of these elements have their impedances (Z) and admittances (Y). For a given angular frequency(ω), impedance and admittance of these passive elements is shown in table 2.1.

	Resistance (R)	Inductance (L)	Capacitance (C)
Impedance (Z)	R	$j\omega L$	$\frac{1}{j\omega C}$
Admittance (Y)	$\frac{1}{R}$	$\frac{1}{j\omega L}$	$j\omega C$

Table 2.1: Impedances and admittances

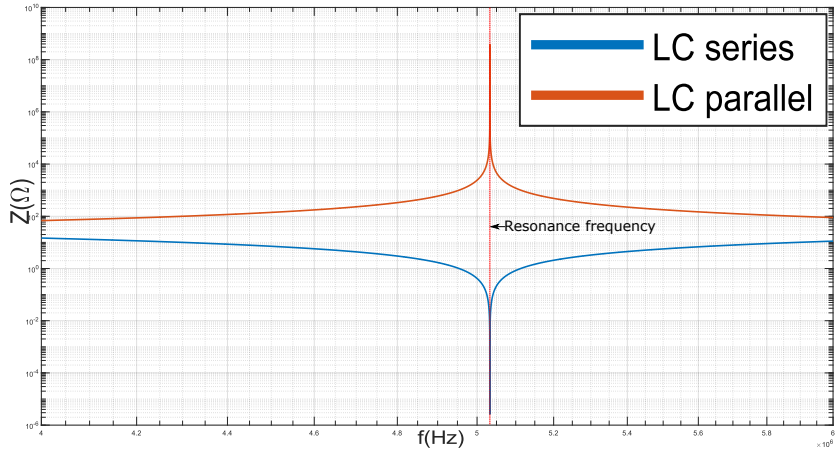


Figure 2.1: Series and parallel impedance of LC circuit

Figure 2.1 shows impedance of series and parallel connection of inductor and capacitor. At a particular frequency, series impedance of the combination is minimum and parallel impedance is maximum. This frequency is called resonance frequency. Combination of more than 2 can result in multiple resonance frequencies. This property is utilized in multiple applications for filtering of signals by providing

higher/lower impedances at all frequencies apart from resonance frequency. At resonance, energy required to set up magnetic field in inductor and energy required to set up electric field in capacitor resonates between each other. This property, if utilized in power conversion application, it can result in higher efficiency of the converter as losses associated with set-up of the fields is reduced.

2.3. Resonant converters

Converters which utilize the electrical resonance property for power conversion are called resonant converters. Most of the resonant converters are made with resonant inverter and rectifier. Resonant

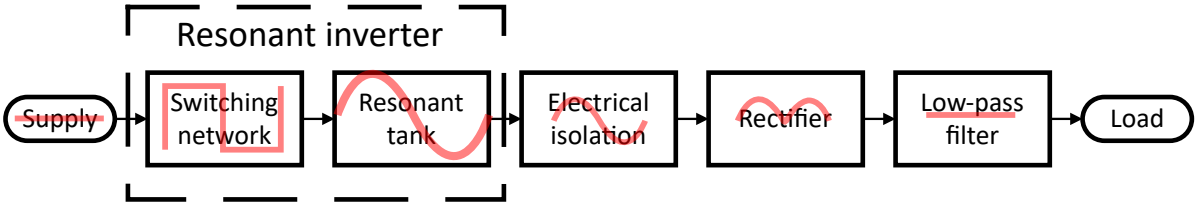


Figure 2.2: Resonant converter [4]

inverter converts DC input into a sinusoidal voltage and rectifier converts sinusoidal voltage into DC which is then filtered to give pure DC. Often due to safety concerns an electrical isolation block is added. This electrical isolation is provided by a transformer which can also step up/down the voltage apart from isolation if required. Figure 2.2 shows the block diagram of resonant converter along with output waveform of each block. In the following sections the options available for different blocks is described and why a particular block is chosen for the given requirements.

2.3.1. Switching network

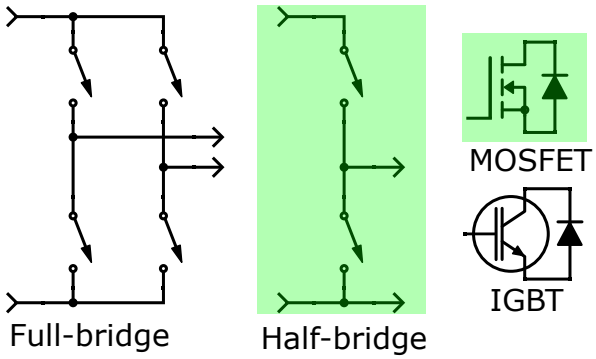


Figure 2.3: Choice for switching network and switch

Figure 2.3 shows the options for switching network for a resonant converter and switch that can be used in the network. As seen from the figure 2.3, half bridge has only 2 switches compared to 4 switches of full bridge. But this saving on switches comes at cost of efficiency as current in half bridge is double of current through full bridge. So, conduction losses in half bridge will be 4 times losses in full bridge. In applications which has higher primary current, using a full bridge is recommended [1]. In application considered here, primary current is not high so saving on cost of 2 switches will be considerably higher than liability due to higher conduction losses.

For the given application switching operation will be at 500kHz and higher. As per [5] MOSFET is the only choice out of MOSFET and IGBT as operating frequency of IGBT ends at around 80kHz.

Choice: MOSFET half-bridge

2.3.2. Resonant tank

Resonant tank can have many forms. Two most basic ones are series resonance and parallel resonance tank. As per [8], series resonance and parallel resonance suffers from high turn off current

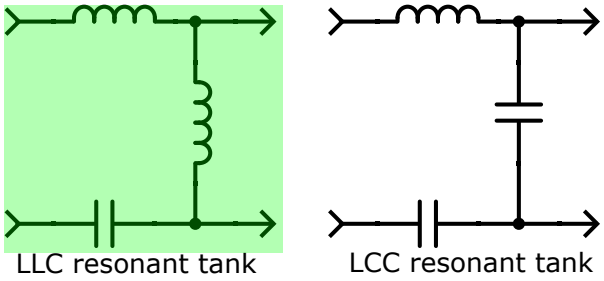


Figure 2.4: Choice for resonant tank

at high input voltage condition , high circulating energy and light load regulation. This makes them unsuitable for front-end power converter applications.

The solution to above problem is series parallel resonance tank. It combines properties of series resonance and parallel resonance. Series parallel resonance tank consists of 3 elements: 1/2 capacitor(s) and 2/1 inductor(s). Load is in series with resonance tank formed by 1 inductor and capacitor and in parallel with remaining capacitor or inductor. Figure 2.4 shows the two possibilities named according to the elements used in the tank, LLC and LCC.

For achieving higher efficiency it is preferable to operate at highest resonant frequency. LCC operates a frequency farther than resonance frequency at higher input voltages. and its lower resonance frequency is in zero current switching region whereas operation in zero voltage switching area is desirable for the given application. LLC gives zero voltage switching operation at all loading conditions and can be designed to be operated at resonance frequency even at higher input voltages [8]. This makes LLC the chosen one for resonance tank.

Choice: LLC resonant tank

2.3.3. Electrical isolation

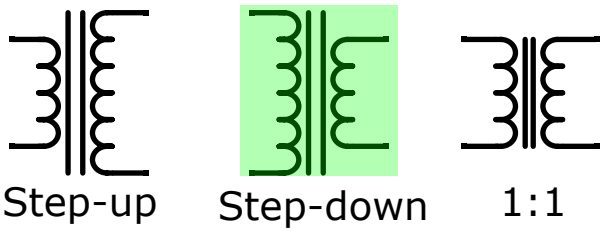


Figure 2.5: Choice for transformer

Electrical isolation is provided by a transformer. Based on application it can also provide step-up/step-down operation apart from isolation. If no voltage level change is required 1:1 transformer can be used to just provide isolation. In the given application, output voltage is lower than input voltage. Step-down transformer aides in this conversion.

Choice: Step-down transformer

2.3.4. Rectifier

Figure 2.6 shows options for secondary side rectification.
Advantages of full-wave rectifier:

- Only 2 diodes
- Conduction losses are half compared to full bridge due to less number of diodes.

Advantages of full-bridge rectifier:

- Secondary winding copper losses are half compared to full-wave.
- Lower voltage rating of diode.

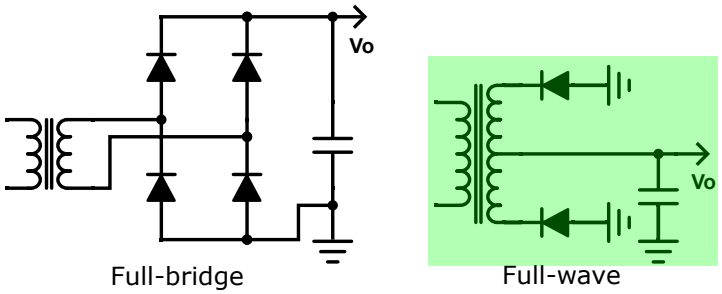


Figure 2.6: Choice for secondary side rectification

Full-bridge rectification is advantageous in applications with high output voltage due to savings on lower voltage rating diodes. Full-wave rectification is advantageous in application with lower output voltages and higher current due to lower total losses and savings on count of components. For the given application, full-wave rectification is used as application has high output current and low output voltage.

Choice: Full-wave

2.4. LLC converter

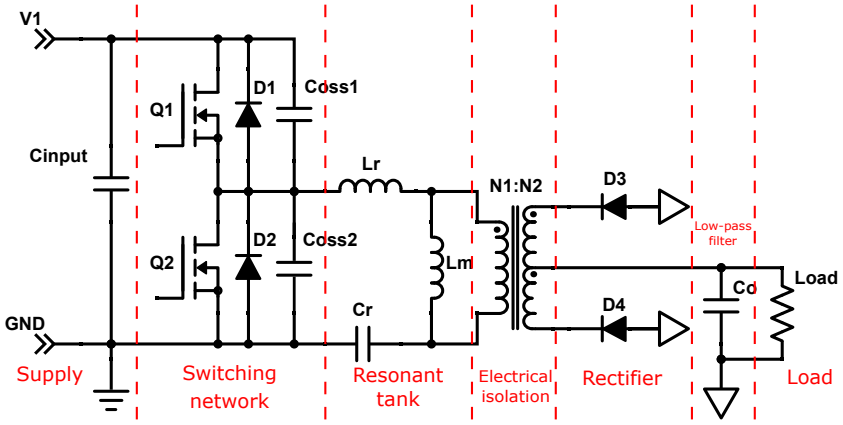


Figure 2.7: Complete circuit diagram of LLC resonant converter

Based on all the choices made in previous section, a complete resonant converter is implemented as shown in figure 2.7. In figure 2.7, Coss1 and Coss2 are output capacitances of the respective MOSFETs. In the upcoming sections, working of LLC converter depicted in figure 2.7 is explained.

Terminology

- HS: Gate voltage of high side MOSFET Q_1.
- LS: Gate voltage of high side MOSFET Q_2.
- V_{HB}: Voltage of the mid-point of MOSFET half-bridge. This would also be Drain to Source voltage of Q_2 and voltage across the resonant tank.
- I_{D_3}: Current through secondary side diode D_3.
- I_{D_4}: Current through secondary side diode D_4.

Energy taking phase

Figure 2.8 shows energy taking phase of LLC resonant converter. In this phase, half of the energy taken from input is delivered to secondary side and other half is used to charge resonant tank. In the half bridge, Q_1 conducts and on the secondary side D_4 conducts.

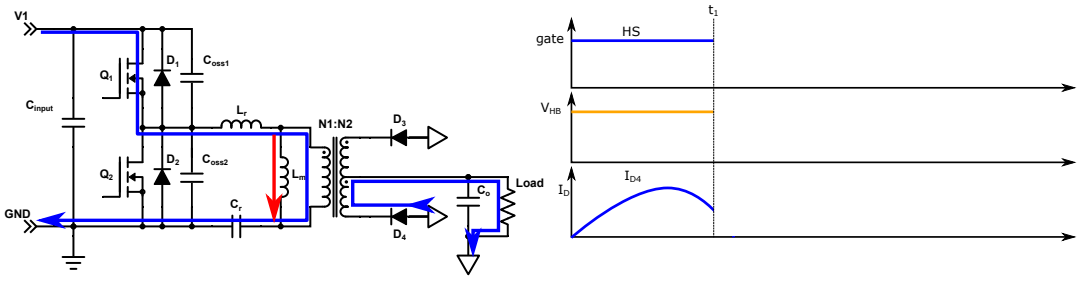


Figure 2.8: Energy taking phase

Zero voltage switching transition from Q_1 to Q_2

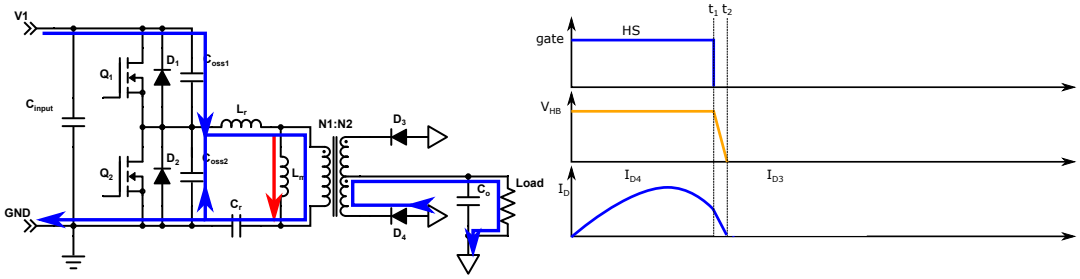


Figure 2.9: Zero voltage switching transition from Q_1 to Q_2

At start of this phase, gate signal to Q_1, HS is removed. This turn-OFF causes turn-OFF losses in the MOSFET. Current flowing through L_m, I_{L_m} discharges C_{oss2} and charges C_{oss1}. At the end of this phase, C_{oss2} is completely discharged and C_{oss1} is completely charged.This causes half bridge voltage V_{HB} to become 0. So, voltage across Q_2 is 0 now and when it turns ON there won't be any turn-ON losses. During this process, current in diode D_4 also becomes zero and it stops conducting. There will not be any reverse recovery losses in diode D_4 as it turns-OFF naturally due to current becoming zero.

MOSFET diode conduction

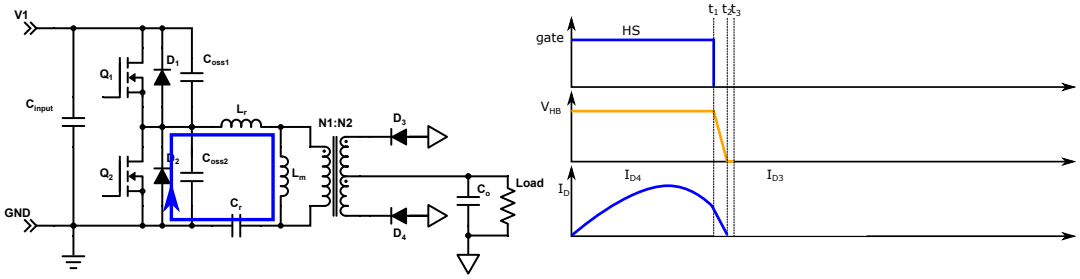


Figure 2.10: MOSFET diode conduction

Figure 2.10 shows this phase. Energy stored in magnetizing inductance freewheels through body diode of Q_2 (D_2) as gate signal to Q_2 (LS) is not applied yet.

Reverse conduction of Q_2

This phase is similar to synchronous rectification. Gate signal is applied to Q_2. But due to direction of current in resonant tank MOSFET conducts from source to drain. Working of this phase is depicted in figure 2.11.

Energy delivery phase

At the start of this phase , resonant tank current reverses its direction. Current starts flowing from drain to source in Q_2. The stored energy in resonant tank during energy taking phase is delivered to

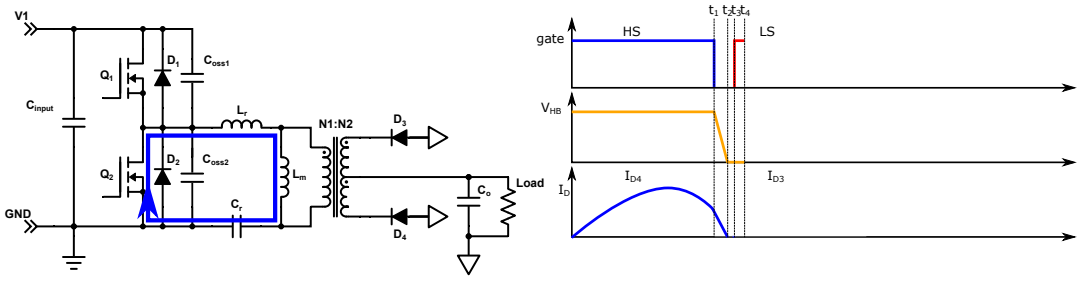


Figure 2.11: Reverse conduction of Q_2

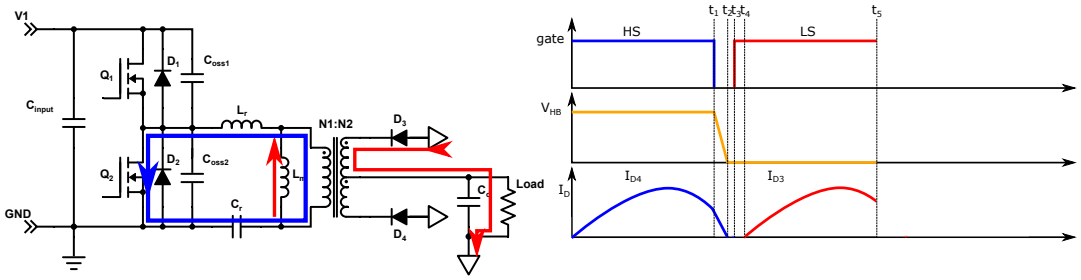


Figure 2.12: Energy delivery phase

secondary side in this phase. On the secondary side, diode D_3 starts conducting.

Zero voltage switching transition from Q_2 to Q_1

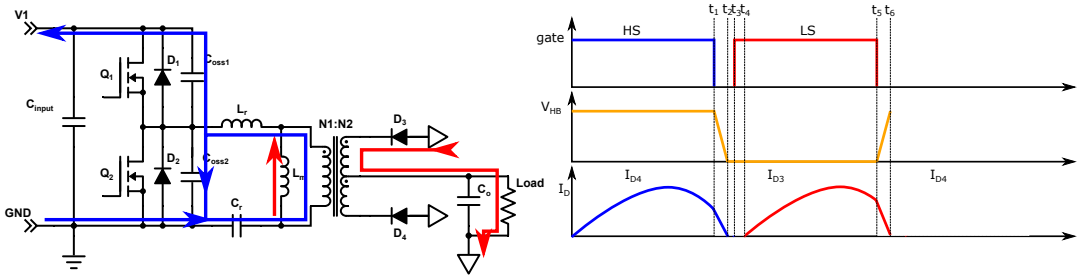


Figure 2.13: Zero voltage switching transition from Q_2 to Q_1

At the start of this phase, gate signal to Q_2 (LS) is turned OFF. Magnetizing inductance current I_{L_m} starts discharging C_{oss1} and charging C_{oss2}. At the end of the phase, this process is completed and half bridge voltage (V_{HB}) reaches input voltage value. Hence, voltage across Q_1 is 0 now and when it turns ON there won't be any turn-ON losses. On the secondary side, current through diode D_3 becomes zero during this process. Similar to Q_1 to Q_2 transition, there will not be any reverse recovery losses in this transition.

MOSFET diode conduction

Similar to Q_1 to Q_2 transition, after half bridge voltage reaches input voltage value, current starts flowing through body diode of Q_1.

Reverse conduction of Q_1

This phase is synchronous rectification of diode D_1. At the start of the phase, Q_1 is turned ON and current flowing through D_1 transfers to Q_1. Which reduces conduction losses.

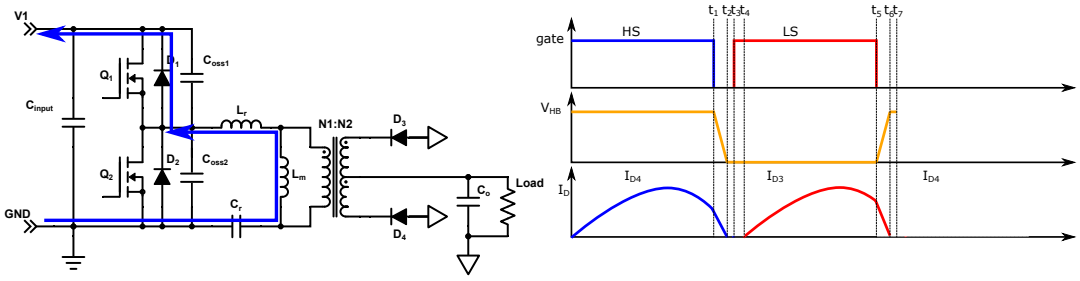


Figure 2.14: MOSFET diode conduction

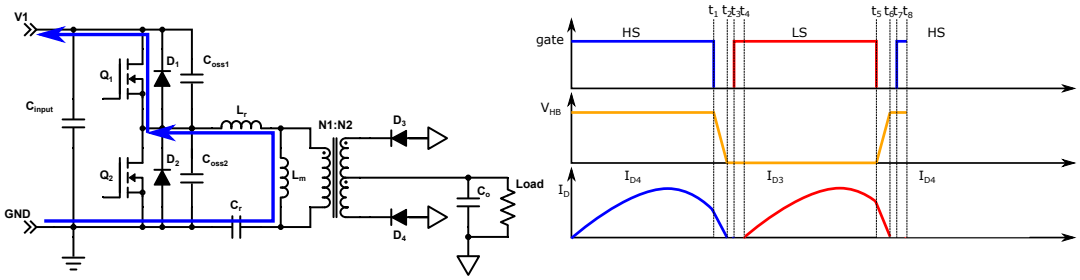


Figure 2.15: Reverse conduction of Q_1

Energy taking phase

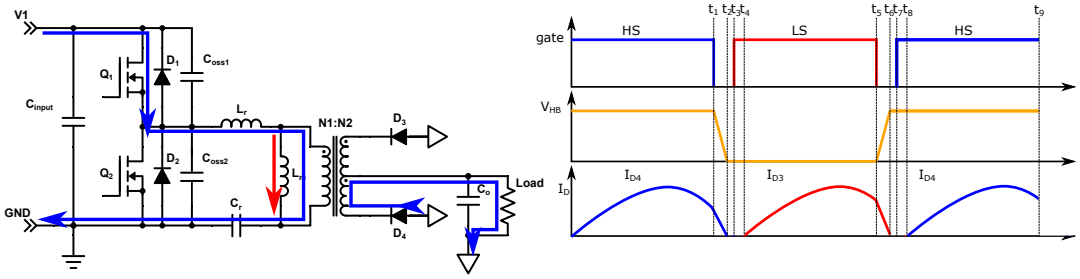


Figure 2.16: Energy taking phase

Figure 2.16 marks completion of one full switching cycle.

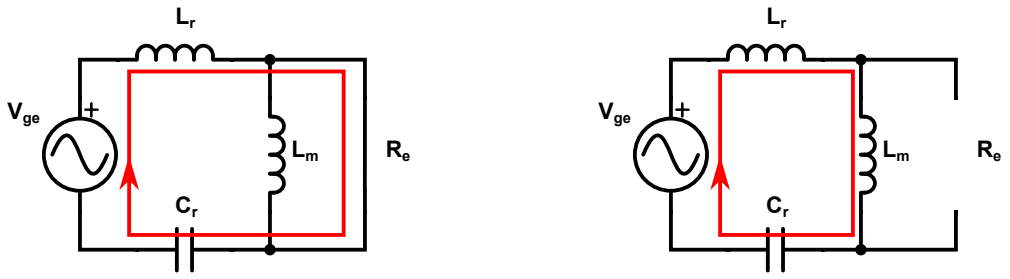
Every switching cycle has 2 resonance frequencies f_{r1} and f_{r2}. f_{r1} is the resonance frequency when only L_r and C_r are forming the resonant tank whereas f_{r2} is the resonance frequency when L_m also takes part in resonance. Equations 2.1 and 2.2 shows the dependence on various circuit parameters for f_{r1} and f_{r2} respectively.

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.1}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2.2}$$

The operation described previously is the operation when switching frequency $f_{sw} = f_{r1}$. During the phases when energy is being delivered to the output, L_m doesn't participate in resonance as load is in parallel to the L_m as seen in figure 2.17a. Hence, during energy taking phase and energy delivery phase the resonance frequency is f_{r1}.

During deadtime between gate signals, L_m starts participating in resonance as load is not in parallel of it anymore. So, during the deadtime L_m is also part of the resonance circuit as seen in figure 2.17b.



(a) Energy delivery to the load

(b) During dead time

Figure 2.17: Conduction path

During the deadtime, energy is not being delivered to the load but some energy is stored in L_m. This energy helps in discharging and charging MOSFET capacitance C_{oss}. In order to completely charge or discharge MOSFET capacitance C_{oss}, energy stored in L_m and L_r should be more than energy to be stored or removed from MOSFET capacitances C_{oss}. Equation 2.3 depicts this condition.

$$\frac{1}{2}(L_m + L_r) \times I_{m\_peak}^2 \geq \frac{1}{2}(2C_{oss}) \times V_{in}^2 \tag{2.3}$$

Apart from having sufficient energy in L_m, dead time also be long enough to facilitate the complete charging or discharging of C_{oss}. This will be achieved by satisfying conditions in equation 2.4.

$$t_{dead} \geq 16 \times C_{oss} \times f_{sw} \times L_m \tag{2.4}$$

When switching frequency f_{sw} is more than f_{r1}, resonant current I_{res} takes longer in the switching cycle to reach the value of I_m. Hence, secondary side diodes conduct for more duration in a cycle. But still, zero voltage switching is achieved and diode reverse recovery losses are avoided.

When switching frequency f_{sw} is less than f_{r1} that's when the real trouble starts. During lower switching frequency, resonant current I_{res} takes shorter duration in the switching cycle to reach the value of I_m. Hence, secondary side diodes conduct for lesser duration in a cycle. So, effectively deadtime is larger as long as secondary side is concerned. During this time, there is a chance that I_m will change its direction before next switch can be started. If it changes its direction, it starts charging/discharging previously discharged/charged MOSFET capacitance. This would mean loosing zero voltage switching when the gate signal is applied to next MOSFET. This operation is called capacitive mode operation and it should be avoided to gain higher efficiencies.

3

LLC controller TEA2016

For this project, controller IC TEA2016 from NXP semiconductors is used. TEA2016 is a digitally configurable combo controller for LLC and PFC converter for usage in resonant power supplies [7]. It contains gate driver and controller for both PFC and LLC in one single package. This project is aimed at operation of LLC converter and its control. So, for the purpose of this project PFC part of the controller IC is disabled digitally. Hence, TEA2016 for the purpose of this project works solely as a controller for LLC resonant converter. In this chapter a general overview of the TEA2016 is given along with its key features. Working a control strategy of TEA2016 is discussed in detail.

3.1. Features of TEA2016 [7]

- Several digitally programmable parameters
- Constant gain of the control loop
- 3 operating modes(Burst, Low Power, High Power)
- Independently configurable levels and timers
- All protections can independently be set to latched, safe restart, or latched after several attemps to restart
- Supply Under Voltage Protection (UVP)
- Over Power Protection (OPP)
- Internal and external Over Temperature Protection (OTP)
- Capacitive Mode Regulation (CMR)
- Accurate Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Inrush Current Protection (ICP)
- Brownin/Brownout protection
- Disable input

3.2. Pin description for LLC part [7]

In this section description of pins of TEA2016 utilised for LLC part is given. Pins utilised for PFC are not described as PFC part of the IC has been disabled.

1. **SNSMAINS**: To sense input voltage and external temperature.
2. **SNSBOOST**: To sense output voltage of PFC stage through a resistive divider.
3. **GATELS**: LLC half bridge low-side MOSFET gate driver and supply for bootstrap capacitor.
4. **GATEHS**: LLC half bridge high-side MOSFET gate driver.
5. **SUPHS**: high side driver supply input from bootstrap capacitor.
6. **HB**: To sense voltage of half bridge node of LLC half bridge for voltage slope detection and low level reference for high-side driver.
7. **SUPIC**: DC supply for the IC.
8. **SNSCAP**: To sense voltage across resonant capacitor through a capacitive and resistive voltage divider
9. **SNSCURLLC**: To measure current in resonant tank through sense resistor.
10. **SNSFB**: Output voltage regulation sense input.

3.3. Frequency control of LLC converter

One of the methods of controlling output power of LLC converters is switching frequency control of half bridge. Most of the LLC controllers available in market employ this strategy. In this section working of frequency control strategy is explained.

Figure 3.1 shows a typical control circuit for frequency control of LLC converter. Output voltage is measured through a voltage divider and compared with standard output voltage requirement using TL431. TL431 controls the flow of current through transmitter of opto-coupler. Current on transmitter side of opto-coupler is reflected on receiver side of opto-coupler. Receiver side is connected with a fixed supply voltage through a resistor. Voltage across receiver (V_{SNSFB}) is given to frequency controller. Frequency controller has an inverse relationship between V_{SNSFB} and switching frequency as shown in figure 3.1.

When load current decreases, output voltage of the converter rises above regulation level. This causes more current to flow through opto-coupler. More current through opto-coupler reduces V_{SNSFB}. As per the internal frequency curve, switching frequency of half bridge is increased which causes input power to be reduced. Reduced input power forces output voltage to return to regulation level.[7]

One of the disadvantage of this control methodology is variable gain of control loop. As operating frequency is variable throughout the operating region, gain of control loop is also different at different operating points. If care is not taken during design of converter it can become unstable. Another disadvantage of this control strategy is point where converter shifts from high power mode to burst mode. The point is entered at a frequency based on relation between output power and switching frequency. Here a small variation in resonant tank components can affect burst mode activation power level.

3.4. Resonant capacitor voltage(energy) control of LLC converter

A different control strategy is utilized by NXP in LLC controller TEA2016. Instead of controlling output power by controlling frequency, it is regulated by adjusting voltage across the resonant capacitor C_r. By regulating voltage across resonant capacitor, TEA2016 in turn regulates energy stored in resonant capacitor. As discussed in working of LLC converter, during energy taking phase half of the energy is stored in resonant tank which is delivered to the load during energy delivery phase. By allowing lower

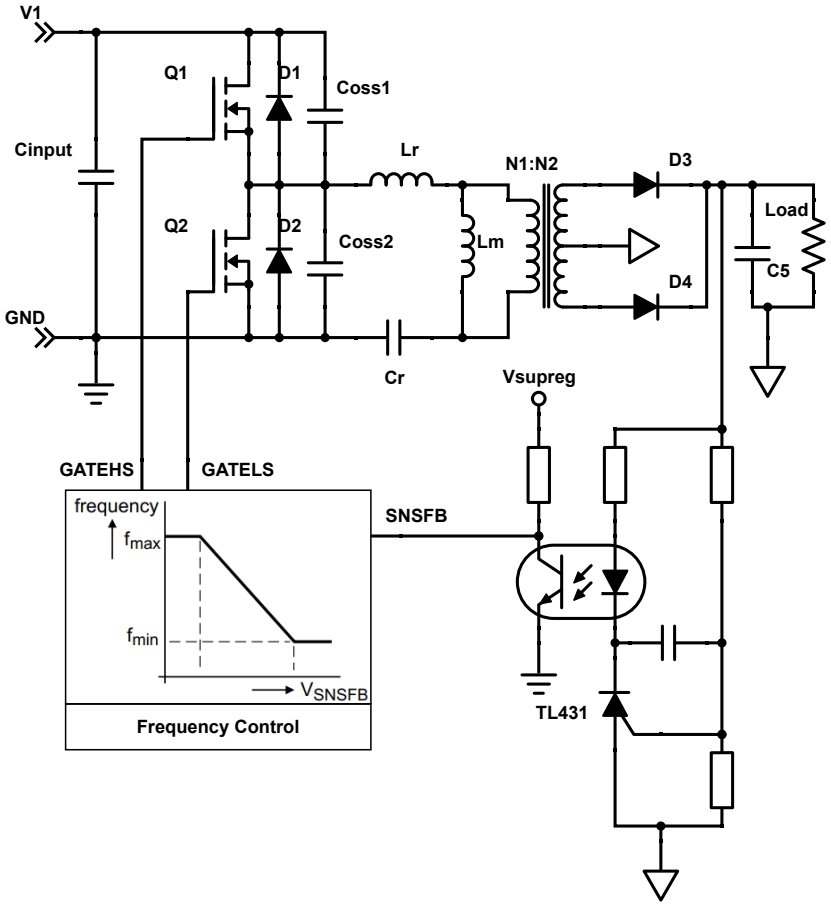


Figure 3.1: Frequency control of LLC converter

energy to be stored in resonant tank, lower energy is delivered to the load which means lower power is delivered to the load. In this way voltage across resonant capacitor can be directly linked with power being delivered. This relation is linear.

$$P_{in} = V_{in} * I_{in} = V_{in} * C_r \frac{dv}{dt} = V_{in} * C_r * \Delta V_{Cr} * f_{sw} \tag{3.1}$$

$$P_{in} \propto \Delta V_{Cr} \tag{3.2}$$

Equation 3.2 shows linear relationship between input power and voltage across resonant capacitor

Figure 3.3 shows the working of new control methodology. During energy taking phase,current shown by red line on primary side flows through resonant capacitor C_r and transformer. Half of the input energy is delivered to the load, capacitor C_r is charged with other half. As capacitor charges, V_{C_r} increases.

During energy delivery phase, energy stored in C_r is delivered to the load as indicated by blue line in figure 3.3. Since energy is being removed from C_r, its voltage decreases.

Figure 3.4 depicts power regulation loop used by TEA2016. Figure 3.4 shows the control circuit diagram whereas figure 3.6 gives the timing diagram of waveforms.

3.4.1. Resonant capacitor voltage (V_{C_r}) sensing

Resonant capacitor voltage (V_{C_r}) is sensed using a capacitive divider network which steps down the actual resonant capacitor voltage (V_{C_r}) to a voltage suitable for IC, V_{SNSCAP}. V_{SNSCAP} is biased at 2.5 V

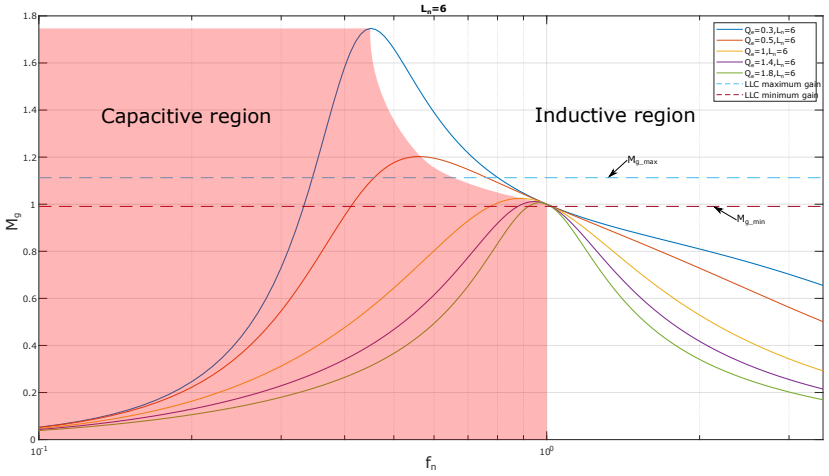


Figure 3.2: Gain plot of LLC converter

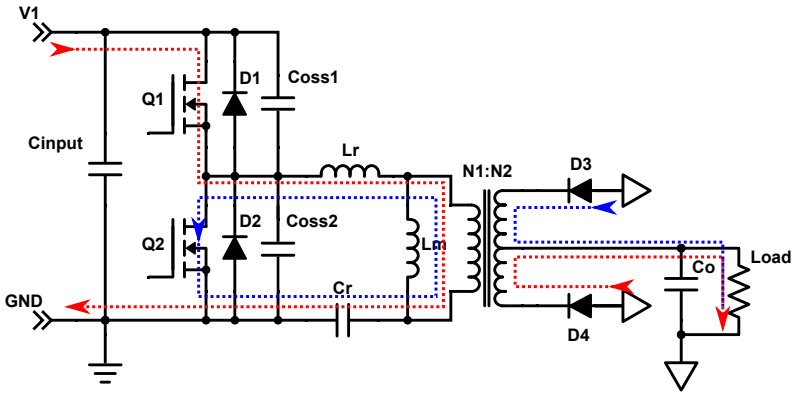


Figure 3.3: Operation of LLC converter

and this bias is ensured by internal current source and resistive divider network parallel to the capacitive divider network. The voltage across resonant capacitor(V_{C_r}) at maximum output power is scaled to 1-4V with 2.5V as the bias point. Figure 3.5 depicts the circuit for resonant capacitor voltage (V_{C_r}) sensing [6].

3.4.2. The switching sequence

1. Initial state: GATEHS is ON and Q_1 is conducting
2. t1: $V_{SNSCAP} > V_{hs(SNSCAP)}$ and GATEHS is turned OFF. Q_1 stops conducting.
3. After a short dead-time, GATELS is turned ON. Q_2 starts conducting. Dead-time can be adaptive or fixed.
4. t2: $V_{SNSCAP} < V_{ls(SNSCAP)}$ and GATELS is turned OFF. Q_2 stops conducting.
5. Again, after a short dead-time, GATEHS is turned ON.

Figure 3.6 depicts this switching sequence. In this control strategy, switching frequency f_{sw} is a outcome of switching , not a control parameter as in case of frequency control. Output power is also an outcome of the control strategy.

The difference between $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ is ΔV_{SNSCAP}. ΔV_{SNSCAP} is proportional to output power. ΔV_{SNSCAP} is decided by opto-coupler current I_{SNSFB} which is in turn dependent on TL431 based output voltage sensing circuit.

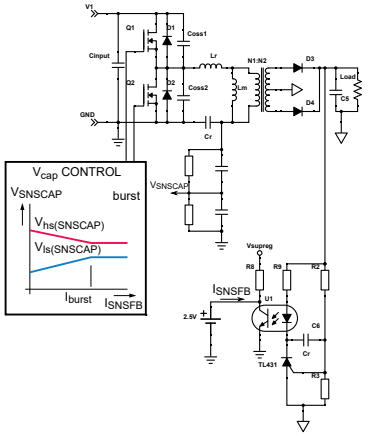


Figure 3.4: Capacitor voltage control [7]

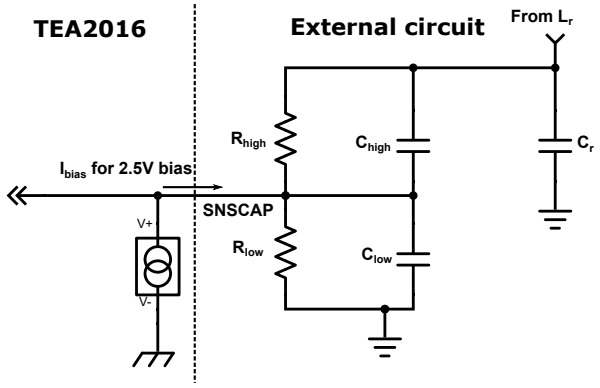


Figure 3.5: Resonant capacitor voltage (V_{C_r}) sensing circuit

Transient behaviour is also depicted in figure 3.6. If load current increases, output voltage goes down which causes opto-current I_{SNSFB} to also go down. In response to that, TEA2016 increases ΔV_{SNSCAP}. During one transient cycle, extra energy is stored in resonant capacitor (V_{C_r}) by keeping GATEHS ON for a longer time. Extra energy is also delivered to the output. This extra energy brings output voltage to normal level while delivering more load current.

Optocoupler current (I_{SNSFB}) is continuously regulated to 80 µA to reduce no-load power consumption of system.

Figure 3.6 also shows half bridge voltage(V_{HB}), resonant current (I_{res}) and magnetization current(I_m). As seen in the figure 3.6, when the load increases resonant current(I_{res}) also increases but magnetization current (I_m) stays same.

3.5. Feedback regulation

As discussed previously, output voltage is sensed with TL431 bsed circuit combined with optocoupler. Optocoupler is connected to SNSFB pin to deliver output voltage information to the TEA2016. The behaviour of TL431 causes more optocoupler current (I_{SNSFB}) when output power is minimum. Which causes more losses at no load. So, it is important to regulate the optocoupler current to a lower level independent of load, to reach maximum efficiency at low load[7].

As seen in figure 3.6, when load increase, initially optocurrent (I_{SNSFB}) decreases. In response to this transient, ΔV_{SNSCAP} is increased which increases output power.

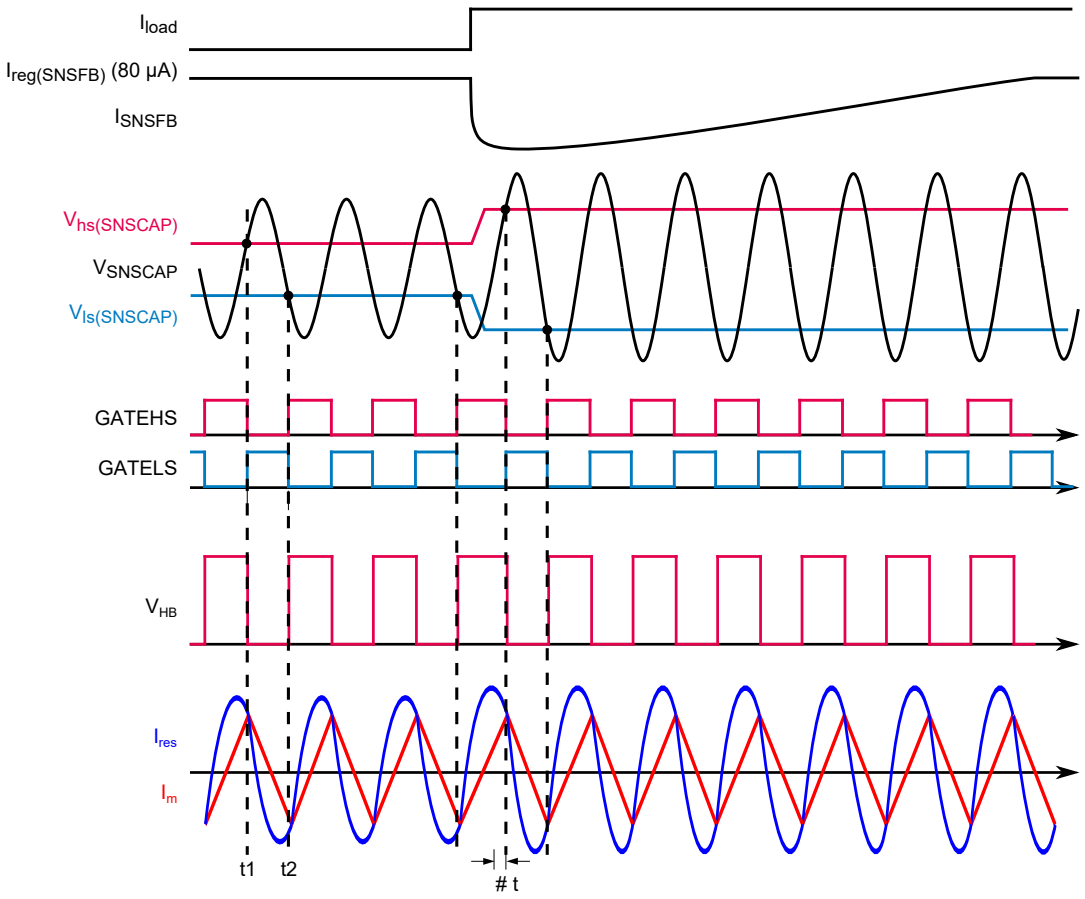


Figure 3.6: Control waveform

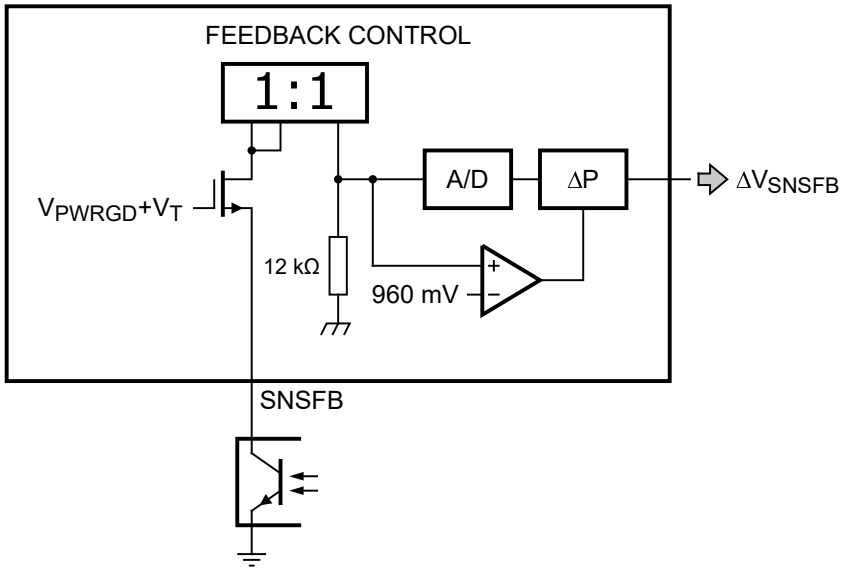


Figure 3.7: Feedback current control

Internally, when I_{SNSFB} is decreased voltage drop across 12kΩ below 960mV(80µA$\times$ 12kΩ) target level. From figure 3.7 it can be seen voltage drop across 12kΩ is compared to 960mV reference and when there is a difference it is given to ΔP block inside IC which gives out ΔV_{SNSFB}. During transient, TEA2016 slowly increases ΔP until optocurrent reaches 80µA. Similarly, when load is decreased, TEA2016 slowly decreases ΔP until optocurrent reaches 80µA. This way, TEA2016 continuously reg-

ulates I_{SNSFB} to regulation level [7].

When load is very low, feedback control won't be able to regulate I_{SNSFB} to 80µA level. When I_{SNSFB} hits 100µA level, burst mode is triggered. New burst cycle starts when I_{SNSFB} comes back to 100µA.

3.6. High power operating mode

The TEA2016AAT has 3 operating modes.

1. High power
2. Low power
3. Burst

For this project, main focus area is high power mode of TEA2016AAT. In the following part working principal of high power mode is discussed.

During initial phase, Q_2 conducts and Q_1 does not conduct. Bootstrap capacitor is charged with GATELS and a diode to help GATHS turn ON. Untill, minimum ON time $t_{on(min)}$ is passed, system will stay in this state. Next state is entered when one of the following conditions are met.

- V_{SNSCAP} is less than the minimum V_{SNSCAP} voltage ($V_{ls(SNSCAP)}$)
- The current in resonant tank exceeds the over current protection(OCP) level
- Converter is near to capacitive mode
- The maximum on-time ($t_{on(max)}$) is exceeded.

Adaptive dead-time In order to avoid false detection of HB voltage, minimum non overlap time($t_{no(min)}$) is introduced. After minimum non-overlap time is passed system checks if slope of HB node is ended. When, this end of slope is detected and current in resonant tank is negative or zero, next state is entered. This dead-time system is called adaptive dead-time. $t_{no(min)}$ can be set to 50nS-200nS.

Even if end of slope for HB node is not detected, system can go into next state after maximum non-overlap time($t_{no(max)}$) has passed. In this way it is always ensured that system does not get stuck in one state.

The 3rd and 4th states in figure 3.8 are same as previous 2 states but with inverse criteria.

3.7. Capacitive mode regulation(CMR)

When input voltage is lower or output power is higher, resonant current can change its direction before capacitor voltage reaches regulation level. When the current changes polarity before switch is turned off and other switch turned on, hard switching happens. This hard switching is called capacitive mode.

In converter operation, capacitive mode should be avoided. TEA2016 employs capacitive mode regulation method to avoid operation in capacitive mode. Whenever, TEA2016 detects that resonant current is in vicinity of changing polarity, it shortens existing gate pulse and starts with the next gate signal as seen in figure 3.9. That way capacitive mode is avoided and zero voltage switching is avoided.

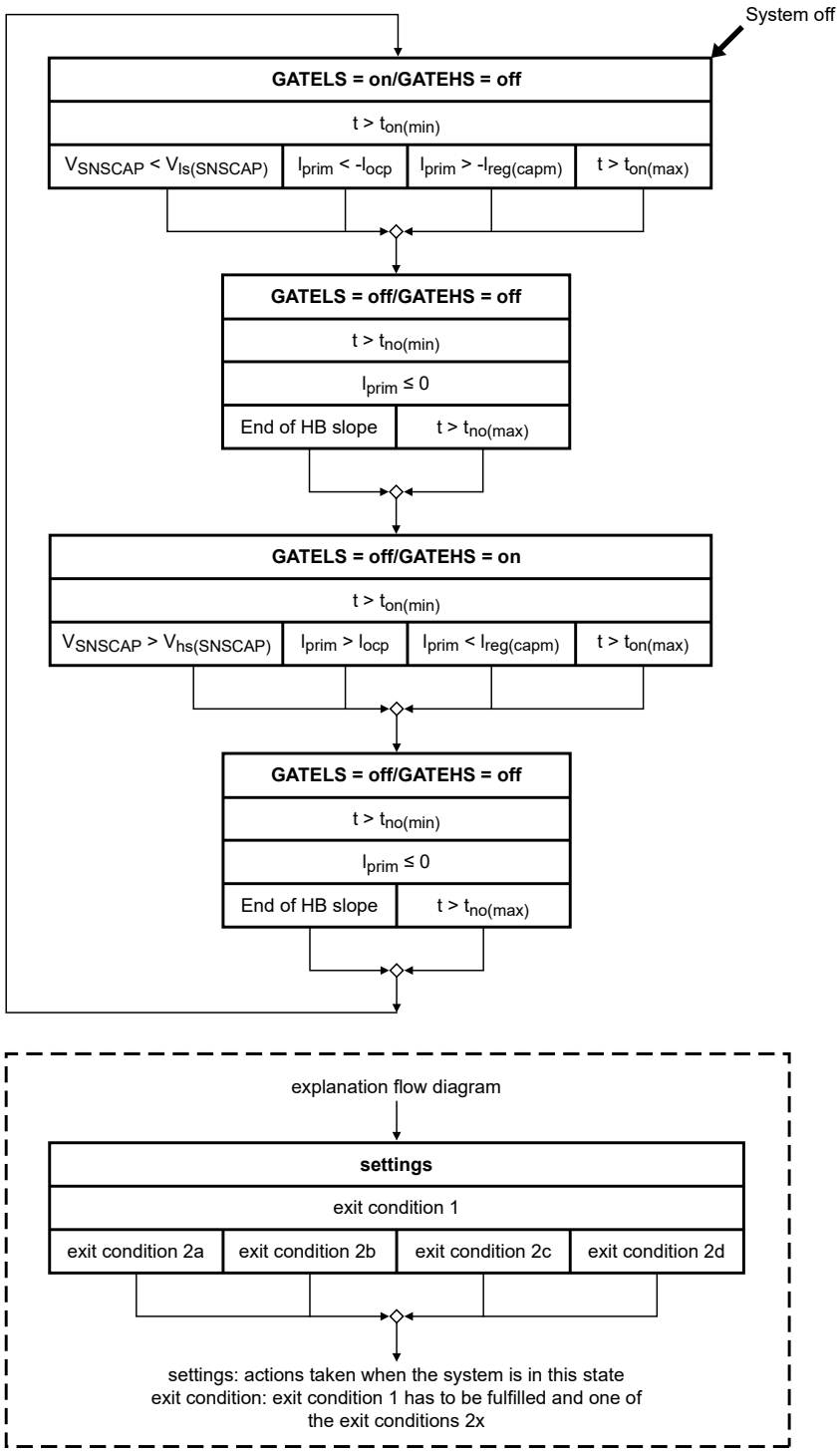


Figure 3.8: High power mode state diagram

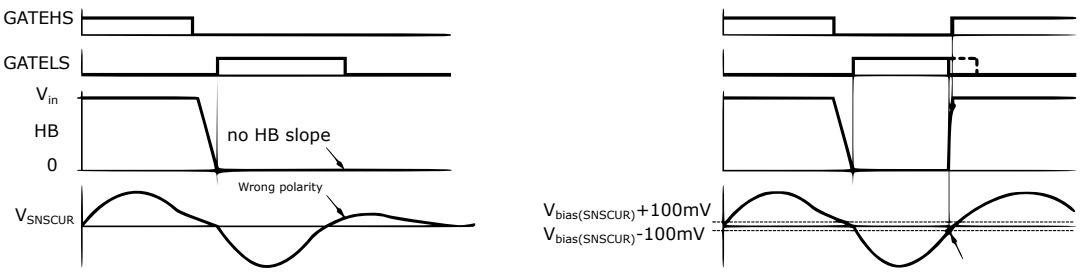


Figure 3.9: Capacitive mode regulation

4

Design of LLC converter for 500kHz operation

4.1. Specifications

The first step of any design procedure is to define what is the expected outcome after the design. In this case, outcome will be the meeting the specifications set up at the start of the design. In this section, required specifications are shown in table 4.1 from introduction chapter for a ready reference.

Parameter	Value
Input voltage	380V-410V(390V nominal) DC
Output voltage	12V DC
Output current	20A
Operating frequency	500kHz

Table 4.1: Specifications

4.2. Modelling of LLC converter

With the given specifications, a model of the converter is needed to accomplice the requirements. The most basic model gives the relationship between input and output of converter. This transfer function can be obtained by finding out all the equations driving LLC converter.

As discussed previously, LLC resonant converter is operated near the series resonant frequency for best performance. The square wave generated by switching network will contain many harmonics as shown in figure 4.1. But fundamental harmonic is most prominent one. If square wave has frequency in vicinity of resonance frequency of resonant tank, all other harmonics can be ignored and only fundamental harmonic can be used. Figure 4.1 shows impedance of LC series tank with resonant frequency of 500kHz superimposed on harmonics of 500kHz square wave. Apart from fundamental harmonic, all other harmonics are met with significant impedance from LC series circuit. This helps in ignoring all other harmonics. This approximation method is called first harmonic approximation (FHA) method [2].

4.2.1. First harmonic approximation (FHA) method

Using first harmonic approximation method, development of relation between input and output voltage becomes easier. Initial steps are as following [2]:

- Square wave input voltage and current replaced by fundamental harmonic component and ignoring other harmonics.
- Effect of secondary side leakage reactance of transformer and output capacitor can be ignored.

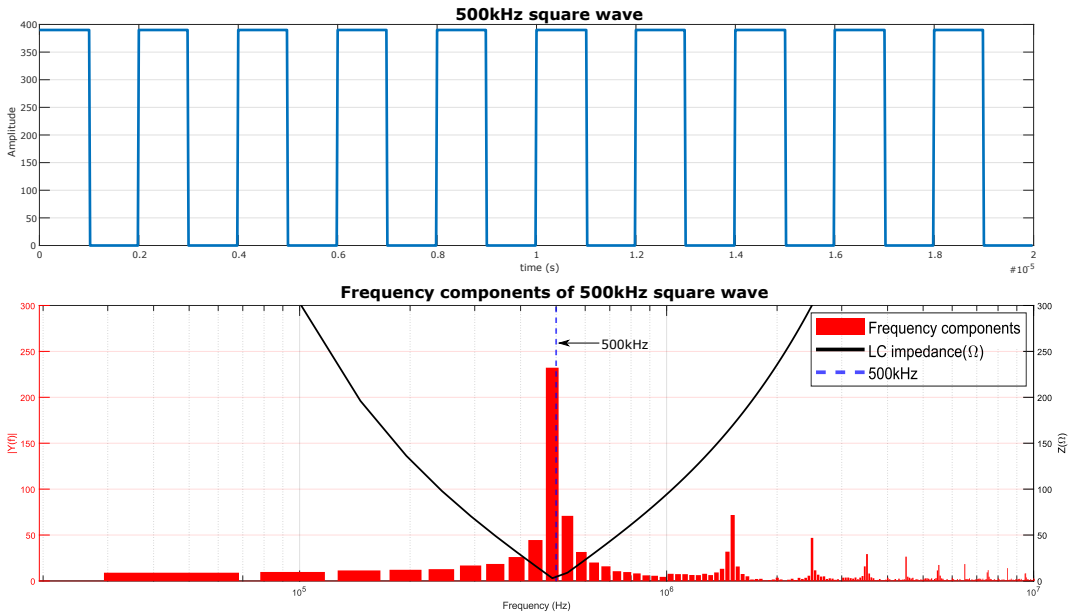


Figure 4.1: 500kHz square wave, its frequency components and LC series impedance

- Transfer secondary side components to primary side
- Similar to primary side parameters, secondary side parameters are also considered with only fundamental harmonic. Higher order harmonics are ignored.

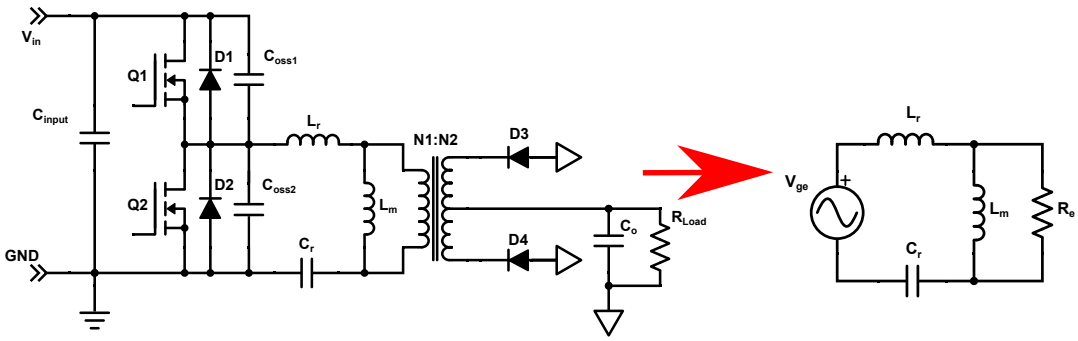


Figure 4.2: Fundamental harmonic approximation of LLC converter

Figure 4.2 shows conversion of actual LLC resonant converter circuit into first harmonic approximated circuit. Table 4.2 shows the parameters of both the circuits.

Description	Actual parameter	FHA Parameter
Input voltage	V_{in}	V_{ge}
Output voltage	V_o	V_{oe}
Load	R_{load}	R_e

Table 4.2: LLC resonant converter parameters

Relationship between actual parameter and first harmonic approximated(FHA) parameter is shown below.

Input voltage

$$v_{ge(t)} = \frac{2}{\pi} \times V_{in} \times sin(2\pi f_{sw} t) \tag{4.1}$$

$$V_{ge(RMS)} = \frac{\sqrt{2}}{\pi} \times V_{in} \tag{4.2}$$

Output voltage

$$v_{oe(t)} = \frac{4}{\pi} \times n \times V_o \times sin(2\pi f_{sw} t - \phi_v) \tag{4.3}$$

$$V_{oe(RMS)} = \frac{2\sqrt{2}}{\pi} \times n \times V_o \tag{4.4}$$

Load

$$R_e = \frac{8 \times n^2}{\pi^2} \times R_{Load} \tag{4.5}$$

Reactance

$$\omega = 2\pi f_{sw} \tag{4.6}$$

$$X_{C_r} = \frac{1}{\omega C_r}, \quad X_{L_r} = \omega L_r, \quad X_{L_m} = \omega L_m \tag{4.7}$$

Transfer function

$$M_g = \frac{V_{oe(RMS)}}{V_{ge(RMS)}} = \left| \frac{jX_{L_m} || R_e}{(jX_{L_m} || R_e) + j(X_{L_r} - X_{C_r})} \right| \tag{4.8}$$

From equation 4.2 and 4.4

$$\frac{V_o}{V_{in}} = \frac{V_{oe(RMS)}}{V_{ge(RMS)}} \times \frac{1}{2n} \tag{4.9}$$

From equation 4.8 and 4.9

$$\frac{V_o}{V_{in}} = M_g \times \frac{1}{2n} \tag{4.10}$$

4.2.2. Normalization of transfer function

For easier design, it is better to normalize values obtained above.

Frequency normalization Switching frequency(f_{sw}) is normalized with respect to series resonant frequency(f_0). f_n is the normalized frequency.

$$f_n = \frac{f_{sw}}{f_0} \tag{4.11}$$

Inductance normalization LLC resonant circuit has 2 inductances. Both the inductances can be linked with each other by normalizing magnetization inductance(L_m) with respect to resonant inductance(L_r). L_n is the normalized inductance. After a design is made L_n stays constant as it represents physical components.

$$L_n = \frac{L_m}{L_r} \tag{4.12}$$

Quality factor Quality factor of circuit is relation between resonant tank components(L_r, C_r) and first harmonic approximated(FHA) load R_e. Q_e values change during operation of converter based on load. Higher the load, higher the Q_e value.

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} \tag{4.13}$$

All 3 new parameters described above are unit-less. M_g in equation 4.8 is a function of L_m, L_r, C_r, f_{sw} and R_e. That means M_g is a 5 variable gain in equation 4.8. By replacing these variables with f_n, L_n and Q_e in equation 4.8, M_g will become a 3 variable gain. Which will make it easier to solve. This 3 variable M_g is given below.

$$M_g(f_n, L_n, Q_e) = \left| \frac{L_n \times f_n^2}{[(L_n + 1) \times f_n^2 - 1] + j[(f_n^2 - 1) \times f_n \times Q_e \times L_n]} \right| \tag{4.14}$$

M_g in equation 4.10 can be replaced by M_g from equation 4.14. Equation 4.10 can be rewritten as below.

$$\frac{V_o}{V_{in}} = M_g(f_n, L_n, Q_e) \times \frac{1}{2n} \tag{4.15}$$

4.3. Selection of parameters

For a given LLC converter specification, from equation 4.15 only V_o and V_{in} is known. f_n, L_n, Q_e and n is unknown. The whole design procedure revolves around selection of these parameters and their effects on converter operation. In this section, an overview of how these parameters are chosen is given.

4.3.1. f_n selection

f_n is the normalized frequency. As per equation 4.11, it is dependent on f_{sw} and f_0. So, selection of f_n is selection of f_{sw} and f_0. The goal of this project is to push the switching frequency(f_{sw}) to 500kHz. For LLC resonant converter, most efficient area of operation is in vicinity of series resonant frequency(f_0). So, switching frequency (f_{sw}) and series resonant frequency (f_0) will be kept same at 500kHz. In that way $f_n = 1$.

4.3.2. L_n and Q_e selection

L_n is normalized inductance and Q_e is quality factor of resonant tank. From equation 4.12 and 4.13, it can be seen that both are dependent of resonant inductor (L_r). That way L_n and Q_e are interdependent and it makes sense to choose both of them together. Before starting the selection process, some terms needs to be defined.

Maximum gain M_{g_max} is maximum gain that resonant tank has to provide in extreme operating conditions(i.e. Minimum input voltage and Maximum output voltage).

$$M_{g\_max} = \frac{n \times V_{o\_max}}{V_{in\_min}/2} \tag{4.16}$$

Minimum gain M_{g_min} is the minimum gain LLC converter will provide in case of conditions inverse of M_{g_max}.

$$M_{g\_min} = \frac{n \times V_{o\_min}}{V_{in\_max}/2} \tag{4.17}$$

Maximum attainable gain M_{g_ap} is maximum attainable gain. It is the maximum gain resonant tank can provide for a given value of L_n and Q_e.

$$M_{g\_ap} = max[M_g(f_n, L_n, Q_e)] \qquad (\because Q_e, L_n = fixed) \tag{4.18}$$

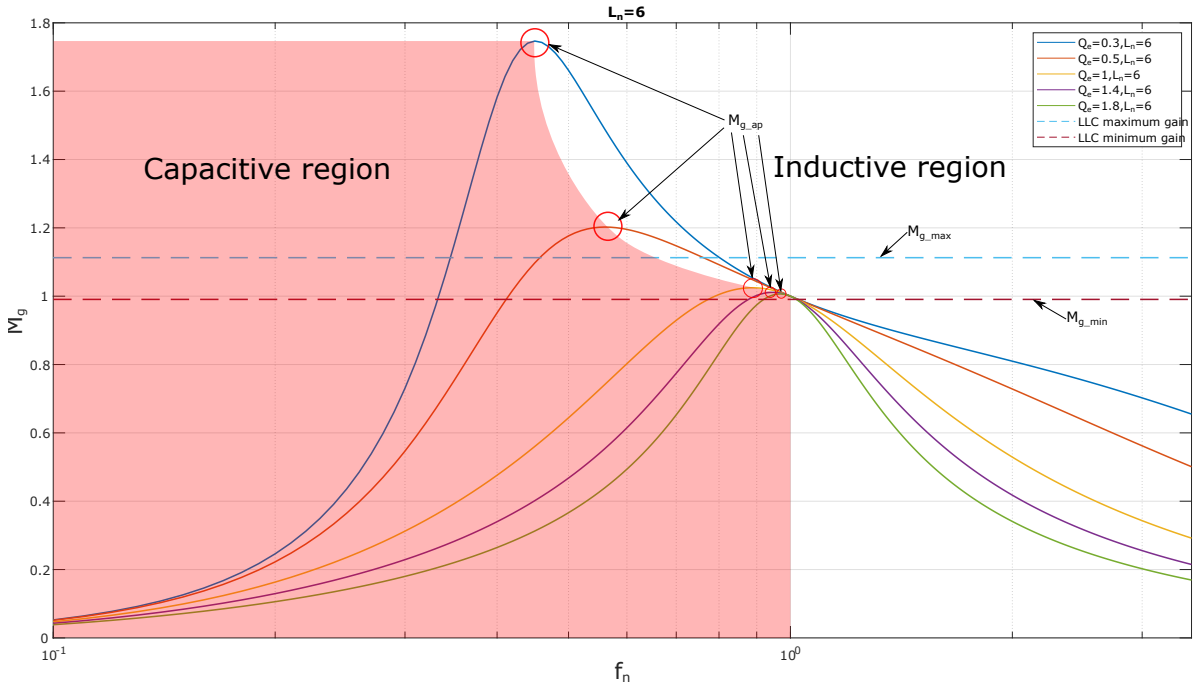


Figure 4.3: Gain curves with maximum and minimum gains

Figure 4.3 shows plot of M_g vs. f_n for a fixed value of L_n and a range of values of Q_e. M_{g_max} and M_{g_min} are 2 horizontal lines in the figure and M_{g_ap} is the circled peaks of each gain curve. Q_e and L_n should be designed in a such way that for all possible values of Q_e for a given L_n, $M_{g\_ap} > M_{g\_max}$.

An easier approach for selection of L_n and Q_e values is usage of M_{g_ap} curves.

Figure 4.4 shows this peak gain curves. Peak gain curve is a curve between peak gain M_{g_ap} and quality factor Q_e for a given value of L_n. All points above M_{g_max} line can satisfy design requirements. But choosing a particular combination of Q_e and L_n depends on design requirements.

1. Higher L_n value increases efficiency but robustness of regulation decreases.

2. Lower Q_e causes higher frequency variation to achieve required gain.

For start of the design, $L_n = 5$ and $Q_e = 0.5$ can be chosen.

4.3.3. n selection

n is the turns ratio of transformer. At normal operating condition, M_g can be considered 1. At normal operating condition, V_{in} is V_{in_nom} and V_o is V_{o_nom}. Replacing these values in equation 4.10 and solving it for n gives the turns ratio of transformer.

$$n = \frac{V_{in\_nom}}{2 \times V_{o\_nom}} \Bigg| M_g = 1 \tag{4.19}$$

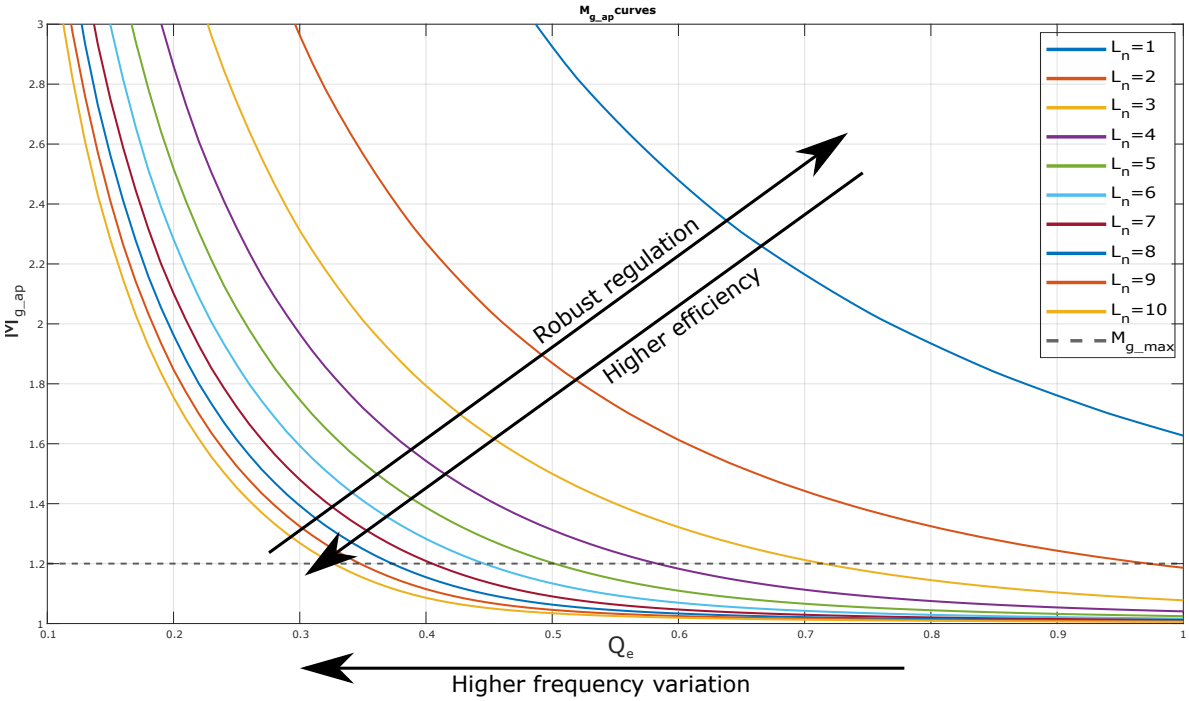


Figure 4.4: Peak gain curve

4.4. Design flow

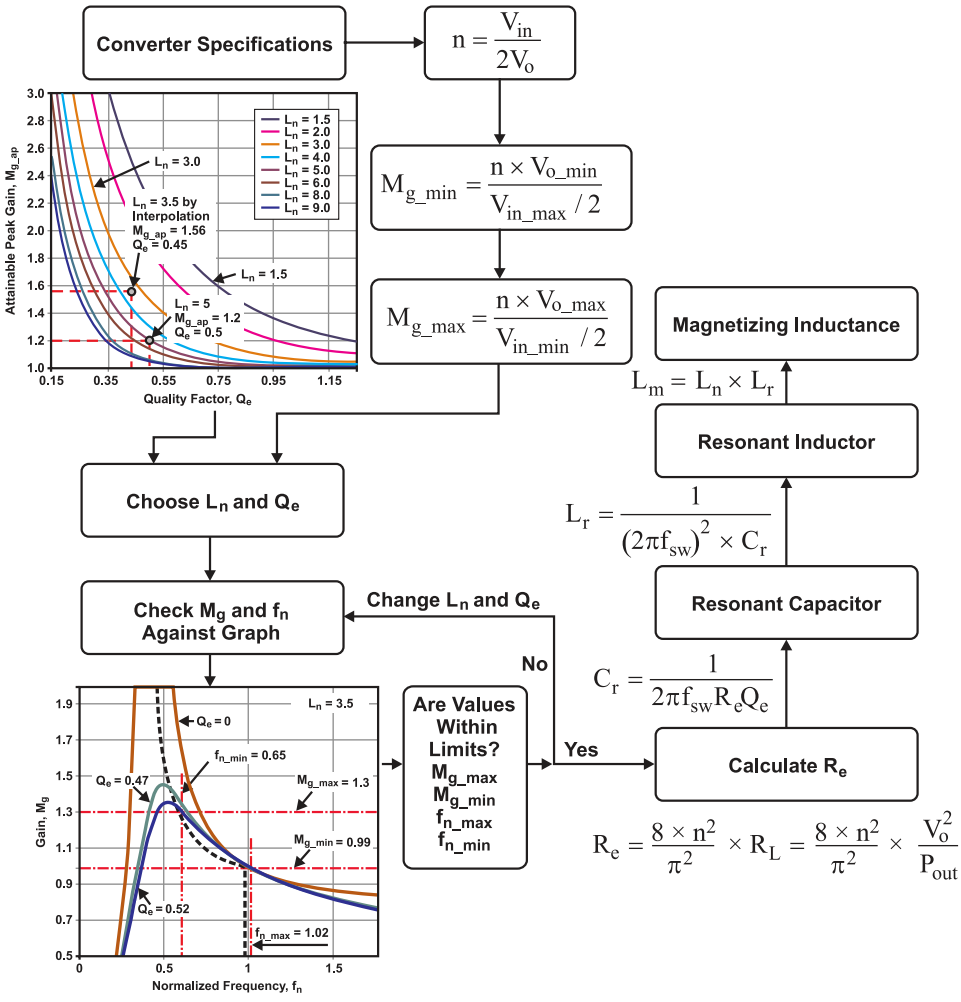


Figure 4.5: Resonant tank parameter design flowchart[2]

Figure 4.5 shows the flowchart of LLC converter design based on the previous discussion. Based on the design procedure in flowchart and specifications given in table 4.1 converter is designed.

Step 1: Transformer turns ratio $\mathbf{n}$

$$n = \frac{V_{in}}{2V_o} = \frac{390}{2 \times 12} = 16.25 \approx 16 \tag{4.20}$$

Step 2: Minimum gain $\mathbf{M_{g\_min}}$

$$M_{g\_min} = \frac{n \times (V_{o\_min} + V_F)}{V_{in\_max}/2} = \frac{16 \times [12 \times 0.99 + 0.7]}{410/2} = 0.98 \tag{4.21}$$

Step 3: Maximum gain $\mathbf{M_{g\_max}}$

$$M_{g\_max} = \frac{n \times (V_{o\_max} + V_F + V_{loss})}{V_{in\_min}/2} = \frac{16 \times [12 \times 1.01 + 0.7 + 1.04]}{380/2} = 1.17 \tag{4.22}$$

V_{loss} is estimated extra voltage required to feed the loss. For a estimated efficiency of 92%, V_{loss} is as below.

$$V_{loss} = \frac{240W \times 0.08/0.92}{20A} = 1.04V \tag{4.23}$$

Considering 10% overload, M_{g_max} value is increased by 10% to avoid converter in going into capacitive region.

$$M_{g\_max} = 1.1 \times M_{g\_max} = 1.1 \times 1.17 = 1.29 \tag{4.24}$$

Step 4: $\mathbf{L_n}$ and $\mathbf{Q_e}$

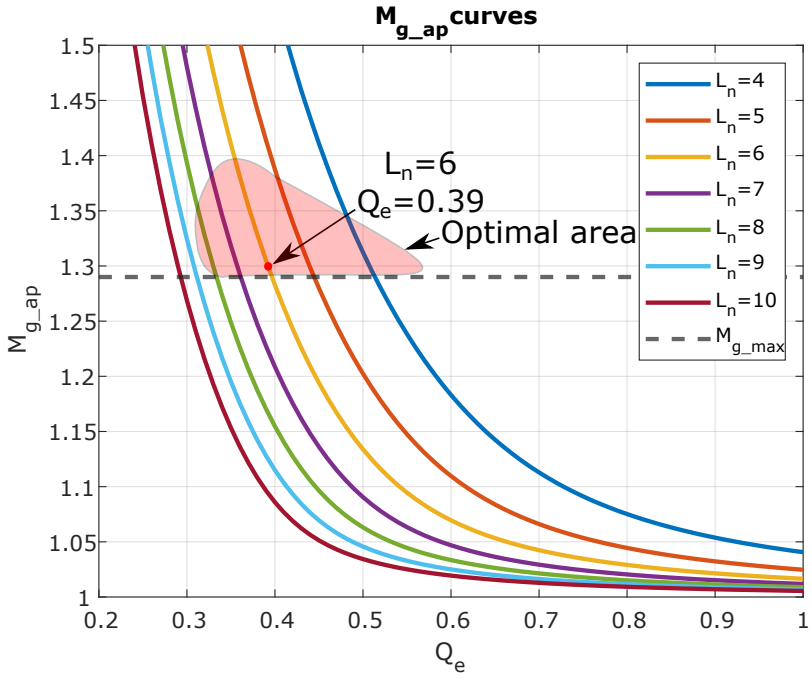


Figure 4.6: Peak gain curve for Ln and Qe selection

Based on peak gain curves of figure 4.6 L_n and Q_e is selected as 6 and 0.39 respectively. These values will provide a good balance between higher efficiency and lower switching frequency range.

Step 5: First harmonic approximated load

From equation 4.5, with 10% overload

$$R_e = \frac{8 \times 16^2 \times 12V}{\pi^2 \times 20A \times 1.1} = 113.18\ \Omega \tag{4.25}$$

Step 6: Resonant tank design

$$C_r = \frac{1}{2\pi \times f_0 \times R_e \times Q_e} = \frac{1}{2\pi \times 500 \times 10^3 \times 113.18 \times 0.39} = 7.21\ nF \tag{4.26}$$

$$L_r = \frac{1}{(2\pi \times f_0)^2 \times C_r} = \frac{1}{(2\pi \times 500 \times 10^3) \times 7.21} = 14.05\ \mu H \tag{4.27}$$

$$L_m = L_n \times L_r = 6 \times 14.05 = 84.3\ \mu H \tag{4.28}$$

4.5. Magnetics design

It is possible to design magnetic components necessary in LLC resonant converter discretely. But apart from having lower losses, LLC resonant converter gives a unique benefit of combining 2 passive magnetic elements L_m and L_r into one single physical component. This integration is achieved by using leakage inductance of a transformer as resonant inductance L_r and magnetizing inductance as L_m.

L_m can be controlled by adding a gap in transformer core, and L_r can be controlled by placement of primary and secondary windings. Introduction of gap changes the design of magnetic component from a design of a transformer for power transfer to design of an inductor based on stored energy. Flux is set-up by current passing through L_m and primary current of transformer decides the losses[9].

Design methodology Design methodology is divide in 2 parts.

1. L_m: Design guidelines given in [9] is followed for L_m. It gives transformer core size and air-gap size.
2. L_r: Using the core data obtained in L_m design and using ANSYS PExprt® software to go through all the winding placement that match the requirement. Then choose whichever winding placement matches required L_r value.

4.5.1. Design considerations for gapped transformer

Maximum flux density (B_{max})

Let current through primary side of transformer be i_p and secondary currents be i_{D1} and i_{D2}. i_{L_m} is the current through magnetizing inductance. Flux produced by i_p and i_{D1}, i_{D2} cancels each other and is used for direct power transfer from primary side to secondary side. i_{L_m} produces the magnetizing flux of the core and feeds the core losses as seen in figure 4.7. B_{max} can be given by below equation [9].

$$B_{max} = \frac{\mu_0 \mu_{eff} N_p I_{L_{m_{peak}}}}{l_c} \tag{4.29}$$

Here,
B_{max}= Maximum flux density
N_p= Primary number of turns
μ_{eff}= effective relative permeability
$I_{L_{m_{peak}}}$ = Peak magnetization current
l_c= Magnetic path length

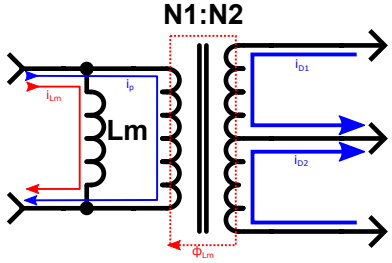


Figure 4.7: Currents and magnetic field in transformer

B_{max} should not exceed saturation flux density B_{sat} for a core to keep converter working properly and avoiding very high core losses.

Fringing effect due to air gap

In flux fringing, magnetic flux in core fringes outwards when there is a significant change of relative permeability(i.e.near an airgap) as seen in figure 4.8. This flux flowing in window area of core causes extra losses in conductors nearby airgap due to opposition current produced by fringing flux in the conductor.

To keep losses due to fringing flux as low as possible, airgap length should be as small as possible.

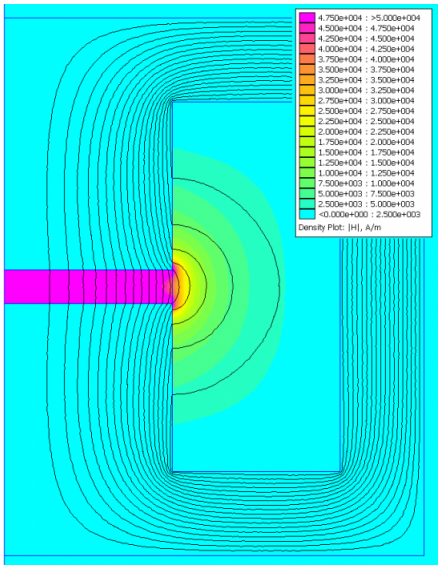


Figure 4.8: Fringing effect near airgap (credit: S. Zurek, Encyclopedia Magnetica, CC-BY-3.0) [10]

4.5.2. Design flow

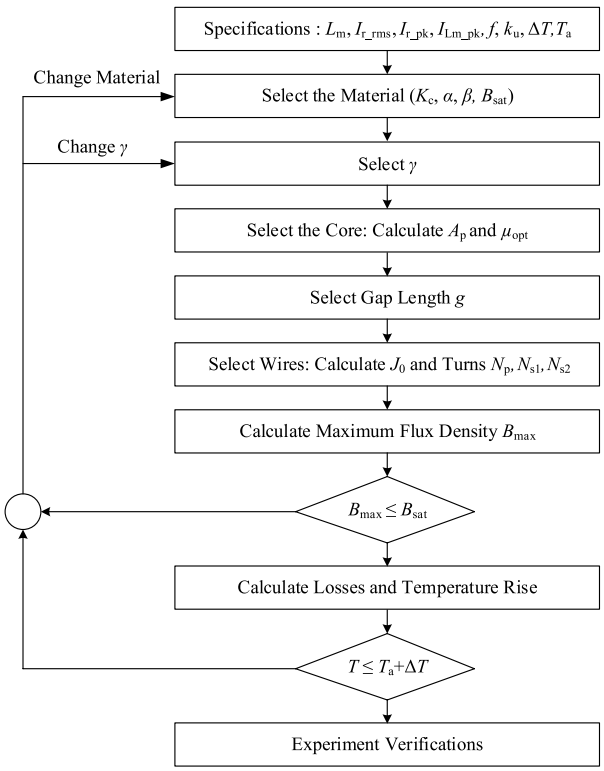


Figure 4.9: Transformer designflow [9]

Step 1: Gathering all parameters as mentioned in specifications box

$$I_{r\_rms} = \sqrt{\frac{n^2 V_o^2 T_r^2 (2T_s - T_r)}{32 L_m^2 T_s} + \frac{\pi^2 I_o^2 T_s^2}{8 n^2 T_r^2}} \tag{4.30}$$

$$I_{r\_peak} = \sqrt{\left(\frac{nV_o}{4 f_r L_m}\right)^2 + \left(\frac{\pi I_o}{2 n f_n}\right)^2} \tag{4.31}$$

$$I_{L_{m\_peak}} = \frac{nV_o}{4 L_m f_r} \tag{4.32}$$

Here,

I_{r_rms} = RMS current through resonant tank
I_{r_peak} = Peak value of current through resonant tank
$I_{L_{m\_peak}}$ = Peak current through magnetization inductance(L_m)
n = Transformer turns ratio
T_r = ON time of 1 switch of half bridge
T_s = T_r + dead time
I_o = Output current
f_r = $1/T_r$

k_u It is the window utilisation factor of the transformer. $k_u = 0.55$ is a good initial choice.

$$k_u = \frac{copper\ area}{window\ area} \tag{4.33}$$

ΔT and T_a ΔT is the temperature rise and T_a is ambient temperature.

Manufacturer	Material	P(kW/m3) @ 500kHz,50mT,100°C	μ_i
Mag-inc	L	115	900
	T	150	3000
	R	175	2300
	P	300	2500
TDK	N49	82.15	1500
	PC200	99.88	800
	N97	212.16	2300
	N87	219.15	2200
	N87	219.18	2200
	N95	231.99	3000
	N92	245.31	1500
	N72	253.43	2500
	N96	268.43	2900
	N88	277.66	1900
Ferroxcube	3F36	90	1600
	3F45	100	750
	3F3	210	2000
	3F4	210	900
Fairrite	79	80	1400

Table 4.3: Different core materials available

Step 2: Core material selection Table 4.3 shows different core materials available from different manufacturer with its core losses P and initial permeability μ_i. 3 highlighted rows show materials suggested by manufacturers for lower losses at higher frequency operation.

Step 3: γ selection γ is loss factor to show all losses in terms of DC copper losses(P_{cu}).

$$P_{total} = (1+\gamma)P_{cu} \tag{4.34}$$

$$P_{cu} = R_{p\_DC}I_{r\_RMS}^2 + 2R_{s\_DC}I_{s\_RMS}^2 \tag{4.35}$$

Where, R_{p_DC} and R_{s_DC} are primary and secondary winding DC resistance.

Core size selection For core size selection, 2 parameter needs to be found: Area product A_p and optimal relative permeability μ_{eff}. Area product A_p of a core is a product of core cross-section area A_c and core window area A_w.

$$A_p = \left(\frac{L_m I_{L_{m\_peak}} I_{r\_RMS} \sqrt{k_u(1+\gamma)}}{B_{max} K_t k_{up} \sqrt{\Delta T}} \right)^{8/7} \tag{4.36}$$

Here,

K_t = Dimensional parameter = 48.2×10^3 [3]

k_{up} = Window utilization factor of primary winding = $k_u \frac{1}{1+\frac{2I_{s\_RMS}}{nI_{r\_RMS}}}$

Based on A_p value, a core size is selected from manufacturer catalogue. This selection gives value of A_w. For calculation of airgap optimum relative permeability is calculated using formula given below.

$$\mu_{eff} = \frac{B_{max} l_c}{\mu_0 \sqrt{\frac{P_{cu\_p} k_{up} A_w}{\rho_w MLT}}} \frac{I_{r\_RMS}}{I_{L_{m\_peak}}} \tag{4.37}$$

Where,

l_c = Length of magnetic path

P_{cu_p} = Primary winding DC copper loss

ρ_w = Conductor resistivity

MLT = Mean turn length for given core shape and size

Step 4: Airgap selection Usually, a core with 3 legs is chosen structural stability. In a core with 3 legs, airgap is distributed in all 3 legs. Based on effective relative permeability, airgap length for a airgap divided over multiple legs can be calculated as below.

$$g = \frac{l_c}{2}\left(\frac{1}{\mu_{eff}} - \frac{1}{\mu_r}\right) \tag{4.38}$$

Here, μ_r = relative permeability of core material

Step 5: Transformer turns calculation Using airgap value found above, inductance per turn A_L can be calculated.

$$A_L = \frac{\mu_0 \mu_r A_c}{2g\mu_r + l_c} \tag{4.39}$$

Total number of primary turns N_p is calculated as below,

$$N_p = \sqrt{\frac{L_m}{A_L}} \tag{4.40}$$

Number of secondary turns can be calculated as below,

$$N_s = \frac{N_p}{a} \tag{4.41}$$

Step 6: Wire size For choosing conductor size, current density J_0 is an important parameter. J_0 is dependent on temperature rise.

$$J_0 = K_t \sqrt{\frac{\Delta T}{k_u(1+\gamma)}} A_p^{-\frac{1}{8}} \tag{4.42}$$

Step 7: Maximum flux density ($\mathbf{B_{max}}$) calculation B_{max} can be calculated from equation 4.29.

Step 8: Losses calculation Core losses are calculated as below

$$P_{fe} = V_c K_c f^{\alpha} B_{max}^{\beta} \tag{4.43}$$

4.5.3. Design flow for achieving required leakage inductance (L_r)

Leakage inductance is decided by placement of windings with respect to each other. Transformer design guidelines available optimize the design for lowest leakage inductance possible and give tips on winding placement to minimize the leakage inductance. These design guidelines doesn't help in achieving a particular leakage inductance value as required in LLC converter magnetics design.

One way to achieve this by taking help of software to go through all the possible placements and get leakage inductance for each placement. And choose the placement which provides the closest value of leakage inductance to the required leakage inductance value. Following images show steps taken in ANSYS PExprt to achieve desired leakage inductance values. This method is especially useful for high frequency designs as it at higher frequency, required resonant inductor value is smaller and more manageable with this brute force method. The design steps are given in appendix.

5

Experimental setup

5.1. Transformer

Transformer is bulit according to design. The specifications are as given in table 5.1. The construction of transformer is depicted in figure 5.1

Parameter	Value
Primary turns	17
Secondary turns	2 × 1
Primary turns configuration	1*50*0.1mm litz wire
Secondary turns configuration	6*50*0.1mm litz wire
Core	2*ETD34/17/11
Core material	3F36
Airgap	0.13mm
Airgap material	55GSM thermal paper

Table 5.1: Transformer construction

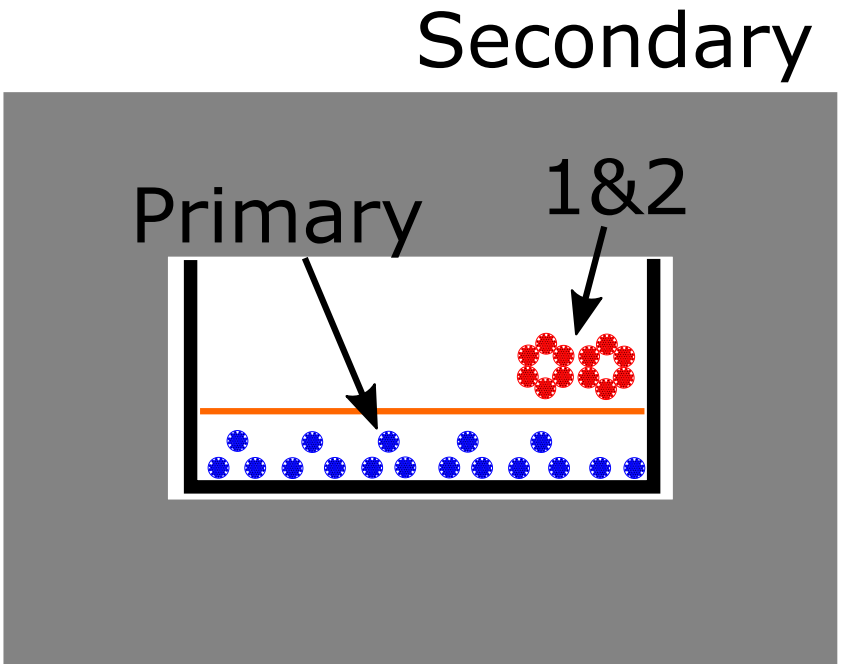


Figure 5.1: Transformer cross-section

5.2. Resonant tank

Parameter	Value
Leakage inductance L_r	19.3µH
Magnetizing inductance L_m	109.2µH
Resonant Capacitance C_r	5.6nF
Resonant frequency f_r	484.1kHz

Table 5.2: Transformer parameters

Based on obtained L_r value, nearest C_r value for achieving resonant frequency near to 500kHz was 5.6nF. With new resonant tank values, resonance frequency is 484.1kHz

5.3. TEA2016 demoboard

NXP has designed a demoboard for TEA2016 for customer evaluation. This board is designed for a similar power rating and output voltage specification.Switching frequency of the demoboard is 87kHz. For proof of concept purposes, it was decided to modify existing demoboard with new resonant tank components and respective measurement components. Demoboard contains secondary side synchronous rectification using NXP IC TEA1995. During initial testing synchronous rectification was kept ON, but after some issues as discussed in results chapter, synchronous rectification was changed to Schottky diodes. The changes done in the board are discussed in this chapter.

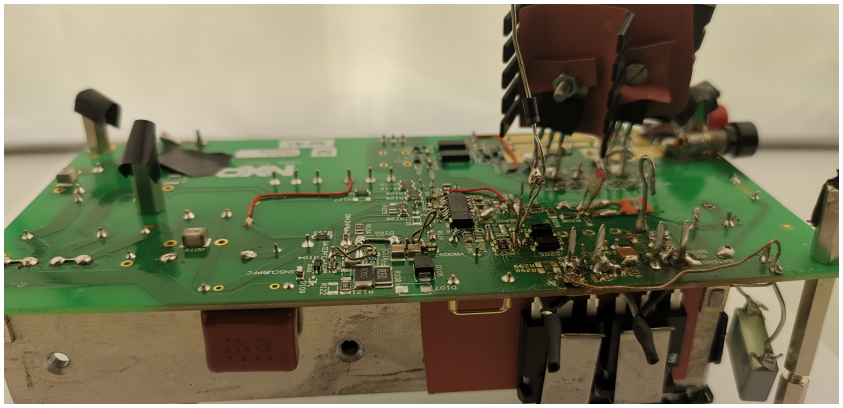


Figure 5.2: Modified TEA2016 demoboard

5.4. Disabling PFC

TEA2016 is a combo controller with PFC and LLC control in a single package. Since the focus of this project is only on LLC controller, PFC section of the controller has to be removed. In TEA2016, this is possible without modifying board contents. TEA2016 is digitally programmable controller. This programming is done using Ringo GUI available from NXP. Ringo GUI gives an option disable operation of PFC controller part of TEA2016. Disabling operation PFC controller part stops gate signal given to PFC boost converter circuit. After disabling PFC controller part, DC supply of 380V-410V has to be given to operate LLC converter properly instead of AC supply.

5.5. Transformer inductance measurement

5.5.1. Leakage inductance(L_r) measurement

Transformer leakage inductance is measured by shorting the secondary side of transformer as seen in figure 5.3. When shorted path is transformed on primary side it creates a zero resistance path parallel to magnetizing inductance (L_m). Hence, when inductance is measured from primary side, the measured inductance is only leakage inductance(L_r) of transformer.

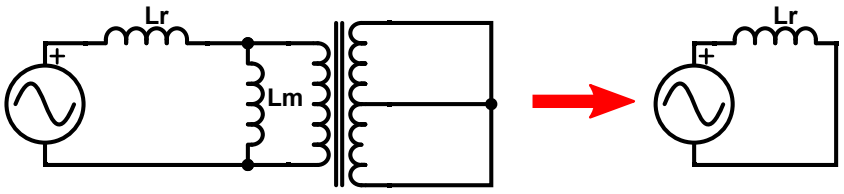


Figure 5.3: Leakage inductance(L_r) measurement circuit

5.5.2. Magnetizing inductance(L_m) measurement

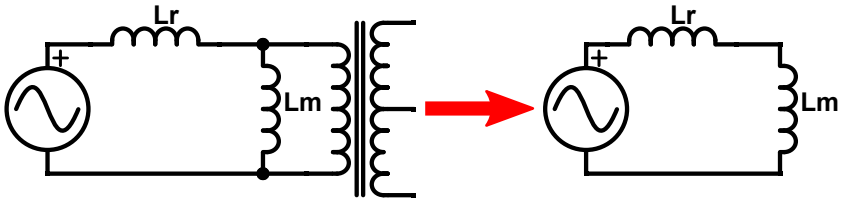


Figure 5.4: Magnetizing inductance(L_m) measurement circuit

Transformer magnetizing inductance is not directly measurable. First, total inductance is measured by open circuit on secondary side of transformer as seen in figure 5.4. It's equivalent circuit is also shown in figure 5.4. Equivalent circuit consists of series combination of leakage inductance(L_r) and magnetizing inductance(L_m). Based on leakage inductance measured previously and series inductance measured here, magnetizing inductance(L_m) can be found.

5.6. V_{SNSCAP} divider calculation

As discussed previously, resonant capacitor voltage (V_{C_r})value is scaled down to V_{SNSCAP} value by using a capacitive voltage divider. In this section, this capacitive divider is chosen.

$$\Delta V_{Cr\_ideal} = \frac{P_O}{V_{in} \times C_r \times f_{HB}} \tag{5.1}$$

Equation 5.1 calculates voltage across resonant capacitor (C_r) for a given output power. This calculated voltage is in case of ideal circuit. But internal delay from IC needs to be considered in measuring voltage across capacitor. Voltage related to this delay is calculated in equation 5.2. Where Δt_{delay} is 150nS+ rise time of half-bridge voltage.

$$\Delta V_{Cr\_delay} = \frac{I_{m,peak} \times \Delta t_{delay}}{C_r} \tag{5.2}$$

Total voltage across resonant capacitor is calculated by equation 5.3.

Parameter	Component number	Value
$C_{SNSCAPhigh}$	C_{208}	330pF(630V)
$C_{SNSCAPlow1}$	C_{219}	5.6nF(50V)
$C_{SNSCAPlow2}$	C_{207}	56nF(63V)

Table 5.3: SNSCAP values

$$\Delta V_{C_r} = \Delta V_{Cr\_ideal} - \Delta V_{Cr\_delay} \tag{5.3}$$

As per [6], ΔV_{SNSCAP} can be calculated as per equation 5.4.

$$\Delta V_{SNSCAP} = 2 \times \frac{1.6V}{V_{in}} \times 0.0075V \times P_{O\%} \tag{5.4}$$

Now, from calculated ΔV_{SNSCAP} and ΔV_{C_r} higher and lower capacitor ratio can be calculated according to equation 5.5.

$$\frac{C_{SNSCAPlow}}{C_{SNSCAPhigh}} = \frac{\Delta V_{C_r} - \Delta V_{SNSCAP}}{\Delta V_{SNSCAP}} \tag{5.5}$$

Based on calculation procedure shown above following values are selected as shown in table 5.3.

6

Results

6.1. Effect of adaptive deadtime

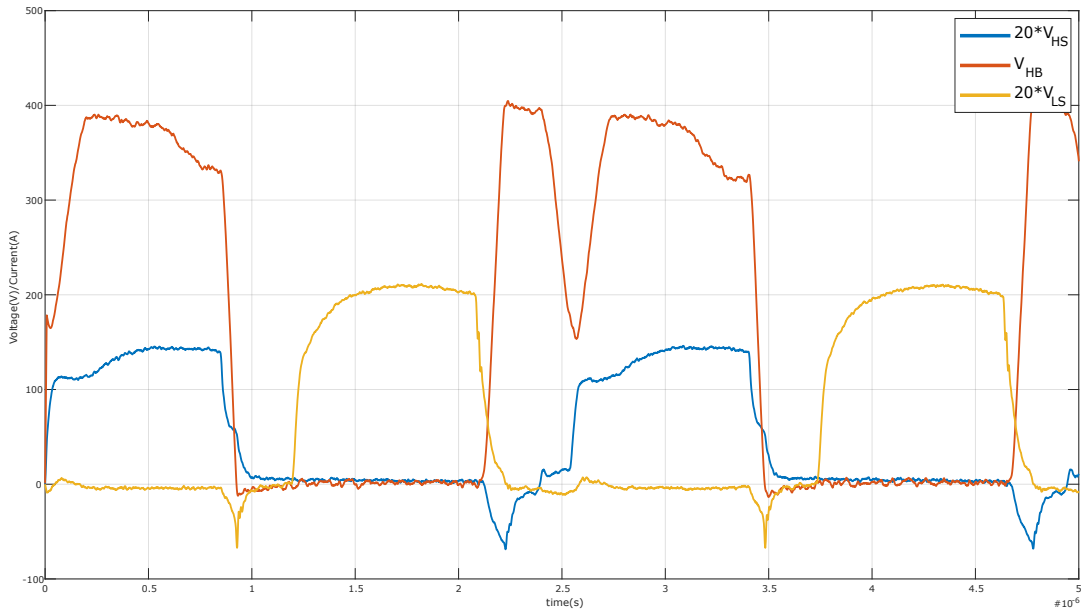


Figure 6.1: Opeartion with adaptive deadtime

Initially, adaptive dead-time is kept on. Due to working of adaptive dead-time explained previously, zero voltage switching is lost as seen in figure 6.1. When, minimum non-overlap time $t_{no(min)}$ is over TEA2016 starts detection for end of slope for half bridge voltage (V_{HB}). Calculation for detection of this end slope takes some time inside TEA2016. When using a SiC MOSFET with very low MOSFET capacitances at higher frequency, half bridge point is charged way faster than Si MOSFET at low frequency operation. Since, capacitance of half bridge point is lower with SiC, the dead time provided by adaptive dead time mechanism is too long. Half bridge point starts getting discharged before HS can turn-on due to longer dead-time which causes loss of zero voltage switching.

Fixed dead-time Problem caused by adaptive dead-time can be solved by using fixed dead-time instead of using adaptive deadtime. In fixed dead-time, next switch is turned ON as soon as minimum non-overlap time $t_{no(min)}$ is passed. This can also result in loss of zero voltage switching but careful selection of minimum non-overlap time $t_{no(min)}$ can ensure discharging of half bridge point and zero voltage switching. This solution is not ideal as one of the important feature of IC TEA2016 is bypassed. Ideal solution would be to reduce end of slope detection time required by TEA2016 so that next switch can be turned ON as soon as end of slope is reached.

6.2. Undesirable dip in half voltage and operation away from resonance frequency

Figure 6.2: Imperfect operation(V_{HB},V_{HS},V_{LS})

As seen in figure 6.2, half bridge voltage V_{HB} has a voltage dip while GATEHS is ON. Apart from this, converter also operates away from resonance point operation.

Reason: Synchronous rectification At this point secondary side still had synchronous rectification by NXP IC TEA1995. During testing it was found that converter output is getting shorted after few minutes of operation. Upon further investigation it was found that synchronous rectification MOSFETs were shorted which causes output to be shorted and causing over power protection(OPP) on primary side to be activated. The cause for this is slow operation of TEA1995.

There is no active communication between TEA2016 on primary side and TEA1995 on secondary side. TEA1995 detects change of polarity on secondary side and turns ON respective MOSFET to reduce conduction losses of diode. But, when operating at higher frequency, slow detection of TEA1995 can turn both MOSFET ON simultaneously. This causes a impulse current to flow through synchronous rectification MOSFETs. This current is also reflected on primary side which causes half bridge voltage (V_{HB}) to drop as seen in figure 6.2. Higher primary current also activates over power protection(OPP) in TEA2016. Further, repeated pulsed current passing though synchronous rectification MOSFETs causes permanent damage and they get shorted.

Solution: Replacement of synchronous rectification with Schottky diode As discussed above, the reason behind undesirable operation is synchronous rectification. The solution to the problem is replacement of synchronous rectification MOSFETs with Schottky diodes. This will increase losses on secondary side compared to synchronous rectification but converter will be able to operate at resonance which means reverse recovery losses in diodes are eliminated and only forward conduction losses remain. Synchronous rectification MOSFETs are replaced by Schottky diodes 32CTQ030 by International Rectifier.

6.3. Operation at resonance

Figure 6.3 shows operation of LLC resonant converter near resonance frequency. Switching frequency is 479.6kHz which is very near to resonance frequency of 484kHz. Zero voltage switching is achieved which can be inferred by absence of miller plateau in waveform of GATELS (V_{LS}) and GATEHS (V_{HS}).

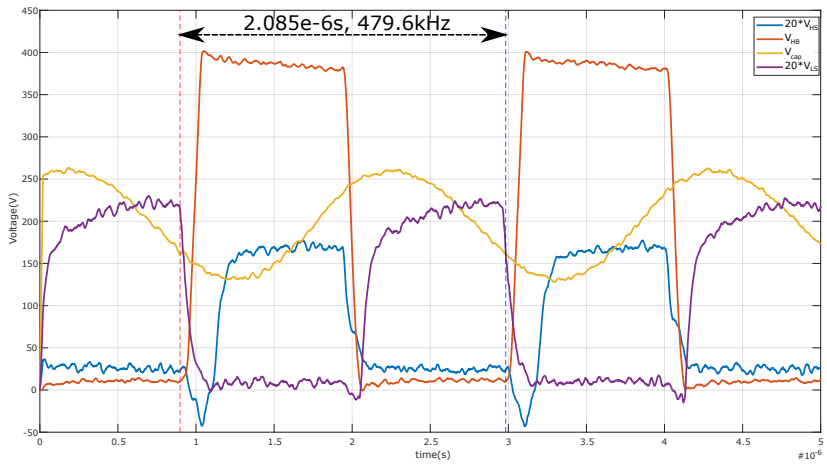


Figure 6.3: Operation at resonance

6.4. Temperature rise of controller

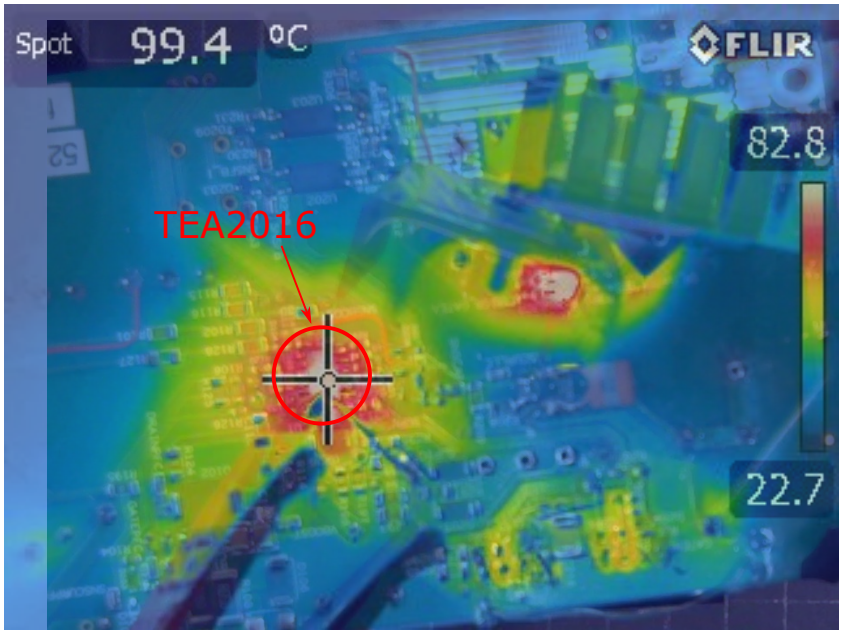


Figure 6.4: Thermal image of TEA2016 at resonance

Figure 6.4 shows infrared image of TEA2016 while converter is operating at resonance. As seen in figure 6.4, temperature of TEA2016 is nearly 100°C. Which is quite high and not good for longevity of IC.

Reason This is an expected behaviour as internal switching related losses are increased when converter is operating at higher frequency because gate driver has to supply the gate more often compared to lower frequency.

Solution:Addition of heatsink Addition of a heatsink can alleviate the higher temperatures. This heatsink can be as simple as a copper foil. After addition of heatsink IC temperature was recorded at 60°C.

6.5. Efficiency

Overall converter efficiency at various loading conditions is visible in figure 6.5. Further figure 6.6

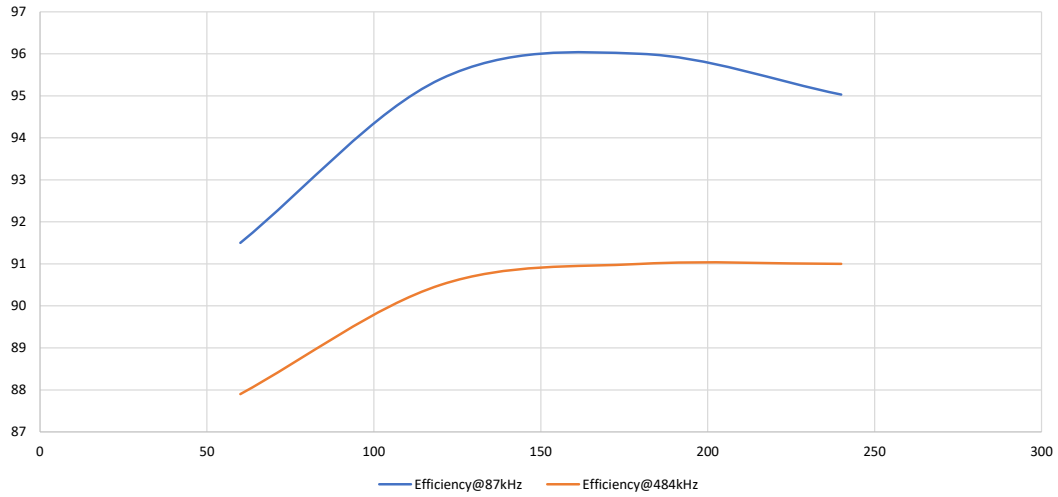


Figure 6.5: Efficiency

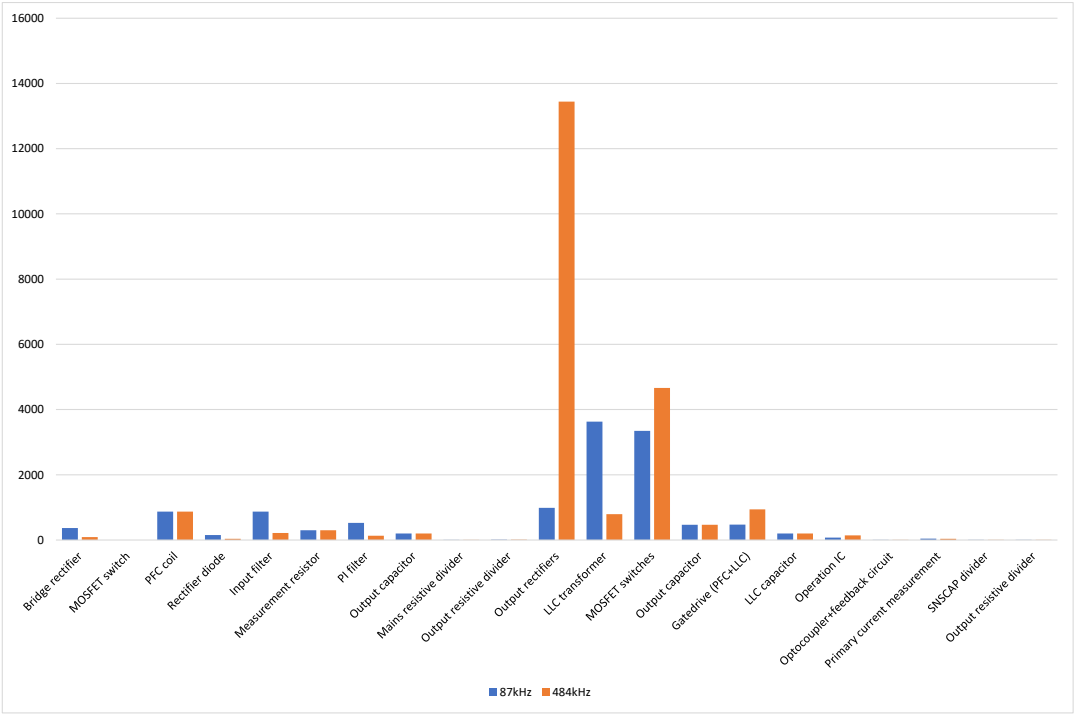


Figure 6.6: Loss bifurcation

shows the bifurcation of losses occuring in the whole converter. As seen in figure 6.6, by far the biggest contributor to the lower efficiency is output rectifier. During solution of previous problem, synchronous rectification was replaced by Schottky diodes. This contributes to significant amount of losses. If schottky diodes are replaced by synchronous rectification, efficiency will be much higher.

Figure 6.7: Transformer size comparison: Same core size ETD34/17/11

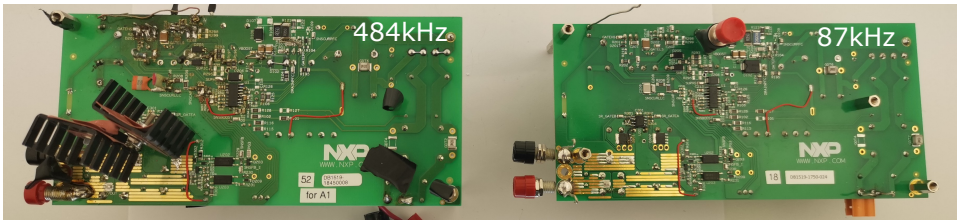


Figure 6.8: Demo board comparison

6.6. Volume

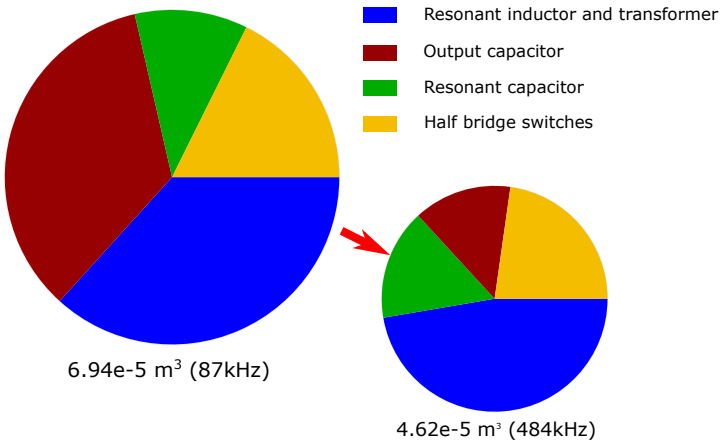


Figure 6.9: Volume reduced by 32%

Volume has been reduced by 32% in 484kHz design compared to 87kHz design. But the main contributor to volume reduction is reduction in output capacitor size. Resonant tank volume remained same even though its values decreased significantly.

Reason For magnetic component, the limitation was from material side. As currently available ferrite materials allow very low magnetic flux density at higher frequencies compared to at lower frequencies in order to keep losses minimum. Further increasing flux density to allow for smaller size leads to higher losses. Also, choices of core shapes available is limited for higher frequency ferrite material. In the current design there is a empty window area which can be reduced while keeping core cross section constant if other core shapes were available.

For resonant capacitor, size reduction is possible but here size remained constant due to unavailability of particular 5.6nF capacitor rated at 500V in laboratory. As a result, 5.6nF 2000V capacitor was utilised which had the same size as 33nF 500V capacitor utilised in 87kHz design.

7

Conclusion

The goal of the research was to design a LLC resonant converter for 500kHz and evaluate its performance and volume compared to lower frequency existing design.The research initiated with study of LLC resonant converter and its working. Various operating phases and their importance is discussed. Further, study of LLC resonant converter controller TEA2016 is done to understand the control mechanism. Various features of the controller and their operation is discussed.

Using the knowledge gained from operation of controller and converter, design methodology for an LLC converter is presented. This design methodology helps in determining values of various resonant tank components. Further, design methodology for integrated magnetics is presented. This methodology incorporates two resonant tank components L_r and L_m inside one single physical component.

Based on the design, an existing LLC resonant converter demo board is modified to operate at 500kHz. Various problems encountered for operation at higher frequency is solved. The final resonant converter is able to achieve an efficiency of 90% while reducing the size of passive components by 32%.

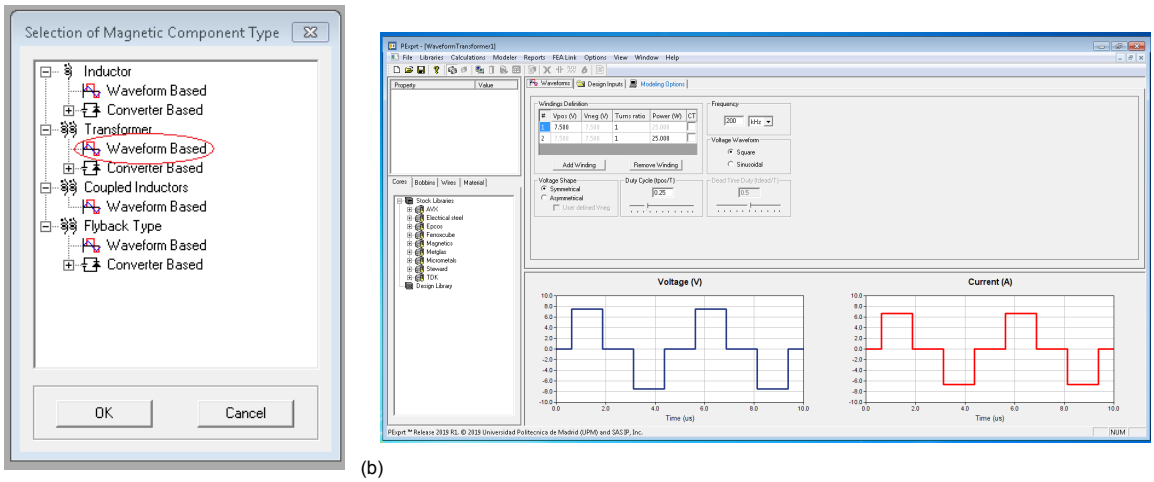
Efficiency can be further improved if a high frequency synchronous rectification is included in the secondary side. Further volume reduction of magentic component is also possible if a better magnetic material which allows for higher magnetic flux density while operating at higher frequency is developed. Using currently available materials also size reduction is possible if more range of shapes is available.

On the controller side, a faster voltage slope detection mechanism is necessary in order to use the feature of adaptive dead-time. A workaround for current design was possible but it might not be the suitable choice for all designs as a very important feature had to be turned off for the workaround.

A

Leakage inductance design

A.1. Waveform input



(a) (b)

Figure A.1: Initial selection of transformer type

A.2. Waveform type, frequency and voltage

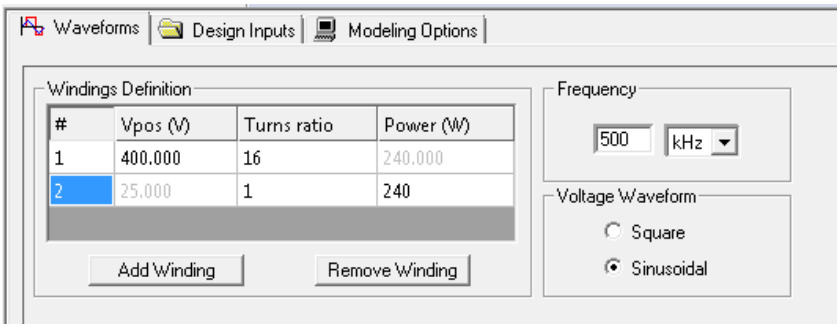


Figure A.2: Waveform type, frequency and voltage

A.3. Design inputs

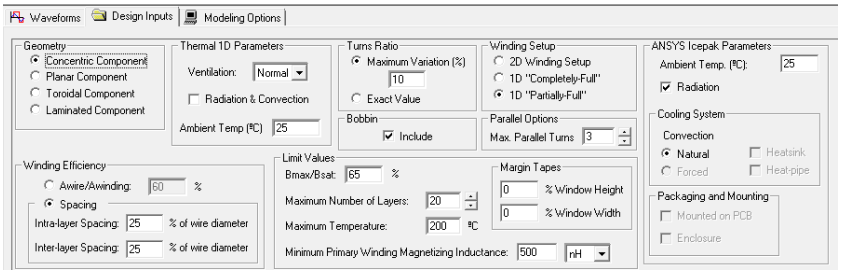


Figure A.3: Design inputs

A.4. Modeling options

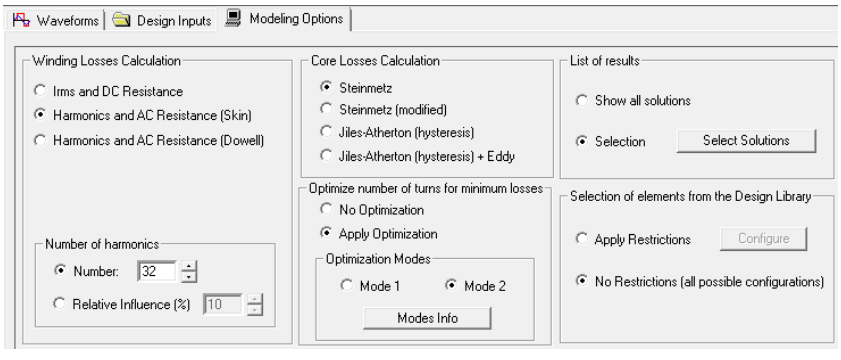
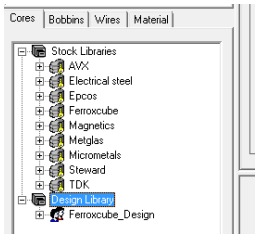
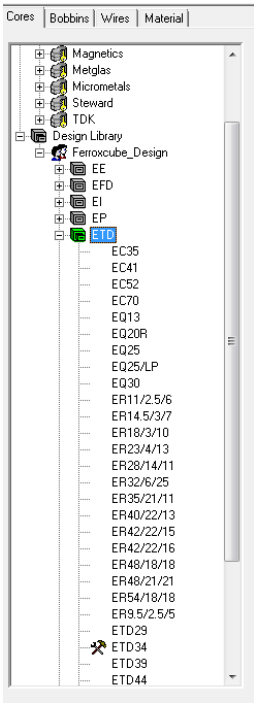


Figure A.4: Modeling options

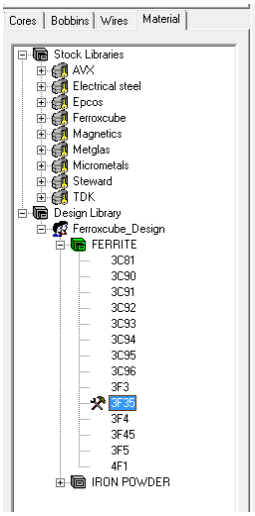
A.5. Library selection



(a) Adding stock library in design library



(b) Selecting core size



(c) Selecting core material

Figure A.5: Library selection

A.6. Results

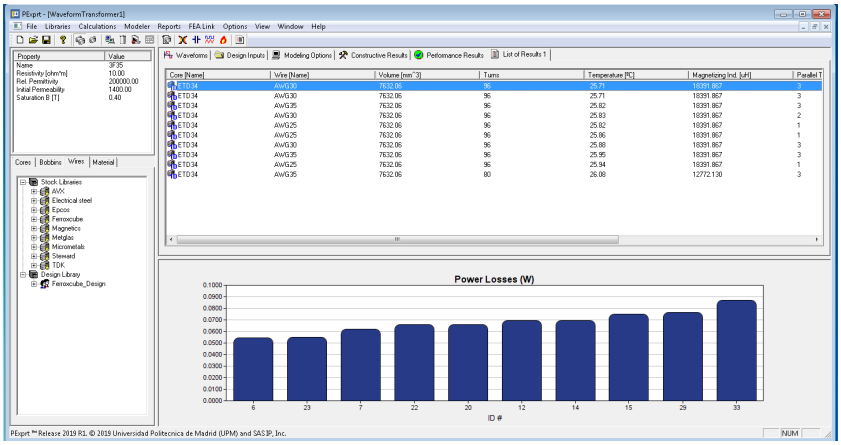


Figure A.6: List of results

A.7. Performance results

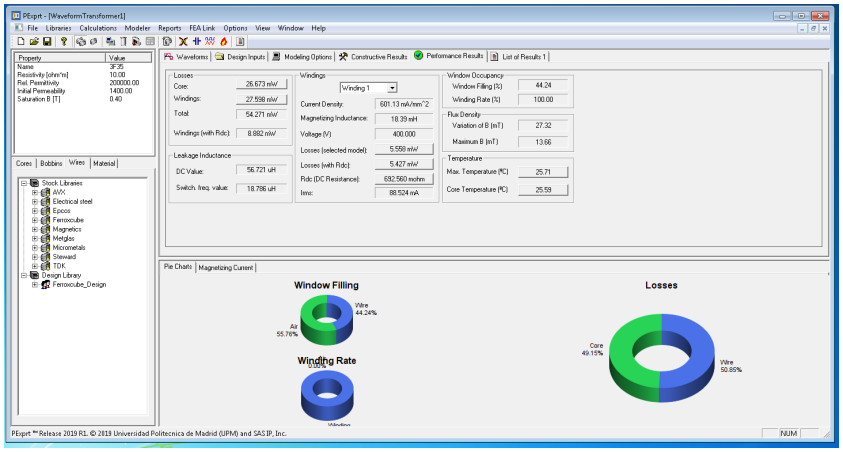


Figure A.7: Performance results

A.8. Constructive results

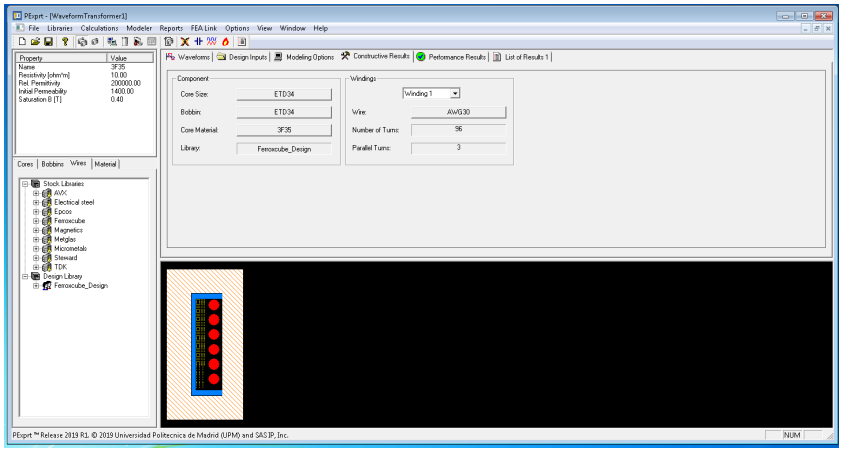


Figure A.8: Constructive results

Bibliography

[1] Sam Abdel-Rahman. Resonant llc converter: Operation and design. *Infineon Technologies North America*, 2012.

[2] Hong Huang. Designing an llc resonant half-bridge power converter. In *2010 Texas Instruments Power Supply Design Seminar, SEM1900, Topic*, volume 3, pages 2010–2011, 2010.

[3] William G Hurley and Werner H Wölfle. *Transformers and inductors for power electronics: Theory, design and applications*. John Wiley & Sons, 2013.

[4] ST Microelectronics. An introduction to llc resonant half-bridge converter. *AN2644*, 2008.

[5] Ned Mohan, Tore M. Undeland, and William P. Robbins. *Power Electronics*. John Wiley & Sons Inc, 2002. ISBN 0471226939.

[6] NXP Semiconductors. Application note tea2016. July 2018.

[7] NXP Semiconductors. *Digital controller for high-efficiency resonant power supply, Objective data sheet*. NXP Semiconductors, July 2018. Rev. 1.

[8] Bo Yang. *Topology investigation of front end DC/DC converter for distributed power system*. PhD thesis, Virginia Tech, 2003.

[9] Jun Zhang, William Gerard Hurley, and Werner Hugo Wölfle. Gapped transformer design methodology and implementation for llc resonant converters. *IEEE Transactions on Industry Applications*, 52(1):342–350, 2015.

[10] Stan Zurek. Flux fringing, 2019. URL `http://www.encyclopedia-magnetica.com/doku.php/flux_fringing`.