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High-Purity Digitally Intensive Frequency Synthesis Exploiting Millimeter-Wave Harmonics

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High-Purity Digitally Intensive Frequency Synthesis Exploiting Millimeter-Wave Harmonics

Zhirui Zong

High-Purity Digitally Intensive Frequency Synthesis Exploiting Millimeter-Wave Harmonics

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on

Monday 24 June 2019 at 12:30 o'clock

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High-Purity Digitally Intensive Frequency Synthesis Exploiting Millimeter-Wave Harmonics,
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Keywords: frequency synthesizer, all-digital phase-locked loop (ADPLL), oscillator, frequency multiplier, frequency divider, harmonic extraction, flicker noise, transformer, millimeter-wave.

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"Simplicity is the ultimate sophistication."

Leonardo da Vinci, 1452-1519

Contents

Chapter

1

Introduction

Recent years have witnessed the blooming of emerging applications, such as 5G wireless communications [1], wireless backhaul, wireless virtual reality (VR) and augmented reality (AR) [2], ultra-high definition multimedia information transmission (e.g., 1080p HD video requires speed of many Gb/s). They all place demands for high data-rate wireless links. As indicated by Shannon theorem, the maximum achievable communication data capacity is proportional to the spectrum bandwidth. In a related field, radars for autonomous driving also require large chirp bandwidth for fine range resolution [3]. Fig. 1.1 illustrates some of these application scenarios.

The low-frequency spectrum (i.e., $<6\,\mathrm{GHz}$) is very crowded and just about to be used up today. It cannot afford the ever-increasing demands for bandwidth. There is a shortage of the low-frequency spectrum to support these emerging applications that may require large spectrum bandwidth. Millimeter-wave frequencies start to catch the eye. This part of the spectrum was seldomly used simply because of the technology limitations. The electronic systems

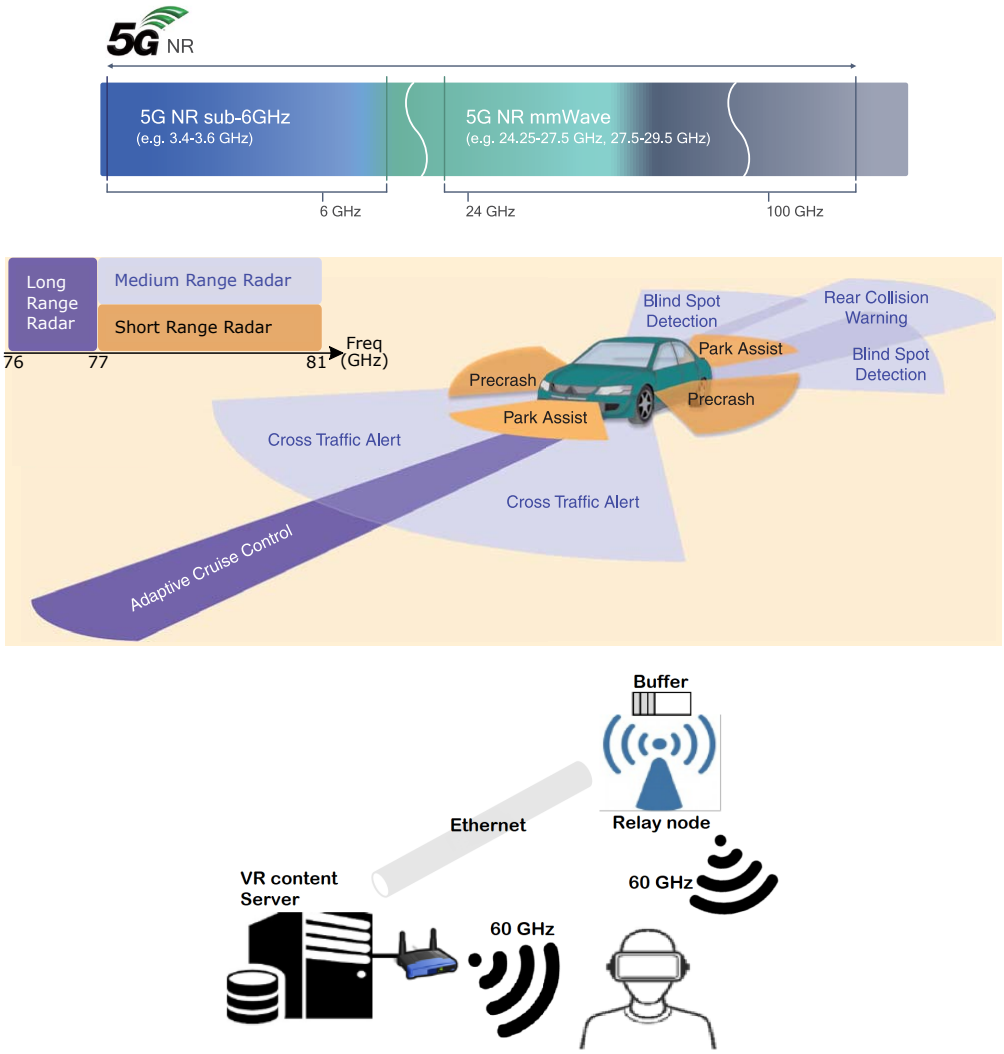


Figure 1.1: Emerging wireless applications that exploit mm-wave spectrum.

operating at such high frequencies were primarily implemented in special technologies, such as GaAs, InP and SiGe, which limit the integration level and are expensive as well. With the rapid advance of CMOS technologies, the cut-off frequency (f_T) of nanometer CMOS keeps on increasing dramatically. Fig. 1.2 summarizes the roadmap of f_T growth over the technology nodes from 0.35 um to 28 nm. As we can see, f_T is close to 300 GHz in 40 nm CMOS, and it exceeds 300 GHz in 28 nm. The advanced CMOS technology is now fast enough to support mm-wave applications. It paves the way to affordable commercial mm-wave applications. The breakthroughs in semiconductor technologies opens the mm-wave spectrum to these emerging applications.

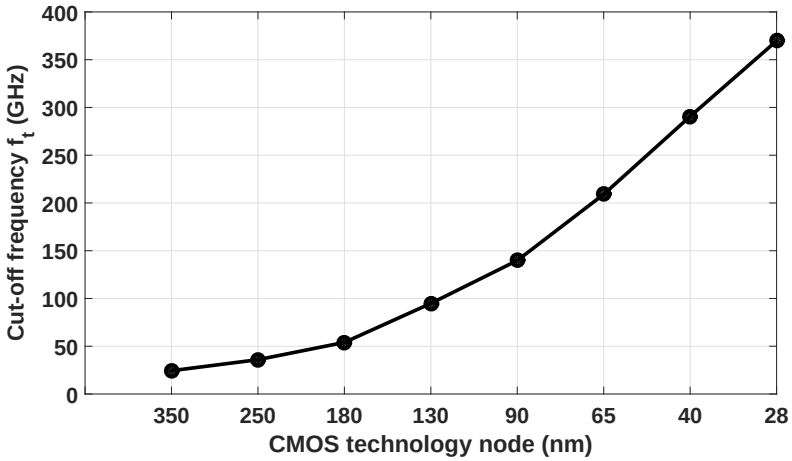


Figure 1.2: Transistor cut-off frequency with the advancement of CMOS technology.

As shown in Fig. 1.3, the data rate in wireline, wireless and cellular communications is consistently growing by about 10 times per 5 years [4]. However, the battery technology has not advanced so aggressively in the meantime. The battery capacity of the smart phones has only increased by around 30% over the last 5 years, as shown in Fig. 1.4 [5]. Though these wireless terminals are getting ever more advanced and powerful, they are limited by the power consumption. To have a long battery lifetime, an ever-decreasing energy per bit is required in the emerging mm-wave communication systems. The power budget in automotive radars is not so strict as in portable terminals. However, too much power dissipation on a small chip area can dramatically heat up the devices and increase the die junction temperature. It could cause thermal reliability issues, especially at the high side of the automotive operating temperature (-40–125°C). Therefore, good power-efficiency is desired in automotive radar systems as well.

On the other hand, the performance requirement on mm-wave transceivers is very demanding. In the communication systems, for certain modulation schemes and data rate, there are minimum requirements on the signal-to-noise ratio (SNR) or error-vector magnitude (EVM) in the transmitters and receivers. In mm-wave radar applications, the detection range and accuracy is dependent on the SNR of the radar transceiver. To achieve long detection range with acceptable resolution, a high SNR is required. The SNR or EVM

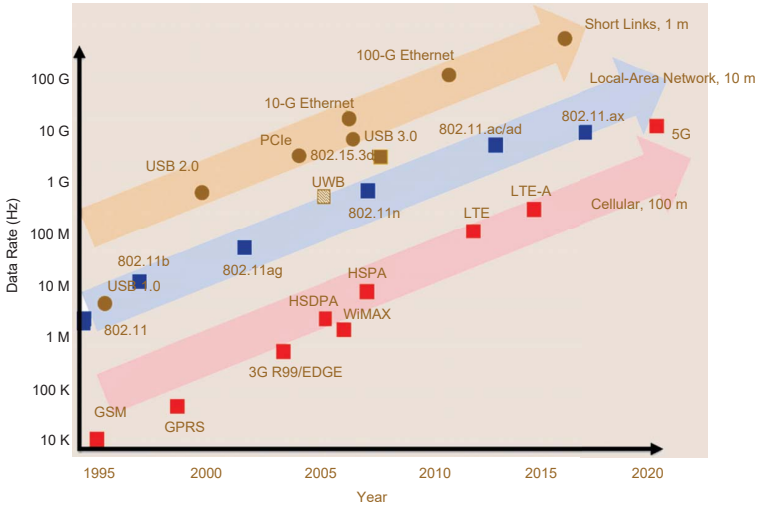


Figure 1.3: Data rate trends in wireline, wireless and cellular communications [4].

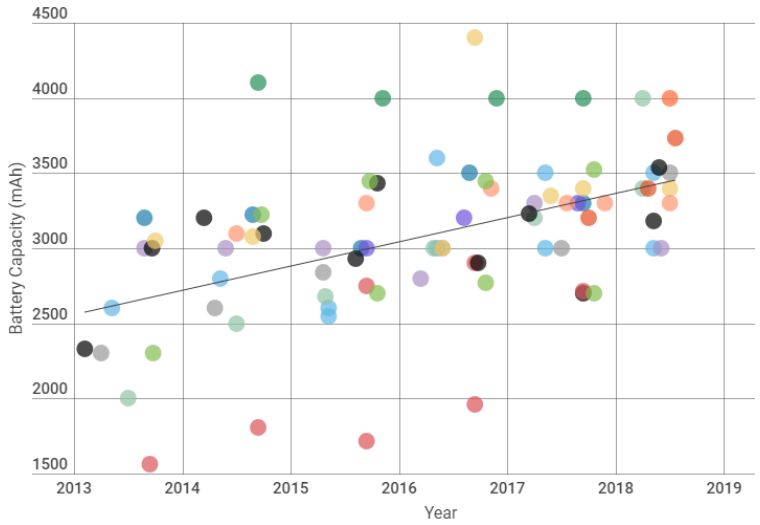


Figure 1.4: The increment of smart phone battery capacity with time [5].

sets an upper bound on the performance of each subsystem in the mm-wave transceivers.

Frequency synthesizers are key subsystems in RF/mm-wave transceivers. In communication systems, they act as the local oscillators (LOs) to deliver the carrier signal for frequency up/down-conversion. In some applications (such as FMCW radars), the frequency synthesizers also function as the frequency/phase modulators. Phase-locked loops (PLLs) are routinely used for frequency synthesis in RF/mm-wave transceivers. Phase noise of the frequency synthesizers degrades the SNR or EVM of the transceivers. Among

many impairments (such as I/Q mismatch and noise of the front-end circuits) in mm-wave transceivers, phase noise is often the dominant constraint on the system SNR [6] [7]. Therefore, it is crucial to maintain the phase noise of the frequency synthesizers low in high-performance mm-wave transceivers. For example, in the IEEE 802.11ad standard, the transmitter EVM specification for single-carrier 16QAM is -21 dB. It requires the 60 GHz frequency synthesizers to achieve less than 230 fs rms jitter. This requirement can be slightly relaxed when wideband carrier tracking loops are available in the baseband circuitry. Power consumption in the mm-wave frequency synthesizers is typically high. It can take up a relatively large portion in the overall power budget of the transceivers. Fig. 1.5 summarizes the power consumption of the frequency synthesizers in several 60 and 77 GHz transceivers in recent publications [8] [9] [10] [11]. It spans from 73 to 284 mW, and is 20-68% of the total power consumption in the TXs or RXs.

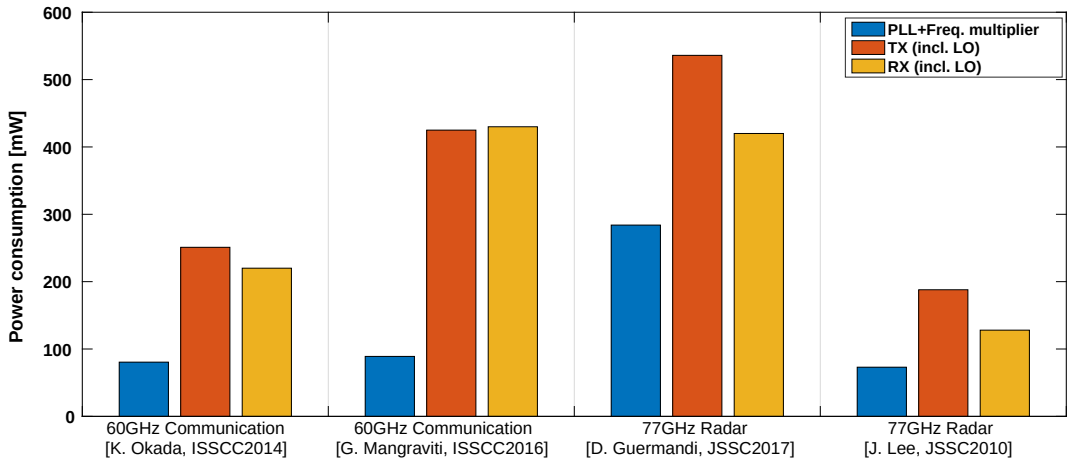


Figure 1.5: Power consumption of frequency synthesizers in mm-wave transceivers.

This dissertation aims to develop a new frequency synthesizer architecture for mm-wave frequencies and innovate the sub-blocks for lower phase noise and better power efficiency than that of the traditional solutions.

1.1 Millimeter-Wave Design in Nanometer CMOS: Challenges and Opportunities

As predicted by the famous Moore's law, the CMOS technology has been rapidly improving towards finer feature size. There are already commercial processor chips developed in 7 nm CMOS [12]. The advance in CMOS technology is mainly motivated by the size and cost reduction in digital circuits. Despite the significant advantages in digital designs, the nanometer CMOS is a double-edged sword to analog and RF/mm-wave integrated circuits. It provides new opportunities, but also poses severe challenges, especially to analog and RF/mm-wave designs.

1.1.1 Challenges

As mentioned above, the high cut-off frequency in nm CMOS has paved the way to mm-wave designs in silicon. However, the maximum cut-off frequency (f_T) is still limited to around 300 GHz. Operating at frequencies that are not faraway from f_T (especially at 60 GHz or above), the mm-wave circuits have to overcome the speed limitation of CMOS technologies. Furthermore, the parasitic capacitance associated with the interconnects does not scale down dramatically with the advancements of CMOS. More current consumption or even inductive peaking is necessary for the circuits to operate at high frequencies. For example, frequency dividers in mm-wave PLLs suffer from this penalty. They are typically power hungry and/or occupy large silicon area when inductors are used.

Along with the ever-advancing CMOS technology nodes, the supply voltage (VDD) has to keep on decreasing for reliability concerns. It is around 1 V or even less beyond the 28 nm node. The dynamic range in analog circuits reduces accordingly. The charge pumps in analog PLLs are the victims of this factor. Also, it becomes more difficult to achieve large signal power due to the limited voltage swing. This is crucial for the oscillators, and can potentially degrade the phase noise. The channel length modulation effects are aggravated

in nanometer CMOS. They reduce the output resistance of MOSFETs and affect the performance of many analog circuits (such as current sources).

Flicker noise is one of the key impairments in analog and RF designs. It dominates the low-frequency noise spectrum of CMOS transistors. In RF VCOs, the flicker noise is upconverted to phase noise at low frequency offset from the carrier through various mechanisms. Flicker noise is exacerbated with the scaling of CMOS technology. High-k material, which is widely used to reduce the leakage current in nanometer CMOS, increases the trap density [13]. Halo doping, which is applied to mitigate the short-channel effects, creates nonuniform threshold across the channel [14]. These effects become prominent in advanced CMOS technologies and degrade the flicker noise performance. Besides the process dependent factors, the flicker noise level is also inversely proportional to the channel area of the transistors [15]. For the highest f_t, mm-wave circuits are typically designed with transistors at the minimum channel length allowed in the technologies. Less channel area is required in smaller technology nodes to achieve the same transconductance gain at the same bias conditions. It leads to higher $1/f$ noise. Mm-wave design in nanometer CMOS therefore suffer from severe flicker noise degradation.

On-chip passive devices, such as inductors and capacitors, are widely used in RF/mm-wave circuits. Quality (Q)-factor is a key metric for the inductors and capacitors. It determines the phase noise of LC oscillators and insertion loss of matching networks. For spiral inductors, the Q-factor (Q_L) at low frequencies is determined by ohmic losses in the metal trace and increases proportionally to the frequency. As the frequency goes up, skin and proximity effects start to reduce the effective cross-section area of the inductor traces thus increasing the ohmic losses. The substrate losses also become prominent at mm-wave frequencies, especially in nanometer CMOS. The top metal layers, which are typically used as inductor traces, get closer to the substrate with technology scaling. As a result, the Q-factor tends to decrease at high frequencies. On the other hand, the Q-factor (Q_C) of the metal-oxide-metal (MOM) capacitors and varactors is inversely proportional

to frequency. In 28 nm CMOS, a 100 fF MOM capacitor has a Q-factor of 400 at 2.4 GHz, but it drops to 15 at 60 GHz. The overall Q-factor (Q_T) of the LC tank is determined by the lowest Q component (i.e., $1/Q_T = 1/Q_L + 1/Q_C$). At single GHz, Q of the inductor dominates the Q of the LC tank. However, in the mm-wave regime, it is in the opposite situation. Q of the tank capacitance becomes so low that it limits the Q of the LC tank. There exists a peak Q_T in the frequency range where this transition happens (typically in 10-20 GHz range in 40 and 28 nm CMOS). As a result, the mm-wave oscillators normally have a worse figure-of-merit than the oscillators operating at lower frequencies.

1.1.2 Opportunities

Despite the evident challenges in the mm-wave design, the advanced CMOS technologies offer several key advantages. The MOS transistors in nanometer CMOS exhibit excellent switching characteristics. For switched capacitors which are widely used as frequency tuning elements in mm-wave circuits, with the same Q-factor, larger C_{max}/C_{min} ratio can be achieved at finer CMOS nodes. This implies wider frequency tuning range in mm-wave oscillators. Meanwhile, the speed of inverters and other logic gates are significantly improved by technology scaling. In 28 nm CMOS, the minimum delay of a single inverter can be below 10 ps. It can naturally provide better resolution for time-domain signal processing. This gives one way to obviate the analog imperfections in nanometer CMOS. One such example is an all-digital PLL (ADPLL) [16]. The rapid improvement in time-domain resolution has brought close the performance gap between the ADPLLs and analog PLLs. These improvements have made it promising to achieve high performance in mm-wave frequency synthesizers by embracing the digitally intensive solution.

1.2 Thesis Objectives

From the aforementioned background information, we can perceive that the performance and power efficiency of the mm-wave frequency synthesizers

suffer from many physical and circuit-level bottlenecks to support emerging applications. To realize such high-performance mm-wave frequency synthesizers with good power efficiency in nanometer CMOS, new concepts and theory must be introduced to overcome those limitations. The objective of this thesis is to develop a new architecture for mm-wave frequency generation to achieve such a goal. Consequently, a proof-of-concept will be demonstrated in this thesis for low-power and low-noise fractional-N digital frequency synthesis at mm-wave band.

To achieve this goal, the performance-limiting sub-blocks need to be identified and significantly improved. The oscillators, frequency prescalers and/or frequency multipliers make up the main differences between mm-wave and single-GHz frequency synthesizers. As discussed in Section 1.1.1, the lossy LC resonator and exacerbated flicker noise in nanometer CMOS transistors deteriorate the phase noise of mm-wave oscillators. This thesis will systematically investigate such effects and introduce new solutions to reduce the phase noise. Low noise is often at the cost of high power consumption. However, for those sub-blocks that are not the dominant noise contributors, their power consumption cannot be traded off straightforwardly with the noise performance of the mm-wave frequency synthesizers. To improve the power efficiency, it is desired to reduce or even eliminate the power budget of these circuits. The frequency prescalers and multipliers fall into this category. This thesis will explore in the direction towards minimizing power consumption in the frequency prescalers and multipliers.

1.3 Organization of the Thesis

This thesis is organized as follows. Chapter 2 gives an overview on the fundamentals and evolution of the mm-wave frequency synthesis. Several frequency synthesis architectures that are applicable at mm-wave bands are presented, with a discussion on their advantages and drawbacks. Physical and circuit-level constraints on mm-wave PLLs are also summarized.

Chapter 3 introduces the concept of a new frequency synthesizer architecture for mm-wave applications. Lying at its heart is an oscillator with inherently implicit frequency tripling. It is capable of generating both the fundamental and strong third harmonic signals simultaneously. This chapter mainly focuses on the third harmonic boosting and extraction techniques. A comprehensive analysis is given on the operational principles and trade-offs. A 20 GHz oscillator with implicit frequency tripler is prototyped in 40 nm CMOS. The measured phase noise is better than -98.8 dBc/Hz at 1 MHz offset from 60 GHz carrier. The figure-of-merit (FoM) advances the state-of-the-art by 3 dB.

Chapter 4 investigates the mechanisms of flicker noise upconversion to phase noise (i.e., $1/f^3$ noise) in the oscillators and their suppression techniques. The $1/f^3$ noise in the oscillators is identified to have a significant impact on the performance of low-noise mm-wave PLLs. Two flicker noise upconversion mechanisms are discovered and verified: direct and indirect upconversion. Possible suppression techniques to different upconversion mechanisms are presented. A generic flicker noise upconversion suppression technique is proposed accordingly. This technique is applied to a 20 GHz digitally-controlled oscillator (DCO) with implicit tripling and prototyped in 28 nm CMOS. The measured $1/f^3$ corner is 300–400 kHz, which is record-low compared to CMOS oscillators at 20 GHz and above.

Chapter 5 describes the implementation of a low-noise fractional-N digital frequency synthesizer for mm-wave applications. The architectures and techniques proposed in Chapters 3 and 4 are exploited in this 60 GHz frequency synthesizer. Mm-wave frequency prescalers and multipliers are not physically needed any more in this implementation. A sigma-delta modulated digital-to-time converter (DTC) and a time-to-digital converter (TDC) comprise the phase detection circuit. The undesired 20 GHz tone from the oscillator is suppressed by a soft-cancellation technique in the 60 GHz output buffer. Design considerations for frequency dividers and digital loop filters are also detailed. Experimental results of this 60 GHz frequency synthesizer in 28 nm

CMOS are presented.

Finally, chapter 6 concludes this thesis with some recommendations for future work.

Chapter

2

Overview of Millimeter-Wave Frequency Synthesis

This chapter gives a brief overview of the mm-wave frequency synthesizers. Section 2.1 goes through the fundamental knowledge of the PLLs and compares the differences between analog and digital PLLs. Different architectures of mm-wave frequency synthesizers are reviewed in Section 2.2. Finally, phase noise performance of the mm-wave PLLs and the noise contributors are analyzed in Section 2.3.

2.1 PLL Fundamentals

Phase-locked loops are negative-feedback control systems. As shown in Fig 2.1, a PLL typically consists of several major building blocks: an oscillator, a phase/frequency detector (PFD), a loop filter (LF), frequency dividers and a reference clock. The oscillator output is scaled by the frequency divider and then compared with the reference clock via the PFD. The detected difference represents the phase error. After being filtered by the LF, it gives the correction input to the oscillator. In this way, the phase of the oscillator tracks that of the reference clock. The output frequency is set by the division ratio, i.e., $f_{out} = N \cdot f_{ref}$. N can be an integer or fractional number. Due to the higher frequency resolution, fractional-N PLLs offer more flexibility than integer-N PLLs in applications.

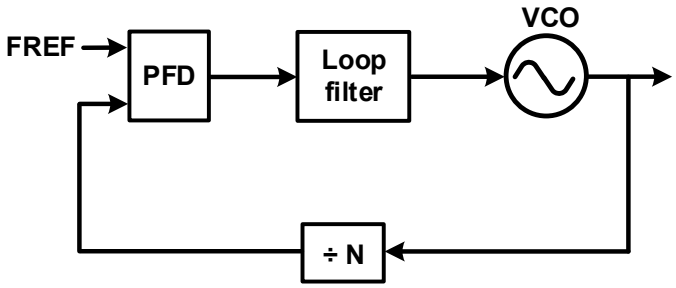


Figure 2.1: Simplified block diagram of a general PLL.

Depending on the loop filter configuration, the PLLs can be categorized into different types and orders. The number of poles in phase-domain close-loop transfer function determines the order. The type is defined by the number of poles at DC (i.e., integrators). The oscillator is an integrator in phase domain. If there is no integrator (pole at DC) in the loop filter, the PLL is of type I. With one integrator in the loop filter, it is of type II. In type-II PLLs, the phase relationship between the reference clock and oscillator output is held constant. This is an important feature in some applications.

2.1.1 Analog PLLs

A traditional PLL implementation is the charge-pump based analog PLL. Fig. 2.2 shows a typical type-II analog PLL. The loop filter is fully composed of resistors and capacitors. The oscillator frequency is controlled by analog voltage (i.e., VCO). The VCO output is scaled by a multi-modulus divider (MMD), which is controlled by a sigma-delta modulator ($\Sigma\Delta$M). The PFD produces UP and DOWN pulses whose width represents the phase error between the MMD output and the reference clock. The UP/DOWN pulses control the charge pump to sink current into/from the loop filter. $C_1 + C_2$ in the LF integrates the pulse current and provides a pole at DC. R_1 acts as lossy element to the integrator C_1. R_1 in combination with C_1 provides a left-plane zero to stabilize the feedback loop. C_1 is typically large to keep the loop bandwidth low, filter out ripples/noise on the control line and to ensure good phase margin. C_2 in combination with R_1 suppresses the high frequency ripples caused by the instantaneously injected current pulses.

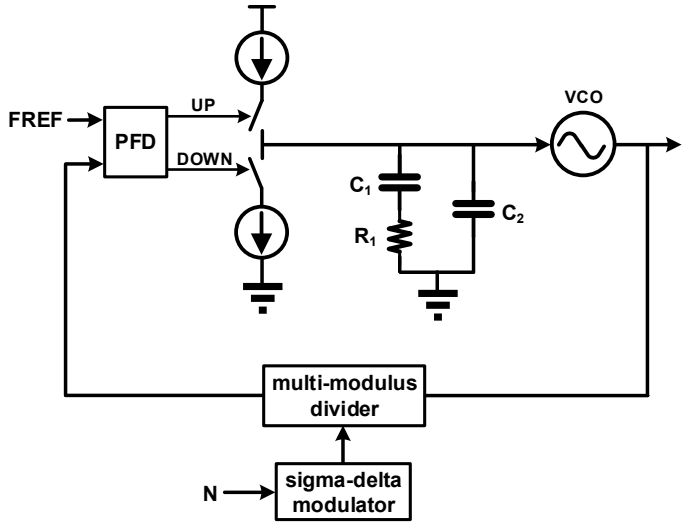


Figure 2.2: Block diagram of a typical type-II analog charge-pump PLL.

The performance of charge-pump based PLL suffers from many analog imperfections. The UP and DOWN current sources are typically made of PMOS and NMOS transistors, respectively. Mismatch between them is unavoidable, and it can introduce spurs. The charge pump and resistor in the

loop filter produce noise and contribute to the phase noise of the PLL. The charge pump is expected to deliver current that is linearly proportional to the phase error. However, it can never be perfectly linear. Mechanisms, such as charge redistribution and channel length modulation, degrade the linearity. The channel length modulation effects cannot be improved with advanced CMOS technologies, but actually get worse. The nonlinearity in charge pump can fold the ΣΔM quantization noise to low frequencies and raise up the phase noise. Also, these analog designs cannot be easily ported to new technology nodes. As mentioned in Chapter 1, the dynamic range of the charge pump output voltage is reduced in nanometer CMOS. To cover a certain frequency range by the varactor in the VCO, a larger K_{vco} is needed. It facilitates the circuit noise to phase noise upconversion. To achieve a loop bandwidth of several hundred kHz or lower, the total capacitance in the loop filter should be at a level of several hundred pF or nF. For monolithic integration, such large capacitance would occupy very large chip area. It simply does not scale with the advancement of CMOS technology.

2.1.2 Digital PLLs

In contrast, all-digital PLLs (ADPLL) can avoid the analog imperfections. In an ADPLL, the time-to-digital converter (TDC) and digitally controlled oscillator (DCO) replace the charge pump and VCO, respectively. There are two ADPLL architectures that are commonly used. Fig. 2.3 shows a simplified block diagram of a counter-based ADPLL. The counter counts the number of accumulated rising edges of the DCO output signal CKV (i.e., PHV_I). The TDC measures the phase difference between the FREF and the closest CKV rising edge and generates the fractional phase information of the CKV (i.e., PHV_F) that cannot be detected by the counter. The combined counter and TDC output represents the variable phase information (i.e., PHV). Phase error PHE is the difference between PHV and PHR, which is the accumulation of FCW on every FREF cycle. It is encoded in digital domain. The digital LF filters the PHE and its output is converted to

digital tuning bits that control the DCO. The bulky analog loop filter is thus avoided. Digital loop filter also provides better reconfigurability. It is typically composed of a proportional-integral (PI) controller and a multistage cascaded infinite impulse response (IIR) filter. It can be dynamically programmed between type-I and type-II, as well as in other loop parameters during the normal operation without any disturbance. Locking/resettling time can be accelerated through gear shifting of the digital loop filter bandwidth. The DCO tuned by digitally controlled switched-capacitors has relatively smaller K_{vco} (the parasitic nonlinear capacitance of the cross-coupled pair still remains). Therefore, it has a better immunity to AM-PM conversion. Circuit noise upconversion to phase noise through this effect is lower. A $\Sigma\Delta$M is typically applied on the least significant bits (LSB) of the DCO to achieve fine frequency resolution.

The other commonly used architecture of ADPLL is divider-based, as shown in Fig. 2.4. The operation principle is similar to the analog PLL in Fig. 2.2. The DCO output is scaled down to FREF frequency by a $\Sigma\Delta$ modulated MMD. The TDC measures the phase difference between the MMD output and FREF. If the $\Sigma\Delta$ modulator is first-order, the required TDC range (after full settling) is one CKV period, which is the same as that in the former ADPLL architecture. In case of a higher-order modulator, the TDC needs to cover a range of several CKV periods.

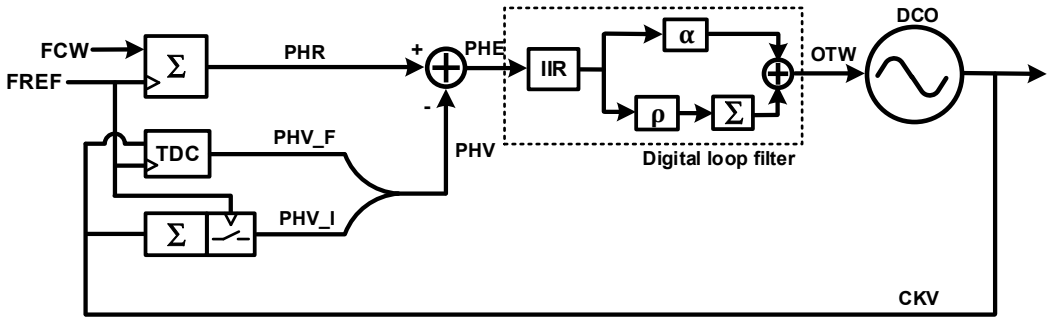


Figure 2.3: Counter-based ADPLL architecture.

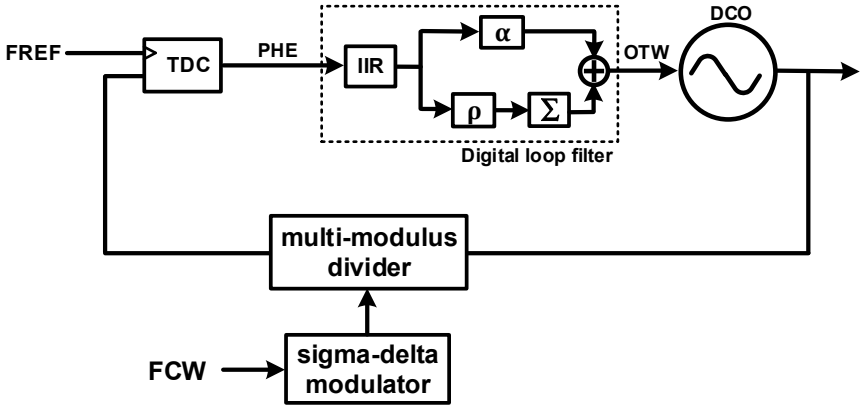


Figure 2.4: Multi-modulus divider based ADPLL architecture.

2.2 Architectures for mm-Wave Frequency Synthesizers

As discussed in Chapter 1, the design of mm-wave circuits suffers from many challenges. Due to those limitations, mm-wave frequency generation in CMOS typically suffers from poor PN, limited TR and high power consumption [17–22]. There have been continuous efforts to explore new solutions and implementations for mm-wave frequency synthesis. Several mm-wave frequency synthesizer architectures have been reported in literature. They can be categorized into three groups [20]: a PLL with a fundamental oscillator [17–20], a low-frequency PLL together with a frequency multiplier [21–23], and a PLL with N-push oscillators [24–26]. Fig. 2.7 shows these three architectures in the case of 60 GHz frequency generation.

In the first architecture [Fig. 2.7(a)] [17–20], the mm-wave oscillators and high-frequency dividers are the key design challenges [27–32]. The difficulties of 60-GHz oscillators are: 1) the parasitic capacitance of active devices takes up a large share of the relatively small tank capacitance, thus limiting the frequency tuning range; 2) to achieve a tuning range of >15%, the poor Q-factor of the tuning capacitance dominates the Q-factor of the 60 GHz resonator, thus limiting the achievable PN. Compared to the LC tank at lower frequencies, the LC resonators at mm-wave frequencies exhibit lower Q-factor

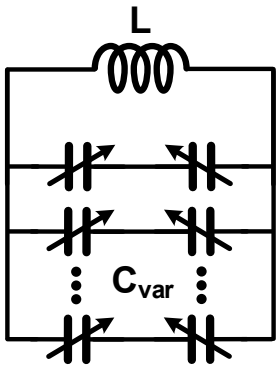


Figure 2.5: The LC tank configuration to characterize its Q-factor at different resonant frequencies.

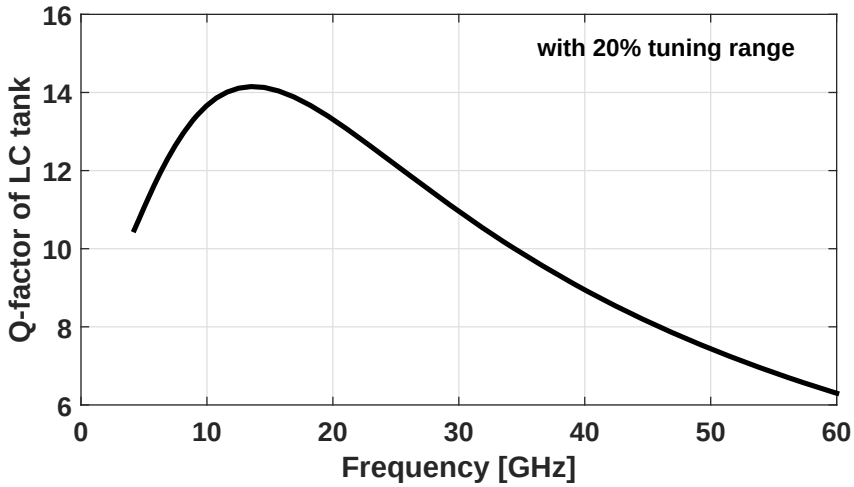


Figure 2.6: Q-factor of the LC tank at different resonant frequencies in 28 nm CMOS.

for the same tuning range. An LC tank is configured in TSMC 28 nm CMOS to investigate the variation of its Q-factor at different resonant frequencies, as shown in Fig. 2.5. The inductance and number of varactors are swept to resonate at frequencies ranging from 4 to 60 GHz, while C_{max}/C_{min} ratio of the varactor is kept constant to maintain the same normalized frequency tuning range (20%). Q-factor of the LC tank is extracted from its 3-dB bandwidth and shown in Fig. 2.6 at various different resonant frequencies. As we can see, with a tuning range of 20%, the Q-factor of the LC resonator peaks between 10–20 GHz. According to this figure, a 20 GHz LC tank has a Q-factor of 13. While for a 60 GHz LC tank with the same tuning range (20%), the Q-factor drops to 6 due to the degraded Q of the tuning capacitors. According to Eq. 2.1 (Leeson Equation), the thermal noise induced phase noise is inversely

proportional to Q^2.

$$L(\Delta\omega) = 10\log_{10}\left(\frac{kT\cdot\Gamma_{rms}^2}{Q^2\cdot P_{sig}^2}\cdot NF\cdot\left(\frac{\omega}{\Delta\omega}\right)^2\right) \tag{2.1}$$

By decreasing the Q-factor from 13 to 6, the phase noise induced by the losses in the LC tank can deteriorate by 6.7 dB (referring to the same carrier frequency). The 60 GHz frequency dividers must achieve wide locking range to ensure sufficient overlap with the oscillator TR under PVT variations. However, there is a strong trade-off between the locking range and power consumption [30–32]. Recently, several injection-locked frequency dividers were reported with large locking range and low power consumption, but at the cost of large silicon area [33, 34]. In many cases, the power dissipated by the frequency dividers is a large part of the total power consumed by the mm-wave PLLs. Fig. 2.8 summarizes the power consumption of several 60 GHz PLLs in the literature. As we can see, 24%-58% of the power consumption in the PLLs is contributed by the frequency dividers. It is desired to significantly reduce this from the power budget.

The aforementioned design challenges in the oscillators and frequency dividers are relieved in PLLs based on frequency multipliers [Fig. 2.7(b)] [21–23]. This solution can improve the phase noise performance. However, the 60-GHz frequency multipliers in this architecture typically have limited locking range, or consume large power in order to achieve large locking range [23, 35–37]. The design challenges remain, but are shifted from mm-wave frequency dividers to frequency multipliers. In PLLs with N-push oscillators (as shown in Fig. 2.7(c) for N =2) [24–26], the frequency dividers operate at $60/N$ GHz, and frequency multipliers are avoided. However, this oscillator type suffers from low output power and mismatches among the N oscillators if $N > 2$. Among this type, push-push oscillators are the most common and easiest to implement. However, the required large common-mode (CM) swing can increase the 1/f noise up-conversion [38]. Moreover, the conversion from single-ended CM signal to a differential output may introduce

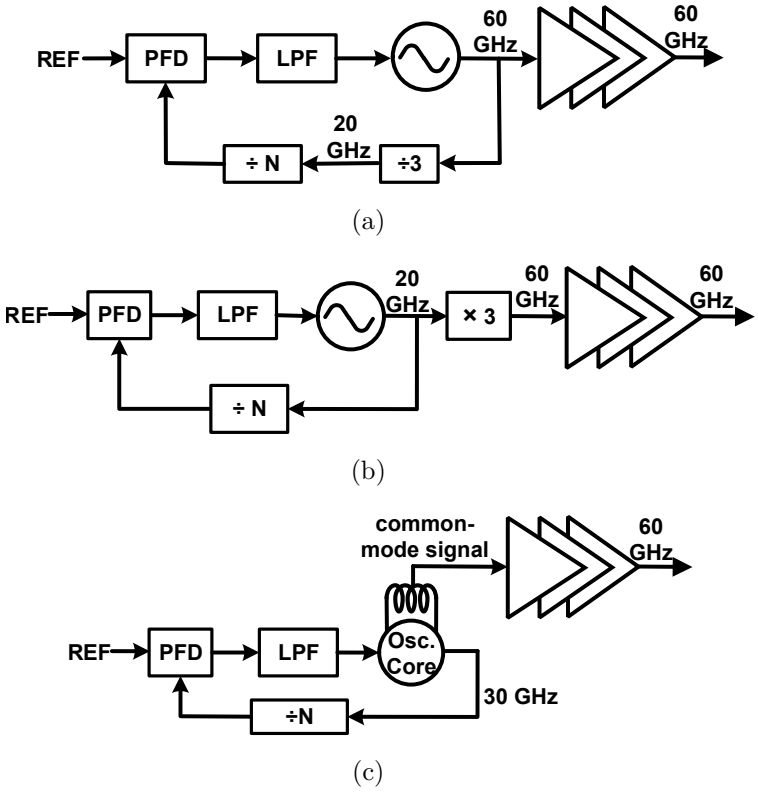


Figure 2.7: Evolution of the mm-wave PLL architectures (a): PLL with fundamental oscillator; (b): PLL with frequency multiplier; (c): PLL with push-push oscillator.

large phase error [24].

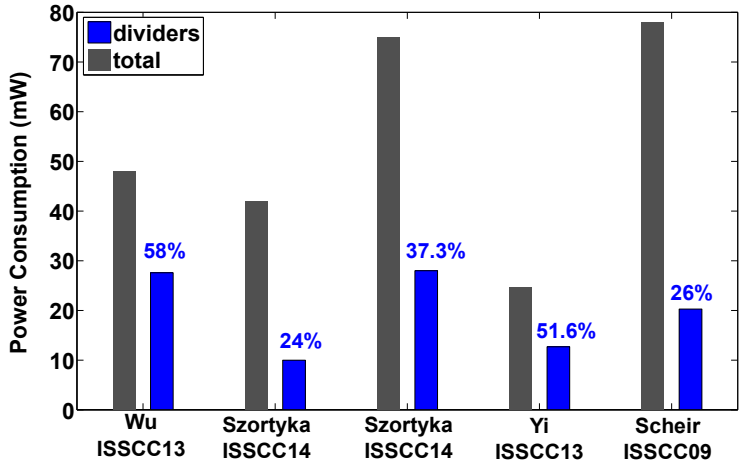


Figure 2.8: Power consumption of frequency dividers in several recently published 60 GHz PLLs.

The evolution of mm-wave frequency synthesizers reaches a consensus that the oscillators should operate at low frequencies for good phase noise.

However, the existing solutions have not broken through the trade-off between power efficiency and phase noise. This calls for new architectures that enable power-efficient low-noise mm-wave frequency generation.

2.3 Phase Noise in mm-Wave PLLs

All the noise sources in the PLL contribute to the output phase noise. They experience, though, different transfer functions to the output. In most digital PLLs, the major noise contributors are the DCO phase noise, TDC quantization noise and FREF noise floor. The contribution from other noise sources (such as noise floor of the frequency dividers) can be maintained much lower in typical designs.

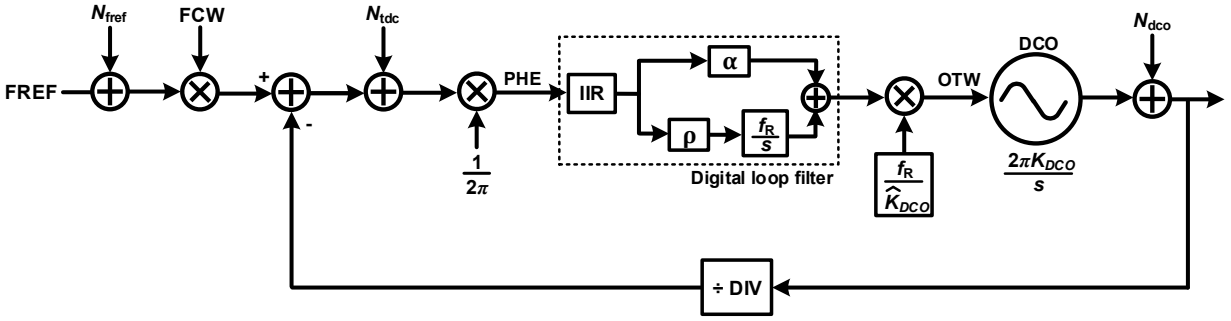


Figure 2.9: Linearized s-domain model of an ADPLL with noise sources.

Fig. 2.9 shows an s-domain linear model of the ADPLL with noise sources. The open-loop transfer function is

$$H_{ol}(s) = \frac{1}{DIV}\left(\alpha + \frac{\rho}{s}\right) H_{IIR}(s) \cdot \frac{f_R}{s} \tag{2.2}$$

$H_{ol}(s)$ is a low-pass-filter function. The phase noise introduced by the TDC quantization noise and FREF noise floor is, respectively,

$$L_{fref}(\Delta f) = FCW \cdot N_{fref}(\Delta f) \cdot \frac{DIV \cdot H_{ol}(s)}{1 + H_{ol}(s)}\Big|_{s=j2\pi\Delta f} \tag{2.3}$$

$$L_{tdc}(\Delta f) = N_{tdc}(\Delta f) \cdot \frac{DIV \cdot H_{ol}(s)}{1 + H_{ol}(s)}|_{s=j2\pi\Delta f} \tag{2.4}$$

Both are low-pass filtered by the loop. They directly contribute to the in-band phase noise without any suppression from the loop filter. The DCO phase noise is high-pass filtered by the loop. Its contribution to the output is

$$L_{dco}(\Delta f) = N_{dco}(\Delta f) \cdot \frac{1}{1 + H_{ol}(s)}|_{s=j2\pi\Delta f} \tag{2.5}$$

Among the three major noise sources, the DCO phase noise and TDC quantization noise are design choices that offer certain flexibilities. They usually can be traded off with power consumption. FREF noise floor is predefined by the external crystal clock. Since the TDC quantization noise contributes to the PN in the same way as the FREF noise, significantly improving TDC quantization noise below the FREF noise floor cannot improve the PN anymore. For the best power efficiency, TDC quantization noise should be at comparable level as the FREF noise.

The low-frequency DCO phase noise is attenuated by the loop. It is desirable to have negligible contribution to the in-band PN. The $1/f^2$ phase noise (i.e., 20 dB/dec region) can be improved by several approaches, such as enhancing the Q-factor of the LC tank or increasing the power consumption. The $1/f^3$ noise typically dominates the DCO phase noise at low frequencies. It is even more prominent in the nanometer CMOS, as discussed in Chapter 1. Unlike the $1/f^2$ noise, the $1/f^3$ noise cannot be easily reduced through these methods. In CMOS mm-wave oscillators, the $1/f^3$ corner is typically >1 MHz. If the optimal loop bandwidth is much narrower than the corner frequency, the $1/f^3$ noise has significant contribution to the output phase noise. This is true in many cases, since narrow bandwidth is required to suppress the fractional spurs and filter out FREF noise and TDC quantization noise. To achieve the ultra-low noise mm-wave frequency synthesis in nanometer CMOS, the $1/f^3$ noise in the oscillators needs to be improved.

Chapter

3

Oscillator with Implicit Frequency Multiplication

This chapter proposes a mm-wave frequency generation technique that improves its phase noise performance and power efficiency. The main idea is that a fundamental 20 GHz signal and its sufficiently strong third harmonic at 60 GHz are generated simultaneously in a single oscillator. The desired 60 GHz LO signal is delivered to the output, while the 20 GHz signal can be fed back for phase detection in a phase-locked loop. Third-harmonic boosting and extraction techniques are proposed and applied to the frequency generator. A prototype of the proposed frequency generator is implemented in 40 nm CMOS. It exhibits phase noise of -100 dBc/Hz at 1 MHz offset from 57.8 GHz and provides 25% frequency tuning range. The achieved figure-of-merit is between 179 and 182 dBc/Hz.

3.1 Introduction

As discussed in Chapter 2, the currently existing mm-wave frequency synthesizer architectures cannot achieve low phase noise at low power consumption. To alleviate the design challenges for mm-wave oscillators and frequency prescalers without shifting more stress onto other blocks, new mm-wave frequency generation techniques are required.

To achieve good phase noise in a mm-wave PLL, it is clear that the oscillator should operate at a lower frequency. Frequency multipliers remain an obstacle for improving the power efficiency and robustness in the frequency synthesizers depicted in Fig. 2.7(b). It is desired to propose a power-efficient approach to realize the frequency multiplication.

The operating principle of a conventional frequency tripler is shown in Fig. 3.1. It relies on the high-order nonlinearities of the input devices to generate the third harmonic current. The harmonic current is converted to large voltage swing through an LC tank tuned at the third harmonic frequency. Since the oscillators undergo a large-signal operation, the oscillating current is typically rich in harmonic. In conventional LC oscillators, the harmonic current is filtered out by the high-Q LC tank resonating at the fundamental oscillation frequency. It will be more power efficient if the harmonic current in the oscillator can be leveraged for frequency multiplication. Instead of regenerating the third harmonic current in the tripler, the readily-existing third harmonic current in a 20 GHz oscillator is reused for implicit frequency tripling in this design.

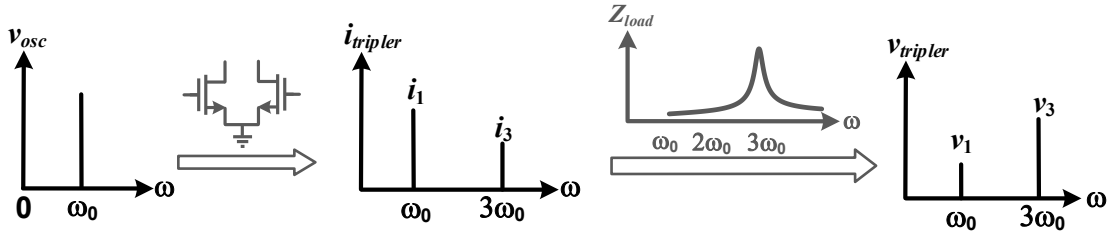


Figure 3.1: Operating principle of a conventional frequency tripler.

In principle, it is also possible to utilize higher-order (e.g., 5th order)

harmonic current in the oscillator so that the oscillator operates at even lower frequencies. However, the amount of harmonic current generated in CMOS transistors decreases dramatically with increased harmonic order. At higher-order harmonic frequencies, the harmonic current is so small that more power consumption will be consumed in the following buffer stages to amplify it and to drive the loads. It counteracts with the power consumption saved by removing the frequency multipliers. The advantage of power efficiency enhancement therefore diminishes in those cases. As a trade-off, the third-harmonic current in the oscillator is a good candidate for implicit frequency multiplication.

3.2 Implicit Frequency Multiplication in Oscillator

In order to realize frequency tripling with the readily available harmonic current in the oscillator, the LC resonator should preserve the third harmonic content instead of filtering it out. At mm-wave frequencies, a practical way of implementing it is to introduce an extra LC resonance at the third harmonic frequency in addition to the fundamental resonance.

With the aforementioned observations, a 60 GHz frequency generation technique based on a 20 GHz oscillator and an implicit $\times 3$ frequency multiplier [39, 40] is proposed in this chapter. As a result, the 60 GHz signal generated from the implicit tripler is delivered to the output, while its 20 GHz counterpart is destined to be used for phase detection in the feedback path of a PLL. Fig. 3.2 introduces a new PLL architecture that employs the proposed 20/60 GHz generator.

The basic concept of this work is to simultaneously generate both 20 GHz and a significant level of its 3rd harmonic at 60 GHz inside a 20 GHz oscillator. The generated 60 GHz signal is fed forward to a buffer with natural band-pass filtering, while the 20 GHz signal is fed back for phase detection after further frequency division, as shown in Fig. 3.2. Since buffers are typically needed for LO distribution in any mm-wave transceivers, there is no extra circuitry cost

in the proposed solution. Consequently, the ideal $\times 3$ functionality is inherent such that no physical divider or multiplier operating at the 60 GHz is needed anymore. This should lead to an improvement in the power efficiency of 60 GHz frequency synthesizers.

Since the oscillator runs at the fundamental frequency of 20 GHz, its resonant tank achieves a better Q-factor than at 60 GHz, which leads to a better PN performance. Also, the tank has a larger inductance (L) and capacitance (C). This increases the variable portion of the total tank capacitance and thus the frequency tuning range.

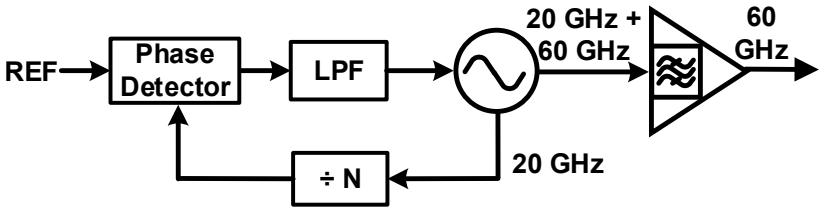


Figure 3.2: Proposed PLL with implicit frequency tripler based on harmonic boosting and extraction.

3.3 Third-Harmonic Boosting and Extraction

To co-generate strong 60 GHz component, third-harmonic boosting and extraction techniques are proposed and applied to a 20 GHz dual-resonance oscillator. The 3$^{\text{rd}}$-harmonic techniques have been exploited in single-GHz oscillators to shape the oscillation waveforms for a better PN performance [41,42]. However, instead of acting as an auxiliary therein, the 3$^{\text{rd}}$ harmonic component in our work is the signal of interest. Its direct extraction and utilization require precise control of the harmonic generation process. Therefore, a detailed insight into its operational principle will be given.

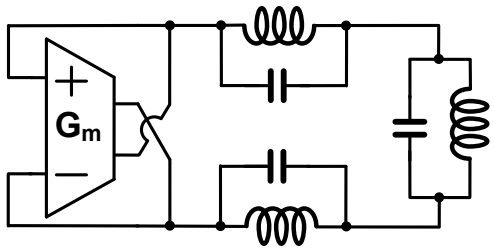
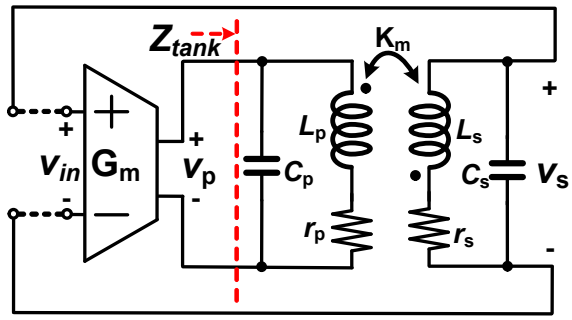


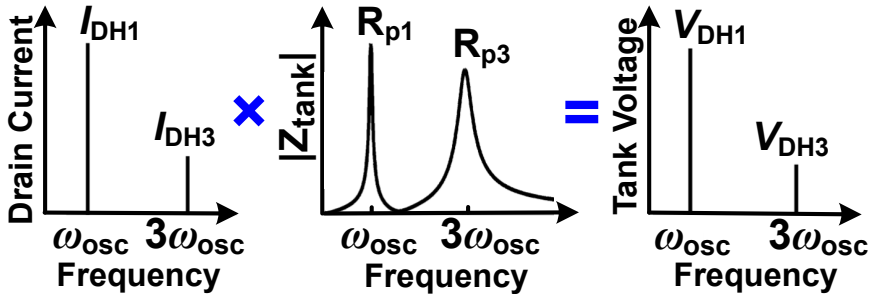
Figure 3.3: One possible harmonic boosting oscillator topology with multiple LC tanks.

3.3.1 Third-Harmonic Boosting Techniques

To generate the 3rd harmonic, one possible approach is to use multiple series-connected LC-tanks resonating at the fundamental and 3rd harmonic [34, 41]. Fig. 3.3 shows the simplified diagram of such an oscillator. The multiple inductors occupy large area. Since the two resonances have the same phase response and transconductance gain in the oscillation loop, undesired oscillation at the auxiliary resonance could be triggered by increasing the level of third harmonic. Therefore, it appears problematic in our case.



(a)



(b)

Figure 3.4: (a): Simplified diagram and (b): operational principle of the proposed oscillator.

A more compact implementation would be a transformer-based dual-tank resonator. The L and C ratios in primary and secondary windings were optimized in [42] to realize fundamental oscillation and its 3$^{\text{rd}}$-harmonic resonance. However, the 3$^{\text{rd}}$-harmonic generated there is relatively weak ($\sim$15% of the fundamental tone), so to make it sufficiently stronger, a high-gain buffering amplifier would be needed. That implies a large power consumption, which would negate the effectiveness of the proposed architecture. Also, thick-oxide transistors were used in [42] due to reliability concerns. In the technology at hand, cut-off frequency (f_T) of the thick-oxide device is <40 GHz. To provide sufficient g_m for the startup of oscillation, either larger power consumption or larger transistor size (i.e., larger parasitic capacitance) would be required. Consequently, thick-oxide device is avoided in this design. In order to reduce the required gain of the following buffer stage, a much stronger third harmonic must be provided by the oscillator. This work proposes such a harmonic boosting technique.

Simplified diagram of the proposed mm-wave oscillator and its operational principle are shown in Fig. 3.4. $I_{DH1,3}$, $R_{p1,3}$ and $V_{DH1,3}$ represent the tank's current, equivalent parallel resistance and voltage, respectively, of the 1$^{\text{st}}$ and 3$^{\text{rd}}$ harmonic components. According to the linear model of oscillators, the oscillation amplitude at the 1$^{\text{st}}$ and 3$^{\text{rd}}$ harmonics is determined by the current component and tank impedance at their respective frequencies. To achieve a larger V_{DH3}/V_{DH1}, there are two possible options: increasing $I_{\text{DH3}}/I_{\text{DH1}}$ or increasing $R_{\text{p3}}/R_{\text{p1}}$. The $I_{\text{DH3}}/I_{\text{DH1}}$ depends on the nonlinearity of the g_m devices and is typically fixed for a certain type of oscillators (e.g., 0.33 for class-B and 0.2 for class-C). It is not straightforward to further increase the $I_{\text{DH3}}/I_{\text{DH1}}$ ratio without extra efforts. Consequently, larger $R_{\text{p3}}/R_{\text{p1}}$ is desired. On the other hand, the equivalent Q-factor (Q_{eq}) at the two resonant frequencies affect the oscillator performance dramatically. High Q_{eq} at ω_{osc} promotes low PN, while low Q_{eq} at $3\omega_{osc}$ is appreciated for better tolerance to the possible frequency misalignment between the second resonance and $3\omega_{osc}$. Moreover, large R_{p1} is beneficial for low power consumption.

The tank impedance of this oscillator can be derived as:

$$Z_{\text{tank}}(j\omega) = \frac{1}{\dfrac{1}{j\omega L_{\text{p}}\left(1+\dfrac{\omega^2 L_{\text{s}} C_{\text{s}} k_{\text{m}}^2}{1-\omega^2 L_{\text{s}} C_{\text{s}} + j\omega C_{\text{s}} r_{\text{s}}}\right) + r_{\text{p}}} + j\omega C_{\text{p}}} \tag{3.1}$$

Since it is a two-port dual-tank oscillator, its equivalent Q is not so straightforward to estimate as in traditional one-port resonators. The equivalent Q-factor (Q_{eq}) is derived from the phase response of the open-loop transfer function $v_{\text{s}}/v_{\text{in}}$ [43]:

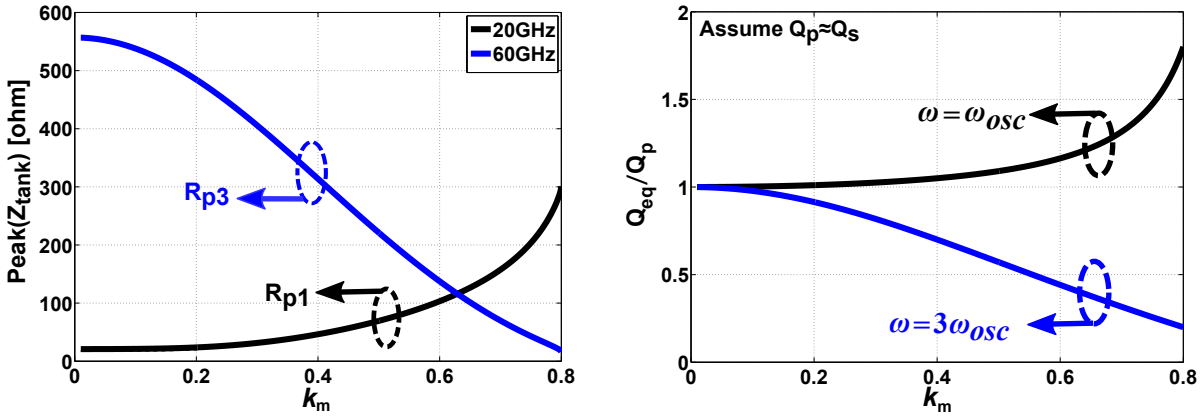
$$H_{ol}(j\omega) = \frac{v_{\text{s}}\left(j\omega\right)}{v_{\text{in}}\left(j\omega\right)} = -G_{\text{m}} \cdot Z_{\text{trans}}\left(j\omega\right) \tag{3.2}$$

$$Z_{trans}(j\omega) = \frac{j\omega M}{\left(1+j\omega C_p r_p - \omega^2 L_p C_p\right)\left(1+j\omega C_s r_s - \omega^2 L_s C_s\right) - \omega^4 M^2 C_p C_s} \tag{3.3}$$

$$Q_{\text{eq}} = \frac{\omega}{2} \cdot \left|\frac{d[\measuredangle H_{ol}\left(j\omega\right)]}{d\omega}\right| = \frac{1+\alpha_{\text{p}}\alpha_{\text{s}} \cdot k_m^2 - \alpha_{\text{p}}\alpha_s}{\dfrac{\alpha_{\text{p}}}{Q_{\text{p}}} + \dfrac{\alpha_{\text{s}}}{Q_{\text{s}}} - \alpha_{\text{p}}\alpha_{\text{s}}\left(\dfrac{1}{Q_{\text{p}}} + \dfrac{1}{Q_{\text{s}}}\right)} \tag{3.4}$$

where, $Z_{trans}(j\omega)$ is the trans-impedance from primary to secondary winding in the tank, $\alpha_{\text{p}} = \omega^2 L_{\text{p}} C_{\text{p}}$, $\alpha_{\text{s}} = \omega^2 L_{\text{s}} C_{\text{s}}$, Q_{p} and Q_{s} are the Q-factors for each winding (i.e., $Q_{\text{p}} = \omega L_{\text{p}}/r_{\text{p}}$ and $Q_{\text{s}} = \omega L_{\text{s}}/r_{\text{s}}$). The two resonances ($\omega_L$ and ω_H) appear at the frequencies where $Im[Z_{\text{trans}}(j\omega)] = 0$. For a transformer-based dual-tank resonator, $\alpha_{\text{p,s}} < 1$ is always true at the low-frequency resonance (i.e., $\omega = \omega_L$). At the high-frequency resonance ($\omega = \omega_H$), $\alpha_{\text{p,s}} > 1/\sqrt{1-k_{\text{m}}^2}$. From (3.4), we can conclude that increasing k_{m} can result in higher Q_{eq} at $\omega = \omega_L$. However, Q_{eq} at $\omega = \omega_H$ will be lower with larger k_{m}.

The above analysis shows that k_{m} affects both the tank impedance (Z_{tank}) and Q_{eq}. Based on Eq. (3.1) and (3.4), the relationships at ω_{osc} and $3\omega_{osc}$ on



(a) (b)

Figure 3.5: Dependency of (a): tank impedance on $k_{\rm m}$ from *Eq.*(1); and (b): $Q_{\rm eq}$ on $k_{\rm m}$ from *Eq.*(3).

k_m are shown in Fig. 3.5. In the calculations, L_p and L_s are kept constant, while C_p and C_s are tuned to achieve the fundamental and 3$^{\rm rd}$-harmonic resonances for each k_m value. As we can see in Fig. 3.5, $R_{\rm p1}$ decreases with smaller $k_{\rm m}$, while $R_{\rm p3}$ behaves opposite. Therefore, smaller $k_{\rm m}$ is desired for larger $R_{\rm p3}/R_{\rm p1}$. However, larger $k_{\rm m}$ is required for high $Q_{\rm eq}$ at ω_{osc} and low $Q_{\rm eq}$ at $3\omega_{osc}$. By reducing k_m for larger $R_{\rm p3}/R_{\rm p1}$, both the PN performance and the tolerance to the possible frequency misalignment between the second resonance and $3\omega_{osc}$ will be degraded. Also, due to the smaller $R_{\rm p1}$, larger power consumption is required to achieve the same oscillation amplitude with reduced k_m. As a trade-off between large 3$^{\rm rd}$ harmonic and optimal oscillator performance, $k_{\rm m}$=0.61 is chosen for $R_{\rm p3}/R_{\rm p1}$>1 with sufficient Q_{eq} and $R_{\rm p1}$.

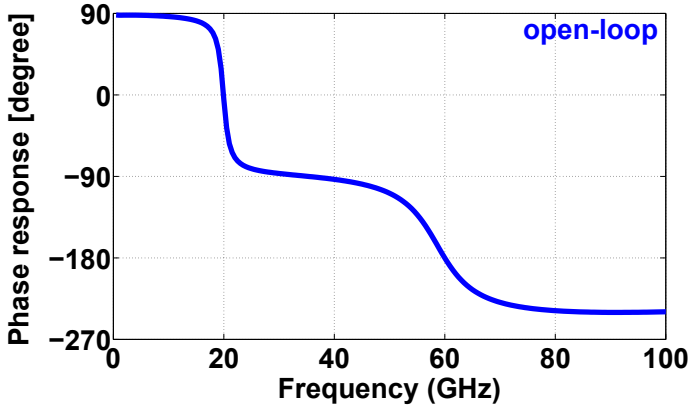


Figure 3.6: Simulated open-loop phase response of v_s/v_{in} in the oscillator.

A concern might arise that the oscillation could happen at ω_H ($\sim$60 GHz) rather than at ω_L ($\sim$20 GHz) due to $R_{\rm p3}$>$R_{\rm p1}$. Start-up conditions are examined to ensure that the oscillation can only happen at ω_L, even if $R_{\rm p3}$>$R_{\rm p1}$: Barkhausen's phase and gain criteria should be satisfied for a stable oscillation. Referring to Eq. (3.2) and (3.3), there is no zero between the two pairs of conjugate poles ($\pm\omega_L$ and $\pm\omega_H$) in $H_{ol}(j\omega)$, which makes this oscillation loop different from [41]. Analysis and simulations show that the open-loop phase response $\measuredangle H_{ol}(j\omega)$=0° at ω_L=ω_{osc}, while $\measuredangle H_{ol}(j\omega)$=−180° at ω_H=3ω_{osc}, as shown in Fig. 3.6. The phase criterion is satisfied only at ω_L. At ω_H, the phase response is -180°, which implies a negative feedback. Therefore, only one stable oscillation mode at $\sim$20 GHz is possible here. This phenomenon also explains the behavior of $Q_{\rm eq}$ in Fig. 3.5. Since the fundamental components at both windings are in-phase, its $Q_{\rm eq}$ at $\omega = \omega_{osc}$ benefits from the mutual inductance. However, due to the fact that the 3$^{\rm rd}$-harmonics at both windings are anti-phase, $Q_{\rm eq}$ at $\omega = 3\omega_{osc}$ decreases with larger $k_{\rm m}$.

Moreover, the transformer tank provides different voltage gain at these two frequencies. The magnitude response of v_s/v_p is investigated. At $\sim$20 GHz, the transformer tank exhibits a voltage gain of 2.2 (6.85 dB). While at $\sim$60 GHz, it has a voltage gain of 0.24 (-12.40 dB). This property filters out the third harmonic in the secondary winding.

Circuit implementation of the proposed third-harmonic boosting oscillator is shown in Fig. 3.7. A 1:2 transformer ($k_{\rm m}$=0.61) together with 4-bit binary weighted switched MOM capacitor banks in both the primary and secondary windings comprises the resonant tank. By changing the separation space between primary and secondary windings, k_m is adjusted to the desired value. C_s provides coarse tuning, while C_p adjusts the second resonance close to 3ω_{osc}. LSB sizes of the switched-capacitor step (ΔC) are 3.5 fF for C_p and 5.8 fF for C_s. To mitigate the breakdown stress on the core transistors while avoiding thick-oxide devices, a lower supply voltage of V_{DD}=0.7 V is used.

Fig. 3.8 shows the simulated tank impedance for the complete design. In

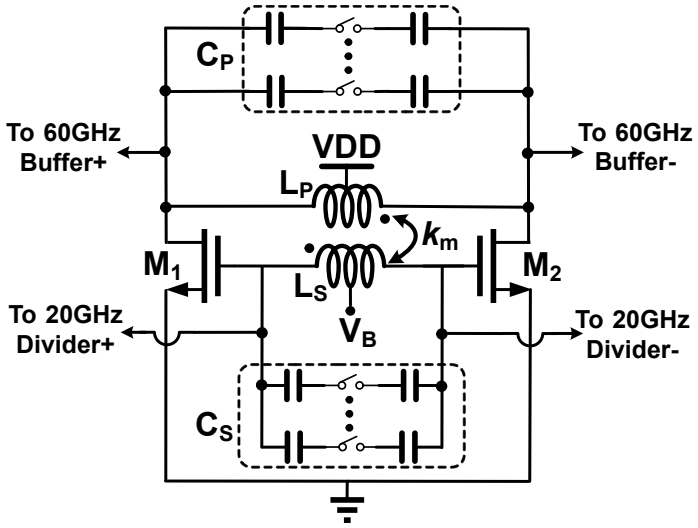


Figure 3.7: Schematic of the 3rd-harmonic boosting oscillator.

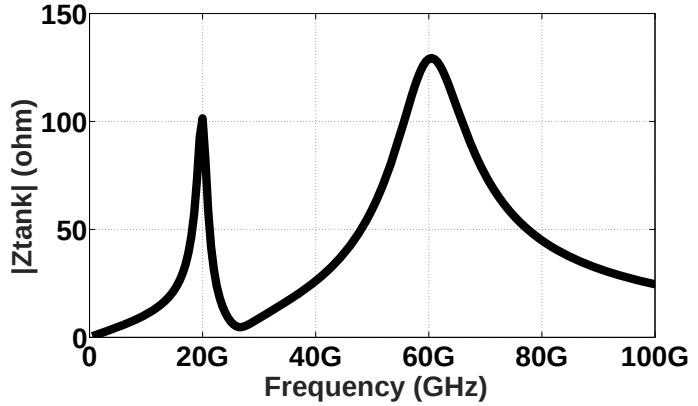


Figure 3.8: Tank input impedance with k_{m}=0.61.

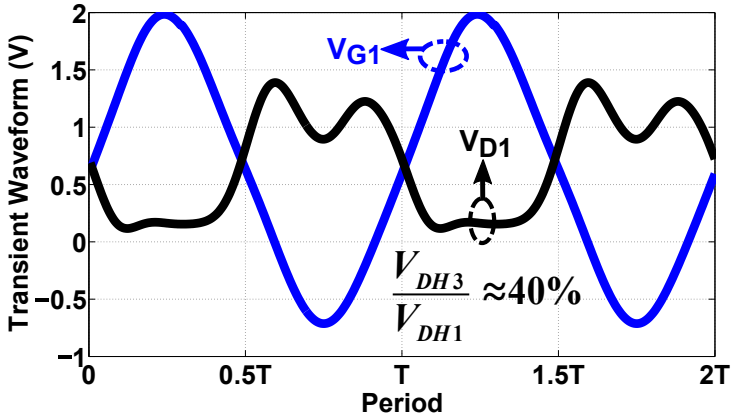


Figure 3.9: Simulated oscillation waveforms at drain and gate nodes.

this case, R_{p1}=102 Ω and R_{p3}=129 Ω. The oscillation waveforms are shown in Fig. 3.9 and reveal that the third harmonic (V_{DH3}) to fundamental component

(V_{DH1}) ratio is ~40% at the drain nodes. Simulated differential amplitude of the 3rd-harmonic tone varies from 350 to 510 mV across the frequency. A sinusoidal waveform at the fundamental frequency is restored at the gate nodes.

3.3.2 Third-Harmonic Extraction

With the above third-harmonic boosting techniques, the oscillator is able to generate a significant harmonic amplitude at ~60 GHz in addition to the fundamental tone at ~20 GHz. To obtain a clean output spectrum at 60 GHz, the fundamental tone needs to be filtered out. LO buffers, which are commonly found in 60 GHz transceivers, are good band-pass filters by nature and are able to provide such filtering capabilities.

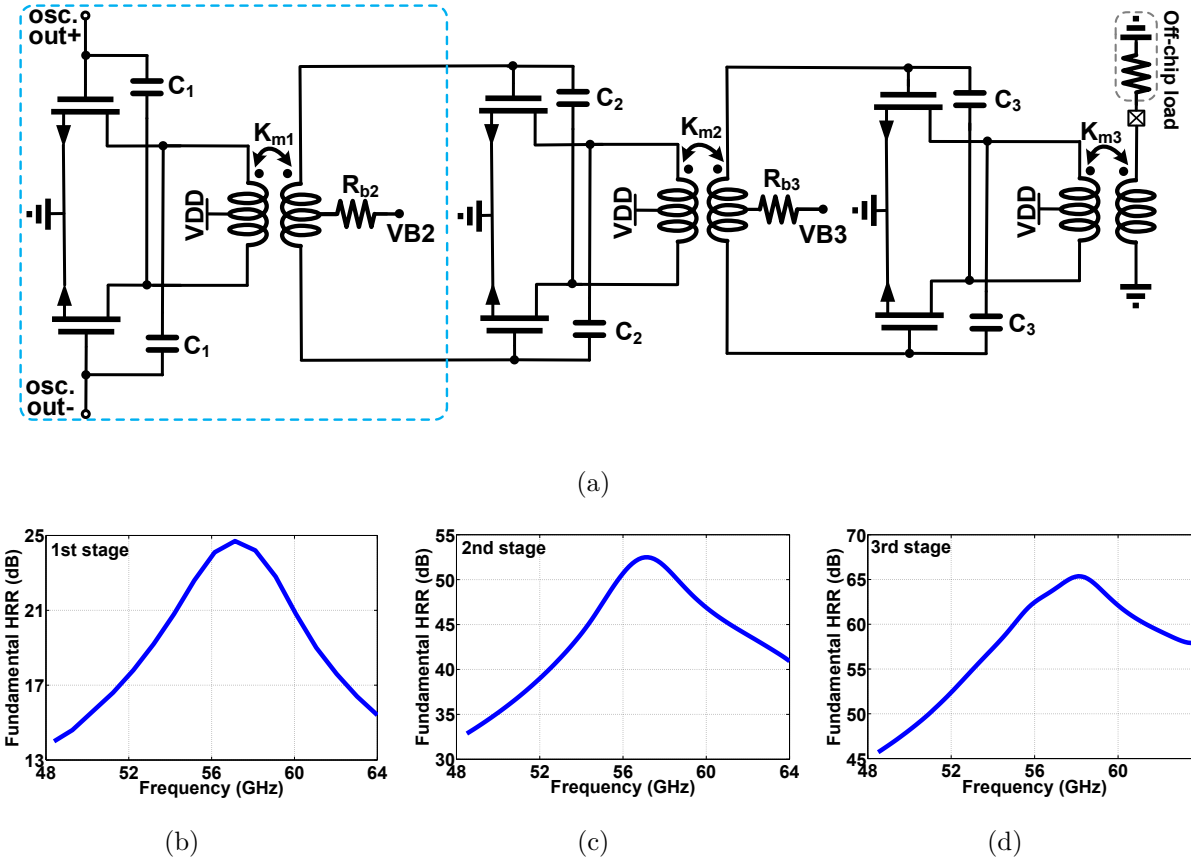


Figure 3.10: (a): Schematic of the 3-stage power amplifier and (b)-(d): simulated fundamental HRR for the each amplifier stage.

A common-source amplifier with transformer loading is designed as one buffer stage, as highlighted in Fig. 3.10(a). At the output of this stage, the simulated fundamental harmonic rejection ratio is 14-25 dB across 48-64 GHz, as shown in Fig. 3.10(b). It is comparable to or better than that of many wideband injection-locked frequency triplers (ILFTs) [44]. This stage consumes 10.5 mA from 1 V supply. No extra cost (e.g., the gain or driving capability) is incurred to obtain such a HRR.

The presence of 20 GHz tone may create several side effects. Inside the amplifier stage, the two-tone (i.e., 20/60 GHz) input could result in harmonic-mixing products. High-order nonlinearities are weak and not a concern. The 2^{nd} and 4^{th} harmonics are closest to the 60 GHz band, but are still 20 GHz away. Moreover, they are generated through the 2^{nd}-order nonlinearity, which can only express itself as a CM distortion. The CM 2^{nd} harmonic at the oscillator output, at ∼18% of the fundamental tone level (see V_{D1} in Fig. 3.9), is also a harmonic source. A large resistor (R_{b2}=1.5 kΩ) is placed at the center-tap of VB2 to prevent the CM signal from propagating to the next stage. However, any unavoidable slight asymmetry in the layout of the oscillator and amplifier could result in some weak conversion from the CM to differential output.

With EM extracted passives, post-layout simulations show that the 2^{nd} and 4^{th}-harmonic levels are <-40 dBc and <-55.8 dBc, respectively, at the differential output of the first amplifier stage over the TR. They are low enough and far away from the 60 GHz band. Therefore, harmonic distortion is not an issue.

At the output of the buffer/amplifier stage, the residual 20 GHz in the 60 GHz LO signal may cause several types of concerns at the system level [45]. One is the out-of-band emission in transmitters (TXs), which should be <-30 dBc at >3.06 GHz offset as specified in [46], and <-40 dBm per FCC regulations [47]. The 60 GHz PLLs will drive upconversion mixers in I/Q TXs, or directly drive PAs in polar TXs. Multi-stage PAs are typically needed to deliver a sufficient output power [8, 48–50]. To satisfy the out-of-band

emission mask, the LC tank in upconversion mixers and multi-stage matching network in the PAs should provide enough suppression of the 20 GHz residual to minimize its transmission. Two extra amplifier stages are added in this design [shown in Fig. 3.10(a)] to verify the adequacy of the natural filtering capability of the TX chain [51]. The simulated 20 GHz HRRs at the output of each amplifier stage are shown in Fig. 3.10(b)-(d).

Another concern is the 20 GHz blocker tolerance on the receiver side. Any incident 20 GHz out-of-band blocker is significantly attenuated by the antenna and LNA matching network. Due to the residual 20 GHz in LO, a 20 GHz blocker will have a non-zero conversion gain in the down-conversion mixer. With the worst-case HRR of -14 dB, the 20 GHz blocker has a conversion gain which is 20 dB lower than that at 60 GHz. In a typical 60 GHz receiver [52], with a 20 GHz blocker level as high as -30 dBm, the down-converted blocker power is well-below the receiver's sensitivity. The above analysis also explains the reasons why the ILFTs, which face similar scenarios as in this design, have found their use in 60 GHz transceivers [8, 48, 50].

3.4 Phase Noise Analysis

The linear time-variant (LTV) phase noise model [53] predicts that the phase noise of an LC-tank oscillator at an offset frequency $\Delta\omega$ is

$$L(\Delta\omega) = 10\log_{10}\left(\frac{\sum_i N_{L,i}}{2\ q_{max}^2\ \Delta\omega^2}\right) \tag{3.5}$$

where, $N_{\mathrm{L,i}}$ is the power of the perturbation generated by the i_{th} noise current source, and $q_{\max}$ is the maximum charge displacement in the tank capacitance. In the case at hand, there are mainly two noise sources that will be converted into phase noise: resonant tank losses and the channel noise of the active devices ($\mathrm{M_1/M_2}$).

Complexity arises from the fact that there are now two resonances (i.e., 20/60 GHz) in the tank. We can no longer rely on the general approach that

models the tank losses as a fixed resistance together with a corresponding current noise source in-parallel to the LC tank. The mechanism of how the two resonant peaks affect the PN is investigated in this section. Regarding the PN contributed from the oscillator core transistors (M_1/M_2), the periodically time-varying g_m and g_{ds} indicate that these noise sources are cyclostationary. Their calculation is discussed later in the section. The oscillator noise sources are shown in Fig. 3.11. The R_{eq} is frequency dependent to reflect the tank's multi-resonance.

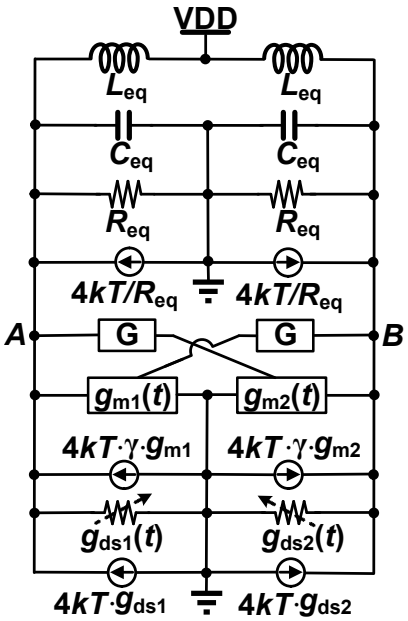


Figure 3.11: Equivalent noise sources in the oscillator.

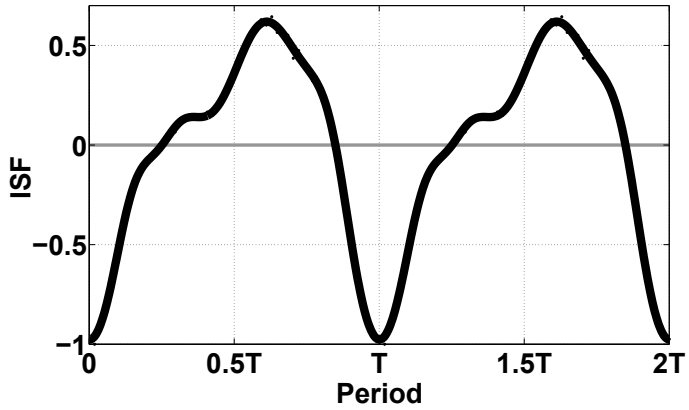


Figure 3.12: Simulated ISF function at the drain nodes.

Prior to the detailed PN analysis and calculations, the ISF function

is obtained through simulations. By injecting current pulses at the drain of M_1/M_2 (node A/B in Fig. 3.11) throughout the oscillation period and measuring the resulting phase shift after settling, the ISF function is extracted and shown in Fig. 3.12. ISF≈0 in the area when the drain waveform is in the bottom flat region (see the waveform V_{D1} in Fig. 3.9). Due to the fact that the rising transition is faster than the falling transition, the ISF is larger at the negative side than at the positive side. It reveals that more circuit noise will be converted to phase noise during the falling transitions.

3.4.1 Tank Noise Upconversion

In our oscillator design, the second resonant impedance at ∼60 GHz is boosted deliberately for a larger third-harmonic magnitude. However, up to this point, the mechanism of how the coexisting two resonant peaks affect the phase noise has not been discussed.

With Fourier series decomposition, the phase perturbation due to the noise source $i_n(t)$ is

$$\phi_{tank}(t) = \frac{1}{q_{max}} \cdot \int_{-\infty}^{t} i_n(\tau) \cdot \sum_{m=0}^{\infty} c_m \cdot cos(m\omega_o\tau) d\tau \tag{3.6}$$

where c_m (m=0, 1, 2, ...) is the Fourier series coefficient of the ISF function $\Gamma(\omega_o t)$. For close-in PN at an offset $\Delta\omega$ ($\Delta\omega \ll \omega_o$), only the noise at $m\omega_o \pm \Delta\omega$ will be converted to PN. Since power spectral density (PSD) of the tank noise source is non-uniformly distributed, it is necessary to divide the spectrum into separate bands around $m\omega_o \pm \Delta\omega$. Each individual band experiences a different conversion factor (c_m) during the conversion process from circuit noise to PN. Fig. 3.13 illustrates such conversion in the frequency domain.

Consequently, the effective noise power generated by the tank losses is

$$N_{tank} = 2 \cdot \left(\frac{c_1^2}{2} \cdot \frac{4kT}{R_{p1}/2} + \frac{c_3^2}{2} \cdot \frac{4kT}{R_{p3}/2} \right) \tag{3.7}$$

where, the factor of 2 accounts for the two single-ended noise sources in the differential oscillator. With stronger third harmonic, c_3 is larger. It facilitates the conversion from tank noise at third harmonic frequency to PN.

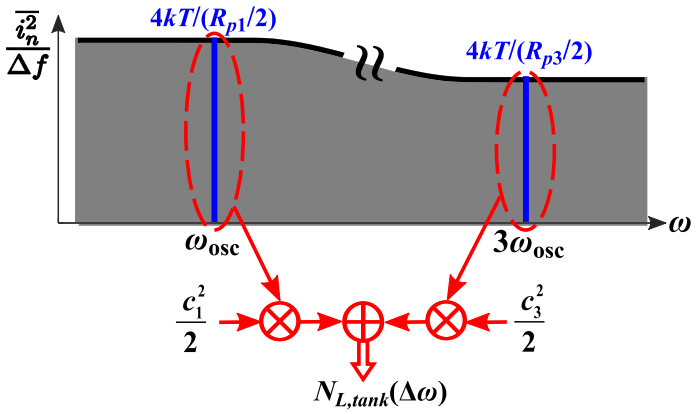


Figure 3.13: Conversion of tank thermal noise into phase noise.

3.4.2 Channel Noise Upconversion

In [42], the effective transconductance (G_{MEF}) and conductance (G_{DSEF}), which was originally derived from the equivalence in the analysis of average power dissipation [54], was adopted in the PN analysis. The cyclostationary properties of the channel noise sources were removed in the PN analysis and calculations. That approach has greatly simplified the analysis process, but has omitted the strong correlation between the ISF function and the channel noise PSD. In some cases, the simplification error might be large.

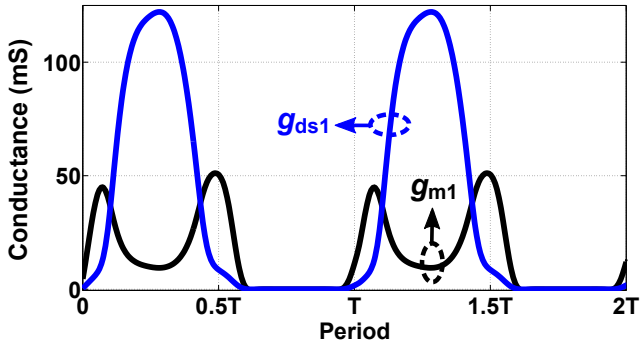
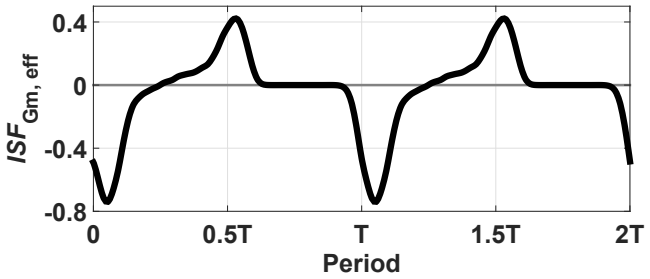
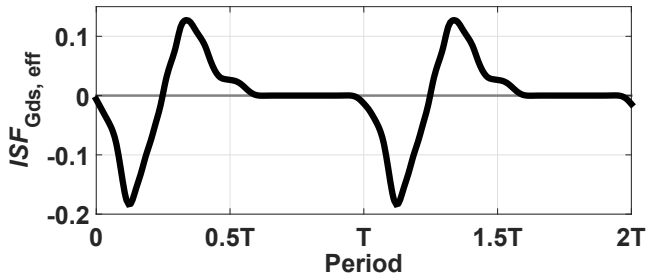


Figure 3.14: Simulated time-varying transconductance and channel conductance of the core transistors in oscillator.



(a)



(b)

Figure 3.15: Effective ISF function for the noise from (a): transconductance $g_{\mathrm{m}}(t)$ and (b): channel conductance $g_{\mathrm{ds}}(t)$.

The periodic time-varying $g_{\mathrm{m}}(t)$ and $g_{\mathrm{ds}}(t)$ in our design are shown in Fig. 3.14. Without losing general applicability, the conversion process from cyclostationary channel noise $i_{\mathrm{n,Gm}}(t)$ to PN is equivalent to that of a stationary white noise source $i_{\mathrm{n0,Gm}}(t)$ with an effective ISF to account for the time-varying effects of $i_{\mathrm{n,Gm}}(t)$ [53]:

$$\overline{i^2_{\mathrm{n0,Gm}}(t)} = 4kT \cdot \gamma \cdot \max[g_{\mathrm{m}}(t)] \tag{3.8}$$

$$\Gamma_{\mathrm{Gm,eff}}(\omega_o t) = \Gamma(\omega_o t) \cdot \sqrt{\frac{g_{\mathrm{m}}(t)}{\max[g_{\mathrm{m}}(t)]}} \tag{3.9}$$

Fig. 3.15(a) shows the corresponding effective ISF for the channel noise $i_{\mathrm{n0,Gm}}(t)$. Most of the PN conversion happens during the rising and falling transitions. The effective noise power generated from g_{m} of the core devices (M_1 and M_2) is

$$N_{\mathrm{Gm}} = 2 \cdot \Gamma^2_{\mathrm{Gm,eff,rms}} \cdot \overline{i^2_{\mathrm{n0,Gm}}(t)} = 0.6 \cdot N_{\mathrm{tank}} \tag{3.10}$$

The same approach is also applied to the PN generated from g_{ds} of the core devices. Its equivalent ISF is shown in Fig. 3.15(b). The effective noise power converted from this part is

$$N_{\mathrm{Gds}} = 2 \cdot \Gamma^2_{\mathrm{Gds,eff,rms}} \cdot \overline{i^2_{\mathrm{n0,Gds}}(t)} = 0.41 \cdot N_{\mathrm{tank}} \tag{3.11}$$

In our case, the total PN generated from the channel noise of the core devices happens to be approximately the same as the PN generated from the tank losses. As we can see from Fig. 3.15, the conversion from channel noise to PN mainly happens during the transitions. When the transistors work in the deep triode region, the channel resistance is low. Due to the absence of a tail current source, the small channel resistance will load the tank. However, since ISF $\approx$0 during this interval, the effective ISF is small. This alleviates the concerns that the small channel resistance in the deep triode region will deteriorate the PN.

To verify the validity of the PN analysis presented above, the derived equations are compared against simulations in SpectreRF at 20 GHz fundamental carrier, as shown in Fig. 3.16. Within the 20 dB/dec region, the difference between the calculated and simulated PN is merely 1.3 dB, testifying to the accuracy of the presented phase noise analysis. Also, Fig. 3.16 shows that the PN at the extracted 60 GHz carrier is 9.5 dB higher (as predicted) than at the 20 GHz signal.

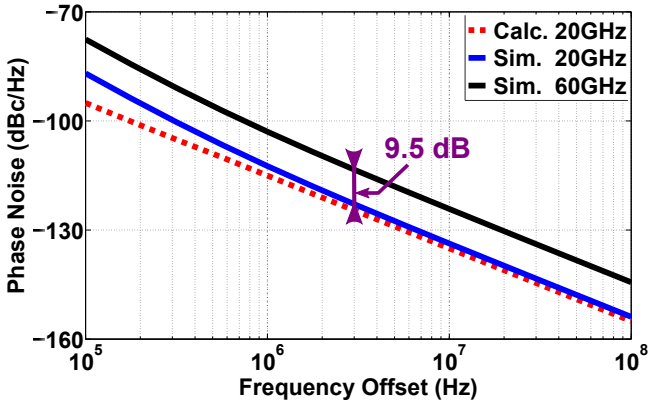


Figure 3.16: Comparison between the simulated and analytical phase noise results.

3.5 More on the Operational Principles of the Proposed Oscillator

3.5.1 Phase Shift in the Oscillation Loop

In traditional single-port LC oscillators, there is no phase shift expected between the drain current and voltage waveforms. In our oscillator, there are two ports (i.e., primary and secondary windings) inside the oscillation loop. Ideally, the phase shift across the two ports ($v_{\rm s}$ and $v_{\rm p}$) would be 180° for ω_L=$\omega_{\rm osc}$ and 0° for ω_H=3$\omega_{\rm osc}$. The gate and drain waveforms are expected to be anti-phase, and the phases of the 1st and 3rd harmonics in the drain waveform should be exactly aligned. However, the waveforms shown in Fig. 3.9 indicate that there is some unexpected phase shift between $V_{\rm G1}$ and $V_{\rm D1}$, and also between the 1st and 3rd harmonics in $V_{\rm D1}$.

This phenomenon indicates that the 2-port transformer-based resonator exhibits non-ideal phase response. To get an insight into this phenomenon, the transfer function from primary to secondary windings is derived:

$$\frac{v_{\rm s}}{v_{\rm p}} = -\frac{k_{\rm m}\cdot\sqrt{L_{\rm s}/L_{\rm p}}}{1-\alpha_{\rm s}(1-k_{\rm m}^2)+\dfrac{\alpha_{\rm s}}{Q_{\rm p}Q_{\rm s}}+j(\dfrac{\alpha_{\rm s}}{Q_{\rm p}}+\dfrac{\alpha_{\rm s}}{Q_{\rm s}}-\dfrac{1}{Q_{\rm p}})} \tag{3.12}$$

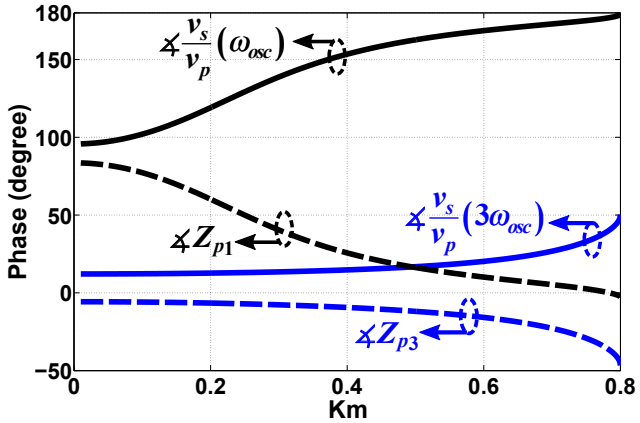


Figure 3.17: Phase response of the transformer based 2-port resonant tank at fundamental and 3rd harmonic frequencies.

Fig. 3.17 shows the phase response of $v_{\rm s}/v_{\rm p}$ at ω_L and ω_H for $k_{\rm m} = 0{-}0.8$. As we can see, $\measuredangle v_s/v_p$ is never exactly 180° at ω_L, and also never exactly 0° at ω_H. The non-ideal phase shift decreases with larger $k_{\rm m}$ at ω_L, while it behaves the opposite at ω_H. To achieve an open-loop $\measuredangle v_s/v_{in}$ as shown in Fig. 3.6, the phase response of $v_{\rm p}/v_{\rm in}$ needs to provide an extra phase shift to compensate for the $\measuredangle v_s/v_p$ non-ideality. To realize that, we recognize that the tank's input impedance $Z_{\rm tank}$ is not a pure resistance at ω_L and ω_H, so the phase shift is generated between the current and voltage waveforms at drain nodes. It is perhaps counter-intuitive at a first glance. Tracing it to the source, it is the leakage inductance and the ohmic losses within each winding that contribute to the extra phase shift. Referring to Eq. 3.1, the phase of $Z_{\rm tank}$ at ω_L ($\measuredangle Z_{\rm p1}$) and ω_H ($\measuredangle Z_{\rm p3}$) is calculated and plotted in Fig. 3.17. As expected, $\measuredangle Z_{\rm p1}$ and $\measuredangle Z_{\rm p3}$ can fully compensate for the non-ideal phase difference introduced in the $v_{\rm s}/v_{\rm p}$ transfer path.

The non-zero $\measuredangle Z_{\rm p1}$ and $\measuredangle Z_{\rm p3}$ result in the phase shift between the gate and drain voltage. The difference between $\measuredangle Z_{\rm p1}$ and $\measuredangle Z_{\rm p3}$ will contribute to phase misalignment between the 20/60 GHz components. Since $\measuredangle Z_{\rm p1} > 0$ and $\measuredangle Z_{\rm p3} < 0$, the fundamental component always leads the 3$^{\rm rd}$ harmonic. By tuning the second resonance ω_H to a proper frequency that is above $3\omega_{osc}$, it would be possible to make $\measuredangle Z_{\rm p3} = \measuredangle {\rm Z_{p1}}$ and therefore eliminate that phase misalignment. However, the original reactive power balance between L and C in the steady-state oscillation tank would be perturbed. The 3$^{\rm rd}$-harmonic of the drain current has to flow through the inductive part in $Z_{trans}(j\omega)$, and it can facilitate the flicker noise to PN conversion [38, 55]. Simulations also show that the flicker noise corner and the close-in PN get worse in that case.

Though the non-zero $\measuredangle Z_{\rm p1}$ and $\measuredangle Z_{\rm p3}$ create waveform misalignment, the reactance part happens to be just a small portion of $Z_{\rm p1}$ and $Z_{\rm p3}$ in our design. Without sacrificing the accuracy, we assume that $R_{\rm p1} \approx |Z_{\rm p1}|$ and $R_{\rm p3} \approx |Z_{\rm p3}|$ for simplicity in the PN analysis in Section III.

3.5.2 The Amount of Third Harmonic: Bounded or Not?

From Section 3.3, we know that the V_{DH3}/V_{DH1} ratio has a positive correlation with $R_{\rm p3}/R_{\rm p1}$. This begs a question: Will V_{DH3}/V_{DH1} be unbounded with an ever-increasing $R_{\rm p3}/R_{\rm p1}$? In the linear oscillator model, the drain current will only flow through the tank impedance represented by $R_{\rm p}$. The 3^{rd}-harmonic amplitude is therefore proportional to $R_{\rm p3}$. So, until now, the answer seems to be affirmative. This model assumes that the oscillation state is time-invariant over the oscillation period. However, in our design, the absence of an ideal current source forces the proposed oscillator to somewhat deviate from the classical linear model.

Due to the lack of good isolation between the transistors and ground, the tank can directly see the loading effects of the channel resistance. M_1/M_2 traverse through different operational regions (saturation, triode and shut off) over the oscillation period, and the channel conductance ($g_{\rm ds}$) varies dramatically. Fig. 3.14 shows the typical $g_{\rm ds}(t)$ of M_1/M_2 in our design. When the large fundamental-harmonic swing drives the transistor into deep triode (during 0.1T$-$0.4T in Fig. 3.9), the transistor behaves like a small resistor that conducts the drain node to ground. The inductor L stops commuting its current with the tank capacitors C, but instead leaks the current to ground through the small channel resistance. Therefore, the oscillation states are forced to change. Due to the time-variant nature of the oscillator [56], the linear model fails to characterize it. During this interval within each period, the oscillation waveform is enforced to flatten. This phenomenon will limit the maximum achievable third harmonic.

Simulations have been carried out to verify this hypothesis. In Fig. 3.18, $R_{\rm p1}$ and V_{DH1} are controlled to be constant, while $R_{\rm p3}$ is swept. When $R_{\rm p3}/R_{\rm p1} < 1.5$, V_{DH3}/V_{DH1} increases dramatically with growing $R_{\rm p3}/R_{\rm p1}$. However, V_{DH3}/V_{DH1} starts to saturate after $R_{\rm p3}/R_{\rm p1} > 1.5$. Therefore, keeping on increasing $R_{\rm p3}/R_{\rm p1}$ cannot increase V_{DH3}/V_{DH1} indefinitely.

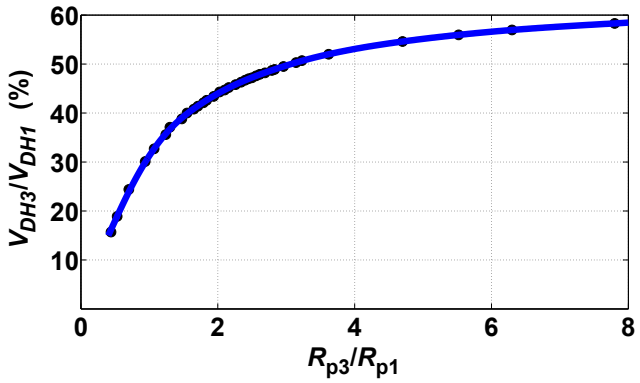


Figure 3.18: Simulated dependency of V_{DH3}/V_{DH1} ratio on $R_{\mathrm{p3}}/R_{\mathrm{p1}}$.

3.6 Implementation and Experimental Results

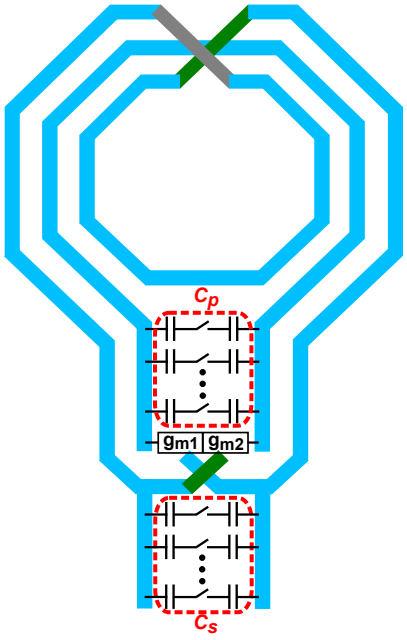


Figure 3.19: Proposed layout for the transformer-based dual-tank oscillator.

To demonstrate the effectiveness of the proposed mm-wave frequency generation scheme, the 3$^{\mathrm{rd}}$-harmonic boosting oscillator together with the 3-stage 60 GHz output amplifier is prototyped in TSMC 40-nm 1P7M LP CMOS. The 1:2 transformer in the oscillator uses a 3.5 um ultra-thick metal (UTM) layer. Its k_{m} is designed to be 0.61. The differential self-inductance of primary and secondary windings are 150 pH and 390 pH, respectively. The Q-factors for primary and secondary windings are similar, and $Q_p \approx Q_s = 15$

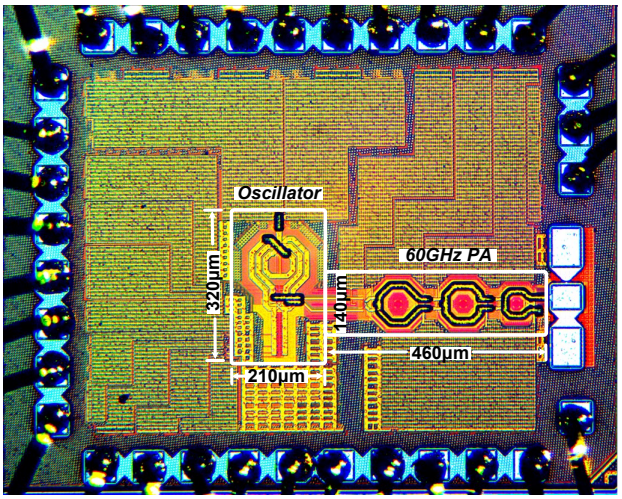


Figure 3.20: Chip micrograph; the core area is 0.13 mm^2.

at 20 GHz. The switched-capacitors' Q is 25 at 20 GHz. In total, an overall Q of 10.5 is achieved at 20 GHz for the entire tank.

The dual-tank oscillator requires special care in layout. The dense interconnects to the two capacitor banks around the core transistors may contribute an extra parasitic inductance and undesired magnetic coupling. Therefore, the layout routing should be optimized to minimize the undesired coupling between the two capacitor banks. Due to the relatively small tank inductance and capacitance, it is sensitive to the layout asymmetry and parasitics. This makes the layout routing challenging. A layout topology is proposed in Fig. 3.19. The transformers in the matching network of the 3 amplifier stages use the UTM layer for primary windings and 1.45 um aluminum capping layer for secondary windings. The chip micrograph is shown in Fig. 3.20.

An R&S FSUP50 signal source analyzer is used with an external mixer to measure the oscillator's PN, whose plot is shown in Fig. 3.21 at 57.8 GHz. The oscillator's power consumption is 24 and 13.5 mW with and without the first amplifier stage, respectively. At 1 MHz offset, the PN is -100.1 dBc/Hz, which is the best-ever reported in CMOS. The $1/f^3$ PN corner is 920 kHz. The 60 GHz frequency generator achieves a 25% TR from 48.4 to 62.5 GHz.

To verify the suppression of the fundamental tone at ~20 GHz, the spectrum is measured around the 58.75 GHz carrier and also from 0 to 50 GHz, as

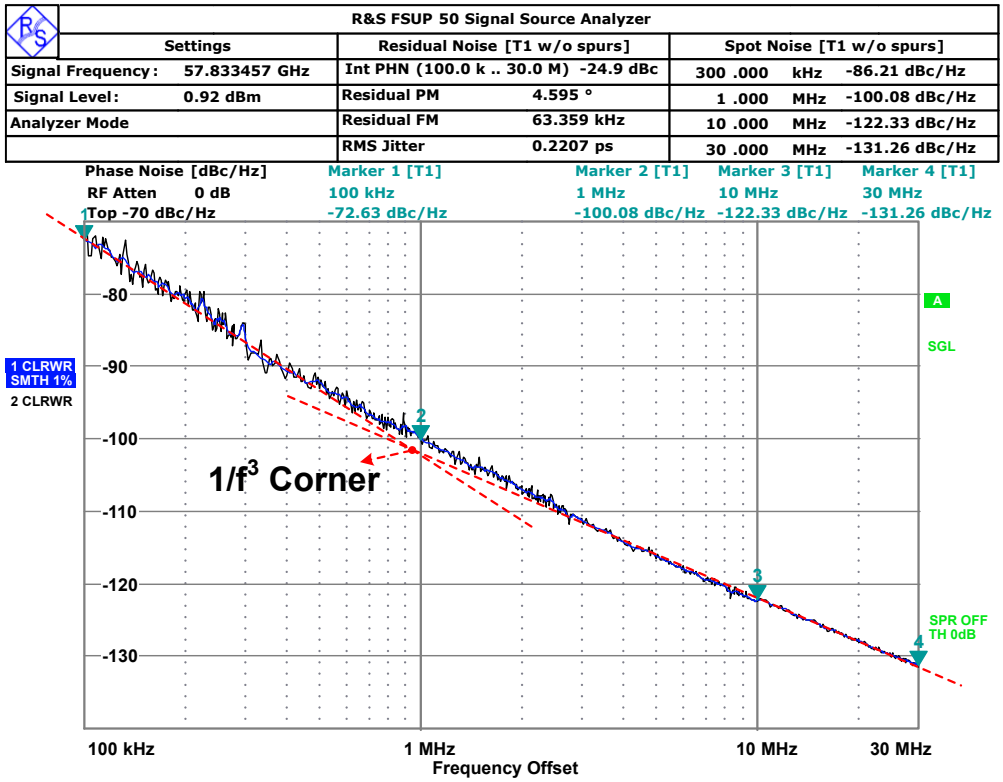
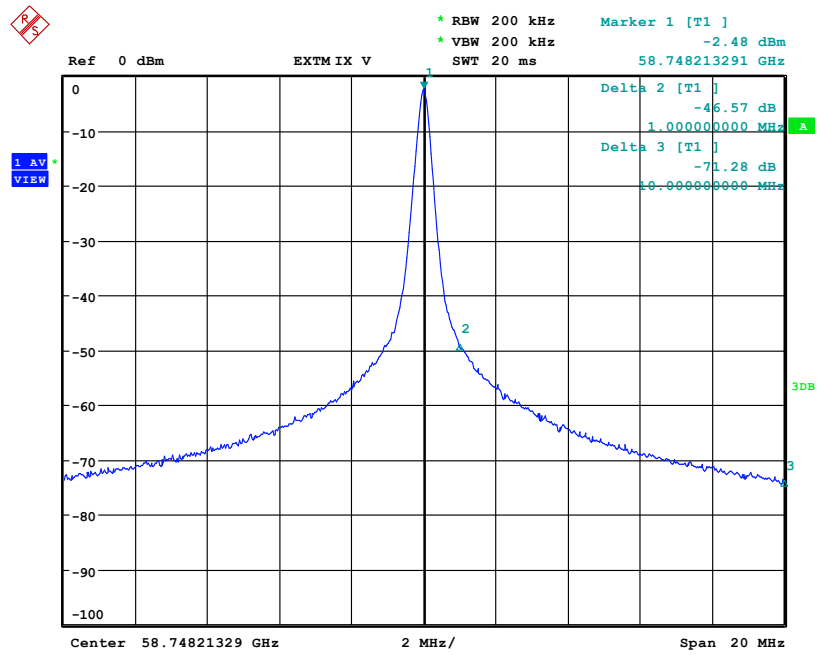
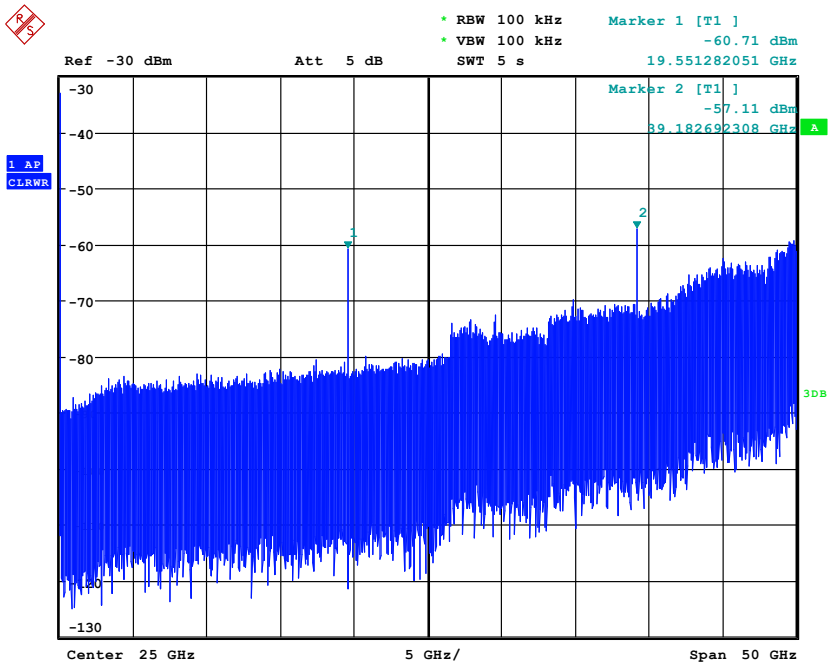


Figure 3.21: Measured phase noise at 57.8 GHz.

shown in Fig. 3.22. At 1 V supply, the 3-stage amplifier delivers a maximum of +6 dBm to the 50 Ω load while consuming 58 mW. The output power across the oscillator's TR is shown in Fig. 3.23(a). Since wideband amplifiers are not the focus in this work, the bandwidth of the amplifiers is not large enough to cover the oscillator's 25% TR; hence the drop in amplitude at <54 GHz. The literature offers a number of wideband techniques [57] to extend the amplifier bandwidth. The measured power of the ∼20 GHz fundamental is -56.5 dBm, which is 62 dB below the carrier. The second harmonic at ∼40 GHz is visible at -51.5 dBm, which is -57 dBc. The leakage power level of the fundamental and 2nd-harmonic tone at the output across the TR is shown in Fig. 3.23(b)-(c). When the amplifiers are supplied at a reduced V_{DD}=0.7 V, they deliver 0 dBm maximum while consuming 22 mW. The HRR varies only 3 dB when changing V_{DD} between 0.7-1 V. The fundamental and 2nd-harmonic power levels satisfy the out-of-band emission mask in IEEE 802.11ad [46] and FCC regulations [47] with sufficient margin. This demonstrates that with



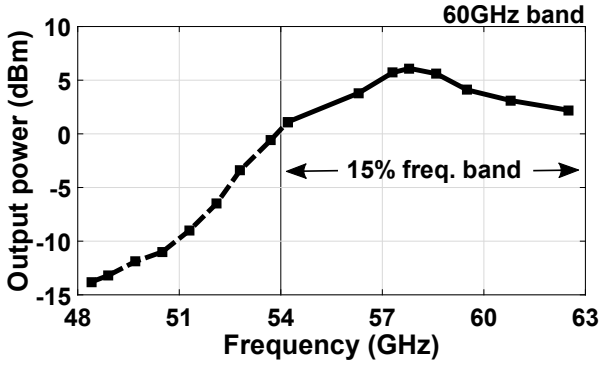
(a)



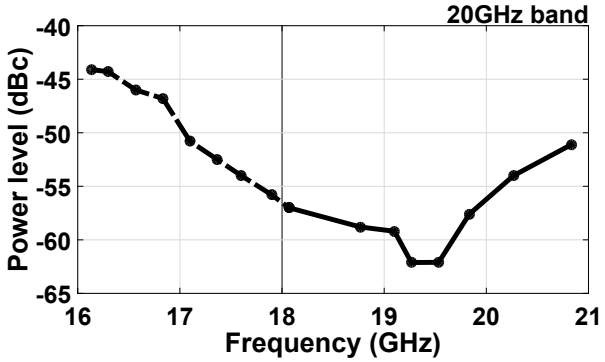
(b)

Figure 3.22: Measured spectrum (a): at 58.75 GHz and (b): 0–50 GHz.

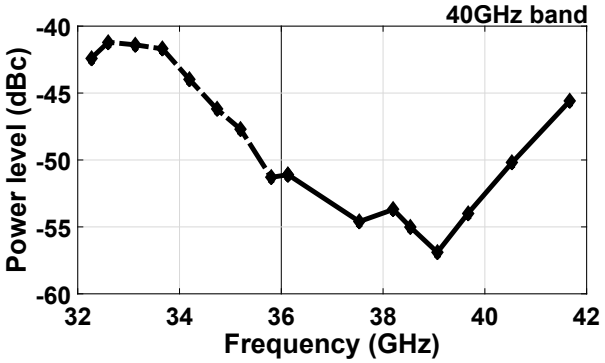
the natural filtering from a multi-stage PA in the TX, the 20 GHz residual emission is not an issue.



(a)



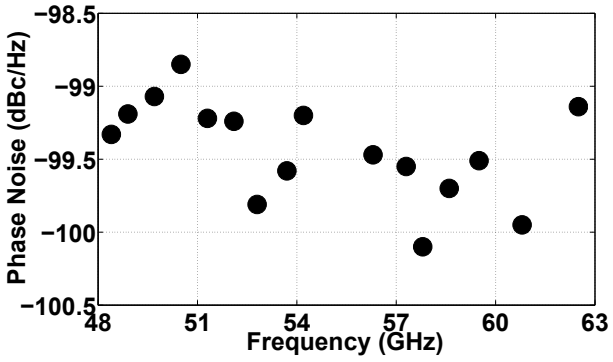
(b)



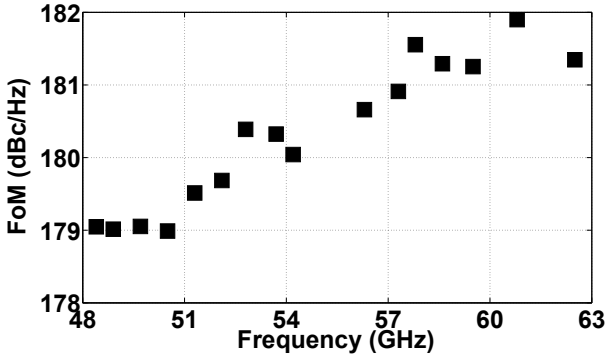
(c)

Figure 3.23: Measured power level at (a): 60 GHz band; (b): fundamental frequency and (c): the 2nd harmonic.

Fig. 3.24 shows the PN at 1 MHz offset and the corresponding FoM across the 25% TR. In Fig. 3.24(b), the power consumption of the first amplifier stage (10.5 mW from 1 V) is included in the FoM calculation. When taking the total power consumption of the 3 amplifier stages (22 mW from 0.7 V) into account, the FoM drops by 1.7 dB. The PN varies between -98.8 and -100.1 dBc/Hz.



(a)



(b)

Figure 3.24: (a): Measured phase noise at 1 MHz offset and (b): the corresponding FoM across the tuning range.

The corresponding FoM changes between 179 and 181.9 dBc/Hz across the frequency range. Since the switched-capacitors have lower Q-factor in on-state, the FoM at lower frequencies decreases.

Compared to traditional 60 GHz oscillators, the proposed solution offers several advantages. Larger L and C of the tank lowers its sensitivity to parasitics, thus resulting in wider TR. The relatively small contribution of the nonlinear parasitic capacitance from the core transistors points to less $1/f$ noise upconversion. Oscillation at 20 GHz benefits from a better Q-factor of the resonant tank. The 3$^{\text{rd}}$-harmonic injection reduces the ISF value, thus lowering the PN.

Table I summarizes the performance of the proposed 60 GHz frequency generator and compares it with the relevant state-of-the-art. The PN is the best, and advances state-of-the-art by 4.3 dB at 1 MHz offset. Since the output

Table 3.1: Performance Comparison with State-of-the-Art 60 GHz Output Oscillator Systems

		This work		[58]	[59]	[28]	[29]	[19]	[37]	[60]	[24]
Technology (nm)		40		90	130	90	65	40	65	65	32 SOI
Type		Harmonic extraction		Fundam-ental	Fundam-ental	Fundam-ental	Fundam-ental	Fundam-ental	Freq. tripling	Freq. tripling	CM extraction
P_{DC} (mW)	Osc.	13.5		14	3.9	8.1	8.4-10.8	14	24	10.6	42
	buf./amplif.	10.5[1]	22[2]	NA	NA	NA	NA	NA	NA	NA	
	× / ÷ [3]	0		4.8	NA	NA	NA	10	23.3	14	0
V_{DD} (V)		0.7/1	0.7	1.2	1	0.7	1.2	0.9	1.2/1	1.2	1
Tuning range (GHz)		48.4-62.5 (25.4%)		55.8-61.6 (9.8%)	59-65.2 (10%)	53.2-58.4 (9.3%)	57.5-90.1 (41.1%)	53.8-63.3 (16%)	70.5-85.5 (19.2%)	58.3-65.4 (11.5%)	46.4-58.1 (22.4%)
PN (dBc/Hz)	1MHz	-100.1		-94	-95/-91	-91	NA	-91–-94.5	-91.7–-95.8	NA	-89
	10MHz	-122.3		NA	NA	NA	-104.6– -112.2	NA	NA	-115	-118
FoM (dBc/Hz)	1MHz	181.5[1]	179.8[2]	176.8	185/181	177.2	NA	172.7-175.4	176.6	NA	167.7
	10MHz	183.7[1]	182[2]	NA	NA	NA	172-180	NA	NA	176.9	176.7
FoM_T (dBc/Hz)	1MHz	189.6[1]	187.9[2]	176.6	185/181	176.6	NA	176.6-179.5	182.6	NA	174.7
	10MHz	191.8[1]	190.1[2]	NA	NA	NA	184.2-192.2	NA	NA	178.1	183.7

[1]: including the power consumption of the *first* buffer/amplifier stage (10.5 mW) at V_{DD}=1.0 V
[2]: including the *total* power consumption of the three amplifier stages (22 mW) delivering 0 dBm at V_{DD}=0.7 V
[3]: power consumption of the 60 GHz frequency divider or multiplier

of the first amplifier stage could not be directly probed in this chip, two sets of FoM and FoM_T are included: 1) with the power consumption of the first amplifier stage at V_{DD}=1.0 V; and 2) with the total power consumption of the 3 amplifier stages at V_{DD}=0.7 V. Compared to state-of-the-art designs which also include 60 GHz frequency dividers/multipliers [19, 24, 37, 58, 60], our achieved FoM and FoM_T are respectively >3 dB and >5 dB better.

Chapter

4

Flicker Noise Upconversion and Suppression in Oscillators

This chapter investigates the process of flicker noise upconversion to PN in LC oscillators. The upconversion mechanisms are comprehensively studied at circuit level [61]. They can be categorized into two types: direct and indirect upconversion. Fundamental and/or high-order harmonics in v_{gs} of the the g_m devices mixes with the baseband flicker noise and directly upconvert it to around fundamental and harmonic frequencies via the nonlinearities of the cross-coupled pair. With any out-of-phase harmonics in v_{gs}, the $1/f$ noise can be converted to phase modulated noise around the oscillation frequency, namely, PN. The upconverted flicker noise at high-order harmonic frequencies in v_{ds} of the the g_m devices can also be indirectly converted down to the oscillation frequency by self-mixing with the periodically varying $g_{ds}(t)$ of the cross-coupled pair. If there is any high-order harmonic in v_{ds} that is out-of-phase, the $1/f$ noise is indirectly converted to PN. To achieve low $1/f^3$

noise, out-of-phase harmonic voltage swing in v_{ds} and v_{gs} should be eliminated. Accordingly, a generic technique is proposed to suppresses the flicker noise upconversion through both the direct and indirect mechanisms.

4.1 PLL Phase Noise Analysis

With the PLL architecture proposed in Chapter 3, the phase noise of the oscillator has been improved significantly, especially at 1 MHz offset. However, the $1/f^3$ noise corner is around 1 MHz, which is still quite high. It is even more than 1 MHz in conventional mm-wave oscillators [28, 58]. As discussed in Chapter 2, when the loop bandwidth is much smaller than the corner frequency, the $1/f^3$ noise has significant contribution to the output phase noise. To verify its contribution, the oscillator phase noise measured in Chapter 3 is taken into an s-domain linear model of a 60 GHz ADPLL. A 40 MHz FREF clock is employed with noise floor of -150 dBc/Hz. The TDC quantization noise is assumed to be at the same level as FREF noise. The other non-dominant noise sources are neglected for simplicity. The loop filter is configured for the lowest integrated phase noise (IPN) performance. Fig. 4.1 shows the phase noise result predicted by the model. The DCO's contribution to the in-band PN is much higher than that caused by the TDC and FREF noise floor. Keeping the other loop components and noise sources identical but improving the DCO $1/f^3$ corner to 300 kHz, the DCO phase noise does not dominate the in-band phase noise any more, as shown in Fig. 4.1. IPN of the PLL with the conventional $1/f^3$ DCO is 2.3 dB higher than that with the low $1/f^3$ DCO. Therefore, the currently achievable $1/f^3$ noise corner should be substantially reduced.

4.2 Flicker Noise Upconversion Mechanisms

Techniques to lower the flicker noise upconversion have been proposed for single-GHz voltage-biased oscillators [62, 63]. However, they are sensitive to parasitic inductances and capacitances between VDD and VSS supply rails. This effect becomes especially important when the VDD routing is physically away from VSS, effects of which are greatly magnified at mm-wave frequencies. Therefore, those techniques have tight constraints in practical mm-wave

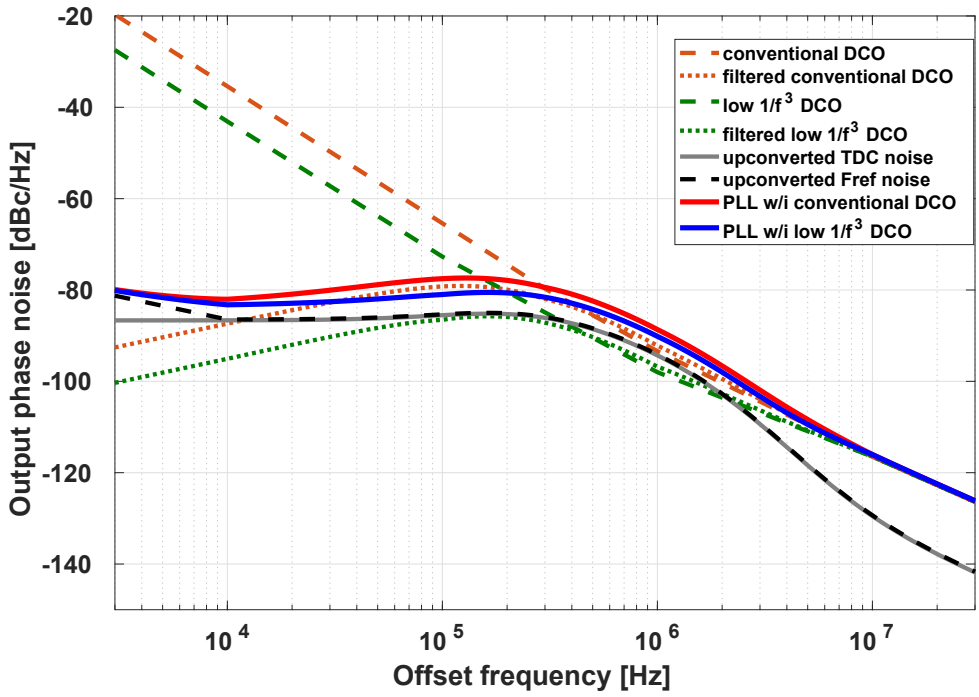


Figure 4.1: 60 GHz ADPLL output phase noise with two different corners of DCO $1/f^3$ noise corner: 1 MHz and 300 kHz.

designs. Moreover, they are not applicable to current-biased oscillators, i.e. those employing a tail current source (e.g. M_T in Fig. 4.7), which is helpful for power supply rejection and oscillation amplitude control. In the presence of tail current, flicker noise in the tail current source can be upconverted to $1/f^3$ PN. With a large transistor size or its outright replacement by digitally controlled resistors, its contribution can be made marginal. However, its parasitic capacitance provides an extra medium for the flicker noise of the $M_{A,B}$ transistors to be upconverted to PN [38]. Moreover, the negative-g_m devices in mm-wave oscillators usually assume the shortest channel length for small parasitic capacitance and can generate significant amount of flicker noise. It has lead to high $1/f^3$ noise in conventional mm-wave oscillators. Until now, the $1/f$ upconversion mechanism has not been yet comprehensively explained.

In this work, we specifically focus on the $1/f$ noise upconversion mechanism by the cross-coupling transistors ($M_{A,B}$) that sustain the oscillation. Flicker

noise in $M_{A,B}$ is upconverted to the respective drain current i_{ds} at oscillation frequency ω_0 and its harmonics through higher-order nonlinearities. Within the physical circuit constraints, assume $v_{gs} = \pm A \sin \omega_0 t + \sum_{n=2k} A_n \cos(n\omega_0 t + \theta_n) \pm \sum_{n=2k+1} A_n \sin(n\omega_0 t + \theta_n) + n_{f\mathrm{A,B}}$, where $n_{f\mathrm{A,B}}$ is the input-referred flicker noise of M_A or M_B and $k = 1, 2, 3 \ldots$. In steady-state oscillation, $M_{A,B}$ traverses through subthreshold, saturation and triode regions. The drain current i_{ds} across these regions is

$$i_{ds} = \begin{cases} I_0 \cdot \exp\left(v_{gs}/V_T\right), & \text{subthreshold} \\ \dfrac{K}{2} \cdot \left(v_{gs} - V_{TH}\right)^2 \cdot \left(1 + \lambda \cdot v_{ds}\right), & \text{saturation} \\ K \cdot \left[\left(v_{gs} - V_{TH}\right) v_{ds} - \dfrac{1}{2} v_{ds}^2\right], & \text{triode} \end{cases} \tag{4.1}$$

where $K = \mu C_{ox} \dfrac{W}{L}$. Over the oscillation periods, the steady-state i_{ds} is determined by v_{gs} and v_{ds} altogether. The nonlinear dependence of i_{ds} on v_{gs} and v_{ds} can be captured by the modified Volterra series with two inputs. As all the parasitic capacitance is absorbed in the LC tank, we only care about the I-V characteristic of the intrinsic MOSFET itself. Memory effects is not present here. With static nonlinearity, the Volterra series can be simplified to

$$i_{ds} = \sum_{m=0}^{N} \sum_{n=0}^{N} H_{mn} v_{gs}^m v_{ds}^n = H_{00} + \sum_{m=1}^{N} H_{m0} v_{gs}^m + \sum_{m=1}^{N} \sum_{n=1}^{N} H_{mn} v_{gs}^m v_{ds}^n + \sum_{n=1}^{N} H_{0n} v_{ds}^n \tag{4.2}$$

In the above equation, the second, third and fourth items depend, respectively, only on v_{gs}, on both v_{gs} and v_{ds} and only on v_{ds}. Eq. 4.2 is the mathematical model. Based on Eq. 4.1, the total i_{ds} can be segmented into 3 parts: i_{ds1} that only depends on v_{gs}, i_{ds2} that depends on both v_{gs} and v_{ds}, and i_{ds3} that only

depends on v_{ds}. They are given by:

$$i_{ds1} = \begin{cases} I_0 \cdot \exp\left(v_{gs}/V_T\right), & \text{subthreshold} \\ \dfrac{K}{2} \cdot \left(v_{gs} - V_{TH}\right)^2, & \text{saturation} \\ K \cdot \left[\left(v_{gs} - V_{TH}\right) V_{DS0} - \dfrac{1}{2} V_{DS0}^2\right], & \text{triode} \end{cases} \tag{4.3}$$

$$i_{ds2} = \begin{cases} 0, & \text{subthreshold} \\ \dfrac{K}{2} \cdot \left(v_{gs} - V_{TH}\right)^2 \cdot \lambda \cdot v_{ds}, & \text{saturation} \\ K \cdot \left(v_{gs} - V_{TH}\right)\left(v_{ds} - V_{DS0}\right), & \text{triode} \end{cases} \tag{4.4}$$

$$i_{ds3} = \begin{cases} 0, & \text{subthreshold} \\ 0, & \text{saturation} \\ -\dfrac{K}{2} \cdot \left(v_{ds} - V_{DS0}\right)^2, & \text{triode} \end{cases} \tag{4.5}$$

where V_{DS0} is the instantaneous drain-source voltage when the g_m-devices transition from saturation to triode region, and $i_{ds} = i_{ds1} + i_{ds2} + i_{ds3}$. V_{DS0} is a fixed DC voltage in steady-state oscillation. The i_{ds1} is a nonlinear continuous function of v_{gs}.

Recalling the second item in Eq. 4.2, the i_{ds1} induced by v_{gs} can be expressed as

$$i_{ds1} = a_1 v_{gs} + a_2 v_{gs}^2 + a_3 v_{gs}^3 + \ldots \tag{4.6}$$

where $a_1, a_2, a_3, \ldots$ represent fundamental and higher-order large-signal nonlinearity coefficients. It directly upconverts the $1/f$ noise in v_{gs} to high frequencies. The i_{ds2} is induced by v_{ds} on the periodically-varying g_{ds} of $M_{A,B}$. Upconverted $1/f$ noise at high-order harmonic frequencies in v_{ds} is mixed with g_{ds}. The $1/f$ noise can be indirectly upconverted to fundamental frequency in this way. The i_{ds3} typically plays little role, and is neglected here.

In practical LC oscillators, higher-order harmonics in v_{gs} are small and so at most only the 2$^{\text{nd}}$ (H2) and 3$^{\text{rd}}$ (H3) harmonics need to be considered. For easy illustration, we take H2 as the only such harmonic. The procedure

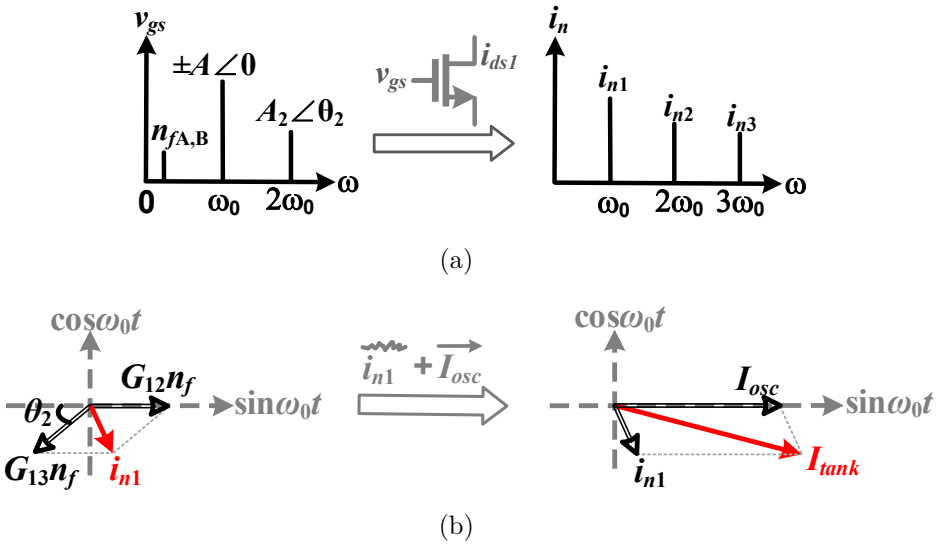


Figure 4.2: (a) Flicker noise upconversion to high-frequency current noise in i_{ds1}; (b) flicker noise direct conversion to PN.

for H3 would be similar. The H2 component is common-mode (CM). Such component is propagated from i_{ds} to v_{gs} of the g_m-pair. Its phase is determined by the CM (trans-)impedance termination at H2 (Z_{trans2}) in this path. If it is resistive, the H2 would be anti-phase with $\cos 2\omega_0 t$. Assuming a realistic phase misalignment with $\cos 2\omega_0 t$ is θ_2:

$$v_{gs} = \pm A \sin\omega_0 t + A_2 \cos(2\omega_0 t + \theta_2) + n_{f\text{A,B}} \tag{4.7}$$

The upconversion of $n_{f\text{A,B}}$ to high-frequency current noise in i_{ds1} is illustrated in Fig. 4.2(a).

4.2.1 Direct Upconversion

Plugging (4.7) into (4.6), the upconverted $1/f$ noise component in i_{ds1} around ω_0 (i.e., H1) is differential (as gathered by the $\pm$ sign):

$$i_{n1} = \pm G_{12} \sin\omega_0 t \cdot n_{f\text{A,B}} \mp G_{13} \sin(\omega_0 t + \theta_2) \cdot n_{f\text{A,B}} \tag{4.8}$$

where upconversion transconductances $G_{12} = 2a_2 A$ and $G_{13} = 3a_3 A A_2/2$. The first term in (4.8) is induced by the 2^{nd}-order nonlinearity. It is in-phase

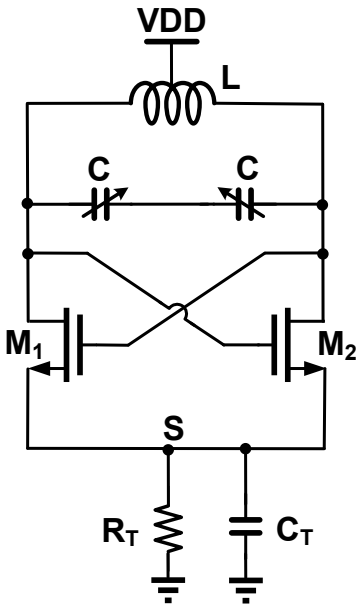


Figure 4.3: A 60 GHz oscillator testbench to verify the contribution of CM $1/f$ noise in the differential g_m-pair to PN.

with the fundamental oscillation current signal, and can only create amplitude noise. The second term in (4.8) is induced by the 3$^{\text{rd}}$-order nonlinearity. Decomposing $n_{f\text{A,B}}$ into CM and differential-mode (DM) components, its DM part clearly cannot introduce PN. For the CM component, if $\theta_2 \neq 0$ or π, it directly induces PN [54], as illustrated in Fig. 4.2(b).

A large impedance at dc (e.g., an ideal current source) that is in series with the differential g_m-pair can suppress the $1/f$ noise in CM to some extent. To verify the this derivation, a testbench is introduced, as shown in Fig. 4.3. The oscillator in this testbench is designed at 60 GHz, and C_T =10 pF to ensure a small impedance at 60 GHz. R_T varies from 0 to 200 Ω. The dc current consumption is kept unchanged by adapting the VDD to the variation of V_S and maintaining a constant dc bias voltage on M_1 and M_2 (i.e., VDD$-V_S$). Fig. 4.4 shows the simulated phase noise with different R_T. As we can see, the phase noise at 10 MHz offset are the same, which is ensured by the same current consumption. At 1 MHz offset and below, the phase noise profile deviates from the 20 dB/dec slope. There is a clear trend that the phase noise is improved with increasing R_T. The $1/f^3$ noise corner is reduced from 1 MHz

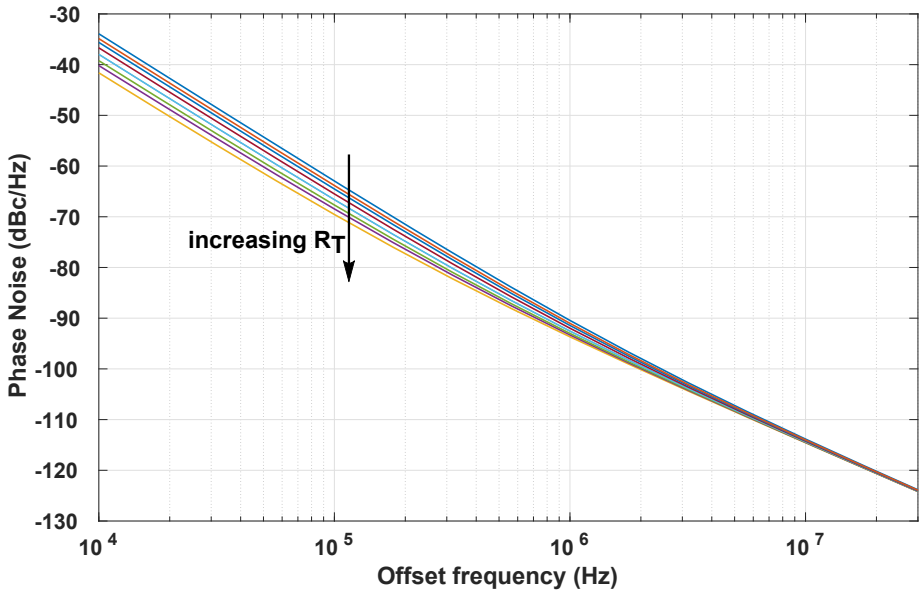


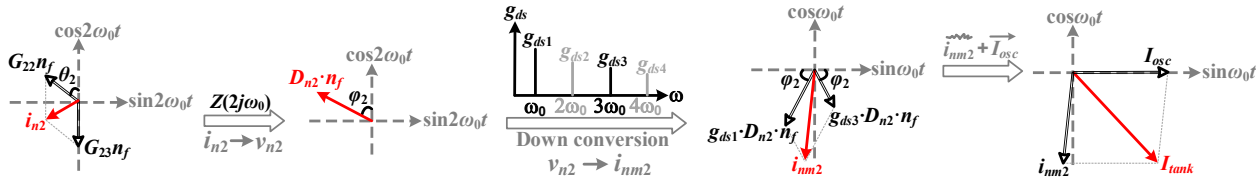
Figure 4.4: Simulated PN of the oscillator in Fig. 4.3 with varying R_T.

to 100 kHz by increasing R_T from 0 to 200 Ω. This testbench validates that a the CM $1/f$ noise in differential g_m-pair is a dominant noise source that induces $1/f^3$ noise, and it can be suppressed by a large dc impedance in series with the differential g_m-pair. Therefore, this DCO employs the tail current source, M_T. However, in 28 nm CMOS, the dynamic output impedance of transistors, r_{ds}, is rather small. Also, the limited voltage headroom and large-signal operation push M_T close to, and momentarily into, the triode region, which further limits its r_{ds}. Therefore, the $1/f$ upconversion to PN from $M_{A,B}$ is still significant.

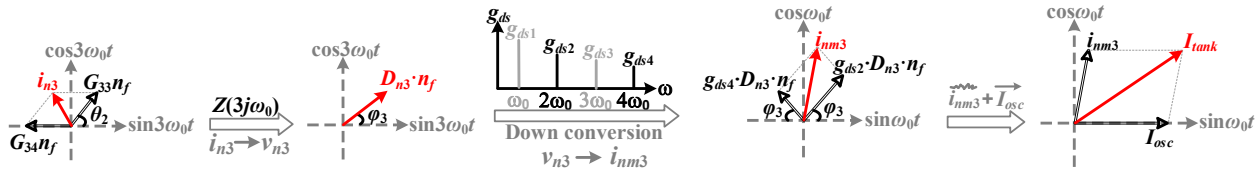
With the relatively small tail-current impedance at dc, there are two possible ways to suppress the direct $1/f$ upconversion in $M_{A,B}$: (1) reducing G_{13} by minimizing the H2 voltage [i.e., A_2 in (4.7)] in v_{gs} of $M_{A,B}$, which essentially requires minimizing Z_{trans2}; (2) forcing $\theta_2 = 0$ or π by tuning the CM Z_{trans2} to resistive at H2.

4.2.2 Indirect Upconversion

The upconverted $1/f$ noise current around H2 (through 2$^{\text{nd}}$ and 3$^{\text{rd}}$-order nonlinearities) is CM:



(a)



(b)

Figure 4.5: Indirect conversion to PN from upconverted flicker noise around: (a) 2nd harmonic frequency; (b) 3rd harmonic frequency.

$$i_{n2} = -G_{23}\cos 2\omega_0 t \cdot n_{f\mathrm{A,B}} + G_{22}\cos(2\omega_0 t + \theta_2) \cdot n_{f\mathrm{A,B}} \tag{4.9}$$

where $G_{23} = a_3 A^2/2$ and $G_{22} = 2a_2 A_2$. That current flows into the CM impedance (annotated as Z_2) that connects the drain with source of cross-coupling transistors via the path from the LC tank through VDD-VSS supply rails to M_T, and induces a voltage swing at H2

$$v_{n2} = D_{n2} \cdot n_{f\mathrm{A,B}} \cdot \cos(2\omega_0 t + \varphi_2) \tag{4.10}$$

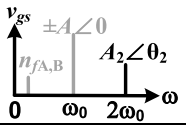
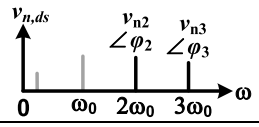
where $D_{n2} = |Z_2 \cdot i_{n2}/n_{f\mathrm{A,B}}|$ is upconversion gain, and φ_2 is the extra phase shift introduced by the reactive tank impedance at H2 in addition to the phase of i_{n2}. v_{n2} mixes with the fundamental and H3 components (differential) in $g_{ds}(t)$ of $M_{A,B}$ and induces a channel noise current i_{nm2}:

$$\pm n_{f\mathrm{A,B}} \cdot [G_{x23} \cdot \sin(\omega_0 t - \varphi_2) - G_{x21} \cdot \sin(\omega_0 t + \varphi_2)] \tag{4.11}$$

where $G_{x21} = D_{n2}{\cdot}g_{ds1}/2$, $G_{x23} = D_{n2}{\cdot}g_{ds3}/2$; g_{ds1} and g_{ds3} are the fundamental and H3 components in $g_{ds}(t)$. Also, only the CM component in $n_{f\mathrm{A,B}}$ will modulate the phase to create PN. This procedure is illustrated in Fig. 4.5(a).

The upconverted $1/f$ noise current around H3 (through 4th and 3rd-order nonlinearities, respectively) is differential

Table 4.1: Summary of direct and indirect $1/f$ noise upconversion mechanisms and the solutions

Mechanism	Root cause	Possible solutions	Design choices	Implementation in this work
Direct conversion	out-of-phase harmonics in v_{gs} 	minimize A_2	minimize Z_{trans2}	extra series *LC* resonance at H2 for explicitly defined CM path; weak CM magnetic coupling at H2 in transformer
		tune θ_2=0	tune Z_{trans2} resistive	N/A
Indirect conversion	out-of-phase upconverted $1/f$ noise at H2 and H3 in v_{ds} 	minimize v_{n2} and v_{n3}	minimize noise current at H2 and H3	N/A
			minimize Z_2 and Z_3	N/A
		tune φ_2=0 and φ_3=0	tune Z_2 and Z_3 resistive	extra series *LC* resonance at H2 for explicitly defined CM path; Z_2 and Z_3 resonate at H2 and H3

$$i_{n3} = \mp G_{34} \sin 3\omega_0 t \cdot n_{f\mathrm{A,B}} \pm G_{33} \sin(3\omega_0 t + \theta_2) \cdot n_{f\mathrm{A,B}} \tag{4.12}$$

where $G_{34} = a_4 A^3/2$ and $G_{33} = 3a_3 A A_2/2$. It flows into the LC tank and induces differential voltage swing at H3:

$$v_{n3} = \pm D_{n3} \cdot n_{f\mathrm{A,B}} \cdot \sin(3\omega_0 t + \varphi_3) \tag{4.13}$$

where $D_{n3} = |Z_3 \cdot i_{n3}/n_{f\mathrm{A,B}}|$, Z_3 is the tank impedance at H3, and φ_3 is the extra phase shift introduced by the reactive tank impedance at H3 in addition to the phase of i_{n3}. v_{n3} is mixed with H2 and H4 components (CM) in $g_{ds}(t)$ of $M_{A,B}$ and induces a channel noise current i_{nm3}:

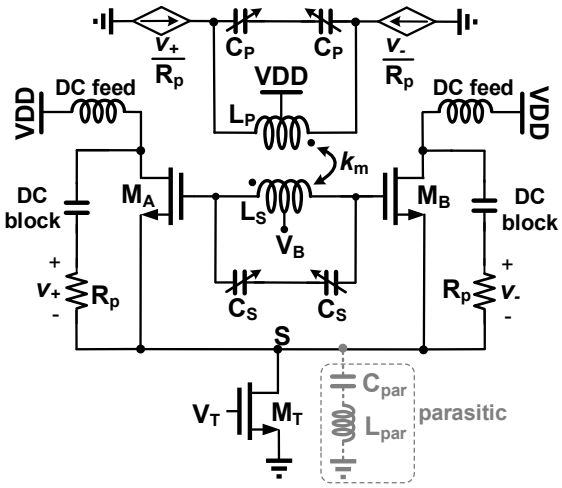
$$\pm n_{f\mathrm{A,B}} \cdot [G_{x32} \cdot \sin(\omega_0 t + \varphi_3) - G_{x34} \cdot \sin(\omega_0 t - \varphi_3)] \tag{4.14}$$

where $G_{x32} = D_{n3} \cdot g_{ds2}/2$, $G_{x34} = D_{n3} \cdot g_{ds4}/2$, g_{ds2} and g_{ds4} are H2 and H4 components in $g_{ds}(t)$. Again, only the CM component in $n_{f\mathrm{A,B}}$ will modulate the phase to create PN. This procedure is also illustrated in Fig. 4.5(b). The i_{nm2} and i_{nm3} are the current noise in i_{ds2}.

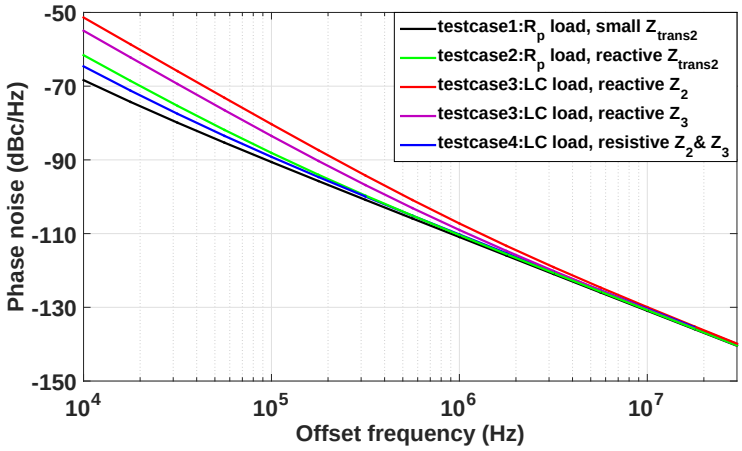
In CMOS transistors, the higher-order nonlinearities are much weaker than the lower-order ones. Therefore, $a_4 < a_3 < a_2$ and $G_{33} < G_{22}$. Moreover, $g_{ds2} < g_{ds1}$ and $g_{ds4} < g_{ds3}$. Depending on the magnitude of reactive part in Z_2 and Z_3, contributions of the upconverted flicker noise i_{n2} and i_{n3} to the oscillator PN vary.

In order to reduce the indirect $1/f$ upconversion through self-mixing, there are two possible solutions: 1) the H2 and H3 noise voltage components in v_{ds} of $M_{A,B}$ (i.e., v_{n2} and v_{n3}) are minimized by suppressing the harmonic noise current in i_{ds} (i.e., i_{n2} and i_{n3}) or minimizing Z_2 and Z_3; 2) φ_2 in v_{n2} and φ_3 in v_{n3} are forced to 0 by tuning the CM Z_2 and DM Z_3 to resistive. These requirements align with those in the direct upconversion mechanisms. Adding a tail filter LC tank resonating at H2 would suppress the H2 current [64]. However, the extra LC tank occupies larger area. To avoid that, two other possible approaches can be applicable: tuning Z_2 and Z_3 to be resistive by creating resonances at H2 and H3; tuning the reactive Z_2 and Z_3 to be very small (e.g., very large capacitive or small inductive loading). Table 4.1 summarizes the direct and indirect $1/f$ noise upconversion mechanisms, as well as the corresponding suppressing solutions.

A circuit simulation testbench is introduced in Fig. 4.6(a) to validate the proposed theory. It is designed to oscillate at 20 GHz. The drain nodes of $M_{A,B}$ are electrically isolated from the LC tank's primary winding by means of a unidirectional signal flow. They are terminated with R_p, i.e., the tank impedance at ω_0. R_p is maintained much lower than the reactive impedance of the C_{ds} in $M_{A,B}$. It ensures that the drain current (i_{ds}) of $M_{A,B}$ only flows through resistive loads. The oscillation current is injected into the tank through an ideal voltage-controlled current source, whose transconductance is $1/R_p$. Z_2 and Z_3 are designed to be strongly reactive. Since the weak CM magnetic coupling in the 1:2 transformer greatly attenuates the H2 signal transferring from the primary (drain) to the secondary (gate) winding, Z_{trans2} is small when no parasitic appears in M_T or the VDD-VSS supply rails. In this case (test case 1), simulated PN shows that its $1/f^3$ corner is not visible (i.e., <10 kHz), as indicated by the black curve in Fig. 4.6(b). Varying the reactive impedance value of Z_2 or Z_3 (e.g., by means of single-ended and differential tank capacitors) has little effect on the $1/f^3$ corner. However, by adding a reactive impedance at H2 between node S and VSS (L_{par} and C_{par} to account for the parasitics in tail current and VDD/VSS supply rails) (test



(a)



(b)

Figure 4.6: (a) Testbench to avoid PN indirect upconversion from $1/f$ noise, and (b) simulated PN with this and Fig. 4.7 testbenches.

case 2), the reactive part in Z_{trans2} increases. It forces $\theta_2 \neq 0$ or π in (4.7) and so the simulated $1/f^3$ corner raises to 80 kHz. This validates the direct upconversion mechanism described above.

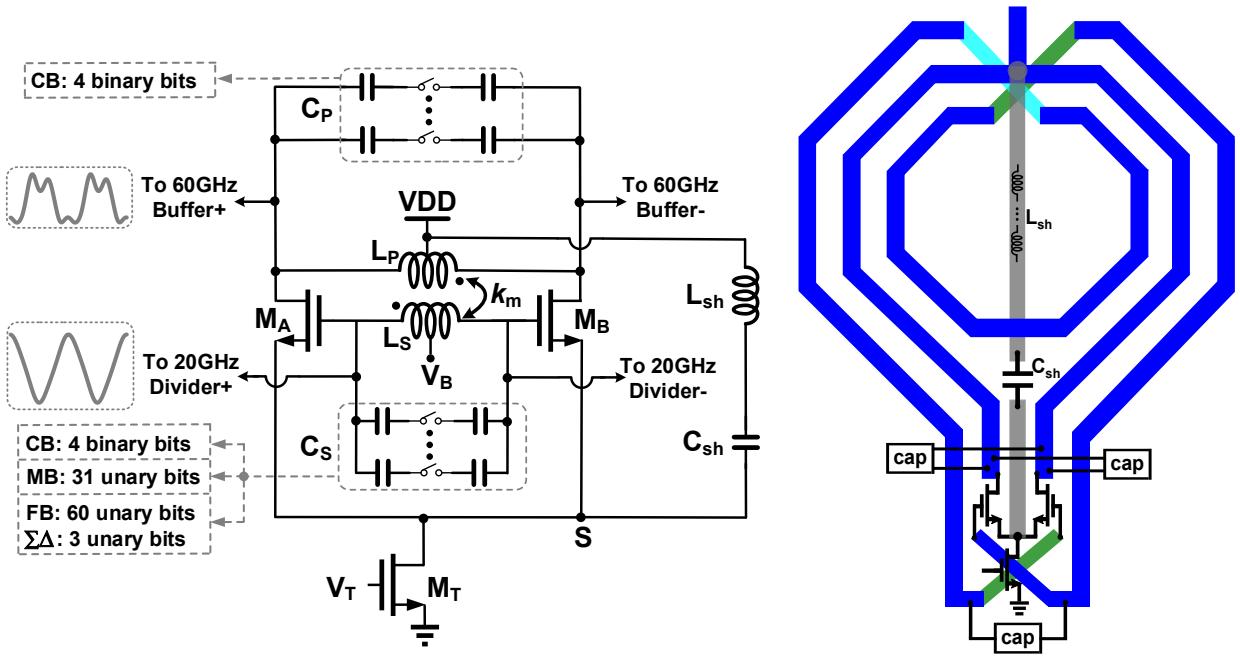
A practical testbench is then configured as in Fig. 4.7 with the same 20 GHz LC tank and transistors as in the Fig. 4.6(a) testbench. Parasitics in VDD-VSS supply rails are not included to keep Z_{trans2} small. When Z_2 or Z_3 is reactive (test case 3), its $1/f^3$ corner is 1 MHz or 450 kHz, respectively. Test cases 1 and 3 suggest that indirect upconversion through self-mixing is a

major mechanism for the $1/f$ noise upconversion to PN. After tuning Z_2 and Z_3 to be resistive (test case 4), the $1/f^3$ corner drops to 30 kHz. Fig.4.6(b) shows the simulated PN with different test cases. It confirms the proposed direct and indirect mechanisms.

4.3 Suppression of Flicker Noise Upconversion to Phase Noise

In this design, the LC tank is tuned for the ancillary resonance at H3, and the H3 component is filtered out at v_{gs}. This coincides with the criteria associated with H3. In traditional single-resonance LC oscillators with reasonably high Q-factors, since H3 is far away from the resonance, the tank impedance at H3 is low. Therefore, the criterion for H3 can be easily satisfied. At H2, the direct and indirect upconversion mechanisms set up a criterion for the CM impedance in two paths: Z_{trans2} and Z_2. However, both paths include the VDD-VSS routing path, which is vulnerable to parasitic inductance and capacitance in layout and difficult to estimate. This is especially true for inductors/transformers with odd number of turns, since the center-tap there is on the opposite side of the terminals. In order to robustly define the CM H2 impedance, the VDD-VSS routing path should be bypassed.

A generic technique to suppress the $1/f$ noise upconversion is proposed here and applied to this DCO. The schematic and layout implementation are revealed in Fig. 4.7. An extra series LC branch (L_{sh} and C_{sh}) is introduced between VDD (transformer's center-tap) and a common-source node of $M_{A,B}$ (node S). Two conditions should be satisfied: 1) the impedance of this series LC feed resonates at H2; 2) the LC network between the drain of $M_{A,B}$ and node S (i.e., Z_2) resonates at H2 in CM. Condition #1 bypasses the practically ill-defined path between VDD and node S with a short-circuit path at H2. Since the H2 current path is explicitly defined by this auxiliary LC branch, it is not subjected to any normal parasitic effects in the VDD/VSS routing. In this way, Z_{trans2} and H2 component in v_{gs} are ensured to be small due to the short path



(a) (b)

Figure 4.7: (a) Schematic and (b) concept layout of the DCO with the proposed $1/f$ noise upconversion suppression technique.

between node S and center-tap at H2. Therefore, condition #1 also prevents the $1/f$ noise upconversion through direct conversion mechanism. Condition #2 ensures that H2 in v_{ds} is in-phase. It reduces the $1/f$ noise indirect upconversion through self-mixing. The respective solutions to suppress the direct and indirect upconversion in the proposed technique are also summarized in Table 4.1. This idea provides an extra design freedom for the $1/f$ noise upconversion reduction at no cost of area or power.

The proposed 20 GHz DCO with the $1/f$ noise upconversion suppression technique is implemented as part of a 60 GHz frequency synthesizer in TSMC 28 nm LP CMOS. The measured $1/f^3$ corner reduced 300–400 kHz across the frequency tuning range. The detailed measurement results will be described in Chapter 5.

Chapter

5

Millimeter-Wave Fractional-N ADPLL Implementation

This chapter describes the implementation details of a low-noise 60-GHz fractional-N ADPLL. It aims to reduce the phase noise (PN) in both the flicker ($1/f^3$) and thermal ($1/f^2$) regions, while minimizing the power consumption. The significant improvement of DCO PN gives more margin and freedom to the performance of other loop components. As a result, a medium-level resolution TDC subsystem, in combination with a relatively narrow loop bandwidth, is employed for low spurs while still achieving low integrated PN. A pair of digital-to-time and time-to-digital converters (DTC-TDC) comprises the phase detection circuit. Sigma-delta ($\Sigma\Delta$) dithering is applied to the DTC to attenuate fractional spurs. A 20 GHz harmonic soft-cancellation technique is proposed. It achieves 10 dB more suppression of the 20 GHz harmonic than with other solutions. Together with the low-k_m transformer matching network, the proposed 60 GHz buffer provides 43–51 dB attenuation at 20 GHz, while

achieving wide bandwidth. The architectural level design choices are discussed in Section 5.1. The proposed 60 GHz ADPLL architecture is presented in Section 5.2, with a noise budget analysis of each block. The detailed DCO design are depicted in Section 5.3. The proposed 20 GHz harmonic soft-cancellation technique is given in Section 5.4. Section 5.5 presents an implementation of frequency dividers. The phase detection subsystem, which includes the high-speed counters, DTC-TDC circuits and the calibration algorithms, are revealed in Section 5.6. It is followed by the loop filters in Section 5.7. Finally, experimental results are provided in Section 5.8.

5.1 60-GHz ADPLL Design Choices

The performance budget on each building block of the 60 GHz ADPLL should be discussed, prior to the circuit-level implementation. With an aggressive performance requirement on the oscillator, the design challenges of the phase detection circuits will be reduced. And, the opposite is also true. Several approaches have been reported to achieve low integrated PN (IPN) of mm-wave PLLs. In [19] and [65], a sub-sampling technique was applied to a 60 GHz integer-N analog PLL. Wide loop bandwidth (BW) of >1 MHz was used to suppress the VCO PN and to achieve good IPN. In [18], low IPN was reported in a 60 GHz integer-N charge-pump (CP) PLL by means of a high frequency reference (FREF) clock of 135 MHz and wide BW. However, those techniques cannot be easily migrated to fractional-N PLLs, where the loop components contribute significant noise. A 60 GHz fractional-N all-digital PLL (ADPLL) with a fine-resolution (450 fs) time-to-digital converter (TDC) was introduced in [66] to achieve low IPN. Again, with a high FREF of 100 MHz and power-hungry fine-resolution TDC, the PLL BW was set to >2 MHz to suppress the oscillator PN. However, complicated offline calibration procedures and stringent timing conditions are required. Wide loop BW is not optimal for spur suppression, either. Similar approaches (i.e., 125 MHz FREF, wide BW and fine-resolution TDC) are adopted in a W-band ADPLL in [67]. In [68], low IPN was achieved in a fractional-N ADPLL with a fine resolution (310 fs) DTC and 20 GHz DCO. However, complicated digital predistortion algorithms were necessary to improve the DTC linearity. An extra LC tank was employed for tail filtering in the DCO for better PN. All the aforementioned solutions demand low-noise loop components to suppress the oscillator PN.

In this thesis, we propose an alternative approach to realize the fractional-N 60 GHz generation at low PN. Instead of pursuing the minimum noise from the reference and feedback loop, the oscillator PN is significantly improved by the proposed $1/f^3$ noise suppression technique and 3rd-harmonic boosted 20 GHz DCO. Meanwhile, implicit frequency tripling is achieved inside the

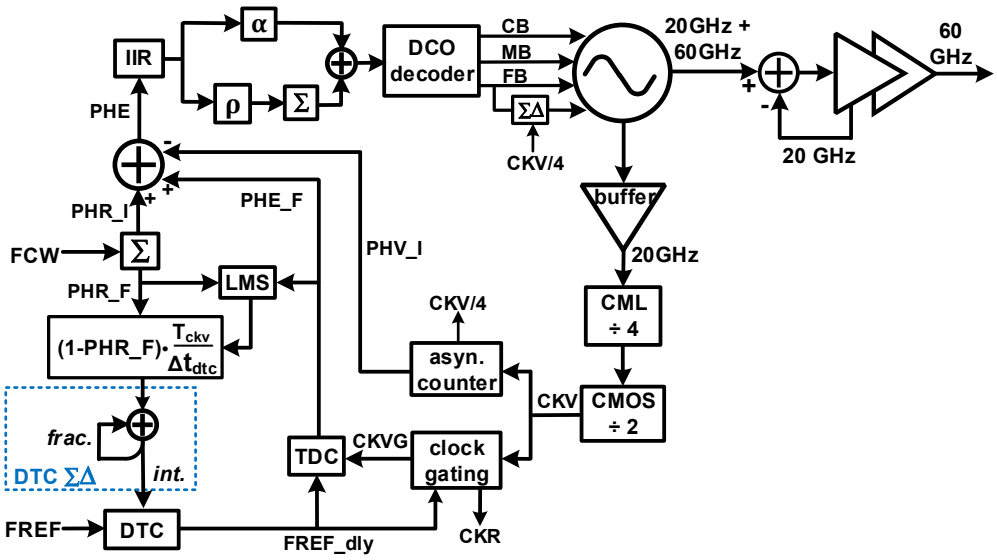


Figure 5.1: The proposed 60 GHz digital frequency synthesizer architecture.

DCO. Since the DCO PN is improved, the constraints on the loop components are simplified. It gives a margin for narrower BW to suppress the TDC quantization noise and spurious tones, while maintaining low IPN. A TDC sub-system with medium resolution is adopted for a better power efficiency and linearity. Furthermore, the implicit tripling in the DCO eliminates frequency dividers or multipliers that operate directly at mm-wave frequencies. The power efficiency is further enhanced with reduced design complexity.

5.2 60-GHz ADPLL Architecture

The system diagram of the ADPLL-based 60 GHz digital frequency synthesizer is shown in Fig. 5.1 [61]. At its center lies a harmonic-boosting 20 GHz DCO featuring improved PN in both the $1/f^3$ and $1/f^2$ regions. Strong 3$^{\text{rd}}$ harmonic at 60 GHz is generated alongside the 20 GHz fundamental in the DCO. The co-generated 3$^{\text{rd}}$ harmonic is extracted and fed forward to the 60 GHz output buffer which simultaneously suppresses the 20 GHz component. In the feedback path, the 20 GHz signal is prescaled by ÷4 CML and ÷2 CMOS dividers to generate variable clock (CKV) for phase detection in the ADPLL. The directly available 60 GHz signal from the DCO exempts the

demands for further frequency multiplication in the feed-forward path. In this way, the conventional 60 GHz frequency dividers or doublers/triplers to 60 GHz, which typically suffer from limited locking range and large power consumption, are avoided. This simplifies the design and enhances its robustness. Compared to the PLLs with 60 GHz fundamental oscillators, the relatively smaller 60 GHz swing from the 20 GHz DCO may require more power consumption in the buffer to amplify it and drive the loads. Similar scenario also happens at the output of the conventional frequency triplers [35]. In this design, the 3rd harmonic swing is boosted in the DCO. This relaxes the requirements on the gain of the buffer and reduces the power overhead in it. Overall, these approaches help to improve the power efficiency of the 60 GHz frequency synthesizer.

An 8-bit counter digitizes the integer part of the CKV phase. The resulting PHV_I[k] is compared to the integer part of the reference phase PHR_I[k] to generate the integer part of phase error, PHE_I[k]. The FREF clock is delayed by a digital-to-time converter (DTC), whose delay is determined by the fractional part of reference phase (PHR_F[k]). The DTC is controlled by a $\Sigma\Delta$ modulator ($\Sigma\Delta$M) and covers a range that is a bit larger than one CKV period. A least-mean-square (LMS) algorithm [69] runs in the background to calibrate the DTC gain. The DTC output, FREF_dly, is used to clock-gate the CKV to generate CKVG, as well as the retimed clock, CKR, for the digital logic [70]. The TDC digitizes the phase difference between CKVG and FREF_dly and provides, after the normalization, the fractional phase error PHE_F[k]. A small TDC detection range can slow down the transient settling or locking time of the ADPLL in some cases. For a more robust operation, it covers a detection range that is 40% of the CKV period. Furthermore, during the settling process, once TDC overflow or underflow is detected, the TDC output is overwritten by a maximum or minimum value. It facilitates the settling speed [70]. After the PLL is locked, only a few cells in the middle of the TDC chain are active. The composite phase error, PHE[k]=PHE_I[k]+PHE_F[k], is fed to the digital loop filter (LF), which

comprises a proportional-integral (PI) controller and a 4th-order IIR filter. The LF output is fed to the DCO as its tuning word through a decoder.

In this work, the PLL bandwidth is optimized for low IPN. As analyzed in Chapter 2, the high $1/f^3$ noise corner of the oscillators could limit the choice of the loop bandwidth. To have less constraints on the loop bandwidth and other loop components, the $1/f^3$ noise of the DCO is targeted to be low with the techniques proposed in Chapter 4. Wideband carrier recovery loops in the transceiver baseband can filter out the close-in PN [71]. However, in some applications (such as radars), they may not be available. This work targets low IPN from the PLL itself. To achieve this goal, the noise contribution from FREF, DTC, TDC and frequency dividers, which are low-pass filtered by the loop, should also be minimized. FREF noise floor is predefined by the crystal oscillator and tends to be conservatively around -150 dBc/Hz for a 40 MHz FREF used in this design. The noise floor of the frequency dividers and DTC are designed to be significantly (about 7 dB) below the FREF noise floor, so that they have negligible contribution to the ADPLL output PN. TDC quantization (Q)-noise can be reduced by improving its resolution, typically at the cost of a larger power consumption and degraded INL linearity that will create fractional spurs [72]. However, significant lowering of the TDC Q-noise below that of FREF or DCO's contribution cannot further improve the in-band PN. With the targeting of low $1/f^3$ DCO, its in-band contribution should be less than or comparable to that of FREF. For the optimal power efficiency and linearity, the TDC Q-noise is designed at the same level as the FREF noise floor. This corresponds to the TDC resolution of 3 ps with 40 MHz FREF.

The DTC $\Sigma\Delta$M quantization noise induced PN is given by

$$L_{dtc}(\Delta f) = \frac{1}{12} \cdot \frac{(\Delta t_{dtc})^2}{f_{ref}} \cdot (2\pi f_o)^2 \cdot \left[2\sin(\frac{\pi \Delta f}{f_{ref}})\right]^2 \cdot |H_{cl}(\Delta f)|^2 \qquad (5.1)$$

where Δt_{dtc} is the DTC resolution, f_{ref} is the FREF clock frequency, f_o is the PLL output frequency, and $H_{cl}(\Delta f)$ is the close-loop transfer function of the

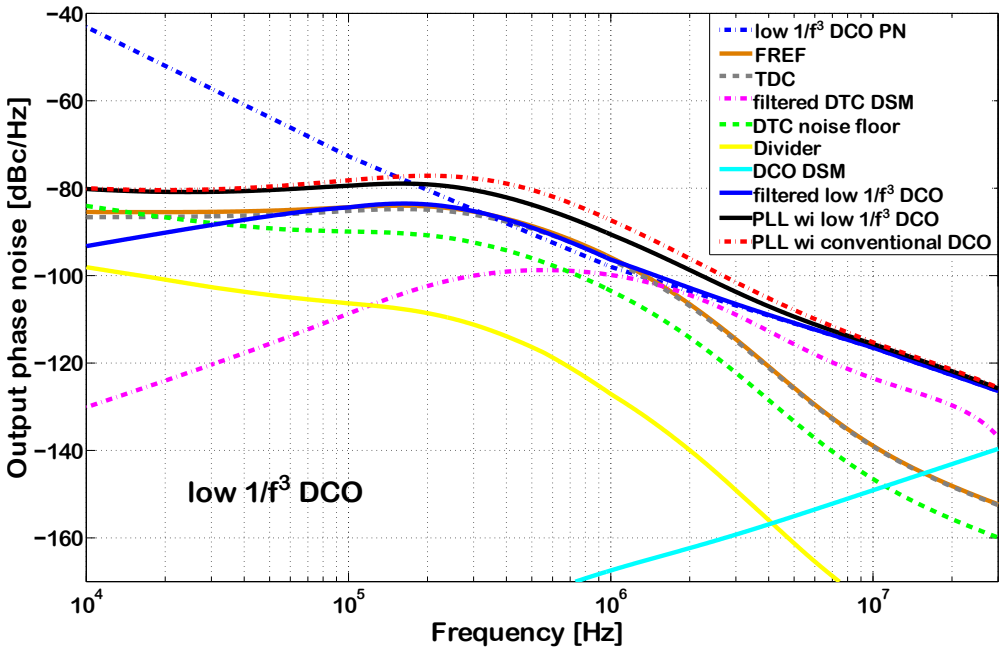


Figure 5.2: PN of the proposed 60 GHz digital frequency synthesizer predicted by s-domain model.

DTC noise to the output. Besides the PI controller, the IIR filter in $H_{cl}(\Delta f)$ provides extra attenuation to the high-frequency $\Sigma\Delta$M quantization noise. The DTC resolution is optimized so that $L_{dtc}(\Delta f)$ has marginal contribution to the IPN. In this design, the DTC resolution should be finer than 16 ps so that its degradation on the IPN is less than 0.5 dB. To reduce the TDC dynamic range, fine DTC resolution is desired as well. On the other hand, with better resolution, more delay unit cells are required in the DTC to cover one CKV period. The long DTC delay chain is typically more prone to linearity degradation. As a trade-off, the DTC resolution is chosen as 12 ps in this design. With all the noise sources included, the ADPLL output noise predicted by the s-domain model is shown in Fig. 5.2.

5.3 60-GHz DCO

Based on the techniques described in Chapters 3 and 4, a low $1/f^3$ noise DCO with implicit frequency tripler is employed to build up the proposed 60-GHz ADPLL. The DCO operating principle and its $1/f$ noise upconversion

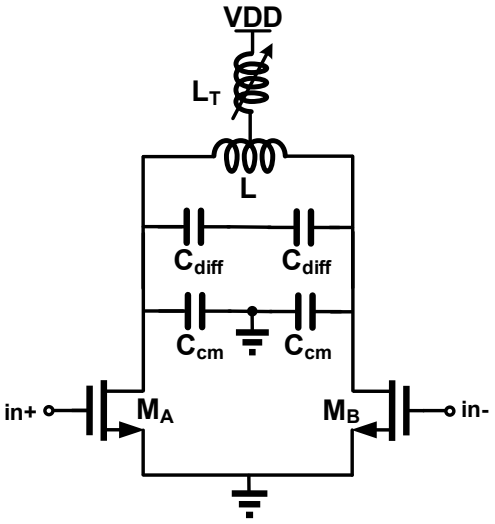


Figure 5.3: Testbench to verify the effect of H2 swing in v_{ds} on I_{DH3}.

suppression have been discussed there. In this section, we focus on the implementation considerations when used in the ADPLL. The schematic and layout illustration are shown in Fig. 4.7.

5.3.1 Third Harmonic Current Boosting

As analyzed in Section 3.5.2, there is an upper bound for V_{DH3}/V_{DH1} with increasing $R_{\mathrm{p3}}/R_{\mathrm{p1}}$. To raise the third harmonic swing, it is desirable if I_{DH3}/I_{DH1} can be boosted as well. The mixing product of the fundamental and second harmonic inside the negative-g_m devices is a source of the H3 current I_{DH3}. As revealed in Chapter 4, the fundamental component in v_{gs} of the g_m devices can mix with the H2 harmonic in both v_{gs} and v_{ds}. A large H2 swing is desired to increase I_{DH3}. The CM impedance of the LC tank at H2 frequency affects the level of the H2 voltage swing. As a consequence, it also influences the H3 current I_{DH3} level. As described in Chapter 4, the H2 harmonic in v_{gs} is suppressed in this design by minimizing Z_{trans2}. It is interesting to investigate the dependency of I_{DH3} on the H2 harmonic in v_{ds} by varying Z_2.

A testbench is introduced to verify this effect, as shown in Fig. 5.3. The input is a differential 20 GHz signal with the same amplitude as in the DCO.

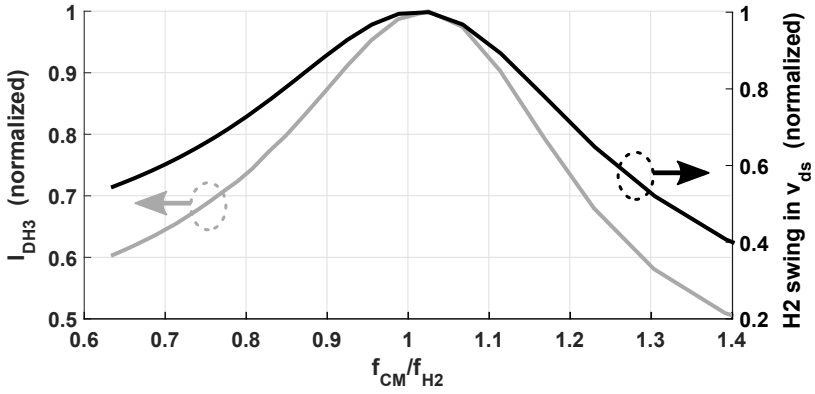


Figure 5.4: Dependence of H2 swing in v_{ds} and I_{DH3} on the resonant frequency of the CM impedance Z_2.

The LC tank is tuned to resonate at 60 GHz differentially. Half of the tank capacitance is single-ended (denoted as C_{cm}). A CM inductance L_T is swept to change the CM resonant frequency. In this way, Z_2 is varied without affecting the DM impedance. Fig. 5.4 shows the the normalized H2 swing at 40 GHz in v_ds of $M_{A,B}$ and H3 current I_{DH3} with respect to different CM resonant frequencies (f_{CM}). As we can see, the H2 swing in v_{ds} and I_{DH3} is maximized when f_{CM} equals the H2 frequency (f_{H2} =40 GHz). It is aligned with the criteria for the suppression of flicker noise upconversion. Therefore, the third harmonic current boosting comes as a byproduct of the technique proposed in Chapter 4.

5.3.2 Capacitor Bank Design

In an ADPLL, the DCO frequency is discretely tuned by its tuning word. To avoid spurious tones and reduce quantization noise, high-frequency $\Sigma\Delta$ dithering and fine frequency resolution is often required. To avoid the performance being contaminated by DCO quantization, the quantization noise level is expected to be below the DCO PN at the offset frequencies of interest. The phase noise contributed by DCO quantization with an n^{th} order sigma-delta dithering is

$$L(\Delta f) = \frac{1}{12} \cdot \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \cdot \frac{1}{f_{dith}} \cdot \left[2\sin\left(\frac{\pi \Delta f}{f_{dith}}\right)\right]^{2n} \tag{5.2}$$

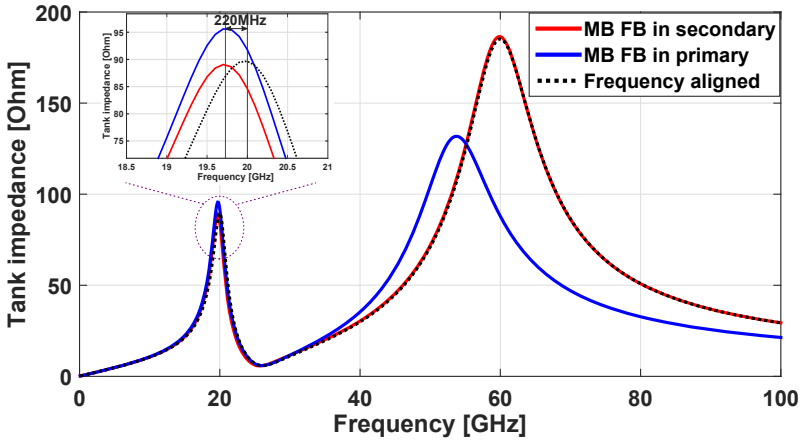


Figure 5.5: Simulated tank impedance with MB and FB in primary and secondary sides.

where f_{dith} is the sigma-delta dithering clock frequency. In this design, the $\Sigma\Delta$ dithering is clocked by the DCO $\div$32 output, which is around 625 MHz. With 3 MHz frequency resolution and 2$^{\text{nd}}$-order sigma-delta modulation, the PN induced by DCO quantization is -169 and -149 dBc/Hz, respectively, at 1 and 10 MHz offset. It is much lower than the DCO PN. At $f_{dith}/2$, the quantization PN peak around -127 dBc/Hz, which is comparable to the noise floor of the DCO buffer. Since the quantization PN level is so low, it does not degrade the IPN or violate the emission mask of any wireless standard. Further refining the DCO frequency resolution can reduce the quantization PN. However, smaller frequency resolution requires more bits in the fine-tuning capacitor bank to cover a specific frequency range. The bulky fine-tuning capacitor bank and long interconnect routing typically degrade the DCO PN and tuning range. In this design, the DCO frequency resolution is chosen to be 3 MHz/bit.

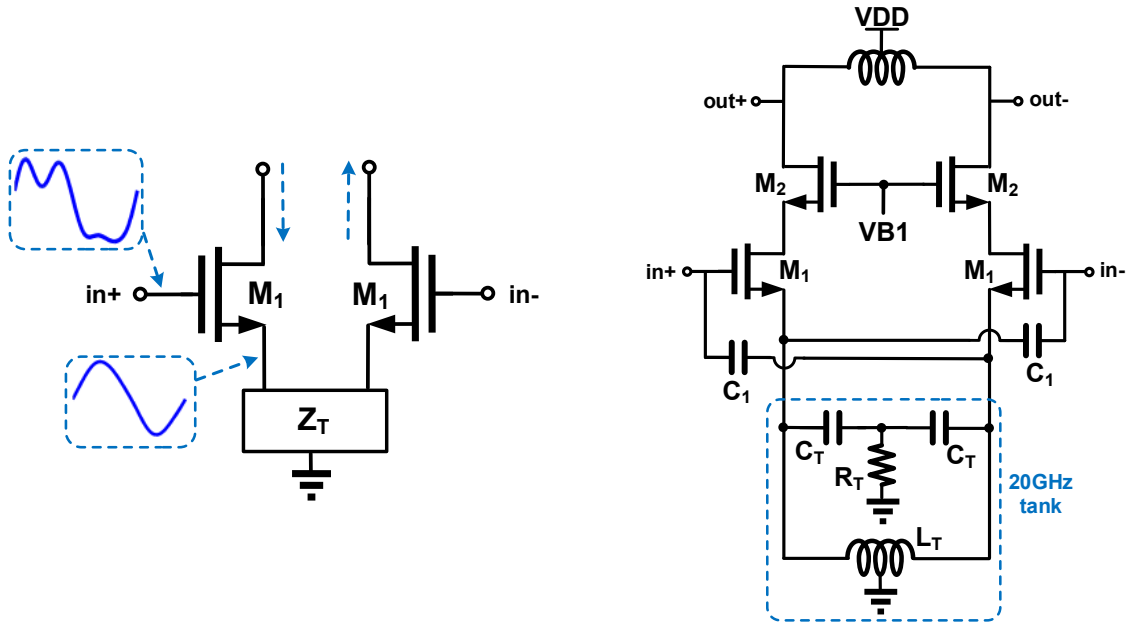
The DCO is segmented into 4 switched-capacitor banks: 4-bit binary coarse tuning (CB), 31-bit unary mid-coarse tuning (MB), 60-bit unary fine tuning (FB), and 3-bit unary FB for a high-speed $\Sigma\Delta$M. In this DCO, the capacitance in both primary (C_p) and secondary (C_s) sides tunes the oscillation frequency. In order to ensure the 2$^{\text{nd}}$ resonance tracks the third harmonic of oscillation frequency (H3), C_s and C_p need to maintain a ratio of $C_s/C_p = 2$. The CB is replicated at the primary and secondary windings with 1:2 capacitance ratio,

both of which are tuned simultaneously. It covers the largest frequency tuning range. For the best third-harmonic tracking, it is desired to replicate MB and FB in both windings. Ideally, both C_s and C_p are desired to be placed as close as possible to the inductor and g_m devices. However, since there are many tuning bits in MB and FB, their replication leads to bulky C_p and C_s in layout. A long interconnect is required to bridge between the inductor and capacitor banks that are far away. It degrades the Q-factor and gives rise to parasitics. Fortunately, MB and FB only need to cover a small frequency range (twice the LSB of CB). It is possible to allocate these two banks to only C_s or C_p. Meanwhile, it should not come at the expense of too much frequency misalignment between the 2$^{\text{nd}}$ resonance and H3. Large variation in the 3$^{\text{rd}}$ harmonic impedance can cause dramatic amplitude and/or phase variation in the generated 3$^{\text{rd}}$ harmonic voltage signal. Without dedicated compensation, it can become an issue in some applications. In the transformer-based oscillator, the two resonant frequencies, ω_L and ω_H, are

$$\omega_{L,H}^2 = \frac{1+\zeta \pm \sqrt{(1+\zeta)^2 - 4\zeta(1-k_m^2)}}{2(1-k_m^2)}\omega_s^2 \tag{5.3}$$

where $\omega_s^2 = 1/(L_sC_s)$ and $\zeta = (L_sC_s)/(L_pC_p)$. Let's consider the case that MB and FB are allocated to C_s first. Switching the control codes of MB and FB from the middle to the lowest and highest, the oscillation frequency is tuned by ±220 MHz around 20 GHz, which is ±2 LSB of CB (i.e., ±10 fF single-ended capacitance). The 2$^{\text{nd}}$ resonance varies by ± 70 MHz. As shown in Fig. 5.5, the impedance magnitude and phase at H3 varies by only 0.8% and 0.8°, respectively. If MB and FB are allocated to C_p, the required ΔC_p is 4.7 times larger (i.e., ±47 fF single-ended capacitance) to achieve the same tuning range. In this case, the 2$^{\text{nd}}$ resonance is tuned by ± 6.14 GHz. The impedance magnitude and phase at H3 varies by 52% (from 185 down to 89 Ω) and -46.5°, respectively.

Consequently, MB and FB are only placed at the secondary winding for a simple and compact layout. As revealed above, the tuning range of MB and FB



(a) (b)

Figure 5.6: (a) Working principle, and (b) schematic of the subharmonic soft-cancellation 60 GHz buffer with LC output matching network

is small so that they will not introduce any significant misalignment between the 2nd resonance and H3 frequencies. The three tuning banks are sized for 260 MHz/bit, 35 MHz/bit and 3 MHz/bit unit steps (i.e., DCO resolution, K_{DCO}) at the 60 GHz carrier, respectively. The MB and FB cover $> \pm 2$ LSB of CB and MB, respectively, to ensure continuous tuning. The high-speed $\Sigma\Delta$M clocked at CKV/4 (625 MHz) reduces the DCO Q-noise. It can be programmed as a 1st or 2nd order.

5.4 20-GHz Component Suppression

The proposed PLL is intended for a wireless transceiver. In such a case as in many others, the undesired 20 GHz tone should be sufficiently attenuated to lie well below the spectrum mask of a transmitter or to meet the blocker tolerance of a receiver. To get a 'pure' spectrum at the 60 GHz carrier output, the 20 GHz fundamental DCO tone should be suppressed in the 60 GHz buffer path. Ideally, the buffer would only react to the H3 component, while

discarding the fundamental component. To achieve this effect, we propose a cancellation scheme of the 20 GHz component. Fig. 5.6(a) reveals the core idea in which the source of buffer's input transistor (M_1) follows the DCO's 20 GHz component, but sees the ground at 60 GHz. In other words, M_1 senses only the H3 component between its gate and source (i.e., v_{gs}). This requires a large impedance at 20 GHz, but a very low impedance (ideally zero) at 60 GHz. A parallel LC tank that resonates at 20 GHz is therefore placed between the source of M_1 and ground. Fig. 5.6(b) shows the schematic of the soft-cancellation technique in a 60 GHz buffer with LC output matching network. At 20 GHz, M_1 is source-degenerated by a large impedance provided by the 20 GHz tail tank. There should be no 20 GHz current flowing in M_1, thus no g_m gain there. The LC tank has a very low impedance ($<10\,\Omega$) at 60 GHz, hence the desired 60 GHz input signal experiences large g_m. Since the capacitive source degeneration at high frequencies in M_1 may cause stability concerns, neutralization capacitor C_1 is added differentially between the gate and source to ensure the DM stability. A dampening resistor $R_T = 10\,\Omega$ is inserted between the common node of the tail tank capacitors C_T and ground to ensure the CM stability. A simulated stability factor shows that this buffer is unconditionally stable.

Compared to the conventional buffers and notch filter solutions (Fig. 5.7) [73], the proposed suppression technique offers several advantages. It achieves a better 20 GHz component rejection, achieves more gain at 60 GHz, and prevents the generation of other harmonic contents (i.e., 40 and 80 GHz). With the same circuit parameters and input signal as that are used in this design, the performance of the proposed subharmonic soft-cancellation buffer (Fig. 5.6(b)) is simulated and compared against those in Fig. 5.7.

In the proposed buffer, the 20 GHz signal gain is

$$\frac{G_m \cdot Z_{load}(j\omega_0)}{1 + G_m \cdot Z_{tail}(j\omega_0)} \tag{5.4}$$

where G_m is the transconductance of the M_1. The effective transconductance

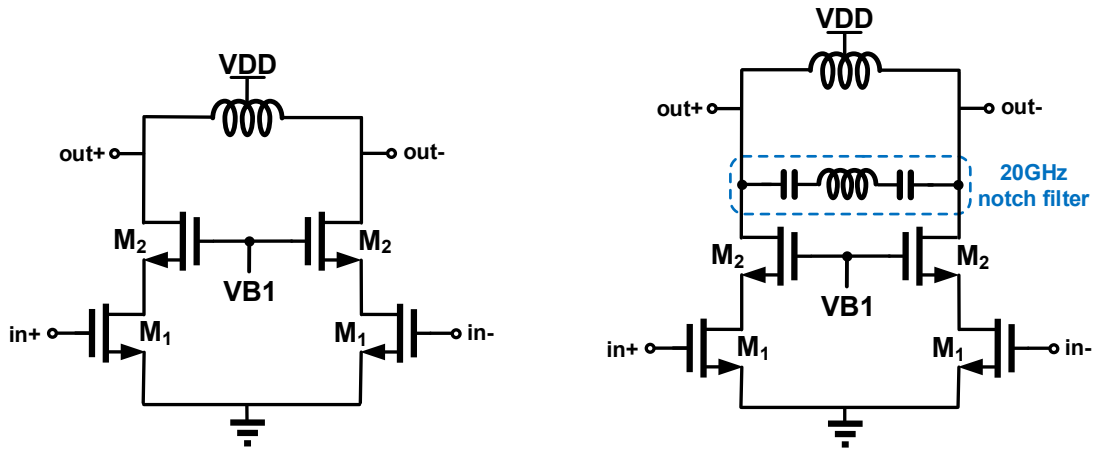


Figure 5.7: Schematic of (a) a conventional buffer, and (b) a buffer with notch filter at 20 GHz.

gain at 20 GHz is decreased by a ratio of $1 + G_m Z_{tail}(j\omega_0)$. Fig. 5.8 shows the simulated drain current in different buffers. With source degeneration by the 20 GHz LC tank, the 20 GHz drain current in the proposed buffer is reduced by 10–23 dB when compared to the other buffers. It validates the effectiveness of the proposed subharmonic soft-cancellation technique.

The proposed subharmonic soft cancellation technique also provides more gain to the signal of interest at 60 GHz. The input of the buffer is the 60 GHz signal accompanied by a large 20 GHz tone. It is well known that a large blocker signal can desensitize the low-noise amplifiers (LNAs) in the receivers. The large 20 GHz tone can also desensitize the buffer in a similar way. The input transistor (M_1) has nonlinearities with a large-signal excitation. In the conventional buffer and the buffer with notch filter shown in Fig. 5.7, the 20 GHz component directly presents in the v_{gs} of M_1:

$$v_{gs} = V_a \cdot \sin(3\omega_0 t) + V_b \cdot \sin(\omega_0 t) \tag{5.5}$$

where V_a and V_b are the amplitude of the 20 and 60 GHz inputs, and ω_0 is the angular frequency of the 20 GHz component. Recalling Eq. 4.6, the drain

current is

$$i_{ds} = a_0 + a_1 v_{gs} + a_2 v_{gs}^2 + a_3 v_{gs}^3 + \dots \tag{5.6}$$

At 60 GHz, the output current is (high-order nonlinearities beyond the third order are neglected)

$$a_1 V_a sin(3\omega_0 t) + \frac{1}{4} a_3 V_b^2 sin(3\omega_0 t) \cdot (6V_a - V_b) \tag{5.7}$$

Since $a_3/a_1 < 0$ [74], the second term (compression item) in Eq. 5.7 reduces the total drain current at 60 GHz if $V_b < 6V_a$. For the buffers in Fig. 5.7, $V_b = 2.5V_a$ as it is at the DCO output. The presence of a large 20 GHz component in v_{gs} of the input transistors decreases the 60 GHz output current. From Eq. 5.7, it is straightforward to conclude that lowering V_b can reduce the compression item when $V_b < 4V_a$. In the proposed buffer, the input 20 GHz tone is attenuated by a factor of $(1 + G_m Z_{load})$ (11 dB in this design) at v_{gs} of M_1. Therefore, $V_b = 0.67V_a$ in this case. The compression item is 19 dB lower in the proposed buffer than that in Fig. 5.7. Fig. 5.10 shows the simulated drain current at 60 GHz in different buffers. Compared to the conventional buffer and buffer with notch filter, the proposed solution delivers the highest drain current at 60 GHz. It is further compared against the case with 20 GHz tone removed from the input (dash line in Fig. 5.10). In the conventional and notch-filter buffers, the compression item reduces the drain current at 60 GHz by 2.6 and 2.8 dB, respectively. With the proposed technique, the reduction is limited to below 0.8 dB.

The reduction of the 20 GHz component in v_{gs} of M_1 also prevents the generation of other harmonic components (such as 40 and 80 GHz), which can result from the second-order nonlinear distortion of the 20 GHz tone or harmonic mixing effects between 20 and 60 GHz. The simulated drain currents at 40 GHz in different buffers are shown in Fig. 5.11. The proposed technique reduces the 40 GHz output current by 12–27 dB across the frequency range.

Besides the subharmonic soft-cancellation technique, the matching network of the buffer also provides extra filtering to the undesired 20 GHz tone.

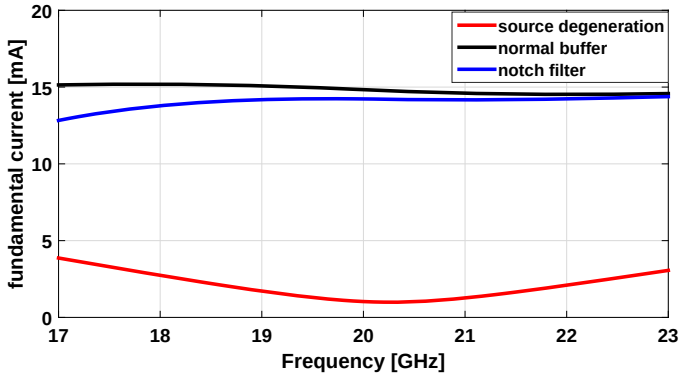


Figure 5.8: Simulated drain current at 20 GHz in different buffers.

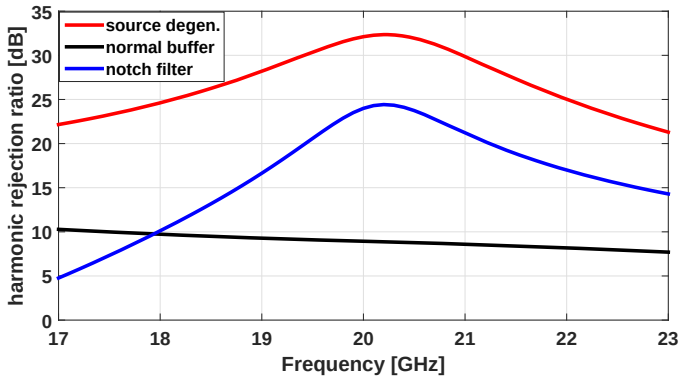


Figure 5.9: Simulated subharmonic rejection ratio at 20 GHz in different buffers.

The matching network can have two possible implementations: a single LC tank (as in Fig. 5.6(b)) and transformer based LC network (Fig. 5.12). The transformer solution prevails at mm-wave frequencies. Benefiting from the mutual inductance, it can achieve better Q-factor and less insertion loss. An extra design freedom is also available for circuit optimization: magnetic cou-

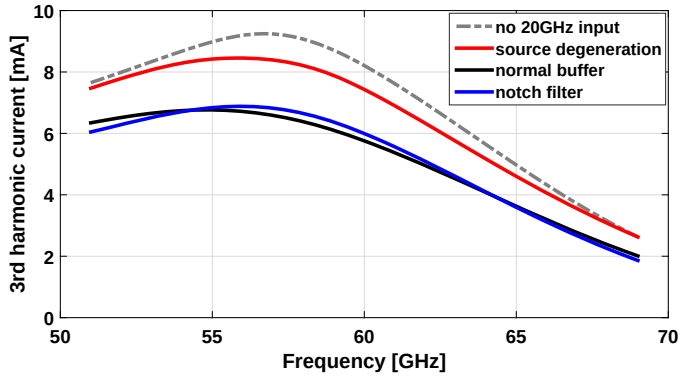


Figure 5.10: Simulated drain current at 60 GHz in different buffers.

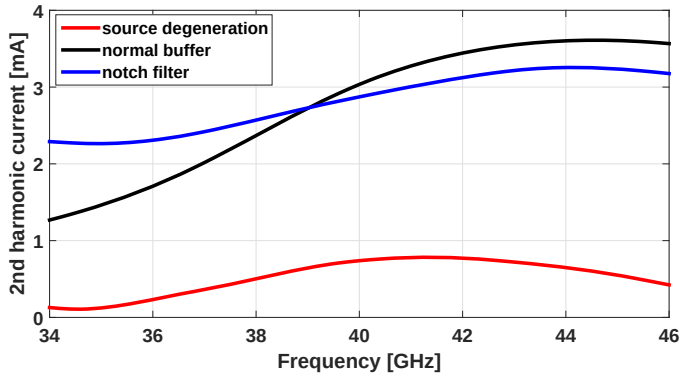


Figure 5.11: Simulated drain current at 40 GHz in different buffers.

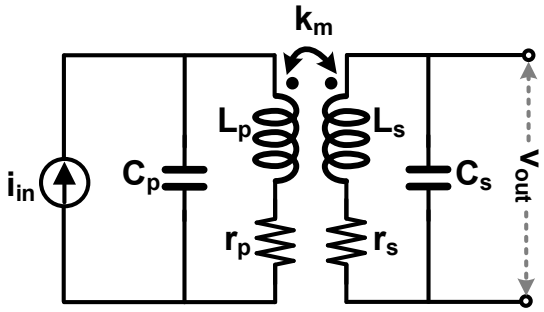


Figure 5.12: Transformer based matching network.

pling coefficient k_m. Recalling Eq. 3.3, the transimpedance of the transformer matching network can be expressed as

$$Z_{trans}(j\omega) \cong \frac{j\omega M}{(1 + j\omega\tau_L - \omega^2/\omega_L^2)\,(1 + j\omega\tau_H - \omega^2/\omega_H^2)}$$

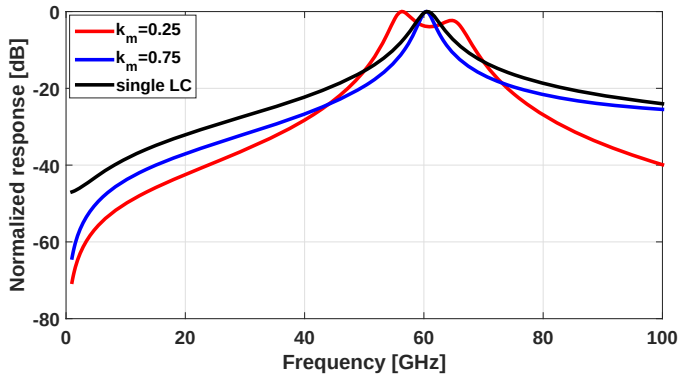


Figure 5.13: Normalized filter response of the single LC tank, low-k_m and high-k_m matching network.

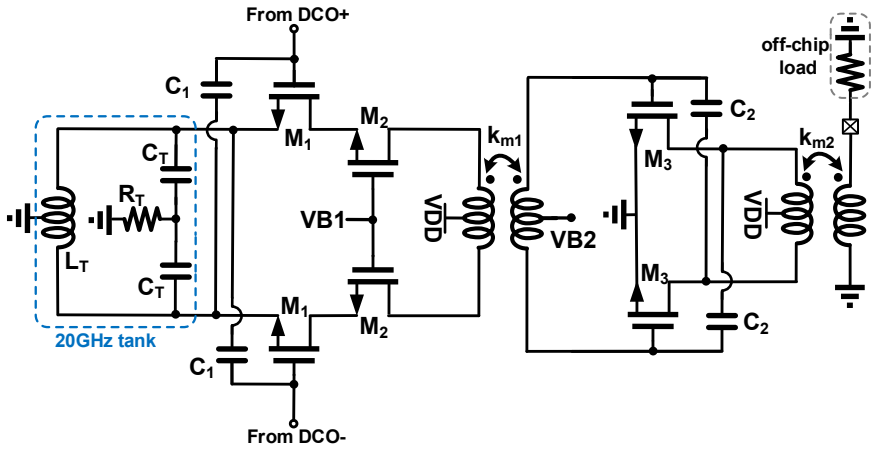


Figure 5.14: Schematic of the subharmonic soft-cancellation 60 GHz buffer with low-k_m transformer matching network and output driver.

where ω_L and ω_H are the frequencies of the two conjugate pole pairs. With a high k_m, the second conjugate pole pair occur at frequency that is much higher than operating frequency of the transformer matching network (i.e., $\omega_L << \omega_H$). A high-k_m transformer matching network can be approximated as a single LC tank with one conjugate pole pair at the frequency of interest. Due to the enhanced Q by the mutual inductance, it provides more filtering capability to out-of-band signal. With a low k_m transformer matching network, the two conjugate pole pairs can be designed to be close to each other (i.e., $\omega_L \cong \omega_H$) [57]. If the two pole pairs are infinitely close, the suppression to the out-of-band signal is twice that of the single LC tank. Fig. 5.13 shows the normalized filter response of the single LC tank, high-k_m ($k_m = 0.75$) and low-k_m ($k_m = 0.25$) transformer matching network (assuming the loading and Q factor of the self-inductance in each winding are the same as that in the single LC tank). These 3 matching network are all centered at 60 GHz. The low-k_m matching network exhibits 5 and 10 dB, respectively, more attenuation to 20 GHz signal than the high-k_m and single LC counterparts. Meanwhile, it also provides the widest bandwidth at 60 GHz.

In this design, a loosely coupled transformer ($k_{m1} = 0.25$) is used for the matching network of the 60 GHz buffer, as shown in Fig. 5.14. The simulated transfer function is shown in Fig. 5.15. With the subharmonic

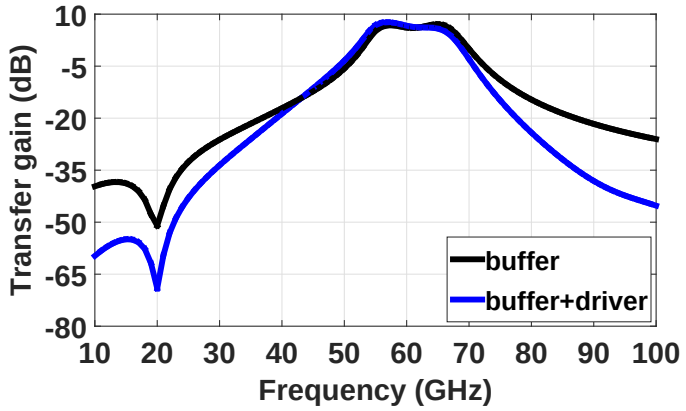


Figure 5.15: Simulated transfer gain of the 60 GHz buffer stage and combined buffer & driver stage.

soft-cancellation technique and low-k_m transformer matching network, this 60 GHz buffer provides a 50 dB suppression at 20 GHz. Across the frequency range, the buffer stage alone provides -43∼-51 dB suppression of the 20 GHz component and 6∼7 dB gain of the 60 GHz input, while achieving 13 GHz (22%) bandwidth. The buffer is followed by an output driver to deliver >0 dBm for measurements. Including the output driver, the two stages provide -70 dB suppression at 20 GHz, as also shown in Fig. 5.15.

5.5 Frequency Dividers

Though the implicit frequency tripling reduces the DCO oscillation frequency, it is still very high. It is challenging to feed the 20 GHz DCO output for phase/frequency detection directly. The counters and TDC running with the 20 GHz input require great design efforts, and it is extremely challenging to guarantee the robustness over PVT variations. Their power consumption will be significantly increased as well. In this ADPLL, the 20 GHz output of the DCO needs to be prescaled by frequency dividers before being fed back for the phase/frequency detection (PFD).

The division ratio in the frequency prescalers is set based on the trade-off between the operating frequency of the counters and dynamic range of the DTC-TDC in the PFD. On one hand, to ensure a robust operation over

PVT variations, there is an upper limitation on the input frequency of the counters and DTC-TDC. On the other hand, a small dynamic range is desired in the DTC-TDC to keep the nonlinearity and power consumption low. In this design, the division ratio is chosen as 8, and the output frequency of the divider chain is 2.5 GHz. At RF/mm-wave frequencies, there are several popular divider topologies: injection-locked frequency divider (ILFD), current-mode-logic (CML) divider and dynamic CMOS divider. The ILFD is based on a harmonic injection-locked oscillator. An LC-based ILFD is a popular choice at mm-wave frequencies. The locking range is inversely proportional to the Q-factor of the oscillator and typically very limited. To ensure robust operation over PVT variations, extra frequency calibration capabilities are necessary. The CML divider comprises CML latches. It does not require a rail-to-rail input level. The operating speed is limited by the RC time constant in the load of the latches. In this design, a divide-by-4 CML divider is employed as the first frequency prescaler stage with 20 GHz input from the DCO. A CMOS buffer stage converts the CML divider output to the rail-to-rail swing at 5 GHz. The dynamic CMOS divider follows the CML divider and scales the 5 GHz signal down to 2.5 GHz.

The schematic of the ÷4 CML frequency divider is shown in Fig. 5.16. It comprises 4 CML latches. In the typical-typical (tt) corner and room temperature, it consumes 5 mW from 1.05 V supply and operates with input frequency ranging between 5 and 34 GHz. Over different process corners (slow-slow, slow-fast, fast-fast, fast-slow and typical-typical) and temperates from -40 to 125 °C, the CML divider can always cover the frequency tuning range of the DCO. The schematic of the dynamic CMOS ÷2 divider is shown in Fig. 5.17. It consumes less than 1 mA with input frequency up to 10 GHz, while delivering rail-to-rail square-wave output. The interstage and output buffers consume 3 mA. As later discussed in Section 5.2, the noise floor of the divider chain is maintained to be lower than the FREF noise. It is simulated with an input swing that is equal to the DCO output. The noise floor at the 2.5 GHz output is shown in Fig. 5.18. Its contribution to the ADPLL output

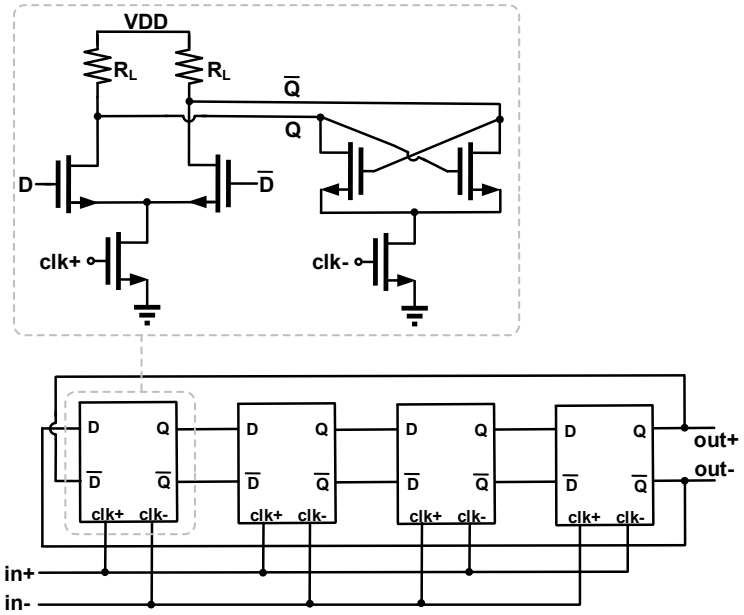


Figure 5.16: Schematic of the ÷4 CML frequency divider.

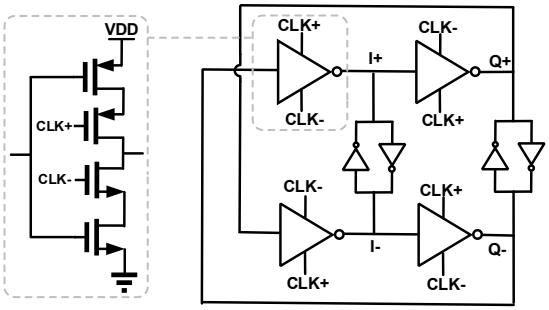


Figure 5.17: Schematic of the ÷2 CMOS frequency divider.

PN is at least 15 dB less than that from the FREF noise.

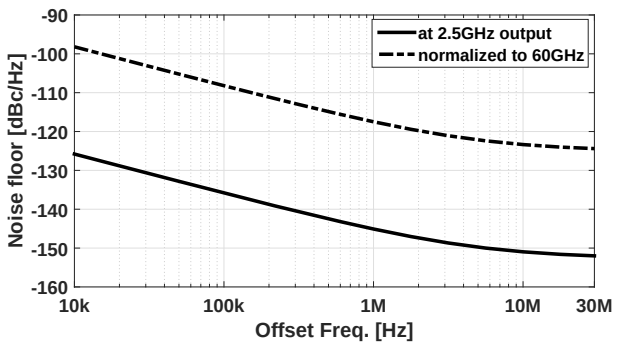
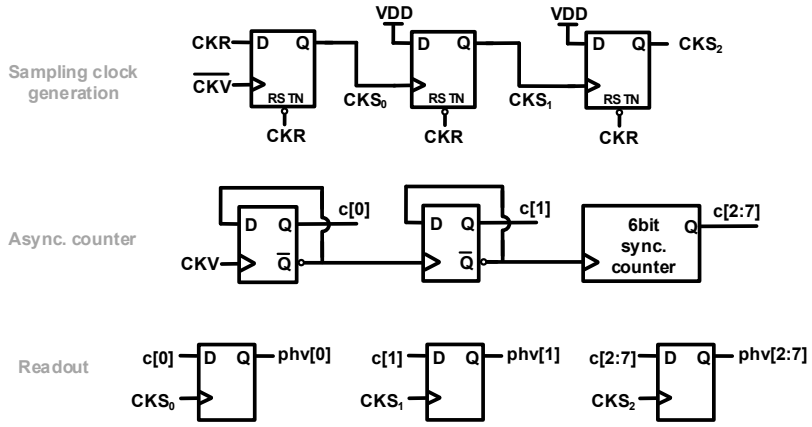
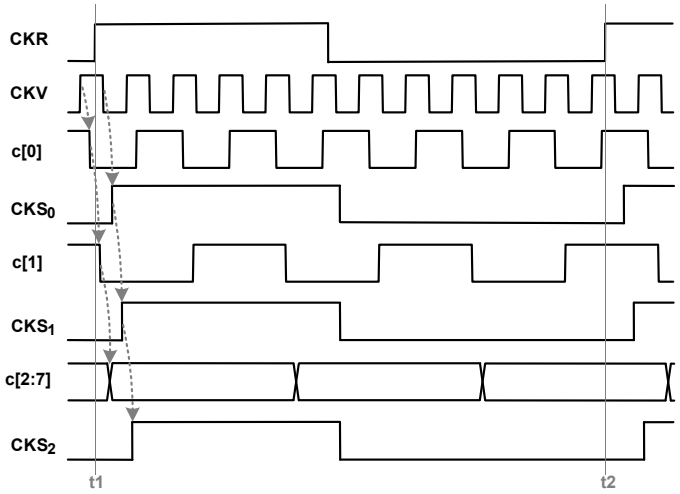


Figure 5.18: Simulated noise floor of the frequency divider chain.



(a)



(b)

Figure 5.19: (a) Block diagram, and (b) timing sequence of the asynchronous high-speed counter.

5.6 Phase Detection

In this design, an 8-bit variable-phase high-speed counter and a noise-shaping DTC-assisted TDC act as the phase detector. There are two design options for a high-speed counter: asynchronous and synchronous operation among different bits. As a trade-off between power consumption and design complexity, the 2 LSB integer bits are handled by an asynchronous counter to support the high speed at low power, The remaining 6 MSB bits are handled by a synchronous counter. Timing for reading out the combined counter output is critical due to its asynchronous and high-speed nature. Due to the

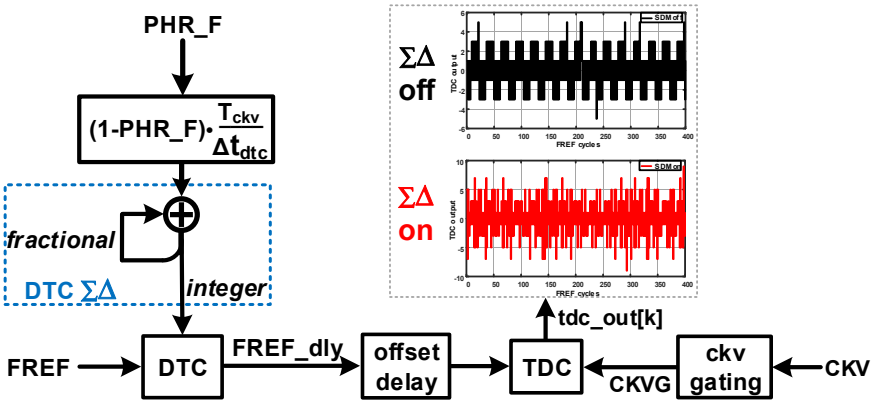


Figure 5.20: Block diagram of the DTC-TDC sub-system.

staggered settling of the counter's LSB bits, extreme care must be taken to guarantee proper sampling of PHV_I by the CKR clock edge, especially over PVT variations. Any misalignment between various bits or metastability will result in catastrophic phase jumps and thus failure in locking.

To ensure a robust operation, an asynchronous sampling scheme is used in the high-speed counter readout. Fig. 5.19 shows the circuit diagram and timing sequence. A specific case is also demonstrated in Fig. 5.19(b), in which the counter output bits c[1:7] are not yet settled at the CKR rising edge t_1. In the proposed solution, the CKV-to-Q delay for each asynchronous bit is added onto the respective sampling clock. The falling edge of CKV samples CKR and generates the sampling clock CKS_0 for bit c[0]. The delay between the rising edge of CKS_0 and c[0] is almost exactly half the CKV period, if the D flip-flops have the same delay. The rising edge of CKS_0 samples VDD and generates CKS_1, the sampling clock for bit c[1]. The sampling clocks for all the other asynchronous bits are generated in this manner. In this way, the delay in asynchronous bits also propagates in the respective sampling clocks. It ensures that each sampling clock always appears half CKV period after the counter bit is settled. The counter output can be robustly read out in each cycle with this asynchronous sampling technique.

The diagram of the DTC-TDC sub-system is shown in Fig. 5.20. A 64-stage DTC with 12 ps resolution is based on current-starved delay cells. Its schematic is shown in Fig. 5.21. The DTC helps to reduce the required

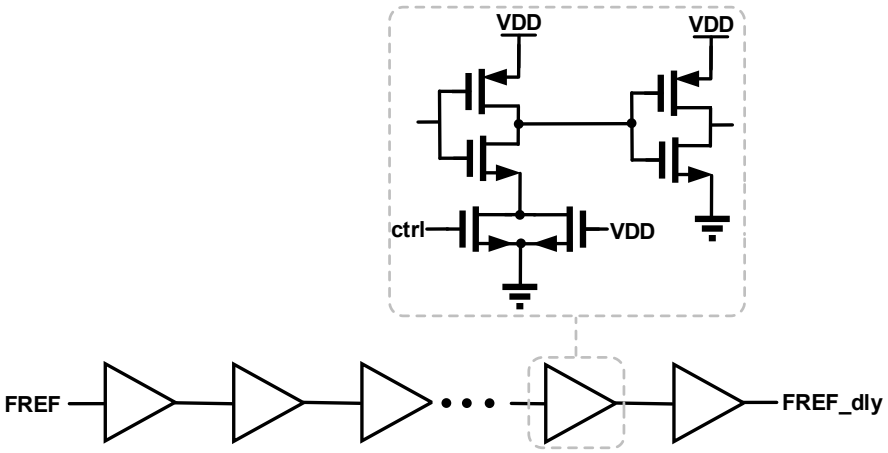


Figure 5.21: Schematic of the DTC.

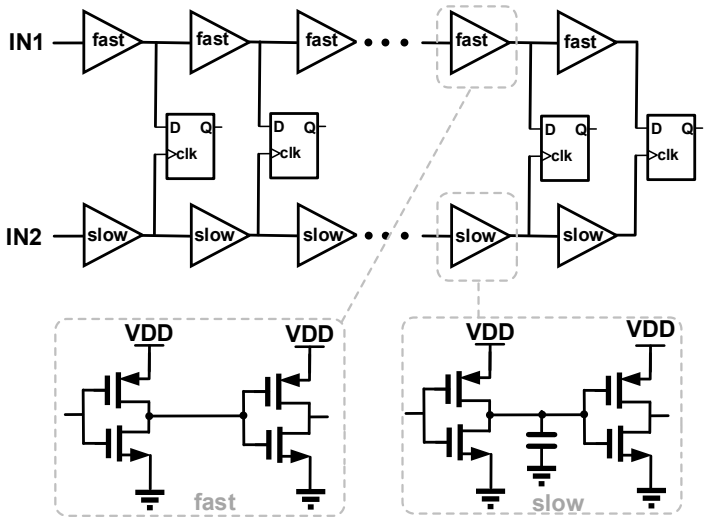


Figure 5.22: Schematic of the vernier TDC.

detection range of the TDC. A 64-stage 2.7 ps fine-resolution TDC uses a vernier line and ensures that its quantization (Q)-noise level is comparable to the FREF noise floor. Each TDC stage comprises a fast buffer, a slow buffer and a D-flip-flop, as shown in Fig. 5.22. To avoid a dead-zone issue in the TDC, the TDC output is encoded in mid-rise code. The transfer curve of the TDC is shown in Fig. 5.23. The TDC dynamic range covers about $0.4 \cdot T_{CKV}$. During the locking or settling process, the TDC input can exceed its TDC dynamic range. When overflow or underflow happens, the TDC output is overwritten by a maximum or minimum value (+64 or -64). In this way, the

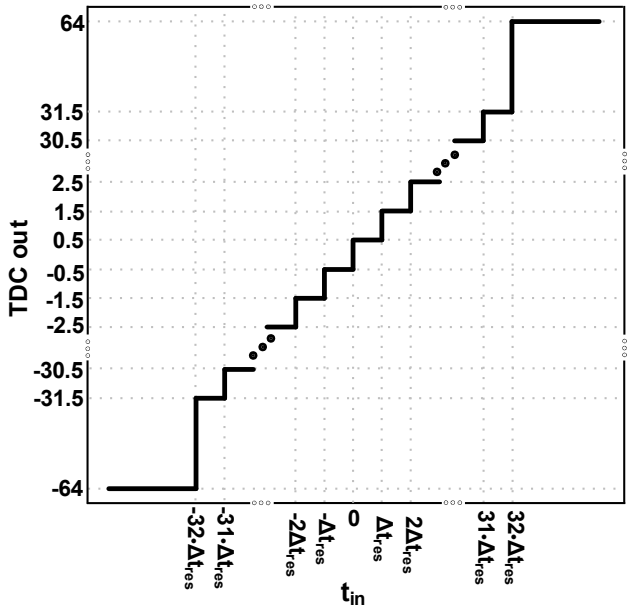


Figure 5.23: Transfer curve of the mid-rise TDC.

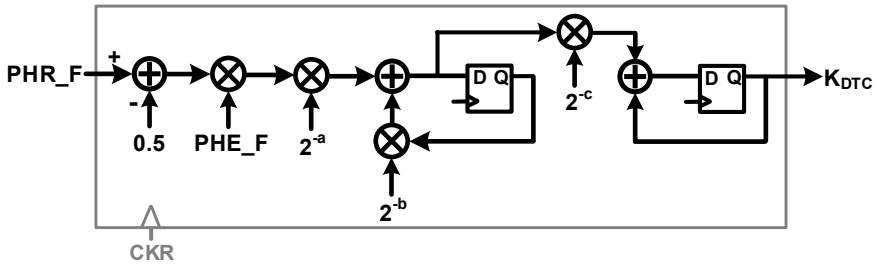


Figure 5.24: Diagram of the LMS algorithm for DTC gain calibration.

loop bandwidth is adaptively increased to facilitate the settling speed. After the PLL is locked, only 7-8 unit cells in the middle of the TDC chain are effectively operating.

The DTC gain inaccuracy can introduce spurious tones at the ADPLL output. An LMS algorithm [69] is employed and implemented on-chip to automatically calibrate the DTC gain (K_{DTC}) in the background. An inaccurate K_{DTC} causes extra phase error at the TDC output. The induced phase error is proportional to PHR_F[k]. The cross-correlation between PHE_F[k] and PHR_F[k] provides an indication of the inaccuracy in K_{DTC}. By iteratively updating the estimated K_{DTC}, an accurate DTC gain can be obtained when the cross-correlation between PHE_F[k] and PHR_F[k] is not detectable. Fig. 5.24 shows the block diagram of the DTC gain calibration algorithm. An

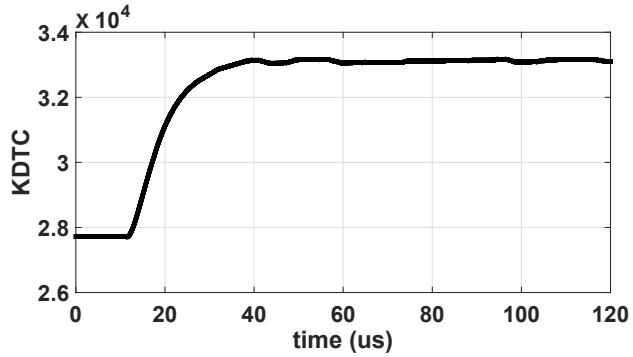


Figure 5.25: Simulated transient converging process of the DTC gain calibration algorithm with 20% initial error.

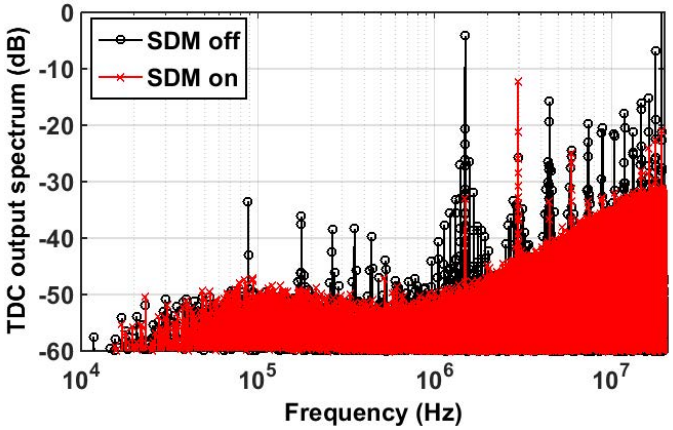


Figure 5.26: Simulated frequency spectrum of the TDC output with DTC ΣΔM on/off.

IIR filter attenuates the high-frequency components in the cross-correlation input. The IIR filter output then updates the K_{DTC} with proper gain. The transient settling behavior of the LMS algorithm is simulated and shown in Fig. 5.25. With 20% initial error in the DTC gain, the calibration converges in 25 us. The residual gain error is only 0.4%.

It is well known that the DTC/TDC Q-error and nonlinearity can introduce spurious tones. An error-feedback ΣΔ modulation (ΣΔM) is introduced to the DTC, as highlighted in Fig. 5.20. It eliminates the spur induced by the Q-error from the DTC-TDC and by the TDC nonlinearity. ΣΔM shapes the DTC Q-noise to high frequencies, which is then filtered by the LF. Moreover, the TDC input is scrambled by the preceding ΣΔM-DTC such that the TDC Q-error and nonlinearity will not induce spurious tones.

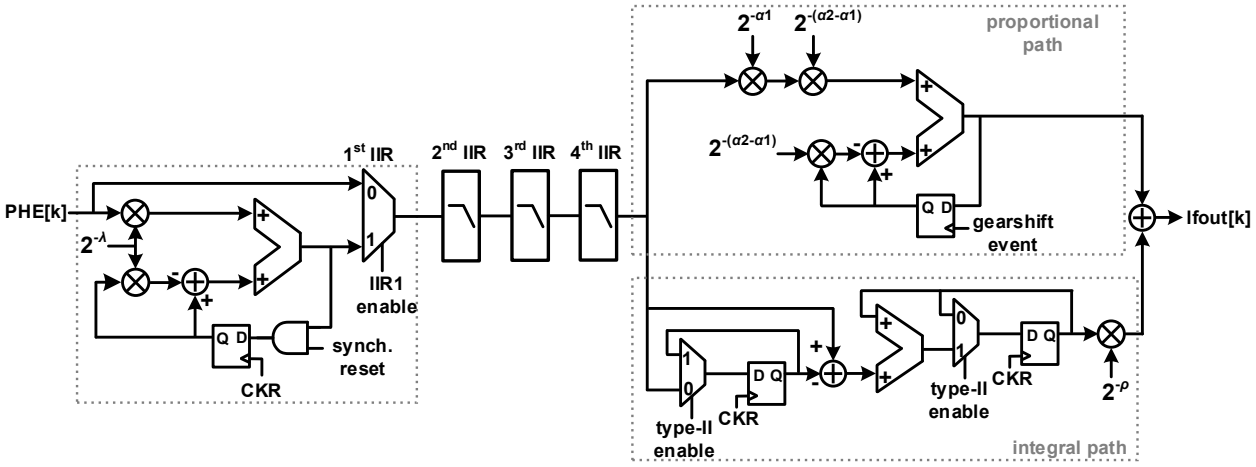


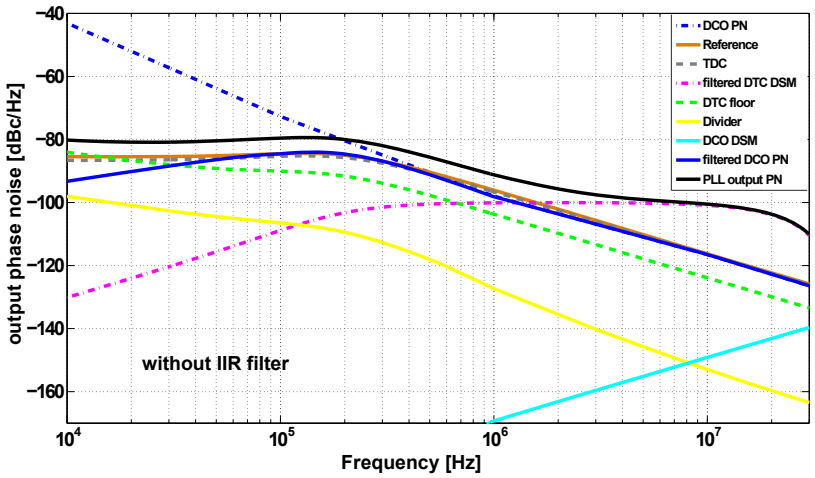
Figure 5.27: Block diagram of the digital loop filter.

With the DTC ΣΔM on/off, the respective TDC outputs are read out in the PLL close-loop simulations. Fig. 5.26 shows the corresponding frequency spectra. As we can see, the low frequency tones at the TDC output disappear or are suppressed below the system noise when the ΣΔM is on. The remaining spurs are caused by the nonlinearity in the DTC and limited cycle output of the ΣΔ modulator. They are attenuated by the following LF.

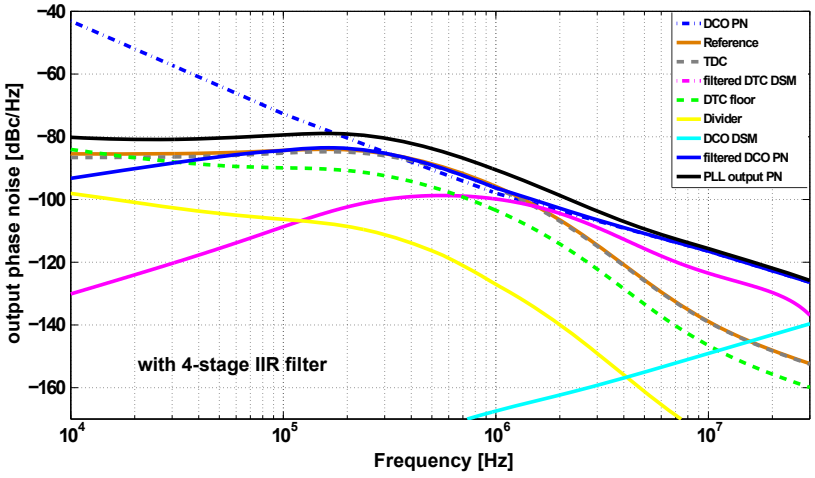
5.7 Digital Loop Filter

The digital loop filter (LF) determines the dynamic behavior and filtering capability to different noise sources in the ADPLL. In this work, the LF comprises a cascaded 4-stage IIR filter and a proportional-integral controller with gear-shifting mechanisms. All the parameters (λ_{1-4}, α and ρ) are programmable. The integral path and each IIR stage can be switched on/off. The block diagram of the LF is shown in Fig. 5.27. When all the IIR filter stages and the integral path are enabled, the ADPLL is type-II and $6th$-order. The gear-shifting mechanisms enable dynamic loop bandwidth in the locking process. Upon initiation, wide loop bandwidth is employed to acquire the desired frequency in short time. Once the loop is locked, it is switched to the optimal loop bandwidth for low IPN performance.

The IIR filter is intended to attenuate the quantization noise of the DTC



(a)



(b)

Figure 5.28: Simulated ADPLL PN with (a) IIR filter disabled, and (b) IIR filter enabled.

$\Sigma\Delta$M at high frequencies. It also helps to attenuate the spurs at high offset frequencies. The DTC $\Sigma\Delta$M quantization noise is shaped to high frequencies. The filtering capability provided by the PI controller may be not sufficient to attenuate the quantization noise below the other noise sources. Fig. 5.28(a) shows the simulated ADPLL PN without the IIR filter through s-domain modeling. All major noise sources are included in the simulation. As we can see, without the IIR filter, the DTC delta-sigma noise can significantly degrade the ADPLL PN at >2 MHz offset frequencies. In this work, the IIR filter bandwidth is configured to be 2–3 MHz, which is much higher than

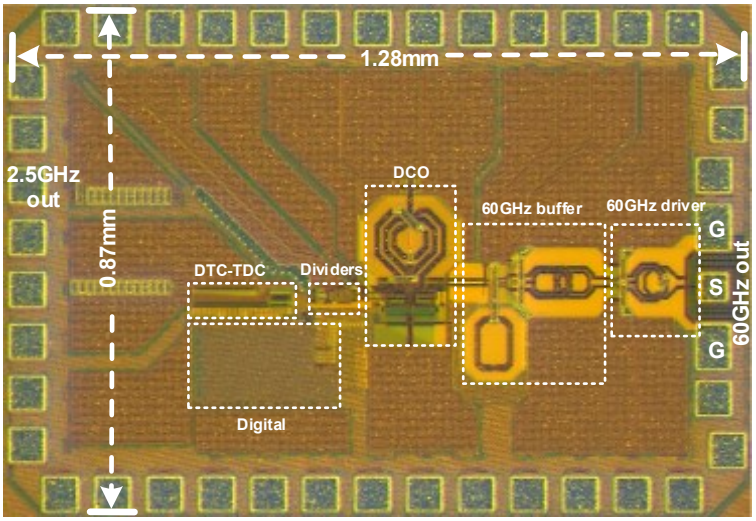


Figure 5.29: Chip micrograph of the proposed 60 GHz ADPLL.

the loop bandwidth (300 kHz). As shown in Fig. 5.28(b), with the IIR filter enabled, the DTC DSM noise is attenuated below the DCO PN. Owing to the IIR filter, the degradation on the IPN caused by the DTC DSM is limited to only 0.3 dB.

5.8 Experimental Results

The proposed 60 GHz digital fractional-N frequency synthesizer is prototyped in 28-nm 1P9M LP CMOS. Fig. 5.29 shows the chip micrograph. The design occupies a core area of 0.38 mm^2, while the total chip area (including pads) is 1.1 mm^2. The phase noise (PN) and spectra of the generated 60 GHz carrier are measured via on-wafer probing. Outputs of the 2.5 GHz frequency dividers could also be conveniently monitored.

5.8.1 Open-loop Test

The ADPLL is first set to an open-loop mode for the DCO performance characterization using a R&S FSUP50 Signal Source Analyzer. The tuning range (TR) of the DCO is 57.5–67.2 GHz, covering all four 802.11ad channels (58.32, 60.48, 62.64 and 64.8 GHz) with sufficient margin. The DCO draws

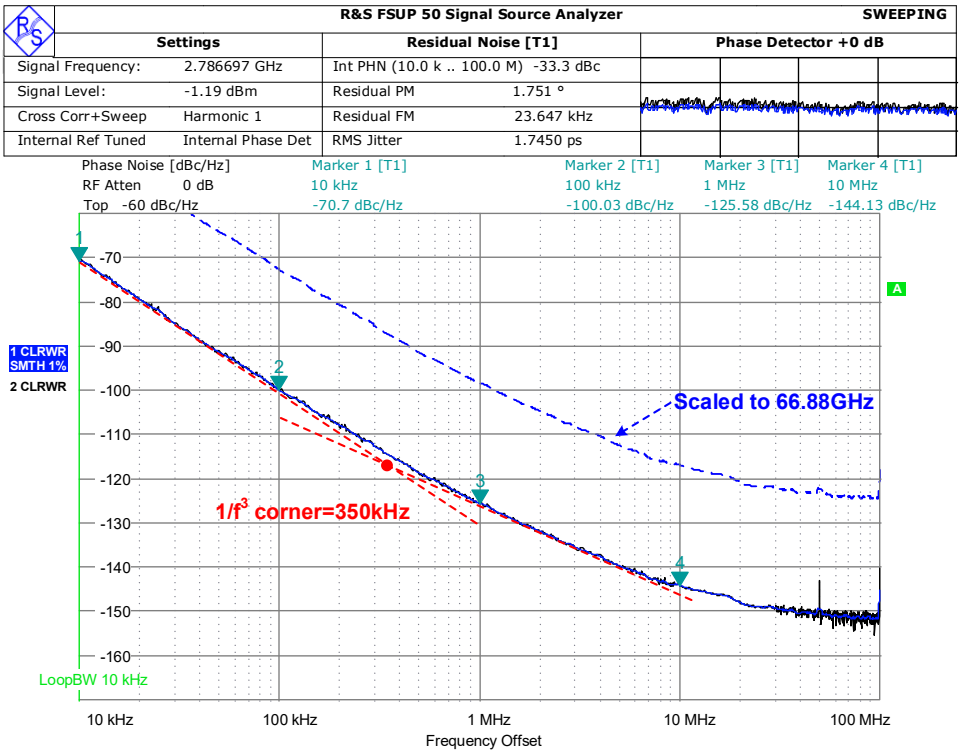


Figure 5.30: Measured DCO phase noise at dividers output and scaled up to 66.9 GHz.

19 mA from a 0.9 V supply. PN of the free-running DCO is measured after the frequency dividers (CKV point in Fig. 5.1), as shown in Fig. 5.30. The PN referred to the 66.88 GHz carrier is −98 dBc/Hz at 1 MHz offset. Across the TR, the $1/f^3$ noise corner varies between 300 and 400 kHz, as shown in Fig. 5.31. The slightly higher $1/f^3$ corner at lower oscillation frequencies is expected to

Table 5.1: Comparison of the DCO with relevant state-of-the-art

		Shi ASSCC15	Vigilante JSSC18	Zong JSSC16	Guo SSCL18	Cherniak ISSCC18	Szortyka JSSC16	This work
Osc. Freq. (GHz)		23.5-27.3 (15%)	16.1-19.8 (20.6%)	16.1-20.8 (25%)	25.3-29.5 (15.7%)	20.4-24.6 (18.7%)	53.8-63.3 (16%)	19.1-22.4 (15.6%)
$1/f^3$ Corner (kHz)		3000	2000	1000	550	NA	1000-4000	300-400
PN (dBc/Hz)	100kHz	-74.6	NA	-81.5	-80.5	NA	-63~-67	-82.1
	1MHz	-101.5	-108	-109.5	-108.7	-102	-91~-94.5	-107.5
P_{DC} (mW)		7.2	75-87.6	13.5	6.6	10	14	17
FoM (dBc/Hz)	100kHz	174	NA	175.9	181.4	NA	-167.6~-170	177.2
	1MHz	180	174	183.9	189.6	178.8	-175~-177.7	182.2
CMOS (nm)		28	28	40	65	65	40	28
No. of inductors		2 (tail filtering)	2	1	3	2 (tail filtering)	2 (tail filtering)	1
Type		VCO	VCO	VCO	VCO	VCO	VCO	DCO

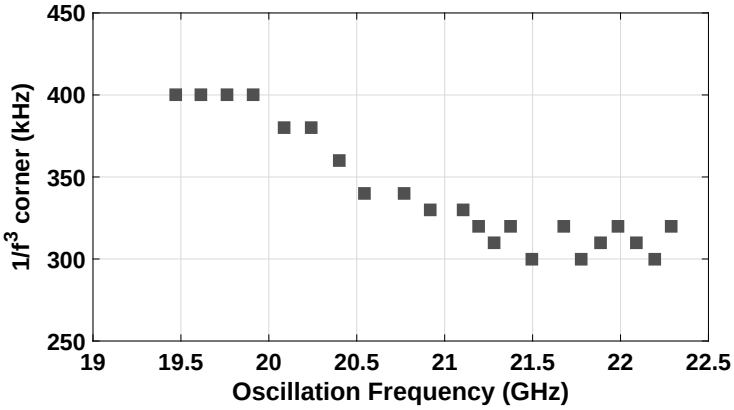


Figure 5.31: Measured DCO $1/f^3$ noise corner over TR.

be caused by the possible misalignment between the auxiliary resonances at H2/H3 and the fundamental frequencies. With a more accurate EM modeling, it can be further improved. The DCO performance is compared with the state-of-the-art oscillators at 20 and 60 GHz, as shown in Table 5.1 [19, 40, 68, 75–77]. The $1/f^3$ corner is the lowest. A better FoM is reported in [77], but at the cost of two extra inductors in the resonator.

5.8.2 Close-loop Test

The ADPLL is separately measured with different external crystal reference clocks of $f_R = 40$ and 100 MHz, at which it respectively consumes 28.6 and 31 mW (17 mW for DCO and 9.5 mW for frequency dividers). The 60 GHz buffer and 50 Ω-load driver stage consume 10.5 and 11.5 mW, respectively. All the circuit blocks (except for DCO) are supplied at 1.05 V (i.e., the nominal voltage for this technology). The ADPLL PN is measured with R&S FSUP50 with an extension V-band harmonic mixer for downconversion. The loop bandwidth is programmed to 200–300 kHz for the lowest RMS jitter. PN at an integer-N channel (65.28 GHz) and a fractional-N channel (65.411 GHz) is shown in Fig. 5.32. With 40 MHz FREF, the RMS jitter integrated from 10 kHz to 30 MHz is 237 fs at 65.28 GHz (integer-N), and 268 fs at 65.411 GHz (fractional-N). With the 100 MHz reference, the in-band PN and integrated jitter are substantially improved (see Fig. 5.33). Fig. 5.34(a)

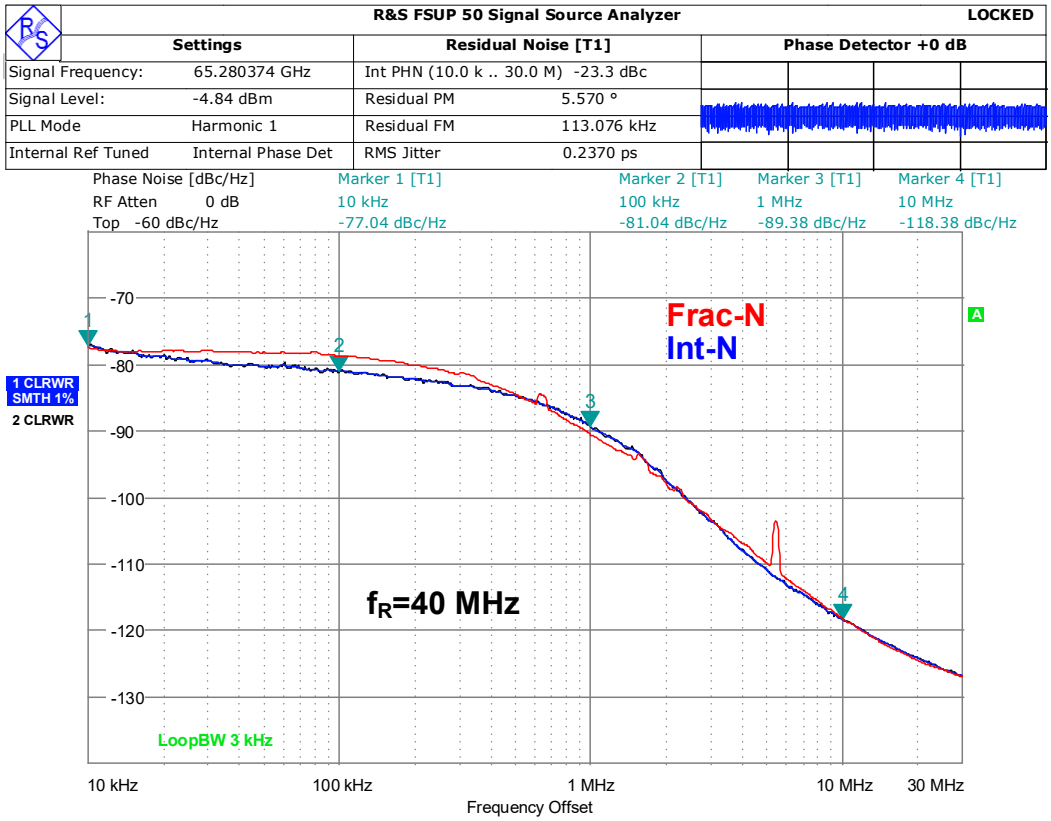


Figure 5.32: Measured ADPLL PN with f_R=40 at integer-N and fractional-N.

shows the spectrum at 65.411 GHz with DTC ΣΔM on (in red) and off (in blue). When the ΣΔM is engaged, the fractional spurs are significantly attenuated and the highest spur level observed at this carrier frequency is -51 dBc. The effect of DTC ΣΔM on the ADPLL PN is examined in Fig. 5.34(b). As we can see, the PN between 1-10 MHz has been slightly increased by <1.5 dB. The degradation on IPN is only 0.3 dB. It is even smaller with the 100 MHz FREF.

The measured RMS jitter across the fractional FCW offsets away from the 60 GHz integer-N channel and with the 40 and 100 MHz references are summarized in Fig. 5.35(a). With $f_R = 40$ MHz, the measured RMS jitter is 236∼266 fs and 236∼316 fs, respectively, across the integer-N (all swept) and fractional-N settings. With $f_R = 100$ MHz, the RMS jitter is improved to 213∼241 fs and 213∼277 fs across the respective channels. Fig. 5.35(a) reveals that the RMS jitter improves at some special fractional FCWs (such as 0.125, 0.25 and 0.5) with $f_R = 40$ MHz, while this reduction becomes smaller

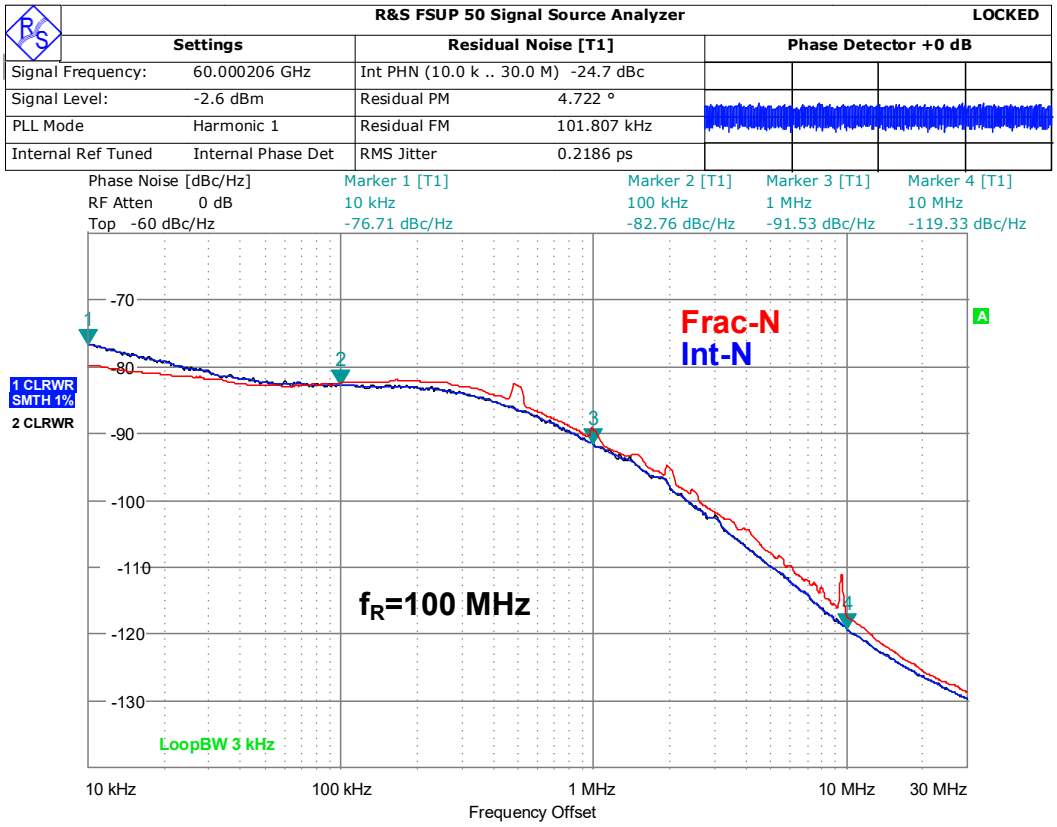
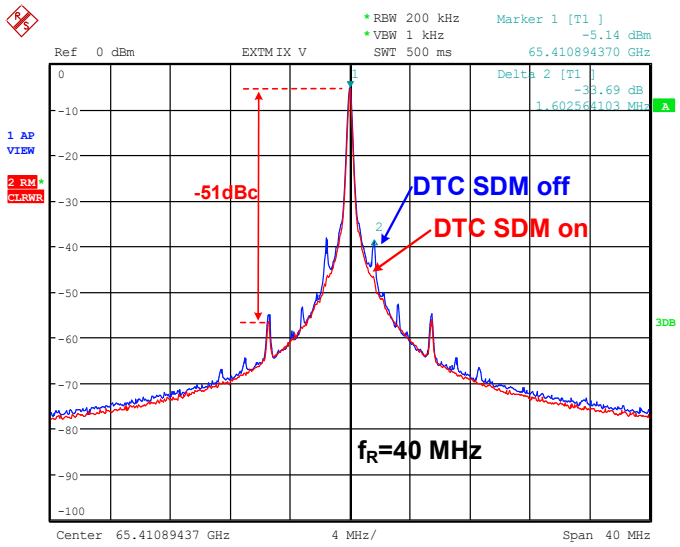


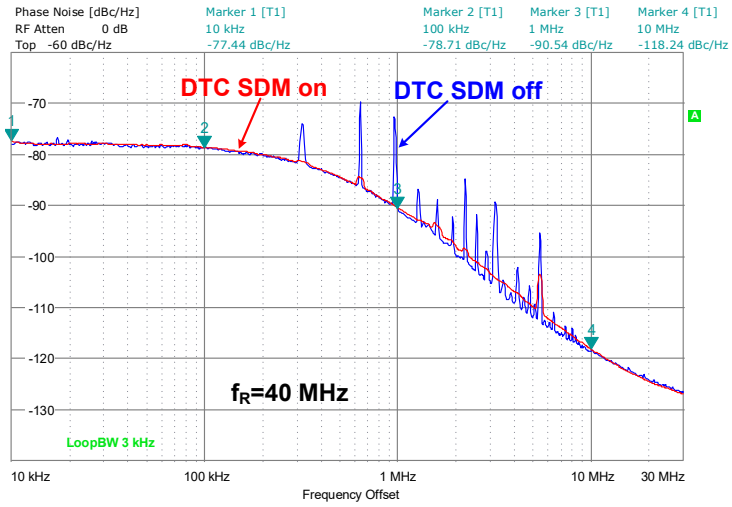
Figure 5.33: Measured ADPLL PN with f_R=100 MHz at integer-N and fractional-N.

with $f_R = 100\,\text{MHz}$. With these fractional FCWs, the TDC quantization error is not uniformly distributed, and its contribution to the ADPLL PN decreases. This causes the drop in RMS jitter in case of $f_R = 40\,\text{MHz}$. Since the uniformly distributed TDC quantization noise with $f_R = 100\,\text{MHz}$ is already a marginal contributor (4 dB below the FREF noise) to the ADPLL PN, the aforementioned effect exhibits less impact on the RMS jitter.

Fractional spurs are measured at the 2.5 GHz divider output with DTC $\Sigma\Delta$M enabled, and scaled to the corresponding 60 GHz frequencies. The fractional spurs across different fractional settings are summarized in Fig.5.35(b). At 2.5 GHz divider output, the fractional spurs are measured <-57 dBc. When referring to 60 GHz carrier frequencies, they are below -30 dBc. It should be noted that only a few papers report fractional spur levels at mm-wave frequencies. In [66], the spur levels appear to have been incorrectly taken from PN plots without accounting for the resolution bandwidth. In [68], with



(a)

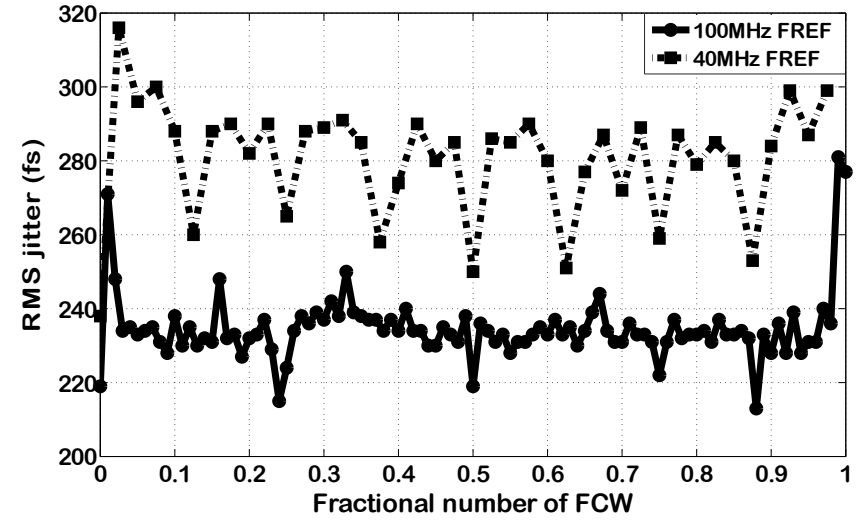


(b)

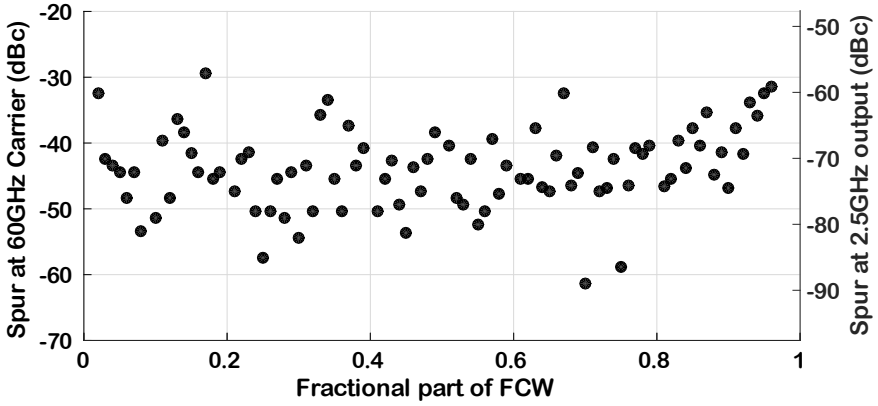
Figure 5.34: Measured ADPLL output (a) spectrum and (b) PN with DTC ΣΔM on/off.

sophisticated DTC nonlinearity calibration, a lower fractional spur of -38 dBc (normalized to 60 GHz) was achieved. There is no DTC/TDC nonlinearity calibration done in our design, but it can be applied if the spurs need further suppression in some applications. Random dithering in ΣΔM [78] can also reduce part of the spurs.

Measurements have been done to verify the transient settling performance of this ADPLL. After the PLL is locked with 40 MHz FREF, a step ΔFCW is added to the original FCW. The step response of the ADPLL is monitored



(a)



(b)

Figure 5.35: Measured ADPLL: (a) RMS jitter, and (b) worst-case fractional spurs, across fractional offsets from 60.0 GHz integer-N.

at the 2.5 GHz divider output. As shown in Fig. 5.36, with a 100 MHz step at 60 GHz, the ADPLL settles within 5 us. With smaller frequency step or higher FREF frequency, the settling is even faster.

The output power level at the 60 GHz carrier and the leaked 20 GHz tone are measured to validate the effectiveness of the 20 GHz tone suppression technique. After de-embedding cable losses, the driver delivers 1 dBm at 60 GHz to the external 50-Ω load, with ±1 dB variation across the TR (see Fig. 5.37). The 20 GHz residual level is within -51∼-57 dBm across the TR. The achieved harmonic rejection ratio is 20 dB better compared to the notch

Table 5.2: Comparison of the 60 GHz fractional-N ADPLL with relevant state-of-the-art

		ISSCC'09 Scheir	JSSC'11 Musa	JSSC'16 Siriburanon	ISSCC'13 Yi	JSSC'14 Wu	JSSC'15 Szortyka	ISSCC'18 Huang	JSSC'17 Hussein	**This Work**	
Architecture		Analog PLL	20G PLL + 60G QILO	20G SSPLL + 60G QILO	Analog PLL	ADPLL	SSPLL	ADPLL	ADPLL	**ADPLL**	
Type		INT-N	INT-N	INT-N	INT-N	FRAC-N	INT-N	INT-N	FRAC-N	**FRAC-N**	
Output frequency (GHz)		57-66 (14.6%)	58-63 (8.3%)	58.3-64.8 (10.5%)	58-68.5 (8.3%)	56.5-63.5 (11.6%)	53.8-63.3 (16.2%)	82-107.6 (27%)	50.2-66.5 (28%)	57.5-67.2 (15.6%)	
Ref. frequency (MHz)		100	36	40	135	100	40	125	100	40	100
PN (dBc/Hz)	In-band	-70	-60	-75	NA	-75	-88~ -92	-84~ -87	-79~ -83	-77~ -81	-81~ -84
	1MHz	-75	-95	-92	-89.8~ -91.5	-90	-88~ -92	-81	-88~ -94.5	-89~ -92	
RMS jitter (fs)	Integer channel	NA	NA	290	238	590.2	200	276~328	223~302.5	**236~266**	**213~241**
	Fractional channel								962~1540	**236~316**	**213~277**
V_{DD} (V)		1.1	1.2	1	1.2	1.2	1	1.2/0.8	1	1.05	
P_{DC} (mW)		78	80	32	24.6	48	42	35.5	46	**28.6 + 10.5 ***	**31 + 10.5 ***
FoM # (dB)	Integer channel	NA	NA	-235.7	-238.5	-227.8	-237.7	-234~ -235.7	-233.8~ -236.4	-235.6~ -236.6 *	-236.2~ -237.2 *
	Fractional channel								-219.6~ -223.7	**-234~ -236.6 ***	**-235~ -237.2 ***
Reference spur (dBc)		-42	<-47	-38	-54.5	-74	<-40	-34~ -52	NA	-62	-65
Area (mm^2)		0.82	1.68	1.09	0.19 **	0.48 **	0.16 **	0.36 **	0.45 **	1.1 (core area is 0.38)	
CMOS technology (nm)		65	65	65	65	65	40	65	65	28	

*: include the power consumption of the 60GHz output buffer stage (10.5mW)
**: only include the core chip area
#: $\text{FoM} = 10 \cdot \log_{10}\left[\left(\frac{\text{Jitter}_{\text{rms}}}{1\text{s}}\right)^2 \cdot \frac{P_{DC}}{1\text{mW}}\right]$

filter solution in [73]. The 40 GHz tone, which is caused by the nonlinear effects in the buffer stage, is measured at -44∼-64 dBm across the TR.

Table 5.2 summarizes the performance of the proposed 60 GHz ADPLL and compares it with relevant state-of-the-art PLLs at 60 GHz or above [17–19, 21, 65–67, 79]. Only two fractional-N PLLs at 60 GHz or above are found in literature. The integrated jitter of our ADPLL is the best compared to the other fractional-N counterparts, while consuming the lowest power. The figure-of-merit (FoM) improves state-of-the-art by 3 dB at the fractional-N operation, even with including the power consumption of the 60 GHz buffer stage.

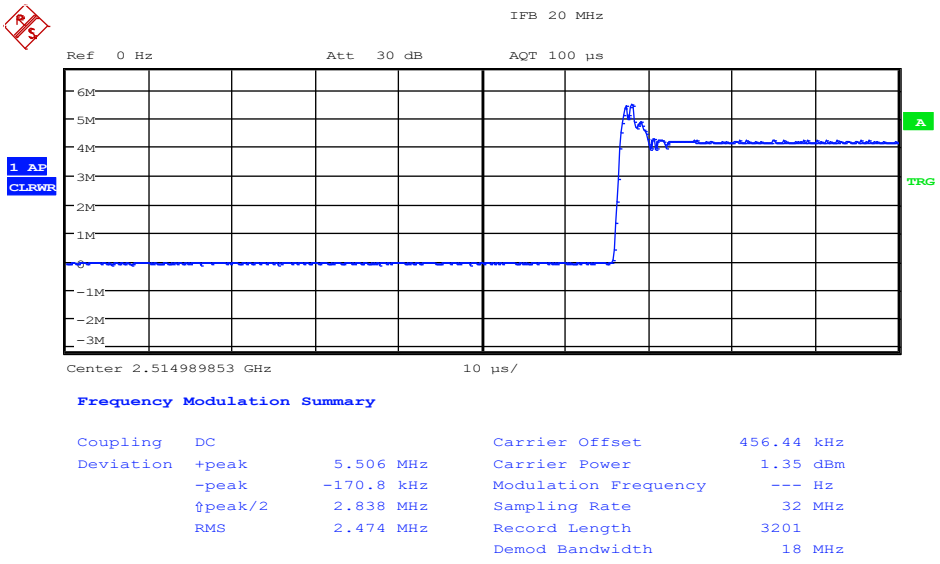


Figure 5.36: Measured ADPLL settling behavior with 100 MHz frequency step at 60 GHz.

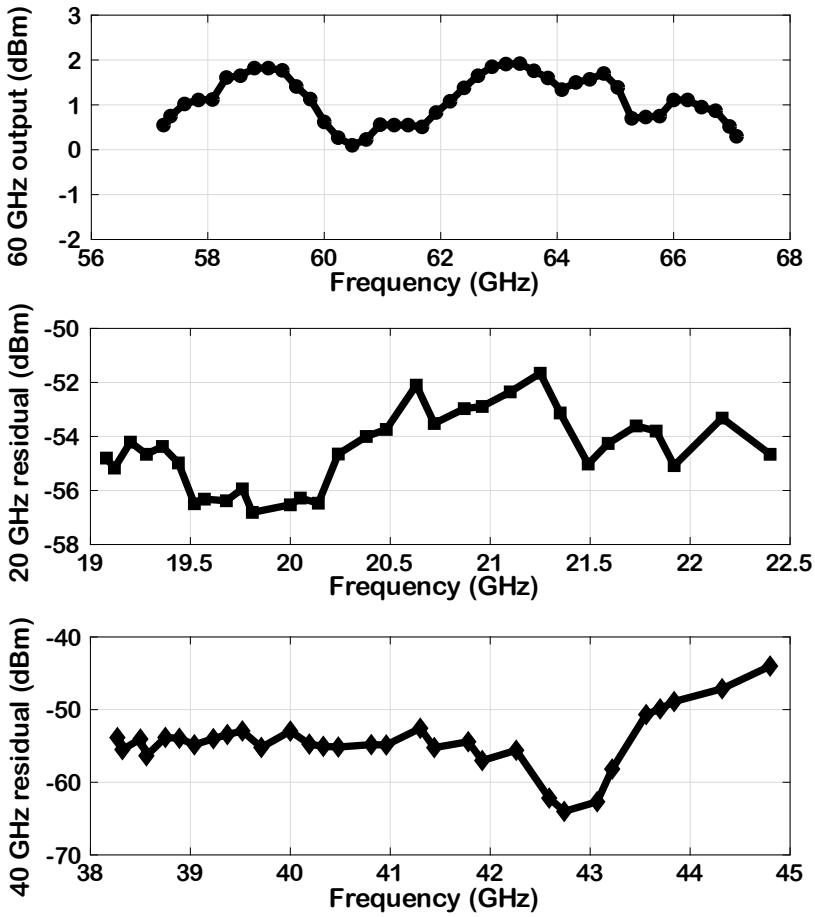


Figure 5.37: Measured power across the tuning range of 60 GHz carrier and 20 GHz residual.

Chapter

6

Conclusions and Recommendations

This dissertation has mainly focused on the design of a power-efficient mm-wave frequency synthesizer with low phase noise in nanometer CMOS technologies. This chapter concludes the thesis with a summary of the original contributions in Section 6.1 and the PhD work outcomes in Section 6.2. Finally, recommendations for the future work will be given in Section 6.3.

6.1 Original Contributions

The original scientific contributions made in this thesis are summarized as follows:

• Introducing a new frequency synthesizer architecture that can improve phase noise and power efficiency for millimeter-wave applications; (Chapters 3 and 5)

• Comprehensive analysis of the phase noise and operating principles of the proposed harmonic boosting oscillator; (Chapter 3)

• Discovering the mechanisms of flicker noise upconverting to phase noise in the oscillators and suggesting possible solutions to them; (Chapter 4)

• Proposing and verifying a generic technique to suppress the flicker noise upconverting to phase noise; (Chapter 4)

• Proposing and implementing a subharmonic rejection technique for (implicit) frequency multipliers that improve the harmonic rejection ratio; (Chapter 5)

• Proposing and applying a method of the sigma-delta modulation to the DTC in the ADPLL for lowering the fractional spurs; (Chapter 5)

• Design and implementation of a low-noise fractional-N ADPLL for high-performance millimeter-wave applications in nanometer CMOS. (Chapter 5)

6.2 Thesis Outcomes

Emerging electronic applications pose ever-increasing demands on bandwidth, SNR and power efficiency of the wireless transceivers. With the advancement of CMOS technology, electromagnetic spectra in the millimeter-wave frequencies have played an important role to enable these applications due to the affordability of wide bandwidths. As key subsystems in the mm-wave transceivers, frequency synthesizers incur significant contributions to the achievable SNR via the phase noise and spurious degradation. The fre-

quency synthesizers also consume significant amount of power. Physical and circuitry-level constraints from the high operating frequencies and CMOS technology scaling have posed great challenges in the design of mm-wave oscillators, frequency dividers and other analog circuits, as described in Chapter 1. Innovations are required to improve their performance and power efficiency.

The currently existing mm-wave frequency synthesizer architectures have evolved towards a direction where low frequency oscillators are employed with a frequency multiplication afterwards in order to maximally improve the phase noise, as summarized in Chapter 2. However, none of these architectures have managed to improve the phase noise performance and power efficiency simultaneously. This has motivated our research towards a new architecture.

The mm-wave frequency generation scheme in Chapter 3 enhances the power efficiency by reusing the readily existing third-harmonic current at 60 GHz inside the 20 GHz oscillator for frequency tripling. MM-wave frequency multipliers or dividers are not physically needed anymore in the proposed frequency synthesizer architecture. To deliver sufficiently strong 60 GHz signal, the third harmonic component inside the 20 GHz oscillator is boosted with a transformer-based resonator at an optimized k_m=0.6. The phase noise is improved owing to the improved Q-factor of the LC tank and low ISF enforced by the boosted third harmonic. The 60 GHz frequency generator prototyped in 40 nm CMOS technology demonstrates -98.8∼-100.1 dBc/Hz phase noise at 1 MHz offset from 60 GHz carrier and a tuning range of 25%. The figure-of-merit (FoM) has advanced the state-of-the-art by 3 dB.

The $1/f^3$ noise in conventional oscillators dominates the in-band phase noise of mm-wave PLLs and has significant contribution to the integrated phase noise (IPN). In order to reduce the $1/f^3$ noise, flicker noise upconversion mechanisms need to be thoroughly comprehended. As explained in Chapter 4, the mechanisms can be classified into two categories: direct and indirect upconversion. The baseband flicker noise is directly upconverted to the oscillation frequency via the nonlinearity of the cross-coupled pair. The upconverted flicker noise at higher-order harmonic frequencies can also be

indirectly converted down to the oscillation frequency by self-mixing with the periodically varying $g_{ds}(t)$ of the cross-coupled pair. Any out-of-phase harmonic voltage swing in v_{ds} and v_{gs} of the cross-coupled pair induces flicker noise upconversion to phase noise, and should be eliminated for low $1/f^3$ noise. The technique proposed in Chapter 4 suppresses the flicker noise upconversion through both the direct and indirect mechanisms. The prototyped 20 GHz DCO in 28 nm CMOS measures a $1/f^3$ corner of 300–400 kHz, which is the lowest ever reported at this frequency. The phase noise is -82.1 and -107.5 dBc/Hz, respectively, at 100 kHz and 1 MHz offset from 20 GHz carrier.

The source soft-degenerated buffer achieves a better suppression to the subharmonic input than the conventional notch filter solutions, as explained in Chapter 5. It is proposed to suppress the 20 GHz tone in the 60 GHz ADPLL with the implicit frequency tripling. The undesired subharmonic input has a very low transconductance gain due to the source degeneration by an LC tank. The gain of the buffer is seldomly affected for the signal of interest, while the gain in conventional notch filter solution is decreased by the large subharmonic blocker. The prototype suppresses the 20 GHz tone to the level of -51∼-57 dBm across a 15% frequency tuning range. The harmonic rejection ratio is 20 dB better than with the notch filter solutions.

The error-feedback sigma-delta modulation in the DTC can reduce the fractional spurs in the ADPLL. It shapes the DTC quantization noise to high frequencies and scrambles the TDC input. The spurs induced by DTC quantization error and by TDC nonlinearity are eliminated. The high-frequency DTC quantization noise is attenuated by the IIR filter in the loop.

The 60 GHz fractional-N ADPLL exploits the implicit frequency tripling, flicker noise upconversion suppression technique and sigma-delta modulated DTC-TDC. The test chip is demonstrated in 28 nm CMOS and consumes 40 mW from 1.05 V supply. It exhibits 213–277 fs and 236–316 fs RMS jitter, respectively, with 100 and 40 MHz reference clock. The fractional spurs are below -30 dBc. It achieves the highest power efficiency among the 60 GHz fractional-N PLLs, and advances the state-of-the-art figure-of-merit (FoM) by

1.5 dB.

6.3 Recommendations for future work

The resolution of the digital-to-time converter (DTC) is very sensitive to process, voltage and temperature (PVT) variations. Inaccuracy in DTC gain calibration, as well as the DTC nonlinearity, can result in large fractional spurs. Digital-to-phase converters (DPCs) can avoid the gain calibration procedure. However, the DPCs are typically realized through phase interpolation, which is inferior in linearity. It would be inspiring to carry out research towards a linear digital-to-phase converter (DPC) in true-phase domain. It can relieve the complexity in calibration, reduce the spur level and smooth the locking process.

Fine tuning capacitor bank in the DCO needs to achieve good resolution and ensure enough frequency coverage. It is comprised of many switched-capacitor units and quite bulky in layout. The long interconnects and parasitics associated with it degrade the Q-factor of the LC tank and frequency tuning range. Some other compact ways of realizing linear fine frequency tuning is clearly in high demand, especially at mm-wave frequencies.

From the derivations in Chapter 4, the $1/f^3$ noise can be further improved by reducing the nonlinearities of the g_m devices. Lowering the oscillation swing in conventional oscillators can render in more linear g_m devices but worse phase noise. This finding can inspire further research work towards new types of oscillators which can improve the linearity of the g_m devices while sustaining large oscillation swing.

In Chapter 3, the adjustment of magnetic coupling coefficient (k_m) is done by varying the space between primary and secondary windings. Large space between windings can degrade the Q-factor of the transformer. A four-port inductor can achieve similar effects as a transformer but gives more freedom in optimizing the k_m. It is certainly worthy to investigate alternative solutions with the four-port inductor.

With the given fine resolution, it is challenging to achieve large dynamic range while still maintaining good integral nonlinearity (INL) in a DTC. In this work, the DTC-TDC subsystem needs to cover a dynamic range of more than 400 ps. However, the time difference between the FREF rising edge and the nearest zero-crossing of the 20 GHz DCO output is no more than 50 ps. This time difference extend is the only signal of interest after the ADPLL is locked. It can significantly reduce the required dynamic range of the DTC-TDC subsystem. More work can be done to figure out solutions to pick up the corresponding zero-crossing for phase detection.

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List of Publications

Journal Papers

- **Z. Zong**, P. Chen and R. B. Staszewski, "A Low-Noise Fractional-N Digital Frequency Synthesizer With Implicit Frequency Tripling for mm-Wave Applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 755–767, Mar. 2019.

- **Z. Zong**, M. Babaie and R. B. Staszewski, "A 60 GHz frequency generator based on a 20 GHz oscillator and an implicit multiplier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1261–1273, May 2016.

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- **Z. Zong**, M. Babaie and R. B. Staszewski, "A 60 GHz 25% tuning range frequency generator with implicit divider based on third harmonic extraction with 182 dBc/Hz FoM," *IEEE RFIC Symp.*, May 2015, pp. 279–282.

- **Z. Zong** and R. B. Staszewski, "Effects of Subharmonics in LO Generation on RF Transceivers," *IEEE MTT-S International Microwave Workshop Series on 5G Hardware and System Technologies (IMWS-5G)*, Aug. 2018, pp. 1–3.

- F.-W. Kuo, **Z. Zong**, H.-N. Ron Chen, L.-C. Cho, C.-P. Jou M. Chen and R. B. Staszewski, "A 77/79-GHz Frequency Generator in 16-nm CMOS for FMCW Radar Applications Based on a 26-GHz Oscillator with Co-Generated Third Harmonic," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2019 (accepted).

- P. Chen, F. Zhang, **Z. Zong**, H. Zheng, T. Siriburanon, R. B. Staszewski, "A 15-uW, 103-fs step, 5-bit capacitor-DAC-based constant-slope digital-to-time converter in 28nm CMOS," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2017, pp. 93–96.

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Book Chapter

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Summary

This thesis focuses on improving the phase noise and power efficiency of millimeter-wave (mm-wave) frequency synthesizers in nanometer CMOS. The mm-wave frequency spectrum is widely adopted in various upcoming volume commercial wireless applications. These new applications provide more interconnection between the physical and digital worlds. It entails a demand for high speed data communications and accurate object sensing, which are enabled by the large bandwidth available at mm-wave frequencies. These systems also require good signal-to-noise ratio (SNR) on mm-wave transceivers. It sets stringent phase noise specifications on the mm-wave frequency synthesizers. On the other hand, the power budget on the mm-wave frequency synthesizers are limited for long battery lifetime and/or thermal reliability. The low phase noise should be achieved at high power efficiency.

Advanced nanometer CMOS technologies are preferred for the integration of mm-wave frequency synthesizers. The scaled transistor size favors the co-integration with baseband circuits and large-scale SoCs. The upgrowing speed of the MOSFETs also extends the upper limits on the operating frequency of the CMOS circuits. On the other hand, the performance of mm-wave frequency synthesizers suffers from various constraints and imperfections in nanometer CMOS technologies. For example, the mm-wave oscillators is inferior in phase noise due to the low quality-factor LC tank and exacerbated flicker noise upconversion. Mm-wave frequency dividers/multipliers are power hungry and limit the power efficiency of the frequency synthesizers. There is

a clear gap in performance between mm-wave and RF frequency synthesizers.

This thesis takes several measures to reduce that gap. A new mm-wave frequency synthesizer architecture is proposed. The main idea is that the oscillator works at one third of the mm-wave frequency. The third harmonic in the oscillator is boosted before directly delivering to output, while the main oscillation signal at one third of the mm-wave frequency is fed back for phase detection. The phase noise is significantly improved due to the higher-Q LC tank at lower frequency. Meanwhile, the readily available third harmonic current in the oscillator is reused for frequency tripling in the proposed architecture. It reduces the power consumption by physically exempting a mm-wave frequency tripler/divider. A transformer-based dual resonance LC tank is exploited in the oscillator to accomplish this goal. The two resonances are designed at the desired mm-wave frequency and one third of it. By optimizing the magnetic coupling coefficient of the transformer, the third harmonic swing in the oscillator is boosted. It is then extracted to the output by a mm-wave buffer. A subharmonic soft-cancellation technique is proposed to suppress the undesired tone at one third of the mm-wave output frequency. With source degeneration by an parallel LC tank resonating at the one third subharmonic frequency, the input transistors sense only the desired mm-wave component with no response to the subharmonic. This technique also improves the gain at the mm-wave signal band.

Flicker noise upconversion to phase noise is a key performance-limiting factor in nanometer CMOS RF/mm-wave oscillators. It has significant contribution to the integrated phase noise in high-performance PLLs. The flicker noise upconversion mechanisms are comprehensively investigated at the circuit level in this thesis. Out-of-phase high-order harmonics in the oscillator facilitate the conversion process of flicker noise to phase noise through different types of mixing. Various possible solutions to suppressing the conversion are summarized. They allow the designers to make the best choice for their specific applications. These insights also lead to a generic flicker noise upconversion suppression technique that is widely applicable to different oscillator topology.

This technique is applied to a 20 GHz DCO and achieves the lowest reported $1/f^3$ noise corner.

The architectural and circuit-level proposals are integrated in a 60 GHz digital-intensive fractional-N frequency synthesizer, which is embraced by the CMOS technology scaling. The significant improvement of the DCO phase noise gives more freedom to the design of other loop components. Low integrated phase noise can be achieved without necessity on ultra fine-resolution TDCs and excessively large loop bandwidth. A pair of digital-to-time converter (DTC) and time-to-digital converter (TDC) with medium-level resolution, in combination with a relatively narrow loop bandwidth, is employed in this thesis work for low spurs while still achieving low integrated PN. Error-feedback sigma-delta ($\Sigma\Delta$) modulation is applied to the DTC to spread out the spurs. With these innovations, the mm-wave frequency synthesizer developed in this work demonstrates superior phase noise performance with the best-ever-reported power efficiency (i.e., figure-of-merit).

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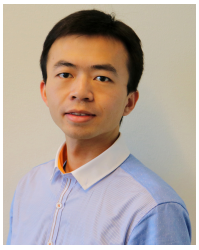

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