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1 Introduction

Ultrasound imaging is widely used in medical diagnosis and treatment. Recent advancements in technology have led to significant changes in the form factor of ultrasound devices, transitioning from traditional handheld probes to smaller and more portable devices, like pocket-sized handheld scanners [1], endoscopes [2], catheters [3], pills [4], and patches [5]. Additionally, 2D arrays capable of generating 3D images are becoming more common, not only in handheld probes but also in miniature probes like endoscopes and catheters [2, 3]. The increased demand for accessibility and ease of use have led to the development of ultrasound devices that are cost-effective and require minimal training. These advancements have the potential to revolutionize medical imaging and enable the early detection and treatment of diseases.

Integrated circuits play a key role in these developments. The electronics architecture of conventional imaging systems, which is based on commercial off-the-shelf components, is not scalable to the new form factors, particularly in terms of size and power consumption. Furthermore, the conventional architectures are not suitable for 3D imaging in terms of channel count. The integration of transceiver circuits with the ultrasound transducer array can address these issues [2, 6, 7]. Additionally, the move from bulk-piezoelectric transducer technology to micro-machined transducers, combined with the integration of circuits, has the potential to significantly reduce the cost of ultrasound devices, making them more accessible for widespread use [1].

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This chapter provides a review of the state-of-the-art in integrated circuits for next-generation ultrasound imaging devices. Section 2 starts by giving an overview of the electronics architecture of conventional ultrasound imaging systems and discusses the limitations of this architecture in terms of channel count and miniaturization. This motivates the use of in-probe integrated circuits. Section 3 focuses on the most commonly used channel-count reduction technique: sub-array beamforming. After discussing its basic operating principle, an overview is given of possible circuit implementations. Section 4 discusses full digitization of the echo signals in the probe, which can provide further channel-count reduction and paves the way to more advanced signal processing in the probe. Section 5 illustrates the use of these techniques in the context of a catheter-based 3D intracardiac probe. This chapter ends with conclusions and an outlook on future work.

2 Ultrasound Electronics Architectures

2.1 Conventional Ultrasound Imaging Systems

Figure 1 shows a schematic representation of a conventional ultrasound imaging system linked to a probe housing an array of N transducer elements, each of which performs the dual role of transmitting (TX) and receiving (RX) acoustic waves [8]. These transducer elements are connected via cables to transceiver channels within the imaging system.

In order to emit an acoustic wave for imaging purposes, these elements are driven by timed pulses, orchestrated by a TX beamformer, with the objective of achieving a desired spatial distribution of the acoustic wave. Typically, this involves focusing the acoustic wave at a selected point along a scan line. To ensure the acquisition of sufficiently strong echoes, even from the most distant points within the imaging region, where signal attenuation significantly reduces signal strength, high-voltage (HV) pulses are commonly utilized to drive the transducer elements. These HV pulses exhibit voltage levels ranging from tens of Volts to well over 100 V.

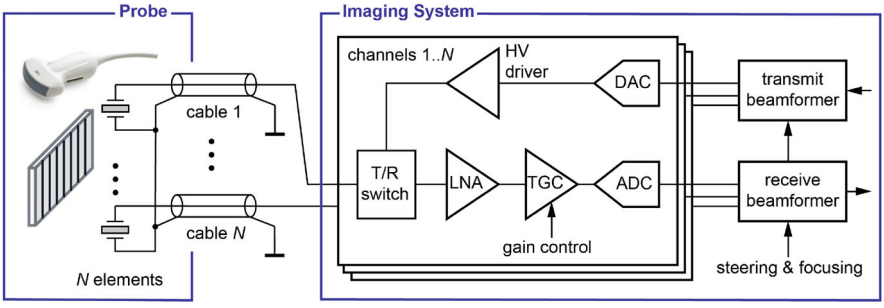

Fig. 1 Block diagram of a conventional ultrasound imaging system

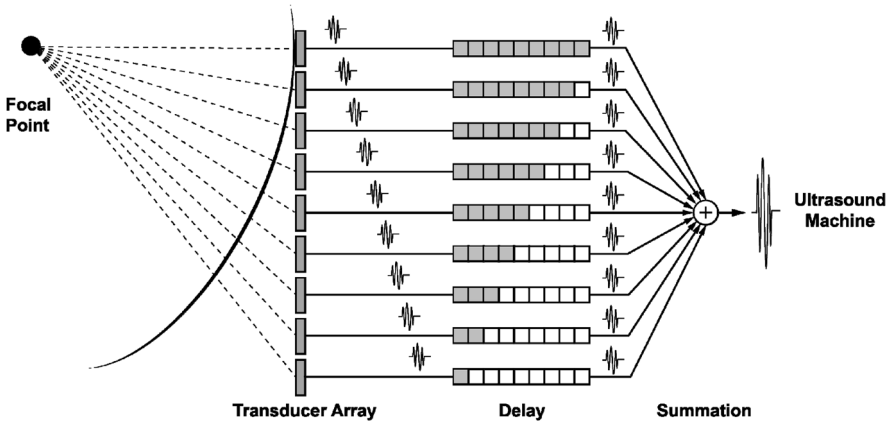

Fig. 2 Receive beamforming by means of a delay-and-sum operation

These pulses are conveyed to the transducer elements through transmit/receive (T/R) switches, which serve the critical role of protecting the low-voltage receive circuits during pulse transmission.

Following transmission, each transducer element receives the resulting echo signals, also referred to as the element-level RF signals, which are amplified by a low-noise amplifier (LNA). The first echo signals received, which come from scatters close to the probe, typically have higher amplitudes than the echoes arriving later, which come from deeper scatters and hence are subject to more propagation attenuation [9]. To compensate for this decrease in signal strength, a time-gain compensation (TGC) amplifier is used. This amplifier provides a gain that increases exponentially with time [8]. This significantly reduces the echo-signal dynamic range. Finally, the echo signals are digitized using an analog-to-digital converter (ADC), usually preceded by an anti-aliasing filter (not shown in Fig. 3).

The digitized echo signals are combined using an RX beamformer, in the simplest case using a delay-and-sum operation, as illustrated in Fig. 2. This process is aimed at constructively adding signals from a specific focal point while suppressing signals from other locations [8, 9]. The resulting beamformed RF signal undergoes additional processing to generate an image. For example, in the case of conventional brightness-mode (B-mode) imaging, both the TX and RX beamformers focus on a scan line within the medium. The beamformed RF signal is subjected to envelope detection and log-compression to obtain the brightness along the corresponding line in the image. To form the complete image, multiple scan lines are combined, each requiring a cycle of pulse transmission and echo reception [9].

In the architecture of Fig. 1, each transducer element is connected using a cable to a transceiver channel in the imaging system. As a result, the number of elements is limited by practical constraints, e.g. in cable count and system size, to a maximum of 256 for high-end imaging systems [10]. This implies that for the matrix transducers

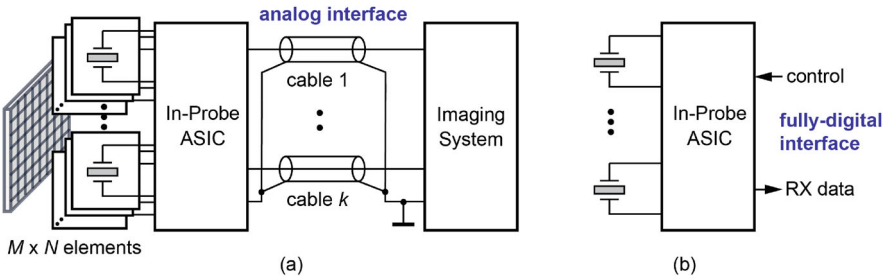

Fig. 3 Ultrasound probe with in-probe ASIC, employing (**a**) an analog interface to an imaging system; (**b**) a fully digital interface

needed for 3D imaging, which readily consist of thousands of elements, alternative solutions are needed, typically involving in-probe electronics.

2.2 In-Probe Electronics

One of the main reasons for incorporating application-specific integrated circuits (ASICs) into ultrasound probes is to address the challenge of interfacing transducer arrays with many elements, as required for 3D imaging, with an imaging system with a much smaller number of channels (as depicted in Fig. 3a). Several strategies have been employed to address this challenge, including the use of multiplexing [11–13] and sub-array beamforming [2, 6, 14, 15], which will be discussed in more detail in Sect. 3. In these cases, the ASIC provides analog output signals to the imaging system. Moreover, in-probe ASICs contribute to enhancing the signal-to-noise ratio (SNR) by locally amplifying the echo signals received by the transducer elements. This local amplification helps prevent the signal loss associated with connecting the small, high-impedance elements of a matrix transducer to long cables [16–18].

To interface with the transducer elements, in-probe ASICs contain front-end transceiver circuits, including high-voltage transmitters, LNAs, and programmable-gain or TGC circuits. While functionally similar to the front-end circuits found in an imaging system (see Fig. 1), these building blocks typically need to meet stringent size and power-consumption constraints when integrated into the probe. Their optimization is therefore an important part of the design of in-probe ASICs. A detailed discussion of the front-end transceiver circuits is beyond the scope of this chapter. The interested reader is referred to [19] for a detailed review.

The potential role of ASICs integrated within the ultrasound probe extends beyond improving SNR and reducing the number of channels. They can offer additional capabilities, such as complete digitization (as shown in Fig. 3b) and additional processing of the echo signals [7, 15, 20–24]. This becomes particularly critical in the context of portable ultrasound probes, where traditional imaging

systems with analog front-ends and ADCs will be replaced by smartphones or tablets [1]. Consequently, the traditional data acquisition functions previously handled by the imaging system now shift to the ASIC, while the image-processing tasks are carried out through software. In-probe digitization will be discussed in detail in Sect. 4.

3 Sub-Array Beamforming

3.1 Operating Principle

Full-array beamforming for large element-count arrays is challenging due to the large delay depth required for each element, which is typically a few microseconds. The sub-array beamforming scheme [14], also known as "microbeamforming," mitigates this issue by dividing the beamforming task into two steps (Fig. 4). A coarse delay that is common for all elements within one sub-array is applied in the external imaging system, while only fine delays for the individual elements (typically less than 1 μs) are applied by the sub-array beamformers in the ASIC, which significantly reduces the implementation complexity of the required on-chip delay lines.

Sub-array beamforming with a sub-array size of N elements reduces the number of channels by a factor of N, thus reducing the complexity of the remaining signal path. However, it does not provide the raw data of the full array and introduces focusing errors [25]. These result in increased grating and sidelobe levels as well as broadening of the main beam, all negatively impacting image quality. Narrower transmit beams can be used to mitigate these effects but require more acquisitions per volume, ultimately leading to a trade-off between sub-array size, with related channel-count reduction, and achievable frame rate [26].

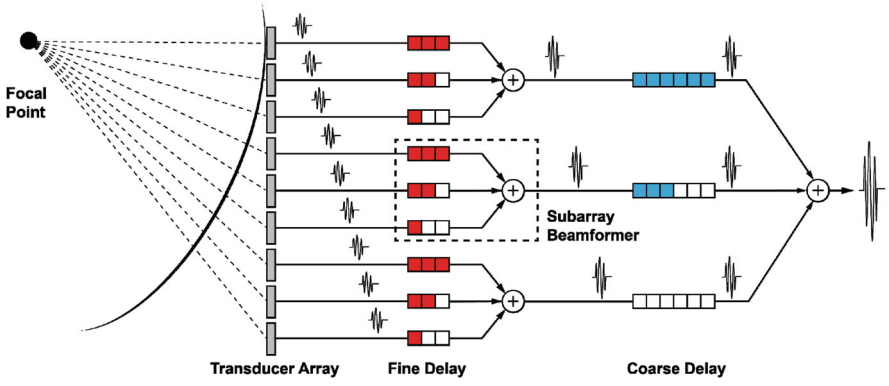

Fig. 4 Subarray beamforming by means of two-step delay-and-sum

3.2 Circuit Implementation

Various RX beamformer topologies have been used to realize the delay-and-sum process. One option is to digitize the element-level RF signals and subsequently beamform these in the digital domain [22]. This solution, however, requires a relatively large die area and power consumption. Analog beamformer topologies can be broadly classified into three categories: beamformers based on phase rotation applied to I/Q demodulated RF signals [27]; beamformers based on continuous-time delay lines, in which the delays are tuned continuously [28, 29]; and beamformers based on discrete-time delay lines, in which the delays are discretized, conforming to a clock signal [2, 14, 15, 30–33].

The phase-rotation-based beamformer as shown in Fig. 5a applies direct I/Q demodulation to bandpass-filtered RX signals followed by digitization. The digitized I/Q signals are fed to a series of phase rotators in the digital domain to approximate time delays before the summation takes place. In [27], a direct sampling I/Q demodulation is employed, and analog-to-digital conversion is required for each I/Q channel.

The solution is attractive for narrow-band ultrasound signals, for which phase shifting is a good approximation for delay, and which can be multiplexed on a

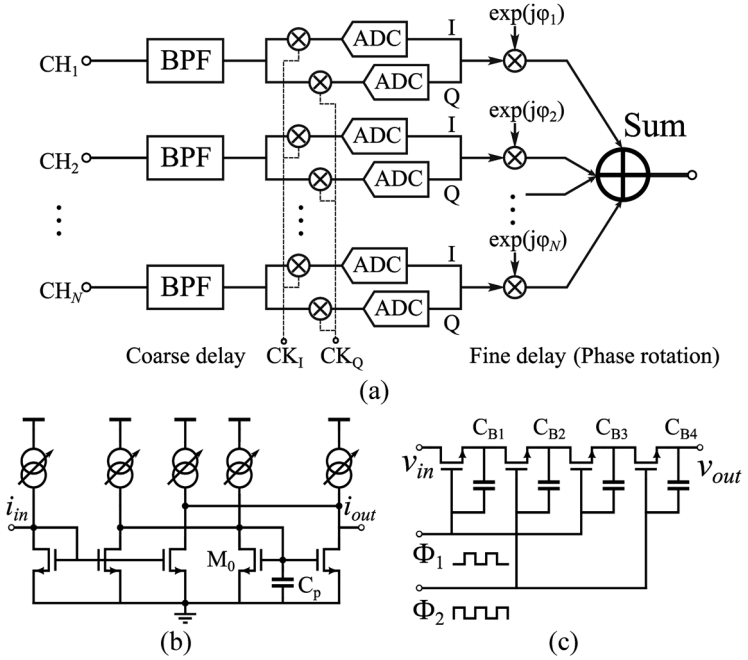

Fig. 5 Circuits for RX beamforming: (**a**) direct I/Q demodulation in conjunction with digital phase rotation [27]; (**b**) continuous-time delay cell [28]; (**c**) BBDs-based delay line [30]

high-speed ADC, thus saving area. However, echo signals in ultrasound imaging generally have a wide bandwidth, e.g., a fractional bandwidth of 80% around the transducer's resonance frequency, calling for many high-speed ADCs and making this solution less attractive.

As depicted in Fig. 5b, a continuous-time delay cell employs current mirror-based circuits to construct an all-pass filter, which is a first-order approximation of an ideal delay, tuned by the bias currents of the current mirror network. A delay line can be constructed by cascading a number of such delay cells [28]. The implementation has no passive devices and is potentially small. However, it suffers from non-linear phase response, resulting in different delays for different frequency components in a wide-band ultrasound signal and high sensitivity to temperature and process drift.

A discrete-time delay line using bucket-brigade devices (BBDs) [30] is shown in Fig. 5c. A series of bucket capacitors, $C_{B1–4}$, stores the information as charge packets transported by means of MOS transistors. The speed of the charge transportation is controlled by two complementary clock signals, making the delay step equal to the clock period. Although the BBD delay line uses a minimum number of transistors and occupies a small area, it suffers from poor charge-transfer linearity.

Other types of discrete-time beamformers are based on switched-capacitor [2, 14, 31] or switched-current delay lines [32]. Figure 6a shows a switched-capacitor implementation, in which every output sample of the beamformer is generated by combining delayed sampled-and-held versions of the input signals, stored on a bank of capacitors. To accommodate delays larger than the sampling interval T_s, k time-interleaved delay-and-sum channels are used, each of which contains N memory capacitors, one for each input channel. These k channels alternately generate the beamformer output, by the successive closing of read switches $R_{1..k}$, which connect the capacitors of one of the channels to the output, causing signal summation in the charge domain. The effective delay experienced by input signal V_j ($1 \leq j \leq N$) is determined by the time delay between the opening of the write switches W_{ij} and the closing of the read switches R_i. Thus, the relative delays between adjacent channels are accurately defined by the falling edges of the write clock signals (e.g., the delay τ_1 between channels 1 and 2 is determined by the falling edges of W_{i1} and W_{i2}).

While, in this example, summation takes place in the charge domain [2], it can also similarly be implemented in the voltage domain [31] or the current domain [32]. A disadvantage of these approaches is that a large number of memory capacitors, i.e. $N \times k$ capacitors, is needed, along with the associated switches and interconnections.

To substantially reduce the number of required components, the delay-and-sum operation can be replaced by a sum-and-delay operation, as shown in Fig. 6b [15, 33]. Here, k time-interleaved channels are used to generate the beamformer output, but each channel only contains one memory capacitor, reducing the number of capacitors by a factor of N. This is enabled by applying the input signals to the beamformer in the current domain, rather than in the voltage domain, allowing the summation of the signals from different input channels to take place in the current domain at the input. The writing switches W_{ij} now determine during which

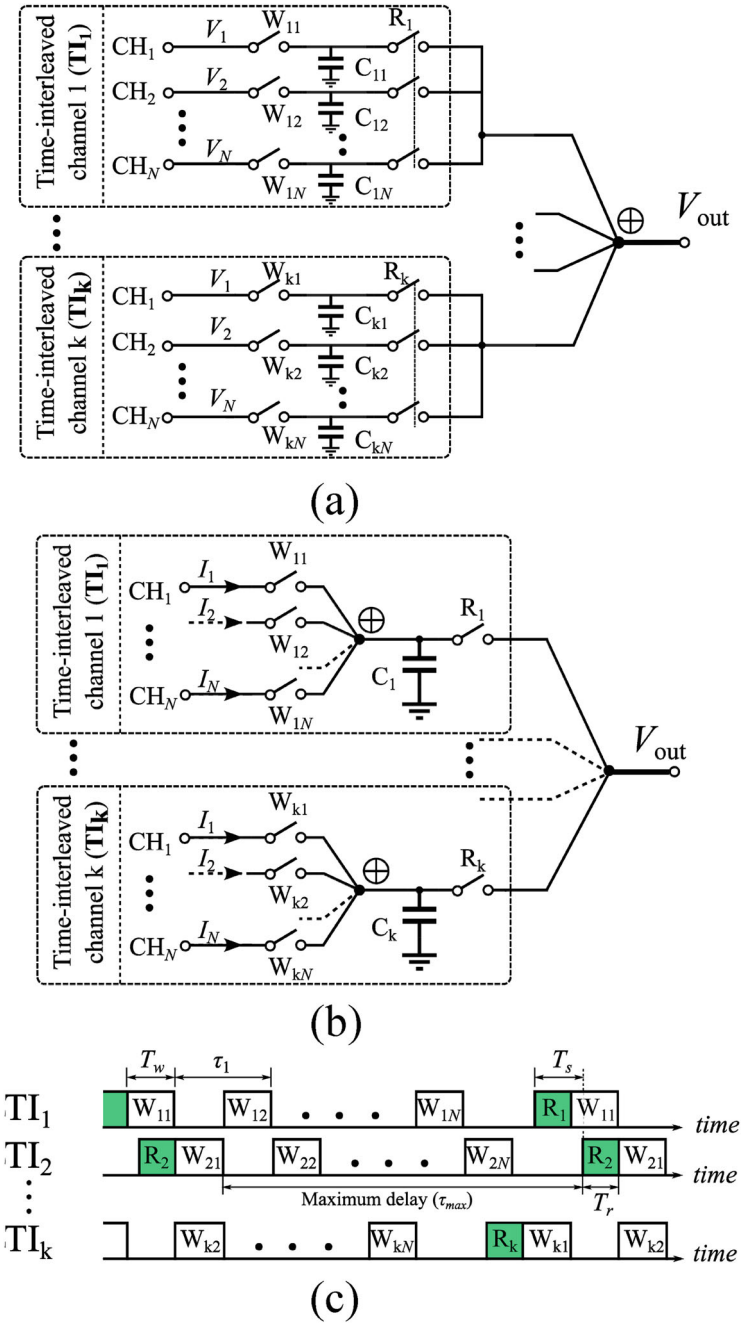

Fig. 6 Discrete-time RX beamformers based on (**a**) sample-and-hold delay lines [2, 14, 31]; (**b**) boxcar integration [15]

time interval the input current is integrated on the memory capacitors, rather than determining when the input signals are sampled-and-held, like in Fig. 6a. As before, the time delay between this interval and the closing of the corresponding read switch R_i determines the effective time delay that an input signal experiences. An added benefit of this solution is that the integration of the current-mode inputs on the memory capacitors forms a boxcar sampler, which provides inherent anti-aliasing for the sampling in the beamformer [15].

4 In-Probe Digitization

Most in-probe ASICs perform signal conditioning, sub-array beamforming, averaging, or multiplexing in the analog domain and provide analog output signals connecting to an imaging system, where digitization takes place. Nevertheless, there is a growing trend to move the analog-to-digital conversion into the probe as well, closer to the transducer. This offers many potential benefits, including further cable-count reduction by leveraging high-speed digital datalinks [21, 23, 34], and the integration of digital processing functions into the probe [1, 35]. In-probe digitization can take place at the element-level, or after initial processing of the signals of multiple elements in the analog domain, e.g., after sub-array beamforming.

4.1 Element-Level ADCs

Element-level digitization has the important advantage that it grants direct access to the RF data from all individual elements, eliminating any constraints imposed by analog pre-processing on the imaging algorithms. The main challenge associated with element-level digitization is the limited power and area budget typically available for element-level ADCs.

Various attempts have been made to tackle this challenge. In [36], a digital beamformer using element-level successive-approximation-register (SAR) ADCs following conventional analog front-ends was presented. The ADC employs a conventional charge-redistribution capacitive digital-to-analog converter (DAC), hence requiring substantial silicon area, preventing it from being pitch-matched integrated with the transducer array. In [22], this issue was addressed by leveraging a nanoscale CMOS process to integrate a $\Delta\Sigma$ ADC along with an analog front-end within the area of a single transducer element, albeit at an energy efficiency that is not yet competitive with the analog approach.

Improvements in size and energy efficiency can be potentially obtained by exploiting specific characteristics of the ultrasound signals being digitized. For instance, in [37], a dynamic-bit-sharing technique was proposed based on the similarity of beamformed ultrasound signals, which allows adjacent element-level

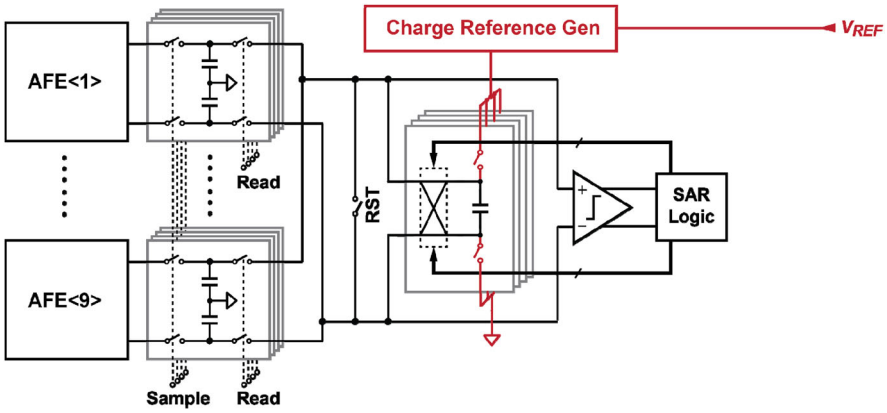

Fig. 7 Beamforming SAR ADC [21]

SAR ADCs in a 2 × 2 sub-array to share the most-significant bits, thus saving power. Another opportunity to save power and reduce size is to exploit specific characteristics of the transducer in the digitization process. An example is the use of the transducer as the electromechanical loop filter of a bandpass $\Delta\Sigma$ ADC in [38].

4.2 Beamforming ADCs

To avoid the large area and power impact of element-level digitization, several designs have employed converters that operate based on the output of a preceding sub-array beamformer. In [39], analog sub-array beamforming based on capacitive sample-and-hold cells precedes digitization with a SAR ADC. While this effectively reduces the required number of ADCs, the approach still requires an additional summing amplifier to realize the sub-array beamforming and a separate ADC driver.

To reduce these additional cost factors, [21] proposed the merging of sub-array beamforming and digitization to a dedicated beamforming ADC, as shown in Fig. 7. Multiple element-level signals are provided via individual analog front-ends to capacitive sample-and-hold cells to time-delay the element-level RF signals. To avoid the summing amplifier, summation is accomplished by passive charge redistribution when switching capacitive cells in parallel based on pre-determined timing. By employing a charge-sharing ADC, the combined charge can directly be used as the input for digitization. The converter operates by switching binary-scaled units of a pre-charged capacitive digital-to-analog converter (CDAC) in parallel or anti-parallel to the charge-domain input. The switching polarity is determined with an asynchronous comparator and SAR logic to successively approximate input signal. A low-bandwidth reference generator can be applied by using two CDACs and pre-charging one while the other is in operation.

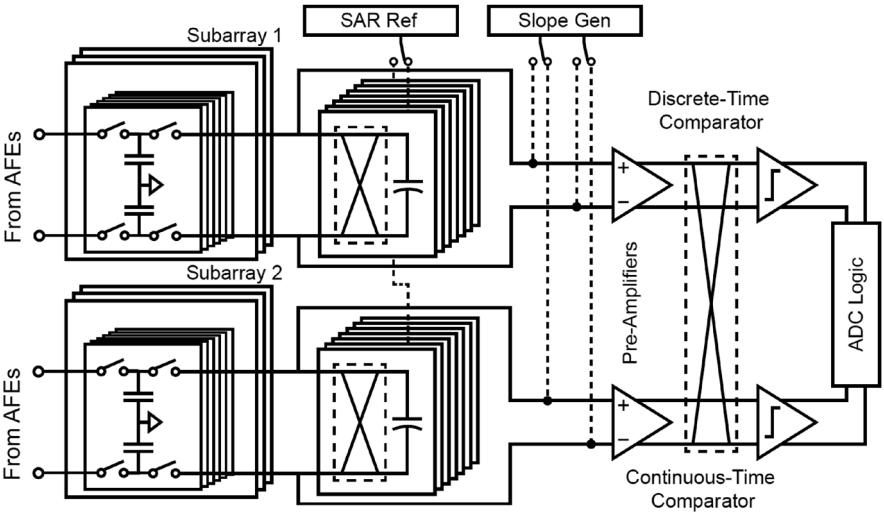

Fig. 8 Hybrid Beamforming ADC [24]

This approach is particularly efficient in reducing the element-level power consumption, but still limits integration density due to the relatively large footprint. Two of the main challenges for the reduction of area are the requirement for a second CDAC and exponential scaling of the size of the SAR architecture with increased resolution.

One way to mitigate the area impact of the converter is to transition to a hybrid beamforming ADC, as proposed in [24] and displayed in Fig. 8. While a slope ADC is typically too slow to efficiently convert ultrasound signals with center frequencies in the order of several MHz, it can be employed to convert the residue of a preceding SAR step. The SAR is again implemented as a charge-sharing topology for direct integration with the sub-array beamformer, but the overhead from exponential scaling is reduced due to its lower resolution requirement. Additionally, no second CDAC is required as the pre-charging can be performed during slope conversion. By letting the SAR and slope phase of two neighboring sub-array converters run in opposite phases, the design makes efficient use of the arrayed nature of ultrasound imaging with hardware sharing. One SAR reference generator and one slope generator are sufficient to serve two channels. While the slope ADC requires a continuous-time comparator and the SAR operation a discrete comparator, these can also be efficiently shared by switching them between two channels.

In conclusion, in-probe digitization can provide significant channel-count reduction and enable upcoming signal processing. Current developments in data converters tailored to ultrasound imaging have made the associated power and area requirement feasible and make the technique one of the major drivers of product miniaturization.

4.3 Datalink Solutions

Once in-probe digitization is adopted, the conventional analog RX signal transmission from the probe to the imaging system is replaced by a digital datalink. To realize this at modest data rates, a solution is to multiplex the entire array onto a single ADC and data channel [20]. This implies that multiple transmit/receive cycles are needed to acquire a full RX data set, leading to a reduction in frame rate.

This problem can be mitigated, without increasing the cable count to the number of RX channels, by exploiting the fact that most cable connections between probes and imaging systems have bandwidths exceeding the bandwidth required by a single RX channel. Therefore, a single cable can be in principle shared by multiple RX channels. For analog signaling, this has been realized using time-division multiplexing (TDM) techniques [13, 40]. TDM is also possible in the digital domain [21] and provides the additional benefit of avoiding the susceptibility to crosstalk and interference associated with transmission of analog signals across non-ideal cable assemblies [40]. Together with potential benefits from upcoming in-probe data processing, this makes digital links especially promising.

To date, probes with digital interfaces typically employ conventional communication standards like low-voltage differential signaling (LVDS) [21, 24, 38]. While such standards ensure reliable communication with very low bit-error rates, they may be too power-hungry for power-constrained probes like imaging catheters. Power can be saved by exploiting the fact that bit error rates can be tolerated in digitized ultrasound RF data that are orders-of-magnitude higher than what is typically acceptable in datalinks, without noticeable impact on B-mode image quality [41]. To reduce the power consumption associated with data transmission and the cost of complex cable assemblies, [23] has investigated a custom datalink specifically for catheter-based ultrasound probes. An optimization of the channel bandwidth is achieved with multi-level signaling and a load modulation architecture shifts part of the associated power consumption from the probe to the imaging system in order to reduce heating of the catheter tip.

An alternative path is explored in optical communication [42]. With advances in the integration of optical modules, the larger bandwidth provided by optical fiber communication becomes more accessible and can potentially enable large channel-count reduction factors in the future.

5 Case Study: A 3D Intracardiac Probe

The following case study demonstrates the principles discussed in this chapter using the example of a 3D intracardiac echocardiography (ICE) probe as it reflects the challenges associated with upcoming miniaturized 3D ultrasound imaging devices. ICE is typically used in minimally-invasive cardiac procedures, such as catheter ablation used to treat cardiac arrhythmia [43]. The imaging catheter is inserted into

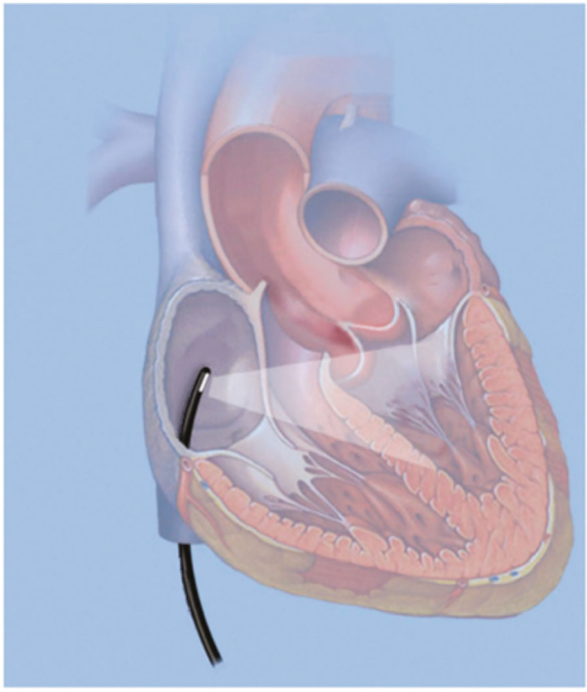

Fig. 9 Intracardiac echocardiography procedure example

the heart via the vascular system as shown in Fig. 9 and provides guidance for the intervention. Due to the size constraints of the ICE catheter, with a diameter in the order of 3 mm, integration of circuitry at the catheter tip is challenging, and the number of cables that can be accommodated in the catheter shaft is limited. In addition, power consumption is tightly constrained in order to prevent excessive tissue heating. The presented design implements a high-frame-rate imaging scheme described in [25]. The design is described in detail in [23, 24].

Figure 10 shows the global architecture of the implemented design. Each transducer element connects to element-level unipolar pulsers with an integrated transmit/receive (T/R) switch. On the receiver side, each transducer connects to a separate analog front-end, consisting of a first-stage low-noise amplifier (LNA) and a second-stage programmable-gain amplifier (PGA), which also performs conversion of the single-ended transducer signal to a differential output. Together, the two stages provide time-gain compensation (TGC) to limit the dynamic range of the signal for the following blocks. This is achieved by adjusting their gain along with the time-dependent attenuation of the ultrasound signal in the imaged medium.

Three element-level receiver outputs are subsequently combined in a sub-array beamformer. By only combining three elements in one direction of the 2D transducer array, only few acquisitions have to be performed per reconstructed volume and a high frame rate can be achieved. The beamformer is realized using capacitive sample-and-hold cells. Two beamformers are merged with a hybrid ADC

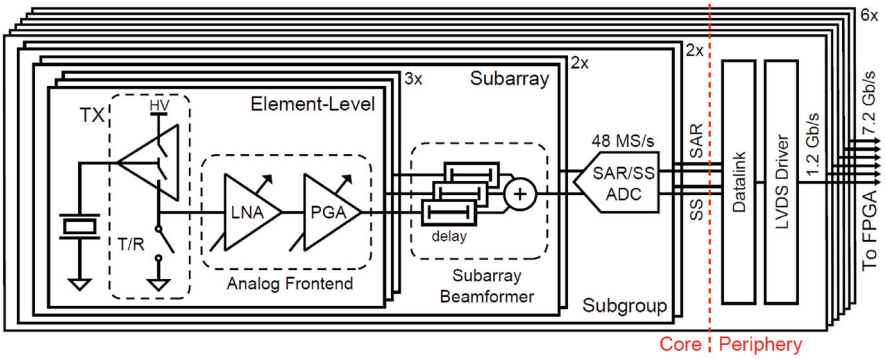

Fig. 10 Architecture of a prototype ASIC for a high-frame-rate 3D ICE probe

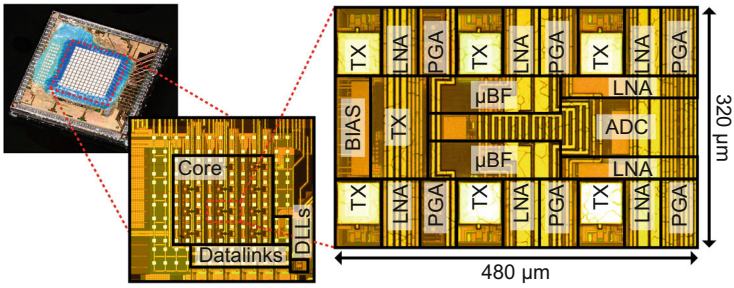

Fig. 11 Chip micrograph and subgroup layout

in a subgroup. The ADC operates based on a SAR first stage and a single-slope (SS) second stage, as discussed in Sect. 4.2.

To maximize the available area for circuitry underneath the transducer array, the signals are forwarded to the periphery of the chip as soon as they are quantized. While the core area is quite constrained by the 160-µm pitch of the transducer elements, there is more space available at the long ends of the catheter tip, and a digitally synthesized module is implemented at the periphery. This implements recombination of the hybrid ADC output, 8-bit/10-bit encoding, and serialization to LVDS drivers for data transmission.

An overview of the implemented prototype is given in Fig. 11. It shows the fabricated chip with a transducer matrix manufactured on its surface. The chip was fabricated using a 180-nm BCD process, and the transducer array has a pitch of 160 $\times$ 160 µm with a center frequency of 6 MHz. There are a total of 72 active elements plus two rings of dummy transducers in order to reduce edge effects.

The first inset shows a micrograph of the electronics below the transducer array. The core area features circuitry pitch-matched to the transducers, and the datalinks are concentrated on one side in order to enable scalability to a full probe in the order of 1000 elements.

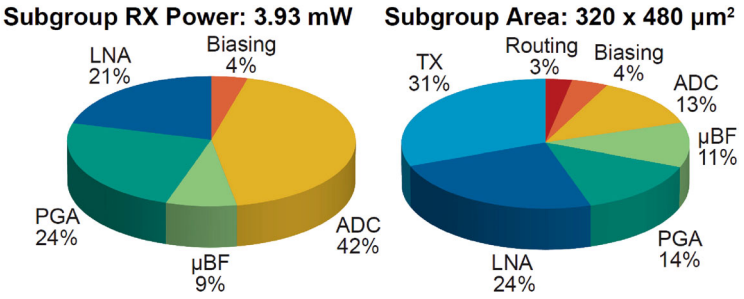

Fig. 12 Element-level power and area distribution

	This Work	Lee et al. JSSC'21	Li et al. VLSI'19	Chen et al. JSSC'18	Wildes et al. TUFFC'16
Process	**180 nm BCD**	180 nm	180 nm	180 nm	N/A
Transducer	**6 MHz 2D PZT**	5 MHz 2D PMUT	5 MHz 2D PZT	5 MHz 2D PZT	5.6 MHz 2D PZT
Array Size	**8 x 9**	6 x 6	4 x 4	6 x 24	60 x 14
Integrated Transducer	✓	✗	✓	✓	✓
Pitch-Matched	✓	✗	✓	✓	✓
Element Pitch	**160 µm x 160 µm**	250 µm x 250 µm	150 µm x 150 µm	150 µm x 150 µm	110 µm x 180 µm
Integrated TX	**65 V**	13.2 V	✗	✗	40 V
Digitization	✓	✓	✓	✓	✗
Chan. Reduction	**12–fold**	N/A	N/A	36–fold	15–to 20–fold
Supported Frame-Rate	**1000 vol/s**	N/A	N/A	200 vol/s	50 vol/s
RX Power / El.	**1.23 mW**	1.14 mW	1.54 mW	0.91 mW	< 0.12 mW
Input DR	**91 dB**	N/A	N/A	85 dB	N/A

Fig. 13 Comparison to the prior art

The second inset shows the footprint of a single subgroup of six elements. Two sub-array beamformers are laid out together in order to make best use of the hardware sharing in the hybrid ADC. The subgroup is used as the lowest unit-cell and is replicated in order to achieve larger apertures.

The distribution of RX power and area per elements is shown in Fig. 12. The power is fairly and evenly distributed between the analog front-end and the ADC. TX power consumption depends heavily on the applied imaging mode but has generally a fairly low contribution due to the heavy-duty cycling between transmit and receive in ultrasound imaging.

In the area overview, the effect of hardware sharing in the ADC in visible. With the sub-array beamformer included, the beamforming ADC only occupies 24% of the total subgroup space, and the transmitter is actually the largest contributor with almost one-third. This is due to the large spacing required for HV structures in junction-isolated technologies.

Figure 13 summarizes the system characteristics and compares the design to the prior art in catheter-based ultrasound systems. This is the first work to integrate HV transmitters, analog front-ends, sub-array beamforming, and in-probe digitization for scalable 3D imaging. A dedicated architecture enables the highest reported frame rate at a competitive power consumption.

6 Conclusions

This chapter has reviewed pitch-matched circuit solutions for emerging ultrasound imaging devices, such as 3D imaging catheters, portable ultrasound scanners, and wearable ultrasound patches. It has focused on approaches for in-probe receive beamforming and digitization, which are crucial for the channel-count reduction needed in high-element-count probes for 3D imaging.

Currently, most in-probe ASICs act as an interface between the transducer and a conventional imaging system, providing amplification for improved SNR, and channel-count reduction for 3D imaging, by multiplexing or sub-array beamforming. An emerging trend is to move from analog outputs to full in-probe digitization, to provide a robust digital interface to the system. This will enable further data reduction by means of in-probe digital signal processing. Moreover, standardized digital interfaces could ease the integration with other tools supporting the physician. Eventually, this can lead to the disappearance of imaging systems, with all front-end electronics integrated on-chip in the probe, and image processing moved to software. Compared to PCB-based solutions [44], this is an essential step to reduce the size and cost of handheld ultrasound scanners. It is even more crucial for future wearable ultrasound devices, which can bring ultrasound technology to the home environment, for instance for long-term monitoring applications. Such devices will have to operate from a small battery and communicate wirelessly, for instance with a smart phone. This will come with many new challenges, such as the need for drastic data reduction and improvements in power efficiency, which call for further advances in integrated circuit design for ultrasound applications.

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