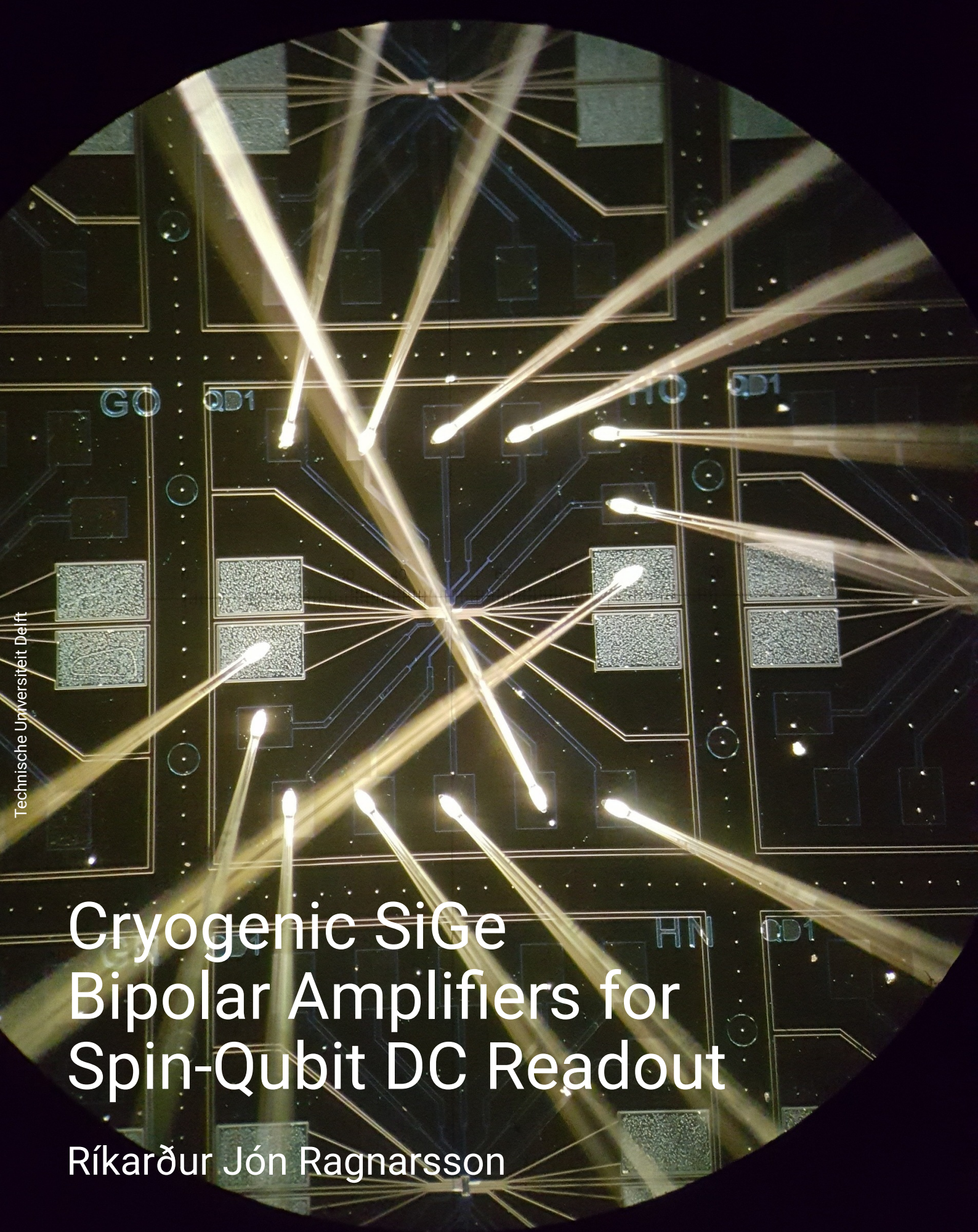

Technische Universiteit Delft

Cryogenic SiGe Bipolar Amplifiers for Spin-Qubit DC Readout

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TU Delft

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by

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TU Delft

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Ríkarður Jón Ragnarsson
Delft, January 2021

Abstract

In recent years, quantum computers have become increasingly popular, with high-profile companies investing more and more resources into the development of quantum-computing prototypes. Such interest is motivated by the exponential increase in the computing power that quantum computers offer over classical computers, which may be used in several practical applications, such as producing faster and more accurate solutions to machine learning algorithms, the quantum simulations of molecules for drug and material synthesis, techniques that combat cybersecurity threats, and more. Quantum processors are typically placed in a dilution refrigerator, which cools down the processor to near absolute zero to make use of their quantum behavior. These fridges are large in scale and require multiple long wires from the processor to the readout/control equipment, which mostly resides at room temperature. However, although this approach is suitable for currently available systems with few quantum bits (qubits), it is unpractical for future quantum computers, with thousands or millions of qubits, due to the interconnect bottleneck. One solution is to move the readout/control circuits closer to the processor to avoid the need for bulky unreliable interconnects. However, this has proven to be difficult due to the limited cooling power of the fridges, which is below a few Watts at 4 K and below a few mW at temperatures below 100 mK. These limitations stress the need for low power readout/control circuitry of the processor as the number of qubits in a single processor increases. This thesis focuses on an ultra-low-power cryogenic amplifier design for the readout of spin qubits.

Only recently, the cryogenic performance of Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBT) has been demonstrated to be specifically suited for the cryogenic readout of spin qubits, because of their ultra-low-power and their high sensitivity. This thesis focuses on the standard SiGe HBT available in the IHP 0.13μm SG13G2 BiCMOS process and on an optimized variant with modified doping profiles for enhanced current gain. As a first step, a comprehensive cryogenic (4 K or 15 K) DC characterization of the SiGe HBTs, CMOS transistors, and resistors is performed. This data proves the suitability of such technology for cryogenic application and will enable the future integration of a complete qubit readout, including SiGe front-end amplification and CMOS back-end post-processing. The measurement results of the SiGe HBT characterization show outstanding cryogenic performance for low power applications, with an attainable current gain in the standard HBT of 100, 500, and 1000 at a power dissipation of 61nW, 2μW and 30μW, respectively, and, for the modified HBT, of 100, 500 and 1000 at a power dissipation of 5.5nW, 90nW, and 140nW, respectively.

To mimic the spin qubit readout, a discrete amplifier employing a SiGe HBT produced in the IHP SG13G2 process has been built and used to characterize a single-electron transistor (SET), with both the SET and the amplifier operating at 4 K. By comparing the charge-stability diagram measured with room-temperature equipment, the proper operation of the proposed amplifier is demonstrated. Furthermore, the amplifier characterization showed a gain > 40 dB with an 113 kHz -3-dB bandwidth, and Signal-Noise Ratio (SNR) above 10 dB for a total measurement time of $t_{total} < 10$ μs, thus demonstrating performance compatible with the requirements for single-shot readout in state-of-the-art spin-qubit computers. Overall, the results show the capabilities of the SiGe HBT in low power cryogenic applications as well as the capabilities of the 0.13μm BiCMOS technology for the future full integration of qubit readout schemes.

Contents

List of Figures

List of Tables

1 Introduction

1.1. Quantum Computing

The fundamental principle of a conventional computer is storing and processing information represented by strings of logical bits, ones and zeros, meaning that each bit can either be considered in a low state (0) or a high state (1). A quantum computer, however, uses quantum states to encode information. Similar to the classical bits, the quantum state can be the ground state $|0\rangle$ or the excited state $|1\rangle$. Different from classical computing, quantum physics allows the state to be in a superposition of both states at the same time until it is read out for processing. The advantage of such quantum bits (or "qubits") is that quantum superposition and quantum entanglement can be used to achieve massive parallelism, unlike the classical computers in which bits must be processed individually. This exponentially increases the computing power of a quantum computer in comparison to a classical computer, by doubling the computing power for each additional qubit. To put this into perspective, the information represented by only 50 qubits cannot even be stored in the memory of the largest supercomputer today [1], thus showing the immense potential of multi-qubit systems and the incentive for further development into quantum computers.

The development of large scale quantum computers would be crucial for enabling several practical applications that involve algorithms of exponential complexity, such as producing faster and more accurate solutions to machine learning algorithms, the quantum simulations of molecules for drug and material synthesis, techniques that combat cybersecurity threats, and more [2].

1.2. Cryogenic Electronics

Quantum processors are typically placed in a dilution refrigerator, which cools down the processor to near absolute zero to let the qubit manifest their quantum behavior. These fridges are large in scale and require multiple long interconnects from the processor to the readout/control equipment, which mostly resides at room temperature. Although this approach is suitable for systems with the few qubits (< 100) available today, it is unpractical for future quantum computers due to the interconnect bottleneck, e.g. with a million qubits, interconnects on the order of a million are needed [3]. This is evident in the cumbersome setup of a state-of-the-art 72-qubit processor, developed by Google in figure 1.1 [4]. So a more scalable solution is needed to reduce the complexity and ensure the reliability of the interconnects.

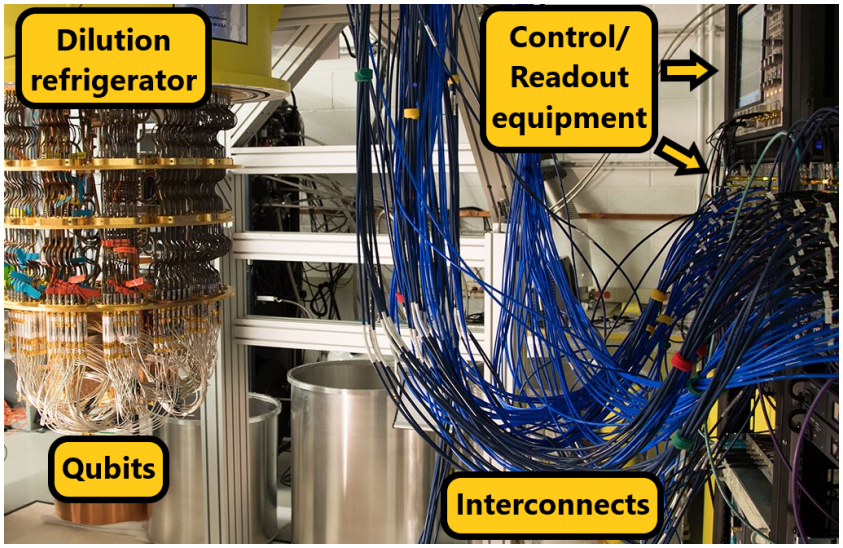


Figure 1.1: A 72-qubit system from Google, dilution refrigerator (Left) and control/readout equipment (Right) [5]

To solve the scalability issue of quantum computers, further development towards moving the control and readout equipment to lower temperatures and closer to the physical qubit is needed [6]. A system-block diagram of such approach can be seen in figure 1.2. This would significantly decrease the number of interconnects from room temperature down to cryogenic temperatures. This solution results in several challenges. First, the closer the circuitry gets to the mK-stage of the fridge, the less power it is allowed to dissipate before drastically affecting the temperature of all temperature stages in the fridge. The power dissipation is limited to roughly 1 W at the 4-K stage and a few mW below 1 K, thus increasing the need for low-power electronics at cryogenic temperatures. Second, the electrical characteristics of active and passive electronics are known to drastically change at cryogenic temperatures. Much research has gone into the characterization of silicon-based electronics over the last century, which has prompted further design of cryogenic circuits.

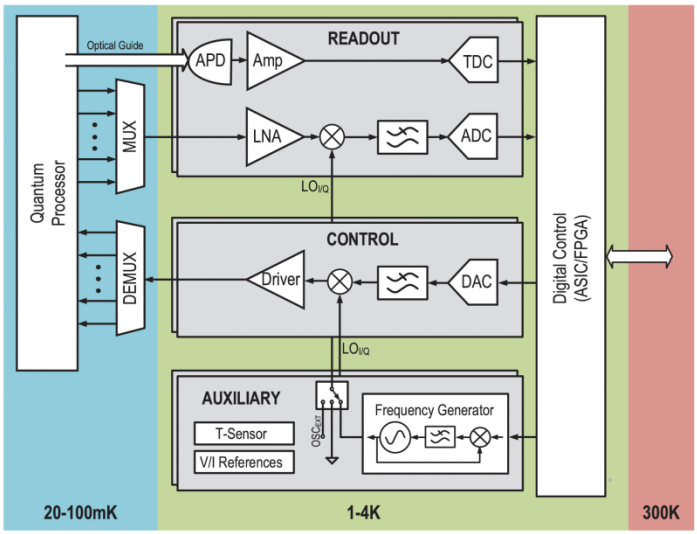


Figure 1.2: Cryogenic CMOS controller [6]

1.3. Thesis motivation

The motivation for this project is to enhance the readout of spin qubits. Spin qubits store information in the spin of an electron, distinguished by either spin up or spin down. The spin of an electron is difficult to readout directly, therefore a spin-to-charge conversion is employed in such readout schemes, where the elec-

tron charge is dependent on the spin state. Spin-to-charge conversion is performed using a single-electron transistor (SET) or a quantum point contact (QPC) which is capacitively coupled to the quantum dot and changes its conductance depending on the occupancy of the quantum dot. Multiple readout methods exist, mainly categorized into either radiofrequency reflectometry (RF readout) or DC current based readout (DC readout). Each method has benefits and drawbacks. The RF readout does not suffer from the parasitic capacitance of the long interconnects from room temperature down to cryogenic temperatures and mainly relies on the quality factor of an impedance-matching network for the detection bandwidth. Additionally, RF readout suffers from scalability issues due to its need for a large matching network and a directional coupler, which are difficult to integrate. DC readout suffers from the 1/f noise of the measurement equipment and the parasitic capacitance of the long interconnects that limits the readout time of the qubits to roughly 100s of microseconds [7]. State-of-the-art DC readout employs a cryogenic SiGe amplifier that relaxes the bandwidth limitations and lowers the readout time to below 10 μs [8]. These readout improvements motivate the investigation of SiGe devices in BiCMOS technologies as it provides the ultra-low-power, low-noise SiGe devices and the integration possibilities of silicon CMOS devices, further increasing the capabilities of future spin qubit readout/control systems. Therefore, this thesis will focus on the cryogenic characterization of the state-of-the-art 0.13μm BiCMOS technology from IHP to demonstrate its viability for the implementation of an integrated spin qubit readout.

1.4. Thesis objectives

There are two main objectives in this thesis. First, the cryogenic characterization of SiGe HBT, CMOS, and passive devices in a state-of-the-art SG13G2 0.13 μm BiCMOS technology and validate their functionality as a candidate for cryogenic circuits. The second is to show the potential performance of the characterized HBTs as an ultra-low-power cryogenic amplifier for the readout of DC spin qubits. This involves the aforementioned characterization of the HBT devices as well as the characterization of a single-electron transistor (SET), and the experimental characterization of a discrete HBT amplifier interfaced with an SET.

1.5. Thesis outline

The thesis outline is as follows:

Chapter 2: background information on the cryogenic behavior of SiGe HBT, CMOS, and passive devices, as well as an introduction to SETs and readout methods of spin qubits.

Chapter 3: A comprehensive cryogenic characterization of the BiCMOS technology and its comparison to room temperature and reported behavior from literature.

Chapter 4: An introduction and characterization of the SET device chosen for the project, as well as a demonstration of the tune-up process of a quantum dot.

Chapter 5: An analysis of a cryogenic ultra-low-power SiGe HBT amplifier for the readout of DC spin-qubits

Chapter 6: Conclusions and a discussion on possible future improvements in the field of DC spin-qubit readout.

2

Background

This chapter presents the cryogenic behavior of MOSFET and BJT devices as well as an introduction to spin qubits and various readout methods of spin qubits. The temperature dependence of the bipolar transistor is explained along with the advantages of the heterojunction bipolar compared to the homojunction bipolar for cryogenic operation. Changes in device parameters, such as the threshold voltage, the mobility, and the subthreshold slope in field-effect transistors are introduced, along with non-idealities, such as the kink effect and hysteresis. The chapter concludes with an introduction to the single-electron transistor as well as an introduction to readout methods of spin qubits.

2.1. Cryogenic performance of BJTs

Limited research has gone into the characterization of homogeneous bipolar transistor (BJT) at temperatures below liquid nitrogen temperatures due to their performance degradation with lower temperatures [9], resulting in them primarily being characterized at temperatures above 77 K (liquid nitrogen) [10] [11] [12] [13]. In [13], the optimization of epitexial silicon bipolar technology is explored for temperatures down to 77 K. The characterization shows a significant decreases in the current gain (fig. 2.1a) as well as an increased base resistance at lower temperatures due to base freeze-out (fig. 2.1b). The drastic degradation of these performance parameters at cryogenic temperatures has made the transistor unappealing as building blocks of cryogenic amplifiers or digital gates.

The decrease in the current gain is related to the temperature dependence in the bandgap energies of the emitter and base regions [14]. This temperature dependence can be understood with the following set of equations, beginning with equation 2.1.

$$\beta_{DC} \approx \frac{n_{i,B}^2 \cdot N_E}{n_{i,E}^2 \cdot N_B} \tag{2.1}$$

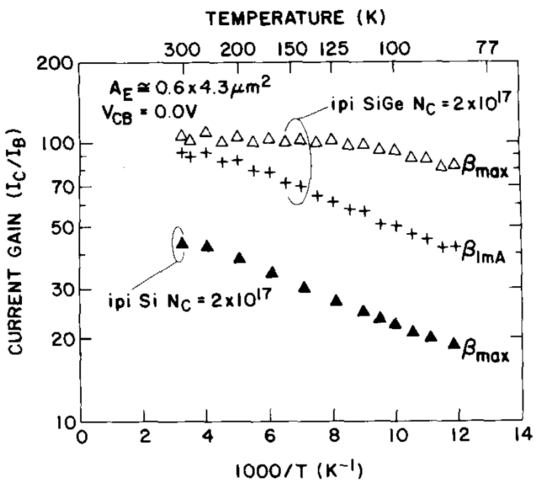
Where $n_{i,B/E}$ is the intrinsic carrier concentration of the base/emitter, and $N_{B/E}$ is the dopant concentration in the respective regions. With the intrinsic carrier concentration described with the following equation:

$$n_{i,B/E}^2 = exp\left(\frac{-\left(E_{g,Si} - \Delta E_{g,B/E}\right) \cdot q}{k \cdot T}\right) \tag{2.2}$$

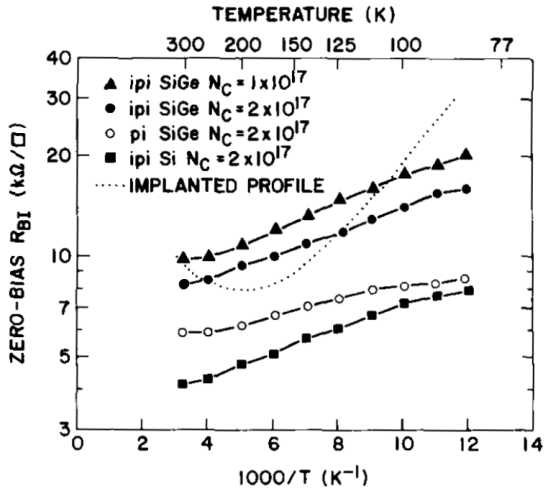
Where q is the charge of a single electron, k is the Boltzman constant, T is the temperature, E_g is the band gap energy of silicon, and $\Delta E_{g,B/E}$ is the band gap narrowing due to low temperature effects in the base/emitter regions. Combining equations 2.1 and 2.2 gives the following expression for the current gain:

$$\beta_{DC} \approx exp\left(\frac{q \cdot \left(\Delta E_{g,B} - \Delta E_{g,E}\right)}{k \cdot T}\right) \cdot \frac{N_E}{N_B} \tag{2.3}$$

Since the base and the emitter are of the same material, the band gap energy E_g is the same and cancel out by combining equations 2.1 and 2.2. However, the emitter has higher doping concentration than the base, so the low-temperature band gap narrowing of the base is lower than that of the emitter ($\Delta E_{g,B} < \Delta E_{g,E}$), resulting in a current gain decreases for lower temperatures (T) [15]. As for the base resistance, the freeze-out of carriers causes an increase in the base resistance. One way to combat the high base resistance is an increased base doping concentration (N_B) which would allow for lower resistance, however, it would also lower the current gain of the BJT, which is much less preferred in analog designs.



(a) Current gain [13]



(b) Zero-bias intrinsic base sheet resistance [13]

Figure 2.1: Performance degradation with decreasing temperature of Si BJT and SiGe HBTs in an epitexial bipolar technology

2.2. Cryogenic performance of HBTs

Due to the realization of the poor cryogenic performance of the homogeneous bipolar transistor, the research interest has shifted towards the heterojunction bipolar transistors (HBT) and their use of band gap engineering. Several materials can be implanted in the base to create the heterojunction, but the most popular is the implantation of Germanium (Ge) and thus, this thesis will focus on the Silicon Germanium (SiGe) HBT and its cryogenic characteristics.

In the SiGe HBT, the base region is induced with a graded profile of Germanium, which has different bandgap energy than silicon (Ge = 0.66 eV, Si = 1.11 eV at 300 K). A comparison of the BJT and the SiGe HBT band-diagrams is represented in figure 2.2, with a graded Ge profile below. As the Ge concentration increases, the bandgap energy of the base decreases which is represented by the gradient in the conduction band E_C. The energy decrease is mainly seen in the conduction band due to the similar electron affinity of the two semiconductor materials. This hinders the reverse injection of holes from base to the emitter in the valance band (E_V) which consequently increases the injection efficiency of electrons in the emitter-base region effectively increasing the current gain as well as allowing for more leniency towards changes in the doping concentration to improve other factors such as base resistance, noise figure and frequency behavior [16].

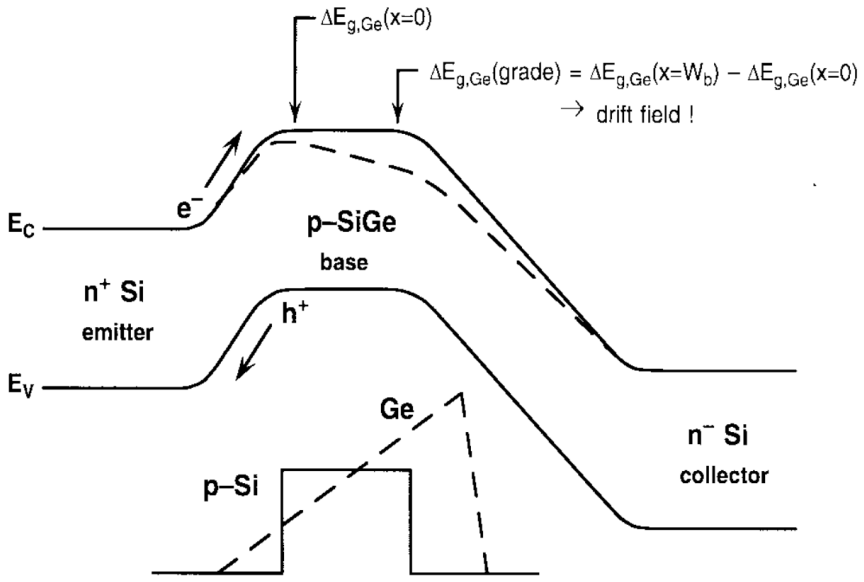
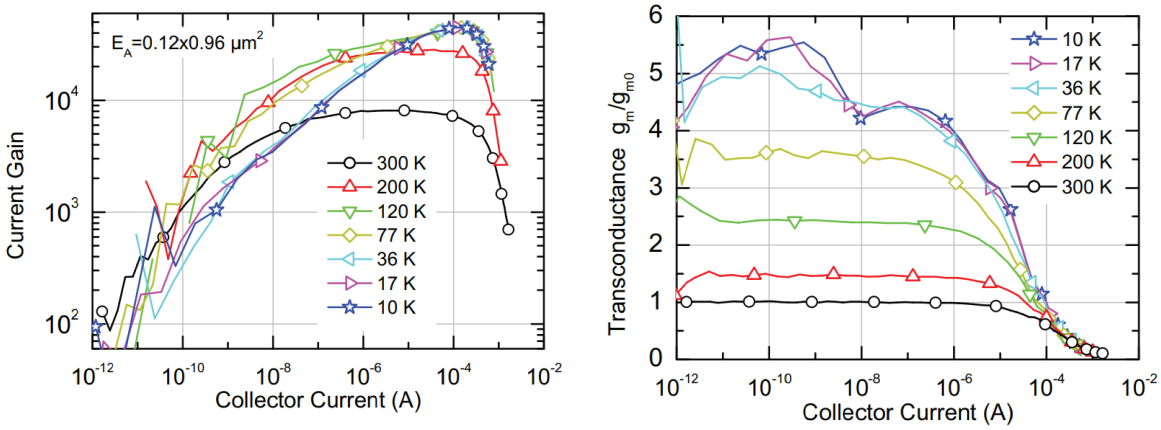


Figure 2.2: Band-diagram comparison of a BJT and a SiGe HBT with a graded Ge profile below [17]

Following up on the calculations performed in section 2.1 (eq. 2.3), the temperature dependence of the current gain can be changed by introducing a different material with different bandgap energy. The performance increase of the SiGe HBT at cryogenic temperatures comes from the bandgap energy difference in the Ge material. With the added bandgap energy of the Ge in the base region, $\Delta E_{g,B} - \Delta E_{g,E}$ starts to approach zero and can even become $\Delta E_{g,B} - \Delta E_{g,E}$ positive, thus inverting the temperature dependence of the current gain as compared to the BJT temperature dependence. Therefore, the SiGe HBT can show increased current gain when cooled down to cryogenic temperatures.

$$\beta_{DC} \approx exp\left(\frac{q \cdot \left((E_{g,B_{SiGe}} - E_{g,E_{Si}}) + (\Delta E_{g,B_{SiGe}} - \Delta E_{g,E_{Si}})\right)}{k \cdot T}\right) \tag{2.4}$$

These improvements have been reported in literature [18] [19], and are represented in figure 2.3 where a saturation of both the current gain and the transconductance appears for temepratures below 36 K. It should also be noted that the performance of the SiGe HBTs, in the same BiCMOS technology that is characterized in this thesis, was reported in [20] after measurements were performed for this thesis.



(a) Current gain [21]

(b) Transconductance, g_m = measurement temperature, g_{m0} = 300 K [21]

Figure 2.3: Performance saturation, due to temperature, in the current gain and transconductance of a SiGe HBT in a BiCMOS technology

In the Gummel characteristics of a SiGe HBT measured over various temperatures (fig. 2.4), the collector and base currents slope increase and saturate at 36 K. This represents the shift from conventional drift-diffusion transport mechanism towards a tunneling based mechanism, where at cryogenic temperatures electrons can tunnel from the emitter to the collector through the base [22].

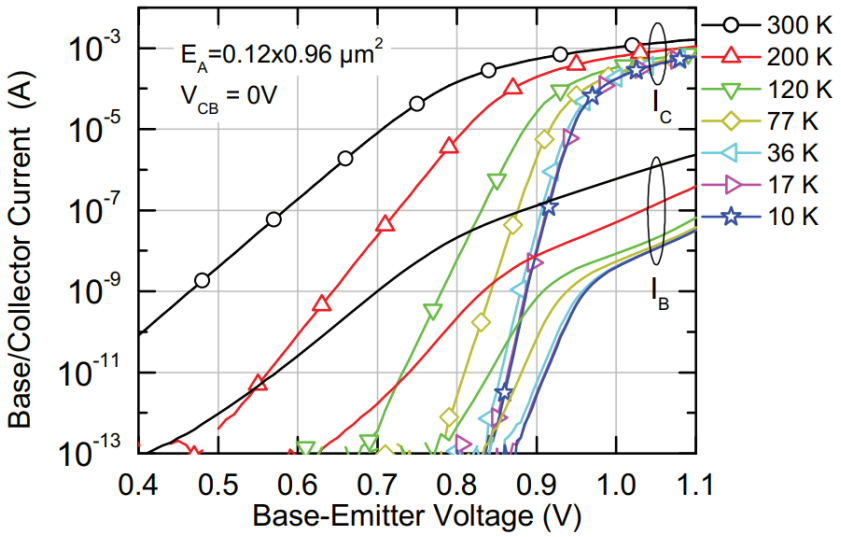
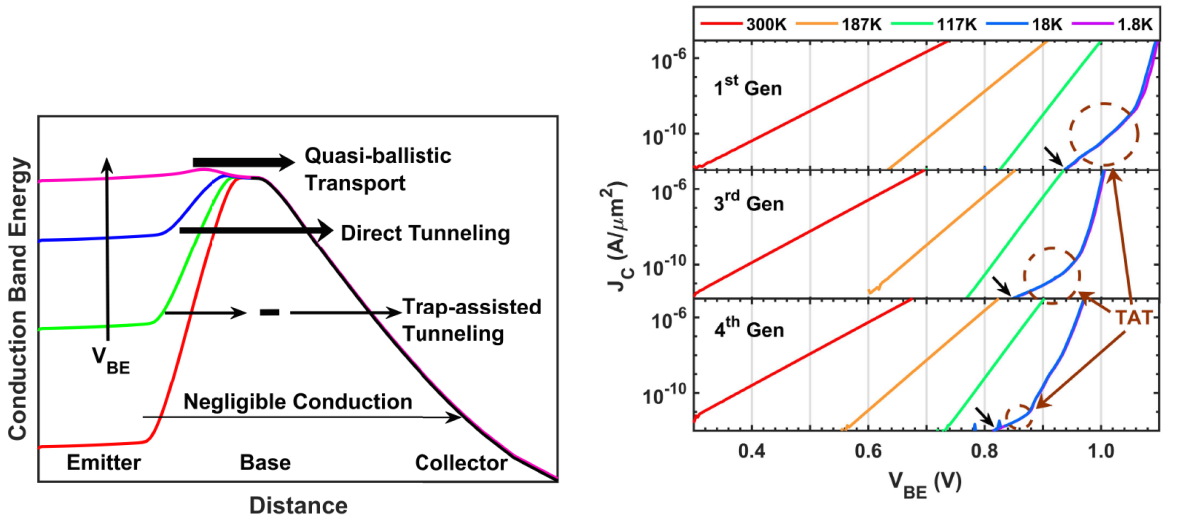


Figure 2.4: Gummel characteristics of a SiGe HBT down to cryogenic temperatures [21]

Three transport mechanisms are reported to exist at cryogenic temperature: quasi-ballistic transport [23], trap-assisted-tunneling (TAT) [24], and direct tunneling [18], [25] (fig. 2.5a), with the trap-assisted-tunneling being more prevalent in older generations and the quasi-ballistic transport dominating at currents above 10 nA/μm^2 (fig. 2.5b).



(a) Representation of transport mechanisms at various V_{BE} [22]

(b) Collector current of 3 generations of HBTs showing deviation caused by TAT [22]

Figure 2.5: Analysis of transport mechanisms in SiGe HBTs at cryogenic temperatures

Another anomaly observed in literature is a non-ideal step effect (bump in fig. 2.6) in the base current characteristics at cryogenic temperatures. The effect is observed in a newer generation of 90 nm SiGe HBT, and can significantly change the current gain in low power applications. Further investigation of the bump, by magnetic field exposure, showed that the cause of this bump is due to discrete trap levels.

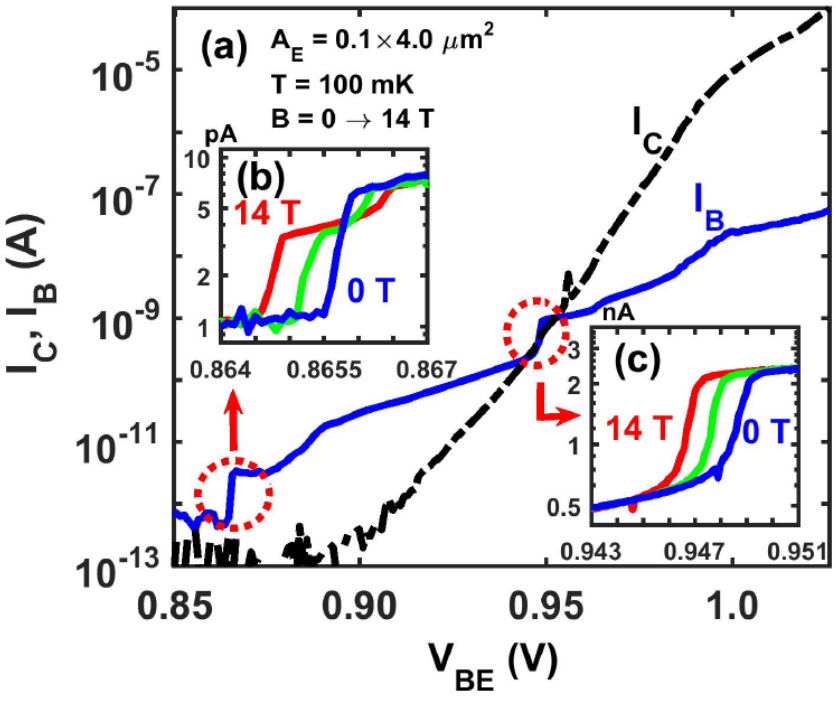
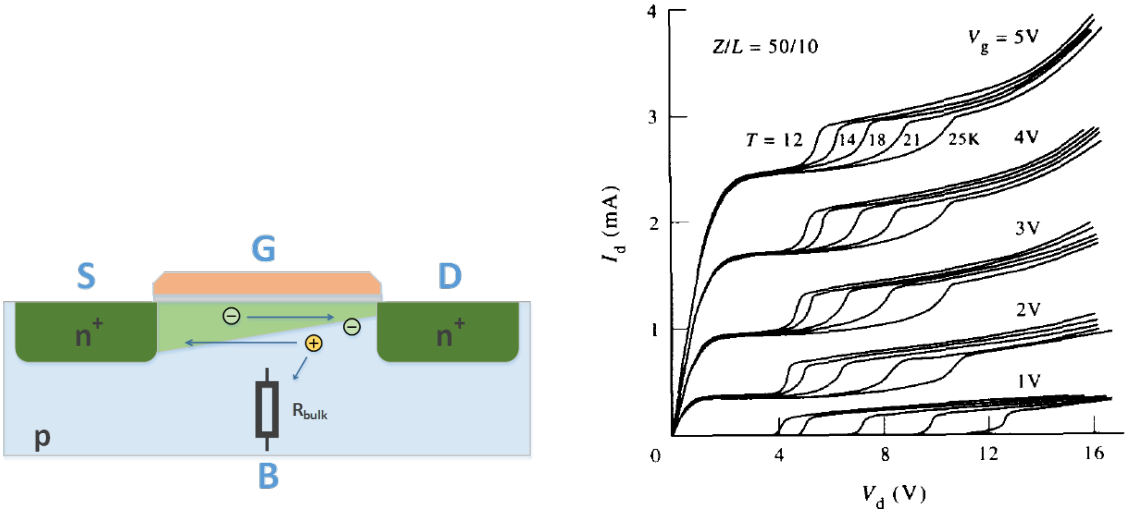


Figure 2.6: A non-ideal step in the base current of a SiGe HBT [18]

2.3. Cryogenic performance of MOSFETs

2.3.1. Kink effect

Among the most prominent cryogenic effects in MOSFET devices is the kink effect. This is described as a drain current increase in the output characteristics at high drain-source voltages. This effect is mainly visible in large devices as well as older technologies. The cause of this effect is the self-polarization of the bulk as majority carriers, generated by impact ionization near the drain, flow into the frozen-out bulk. The change in the bulk bias influences the threshold voltage which allows for more current to flow from source to drain, hence the increase in the drain current at higher drain-source voltages [26].



(a) The cross section of bulk NMOS

(b) The output characteristics at various cryogenic temperatures [27]

Figure 2.7: The kink effect in MOSFET devices

2.3.2. Electron mobility

The electron mobility is dependent on scattering effect and drift mechanisms, where the temperature dependence is mainly contributed by the scattering effects. At temperatures above 100 K, the scattering effect is dominated by acoustic, and intervalley phonon scattering, below 100 K the scattering is mainly contributed by ionized impurities in the bulk and interface charges in the silicon-oxide interface [28]. The increased mobility in bulk silicon over temperature can be seen in figure 2.8.

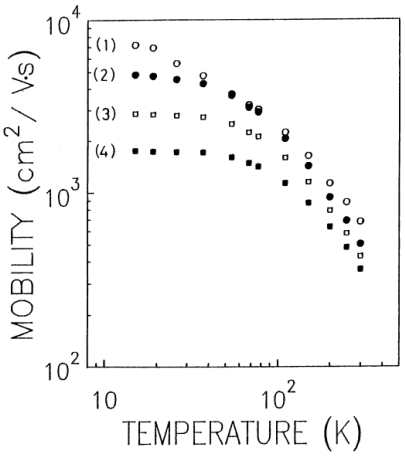


Figure 2.8: Electron mobility over temperature, (1) $N_s = 1 \cdot 10^{12} cm^2$, (2) $N_s = 3 \cdot 10^{12} cm^2$, (3) $N_s = 5 \cdot 10^{12} cm^2$, (4) $N_s = 7 \cdot 10^{12} cm^2$. [28]

2.3.3. Threshold voltage

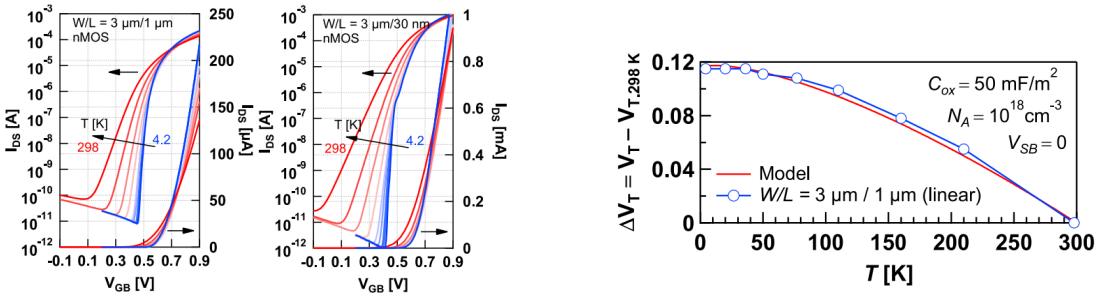
The temperature dependence of the threshold voltage leads to an increase in threshold voltage of roughly $\Delta V_T \approx 100$ - 200 mV at cryogenic temperature (fig. 2.9b). The threshold voltage of an NMOS transistor can be described by the following equation:

$$V_{T,NMOS} = \frac{|Q_{SD} - Q_{SS}|}{C_{ox}} + \phi_m - \chi_{Si} - \frac{E_g}{2} + \phi_{fp} \tag{2.5}$$

Where Q_{SD} is the charge in the depletion region, Q_{SS} is the fixed charge in the silicon-oxide interface, C_{ox} is the oxide capacitance, ϕ_m is the metal work function, χ_{Si} is the silicon work function, E_g is the band gap energy of the semiconductor, and ϕ_{fp} is the energy difference between the intrinsic Fermi level (E_{Fi}) and the Fermi level (E_F). ϕ_{fp} is the main contributor to the temperature dependence of the threshold voltage, which can be described by the following equation:

$$\phi_{fp} = \frac{kT}{q} \cdot ln\left(\frac{N_a}{n_i}\right) \tag{2.6}$$

Where k is the Boltzman constant, T is the temperature, q is the charge of an electron, n_i is the intrinsic carrier concentration and $N_{d/a}$ is the acceptor concentration in the p-type bulk.



(a) Transfer characteristics at various temperatures [29]

(b) Threshold voltage over temperature [29]

Figure 2.9: Threshold voltage change at cryogenic temperatures

2.3.4. Hysteresis

Hysteresis effect can be observed mostly in larger devices at cryogenic temperatures. The effect is noticeable in the output characteristics of the device where the forward-swept current does not follow the reverse swept current (fig. 2.10). This is due to the slow release time of electrons that are trapped in the impurity atoms in the channel of the transistor [30].

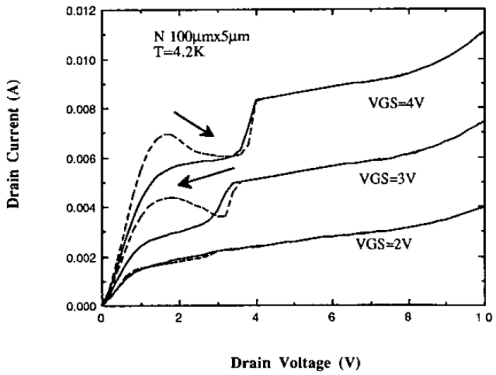
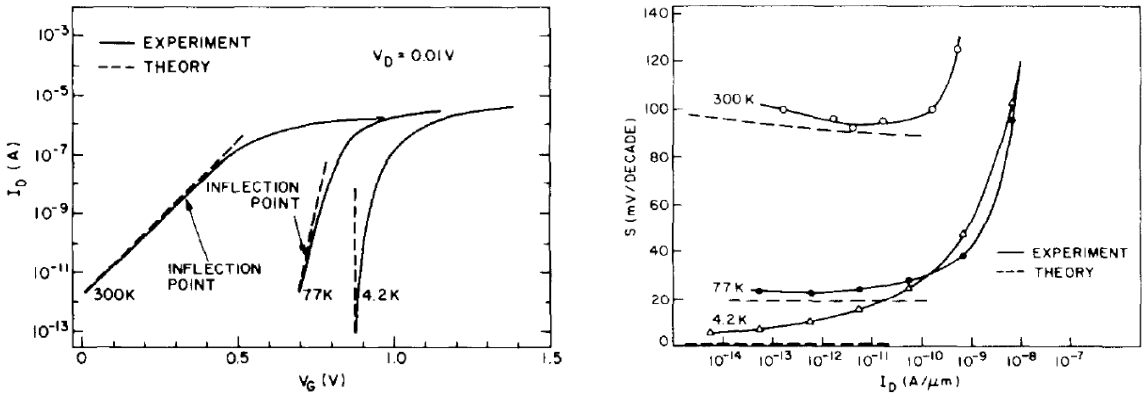


Figure 2.10: Hysteresis effect in MOSFETs at cryogenic temperature [31]

2.3.5. Subthreshold slope

In figure 2.11a, the subthreshold slope is seen to increase with decreasing temperatures. This allows for a higher subthreshold swing, which is described as the gate voltage increase required for an increase of a decade (x10) in the drain current when biased below its threshold voltage (fig. 2.11b)



(a) Transfer characteristics on a logarithmic scale [32]

(b) Subthreshold swing over the normalized drain current [32]

Figure 2.11: Subthreshold slope behavior at cryogenic temperatures

The subthreshold swing is described with equation 2.7, which suggests a linear dependence on temperature (T). However, the dependence becomes non-linear below 77 K-temperatures which results in larger subthreshold swing than expected from equation 2.7 [32].

$$SS = ln(10) \cdot n\frac{kT}{q} \tag{2.7}$$

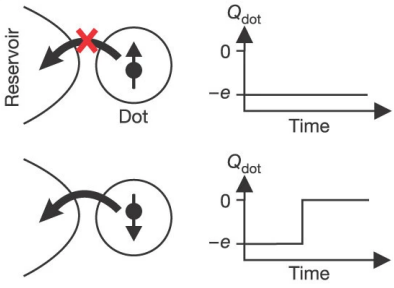
Where k is the Boltzman constant, T is the temperature, n is the non-ideality factor and q is the charge of an electron.

2.4. Spin qubits

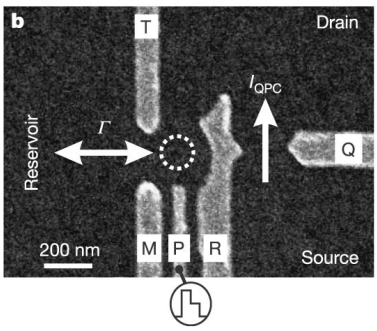
The spin qubit is considered to be one of the prominent candidates for the implementation of large-scale quantum computers, due to its scalability and ease of integration to conventional semiconductor circuits. Additionally, spin-qubits have the potential to operate at 1 K temperatures (Hot qubits) [33], [34], which would be instrumental to the development of scalable quantum computers. Spin qubits are controlled electrically and utilize the spin state of an electron to store information.

2.4.1. Spin-to-charge conversion

The spin state of an electron is difficult to detect directly, therefore it needs to be converted to charge. In figure 2.12a, the principle of a spin-to-charge conversion is demonstrated, where the charge of the quantum dot is affected by the spin state of the electron. When an electron with a spin ↑ state is in the quantum dot, it is not able to tunnel out of the dot and the charge remains the same, while a spin ↓ state allows the electron to tunnel out of the dot and further change the charge of the quantum dot. This charge can then be sensed by a nearby single-electron transistor or a quantum point contact (QPC), seen in figure 2.12b, e.g. by measuring the QPC current (I_{QPC}) variations due to any change in the charge of the dot due to an electron tunneling [7].



(a) Charge difference of the separate spin states [7]

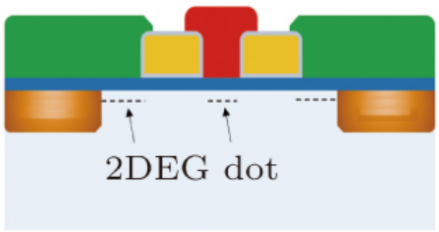


(b) Scanning electron micrograph of a quantum device [7]

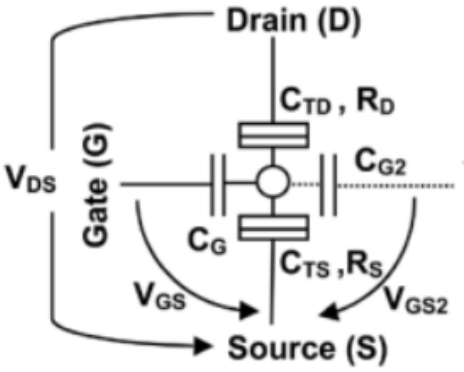
Figure 2.12: The principle of a spin-to-charge conversion

2.4.2. Single-electron transistor

The single-electron transistor (SET) is an extremely sensitive electrostatic sensor that uses the Coulomb blockade effect to allow for the sensing of a single or multiple electrons. The SET can confine electrons in a single dot, by forming 2-dimensional electron gas (2DEG) quantum dot in the substrate/oxide interface under the dots' respective gate. A schematic representation of a single dot SET can be seen in figure 2.13b, where the circle in the middle represents the quantum dot, the two rectangles above and below the dot represent the tunnel junctions on either side of the dot and the capacitor (C_G) represents the capacitive coupling to the control gate, often referred to as the plunger gate. An optional gate is also represented in this schematic on the right side of the dot (C_{G2}), for further manipulation of the dot. In figure 2.13a, a cross-section of a CMOS quantum dot can be seen. The SET has two ohmic contacts (orange) representing the drain and the source of the transistor. The SET has 3 gates which are placed on top of a silicon dioxide (SiO_2) layer, isolating the gates and the semiconductor substrate. The center gate (red) is the plunger gate which is used for controlling the charge potential of the dot. On either side of the plunger gate, are the barrier gates (yellow). The barrier gates control the barrier potential of the tunnel junctions which the electrons have to tunnel through [35], [36].



(a) Cross-sectional view of a single dot SET [35]



(b) Schematic representation [36]

Figure 2.13: The single-electron transistor

In order for electrons to be indivisually measured, two conditions must be met: First, the temperature needs to be low enough such that the electrons can not tunnel through the barriers due to their thermal energy. The energy needed to tunnel into the island is dependent on the charge coupling of the dot, described as $E_C = e^2/C$, where e is the charge of a single electron and C is the total capacitance of the dot. The thermal energy is determined as kT, where k is the Boltzmann constant and T is the temperature. In order for electrons to be measured discretely, $E_C = e^2/C >> kT$. Second, the tunneling resistance R_T of the barriers must be much larger than the quantum resistance of $h/e^2 = 25.8\ k\Omega$ to reduce the Heisenberg uncertainty relation $(e^2/C)R_TC > h$ and prevent unwanted tunneling due to low tunnelling resistance [37].

With the two aforementioned conditions being met, a quantum dot can be formed in the 2DEG under the plunger of the SET. Figure 2.14 shows the schematic diagrams of the electrochemical potential at two biasing conditions of the SET. The energy difference between the source and drain ($\mu_S - \mu_D$) represents a window in which the discrete electrons are able to tunnel in or out of the dot. The energy levels (μ_N) in the middle are the representation of the energy level of each electron in the dot. The levels are spaced out by the additional energy $E_{add} = E_C + \Delta E$, where E_C is the charging energy and ΔE is the energy spacing in between two discrete quantum levels. By manipulating the plunger gate potential V_G (increasing/decreasing the charge of the dot), the energy levels shift uniformly up or down and as an energy level shifts in between the drain-source energy levels, an electron is able to tunnel in or out of the dot [38]. Two important output characteristics of an SET

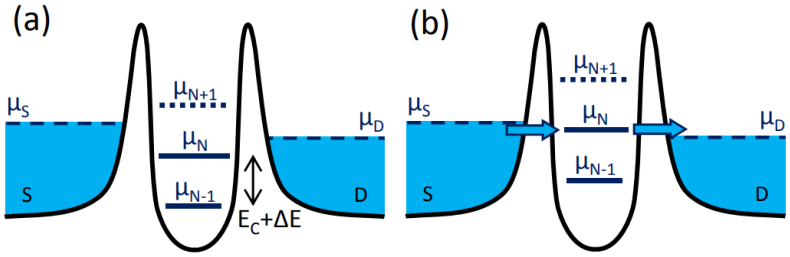
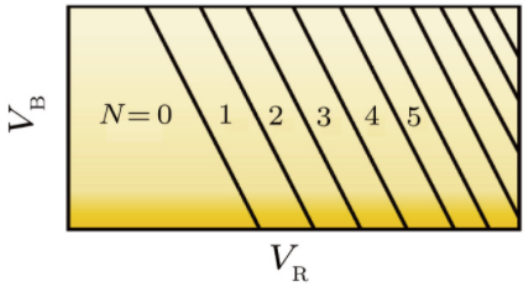
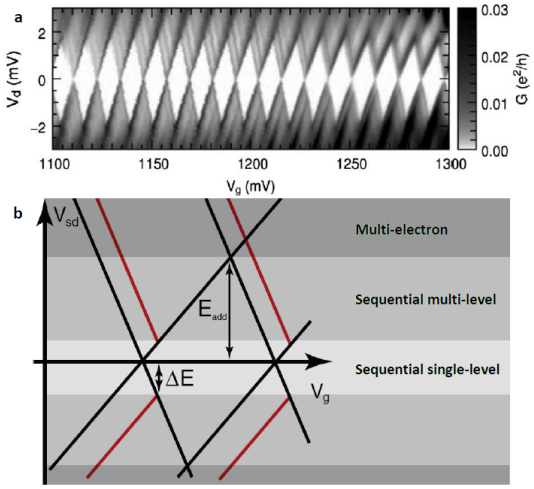


Figure 2.14: Schematic diagrams of the electrochemical potential in a single-electron transistor [38]

are the charge stability diagram and the coulomb diamonds. These diagrams vary between SETs, depending on the number of quantum dots that the SET is capable of forming (single dot in this case). The stability diagram (fig. 2.15a) shows the energy state of the dot in relation to the biasing conditions. The diagram can be attained by sweeping the plunger gate voltage and stepping the barrier gate voltage. By manipulating the plunger gate voltage (V_R) at a set barrier voltage (V_B), the energy levels (N) in the dot can be manipulated. The coulomb diamond plot (fig. 2.15b) is produced by sweeping the drain/source voltage and stepping the plunger voltage, the conductance is then plotted out at each measurement point. The charging energy (E_C) can be determined as roughly the height of the diamonds. Additionally, the balance between the two barrier gate can be determined by the slope of the diamond, a non-tilting diamond represents an equal barrier potential on both sides of the dot.



(a) Representation of a charge stability diagram of a spin-qubit [35]



(b) Coulomb diamonds, example from measurements (above) [39] and an explinantion of the different energy levels (below) [40]

Figure 2.15: Charge stability diagram and coulomb diamonds of a spin qubit

2.5. Spin qubit readout

There are several ways to readout spin qubits, however, this thesis will focus on the gate-based readout of spin qubits. The following sections describe several charge sensing methods including the Pauli spin blockade, energy selection (also known as Elzerman method), and Tunnel-rate selection, where the charge difference of the separate spin states is utilized. These spin-to-charge methods are followed by either a DC-based readout or an RF-based readout via an SET as the charge sensor.

2.5.1. Spin-to-charge conversion

Pauli-spin blockade

A common charge sensing method of spin qubits is based on the Pauli exclusion principle. The basis of this principle is that an orbital state of an atom can only be occupied by two electrons of different spin states. This is demonstrated in figure 2.16, using a double quantum dot with an electron of a known spin state (spin ↑ in this case) in the right dot and an electron of an unknown spin state in the left dot. In the case of a spin ↓ state of the unknown electron in the left dot, the electron is free to tunnel into the empty energy state in the right dot. However, in the case of a spin ↑ state of the unknown electron in the left dot, the electron is unable to tunnel into the right dot due to the Pauli spin blockade. Similarly, if the electron in the right dot has a spin ↓ state, only an electron with a spin ↑ state can tunnel into the empty state above it [41].

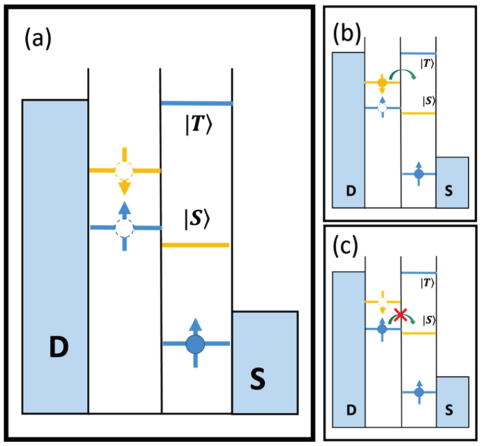


Figure 2.16: Schematic of the electrochemical potential describing the Pauli spin blockade [41]

Energy selective readout

Energy selective readout (E-RO), introduced in 2004 and also known as the Elzerman readout method, uses the difference in the energy states of the spin ↑ state and the spin ↓ state to distinguish the respective state of an electron. The readout consists of three steps, represented in figure 2.17a,b, where figure 2.17a represents the control signal and figure 2.17b represents the read-out signal: first, the dot is emptied of an electron, the second step involves injecting an electron into the dot with an unknown spin state, and finally, the third step involves reading out the spin state. These steps are controlled via the plunger gate and are then repeated for each measurement cycle.

Looking at figure 2.17c, the energy diagrams for both cases are shown. To empty the dot, the spin ↑ and spin ↓ are positioned above the reservoir μ_{res} by applying a voltage pulse on the plunger gate. Then the energy levels are brought below the reservoir and an electron is injected into the dot. With an electron of an unknown spin state in the dot, the energy level of the spin ↓ is brought up above the energy level of the reservoir while keeping the energy level of the spin ↑ below the energy level of the reservoir. If the electron has a spin ↓ state (upper energy diagrams), it is able to tunnel back into the reservoir and an electron with a spin ↑ can tunnel into the dot, resulting in a pulse-like signal (dotted line in fig. 2.17b) in the output signal of the read-out stage. If the electron has a spin ↑ state (lower energy diagrams), the electron remains in the dot during the read-out stage resulting in a flat output signal.

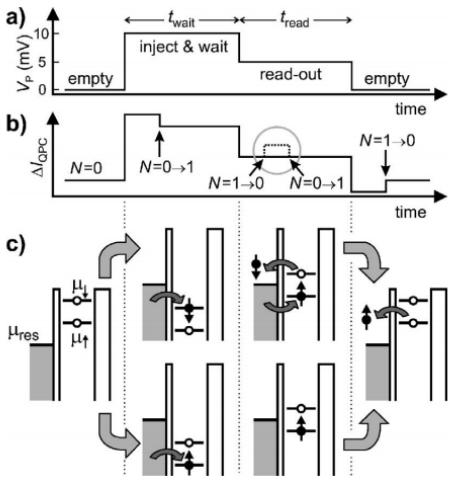


Figure 2.17: Schematic of the electrochemical potential describing the energy selective readout method [7]

Tunnel-rate selective readout

Tunnel-rate selective readout (TR-RO) uses the difference in the tunneling rate (Γ) of the different spin states, which can either be a spin-singlet ground state $|S\rangle$ or a spin-triplet state $|T\rangle$, where the tunneling rate from the triplet state (Γ_T) is much larger than the tunneling rate of the singlet state (Γ_S). Similar to the E-RO method, the stages are controlled by voltage pulses (fig. 2.18a) and the output signal from a QPC is measured (fig. 2.18b).

Referring to figure fig. 2.18c, the readout starts with an empty dot by raising both energy states above the energy level of the reservoir μ_{res}. Then both energy levels are pulled below the reservoir and an electron, with an unknown spin, tunnels into the dot which is then measured. In the wait stage, the electron is kept in the dot for a wait time of t_{wait}, where $\Gamma_S^{-1} >> t_{wait} >> \Gamma_T^{-1}$, is executed. During t_{wait} the electron with a tunnel-rate of the Γ_T state is much more likely to tunnel out of the dot and back into the reservoir. This would result in a flat output signal in the readout stage as there would be no electron in the dot during that stage. If an electron with a tunnel-rate of the Γ_S state, the electron would tunnel out of the dot after the wait time t_{wait} and during the readout stage, resulting in a step-like output signal shown in figure 2.18b [42].

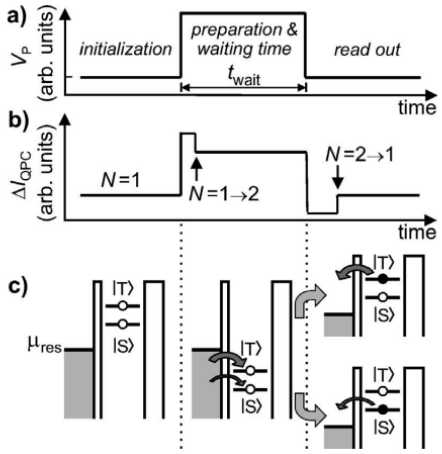


Figure 2.18: Schematic of the electrochemical potential describing the tunnel-rate selective readout method [42]

2.5.2. SET readout

DC readout

DC-based readout utilizes the conductance change in a charge sensing SET, which is coupled to the quantum dot, as electrons move in and out of the quantum dot. The current through the SET is then sensed via a transimpedence amplifier, placed at room temperature. The main limiting factor to a DC-based readout is the parasitic capacitance of the long interconnects between room temperature equipment and cryogenic components that severely limits the detection bandwidth of the system.

Radio-frequency reflectometry

Radio-frequency reflectometry readout (RF-RO) measures the change in the reflection coefficient as electrons tunnel in or out of the dot. The electron tunneling modulates the impedance of the SET, which changes the reflection coefficient in the transmission line, resulting in a change in the magnitude of the reflected wave. In figure 2.19, a simple resonant circuit can be seen for an RF-RO. The impedance of the SET is matched to a 50 Ω network composed of the parasitic capacitance and the impedance (L). An RF signal is generated via a signal generator which resides at room temperature. If the electron injected into the dot is in a spin ↑ state, the signal power is absorbed by the SET. If the electron injected into the dot is in a spin ↓ state, the electron tunnels out of the dot and change the impedance of the SET further resulting in an impedance mismatch to the matching network and a partial reflection of the signal power. [43], [44]

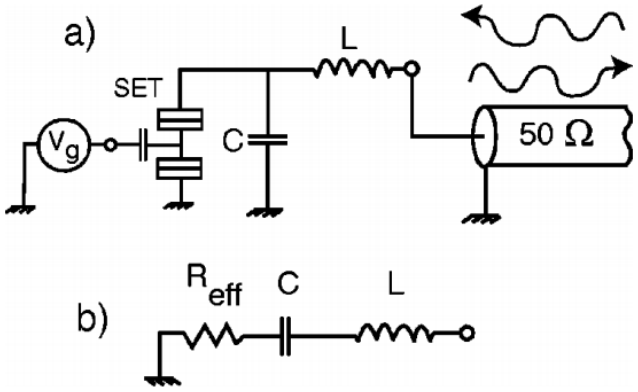


Figure 2.19: Model of the resonant circuit for radio frequency reflectometry [45]

3

Cryogenic characterization of the BiCMOS process

This chapter describes the comprehensive cryogenic DC characterization of the SG13G2 0.13μm BiCMOS technology. The main topic of this thesis is the cryogenic SiGe HBT amplifier to be used for pre-amplification of a single electron transistor and, consequently, the cryogenic characterization of the SiGe HBT is the first step of the project that will enable the circuit design. Although the focus of the thesis is to characterize the SiGe HBT at cryogenic temperature, it is of as much importance to characterize and validate the function of the MOSFET and the resistors at cryogenic temperatures, as this would allow for further development and integration of MOS devices and resistors with the SiGe devices with consequent full exploitation of the benefits of this BiCMOS technology. The samples chosen for the characterization consist of devices that already come with simulation models valid at room temperature, which is possible to compare with measurement data. Additionally, several experimental MOSFET and HBT devices, for which no simulation models are available, have been also characterized to compare with the standard devices. The chapter is split into three main sections: first, the characterization of the SiGe HBTs, second, the characterization of the MOSFET devices, and third, the characterization of the Resistors. The cryogenic effects and performance comparisons of the devices are discussed in their respective sections.

3.1. Silicon Germanium Heterojunction Bipolar Transistors

The technology under analysis is the IHP SG13G2 technology, a 0.13μM BiCMOS technology. This technology focuses on the high-speed capabilities of the SiGe HBTs. The transistor's intended use is in applications such as high-data-rate communications, high-resolution imaging, and radar. The HBT exhibits a maximum oscillating frequency f_{max} of 500GHz, transit frequencies f_T of 300GHz, breakdown voltages of BV_{CEO} = 1.6 V [46].

Three SiGe HBT devices are under investigation for this project:

- A transistor fabricated using the standard fabrication process of the SG13G2 technology, with 8 emitters in parallel and a pad layout for RF measurements henceforth referred to as RF structure HBT (GND-signal-GND pad layout in fig. 3.1).
- A transistor fabricated using a process modification of the SG13G2 technology with high beta and modified doping profiles, with 8 emitters in parallel and a pad layout for RF measurements, henceforth referred to as RF structure HBT (GND-signal-GND pad layout in fig. 3.1).
- A transistor fabricated using the standard fabrication process of the SG13G2 technology, with 1 emitter and a regular pad layout, henceforth referred to as DC structure HBT (Fig. 3.2).

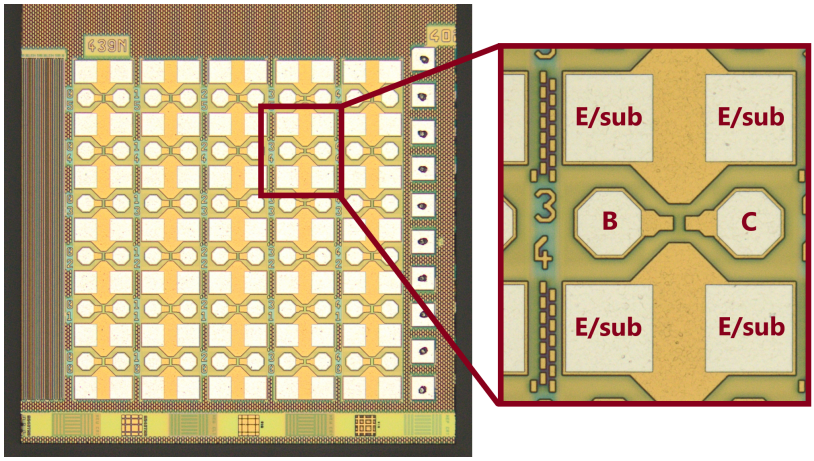


Figure 3.1: Micrograph of the RF structure HBT, ground-signal-ground pad layout

3.1.1. Measurement set-up

Both the standard and modified versions of the RF structures are glued on a copper plate using GE Varnish. The plate is then placed and firmly clamped down on the chuck of a CryoTech probe-station. A temperature sensor is also placed and firmly clamped down on the copper plate, close to the samples, for more accurate temperature readings. RF probes (GND-Signal-GND) are placed on the pads of the structure. The base is routed via coax cable to a bias-T and then to a Keithley 2636B Source Measurement Unit (SMU). The collector is routed to the SMU using a Triax cable and the emitter/substrate is connected to the chassis of the SMU via the shielding of the Triax and coax cables. 2 additional DC needles are connected to the emitter/substrate (E/sub pads in fig. 3.1) pads of surrounding structures for better grounding.

Measurements are performed at room temperature and later on, the samples are cooled down to cryogenic temperatures for further measurements. For measurements at cryogenic temperatures, the probe station is cooled down to liquid helium temperatures of 4.2 K. This means that the temperature of the chuck, inside the probe station, reaches 4.2 K. However, the thermal conductance through the chuck and the copper plate increases the temperature of the sample to about 15 K, which is measured by a separate temperature sensor that is placed close to the sample on the copper plate. Therefore, the temperature of the samples is assumed to be at 15 K. This however is of not much concern due to the low-temperature dependence of the HBTs performance at temperatures below 40 K [18].

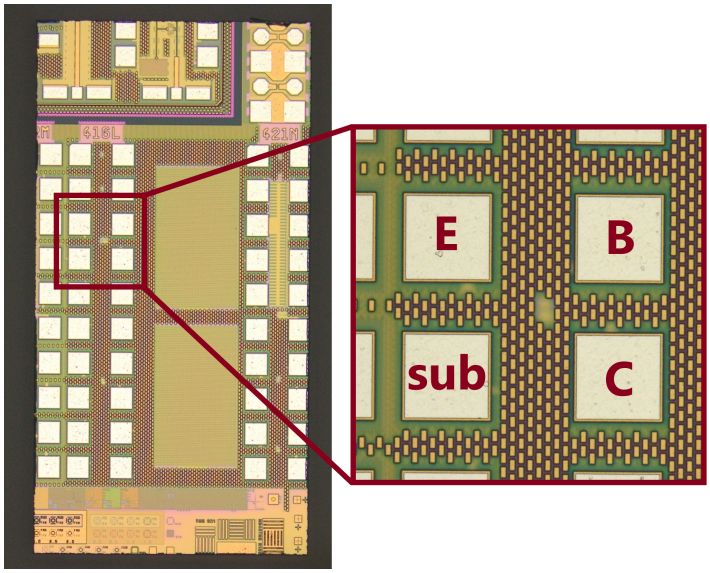


Figure 3.2: Micrograph of the DC structured HBT, regular pad layout

Due to the low intrinsic stability of the SiGe HBT at low frequencies, the HBTs were prone to self-oscillations [47] at higher currents and the full range measurements could not be performed in a dip-stick set-up. Measuring using a dip-stick would ensure a more stable temperature of the sample and would make the measurement process easier. However, the parasitics of the bond wires and the PCB traces, required in a dip-stick set-up, negatively effects the self-oscillating behaviour of the device resulting in the need for a probe-station measurements where ground-signal-ground probes are able to directly probe the bipolar device on the chip. Additionally, as stated before the HBT characteristic exhibits negligible change at temperatures below 40K, and therefore the 15K measurements performed in the probe station would be valid for designs at even lower temperatures. The HBT pads are probed with RF probes which lead to a bias-T and from there to the SMU for sourcing and measuring. A schematic of the measurement set-up can be seen in figure 3.3.

3.1.2. Measurement technique

Each SiGe HBT is measured in the common-emitter scheme over the range of interest. The Base-Emitter voltage is swept from 0.4 V to 1 V (300 K) and 0.8 V to 1 V (15 K) at a fixed Collector-Emitter voltage from 0 V to 1.5 V and the collector current and base current is measured. The step size of the Base-Emitter sweep is 7.5 mV and after each sweep, the Collector-Emitter voltage is raised by 10 mV. This results in a matrix of data (V_{BE}xV_{CE}: 200x200 @300K and 100 x 150 @15K) which is graphically displayed in the measurement results. A visual representation of the measurement scheme can be seen in figure 3.4. On the left image, the base-emitter voltage is swept from either 0.4 V or 0.8 V (blue arrow) to 1 V. Following each sweep, a 0.01 V step in the collector-emitter voltage (Orange dashed line) is made. This procedure is repeated until the collector-emitter voltage has reached its maximum value of 1.5 V. The results can then be plotted out in a colormap style figure (Right side), where the colors represent the magnitude of the measured collector or base current at each point of the measurements.

3.1.3. Measurement results

As expected from literature [21], the performance of the SiGe HBT shows improvements when cooled down to cryogenic temperatures. Full range measurements were performed on the NPN13G2 8 finger device in the standard and modified process technology. Figures 3.5 and 3.6 show the extracted characteristics of both devices in forward active mode (V_{CB} = 0V). This biasing point is chosen for further use in chapter 5. Both devices show an increase in peak current gain. In figure 3.5a, the V_{BE} operating range for unity current gain and above, shifts to higher voltages and becomes narrower as the transport mechanism shifts from drift/diffusion to tunneling [22]. This causes the current gain to decrease faster at lower currents as seen in figure 3.5b. The transconductance increases by a factor of x35 at 15 K temperature while the base input resistance (r_π) of both devices decreases due to the increased mobility at lower temperatures. Additionally in figures 3.7 and 3.8, the colormap of the current gain in both devices can be seen over the whole measurement range.

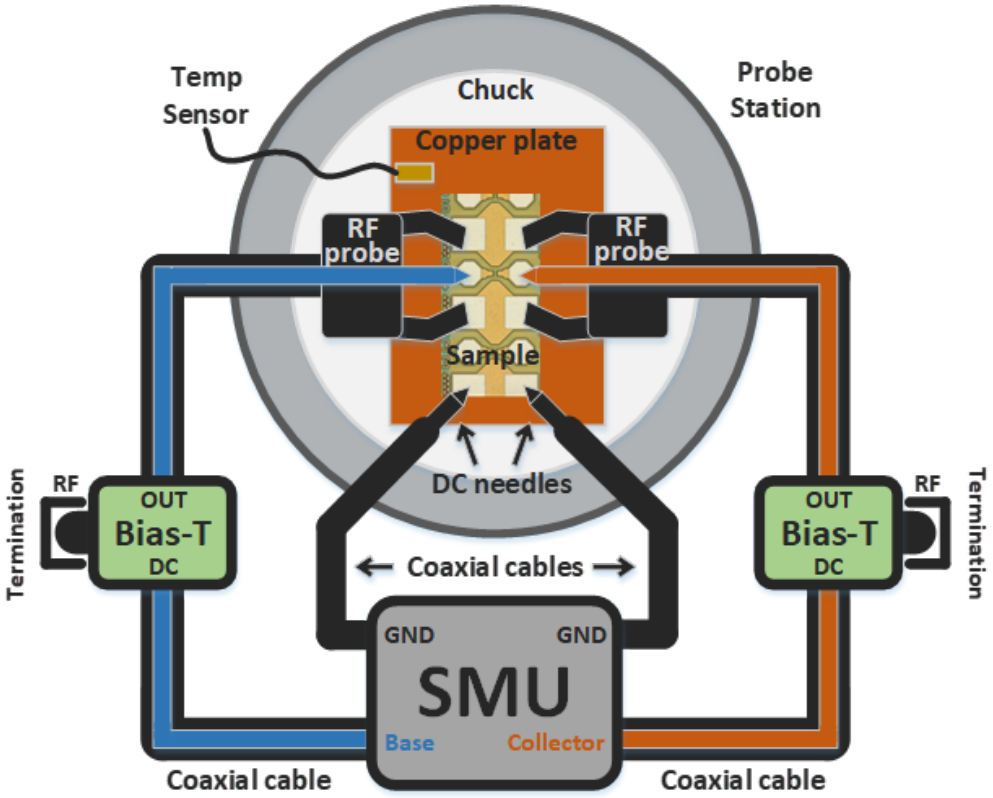


Figure 3.3: Schematic of the measurement set-up for HBT measurements in the probe station

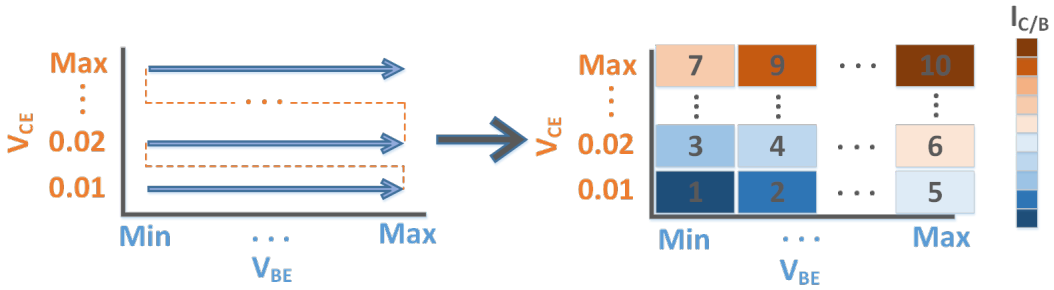
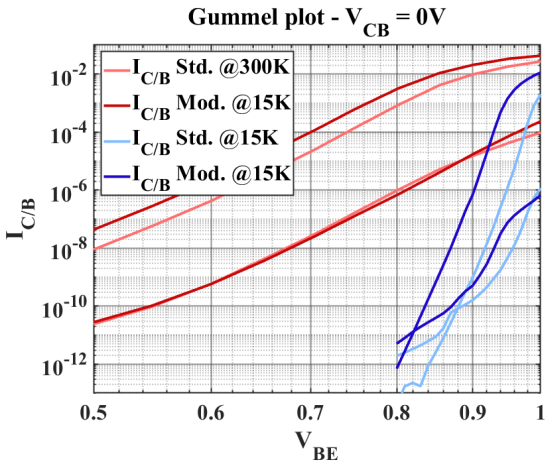
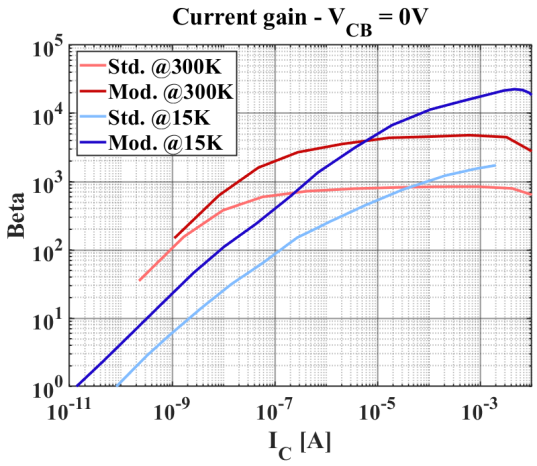


Figure 3.4: Measurement technique, the procedure (Left) and the resulting colormap (Right)

Looking at the low power performance of each device, the current gain is plotted over the dissipated power to view the achievable current gain for the lowest power dissipation (Fig. 3.9). The lowest achievable power dissipation, over the measurement range of V_{CE} = 0.4 - 1.5 V, V_{BE} = 0.4 - 1 V, is noted in the graph for the current gain of 10, 100, and 1000. Both HBTs show very high gain at low power making them very good candidates for ultra-low-power amplifiers at cryogenic temperatures. To verify the saturation of the devices as temperature decreases, both devices were measured in a dip-stick setup at multiple temperatures below 100 K. As mentioned in section 3.1.1, the self-oscillating nature of the HBT allowed for only low current measurements in the dip-stick set-up, therefore the dip-stick measurements are stopped before the devices start to oscillate. The resulting measurements of the collector and base currents for both the standard process and the modified process are displayed in figures 3.10 and 3.11. For additional reference at room temperature, the collector and base currents of the probe station measurements are also displayed with broken lines. It should be noted that the probe-station measurements display results from a different sample of the same HBT device. Both the collector and base characteristics of both devices start to saturate at around 40 K. This allows for reliable cryogenic characterization of SiGe HBT devices. Additionally, a bump can be seen in the base current of the modified HBT (Fig. 3.11b) which also translates to the bump in the current gain of the device (Fig. 3.12b).

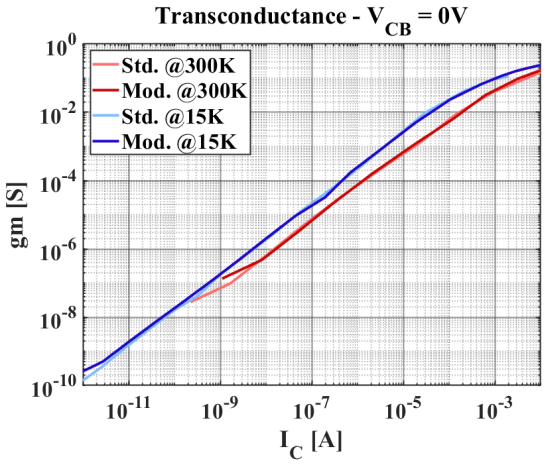


(a) Gummel characteristics

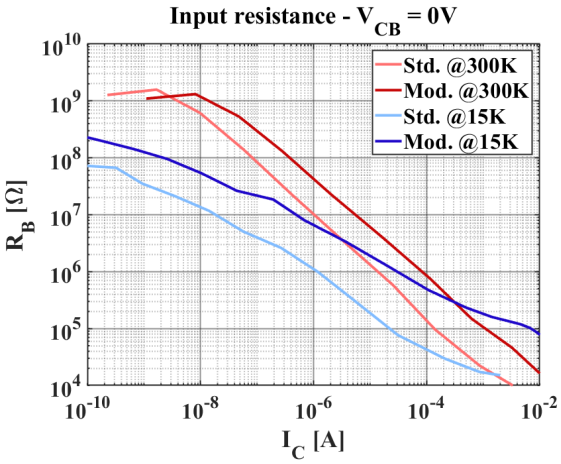


(b) Current gain over collector current

Figure 3.5: Gummel plot and current gain of the standard and modified HBTs



(a) Transconductance over collector current



(b) Input resistance over collector current

Figure 3.6: Transconductance and input resistance of the standard and modified HBTs

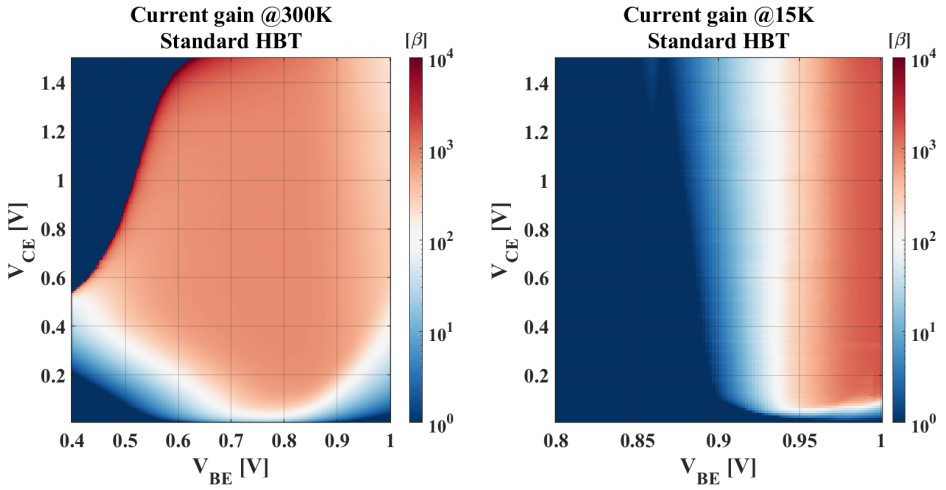


Figure 3.7: Current gain colormap of the standard HBT

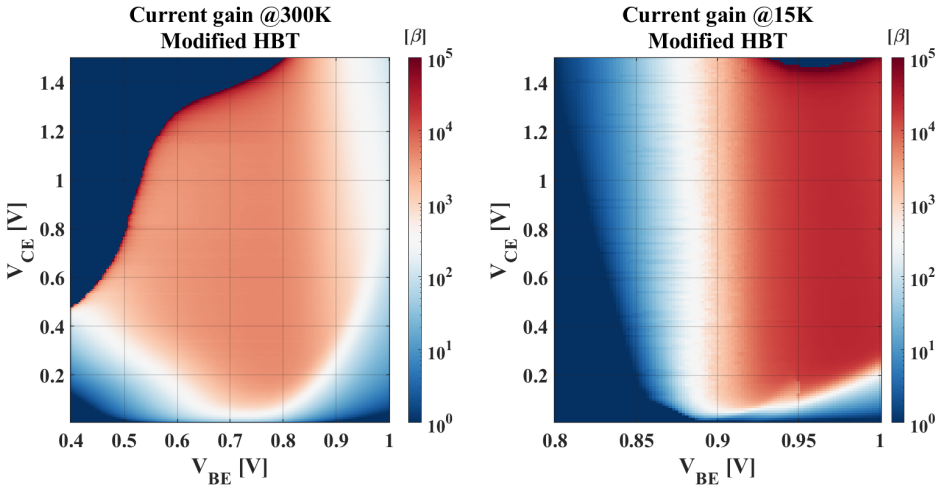


Figure 3.8: Current gain colormap of the modified HBT

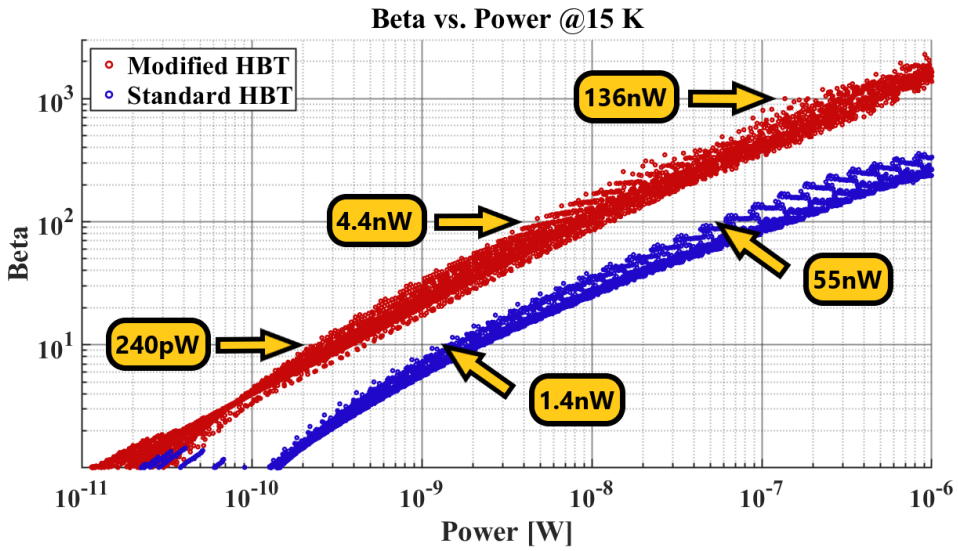
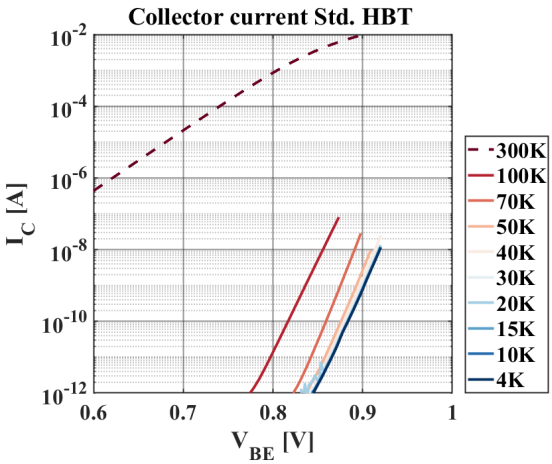
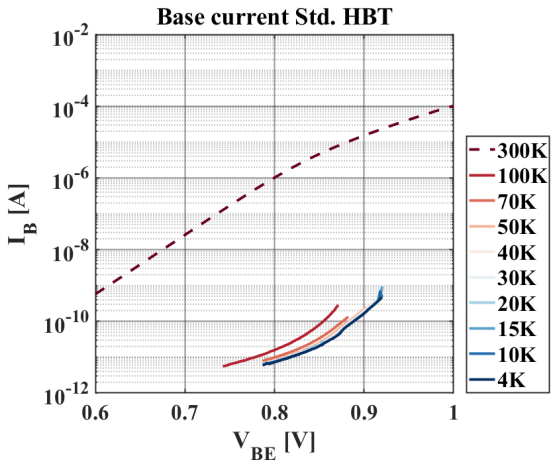


Figure 3.9: Current gain over dissipated power at cryogenic temperature, V_{CE} = 0.4 - 1.5 V, V_{BE} = 0.4 - 1 V

The bump in the base current of the modified HBT (Fig. 3.11b) can also be seen in the probe station measurements of the standard device figure (Fig. 3.5a, dark blue curve), indicating that it is present in some devices of the same structure. Additional low current measurements of 3 standard 8-finger HBTs in the dip-stick set-up were performed to check for repeatability. The resulting Gummel plot and the current gain are plotted in figure 3.13 and show this bump in only one of the devices (Sample 2) indicating that it does not show in all devices. A similar effect has been reported in literature and is discussed in section 2.2, which involves a high field tunneling event in the base-emitter region due to interface traps [18].

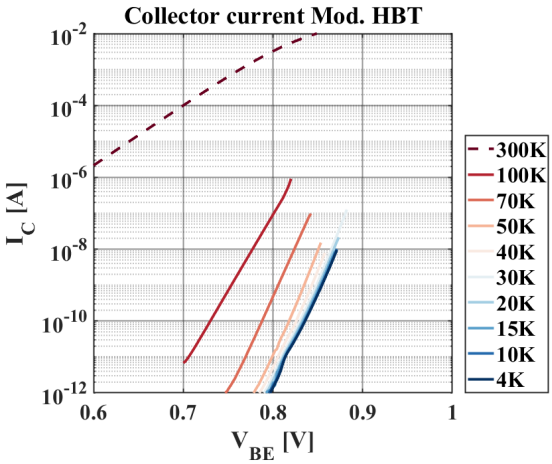


(a) Probe station (broken lines), dip-stick (solid lines)

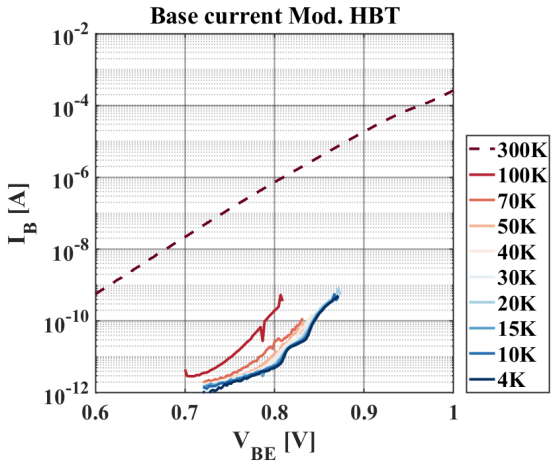


(b) Probe station (broken lines), dip-stick (solid lines)

Figure 3.10: Temperature dependence of the collector and base currents of the standard HBT, V_{CE} = 1 V

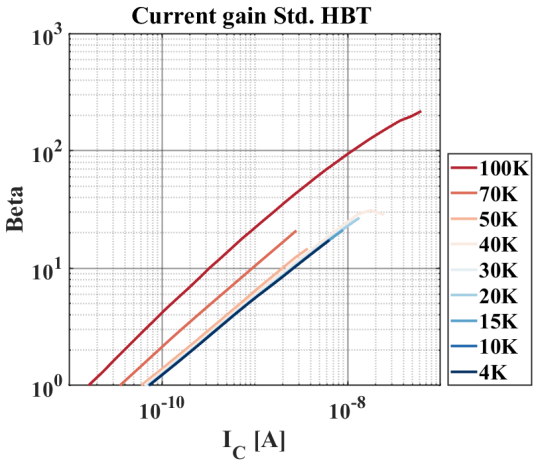


(a) Probe station (broken lines), dip-stick (solid lines)

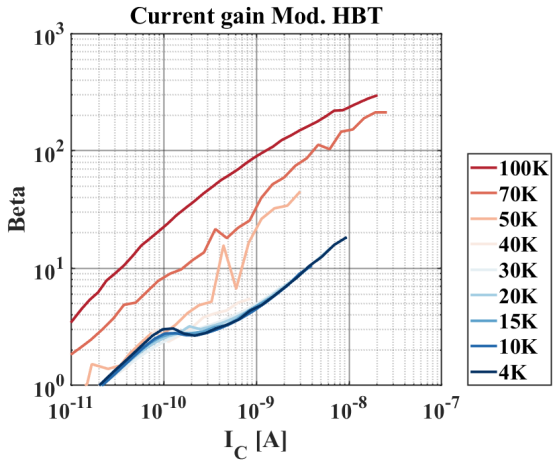


(b) Probe station (broken lines), dip-stick (solid lines)

Figure 3.11: Temperature dependence of the collector and base currents of the modified HBT, V_{CE} = 1 V

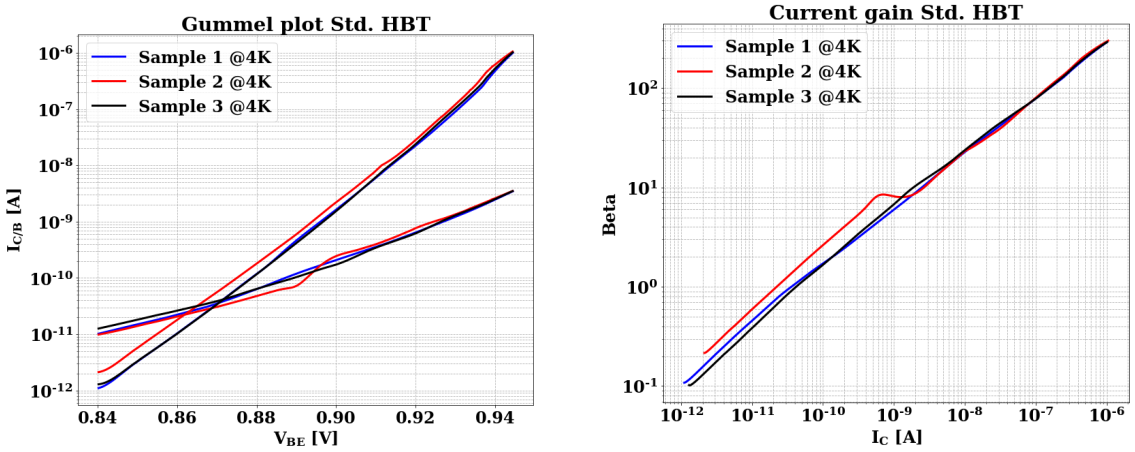


(a) Standard HBT



(b) Modified HBT

Figure 3.12: Current gain of the standard and modified HBTs over multiple temperatures

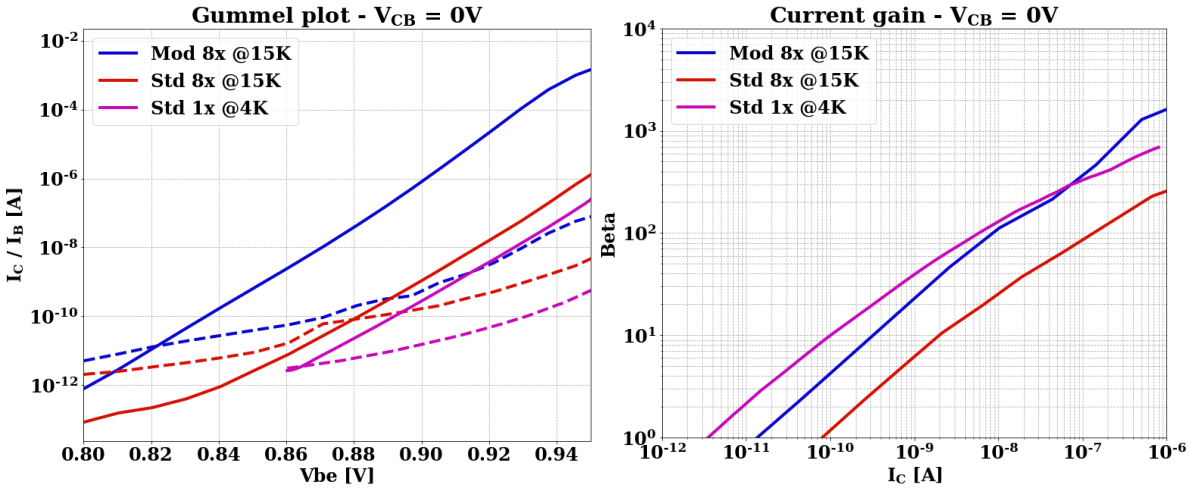


(a) Gummel plot

(b) Current gain

Figure 3.13: Gummel plot and current gain of several 8-finger standard HBTs

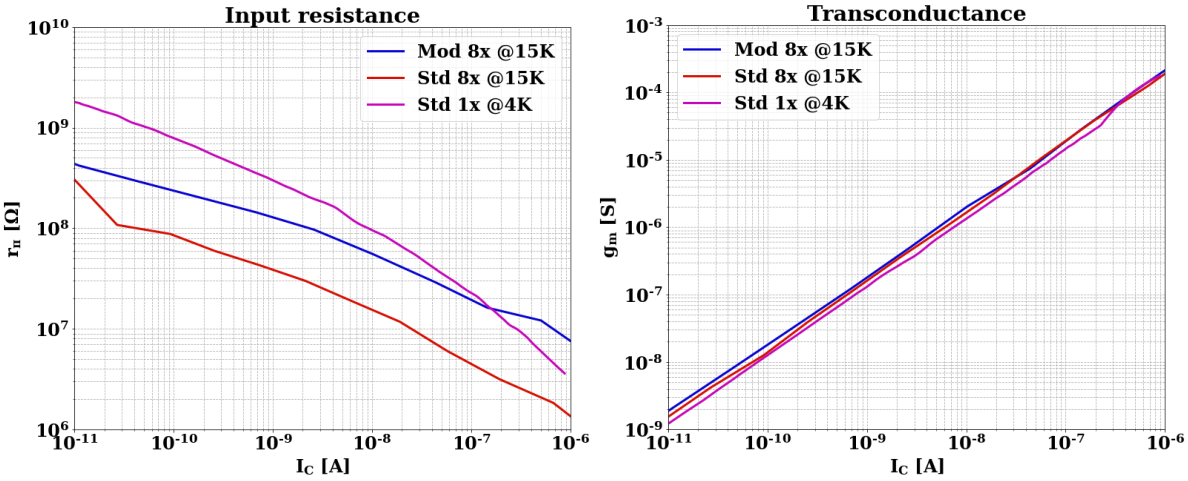
In the above results, the 1-finger DC structure HBT (Mentioned in section 3.1, fig. 3.2) in the standard process technology has not been mentioned. Due to time constraints, this device was only measured at $V_{CB} = 0$ V. The measurements were performed in the dip-stick set-up in the low current regime, which results in less current gain and furthermore no self-oscillations. Additionally, the dip-stick set-up allows for better thermalization. Every node of the transistor is wire-bonded to a PLCC package which is mounted onto a measurement PCB in the dip-stick and directly routed via Coax cables to the measurement equipment at room temperature. The 4 K measurement results of the 1-finger device can be seen in figure 3.14 along with the low current measurements from both 8-finger devices. The collector and base current (Fig. 3.14a) of the 1-finger device is 8 times lower than that of the standard 8-finger device and therefore has higher current gain (Fig. 3.14b) at lower power ($P \approx I_C$). Additionally, the input resistance (Fig. 3.15a) and the transconductance (Fig. 3.15b) is plotted over the collector current. The results show how the 1-finger device shows increased current gain at lower biasing currents, even compared to the HBTs in the modified process technology, and would be a really good candidate for a low power amplifier at cryogenic temperatures.



(a) Collector current (solid lines), Base current (broken lines)

(b)

Figure 3.14: Gummel plot and current gain of the three HBT devices at cryogenic temperature



(a) (b)

Figure 3.15: Input resistance and transconductance of the three HBT devices at cryogenic temperature

3.1.4. Small signal model

To conclude this section, a DC equivalent small signal model of the HBT is introduced, which will be used further for calculations concerning the amplifier in chapter 5. The model used is the simplified low frequency Hybrid-Pi model, seen in figure 3.16. Using the parameters from the measurements above (I_C, I_B, V_{BE}), the input resistance r_π (fig. 3.15a), the transconductance g_m (fig. 3.15b), and the current gain β (fig. 3.14b) can be calculated. The transconductance is the derivative of the collector current over the base/emitter voltage (Eq. 3.2) and the input resistance is the derivative of the base-emitter voltage over the base current (Eq. 3.1). The current gain (β) is defined as the difference between the collector current and the base current (Eq. 3.3) and can also be calculated using the aforementioned parameters (g_m and r_π). The relationship between the g_m and r_π becomes relevant in the amplifier design, where an additional resistance is imposed parallel to the base-emitter node, changing the extrinsic current gain of the amplifier.

$$r_\pi = \frac{dV_{BE}}{dI_B} \tag{3.1}$$

$$g_m = \frac{dI_C}{dV_{BE}} \tag{3.2}$$

$$\beta = \frac{I_C}{I_B} = g_m \cdot r_\pi \tag{3.3}$$

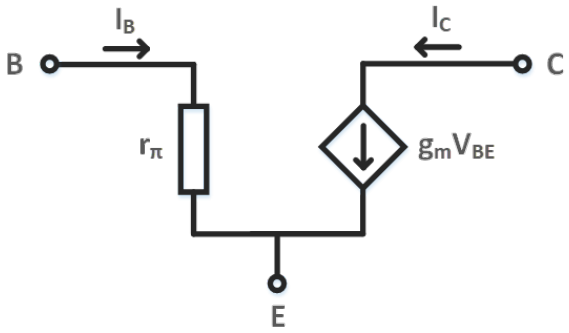


Figure 3.16: HBT small signal model

3.2. MOSFETs

The MOSFET samples come in 2 types of structures, denoted with segment numbers from S380 to S385M and from S540 to S541. The S380-S385M segments each contain six devices: four with corner aspect ratio; the remaining two are either intermediate-size devices or experimental devices (10/0.12μm) which reach beyond the technology length limit of 0.13μm. Those MOSFET segments consist of three segments of 1.2V logic CMOS thin-oxide MOSFETs 0.13-μm (S380, S381 and S382) and three segments of 3.3V I/O CMOS thick-oxide 0.33-μm MOSFETs (S383M, S384M, S385M). Each segment contains individual pads for drain, source, and gate connections of each device and share a single pad for the Bulk connection (Fig. 3.17). The gate dimensions of each device in the S380-S385M structure can be seen in tables 3.1 and 3.2.

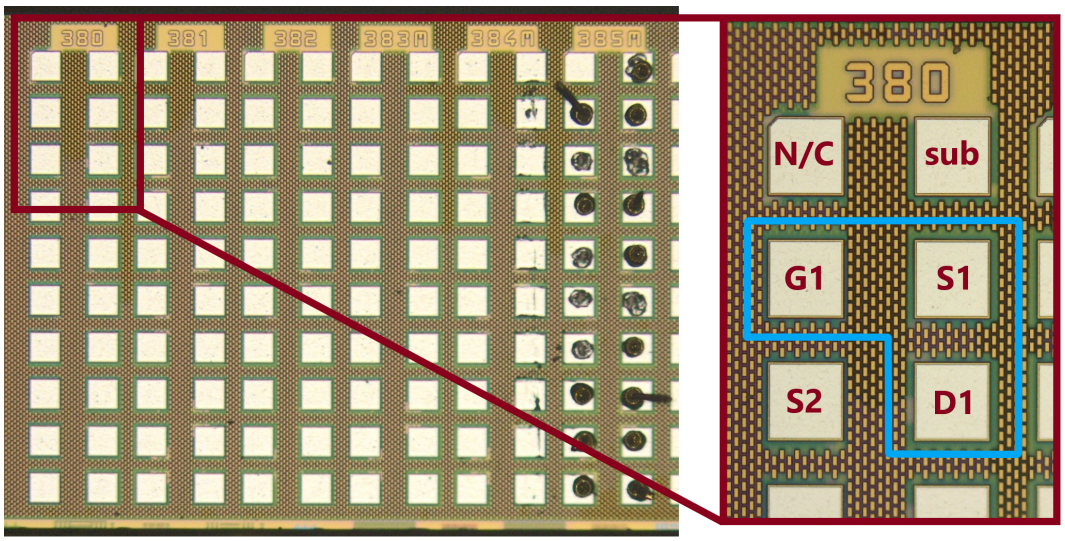


Figure 3.17: Micrograph of the S380-S385M MOSFET structure, close-up of a single device (blue area)

The S540-S541 segments each contain 5 thin-oxide NMOS devices of a fixed width of 10μm and varying lengths from 0.12 – 10μm. Those segments both consist of 1.2V logic CMOS thin-oxide 0.13-μm MOSFET segments. Segment S540 contains 5 devices with a fixed gate width of 10μm and gate length varying from 0.12 – 0.18μm. Segment S541 also contains 5 devices with a gate width of 10μm and a gate length variation of 0.5 – 10μm. Each segment contains individual pads for drain, source, gate, and substrate connections of each device (Fig. 3.18). The gate dimensions of each device in the S540 and S541 structure can be seen in table 3.1.

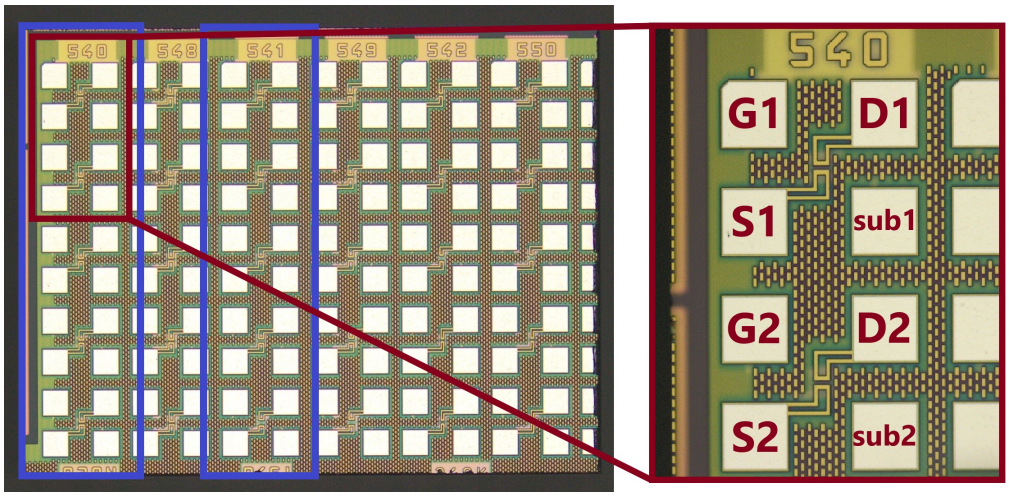


Figure 3.18: Micrograph of the S540 and S541 MOSFET structure, devices to be measured (blue area)

The denotations LS, SS, SL ,and LL will be used in the following paragraphs to describe the aspect ratios of the devices. The first letter indicates the width and the second letter indicates the length, where "L" stands for large and "S" for small, e.g. an LS device is a device with a large gate width and a small gate length.

W/L [μm]	**Thin oxide NMOS**	**Thin oxide NMOS**	**Thin oxide NMOS**	**Thin oxide iso. NMOS**	**Thin oxide PMOS**
Segm.	**S380**	**S540**	**S541**	**S381**	**S382**
DUT1	10/0.12*	10/0.12*	10/0.5	10/0.12*	10/0.12*
DUT2	10/0.13	10/0.13	10/1.2	10/0.13	10/0.13
DUT3	10/0.18	10/0.14	10/2	10/0.18	10/0.18
DUT4	0.15/0.13	10/0.15	10/5	0.15/0.13	0.15/0.13
DUT5	0.15/10	10/0.18	10/10	0.15/10	0.15/10
DUT6	10/10	-	-	10/10	10/10

Table 3.1: Gate dimensions of thin oxide MOSFET devices (* = experimental device)

W/L [μm]	**Thick oxide NMOS**	**Thick oxide NMOS**	**Thick oxide PMOS**
Segm.	**S383M**	**S384M**	**S385M**
DUT1	10/0.45	10/0.45	10/0.4
DUT2	10/0.33	10/0.33	10/0.33
DUT3	0.3/0.45	0.3/0.45	0.3/0.4
DUT4	0.3/0.33	0.3/0.33	0.3/0.33
DUT5	0.3/10	0.3/10	0.3/10
DUT6	10/10	10/10	10/10

Table 3.2: Gate dimensions of thick oxide MOSFET devices

3.2.1. Measurement set-up

Both room and cryogenic temperature measurements have been performed in a dip-stick set-up, using an SMU for sourcing and measuring. A schematic overview of the set-up can be seen in figure 3.19. An individual chip is used for each segment, each chip is bonded to an open PLCC package and the package is then mounted on a measurement PCB with a temperature diode mounted in a holder, above the sample. Mechanical relays are mounted on the measurement PCB in order to automate the measurement process of all devices on a single chip. Each relay gives access to the drain and gate of a single device for measurements while grounding the nodes of all other devices. The drain and gate are routed up to a connecting PCB (Top PCB) via coaxial cables and, from there, they are routed to the SMU via triaxial cables. The source of each device is grounded via the PCB ground plane.

The shield of the Triax cables connects to the frame of the dip-stick and the guard of the Triax cables connects to the shield of the Coax cables to allow for low leakage measurements down to the measurement PCB. The resistance of the Triax/Coax line from the measurement equipment to the Bottom PCB is measured to be 0.225Ω. This resistance may affect the measurement data, mainly the line resistance imposed on the source, which would alter the measured transconductance of the transistor ($Gm = gm/(1 + gm \cdot R_S)$. The effect of this parasitic resistance could be reduced with a 4-wire measurement scheme. However, the resistance introduces, at most, a roughly 0.2% error (max 10) in the measurements, which is low enough to avoid the complications of a 4-wire measurement scheme. Additionally, this error is reduced due to increased mobility in the copper leads at cryogenic temperatures [48].

On-chip, the substrate of all devices connect to a single pad which is routed directly to the Top PCB and from there to the SMU for further manipulation of the device under testing (DUT). For cryogenic measurements, the dip-stick is slowly lowered into a Dewar containing liquid helium, which has a melting point of 4.2 K. The device is lowered until the temperature sensor mounted above the device reads a temperature of 4.2 K indicating that the device is submerged in the liquid. Therefore, the cryogenic measurements are presumed to be at 4.2 K.

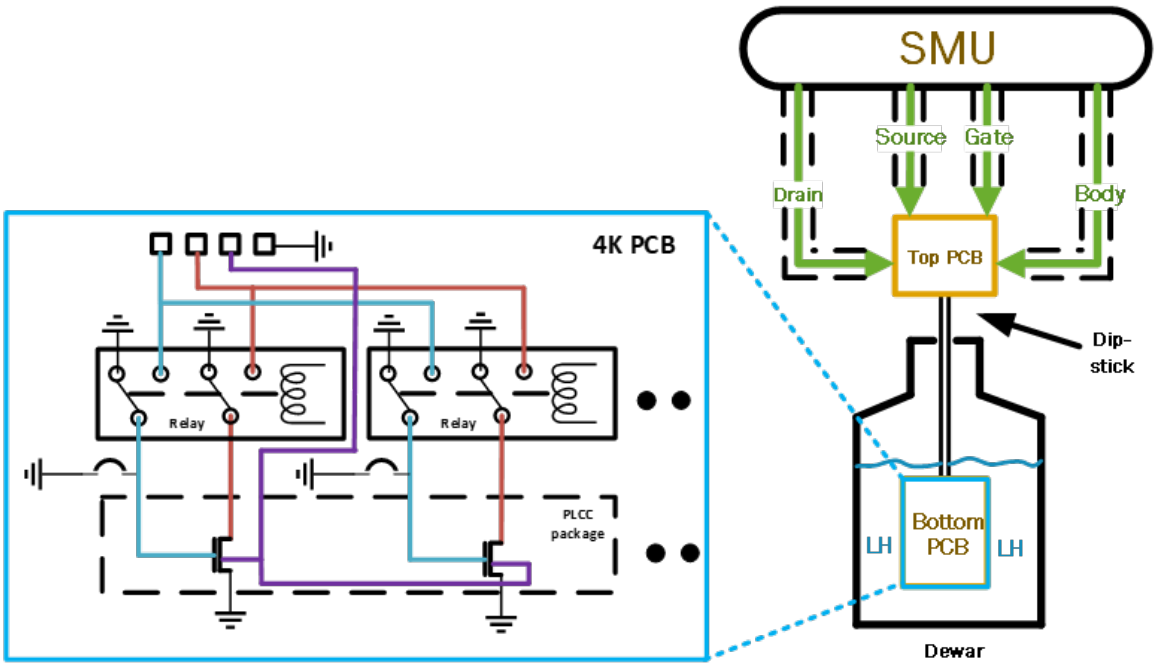


Figure 3.19: Measurement set-up for the dip-stick measurements of MOSFETs

3.2.2. Measurement technique

The measurements are performed in the common source scheme, with the source and substrate voltage at ground level and sweeping the gate-source voltage at a fixed drain-source voltage. The voltage sweep ranges from ±0.01 V - ±1.2 V for the thin oxide MOSFETs and ±0.01 V - ±3.3 V for the thick oxide MOSFETs, both with a voltage step size of 10 mV. The device characteristics throughout the whole voltage range is attained with a parametric sweep, where the gate voltage is swept over multiple drain-source voltages, resulting in a V_{GS} x V_{DS} data matrix which can be used for the extraction of both output (I_D/V_{DS}) and transfer (I_D/V_{GS}) characteristics as well as plotting out the complete characteristics in a single colormap style figure. A visual representation of the measurement scheme can be seen in figure 3.20. On the left, the gate-source voltage is swept from 0.01 V (blue arrow) to either 1.2 V or 3.3 V for thin and thick oxide NMOS, respectively. Following each sweep, a 0.01 V step in the drain-source voltage (Orange dashed line) is made. This procedure is repeated until the drain-source voltage has reached either 1.2 V or 3.3 V for thin and thick oxide NMOS, respectively. The same procedure is performed on the PMOS devices but the gate-source voltage sweeps and the the drain-source voltage steps are swept/stepped from -0.01 V to -1.2 V or -3.3 V. The results can then be plotted out in a colormap style figure (Right side), where the colors represent the magnitude of the measured drain current at each point of the measurements. Additional measurements of the output characteristics in thick oxide devices are performed at cryogenic temperature to measure for hysteresis. The hysteresis effect is measured by forward sweeping the V_{DS} from 0.01V to maximum voltage, followed by a reverse sweep down to 0.01V, this effect is further discussed in section 3.2.6.

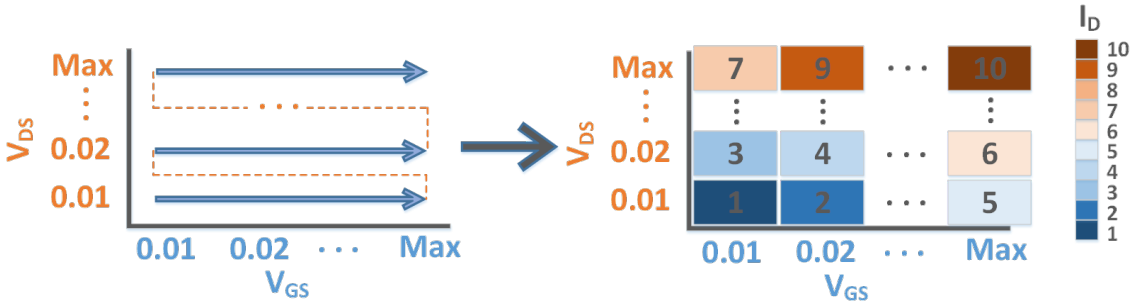


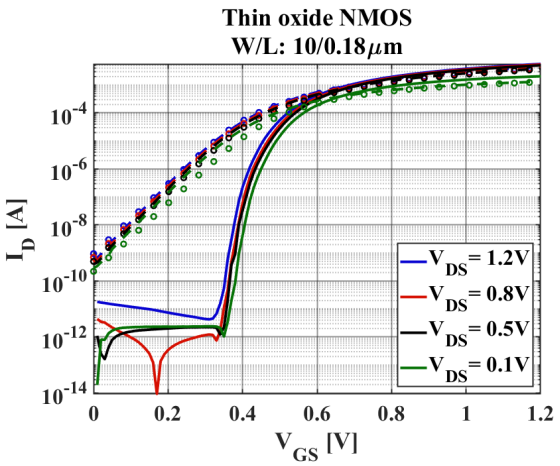
Figure 3.20: Measurement technique, the procedure (Left) and the resulting colormap (Right)

3.2.3. Measurement results

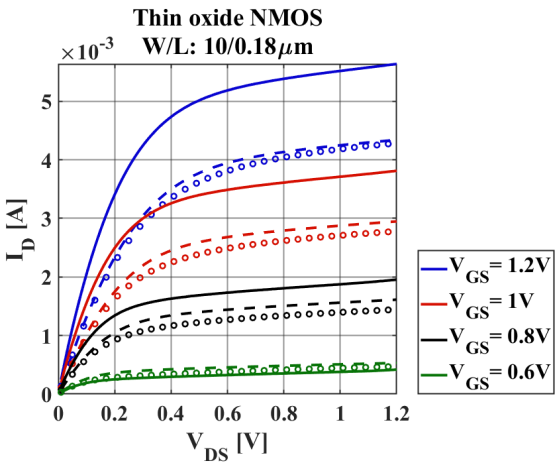
The output characteristics and the transfer characteristics of a few chosen devices can be seen in figures 3.21 - 3.24, as well as a colormap displaying the drain current for all measurement points (figure 3.25). The measurement results show the commonly observed characteristic changes at cryogenic temperature as reported in literature [49],[50], which comprise an increase in the drain current (I_D) due to the increase in carrier mobility at cryogenic temperatures. Additionally, these results show an increase in the subthreshold slope, as well as an increase in threshold voltage and a decrease in the output resistance.

Additional cryogenic effects (noted with yellow arrows) that can be observed in the following figures include:

- A kink in the output characteristics of thick oxide devices (Figures 3.23b and 3.24b), described in section 2.
- A hysteresis effect in the transfer characteristics, where a very sharp turn on slope of thick oxide devices at high V_{DS} (Figures 3.23a and 3.24a).
- Bumps occurring in the subthreshold region of thin and thick oxide devices (Figure 3.22a).

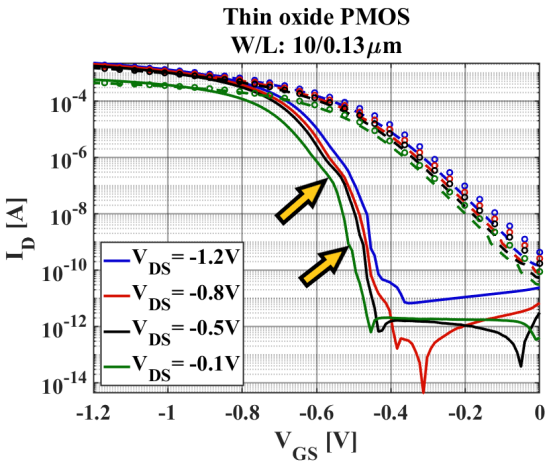


(a) RT (Broken lines), LH (Solid lines) and simulated (Circles)

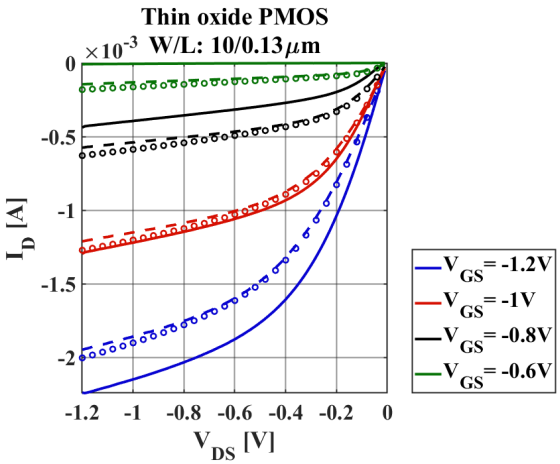


(b) RT (Broken lines), LH (Solid lines) and simulated (Circles)

Figure 3.21: Transfer and output characteristics of thin oxide NMOS device

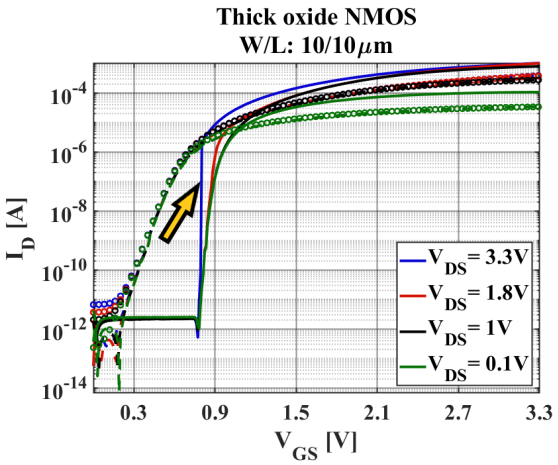


(a) RT (Broken lines), LH (Solid lines) and simulated (Circles)

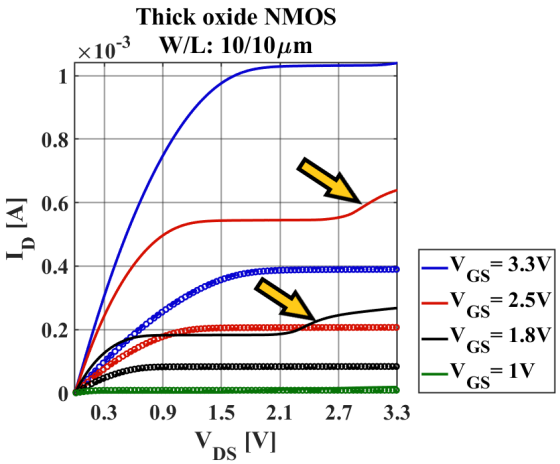


(b) RT (Broken lines), LH (Solid lines) and simulated (Circles)

Figure 3.22: Transfer and output characteristics of thin oxide PMOS device

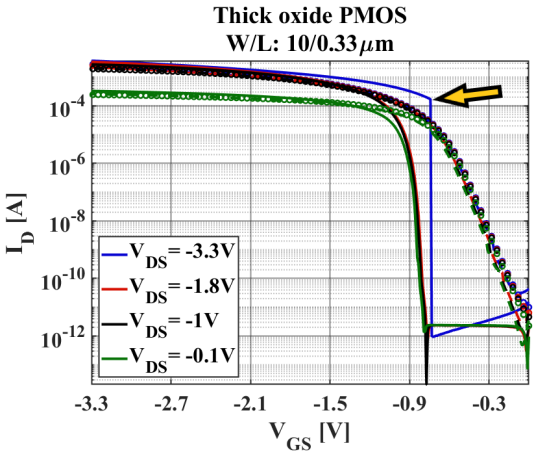


(a) RT (Broken lines), LH (Solid lines) and simulated (Circles)

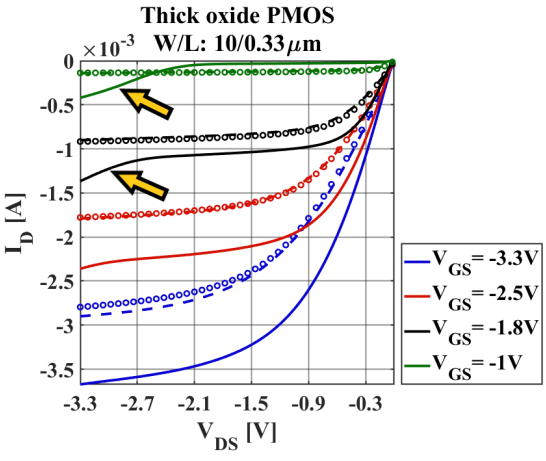


(b) RT (Broken lines), LH (Solid lines) and simulated (Circles)

Figure 3.23: Transfer and output characteristics of thick oxide NMOS device



(a) RT (Broken lines), LH (Solid lines) and simulated (Circles)



(b) RT (Broken lines), LH (Solid lines) and simulated (Circles)

Figure 3.24: Transfer and output characteristics of thick oxide PMOS device

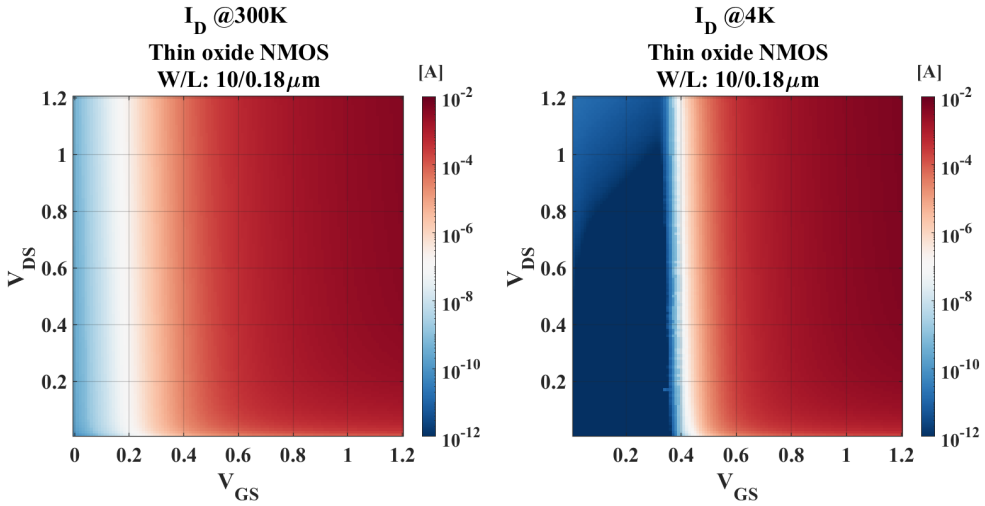


Figure 3.25: Drain current colormap of a thin oxide NMOS device at room temperature (left) and cryogenic temperature (right)

Additional NMOS measurements

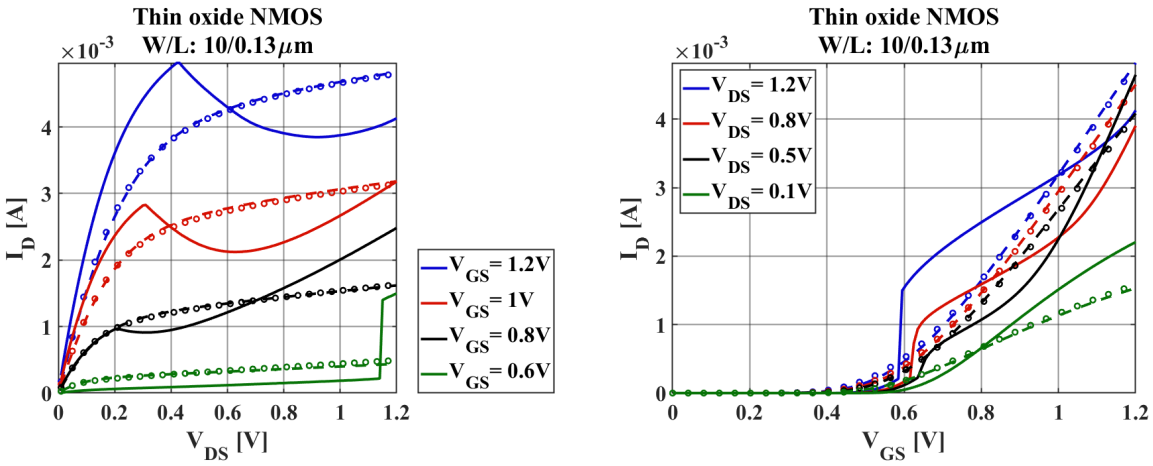
A recurring issue arose in LS devices (Red devices in table 3.3), where the I_D/V_{DS} characteristics follow simulation data at room temperature, but at 4K temperature, the device displays a sudden drop in the drain current in the output characteristics before gradually rising again, as seen in figure 3.26. Those devices were measured again to determine if hysteresis was at play, as well as manipulating the substrate voltage for a better understanding of the behavior. However, this behavior persisted and it has been attributed to damage from Electrostatic Discharge (ESD). Therefore, the decision was made to measure in a probe station setting to minimize the risk of damage that could be caused in the wire bonding process or by further handling.

W/L [μm]	**Thin oxide NMOS**	**Thin oxide NMOS iso.**	**Thin oxide PMOS**	**Thick oxide NMOS**	**Thick oxide NMOS iso.**	**Thick oxide NMOS**
Segm.	**S380**	**S381**	**S382**	**S383M**	**S384M**	**S385M**
DUT1	10/0.12*	10/0.12*	10/0.12*	10/0.45	10/0.45	10/0.4
DUT2	10/0.13	10/0.13	10/0.13	10/0.33	10/0.33	10/0.33
DUT3	10/0.18	10/0.18	10/0.18	0.3/0.45	0.3/0.45	0.3/0.4
DUT4	0.15/0.13	0.15/0.13	0.15/0.13	0.3/0.33	0.3/0.33	0.3/0.33
DUT5	0.15/10	0.15/10	0.15/10	0.3/10	0.3/10	0.3/10
DUT6	10/10	10/10	10/10	10/10	10/10	10/10

Table 3.3: List of MOSFET devices that exhibit abnormal behavior (Red), (* = experimental device)

Probe station set-up

Both room and cryogenic temperature measurements have been performed in a LakeShore cryogenic probe station. A single chip, containing both S540 and S541 segments has been glued to a copper plate using thermally conductive glue. The copper plate is placed on the chuck in the probe station and clamped down. A temperature diode is placed close to the chip and clamped down on the copper plate to more accurately monitor the temperature of the chip. Four DC needles are used as contact points to the Source/Drain/Gate/Substrate pads of each DUT and connected to an SMU via Triax cables for measurements. For cryogenic measurements, the probe station is depressurized with a vacuum pump and helium is allowed to flow into the probe station. Even though the temperature sensor of the chuck reads 4.2K, the temperature of the sample is still not guaranteed to be at 4.2K since it is not submerged in liquid helium and depends on the thermal conductivity from the chuck to the sample as well as the state of vacuum in the chamber and thermal leaks via the needles. Hence, the temperature diode has been placed beside the chip on the copper plate. When the temperature has settled, this diode reads a temperature of 15K while the chuck sensor reads 4.2K. Therefore, the cryogenic measurements in the probe station are presumed to be at a stable temperature of 15K. The measurement set-up can be seen in figure 3.27.



(a) Output characteristics

(b) Transfer characteristics

Figure 3.26: Output and transfer characteristics of an LS NMOS device showing abnormal behaviour at 4K temperature

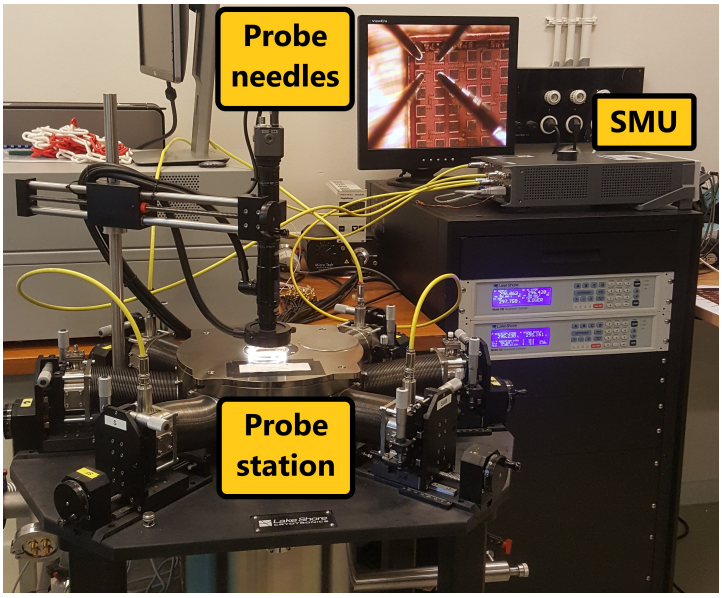
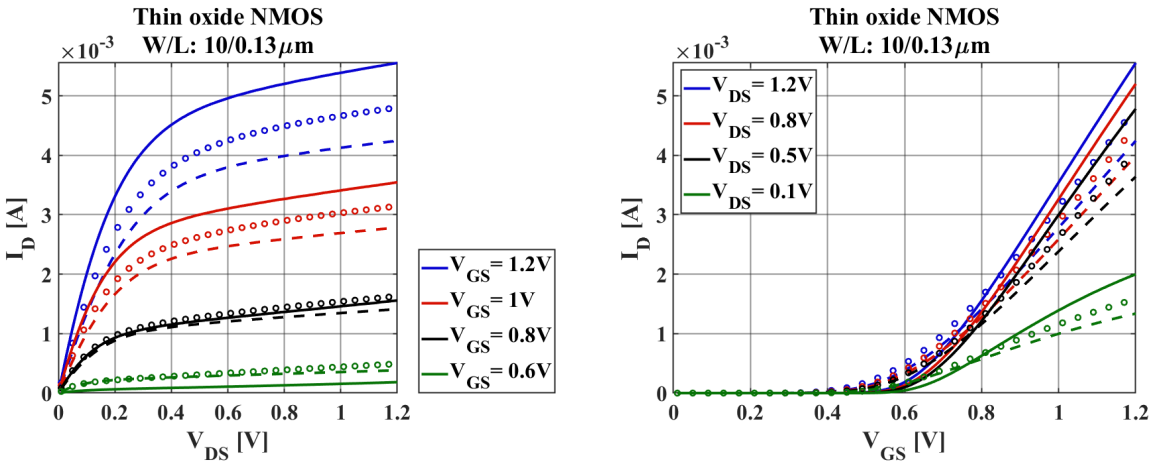


Figure 3.27: Measurement set-up for probe station measurements of MOSFETs

The probe station measurement results exhibit normal behavior (seen in figure 3.28) in all 10 devices in segments S540 and S541. Although these samples are different from that of the ones that display the abnormal behavior, the conclusion is that the behavior seen in figure 3.26 is likely caused by an ESD event, whether it is from the bonding process or the handling remains unknown.

3.2.4. Cryogenic behavior

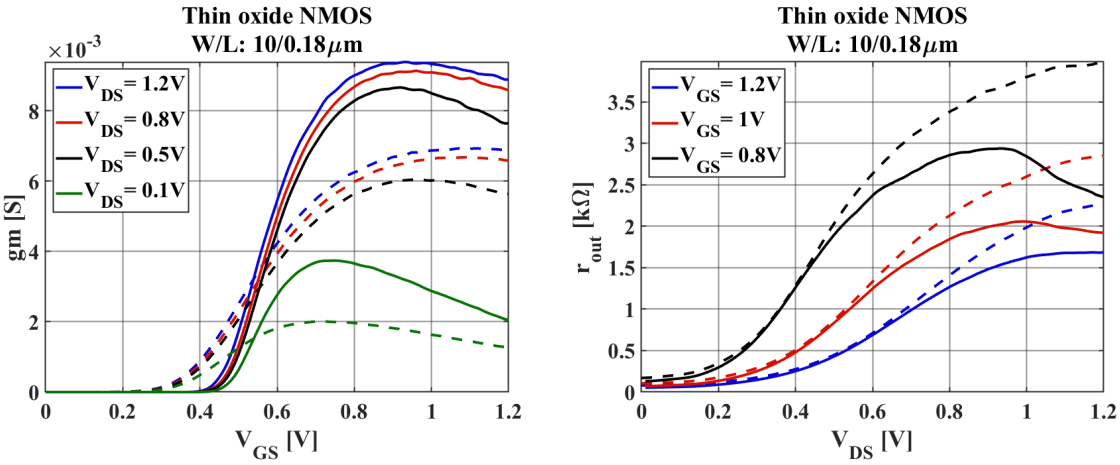
Several parameters can be extracted from the measurement data in the figures above that could shed extra light on the performance changes of the transistors. The most relevant device for the analog designer is the minimum-length thin-oxide 10/0.13μm NMOS device. However, as discussed in the section above (section 3.2.3), issues arose in that particular device. Therefore, a further analysis of the thin oxide 10/0.18μm NMOS device will be discussed in the figures 3.29a - 3.30b. First, the transconductance is calculated from the transfer characteristics (Fig. 3.29a), which shows an increase as the temperature decreases. Second, the output resistance is calculated from the output characteristics (Fig. 3.29b), which shows a decrease as the temperature decreases. This is, as mentioned in chapter 2, due to the increase in carrier mobility at lower temperatures.



(a) Output characteristics, RT (Broken lines), LH (Solid lines) and simulated (Circles)

(b) Transfer characteristics, RT (Broken lines), LH (Solid lines) and simulated (Circles)

Figure 3.28: Output and transfer characteristics of an LS NMOS device showing normal behaviour at 15K temperature

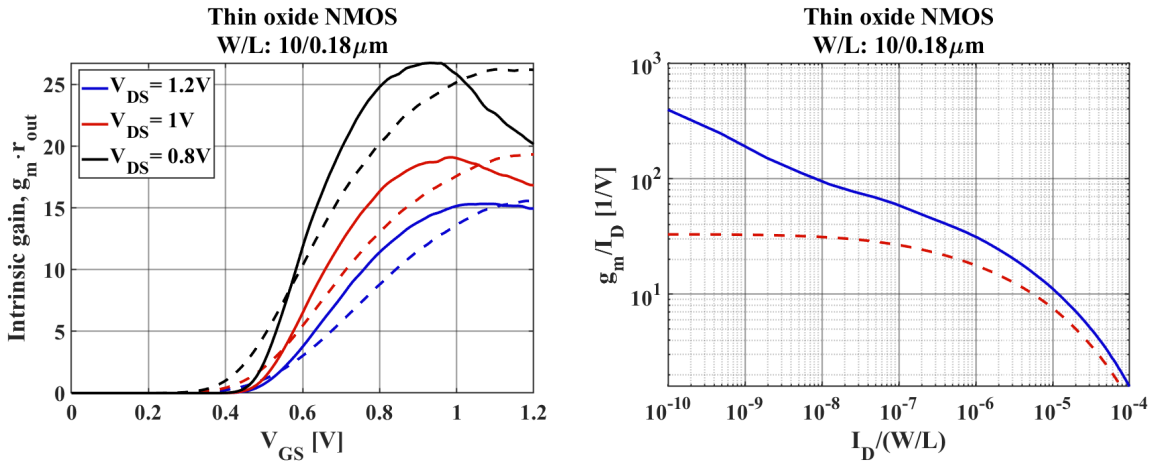


(a) RT (Broken lines), LH (Solid lines)

(b) RT (Broken lines), LH (Solid lines)

Figure 3.29: Transconductance and output resistance of a thin oxide NMOS

Other parameters, that are useful for an analog designer, are the intrinsic gain (Fig. 3.30a), and the transconductance efficiency g_m/I_D (Fig. 3.30b). The intrinsic gain is described as $A_{V0} = g_m \cdot r_{out}$ and since one parameter increases while the other decreases at cryogenic temperatures, the overall effect on the intrinsic gain is of interest. Comparing the temperature difference of the intrinsic gain in figure 3.30a, the 4-K measurements show a small deviation from the 300-K measurements indicating that the two parameters compensate for each other's changes at cryogenic temperatures. The transconductance efficiency g_m/I_D is a popular design variable for analog circuits, especially suited for low power designs. The g_m/I_D is plotted over the drain current normalized with the aspect ratio of the transistor (W/L). This relationship provides the designer with a simple tool for calculating device dimensions for a given maximum current [51]. The comparison between the two temperatures shows an overall increase in efficiency at cryogenic temperature. A continuous increase can be seen at lower drain currents at cryogenic temperature, which suggests a non exponential behaviour at weak inversion. It is unknown what the precise cause of this might be, but experimental data suggests that this might be the cause of discrete traps levels.



(a) RT (Broken lines), LH (Solid lines)

(b) RT (Broken line), LH (Solid line), V_{DS} = 1 V

Figure 3.30: Intrinsic gain (left) and the transconductance efficiency (right) of a thin oxide NMOS

As mentioned in section 3.2.3, the field effect transistor exhibits increased drain current at cryogenic temperatures due to carrier mobility increase at lower temperatures. This current increase can be seen in table 3.4, as well as the temperature influence on the gate width of the devices. The temperature influence is measured using equation 3.4, where the ratio of the maximum currents, of two devices with matching lengths, is normalized to the ratio of the width. The resulting calculations show minimum deviation between 300 K measurements and 4 K measurements, showing that temperature influence on gate width is very low.

$$LS/SS = \frac{I_{D,LS}/I_{D,SS}}{(W/L)_{LS}/(W/L)_{SS}} \tag{3.4}$$

As mentioned in section 3.2.3, there were issues with some LS devices (Table 3.3) and the 10/0.13μm thin oxide NMOS device could not be measured at 4K, therefore the 10/0.18μm device is used for the examination of temperature influence on the gate width. When examining the temperature influence on device scaling, the results in table 3.4 (LS/SS) indicates that the current scales proportionally to the gate width at both cryogenic and room temperature, except for small discrepancies possibly due to edge effects.

I_D	Thin oxide NMOS		Thin oxide PMOS		Thick oxide NMOS		Thick oxide PMOS	
	300K	**4K**	**300K**	**4K**	**300K**	**4K**	**300K**	**4K**
LS	4.334e-3	5.638e-3	1.948e-3	2.238e-3	6.496e-3	8.756e-3	2.456e-3	3.125e-3
SS	8.450e-5	1.011e-4	4.411e-5	5.037e-5	9.460e-5	1.319e-4	6.788e-5	9.112e-5
SL	2.515e-6	5.209e-6	5.891e-7	1.541e-6	8.904e-6	1.985e-5	2.575e-6	8.764e-6
LL	1.869e-4	5.559e-4	2.707e-5	4.438e-5	3.185e-4	8.541e-4	6.582e-5	1.551e-4
LS/SS	1.065	1.158	0.662	0.666	2.060	1.992	1.085	1.029
LL/SL	1.115	1.601	0.689	0.432	1.073	1.291	0.767	0.531

Table 3.4: Temperature effect on scaling ratio of thin oxide MOSFET, measured at $V_{GS} = V_{DS} = 1.2V$ for thin devices and $V_{GS} = V_{DS} = 3V$ for thick devices.

In table 3.5 the following parameters are displayed for a thin oxide NMOS and PMOS device.: temperature influence on the threshold voltage (V_{TH}) which is calculated using the extrapolation in the linear region method (ELR method [52]), subthreshold swing (SS) calculated using equation 2.7, drain current in the ON-state and OFF-state (I_{ON}/I_{OFF}), transconductance (g_m), and the output resistance (r_{out}) at $V_{GS} = V_{DS} = 1.2V$.

Type	Dim. [μm]	Vth [V]		SS [mV/dec]		Ion /Ioff		gm4K /gm300K	go4K /go300K
		300K	4K	300K	4K	300K	4K	4K /300K	4K /300K
Thin oxide NMOS	**10/0.18**	0.425	0.543	74.2	11.2	4.3e-3 /5.7e-10	5.6e-3 /1.8e-11	1.30	1.35
Thin oxide PMOS	**10/0.13**	-0.385	-0.537	75.7	12.2	-1.9e-3 /-1.4e-10	-2.2e-3 /-2.4e-11	1.34	1.28

Table 3.5: Main cryogenic performance figures for the smallest PMOS and NMOS, $V_{GS} = V_{DS} = 1.2V$

3.2.5. Kink effect

The kink effect, introduced in chapter 2, is observed in the thick-oxide devices (Noted with arrows in figures 3.23b and 3.24b). At high drain-source voltage, the drain current starts to increase in the saturation region. This effect is only visible in the thick oxide devices which corresponds to what has been reported in literature [49]. The effect is not seen in the thin oxide devices due to the thinner oxide which increases the vertical electric field in the channel furthermore decreasing the effect of impact ionization which correlates to the kink effect.

3.2.6. Hysteresis effect

Evidence of hysteresis effect, introduced in chapter 2, can be observed in the transfer characteristics (I_D/V_{GS}), where a sharp turn on slope is visible at a high V_{DS} bias (Figures 3.23a and 3.24a, highlighted with arrows). Additionally, hysteresis effect in the output (I_D/V_{DS}) characteristics can be observed when plotting the output resistance of thick oxide devices. The first hint of the effect being present can be seen in the right colormap of figure 3.31 at $V_{GS} = 0.9 - 1.5$ (Yellow rectangle) where the blue area extends above the threshold voltage region, indicating that the output resistance in that area is negative.

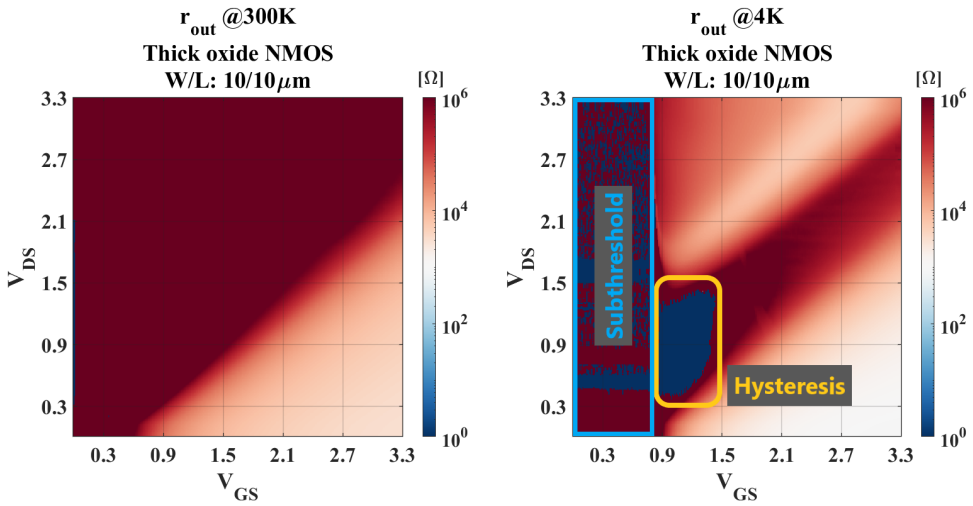
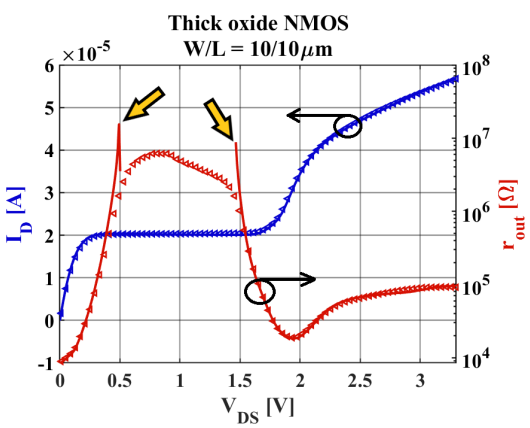
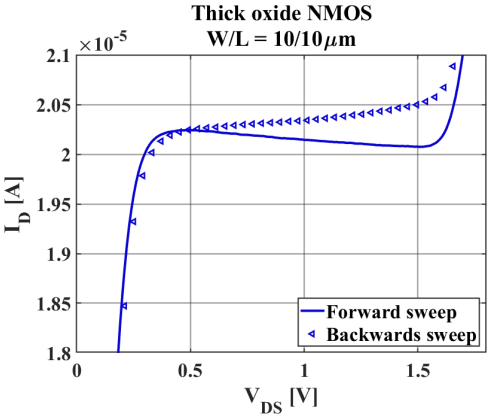


Figure 3.31: Colormap of the output resistance of a thick oxide NMOS showing evidence of hysteresis (Yellow rectangle)

Further examination in the region, in figure 3.31, is done by biasing the gate voltage between 0.9V and 1.4V and performing a forward sweep followed by a backward sweep of the V_{DS}. From those measurements, the output resistance is calculated and plotted in the same graph (Fig. 3.32a). The solid line indicates the forward sweep and the triangles indicate the backward sweep. In the forward sweep, the output resistance takes a steep dive below zero (Discontinues, highlighted with yellow arrows in fig. 3.32a) at 0.5 V_{DS} until 1.4 V_{DS}, indicating that the slope of the solid line in the I_D/V_{DS} curve is negative and effectively showing a negative-differential-resistance. However, when sweeping backward (Triangles), the output resistance takes a natural line through that region. In figure 3.32b, a zoomed-in view of the output characteristics in figure 3.32a can be seen, where the forward sweep and the backward sweep do not follow each other.



(a) Output characteristics (Blue) and output resistance (Red)



(b) Zoomed in view of the output characteristics, showing the hysteresis effect

Figure 3.32: Hysteresis effect in the output characteristics, forward sweep (solid line), backward sweep (triangles)

3.2.7. Subthreshold swing

In figure 3.22a (Highlighted with arrows), the drain current exhibits deformities in the subthreshold region. This can be examined by looking at the subthreshold swing shown in figure 3.33, the subthreshold swing at 4 K of 2 thin oxide PMOS devices are plotted with respect to drain current to examine the deformities in the subthreshold region. The 10/0.18 μm device exhibits relatively normal and smooth characteristics over the drain current while the 10/0.13 μm device shows an increase in the subthreshold swing at $I_D = 10^{-7}$ range. This behavior can be explained as discrete trap energy levels in the oxide or the interface. As electrons get trapped, more gate-source voltage is needed to increase the current in the channel, hence the increase in the subthreshold swing [53],[29],[54].

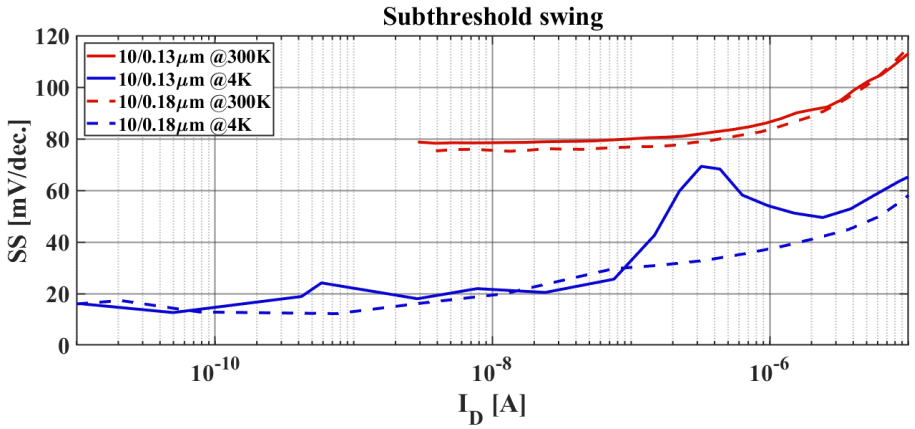


Figure 3.33: Subthreshold swing of 2 thin oxide PMOS devices

3.3. Resistors

Four types of resistor segments are under investigation, denoted as segments S300, S317k, S318k, and S319k. Each segment contains 4 resistors of different widths and lengths, seen in table 3.6, and the material of which the resistor is composed varies between the segments:

- Segment S300 contains a Metal1, Metal2, and unsilicided P+ Polysilicon and N+ polysilicon resistors (Referred to as "Multi Structure" segment in the following paragraphs).
- Segment S317k contains 4 unsilicided P+ doped Polysilicon resistors.
- Segment S318k contains 4 unsilicided N+ doped Polysilicon resistors.
- Segment S319k contains 4 silicided N+ doped Polysilicon resistors.

W/L [μm]	Multi Structure	Unsilicided P+Poly (Rppd)	Unsilicided N+Poly (Rhigh)	Silicided N+Poly (Rsil)
DUT1	M1 - 1.6/560	0.5/1	0.5/1	0.5/1
DUT2	M2 - 2/560	1/2	1/2	1/2
DUT3	Rsil - 1.3/400	1/8	1/8	1/8
DUT4	Rppd - 1.3/400	4/8	4/8	4/8

Table 3.6: Resistor dimensions

3.3.1. Measurement set-up

Both room and cryogenic temperature measurements are performed in a dip-stick set-up, using a Keithley 2636B SMU for sourcing current and a Keithley 2002 multimeter for voltage measurements due to its higher measurement accuracy compared to the SMU, as needed for the lower resistances of the metal resistors. A single chip is used for each segment, which is bonded onto a PLCC package and mounted on a PCB. The PCB contains relays that connect the DUT to the SMU. The set-up is similar to the one described in section 3.2.1

The S317k-S319k segments have 5 pads for each resistor: 4 pads are intended for 4-wire measurements and the remaining pad is connected to the center of the resistor, splitting the resistor in half. In this project, this middle pad is not utilized. In the S300 segment, each resistor is split into half, one half containing a single wide line and the other half containing 10 small lines with a total thickness which adds up to that of the single, wide line. This structure can be used to look into the heat dissipation of wide compared to small lines. However, this is not investigated in this thesis. A micrograph of the structures can be seen in figure 3.34, the first device of the S300 structure is highlighted with the force and sense pads noted in the figure.

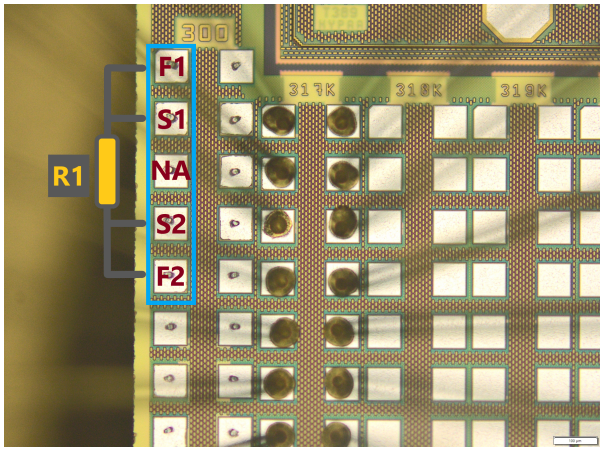


Figure 3.34: Micrograph of the resistor structure, one device highlighted (blue area)

3.3.2. Measurement technique

Measurements of each resistor are performed at a predefined power dissipation from 1 nW to 10 mW with a step size of a single decade. First, the DUT is coarsely measured by forcing a voltage and reading the current. The roughly measured resistance of the DUT is then used to calculate the current that is to be forced for the corresponding power dissipation. This is done to get more consistent measurements due to the self-heating of each resistor. A measurement restriction is imposed by the maximum current allowed in the resistors/vias, which is indicated in the process technology document provided by IHP.

3.3.3. Measurement results

Tables 3.7 and 3.8 display the calculated sheet resistance ($R_S = R_{measured} \cdot W/L$) from the measured resistance of each resistor along with the comparison of the expected room temperature data from the process document. In the calculations of the sheet resistance, the contact resistance on each side of the resistor is not taken into account and as the sheet resistance changes with the length of the resistor, the calculation of the contact resistance becomes difficult. Therefore the contact resistance is neglected in the calculations and the focus is kept on the temperature comparison.

- The unsilicided P+Poly resistor shows the most promise as it shows no strong dependence on temperature or dimensions when cooled down to liquid helium temperature.
- The first device of the unsilicided N+Poly (Rhigh) segment was damaged and therefore no measurements are shown. However, the other devices of the segment showed a clear temperature dependence where the resistance doubled for all devices at cryogenic temperature.
- The silicided N+Poly resistors showed dependence on both temperature and dimensions as the resistance decreased with temperature as well as decreasing with increasing resistor length.
- Measurements results of the multi-structure segment show that more extensive research is needed to fully understand the influence on the resistor dimensions at cryogenic temperatures. The Rppd and the Rhigh resistors in the segment are both 400μm long resistors and the do not follow the measurement results of the shorter devices in segments S317k and S319k when looking at the scaling factor in table 3.9. The resistance of the metal 1 and metal 2 resistors significantly decreases at cryogenic temperatures which would be highly beneficial in both the signal and supply paths in high-frequency designs at cryogenic temperature.

Sheet resistance	**Multi structure**		
W/L [μm]	PDK $\Omega/sq.$	300K $\Omega/sq.$	4K $\Omega/sq.$
1.6/560	0.11	0.115	0.016
2/560	0.088	0.089	0.011
1.3/400	6.94	6.07	1.81
1.3/400	260.17	6.54	2.19

(a) Multi structure resistance segment

Sheet resistance	**Uncilisided P+Poly (Rppd)**		
W/L [μm]	PDK $\Omega/sq.$	300K $\Omega/sq.$	4K $\Omega/sq.$
0.5/1	330	584	617
1/2	295	311	314
1/8	269	272	265
4/8	269	213	219

(b) Unilicided P+Poly resistance segment

Table 3.7: Sheet resistance from measurement results

Sheet resistance	**Unsilicided N+Poly (Rhigh)**		
W/L [μm]	PDK $\Omega/sq.$	300K $\Omega/sq.$	4K $\Omega/sq.$
0.5/1	1.64 k	NA	NA
1/2	1.49 k	1.30 k	2.23 k
1/8	1.44 k	1.44 k	2.76 k
4/8	1.39 k	1.41 k	2.65 k

(a) Unsilicided N+Poly resistance segment

Sheet resistance	**Silicided N+Poly (Rsil)**		
W/L [μm]	PDK $\Omega/sq.$	300K $\Omega/sq.$	4K $\Omega/sq.$
0.5/1	15.78	74.65	75.45
1/2	11.39	17.32	5.14
1/8	8.01	8.87	1.40
4/8	8.10	12.55	1.85

(b) Silicided N+Poly resistance segment

Table 3.8: Sheet resistance from measurement results

Table 3.9 shows the R_{300K}/R_{4K} factor of each device, further showing the temperature behavior of each devices. As noted above, the behavior of the Rppd resistor remains unaltered at cryogenic temperatures. The Rhigh structure shows a lower temperature scaling factor as resistance increases at lower temperatures, but a uniform scaling factor over W/L aspect ratios. The Rsil structure show varied scaling factor over both temperature and W/L aspect ratio due to the added silicide layer on the N+Poly resistor.

R300K /R4K	**Multi Structure**	**Unsilicided P+Poly (Rppd)**	**Unsilicided N+Poly (Rhigh)**	**Silicided N+Poly (Rsil)**
DUT1	M1 = 7.01	0.95	NAN	0.99
DUT2	M2 = 7.97	0.99	0.58	3.37
DUT3	Rsil = 3.35	1.02	0.52	6.34
DUT4	Rppd = 2.99	0.97	0.53	6.76

Table 3.9: Temperature scaling of sheet resistances

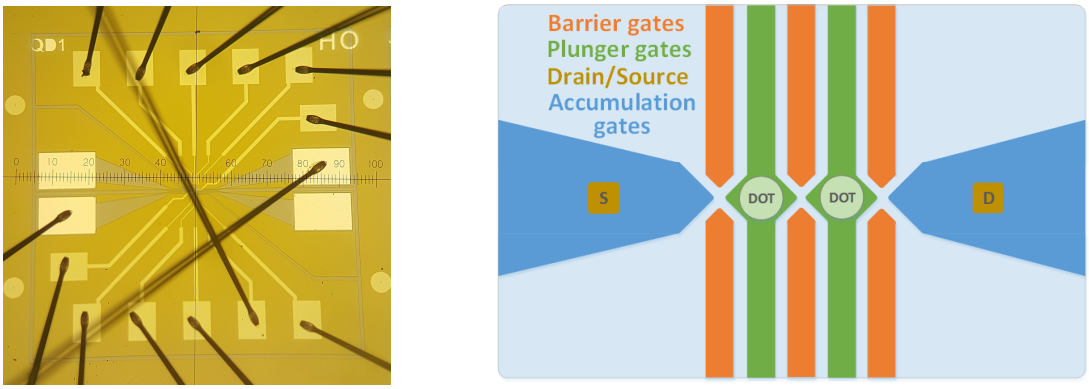
4

SET characterization

This chapter describes the characterization of a single electron transistor (SET) and the procedure of bringing up coulomb blockade oscillations. First, the structure and the general operation of the SET used in this project will be introduced. Then, a comprehensive tune-up procedure to bring up coulomb blockade oscillations is explained, followed by the measurements of a charge stability diagram as well as the extraction of design parameters and interpretation of the measurement data.

4.1. Double quantum dot, etched gate single electron transistor

The sample used in this project is a single layer silicon MOS structured double quantum dot (DQD) device, gate defined by reactive-ion etching. As mentioned in chapter 2, a quantum device for spin qubits consists of a single or multiple qubits, depending on the sample, and for each qubit, a sensing dot is required to readout the state of its respective qubit. The structure of the sensing dot can be reduced to a single dot device and therefore only a single dot of this DQD device is used for the purpose of this project. The existence of the extra dot is, however, an added practical benefit: in the case of either dot failing due to bonding or any other connection issues to the device, one could simply use the other dot of the device. A micrograph of the wire-bonded device (left) as well as a top-down view depicting the contacts and the dot locations (right) can be seen in figure 4.1. Two gates control each barrier from the top and the bottom (orange), one gate controls each plunger (green) and one gate controls each accumulation (blue) at the drain/source wells (yellow).



(a) Micrograph

(b) Top-down view

Figure 4.1: Micrograph of the SET

Comparing the cross-sectional view of the SET (figure 4.2) to a common MOSFET structure, one can see some similarities. Both structures have doped drain/source wells and between them, a gate to form a channel between the two. But in the SET's case, multiple gates are used to form a conductive channel between the source and the drain. The center gates are a 10 nm NbTiN layer spaced with a 60 - 50 nm pitch and isolated with a 7 nm SiO_2 layer. Adding potential to the gates forms a two-dimensional electron gas (denoted 2DEG in figure 4.2) at the Oxide/Silicon interface underneath the gates which allow the electrons to move from source to drain. In order to form a dot underneath the plunger, the potential of the two neighboring barrier gates must be decreased to pinch off the channel formation, creating barriers on each side of the plunger and forming a small accumulation of 2DEG under the plunger. As the dot is formed, each surrounding gate is capacitively coupled to the dot.

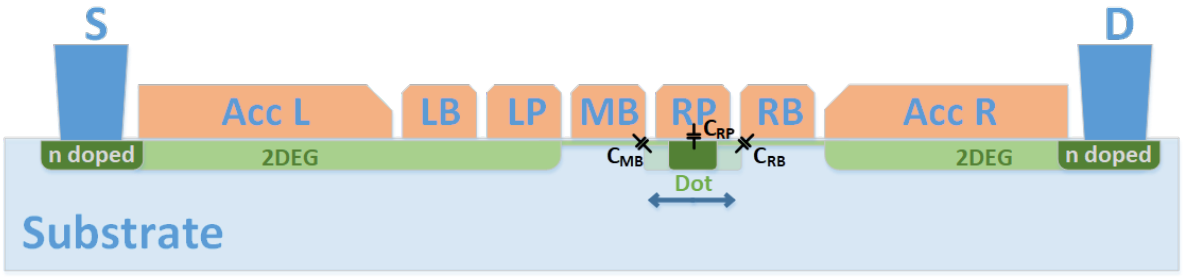


Figure 4.2: Cross-sectional view of the SET

4.2. Measurement set-up

The SET is characterized at liquid helium temperature (4 K) using a dip-stick set-up. The SET sample is bonded to a PLCC package that resides on a PCB. The drain and source pads are routed to room temperature and to the measurement transimpedance amplifier (TIA) [55] via coaxial cables for low leakage measurements of the drain current. The gates of the SET are routed via DC lines to room temperature and connect to a matrix module which is utilized for easy manipulation of gate connections. An in-house built 18-bit DAC at room temperature provides the voltage to the gates of the SET [56]. The drain of the SET is also biased via the DAC and a TIA provides a virtual ground signal to the source while measuring the drain current of the SET.

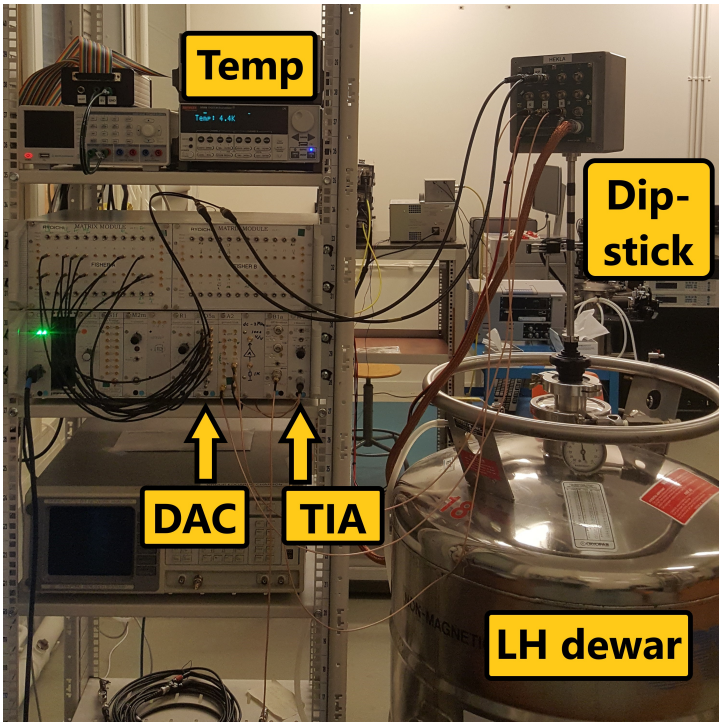
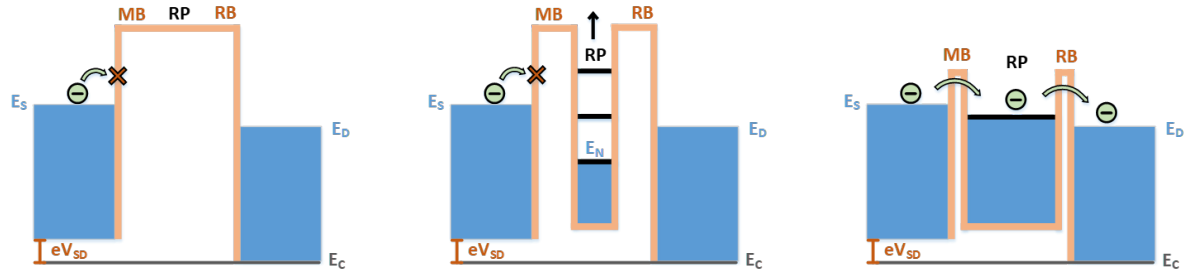


Figure 4.3: The measurement set-up for SET measurements

4.3. SET tuning procedure

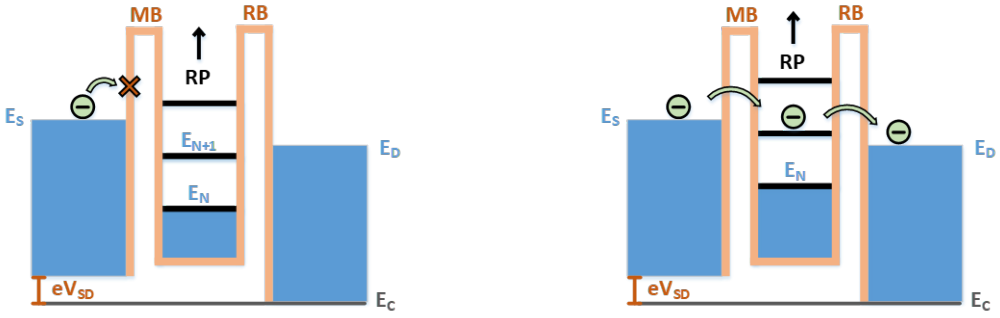
In order to bring up coulomb blockade oscillations, the SETs 2DEG dot must be properly tuned by biasing its respective gates. This involves tuning the plunger and neighboring barriers to form a 2DEG dot under the plunger with coulomb blockades on either side of the dot. As the 2DEG dot is formed, it becomes capacitively coupled to the plunger gate and its respective barrier gates on either side of the dot due to the small proximity to other gates. The coupling is then used for spin-to-charge conversion of the qubit as the coupling in the sensing dot changes with respect to the electron occupancy of the qubit dot that is being sensed. Therefore, the thickness and potential of these barriers are determined by the potential of the barrier gates as well as the potential of the plunger gate. If there is no voltage on the plunger gate, a dot is unable to form and the plunger acts as a barrier (Fig. 4.4**a**). If the voltage on the neighboring barriers is too high the barrier potential becomes too high and the thickness becomes too much for tunneling to occur (Fig. 4.4**b**). If the voltage on the barriers is too low, the barrier potential lowers and the thickness decreases (Fig. 4.4**c**), lowering the tunneling resistance to the point where quantization of electrons is indistinguishable and the electrons will continuously move through the channel.



(a) (b) (c)

Figure 4.4: Energy band diagram for tuning an SET

The optimal point is when the barrier thickness is high enough to not allow electrons tunneling through the barriers when the energy bands of the plunger are not between the energy bands of the source and drain (figure 4.5a). But when the capacitance of the dot is changed by changing the plunger potential and moving an energy band of the plunger between the energy potential of the source and drain, the electrons are able to discretely tunnel through the barriers and into or out of the dot (figure 4.5b).



(a) Tunnel junction in the coulomb blockade regime

(b) Tunnel junction in the tunneling regime

Figure 4.5: Energy band diagram of an SET

The first measurement procedure is checking for accumulation under the gates. This procedure involves forward sweeping all gates from 0 V until a 2DEG channel forms under the gates and current flows from drain to source. To limit the current flow in the channel, the drain-source voltage is set to 100μV. In figure 4.6 a voltage is swept from 0 V over all gates (plunger, barrier, and accumulation) simultaneously while measuring the drain current of the SET. A simple code can be executed to monitor the point of saturation and subsequently limit the sweeps to a voltage range below saturation. Getting the voltage range is crucial for the operation of the SET since too much accumulation under a gate can cause overlap of neighboring gates and therefore negating the effect of a barrier or a plunger that is to be swept later on.

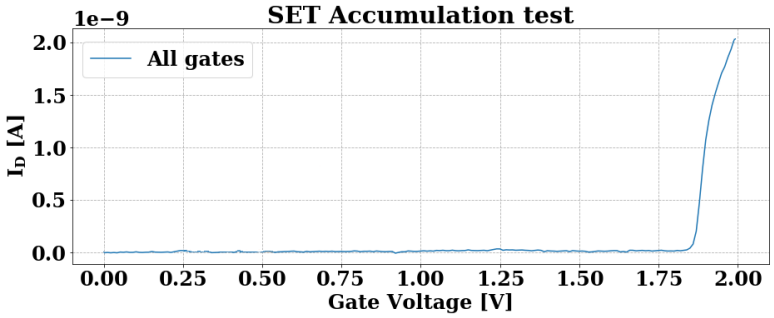
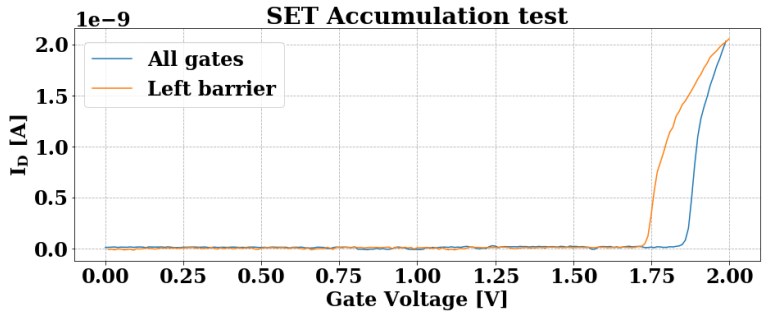
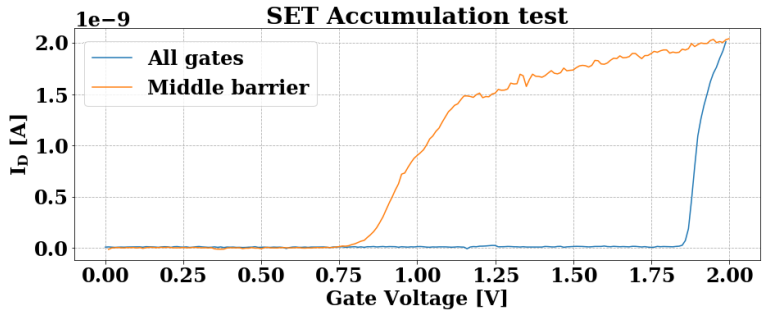


Figure 4.6: Channel formation in the SET

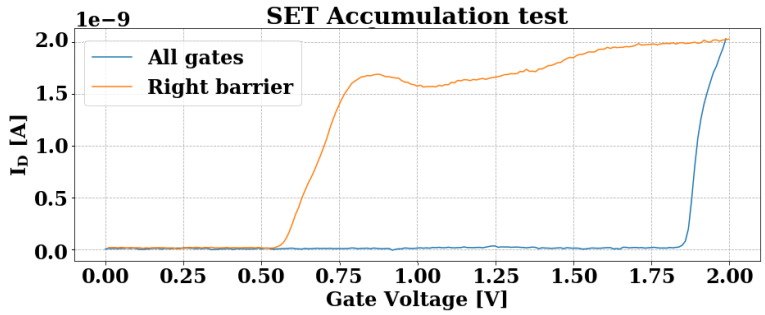
Next, individual gate characteristics can be collected for each barrier. This is done by forward sweeping all gates to the point of saturation followed by a reverse sweep of a single barrier gate. These two sweeps are performed for all barriers to get an estimate of the biasing points of the SET dots. Figures 4.7a, 4.7b and 4.7c show the barrier check of the left, middle and right barrier, respectively. The measurements show that the right and middle barrier have a pinch-off voltage at around 0.5 - 0.7 V, while the left barrier pinch-off is at 1.7 V. This deviation could be an indication of many defects, for example, an issue in the fabrication or an issue with one of the two gates controlling the barrier. However, the SET had previously been measured and the results of those measurements showed a pinch-off voltage of 0.6 V for all barriers. Therefore, the issue is more likely not due to fabrication, but to handling in the measurement process. It should be noted, however, that a dot can be formed with the left barrier but for the sake of this project, only one dot is needed and therefore the right dot can be used while the left barrier is simply used as an accumulation gate.



(a) Left barrier, forward sweep (blue) and reverse sweep (orange)



(b) Middle barrier



(c) Right barrier

Figure 4.7: Accumulation test of barrier gates

The pinch-off point of the barrier gates in figures 4.7a, 4.7b and 4.7c gives an approximation of the biasing range of each barrier required to produce coulomb oscillations. When sweeping for coulomb oscillations of a single dot, the accumulation gates are set to a voltage above the saturation point. As mentioned above, the dot in question is the right dot, meaning that further adjustments of the middle barrier (MB), right plunger (RP), and right barrier (RB) must be made, while the rest of the gates are set to the accumulation voltage.

The next step is finding the optimal barrier thickness to produce coulomb oscillations. In figure 4.5, the plunger voltage is swept continuously at 4 bias points for the right barrier while the middle barrier is kept at a constant potential of 0.6 V. The red line indicates that the barrier thickness/height is too large but as the

barrier potential is lowered by raising the right barrier voltage (green and yellow lines), the electrons are able to tunnel discretely through the barriers. But when the barrier voltage is too high (blue line) the electrons start to flow continuously through the channel. If the current remains flat (red line) over all voltage biases for the right barrier (RBs), then the voltage of the opposite barrier (middle barrier) can be increased from 0.6 V and vise versa if the drain current follows the blue line for all middle barrier biases. However, the balance between the two barriers should remain to have equal barrier thickness/height on both sides of the 2DEG dot. It should be noted, again, that the measurements are performed at 4.2K temperature, and due to thermal broadening (k_BT approaches the quantum level spacing ΔE) the peaks are less defined and the conductance gradually increases at higher plunger voltages [57].

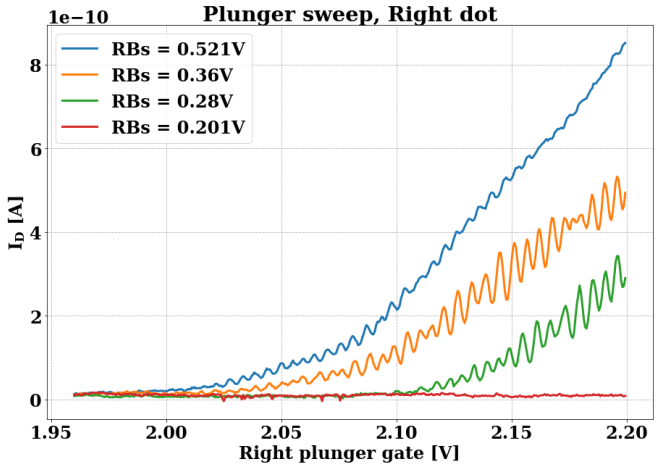


Figure 4.8: Bringing up coulomb oscillations

4.3.1. Charge Stability Diagram

After tuning the SET, a charge stability diagram can be attained. The charge stability diagram shows the charge occupancy of the dot at a given gate voltage. A fine parametric sweep is performed by biasing the accumulation gates as well as the middle barrier and sweeping the right plunger while stepping the right barrier. This results in the charge stability diagram seen in figure 4.9. The coulomb oscillations display a slope like behavior as the right barrier potential is raised. This indicates that a dot is present in the SET and is capacitively coupled to its respective gates (plunger, barriers). From the charge stability diagram, the signal amplitude of the oscillations is extracted as a signal with a maximum amplitude of 100 pA to 130 pA.

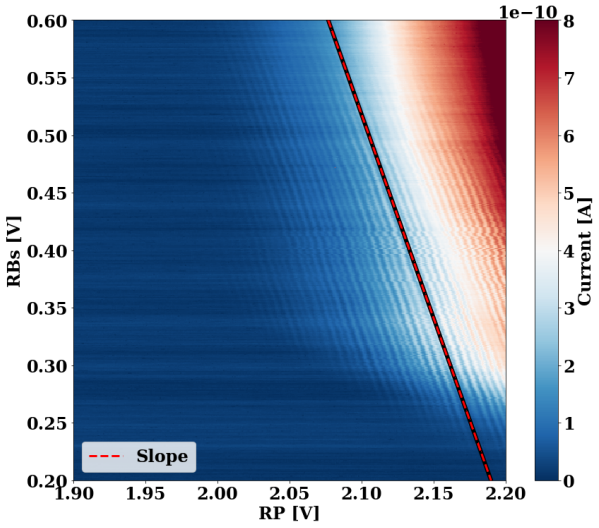


Figure 4.9: Charge stability diagram

At an RB potential of 0.4 V, there is a visible shift in the oscillations. This shift is an indication of a discrete trap level in the oxide or in the interface which the charge carriers can jump in and out of, causing a change in the capacitance of the dot. This discrete trap has been used in literature [58] to emulate single-shot readout of an SET, where the trap acts as a qubit, and depending on the state of the trap, the coupling between the dot and the trap changes and further changing the output signal of the SET.

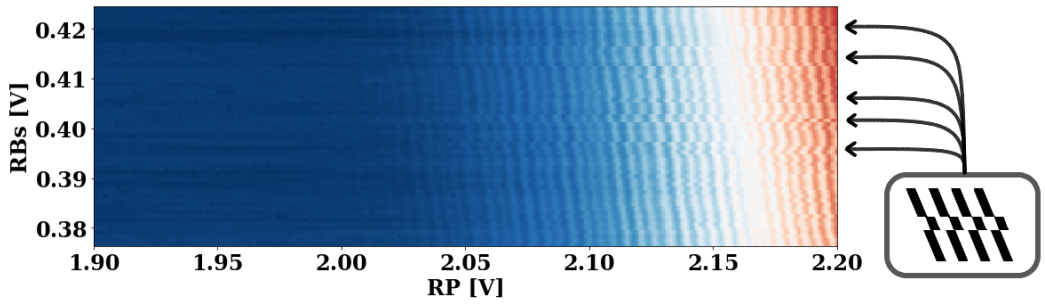
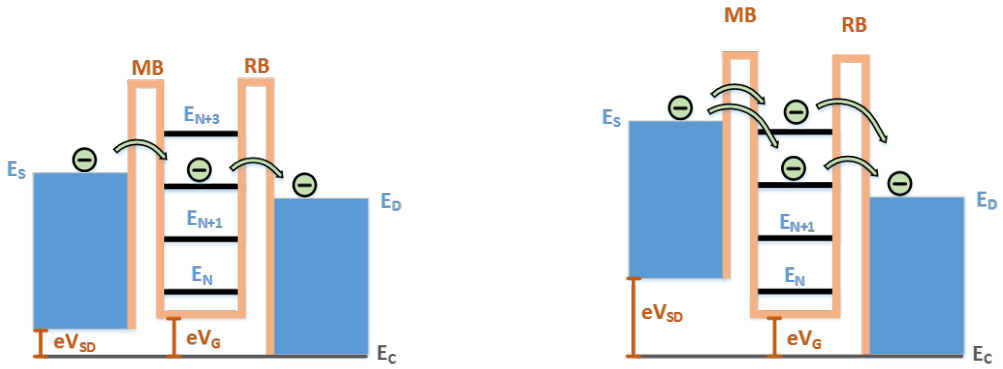


Figure 4.10: Close-up view of the charge stability diagram

4.3.2. Coulomb Diamonds

Now that a 2DEG dot is established in the SET, the charging energy of the dot can be measured by sweeping the drain/source voltage and stepping the right plunger (figure 4.13). The figure shows a diamond-like structure, hence the name coulomb diamonds. From the coulomb diamonds, the charging energy can be established by the height of the diamonds, as mentioned in figure 2.15b, chapter 2. Looking at the energy band diagram (figure 4.11), the Fermi level difference between source and drain is manipulated. The charging energy is defined as the difference between energy levels in the plunger, $\Delta E = E_{N+1} - E_N$. As the drain voltage increases, the difference between the drain/source fermi levels increases and the plunger starts to fit more energy levels into that drain/source gap thus, allowing more than one electron to tunnel in and out of the dot. In figure 4.12, a representation of the drain current corresponding to three different drain/source bias points in the single electron regime, where the diamonds (blue area) represent a biasing point where no electron occupies the dot. In the multi-electron regime, the borders of the dot represent an electron tunneling in or out of the 2DEG dot. If the drain/source bias is increased further, more electrons can tunnel through the barriers, as represented in figure 4.11b.



(a) (b)

Figure 4.11: Energy band diagram of an SET

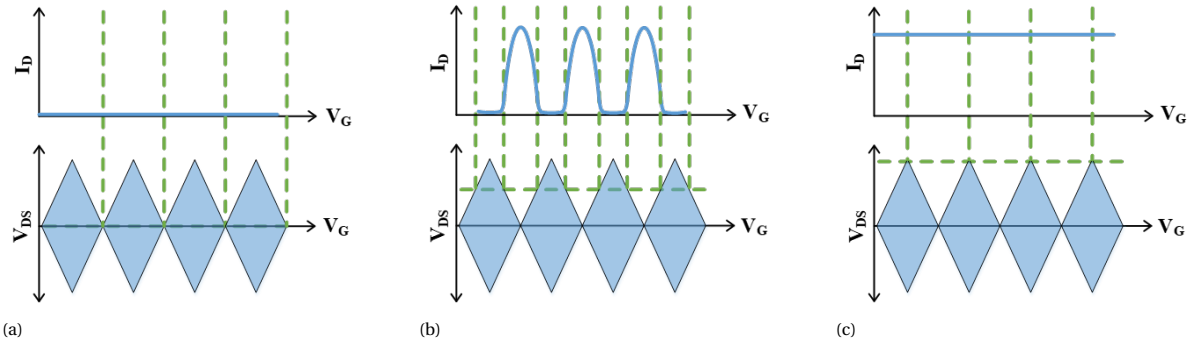
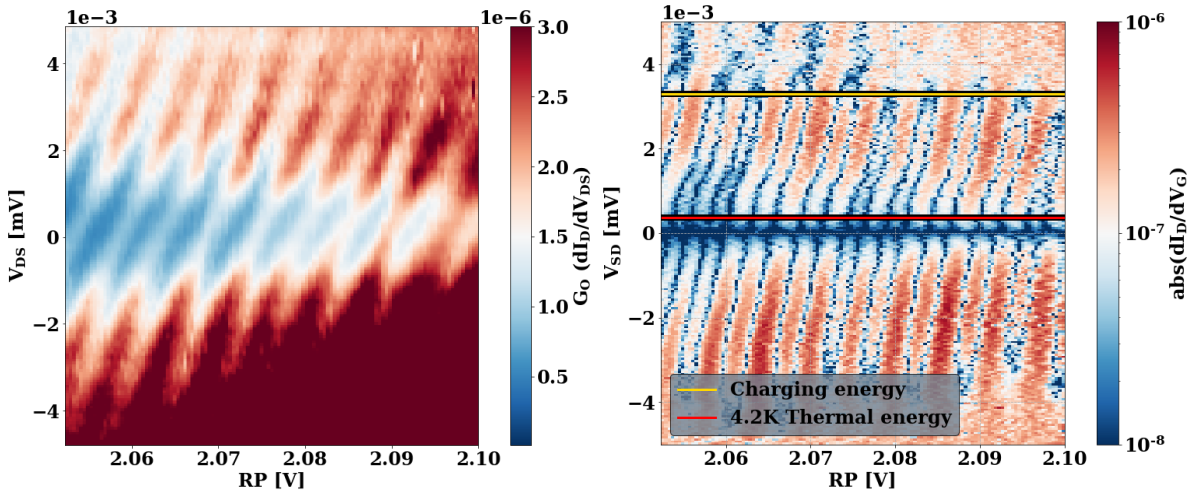


Figure 4.12: Coulomb diamonds and the corresponding drain current

To get a better visual of the diamonds, the conductance (dV_{DS}/dI_D) is plotted on the z-axis (color axis). However, the increased conductance at 4.2 K temperature due to thermal broadening makes it hard to distinguish the peaks of the diamonds. Therefore, the dI_D/dV_G is also plotted on the color-axis, with V_G as the right plunger gate voltage. This shows the point where the coulomb oscillation in figure 4.8 smooth out and the voltage over the drain/source of the SET has become larger than the charging energy of the SET, represented in figure 4.12**c**.

The charging energy determines the energy needed to charge the dot with an electron. This energy must be higher than the thermal energy kT (with k the Boltzmann constant and T the temperature at which the SET is measured) in order to avoid charges to enter the dot due to thermal activation. At liquid helium temperature of 4.2 K, the thermal energy is 362μ eV. From the height of the diamonds in figure 4.13b (yellow line), the charging energy of the dot is determined to be 3.3 meV and furthermore, higher than the thermal voltage making the device capable of quantum formation. The charging energy, established in this section, is a parameter that needs to be considered for chapter 5.



(a) dV_{DS}/dI_D (b) dI_D/dV_G

Figure 4.13: Coulomb diamond plots from measurements

From the coulomb diamond, the small-signal output resistance of the SET can be extracted ($R_{SET} = dV_{DS}/dI_D$). In figure 4.14 the output resistance is plotted over the drain-source voltage for several biasing points of the plunger gate. The output resistance of the SET is seen to vary from 100s of kΩ to 10s of MΩ, depending on the biasing of the barrier and plunger gates of the 2DEG dot. This compares well with what has been reported in literature [58].

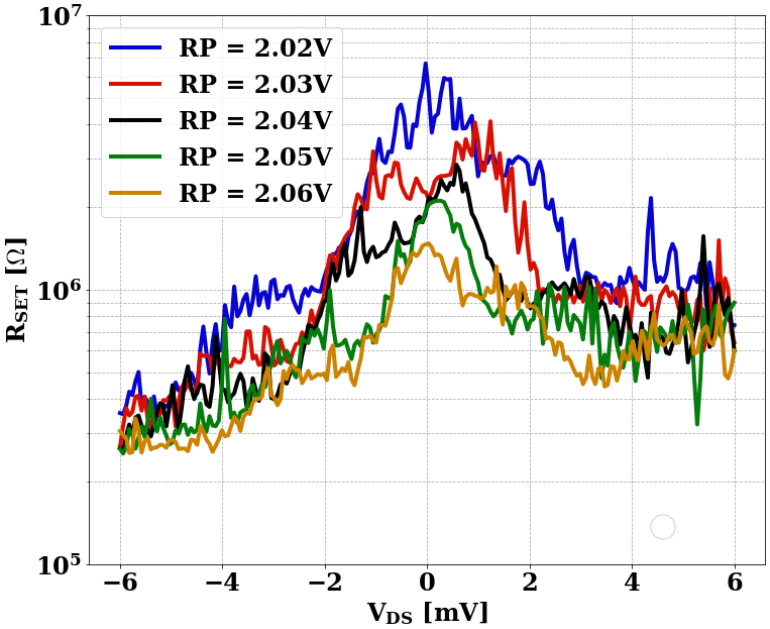


Figure 4.14: SET resistance over several biasing points

The measurements performed in this chapter confirm the functionality of the SET as a state detector for a spin-qubit readout. Additionally, crucial parameters for the cryogenic SiGe HBT amplifier are determined. Firstly, the output signal amplitude of the SET (100 pA to 130 pA) as an electron tunnels through a barrier and secondly, the output resistance of the SET (100s of kΩ to 10s of MΩ). These parameters are crucial for further calculations in chapter 5.2, which involve the analysis of the HBTs characterized in chapter 3 interfaced with the SET characterized in this chapter.

5

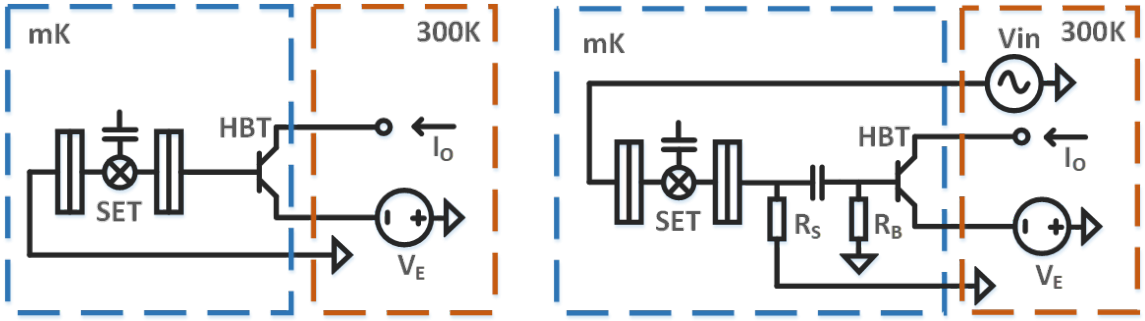
Cryogenic amplification of an SET

This chapter contains a comprehensive analysis of an ultra-low-power cryogenic amplifier using SiGe HBTs. The purpose is to validate the three HBTs available in the 0.13 μm BiCMOS technology as viable candidates for cryogenic amplification of a single-shot readout of DC spin qubits. Analysis of all 3 SiGe HBTs (Standard 8-finger, Standard 1-finger, and modified 8-finger), characterized in chapter 3, will be performed in conjunction with the charge sensing SET, characterized in chapter 4. The performance of the three SiGe HBTs will be compared to discuss further enhancement possibilities of the single-shot readout performance of spin qubits. First, the circuit architecture is chosen based on what has been reported in literature and the biasing conditions are established, followed by an analysis of the room temperature equipment. Then, DC measurements are performed on the SET with and without the SiGe HBT amplifier to validate the SETs ability to produce coulomb oscillations while connected to the amplifier. The chapter will conclude with an analysis of a capable single-shot readout performance for the 3 SiGe HBTs, i.e. analysis of the input signal, noise, bandwidth, and the SNR. The goal of this analysis is to prove that the three SiGe HBTs are capable of enhancing the single-shot readout performance by achieving an SNR of more than 7 dB at a bandwidth of 1 MHz.

5.1. Circuit architecture

5.1.1. Proposed topology

The proposed circuit topology for this thesis is a simple SiGe HBT amplifier, introduced in [58]. The amplifier consists of a single SiGe HBT device which is used to current bias the SET through the base-emitter junction and amplifies the signal it produces from qubit interactions. This current biasing amplifier design (CB-HBT) has been reported in literature and compared to a similar design which AC-couples the amplifier to the SET (AC-HBT). The comparison of the measurement results for the two circuit architectures shows a lower -3-dB bandwidth for the CB-HBT. However, the CB-HBT shows a higher gain, lower power consumption, and noise figure, as well as being a more simplistic design than the AC-coupled amplifier [58], therefore the CB-HBT design is chosen for this project. A streamlined schematic of both circuits can be seen in figure 5.1.



(a) Current biased amplifier

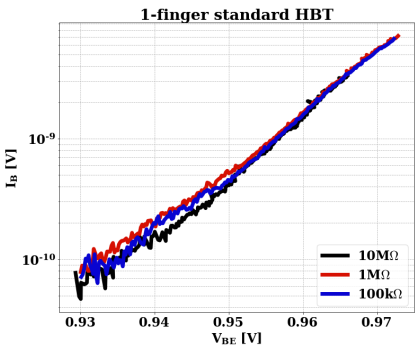
(b) AC-coupled amplifier

Figure 5.1: Simplified schematic of a current biased and AC-coupled SET amplifier circuits

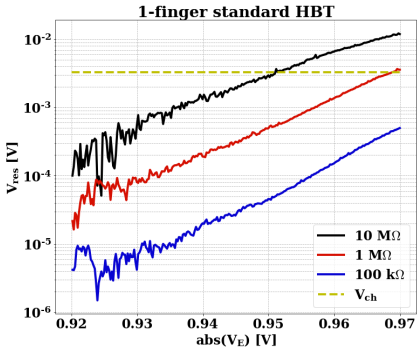
Referring to figure 5.1a, the CB-HBT circuit is described as such: The source of the SET is grounded and the drain is directly connected to the base of the HBT; The collector of the HBT is connected to an amplifier at room temperature which senses the output current; The emitter of the HBT is connected to a room temperature DAC for the voltage biasing of the HBT. The base-emitter voltage forces the drain voltage of the SET, which furthermore creates a current source which biases the SET. The emitter voltage can be adjusted for a desired current gain, SET biasing current, or power consumption of the amplifier. The gates of the SET (Barriers and Plunger, not shown in the figure) are routed to a room temperature DAC for further biasing of the 2DEG dot.

5.1.2. Biasing conditions

As mentioned in chapter 4, in order for the SET to produce coulomb oscillations, the voltage over the SET must not exceed the charging energy of the SET (3.3 mV). This limits the available emitter voltage range that is used to current bias the SET, as too much current would cause the voltage over the SET to exceed the charging voltage. To investigate this further, additional measurements of the 1-finger HBT device were performed, where the base current was measured over the emitter biasing voltage (V_E) with multiple shunt resistors (100 kΩ, 1 MΩ, 10 MΩ) in series with the base, to emulate the SET resistance. The base-emitter voltage (V_{BE}) can be calculated by subtracting the voltage over the resistor by the emitter voltage ($V_{BE} = |V_E| - (I_{base} \cdot R_{shunt})$). From there the Gummel characteristics for the base can be plotted (fig. 5.2a) and shows a minimum deviation when increasing the shunt resistance. This plot can be used as an estimation for the biasing current through the SET. Furthermore, the voltage over the SET, while connected to the HBT, can be estimated for a given biasing voltage $V_{SET} = |V_E| - |V_{BE}|$. Figure 5.2b shows the voltage over the 3 shunt resistors over the emitter voltage, along with the charging energy calculated in chapter 4, giving a good estimate of viable emitter voltage range for a given SET resistance.



(a) Base current over the base-emitter voltage for different shunt resistors



(b) HBT measurements for multiple series base resistance

Figure 5.2: Biasing conditions for the HBT amplifier

5.1.3. Room temperature equipment

The bandwidth of the system is an important parameter in order to improve the single-shot readout time of qubits in both selective and tunnel-based readout.

In chapter 4, the DC measurements of the SET were performed using an in-house built TIA with a limited bandwidth of DC to 10 kHz. This bandwidth would not meet the predefined specifications of the envisioned single-shot readout, therefore another in-house built room temperature amplifier was implemented. The options were defined between a TIA or a simple voltage amplifier. Analysis of the gain figures of the two designs (fig. 5.3) shows that neither design has a significant advantage over the other with the of the transfer function being displayed in equations 5.1 (Large gain approximation) and 5.2 for the TIA and the voltage amplifier, respectively.

$$\frac{V_{out}}{I_{in}}_{TIA} = \frac{R_f}{1 + s \cdot R_f \cdot C_f} \tag{5.1}$$

$$\frac{V_{out}}{I_{in}}_{Vamp} = A \cdot \frac{R_p}{1 + s \cdot R_p \cdot C_p} \tag{5.2}$$

Additionally, the input referred noise of either designs show no significant advantage over the other since the noise of R_p is significantly reduced due to the low temperature. Due to no significant difference in performance of the two amplifiers, a decision was made to implement a voltage amplifier. The amplifier used in the experiment is a voltage amplifier with a gain of 60 dB and a bandwidth of DC to 2 MHz, which exceeds the goal of 1 MHz bandwidth. The input is equipped with a 1 kΩ resistor used for current-to-voltage conversion of the output signal from the collector of the HBT. The amplifier input voltage noise is calculated by measuring the output signal of the amplifier with the input resistor at room temperature. The output signal (11 mV_{rms}) is then divided by the amplifier gain and the square root of the bandwidth ($\sqrt{2MHz}$) to get the total input voltage noise power of the amplifier. The calculated thermal noise power of the resistor is then subtracted from that figure, which gives an amplifier input noise of 6.6 $nV/\sqrt{Hz}$

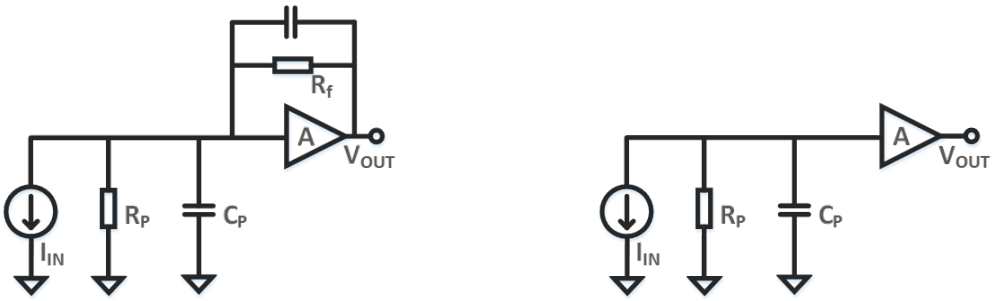
$$V_{n,amp} = 6.6 nV/\sqrt{Hz} \tag{5.3}$$

5.1.4. Circuit validation

Before going into the analysis of the single-shot readout performance of the 3 HBTs, the SETs' ability to produce coulomb oscillations while connected to the HBT amplifier is checked. Charge stability diagrams are produced, with and without the HBT amplifier, through DC measurements of the SET to validate the biasing conditions and to check the operation of the room temperature amplifier.

Measurement set-up

The measurement setup for the SET without the HBT amplifier can be seen in section 4.2. The measurement set-up for the SET connected to the amplifier was the same as in section 4.2, apart from the room temperature amplifier, which was introduced in the section above. To reduce the noise of the room temperature

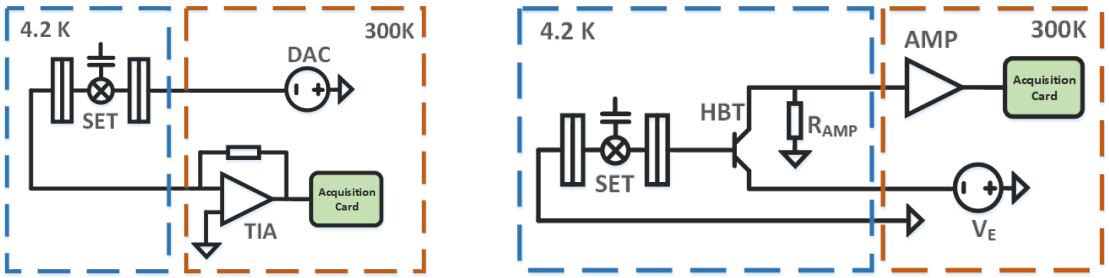


(a) Transimpedence amplifier

(b) Voltage amplifier

Figure 5.3: Schematic of the room temperature amplifiers

amplifier, the 1 kΩ thin film resistor, used for current to voltage conversion, was placed on the measurement PCB, to reduce its ambient temperature and thus reducing the noise of the resistor. A simplified schematic representation of both circuits can be seen in figure 5.4, in addition, the set-up can be seen in figure 4.3.



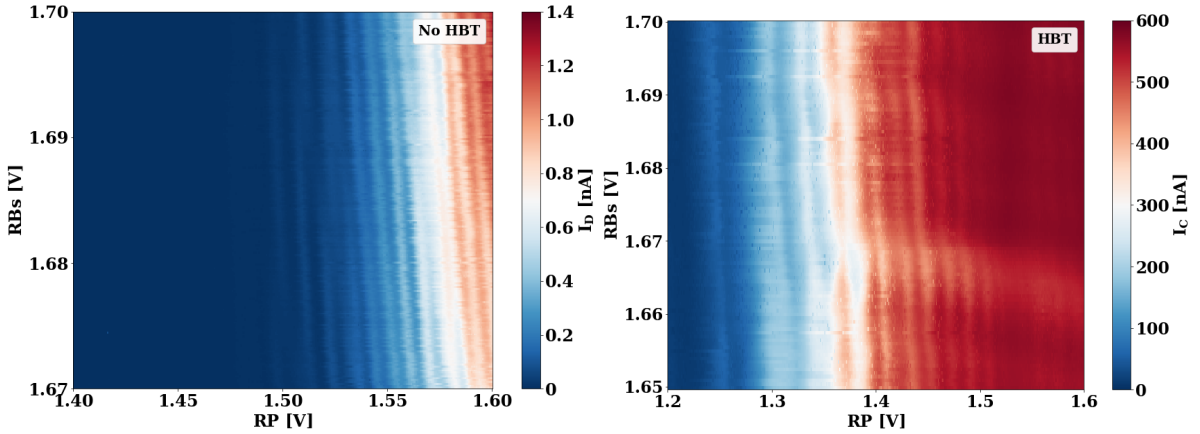
(a) Without the HBT

(b) With the HBT

Figure 5.4: Simplified schematic representation of SET measurement set-up with and without the HBT amplifier

Measurement results

For both measurements, the SET barrier and plunger gates were tuned/biased such that the SET was able to produce coulomb oscillation (section 4.3). Then the drain-source voltage was swept over multiple plunger gate voltages and plotted in a colormap style figure, otherwise known as a charge stability diagram. The stability diagram of both cases can be seen in figure 5.5 and show that with and without the HBT amplifier, the SET was able to form a 2DEG dot that is capacitively coupled to its respective gates. Without the HBT (Fig. 5.5a), the stability diagram shows a stable 2DEG dot with low charge coupling to the barrier gates (Spacing between coulomb peaks, $V_{g1} = e/C_g1$). Measurements of the SET with HBT (Fig. 5.5b) were made with the 1-finger HBT with an emitter bias of 0.957V, which according to figure 5.2b kept the voltage over the SET at around 1 mV. The measurements with the HBT show a less stable 2DEG dot with larger spacing between coulomb peaks, meaning that the coupling between the 2DEG dot and barrier gates is very low. However, the stability diagram shows a clear formation of a 2DEG dot. The SET measurements without the HBT show a drain current coulomb peak amplitude of 100 pA to 130 pA. The SET measurements with the HBT show a peak amplitude in the collector current of roughly 90 nA to 120 nA, hence indicating a capable DC gain of roughly 50 dB with the 1-finger HBT in the standard process, which is close to the expected current gain at a collector current of 200 nA to 600 nA from previous measurements (Fig. 3.14b).



(a) Stability diagram without the amplifier

(b) Stability diagram without the amplifier

Figure 5.5: Stability diagram with and without the HBT amplifier

Over the course of the previous measurements in chapter 4, the SET characteristics began to drastically change and some barrier gates were later shown to have discontinued from top connection to bottom connection, presumably due to ESD events. This raised the barrier gate voltage range (Y-axis) required to produce coulomb oscillations, as can be seen in figure 5.5 where the right barrier ranges from 1.67 V to 1.7 V compared to the barrier range of 0.2 V to 0.6 V in figure 4.9. Attempts were made to change the barrier potentials by adjusting the voltage potential of the barrier and plunger gates, but those attempts were unsuccessful. Plans were made to measure the 2 remaining HBTs and compare the results of all three HBT devices, but the SET sample broke down after the measurements of the 1-finger device resulting in no further measurements for the remaining 2 HBT devices. However, since the 1-finger HBT device is shown to work with the SET sample, the remaining 2 HBTs are assumed to show similar workings when connected to the SET.

5.2. Single Shot Readout

Due to the difficulties from directly measuring the spin state of an electron, a single-shot readout of DC spin-qubits employs a spin-to-charge conversion to measure the spin-up or spin-down state of an electron. Several methods can be used to measure the readout stage, e.g. Energy selective readout and tunnel rate selective readout, discussed in chapter 2. Both methods have 3 phases: Phase 1 is when the dot is emptied of an electron, phase 2 is when an electron with an unknown spin is injected into the dot, and phase 3 is when the spin state of the electron is read-out, the process is then repeated for another measurement. The phase of interest, for this project, is the readout phase (Phase 3). Additionally, a tunnel-rate selective readout scheme will be employed for the upcoming analysis of the single-shot readout performance.

5.2.1. Small signal analysis

The hybrid-pi model, introduced in section 3.1.4 (Fig. 3.16), is used for the small signal analysis of the SiGe HBT device. Connecting the SET to the base of the amplifier (biased with current I_{Bias}), introduces the output resistance of the SET (R_{SET}) in parallel with the input resistance (r_π) of the HBT in the small signal model (Fig. 5.6).

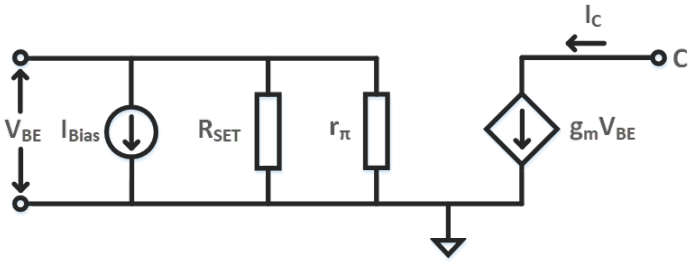


Figure 5.6: Small signal model of the HBT amplifier interfaced with the SET

This means that the current signal produced by the SET, due to qubit interactions, is divided between these two resistances which attenuates the extrinsic gain of the amplifier and further decreases the output signal of the amplifier. The output resistance of the SET is measured in chapter 4 (Fig. 4.14) and can vary from 100s of kΩ to 10s of MΩ, depending on the bias of the SET.

Those measurements were performed at 4 K temperature while a single-shot readout would be performed at the mK range, so for the sake of these calculations, the SET resistance is presumed to be 2 MΩ. The input resistance of the amplifier (r_π) can be extracted, for each biasing point, from the HBT measurements using equation 3.1 and ranges from 500 kΩ to 1 GΩ, depending on the biasing conditions (Fig. 3.15a). Knowing these two parameters allows for the calculation of the extrinsic gain of the amplifier, which shows the real current gain of the amplifier with the attenuation from the SET resistance. With the imposed SET resistance, the gain is calculated by multiplying the transconductance (Eq. 3.2) with the two resistors in parallel (Eq. 5.4). In figure 5.7, the calculated extrinsic gain at, 4-K temperature, of all three devices is plotted over the collector current and shows the excellent gain of the 8-finger modified device compared to the 8-finger standard device.

$$Gain_{HBT} = g_m \cdot (R_{SET} || r_\pi) \tag{5.4}$$

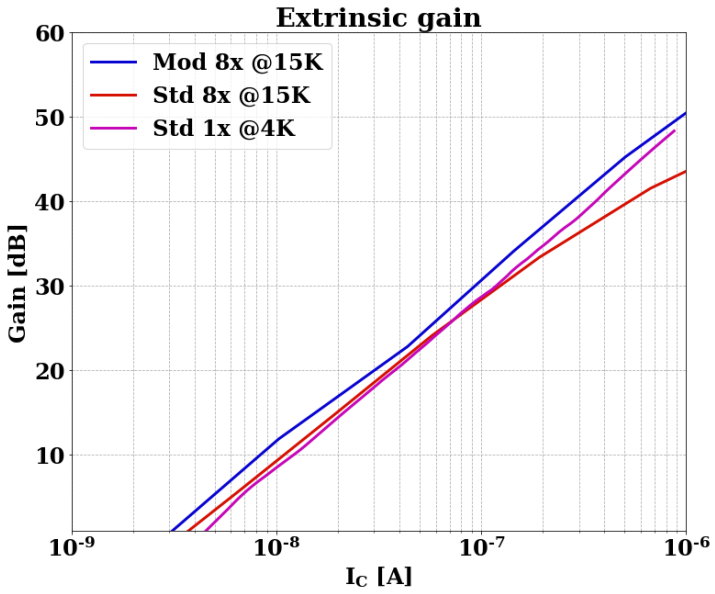


Figure 5.7: Extrinsic gain, r_π = 2 MΩ

5.2.2. Bandwidth consideration

The bandwidth is a crucial factor when it comes to the readout of spin-qubits due to it determining the rise time of the readout signal. This affects the total measurement time needed for a desired SNR of the signal. For the current biased circuit topology, there are two separate parasitic capacitances (C_p and C_l in fig. 5.8) to consider for determining the -3 dB bandwidth of the circuit.

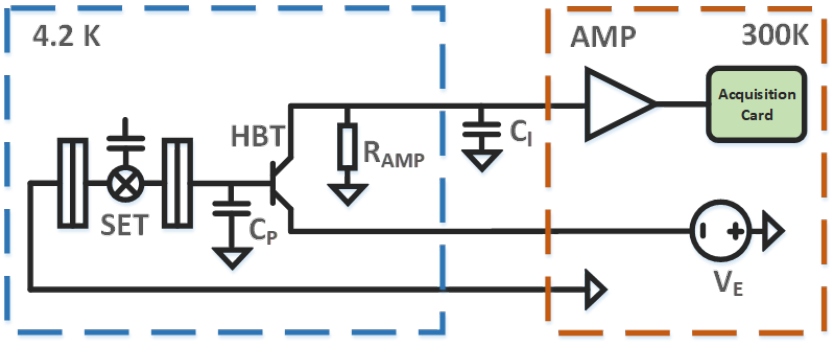


Figure 5.8: Schematic diagram of the current biased SET with relevant parasitic capacitances

The first parasitic capacitance (C_p) is imposed on the line between the SET-drain and the HBT-base. The set-up for the experiment is a package to package set-up. The HBT sample is glued to a PLCC package and the base is wire bonded to a pad in the package. Likewise, the SET sample is glued to another package and the drain is bonded to a pad in the package. Both packages reside in package holders, with a very short PCB trace connecting the two. Although it is difficult to accurately calculate this capacitance, it is assumed to be below 0.7 pF. Calculating the expected -3-dB frequency from the respective parasitic capacitance and the 2 MΩ resistance of the SET using equation 5.5, gives a minimum -3dB-frequency of f_{-3dB} = 113 kHz.

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R_{SET} \cdot C_P} \tag{5.5}$$

The second parasitic capacitance is the line capacitance (C_l) imposed on the collector node from the coaxial wire that routes the signal to the room-temperature equipment. From the factory specifications of the cable, the capacitance is 100 pF/m. Since the length of the coaxial cable is around 3 meters, the total capacitance is assumed to be 300 pF. This was proven by measuring the frequency response of the HBT. The output signal of the modified HBT was measured over multiple frequencies at 300-K temperature and 4.2-K temperature in the dip-stick set-up. A function generator provides the input signal to the base through a 1 kΩ resistor which is placed on the measurement PCB and connected in series with the base of the HBT. The collector is connected to the room temperature voltage amplifier and the gain of the amplifier is calculated and plotted over frequency in figure 5.9. A -3-dB frequency was measured at 470 kHz and the line capacitance of the coaxial cable is computed as 330 pF, which matches nicely with the expected value.

Comparing the measured -3dB frequency pole from the coaxial line to the expected -3dB frequency pole from the parasitic capacitance of the SET-drain/HBT-base contact, it can be assumed that the parasitic capacitance imposed on the drain-base node is the dominant pole of the circuit. This dominant pole gives a -3-dB frequency of 113 kHz with the assumption of a 0.7 pF parasitic capacitance and a 2 MΩ SET resistance. The parasitic capacitance and SET resistance is estimated from measurement results and figures reported in literature [8]. Furthermore, this -3-dB frequency is much lower than the 1 MHz goal, set at the beginning of the chapter, meaning that the bandwidth of 1 MHz will not be achieved in this project. This -3-dB frequency of the SET-drain/HBT-base contact can be further enhanced by reducing the parasitic capacitance of the drain-base node by directly wire-bonding from the drain to the base of the two samples or by further integrating the HBT with the SET sample. However, this would mean that the drain-base parasitic capacitance would have to be reduced to below 200 fF with the presumed SET resistance to achieve the 1 MHz bandwidth, therefore, the predefined goal of a 1 MHz bandwidth is not feasible for the project of this thesis.

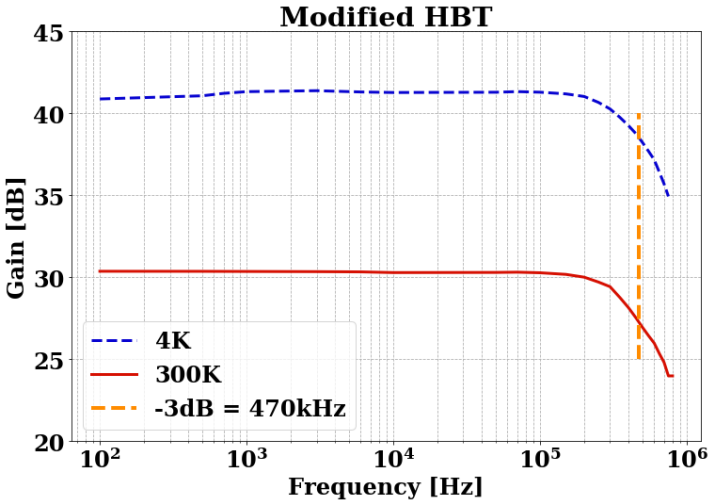


Figure 5.9: Frequency response of the modified HBT in the measurement set-up

5.2.3. Noise analysis

The noise sources that need to be examined are the shot noise of the SET and HBT, as well as the input noise of the room temperature amplifier and the thermal noise of the amplifier's resistor used for current to voltage conversion. To examine the noise sources of the HBT amplifier, the noise sources are added to the small-signal model in figure 5.8. The base shot noise and the SET shot noise are parallel to the base-emitter contact and the collector shot noise is parallel to the collector-emitter contact. To simplify the interpretation of the

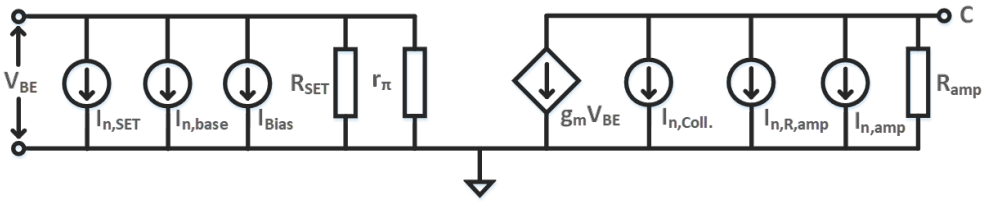


Figure 5.10: Small signal model with noise sources of the HBT amplifier interfaced with the SET

noise in this section, the calculations of the noise sources are referred to the collector node. The shot noise of the SET and the base of the HBT can be examined in parallel since they share the same biasing current. The noise is calculated with equation 5.6, where q is the elementary charge of an electron, I_{Bias} is the DC biasing current, determined by the biasing voltage of the amplifier (V_E). The noise is then referred to the collector by multiplying the noise by the extrinsic gain (Gain) at the respective biasing current (Calculated in section 5.2.1).

$$I_{n,SET,out} = I_{n,Base,out} = \sqrt{2 \cdot q \cdot I_{Bias}} \cdot Gain_{HBT} \tag{5.6}$$

The collector shot noise is calculated with the same method as the SET and the base shot noise (Eq. 5.7.

$$I_{n,Collector} = \sqrt{2 \cdot q \cdot I_C} \tag{5.7}$$

The input resistance of the room temperature amplifier (R_{amp}) produces a thermal noise which is calculated with equation 5.8, where the k_B is the Boltzman constant, T is the temperature and R_{amp} is the resistance value (1 kΩ). At room temperature (T = 300 K), the current noise of the resistor is 4.07 pA/$\sqrt{\text{Hz}}$, which can be further reduced to 480 fA/$\sqrt{\text{Hz}}$ by placing the resistor at the measurement temperature (4.2 K).

$$I_{n,Ramp} = \sqrt{\frac{4 \cdot k_B \cdot T}{R_{amp}}} \tag{5.8}$$

The total current noise can then be calculated, using equation 5.9.

$$I^2_{n,total} = I^2_{n,SET,out} + I^2_{n,Base,out} + I^2_{n,Collector} + I^2_{n,Ramp} + I^2_{n,amp} \tag{5.9}$$

In figure 5.11, the noise sources are individually plotted over the collector current (Noise was only plotted for one device due to similarity). The noise for the 1 kΩ resistor is calculated at 4 K temperature. In the figure, the amplifier noise is seen to be the dominant noise source at lower Power (Power ≈ I_C), but at the relevant power (within the "Operating region", yellow area, which is determined by the biasing current through the SET), the SET and base shot noise become the dominant noise source.

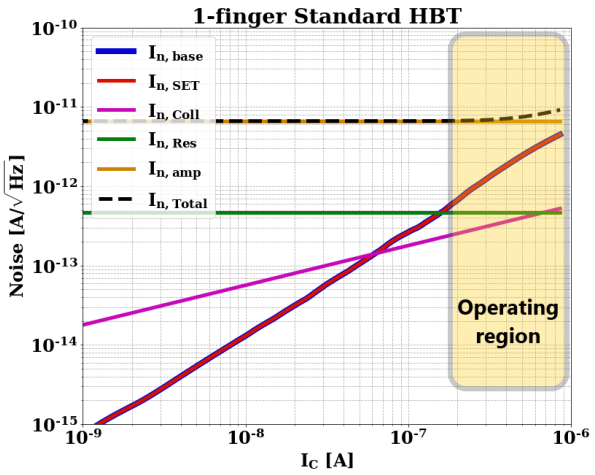


Figure 5.11: Current noise of the HBT amplifier referred to the input of the room temperature amplifier

5.2.4. Readout method

As mentioned in section 5.2, phase 3 of the readout is the phase of interest and the readout method is the tunnel-rate selective readout. The readout phase can be split into 2 time frames: t_{delay}, which is the time it takes for the signal to be distinguishable as a spin-singlet ground state or spin-triplet state, and t_{int}, the time it takes to average the signal for a desired SNR. These two variables add up to a total readout time of t_{total}. An example of such output signal can be seen in figure 5.12, which shows 100 readout traces and the separation of the two spin-states occurring at roughly 4 μs.

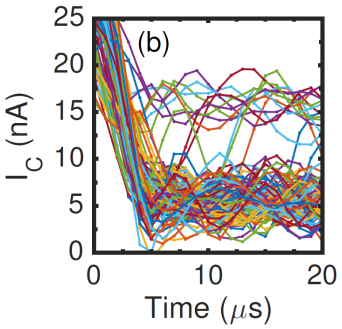


Figure 5.12: An example of 100 single shot readout traces for a tunnel-rate selective readout [58]

The delay time (t_{delay}) is reliant on the bandwidth of the signal and can be estimated from the rise time of the pulse. First, the time constant is calculated (Eq. 5.10) from the -3-dB bandwidth and from there, the rise time is calculated (Eq. 5.11) and assigned as the delay time, t_{delay}.

$$\tau = \frac{1}{2 \cdot \pi \cdot f_{-3dB}} \tag{5.10}$$

$$t_{delay} = t_{rise} = \approx 2.2 \cdot \tau \tag{5.11}$$

$$t_{signal} = t_{total} + t_{delay} \tag{5.12}$$

The signal amplitude from the SET measurements in section 5.1.4 is stated as 100 pA to 130 pA. The measurements are performed at 4.2-K temperature but the amplitude can be estimated to be in the same range at mK-temperatures (Dilution refrigerator), therefore, it will remain as the input amplitude range for the ongoing calculations. Further calculation of the SNR is done by waiting for a certain amount of time (t_{delay}) and then averaging the signal for additional time period (t_{signal}), summing up to the total measurement time (t_{total}) and the averaged signal over the total measurement time is calculated using equation 5.13.

$$I_{rms} = I_{amplitude} \cdot \frac{t_{signal}}{t_{total}} \tag{5.13}$$

5.2.5. SNR and Power

Having obtained the necessary calculations from the above paragraphs, the estimated SNR can be computed. Before SNR calculations can commence, several important parameters have to be established.

- Biasing current of 1 nA through the SET from section 5.1.2, to keep the voltage over the SET below the charging energy.
- SET resistance of 2 MΩ from section 5.2.1, estimation based on measurements and reported values from literature.
- Bandwidth of 113 kHz from section 5.2.2, calculated from an estimated parasitic capacitance of 700 fF on the drain-base node.
- Signal amplitude of 100 pA from section 5.2.4, estimation based on measurements and observed values in literature.

With an established signal amplitude of the SET the output signal can be referred to the output of the room temperature amplifier with equation 5.14, where I_{rms} is the averaged signal over the measurement time, $Gain_{HBT}$ is the extrinsic gain of the HBT amplifier, R_{amp} is the 1 kΩ resistor for the current-to-voltage conversion and $Gain_{amp}$ is the voltage gain of the room temperature amplifier.

$$V_{out} = I_{rms} \cdot R_{amp} \cdot Gain_{HBT} \cdot Gain_{amp} \tag{5.14}$$

Likewise, the total integrated voltage noise, referred to the output of the room temperature amplifier, can be calculated using equation 5.15. Where $V_{n,total}$ is the accumulated voltage noise referred to the HBT collector node (Eq. 5.9), $Gain_{amp}$ is the room temperature amplifier gain, R_{amp} is the 1 kΩ resistor for the current-to-voltage conversion, and $\sqrt{BW}$ is the estimated bandwidth.

$$V_{n,out} = I_{n,total} \cdot R_{amp} \cdot Gain_{amp} \cdot \sqrt{BW} \tag{5.15}$$

The power dissipation of the HBT amplifier lies mainly on the collector current due to it being much larger than the base current. The HBT is biased at a V_{CB} = 0 V, hence the base-emitter voltage can be assumed to be the same as the collector-emitter voltage. The power dissipation is calculated using equation 5.16.

$$Power = V_{CE} \cdot I_C + V_{BE} \cdot I_B \tag{5.16}$$

The signal-to-noise ratio can finally be computed with equation 5.17.

$$SNR = 20log\left(\frac{I_{out}}{I_{n,out}}\right) \tag{5.17}$$

For the estimated parameters, mentioned above, the SNR is plotted over the power dissipation (Fig. 5.13). The extracted measurement results of the 3 HBT devices are utilized in the aforementioned calculations and the used as a demonstration of their performance. As mentioned in section 3.1.3, only low current measurement were performed on the 1-finger HBT, which explains the discontinuation of the curve (Pink/Purple curve).

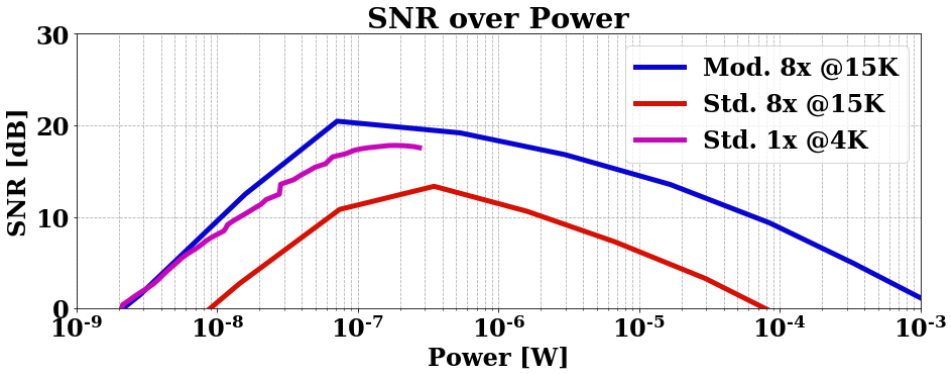


Figure 5.13: SNR over power dissipation for a single-shot readout

Additionally, the SNR over the total measurement time of a single-shot readout is plotted (Fig. 5.14). A constant delay time (t_{delay}) of 3.08 μs is established from calculations in section 5.2.4 and the integration time (t_{int}) is swept from 0 to 15 μs. In the graph, the calculations for the modified 8-finger device and the standard 1-finger device show good performance, where at a total measurement time of 6 μs an SNR > 10 dB is observed. However, the standard 8-finger device shows significant attenuation in the SNR compared to the other 2 devices. This is due to the biasing current, of 1 nA, being too low for the maximum SNR of the device, discussed in the following paragraph. The power dissipation of the three HBTs under these biasing conditions are 484 nW, 14 nW, and 175 nW for the modified 8-finger device, standard 1-finger device, and standard 8-finger device, respectively which can be changed further by increasing or decreasing the biasing current.

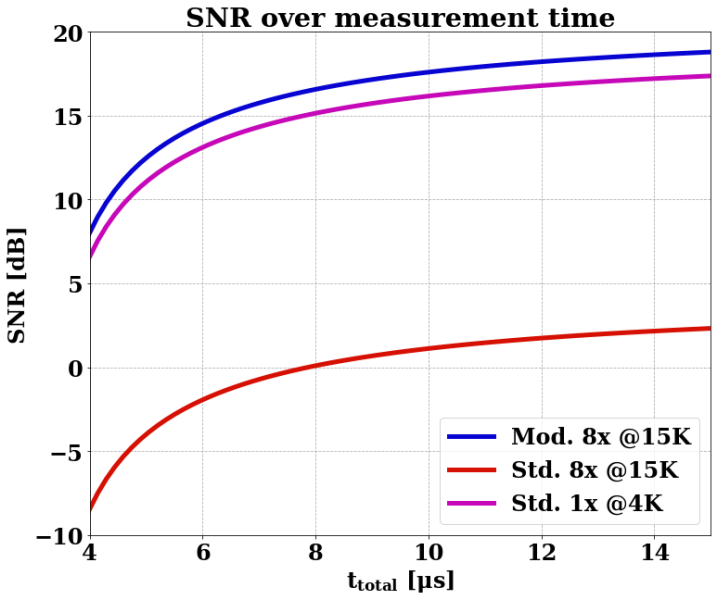


Figure 5.14: SNR over total measurement time for a single-shot readout, estimated for a biasing current of I_{SET} = 1 nA.

The lack of performance in the standard 8-finger device is investigated further by plotting the SNR over the base current of all devices to see the optimal biasing current for the maximum SNR (Fig. 5.15). As can be seen, the peak SNR for the modified 8-finger device and the standard 1-finger device occurs at a biasing current of 1 nA while for the standard 8-finger device, the peak SNR is at a biasing current of 3 nA. An instinctive approach to the solution would be to simply raise the biasing current of the SET. However, raising the biasing current for a better SNR increases the voltage potential over the SET which further decreases the signal amplitude due to the SET-voltage approaching the charging energy of the SET. Therefore, the standard 8-finger device is considered the worst performing HBT out of the three that were chosen. These results should be taken with consideration of a change in the estimated parameters, mentioned at the beginning of the section, which can vary and therefore would change the performance of the amplifier.

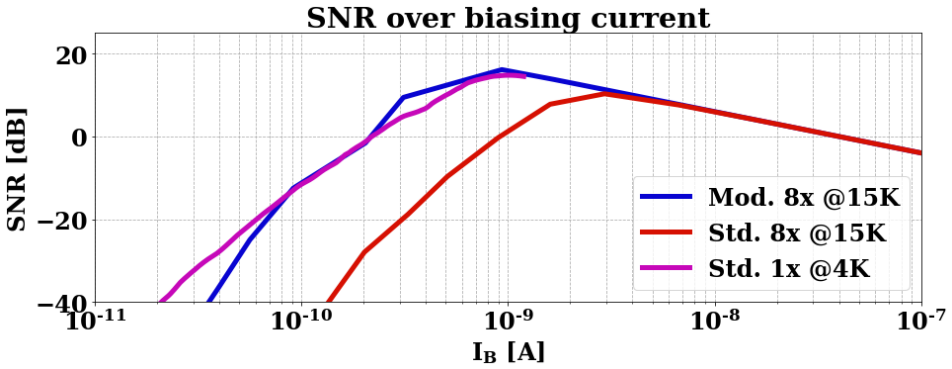


Figure 5.15: SNR over the HBT amplifier biasing current for a single-shot readout, showing the optimum biasing point of each HBT device

The aforementioned estimation of the single-shot readout shows similar performance to the state-of-the-art readout performance reported in [8]. Where an SNR above 7 is achieved in times less than 10 μs, similar to the results presented in figure 5.14, where an SNR of above 10 is observed at a total measurement time of 5 μs. Additionally, the power dissipation compares well with literature, with the dissipation of P $\approx$ 50 - 500 nW. It should also be emphasized that the results in [8] are from single-shot measurements while the results presented in this thesis is an estimation from measurement results of the circuit components (SET and the HBTs).

6

Conclusion and Future Work

6.1. Conclusion

This thesis has resulted in 3 main achievements.

1. A comprehensive cryogenic characterization of the 0.13 μm BiCMOS technology from IHP, of which three versions of SiGe HBTs, thin and thick oxide NMOS/PMOS, and multiple poly and metal integrated resistors were characterized.
2. The characterization of a silicon MOS based single-electron transistor at 4 K-temperature as well as a demonstration of the process of bringing up coulomb oscillations.
3. The three different SiGe HBTs in the respective technology, interfaced with the single-electron transistor, are analyzed as viable devices for a cryogenic amplifier in a single-shot readout of DC spin qubits.

Characterization

SiGe HBT devices chosen for this project are a 1-finger and 8-finger SiGe HBT fabricated in the standard SG13G2 technology, as well as the 8-finger SiGe HBT fabricated using a process modification of the SG13G2 technology. The measurement results show an increase in the peak current gain at cryogenic temperature (2.5x for standard, 5x for modified), lower input resistance, and higher transconductance. The modified HBT showed an attainable current gain of 10 @240 pW, 100 @4.4 nW, and 1000 @136 nW.

CMOS devices chosen for this project are both thin oxide (core) and thick oxide (I/O) NMOS and PMOS devices with several extreme aspect ratios (W/L) as well as intermediate-size devices or experimental devices, with gate widths of core devices ranging from 0.12μm to 10μm. The measurement results show the common cryogenic traits observed in literature, which include increased threshold voltage ($\Delta V_{th} \approx 150$mV), output current ($\Delta I_D \approx 30\%$), transconductance ($\Delta g_m \approx 30\%$) and output conductance ($\Delta g_o \approx 30\%$) and a decreased subthreshold swing ($\Delta SS \approx 63$mV/dec) for devices with high aspect ratios (W/L).

Resistors chosen for this project are a variation of silicided and unsilicided, N+ and P+ PolySilicon resistors as well as metal resistors in the metal 1 layer and metal 2 layer of the technology. The measurement results show that the resistance of the unsilicided P+ PolySilicon resistors remains unchanged and is independent of temperature, while the resistance of the unsilicided N+ PolySilicon resistors scales up by a factor of 2x at 4 K. The resistance of the silicided N+ PolySilicon resistors decreases at 4 K with the sheet resistance showing dependency on the resistor dimension and temperature. The metal resistors of metal 1 and metal 2 both decrease by a factor of roughly 7x at 4-K temperature.

Cryogenic SiGe amplifier

Chapter 5 presents the analysis and comparison of the three SiGe HBTs, previously characterized, as devices for a cryogenic readout amplifier of DC spin qubit. Bandwidth analysis shows that the dominant pole (estimated as $f_{-3dB} \approx 113$ kHz) of the system is located at the interconnecting line between the SET and the HBT.

Analysis of the noise sources shows that, with respect to power dissipation, the dominant contribution at the appropriate region of operation (0.4 μW to 1 μW) comes from the current shot noise of the SET and the base current shot noise of the HBT. At any lower power dissipation, the amplifier residing at room temperature becomes the dominant noise source. The results of the total analysis show that under the same biasing conditions, a capable SNR of higher than 10 dB in a total measurement time of 6 μs for the modified 8-finger HBT and the standard 1-finger HBT, while the standard 8-finger HBT showed an SNR of below 0 dB in the same time frame. These results show similar performance to the state-of-the-art readout performance reported in [8]. Where an SNR above 7 is achieved in times less than 10 μs. Additionally, the power dissipation compares well with literature, with a dissipation of P $\approx$ 50 - 500 nW compared to a 0.1 - 1 μW in [8].

In the analysis, the parasitic capacitance of the interconnecting line between the SET and the HBT is estimated as 0.7 fF and should be taken into consideration when evaluating the overall analysis. This capacitance is the main bottleneck of the system, as it decreases the readout bandwidth of the system. The capacitance relies heavily on the implementation of the measurement set-up, which in this project, is implemented as a PLCC-to-PLCC package set-up, where the SET and the HBT samples reside in different PLCC packages and rely on bond wires and a PCB trace as the interconnection.

6.2. Future work

Following the conclusions of this thesis, the recommended future steps are listed below:

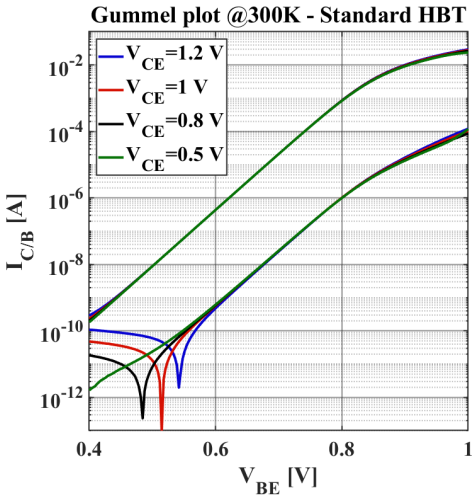
- The implementation of a single-shot readout which includes: Adapting the measurement set-up to a dilution refrigerator for sub-Kelvin measurements; Attaining a new quantum dot device containing both the quantum dot and the charge detecting SET. This enables further measurements and analysis of noise behavior, gain, and bandwidth of the overall system as well as proving or disproving the presented capabilities of the respective SiGe HBT devices.
- Further improvements can be made by employing a sample-to-sample bond wiring scheme, where the interconnecting line between the SET and HBT consists of only a single bond wire. This, however, is a delicate process, as the characteristics and the workings of the SET would not be established beforehand due to the SETs fragile nature towards handling.
- With the established cryogenic performance gains of the 8-finger HBT, fabricated using process modification, being superior compared to the standard fabricated devices. The additional cryogenic characterization of a 1-finger SiGe HBT device of the same fabrication process would be of high interest, expecting a further decrease in the power dissipation while retaining its outstanding current gain.
- More detailed characterization of the SiGe and MOSFET devices, including low- and high frequency noise analysis, frequency behavior, and mismatch.
- Accurate cryogenic models of the characterized devices are needed and would improve further development of the SiGe HBT amplifier as well as other possible cryogenic circuits developed in the respective technology.
- In the long term, the work performed in this thesis shows the possibilities of future integration of cryogenic CMOS readout circuits and SiGe devices, edging the development of quantum computers further towards large scalability. Therefore, a further look into integrating CMOS devices with SiGe devices would be of interest.

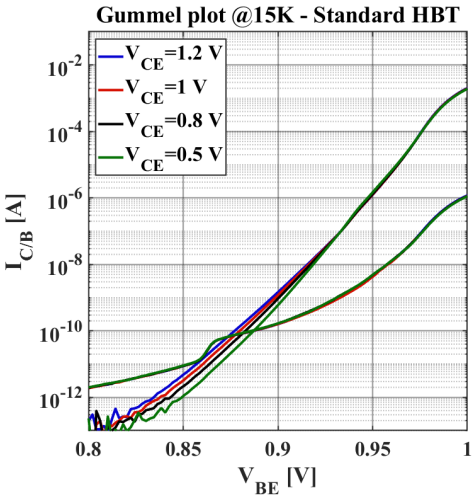
A

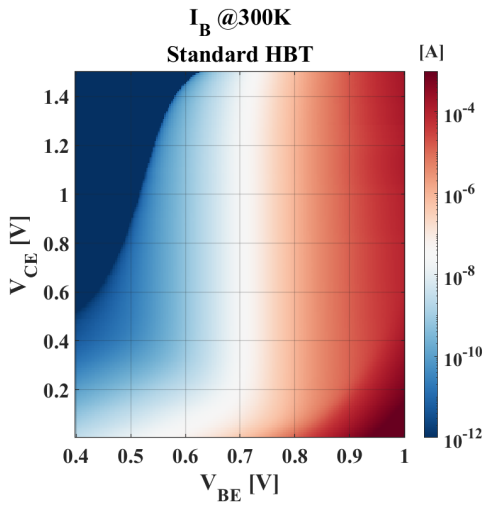
Appendix A

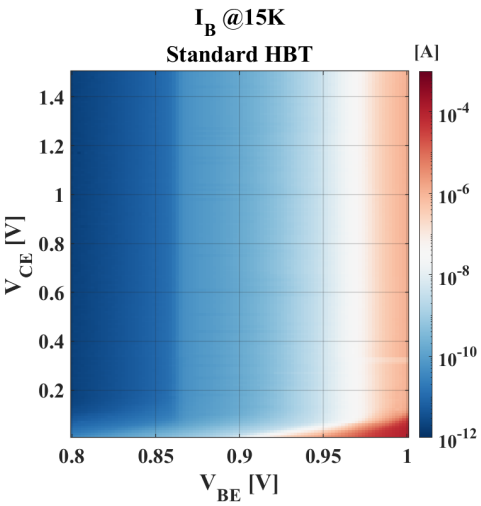
The following figures display the measurement results of the SG13G2 SiGe HBTs in the standard process technology and the modified process technology. Measurements are performed at both 300 K and 15 K in a probe-station set-up. Gummel characteristics are plotted, as well as the colormaps displaying the base and collector current separately.

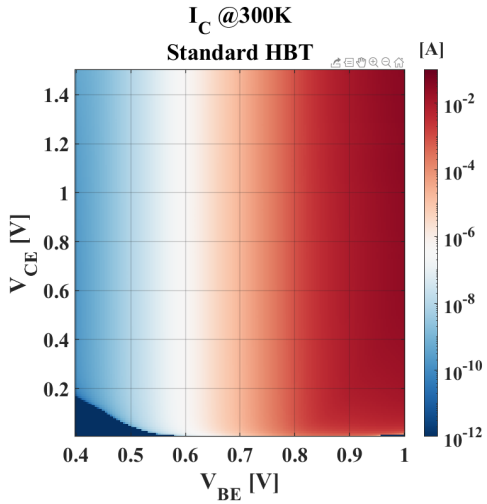
8-finger SiGe HBT fabricated in the standard process

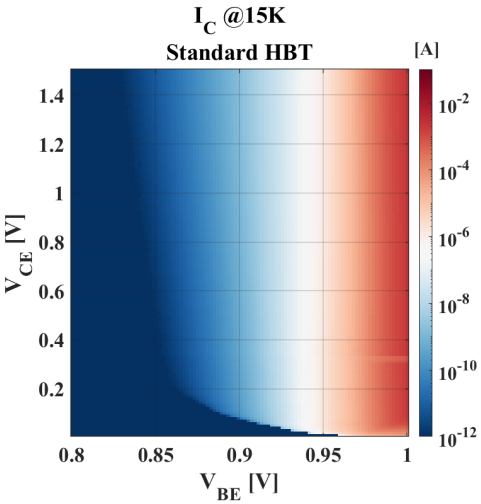


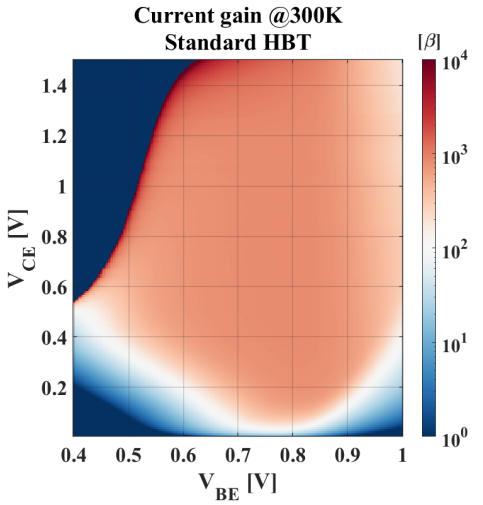


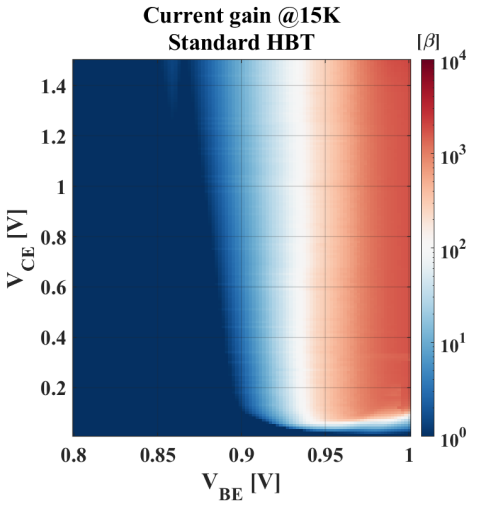









Current gain @300K
Standard HBT
[β]
10^4
10^3
10^2
10^1
10^0
1.4
1.2
1
0.8
0.6
0.4
0.2
V_{CE} [V]
0.4 0.5 0.6 0.7 0.8 0.9 1
V_{BE} [V]


Current gain @15K
Standard HBT
[β]
10^4
10^3
10^2
10^1
10^0
1.4
1.2
1
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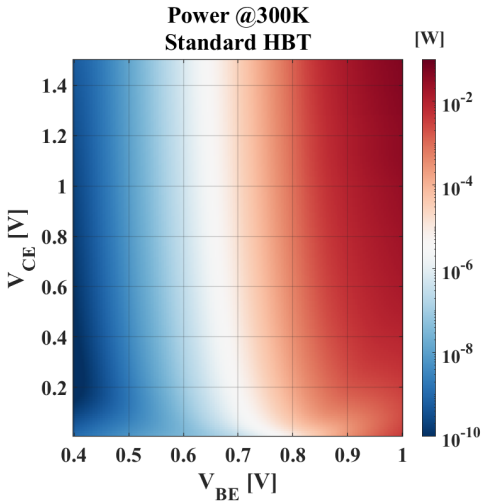
0.6
0.4
0.2
V_{CE} [V]
0.8 0.85 0.9 0.95 1
V_{BE} [V]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10^{-8}
10^{-10}
1.4
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V_{CE} [V]
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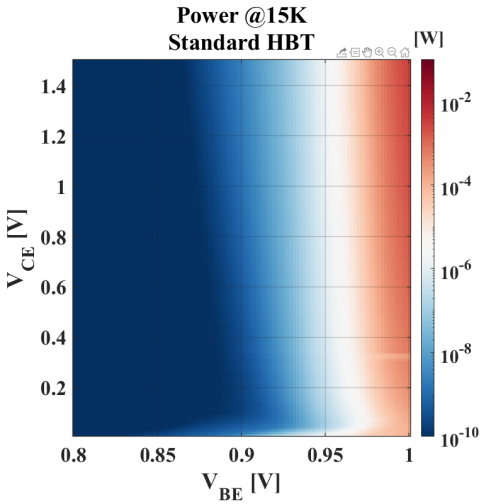
V_{BE} [V]


Power @15K
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V_{CE} [V]
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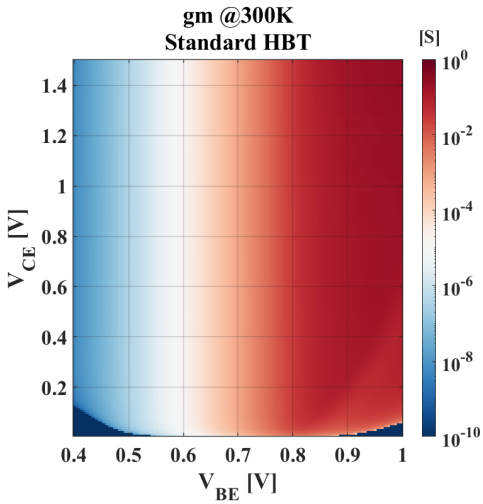
V_{BE} [V]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10^{-8}
10^{-10}
1.4
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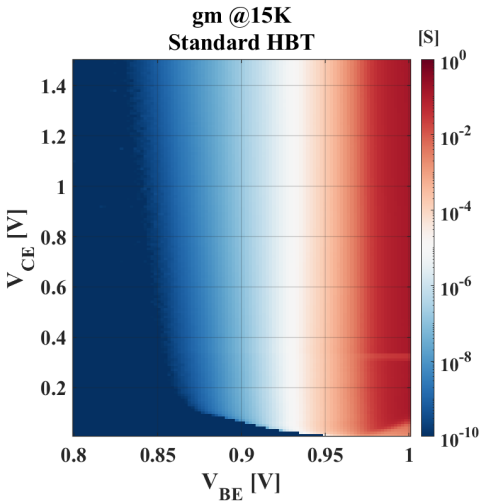
V_{CE} [V]
0.4 0.5 0.6 0.7 0.8 0.9 1
V_{BE} [V]


gm @15K
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V_{CE} [V]
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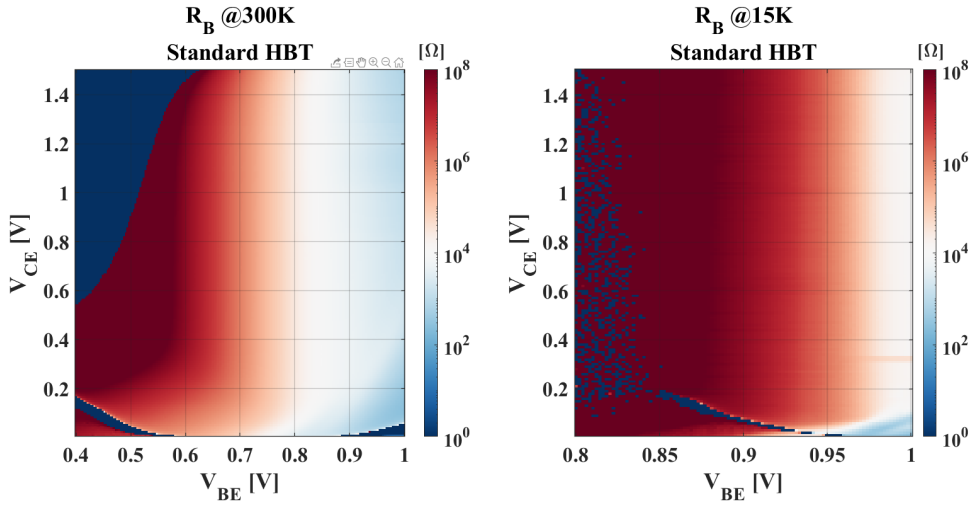
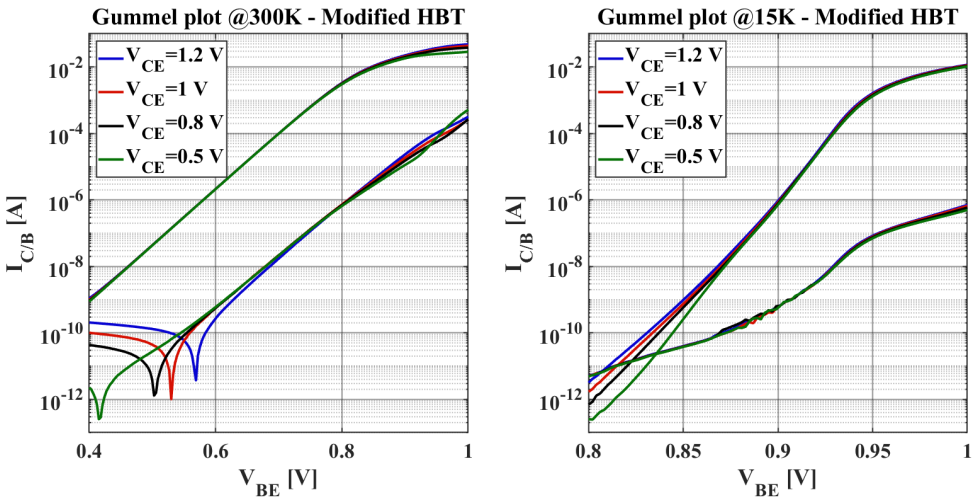
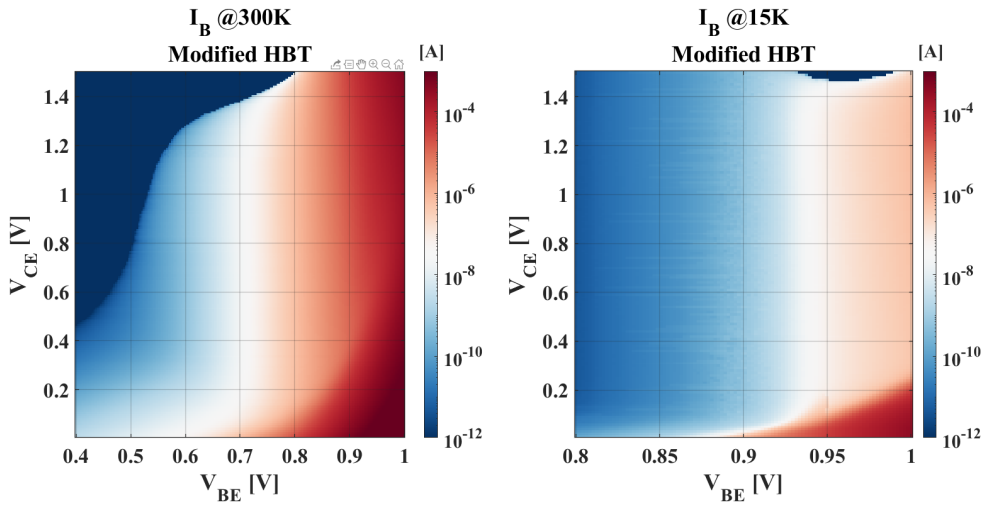
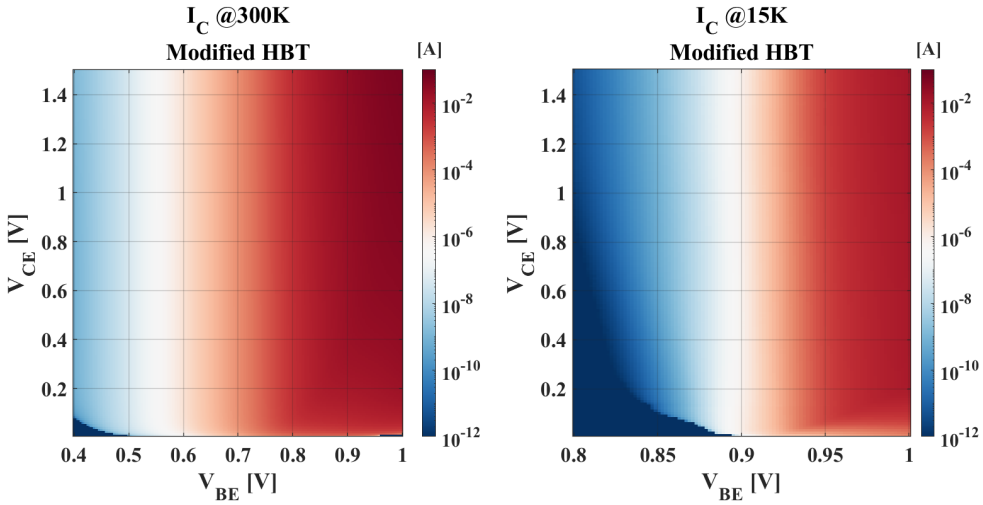
V_{BE} [V]



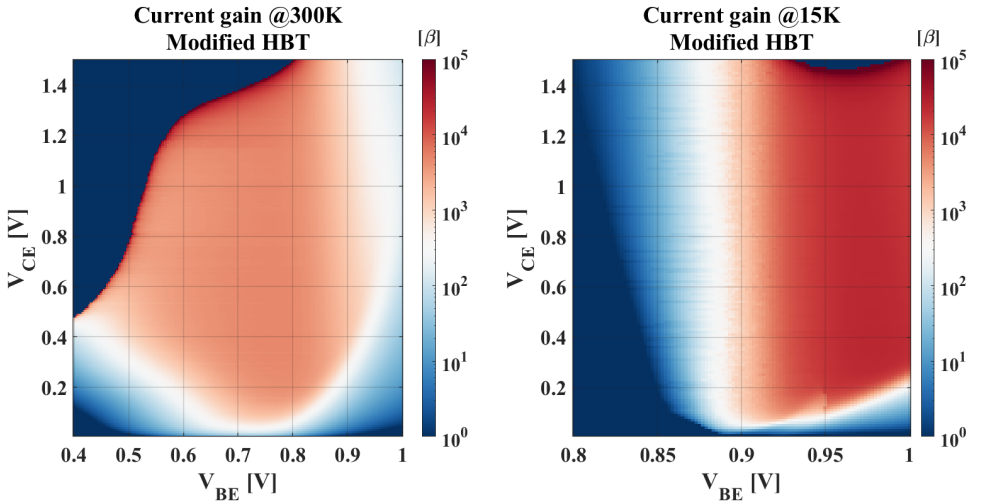
8-finger SiGe HBT fabricated in the modified process



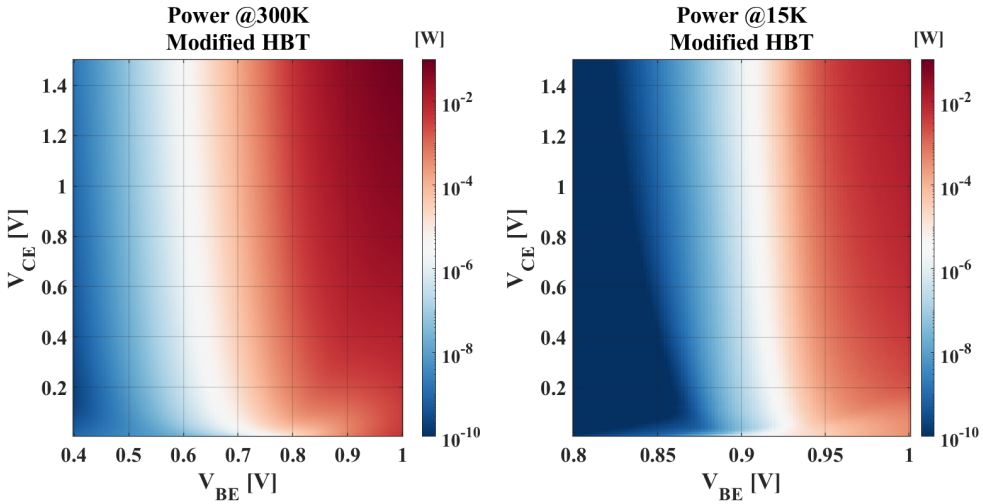



I_C @300K
Modified HBT
[A]
V_CE [V]
V_BE [V]

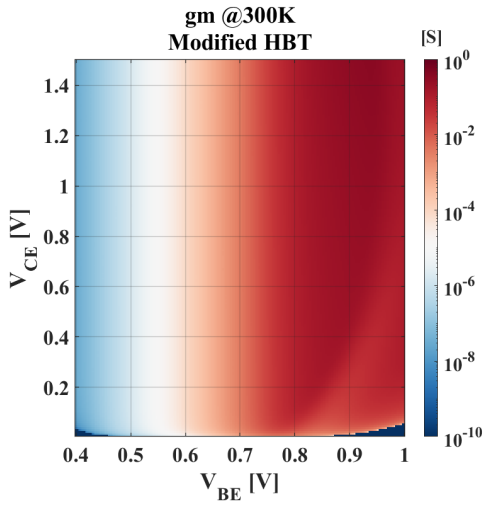
I_C @15K
Modified HBT
[A]
V_CE [V]
V_BE [V]

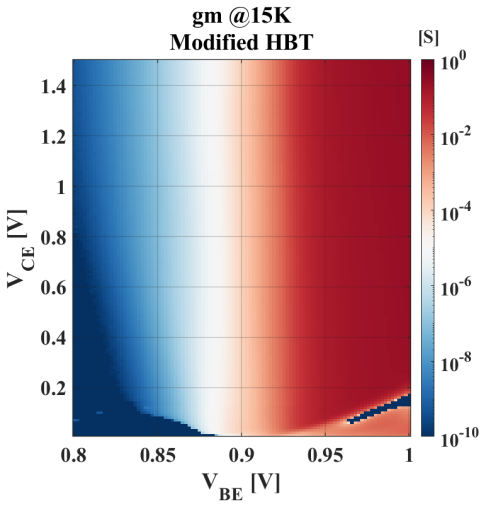

Current gain @300K
Modified HBT
[β]
V_CE [V]
V_BE [V]

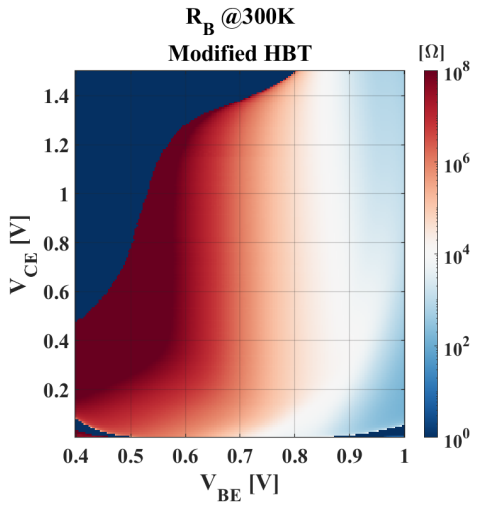
Current gain @15K
Modified HBT
[β]
V_CE [V]
V_BE [V]

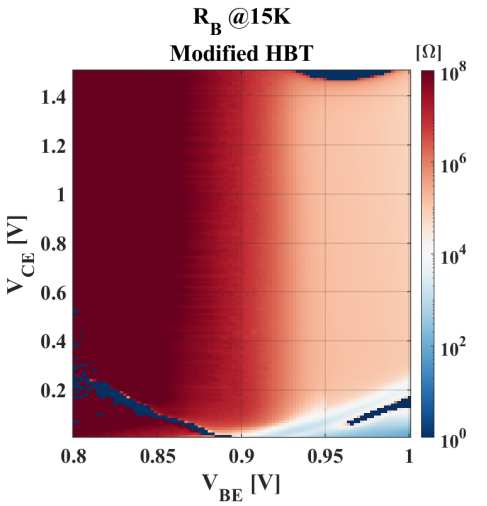

Power @300K
Modified HBT
[W]
V_CE [V]
V_BE [V]

Power @15K
Modified HBT
[W]
V_CE [V]
V_BE [V]


gm @300K
Modified HBT
[S]
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
1.4
1.2
1
0.8
0.6
0.4
0.2
V_{CE} [V]
0.4 0.5 0.6 0.7 0.8 0.9 1
V_{BE} [V]


gm @15K
Modified HBT
[S]
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
1.4
1.2
1
0.8
0.6
0.4
0.2
V_{CE} [V]
0.8 0.85 0.9 0.95 1
V_{BE} [V]


R_B @300K
Modified HBT
[Ω]
10^{8}
10^{6}
10^{4}
10^{2}
10^{0}
1.4
1.2
1
0.8
0.6
0.4
0.2
V_{CE} [V]
0.4 0.5 0.6 0.7 0.8 0.9 1
V_{BE} [V]

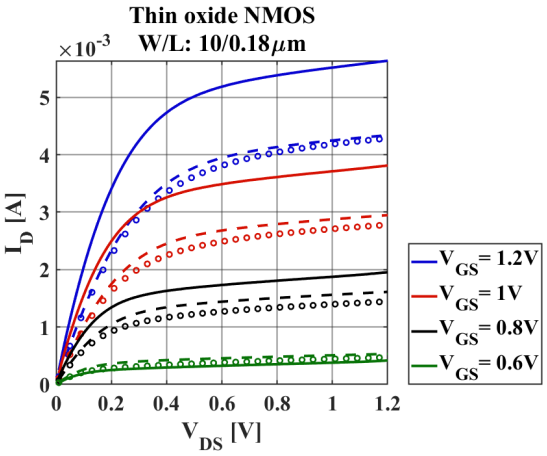

R_B @15K
Modified HBT
[Ω]
10^{8}
10^{6}
10^{4}
10^{2}
10^{0}
1.4
1.2
1
0.8
0.6
0.4
0.2
V_{CE} [V]
0.8 0.85 0.9 0.95 1
V_{BE} [V]

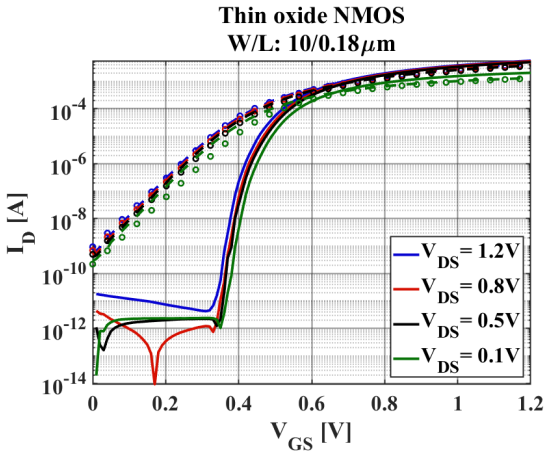
B

Appendix B

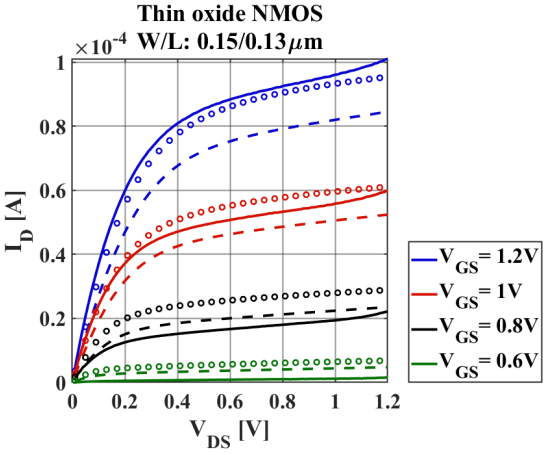
The following figures display the measurement results of the thin and thick oxide MOSFETs in the SG13G2 process technology from IHP. Measurements are performed at both 300 K, 15 K (probe-station set-up), and 4.2 K (dip-stick set-up). Output and transfer characteristics are displayed for each device at a given bias point. Measurement results of devices that are presumed damaged are not displayed.

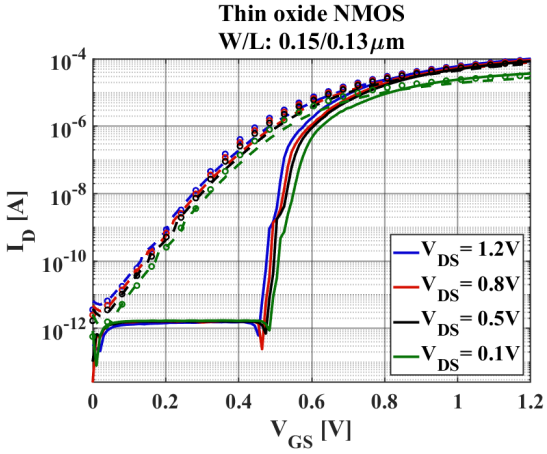
Thin oxide NMOS, Dip-stick set-up



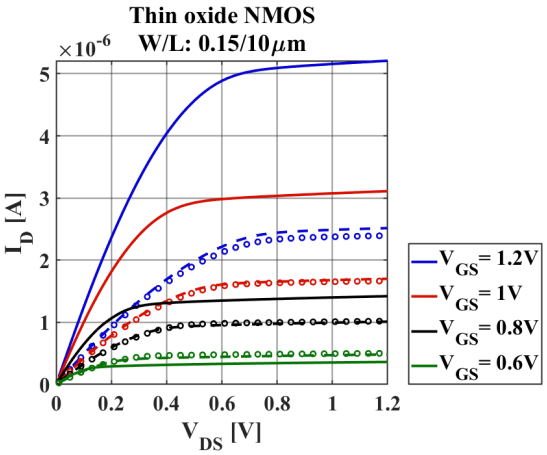


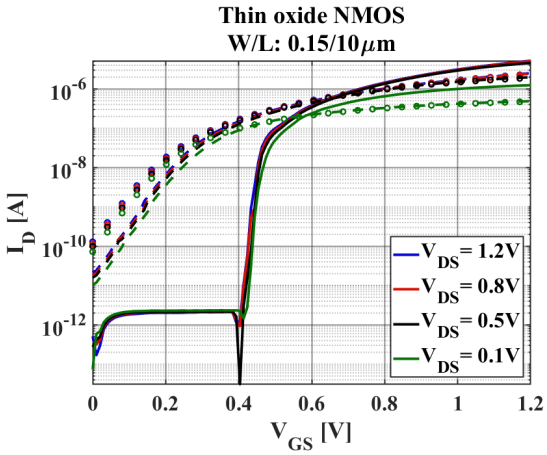
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



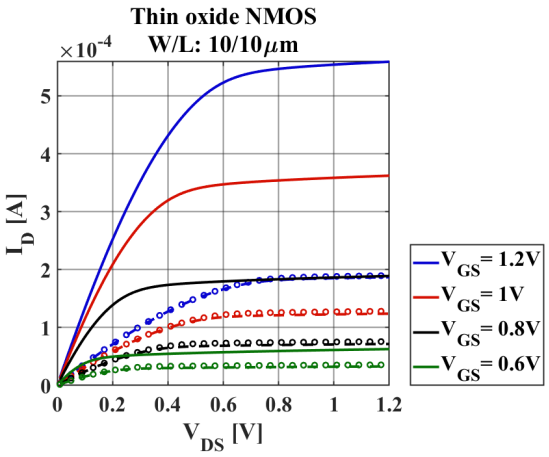


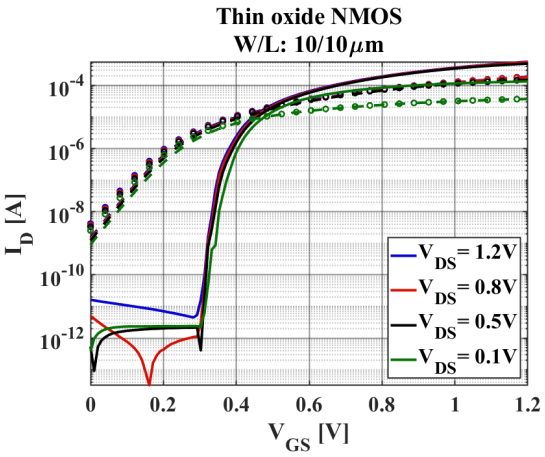
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)





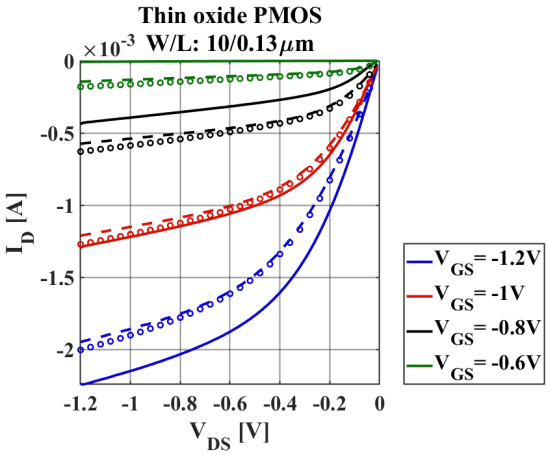
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)

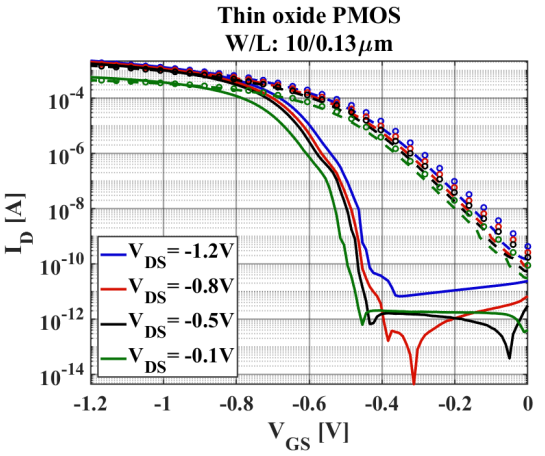




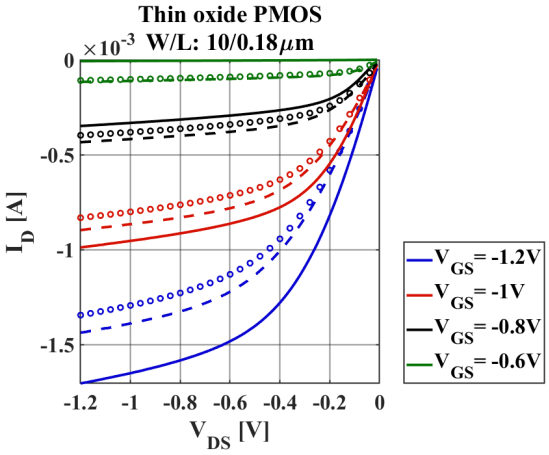
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)

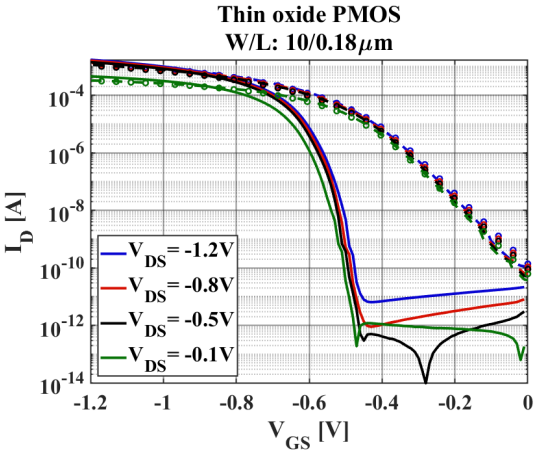
Thin oxide PMOS, Dip-stick set-up



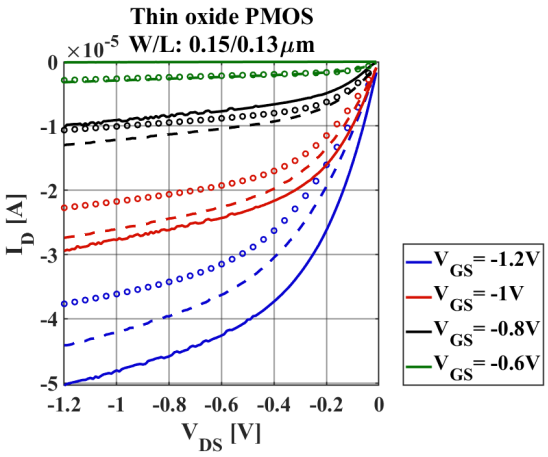


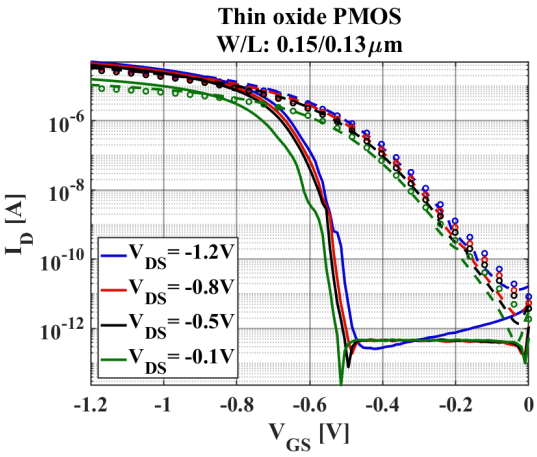
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



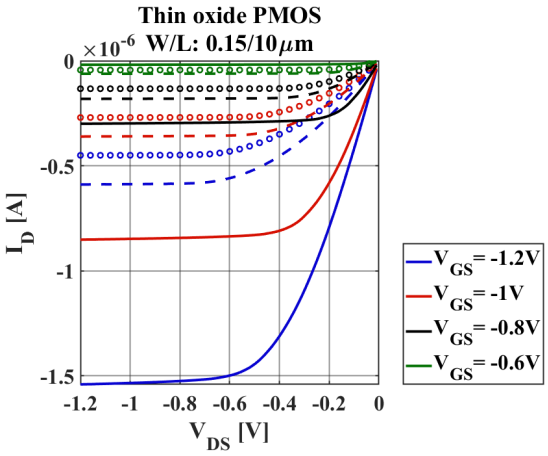


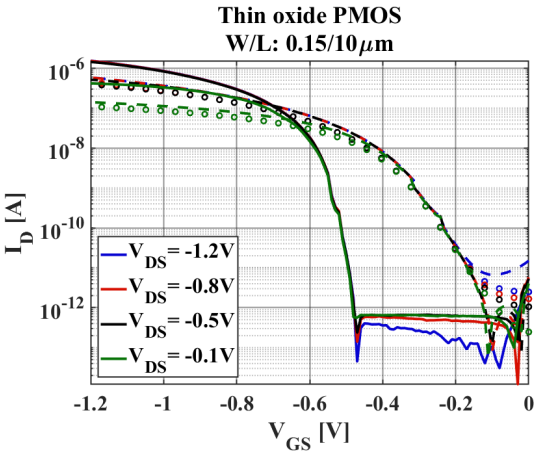
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



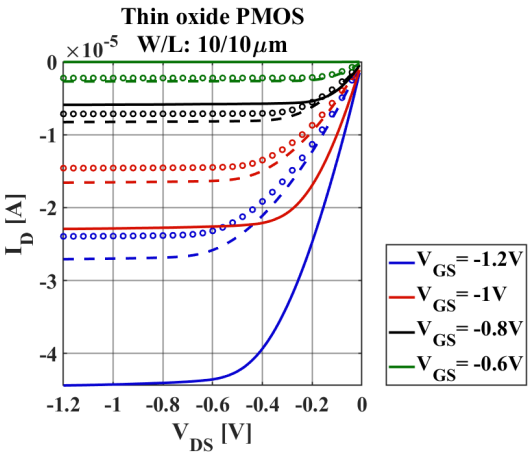


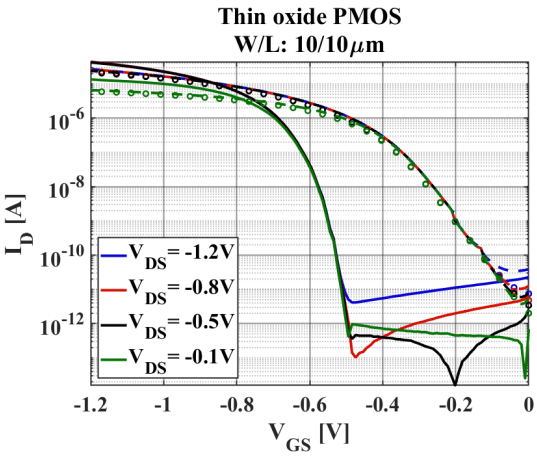
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)





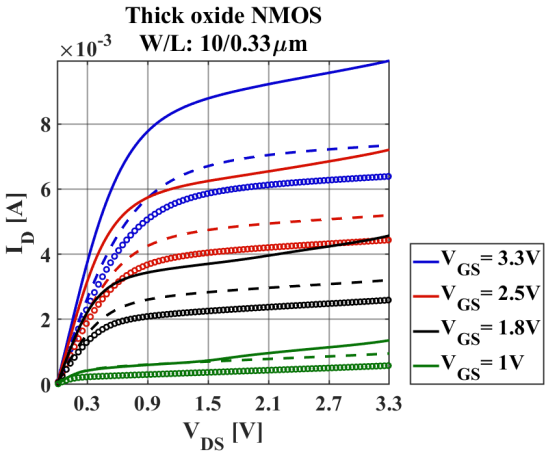
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)

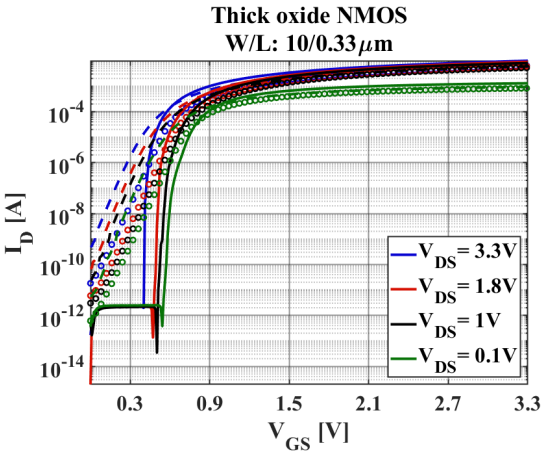




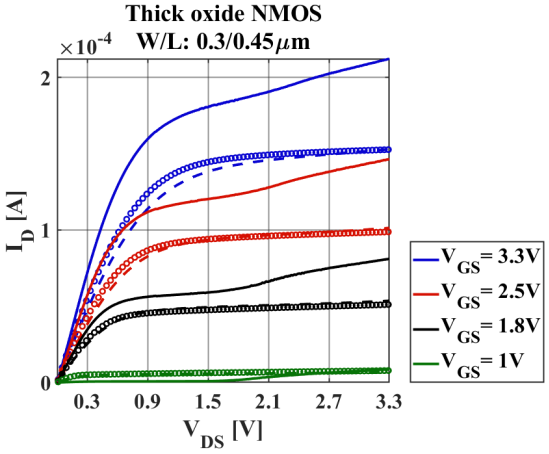
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)

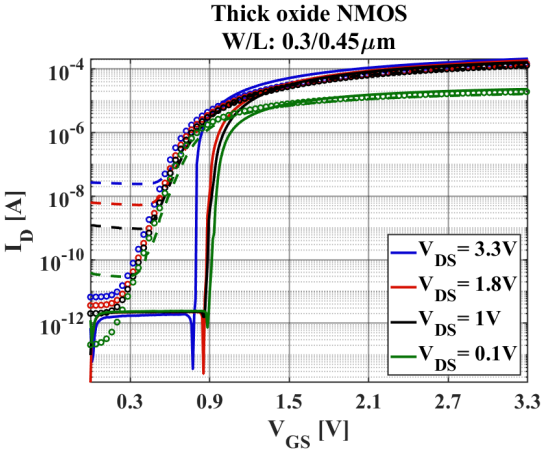
Thick oxide NMOS, Dip-stick set-up



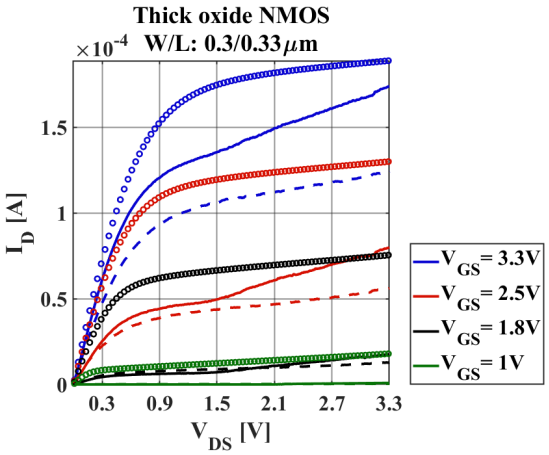


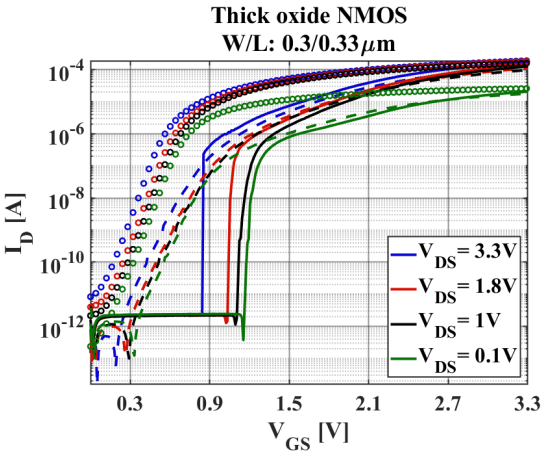
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



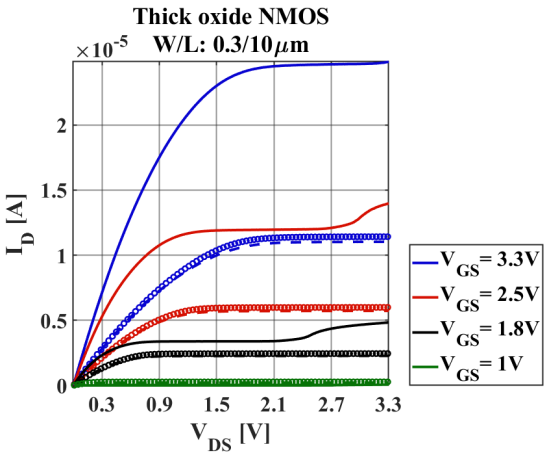


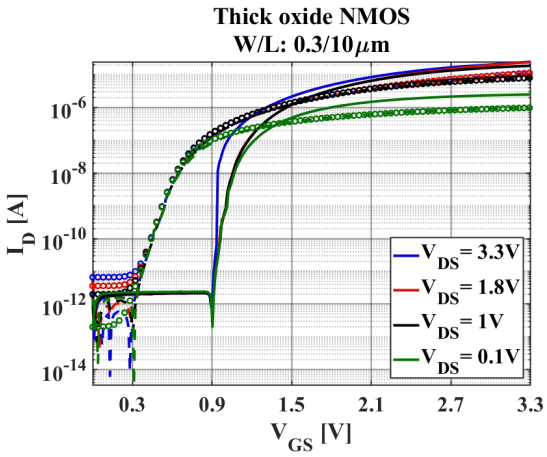
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



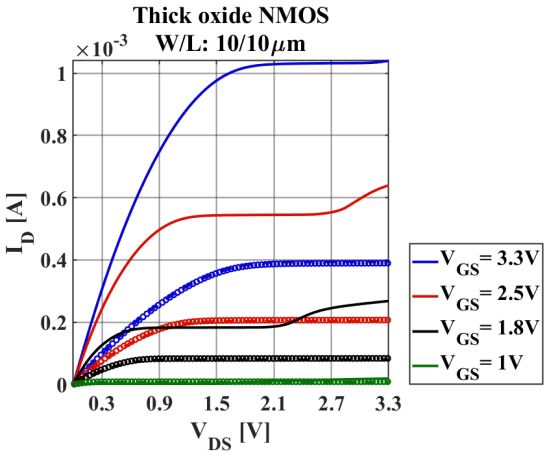


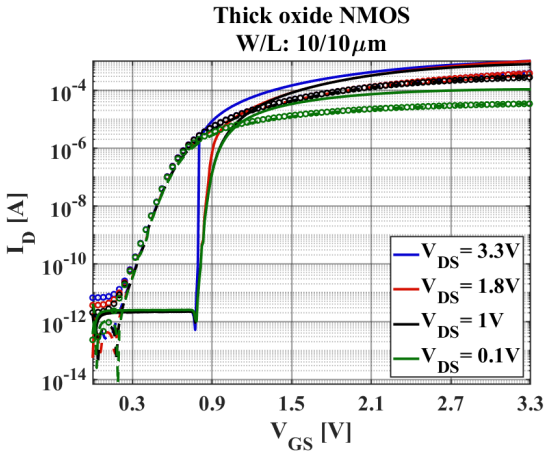
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)





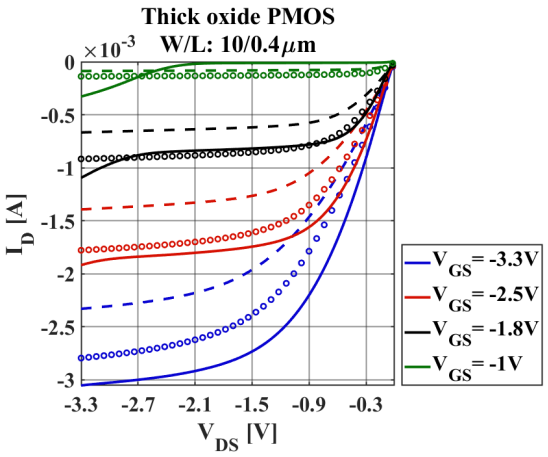
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)

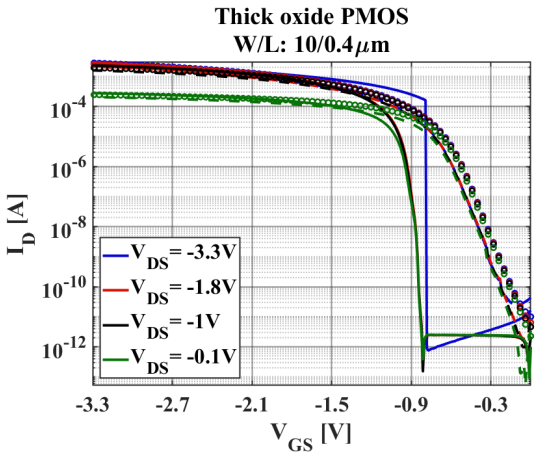




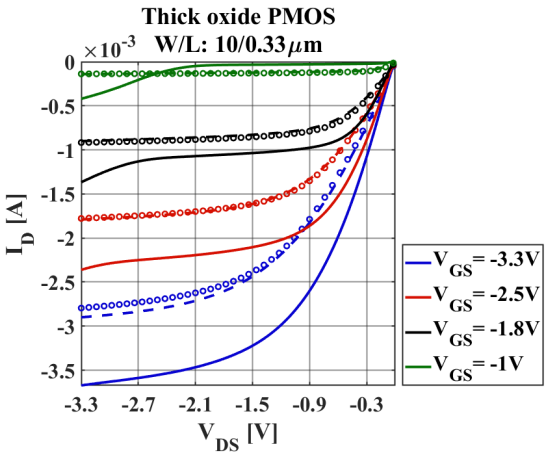
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)

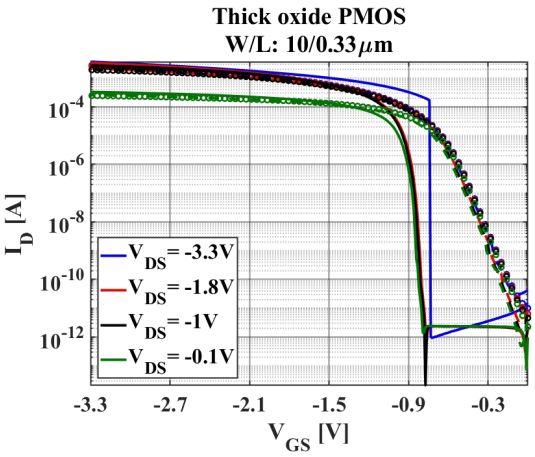
Thick oxide PMOS, Dip-stick set-up



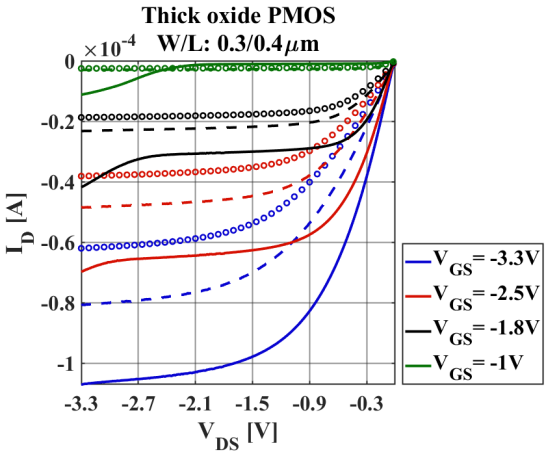


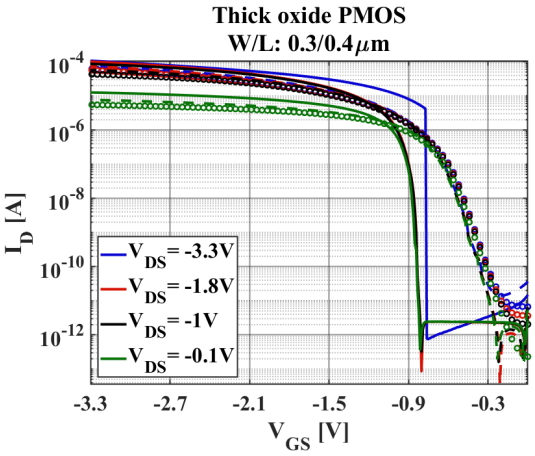
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



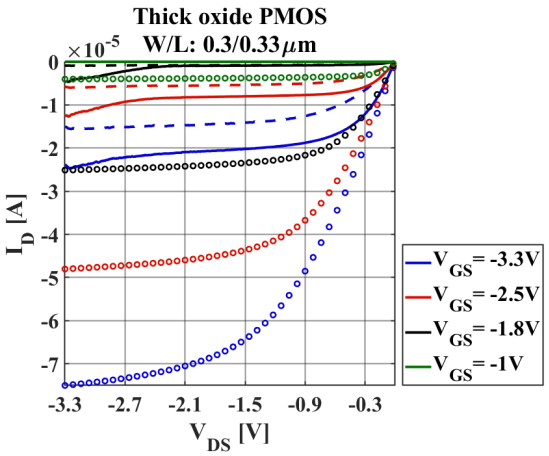


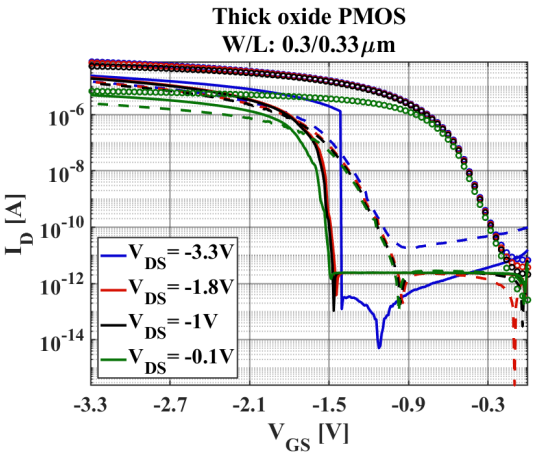
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



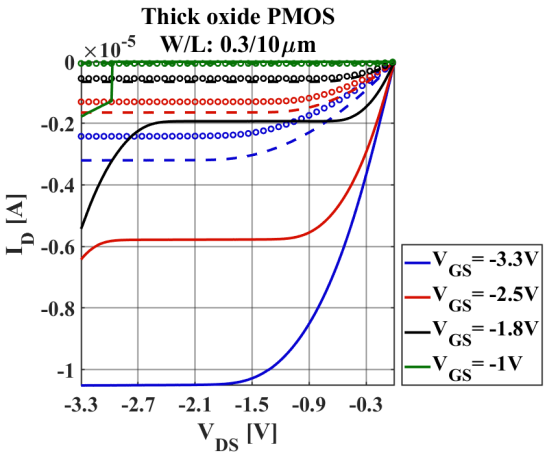


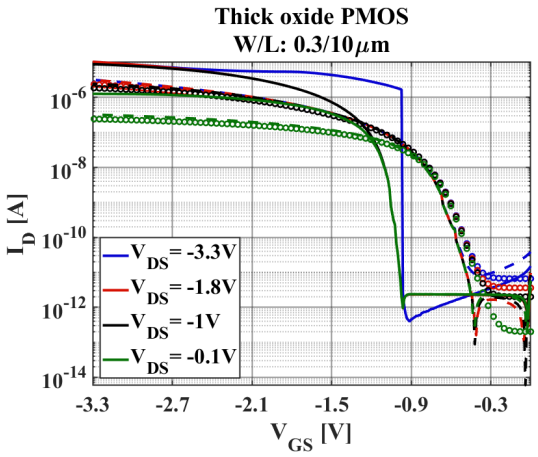
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)



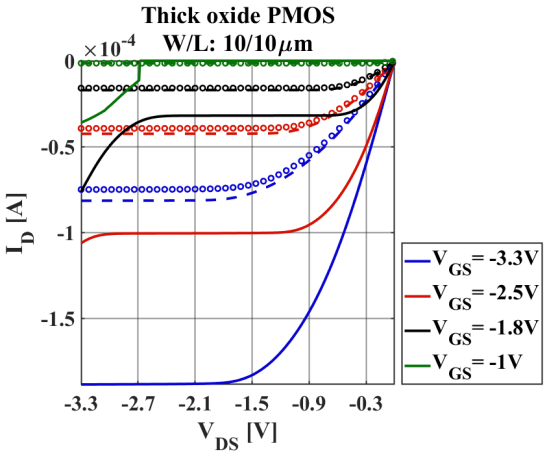


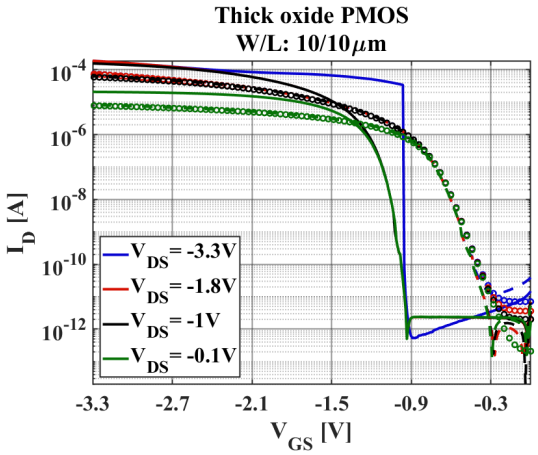
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)





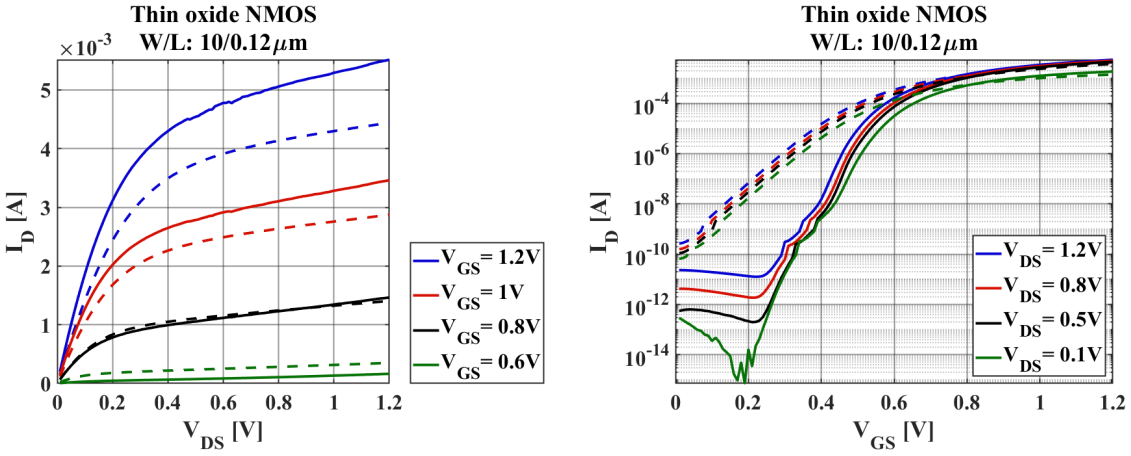
[
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)]



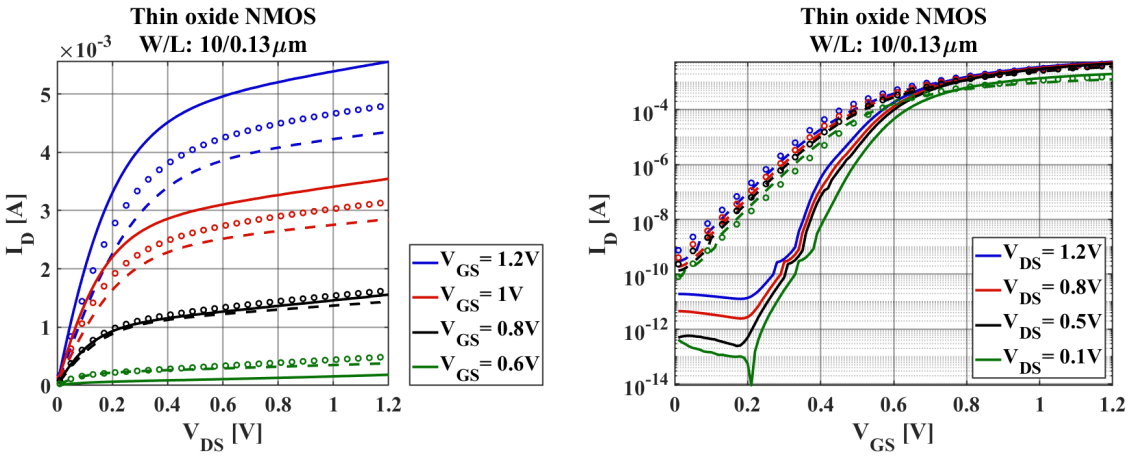


[
300 k (Broken lines), 4.2 k (Solid lines) and simulation (Circles)]

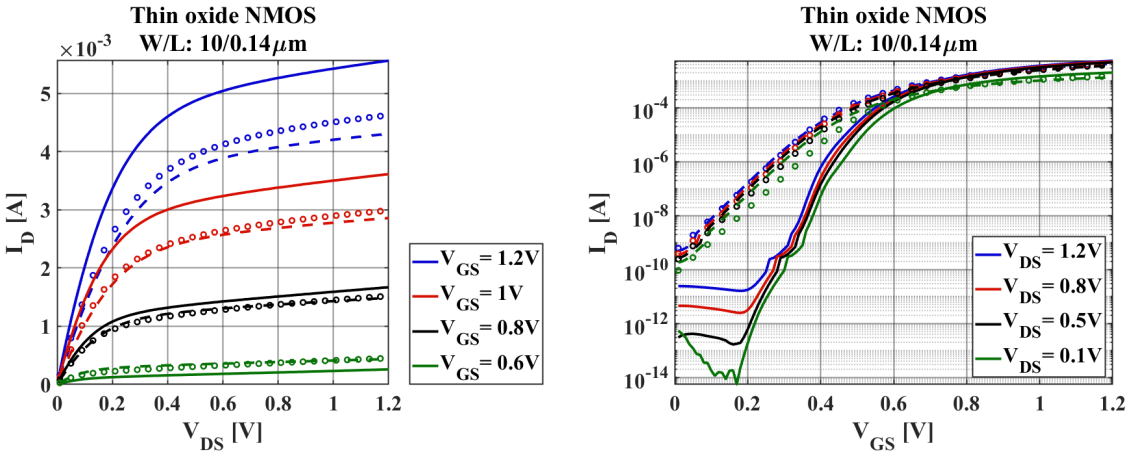
Thin oxide NMOS, Probe-station set-up



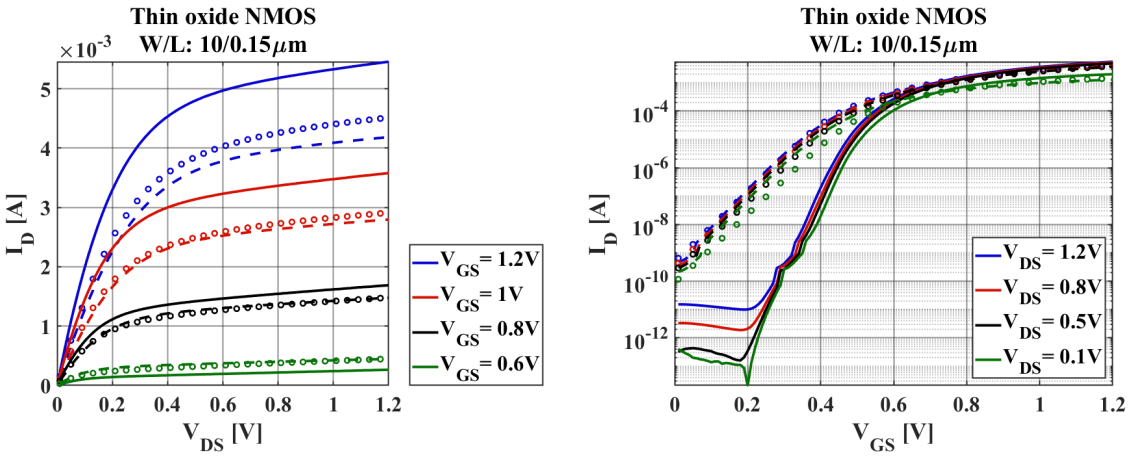
[
300 k (Broken lines), 15 k (Solid lines) and simulation (Circles)]



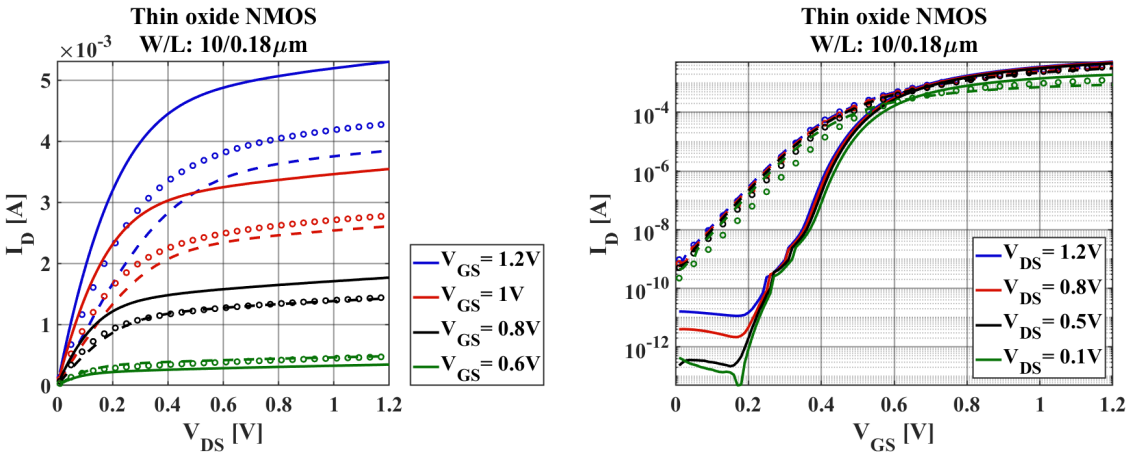
[
300 k (Broken lines), 15 k (Solid lines) and simulation (Circles)]



[
300 k (Broken lines), 15 k (Solid lines) and simulation (Circles)]



[
300 k (Broken lines), 15 k (Solid lines) and simulation (Circles)]



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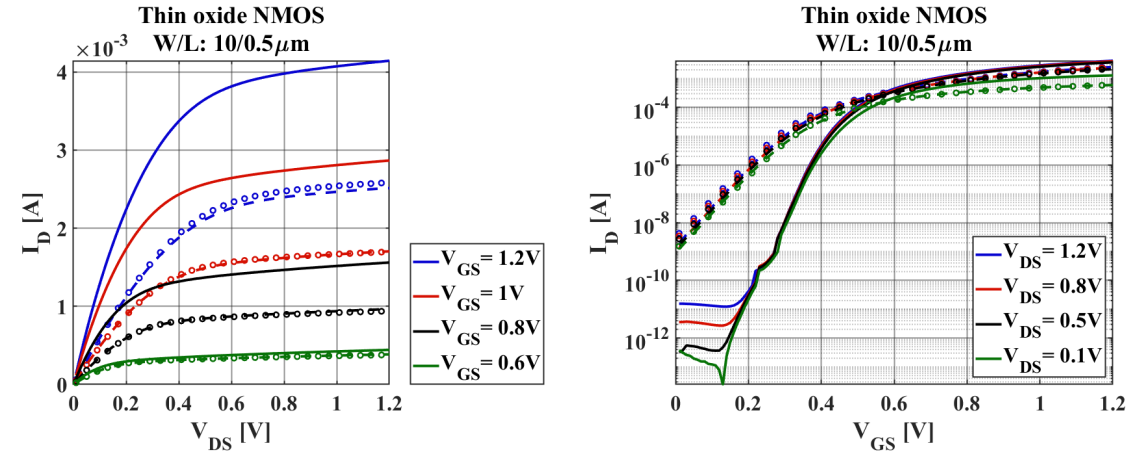

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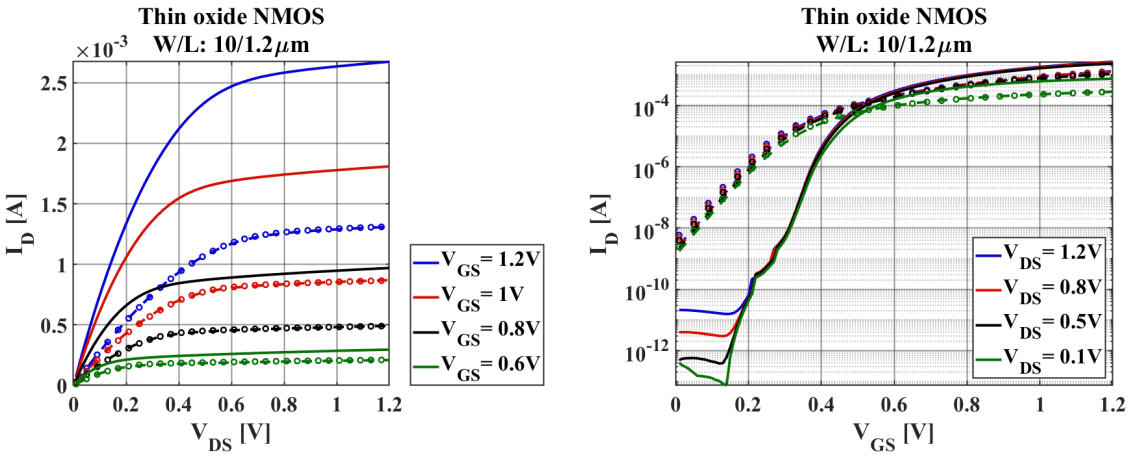

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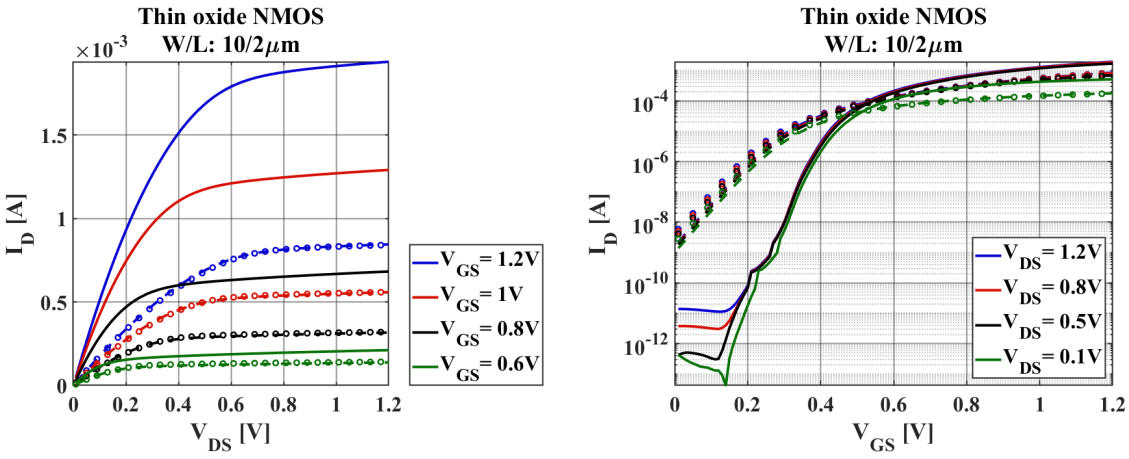

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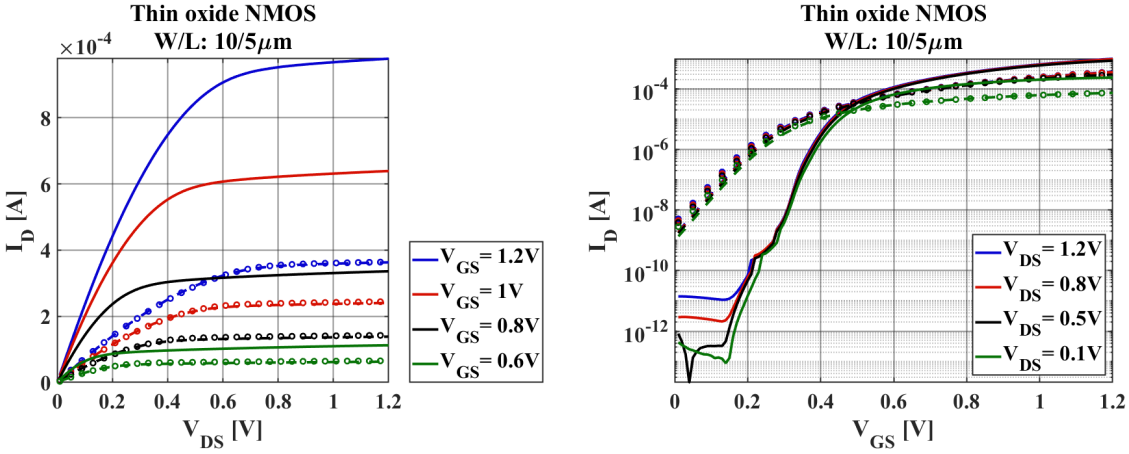

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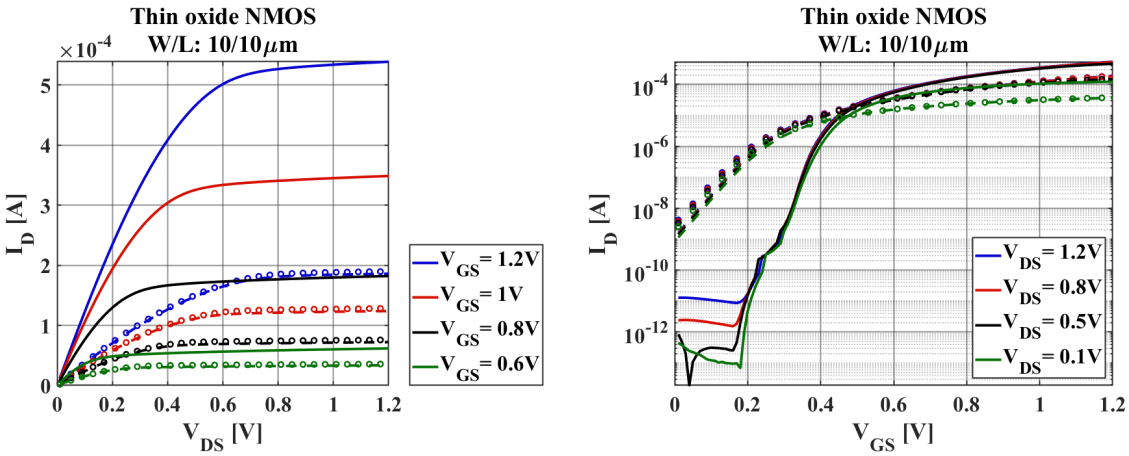

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