Analysis of Power Redistributors for Low-Voltage Distribution Grids

by

Anand Krishnamurthy Iyer

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Student number:	5026482	
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Thesis committee:	Dr. ir. Thiago Batista Soeiro,	TU Delft, Supervisor
	Prof. dr. ir. Pavol Bauer,	TU Delft
	Dr. Aleksandra Lekic,	TU Delft
	Ir. Marco Stecca,	TU Delft, Daily Supervisor

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No problem is so big or so complicated
that it can't be run away from!

Charlie Brown

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Abstract

The phenomenon of phase unbalance is prevalent in the low voltage distribution grid due to the presence of single-phase loads. The unbalance can cause issues such as capacity underutilisation, transformer losses and problems with induction motors. To ensure the reliability of the upstream grid, it is important to maintain balanced three-phase power. This becomes more relevant with the proliferation of Distributed Energy Resources (DERs) and storage. This thesis explores the use of power electronic devices as a power redistributor.

To begin with, different topologies of a converter are discussed. These topologies have their own sets of advantages and disadvantages. Based on various operating and design parameters, a comparison between these topologies is made.

Subsequently, different control strategies for the converter are analysed. Among these, the current control strategy ensures supply of balanced and sinusoidal current to the loads with low computational burden, and is hence chosen. This strategy involves the control of sequence components independently in the double synchronous reference frame.

Low-frequency harmonics occur in the DC-link as a result of the compensation of negative-and zero-sequence components by the converter. The magnitude of this low-frequency harmonic and the overall harmonic Root Mean Square (RMS) current in the DC-link are derived mathematically and validated by simulations to represent this converter. It is observed that the DC-link sizing is mainly dependent on the low-frequency harmonics and thus, their accurate estimation will help in better sizing of the DC-side components.

The various configurations of the converter under consideration are benchmarked against each other on parameters such as Total Harmonic Distortion (THD), Power Losses, and DC-Link Sizing.

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This has been a journey of fun, frustration and insight which I'm happy to have experienced with all these people around. Thank you for the memories!

Anand Krishnamurthy Iyer
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List of Abbreviations

DER Distributed Energy Resource

EV Electric Vehicle

PCC Point of Common Coupling

DOF Degree of Freedom

EMC Electromagnetic Compatibility

PWM Pulse Width Modulation

SPWM Sinusoidal PWM

3P-4W Three-Phase Four Wire

PLL Phase-Locked Loop

CPT Coservative Power Theory

BPF Band-Pass Filter

3P-3W Three-Phase Three Wire

VSG Virtual Synchronous Generator

PI Proportional-Integral

PR Proportional-Resonant

LV Low Voltage

SVPWM Space Vector PWM

DPWM Discontinuous PWM

RMS Root Mean Square

MS Mean Square

VSC Voltage Source Converter

LPF Low-Pass Filter

THD Total Harmonic Distortion

1

Introduction

The problem of phase-unbalance has long existed in the distribution power system due to the presence of a large number of single-phase loads. This can cause issues such as capacity underutilisation, transformer losses in the upstream grid as well as problems with induction motors. However, with the introduction of Distributed Energy Resources (DERs), this phenomenon becomes all the more important and critical in maintaining reliable power distribution.

1.1. Phase Unbalance in in the Low Voltage (LV) Distribution Grid

Various organisations such as IEEE, IEC and CIGRE provide their definitions for phase-unbalance [1]–[3]. Phase unbalance essentially means that the three-phase power in the system is unbalanced. Such unbalance can be caused both by current and by voltage unbalance [4]. This section will now go in to detail as to how critical of an issue Phase-unbalance is in the distribution system, its causes and effects.

1.1.1. Scale of the Problem

The phase-unbalance phenomenon is documented throughout the world [4]. In the UK, it was found that there is a majority of LV feeders having significant phase-unbalance [5]. Proliferation of Electric Vehicles (EVs), DERs with single-phase connection is likely to compound this problem [4], [6].

Another example in Europe is Denmark, where the distribution company does not have control over how single-phase appliances are connected. This inevitably leads to phase-unbalance in the distribution grid [7], [8].

Elsewhere, in the USA, for most of the distribution network, the three-phase system exists only up to the MV feeders. These feeders are connected to three-phase customers or to single-phase laterals which supply power to single-phase consumers [4]. This difference in the topology in comparison with Continental Europe leads to a different scenario. Whereas in Europe, the phase-unbalance is

most prominent in the LV distribution system, in the USA, it is more prevalent in the MV distribution system [4].

Considering the global scenario, in countries like China and Australia as well, this issue is prevalent. It occurs mainly due to the single-phase consumer loads which are unbalanced quite often [4].

1.1.2. Causes of Phase-unbalance

There are a number of reasons for the occurrence of phase-unbalance in the distribution system during normal usage, which are summarised below from [4]:

1. **Load Allocation:** Considering most consumers are connected through single-phase supplies, their distribution is not always done evenly in the three-phase network. This leads to an inherent phase unbalance in the distribution network due to random connections of consumers [7], [9].

2. **Asymmetric network:** The single-phase consumer connection is given by single-phase laterals from the three-phase transformers [9]. As pointed out in [10], the structure of such a network can by itself cause phase-unbalance due to the mutual coupling between lines.

3. **Load Connection:** The presence of a large number of single-phase loads, even with three-phase consumers can create unbalance. Large single-phase loads such as EVs, electric heaters, etc. can lead to real-time unbalance [4]. This unbalance is mainly affected by consumer behaviour [4].

In addition to the above, due to unsymmetrical faults as well, phase-unbalance can occur [4]. However, this is not in the scope of this thesis, since it focuses on phase-balancing during normal operation of the Low Voltage (LV) distribution network.

1.1.3. Effects of Phase-unbalance

The phenomenon of phase-unbalance greatly affects the distribution grid as summarised below.

1. **Capacity underutilisation:** For a three-phase transformer, if one of the phases is heavily loaded compared to the other two phases, the upstream feeder's capacity cannot be fully utilised and is limited by the heavily loaded phase. Thus, the feeder would require capacity upgradation earlier than with balanced three-phase power [11]. Additionally, in Three-Phase Four Wire (3P-4W) systems, the phase-unbalance causes flow of neutral-line current which in turn reduces the transformer capacity due to additional power flow in the neutral line [11].

2. **Transformer Losses:** Unbalanced loading of a distribution transformer can lead to an increase in the transformer copper losses [12].

3. **Problems with Induction Motors:** A small voltage unbalance, and the presence of negative-sequence components can cause significant losses and subsequently lead to heating of the induction motors [13]. This leads to derating the motors connected to an unbalanced network.

4. **Nuisance Tripping:** The presence of neutral return current may trip the protective device leading to pre-mature tripping of loads [4].

1.1.4. Mitigation of Phase-unbalance

This problem of phase-unbalance in the distribution network can be mitigated in a number of ways. Some of these methods are presented below.

1. **Re-phasing on distribution-side:** This methodology involves moving the loads/LV laterals from one phase which is heavily loaded to another lightly loaded phase. This switch can be done either in the online state(when the loads are energised) by the use of semiconductor devices [14] or the offline state (during a power cut) which involves manual re-wiring. However, the addition of such semiconductor devices and manual rewiring of cables in the distribution network is not easily scalable [4].

2. **Use of a Power Redistributor device:** This solution involves the use of a Power-Electronic based converter to re-distribute the currents in the distribution system such that the upstream transformer sees a balanced load. This method has the advantage that it is easily scalable, and in the cases of just load balancing, only a shunt-connected device is necessary and thus, can be installed at any node in the distribution network. The major challenge with this method is its reliability on continuous operation in the long term [4].

3. **Use of DERs, EVs and energy storage:** The proliferation of distributed energy generators and loads such as EVs gives an opportunity to use these resources for balancing the three-phase distribution system. This involves the use of control algorithms to control such generators/loads to compensate the phase-unbalance [4].

In this thesis, we shall explore the design of a **Power Redistributor Device** for use in distribution grids.

1.2. Research Questions

The focus of this thesis is to explore the configurations and various parameters to be taken into consideration during the design of the Power Redistributor. The following are the research questions this thesis aims to answer:

1. What are the possible configurations of a converter suited for the realisation of a power redistributor for use in the LV distribution grids?

2. How does the sizing of the DC-link capacity change based on the configuration of converter selected?

3. What are the different methods of controlling this converter and its implementation?

1.3. Structure of the thesis

The thesis addresses each of these research questions. The chapters of this thesis are summarised here.

- **Chapter 1** gives an introduction to the research topic, some background motivation and methods to tackle the phase-unbalance problem in LV distribution grids.
- **Chapter 2** gives a detailed analysis and working of a Power Redistributor device. The mathematical decomposition of unbalance is introduced, various topologies of the converter, and possible control strategies of the converter are explored in this chapter.
- **Chapter 3** deals with the mathematical modelling of a converter. In this chapter, the major contribution is the DC-Link current ripple derivation which is dealt with in detail. In addition, operating limits of the converter, switch rating and capacitance derivation are dealt with in this chapter.
- **Chapter 4** deals with the detailed design of the control loops used for the converter. The stability of the converter is also explored in this chapter.
- **Chapter 5** deals with the simulation model of the converter and the various topologies under consideration. The topologies are compared on various chosen parameters by operating under different conditions, and the mathematical model of the converter is also verified.
- **Chapter 6** summarises the whole thesis. Some important discussion points are raised, and possible topics of future research are also explored.

2

The Power Redistributor

The Power Redistributor is essentially a three-phase grid-connected converter. The use of such a converter allows for a lot of flexibility with respect to the control of the power flow in the grid. The scenario where single-phase loads/generators are connected in the downstream distribution network is presented in Fig. 2.1. Based on the control strategy employed, the following modes of operation can be achieved [15]:

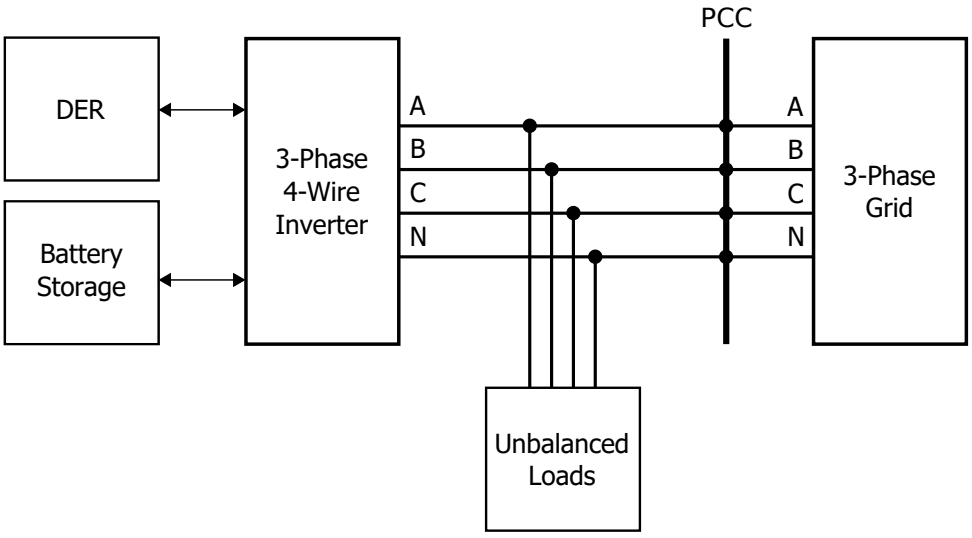


Figure 2.1: System Configuration including the Power Redistributor device

1. **Power Redistribution:** The device can be employed to compensate the phase-unbalance of the distribution network. By employing this strategy, the

upstream transformer sees a three-phase balanced load, which mitigates the phase-unbalance problem.

2. **Grid-connection of DERs and energy storage:** The presence of the DC link gives an opportunity for the use of DC DERs and battery storage as well. This helps in locally compensating energy surplus/shortage leading to better overall efficiency of the power system.

3. **Islanded operation:** During the absence of the grid, the inverter can operate in grid-forming mode. This can help in power supply for loads during grid-blackout.

2.1. Symmetrical Components

In order to analyse the unbalanced behaviour of three-phase systems, the phase quantities can be transformed into their symmetrical components, by means of the Fortescue transformation [16]. This decomposition not only helps in making the analysis of unbalanced systems easier, but also has some physical meaning associated with it [17]. A brief overview of this concept is given in this section.

In a three-phase network, the phase-currents I_A, I_B and I_C are given as shown below in (2.1):

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} |I_A| \sin(\omega t - \phi_A) \\ |I_B| \sin(\omega t - \phi_B) \\ |I_C| \sin(\omega t - \phi_C) \end{bmatrix} \tag{2.1}$$

where ω is the angular frequency of the sinusoidal waveform and ϕ_A, ϕ_B and ϕ_C represent the phase-difference with respect to the reference angle ωt.

In balanced conditions, the phasors have the same amplitude and are exactly at 120° phase-difference with respect to each other. Thus, under these conditions, the system analysis is simple and can be done by considering an equivalent single-phase condition and extrapolating to the three-phase networks.

In unbalanced networks, the situation is different and thus, the analysis becomes complex. To simplify this, Fortescue proposed to decompose this three-phase unbalanced phasors into Positive, Negative and Zero-Sequence Components [16]. These decomposed components are respectively three-sets of balanced phasors. The transformation of line currents into their respective symmetric components is done as per the transformation in (2.2) [16]:

$$\begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{2.2}$$

where $a = e^{j2\pi/3}$, and I_1, I_2 and I_0 are the positive, negative and zero-sequence components of the current respectively. Similarly, the inverse transformation is given in (2.3):

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix} \tag{2.3}$$

Following are the implications of the sequence currents:

- The positive-sequence current represents the actual power flow from source to load and is responsible for Active & Reactive Power Transfer.
- The negative-sequence current is caused by the ripple power which mostly oscillates at double the supply frequency [17]. In addition, the negative-sequence current also determines the selection of DC-link voltage as well as the capacitance for a specified DC-link voltage ripple [18].
- The zero-sequence current determines the current flowing through the neutral conductor. This can be observed from the fact that, in a 3P-4W system, the neutral current is the summation of the individual line currents i.e. $I_N = I_A + I_B + I_C$. From (2.2), it can be concluded, the neutral current is 3 times the zero-sequence current [18].

Thus, based on the impact of these components, an unbalance factor for both the negative and zero-sequence components can be determined as specified by IEC in (2.4) and (2.5) [19]:

$$\text{Unbalance\_n} = \frac{\text{Negative-Sequence Component}}{\text{Positive-Sequence Component}} \times 100\% \tag{2.4}$$

$$\text{Unbalance\_0} = \frac{\text{Zero-Sequence Component}}{\text{Positive-Sequence Component}} \times 100\% \tag{2.5}$$

In the literature, only voltage unbalance limits are generally specified in various standards. The voltage unbalance limits from some common standards such as IEC, NEMA, ANSI and the European standard are summarised in Table 2.1.

Table 2.1: Voltage Unbalance Limits

Standard	Unbalance Limit
ANSI C84.1 [20]	3%
NEMA MG-1-1998 [21]	1%
EN-50160 [22]	2%
IEC 61000-2-12 [19]	2%

2.2. Topologies of the converter

As previously mentioned, the power redistributor is assembled by means of a three-phase power electronics based converter. This converter can be realised using various topologies, each of them having their own advantages and disadvantages. A few prominent topologies and their various features are presented below.

2.2.1. Two-Level Three Leg Converter with split capacitor (3L)

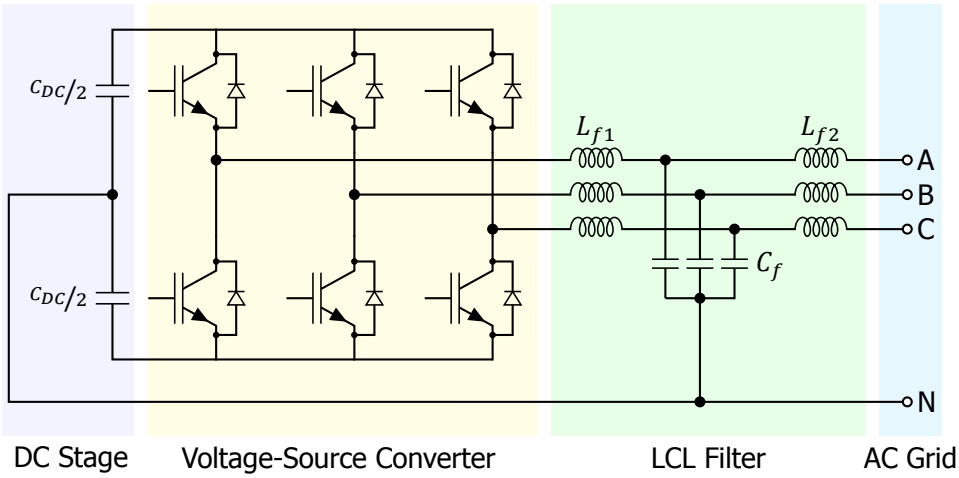


Figure 2.2: Two-Level Three-Leg converter for a 3P-4W system

An example of a 3P-4W system connected to a two-level three-leg converter is presented in Fig. 2.2. From the figure, we can observe that the three-legs converter are connected to the respective phase lines, whereas the neutral is connected to a split-capacitor across the DC-link. Essentially, this means that the capacitor mid-point voltage indirectly controls the neutral current in the system since the harmonic currents can flow through either of the capacitors [23]. Some important features of this topology are presented below:

- This topology requires the use of three equally-rated switches which can carry the line current flowing through each phase.
- The control of the three-phase currents can be done using voltage control loops in the synchronous reference frame.
- An additional controller is necessary to ensure the potential difference across the two capacitors is brought to zero since the neutral is connected at this mid-point [15].
- The capacitors in this topology carry the full neutral current, i.e. 3 times the zero-sequence component of current. In essence, this would imply the

capacitors should be rated to carry three times the individual phase currents in the case of 100% zero-sequence unbalance. Thus, the capacitors will have to be large considering the magnitude of the low-frequency components of currents in addition to the high-frequency switching currents [15].

- The use of the neutral filter inductance is optional. The use of this inductor can help reduce the THD of the line currents. However, in situations of high-unbalance/presence of large zero-sequence currents, this can lead to reduced efficiency [24].

2.2.2. Two-Level Four Leg Converter (4L)

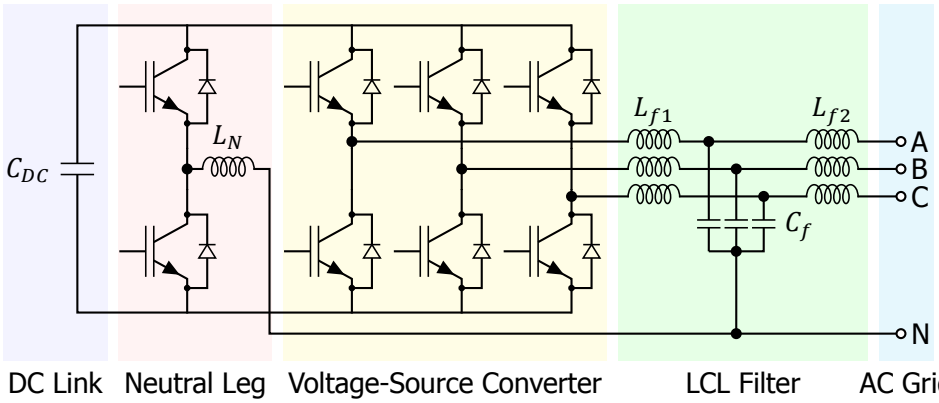


Figure 2.3: Two-Level Four-Leg converter for a 3P-4W system

The two-Level four leg converter is presented in Fig. 2.3. From this figure, we can observe that it is similar to the three-leg converter, with an additional leg added to control the neutral line as well. In this topology, the capacitor mid-point is not connected to the system neutral. Some important features of this topology are:

- The fourth leg carries the neutral current i.e. zero-sequence current. As a result, the switches used in the fourth leg have to be rated for three-times the phase current to ensure its operation during maximum unbalance [15].
- Due to the presence of the fourth leg, the low-frequency components of current do not pass through the capacitor. Thus, the capacitor only compensates the switching components of the current and thus, its rating is lower compared to the three-leg converter [15].
- The fourth leg gives an additional Degree of Freedom (DOF) to control the neutral current.
- There is a potential Electromagnetic Compatibility (EMC) problem since the DC-link is subject to high-frequency transitions with respect to the system

neutral [25]. This can lead to high common-mode current flowing through the system.

2.2.3. Two-Level Four Leg converter with split capacitor (4L-SC)

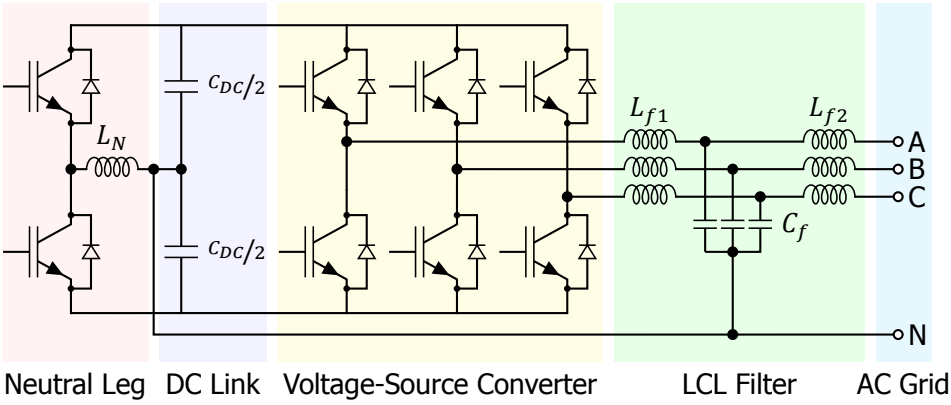


Figure 2.4: Two-Level Four-Leg converter with split capacitor for a 3P-4W system

The two-Level four leg converter with split capacitor is similar to the one presented in Section 2.2.2 except that the DC-link capacitor is split. The schematic is presented in Fig. 2.4. One important point to note is the fact that the mid-point between the capacitor is connected directly to the neutral line after the filter inductance. Thus, the fourth leg does not directly form the neutral point, but can actively balance the split DC-link [25]. Some of the notable features of this topology are:

- The neutral-leg control is completely decoupled from the phase current control.
- Since the neutral-leg is decoupled, the voltage source converter can be assembled also with multilevel topologies [25].
- Both the DC-link and the inverter are at a constant potential with respect to the system neutral leading to better EMC performance as compared to the normal four-leg topology [25].

2.2.4. Three H-Bridge Inverter

This topology entails the use of three single-phase converters as shown in Fig. 2.5. These single phase converters are connected to the three-phase distribution systems through isolation transformers. Few features of this converter are listed below:

- All the switches in this converter have equal rating, thus leading to modularity and similar loss characteristics in all the switches.

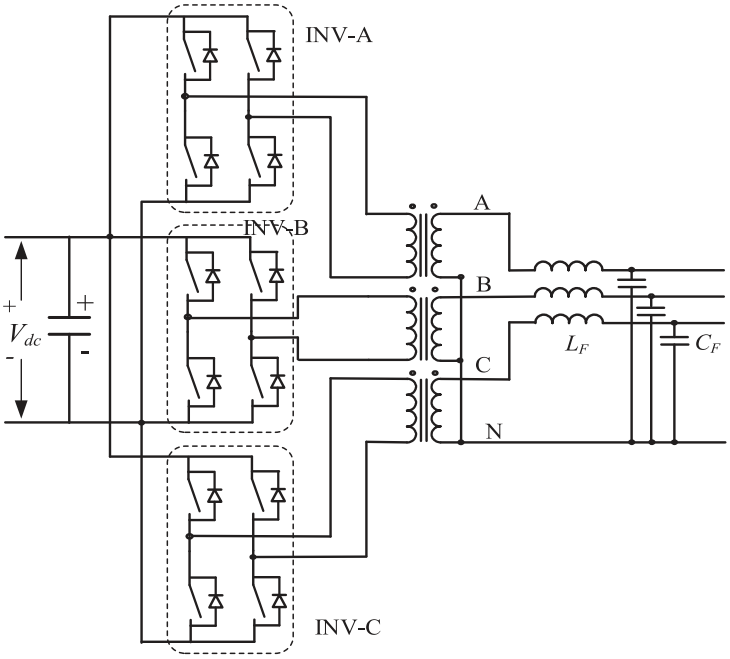


Figure 2.5: Topology of the three H-bridge inverter [15, p. 5158]

- Since the three-phases are connected independently, the overall converter is quite robust, and failure in one phase will still allow the operation of the other phases [15]. This can help in providing power for the operational-phases in the case a DER or battery storage is connected at the DC-link.

- This topology has a lower DC-link voltage requirement, i.e. half of that of the three-phase split capacitor converter [15], thus leading to smaller capacitors and lower switch stress ratings which in turn can lead to better performance.

- The major difference in this topology is the presence of isolation transformers. This increases the cost and size of the converter. In applications where isolation is necessary for grid connection, this can serve to be useful for its robust and independent control. Considering the use of this converter in the LV distribution grids, adding isolation transformers will only lead to an increase in the cost.

- It is to be noted that removing the isolation essentially makes it similar to the two-level four leg configuration, except that three legs are present to carry the neutral current in this configuration.

The various features of the different available topologies were presented. All topologies have their own strengths and weaknesses and are targetted towards

specific applications. The topologies, along with their differences in key parameters are presented in Table 2.2.

Table 2.2: Comparison between different converter topologies [23], [26]

Parameters	3-Leg Converter	4-Leg Converter	4-Leg Converter with Split Capacitor	3 H-Bridge Inverter
DC-Link voltage	High	Medium	Medium	Low
Capacitance	High	Medium	Low(+)	Low(-)
Capacitor current	High	Medium(+)	Medium(-)	Low
Number of switches	6	8	8	12
Switch rating	Equal	Unequal	Unequal	Equal
EMC	High	High	Low	Low
Isolation Transformer	Not Required	Not Required	Not Required	Required

So far the main converter topologies that can be used as power redistributor have been reviewed. The next step will focus on reviewing the control strategies of such converter topologies. The control algorithm gives a voltage-command, which is then used to control the switching devices by using PWM. A brief overview on PWM is given in Section 2.3.

2.3. Pulse Width Modulation (PWM)

The general principle of PWM is that a control signal is compared with a triangular carrier signal of high-frequency. Based on this comparison, either the top or bottom switch is turned on depending on whether the control signal is greater than or lesser than the carrier signal respectively. The generation of PWM for a half-bridge is done as per Fig. 2.6. In Fig. 2.6, v_{ctrl} represents the control signal, $\pm v_{sw}$ represent the triangular carrier signal and $T+$ & $T-$ represent the gate-signal for the upper and lower device of the half-bridge respectively.

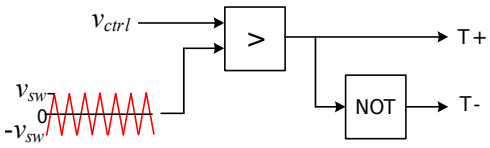


Figure 2.6: PWM Generation [27]

In a three-phase converter, the most fundamental and common method of PWM is the SPWM. In SPWM, a three-phase sinusoidal control voltage is applied to the

carrier triangular wave and this comparison is used to generate the switching pulses. This modulation mechanism and the inverter output with respect to the DC-link is shown in Fig. 2.7.

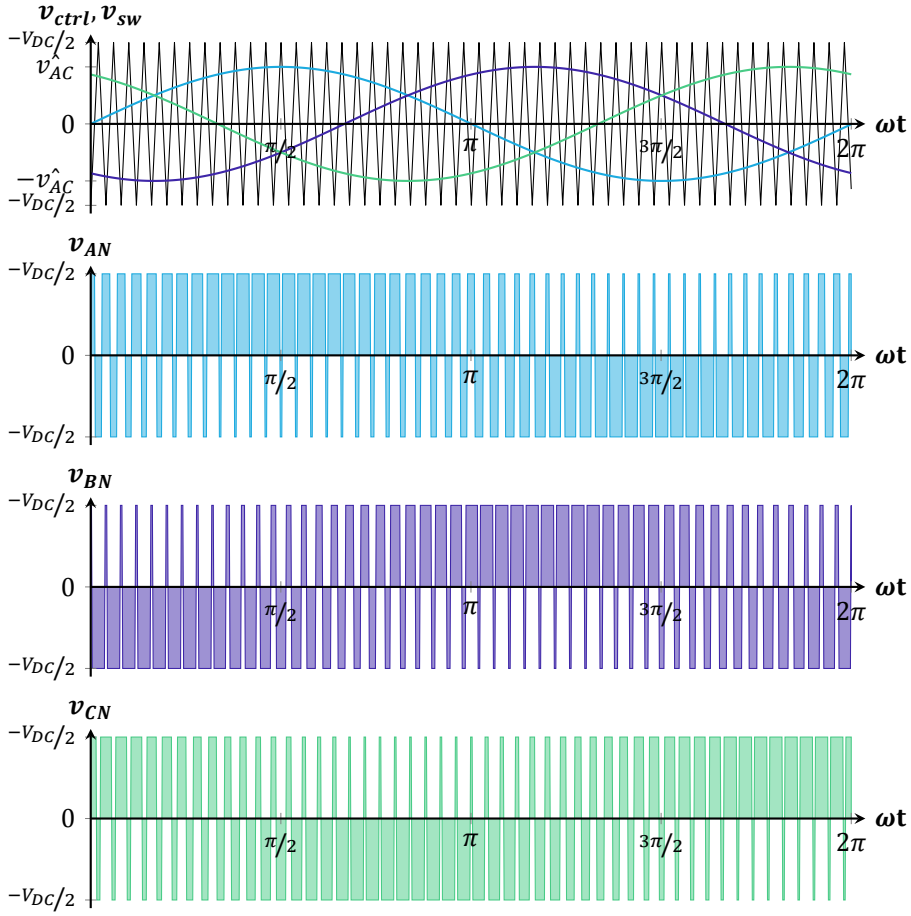


Figure 2.7: Three-phase SPWM

From Fig. 2.7, it can be observed that the output voltage varies between V_{DC} and 0. However, if the capacitor is split and the mid-point is taken to be the neutral connection on the load side, then the phase-voltage would vary between $-V_{DC}/2$ and $V_{DC}/2$.

Essentially, the control algorithm generates the control voltage signal, and this is given to a PWM generator, which in turn controls the inverter.

Other than SPWM, there are other PWM methods to generate the switching signals. Space Vector PWM (SVPWM) is a method which uses a vector-based strategy to generate the switching signals. Discontinuous PWM (DPWM) exploits the fact that the output is shorted for some time and based on switching all of the high-

side or low-side switches, the switching losses can potentially be improved. These modulation techniques are not explored in this thesis, and standard SPWM is used during the operation of the converter.

2.4. Control of the Power Redistributor

There are multiple methods of controlling the Power Redistributor Device. The most important aspect of control is determining what parameters are controlled and what expressions are used to generate the reference quantities. The most intuitive form of control is the PI-based control in the synchronous ($dq0$) reference frame or the use of a Proportional-Resonant (PR) controller which is for use in the stationary (abc) reference frame. Thus, this section shall first cover the control strategies in determining how the Power Redistributor shall be controlled.

2.4.1. The P-Q Theory based Control

This is the most common and the fundamental control method. This control is based on the Clarke and Park Transformation. The Clarke Transformation converts the phase voltages and currents into the $\alpha\beta0$ reference frame, which typically makes analysis easier, since the $\alpha\beta$ represent the projection of the vectors on the stationary reference frame and the 0-axis component represents the error in the projection. This transformation is shown in (2.6):

$$\begin{bmatrix} X_0 \\ X_\alpha \\ X_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{2.6}$$

The above-based Clarke Transformation is the Power-invariant form, which is considered in this case. This transformation is in the stationary reference frame. To transform into the synchronous reference frame, the Park's transform is employed as shown in (2.7):

$$\begin{bmatrix} X_0 \\ X_d \\ X_q \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \sin(\omega t) & \cos(\omega t) \\ 0 & \cos(\omega t) & -\sin(\omega t) \end{bmatrix} \begin{bmatrix} X_0 \\ X_\alpha \\ X_\beta \end{bmatrix} \tag{2.7}$$

In (2.6) and (2.7), the parameter X represents either the voltage or the currents. Based on the above transformations, the power in the $dq0$ reference frame is calculated as shown in (2.8) [28]:

$$\begin{bmatrix} p_0(t) \\ p(t) \\ q(t) \end{bmatrix} = \begin{bmatrix} v_0(t) & 0 & 0 \\ 0 & v_d(t) & v_q(t) \\ 0 & v_q(t) & -v_d(t) \end{bmatrix} \begin{bmatrix} i_0(t) \\ i_d(t) \\ i_q(t) \end{bmatrix} \tag{2.8}$$

where $p(t)$ is the real power, $q(t)$ is the imaginary(reactive) power and $p_0(t)$ is the zero-sequence power. These powers can be divided into their respective continuous and alternating components as shown in (2.9) [28]:

$$\begin{aligned} p_0(t) &= v_0(t)i_0(t) &&= \overline{p_0} + \widetilde{p_0} \\ p(t) &= v_d(t)i_d(t) + v_q(t)i_q(t) &&= \overline{p} + \widetilde{p} \\ q(t) &= v_q(t)i_d(t) - v_d(t)i_q(t) &&= \overline{q} + \widetilde{q} \end{aligned} \tag{2.9}$$

For balanced systems, only the continuous components $\overline{p}$ and $\overline{q}$ are non-zero. In unbalanced systems, the alternating components, $\widetilde{p}$ and $\widetilde{q}$ represent the negative-sequence contribution. The presence of zero-sequence components leads to the occurrence of zero-sequence power $p_0(t)$ [28].

In this strategy, the controller is tuned to control the powers as defined in (2.9) and thus, the power-flow to the loads can be controlled. However, a major disadvantage arises when the voltage is unbalanced or distorted. Since this strategy controls the power and not the currents and the voltage is fixed by the grid, this may lead to some current distortion [28], [29]. Thus, a Phase-Locked Loop (PLL) is necessary to provide only the positive-sequence component of voltage for control, which can help solve this issue [28].

2.4.2. Instantaneous Active and Reactive Current-based Control

Based on the Clarke and Park's transform mentioned in (2.6) and (2.7), the direct transformation of currents in abc reference frame to the $dq0$ reference frame is done using (2.10) [28]:

$$\begin{bmatrix} I_0(t) \\ I_d(t) \\ I_q(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t - 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t - 2\pi/3) \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{2.10}$$

From the above, we can decompose the $dq0$ currents into their respective components as shown in (2.11):

$$\begin{aligned} I_d(t) &= \overline{I_d} + \widetilde{I_d} \\ I_q(t) &= \overline{I_q} + \widetilde{I_q} \\ I_0(t) &= \overline{I_0} + \widetilde{I_0} \end{aligned} \tag{2.11}$$

These currents presented in (2.11) are similar to the power presented in (2.9). For a balanced voltage case, evaluation of (2.8), would lead to a conclusion that $I_d(t)$ and $I_q(t)$ are respectively responsible for the powers $p(t)$ and $q(t)$ respectively [28]. Hence, for an unbalanced voltage, the powers will not be properly compensated. However, the currents will be properly compensated which is the ultimate goal of the shunt-based power redistributor [28].

This current-based control strategy is also employed in [30]. A block diagram of the overall control strategy is presented in Fig. 2.8. From Fig. 2.8, it can be observed that the controller provides reference currents such that, the negative-sequence and zero-sequence components of the line current is provided by the

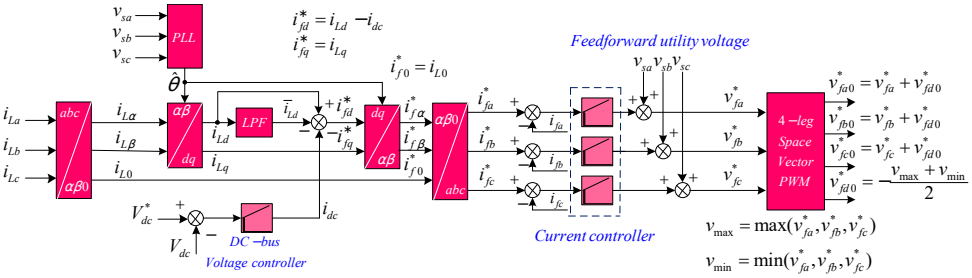


Figure 2.8: Current-based control strategy [30, p. 4]

converter. This helps in reducing the unbalance at the transformer (source) side, thus mitigating the effects of load unbalance on the upstream network. The control of the fourth-leg of the converter shall be dealt with separately in Section 2.4.4

2.4.3. Coservative Power Theory (CPT) based Control strategy

The control based on PQ-theory has issues when operated in unbalanced voltage conditions [29]. One of the alternatives is to control the converter based on the Coservative Power Theory (CPT). This theory allows for an orthogonal separation of current components as shall be presented below [29], [31].

The balanced active currents are given in (2.12) [29], [31]:

$$i^b_{a\mu} = \frac{P}{\boldsymbol{V}^2} v_\mu = G^b v_\mu \tag{2.12}$$

where b represents balanced component, a represents the active component, μ represents a, b, c phase, P represents the active power, $\boldsymbol{V}$ represents the Euclidean norm of the three-phase voltage and G^b represents the equivalent balanced conductance.

The balanced reactive currents are given in (2.13) [29], [31]:

$$i^b_{r\mu} = \frac{W}{\hat{\boldsymbol{V}}^2} v_\mu = B^b \hat{v}_\mu \tag{2.13}$$

where r represents reactive component, W represents the reactive power, $\hat{\boldsymbol{V}}$ is the Euclidean norm of the unbiased voltage integral, B^b is the equivalent balanced reactivity.

The unbalanced currents are defined as given in (2.14) [29], [31]:

$$i^u_\mu = i^u_{a\mu} + i^u_{r\mu} = \left(G_\mu - G^b\right) v_\mu + \left(B_\mu - B^b\right) \hat{v}_\mu \tag{2.14}$$

where G_μ represents the per-phase conductance and B_μ represents the per-phase reactance. These are given by (2.15) and (2.16) respectively:

$$G_\mu = \frac{P_\mu}{V^2_\mu} v_\mu \tag{2.15}$$

$$B_\mu = \frac{W_\mu}{\hat{V}^2_\mu} \hat{v}_\mu \tag{2.16}$$

The void currents are defined as those which do not transfer any active or reactive power and is given by (2.17) [29], [31]:

$$i_{v\mu} = i_\mu - i^b_{a\mu} - i^b_{r\mu} - i^u_\mu \tag{2.17}$$

All these current components, i.e. $i^b_{a\mu}, i^b_{r\mu}, i^u_{a\mu}, i^u_{r\mu}$ and $i_{v\mu}$ are orthogonal to each other leading to simplicity of control [29].

In [29], the grid needs to provide only the active balanced current component i.e. $i^b_{a\mu}$, whereas all the other components are assumed to be provided by the converter. Thus, the currents being compensated by the converter is given by (2.18) [29]:

$$i^*_\mu = i^u_{a\mu} + i^b_{r\mu} + i^u_{r\mu} + i_{v\mu} \tag{2.18}$$

Also, in the case of the converter presented in [29], the capacitor is floating and thus, the converter losses also has to be drawn by the converter. This current component is given by (2.19) [29]:

$$i^b_{a\mu\_dc} = \frac{P_{dc}}{\boldsymbol{V}^2} v_\mu \tag{2.19}$$

Thus, subsequently, the total current reference is generated following (2.20) [29]:

$$i^*_\mu = i^u_{a\mu} + i^b_{r\mu} + i^u_{r\mu} + i_{v\mu} + i^b_{a\mu\_dc} \tag{2.20}$$

Thus, based on this phase-current reference, the reference voltage is generated by using a PR control in [29]. With this, the converter control is achieved. One potential issue with the CPT based control is the use of Band-Pass Filter (BPF) to calculate the unbiased integral. Such filters generally require a very stable frequency reference and thus, can be sensitive to frequency deviations [29].

2.4.4. Control of the Fourth-Leg in a Four Leg topology

In the four-leg topology, the neutral current flows through the fourth leg instead of the capacitor. The presence of this half-bridge, in essence gives an option to control the neutral current of the grid, in addition to the phase-current control. However, based on whether the DC-link is split or not, the control of this fourth-leg will be different. These two cases are dealt with below:

- In the case of a 4-leg topology as presented in Section 2.2.2, the neutral leg control influences the control of the other legs of the converter. For simple SPWM, all the three symmetrical components i.e. positive, negative and zero-sequence components are considered, and the three-phase voltage references are generated. In this case, since the fourth leg is essentially the system neutral, for simple SPWM, the fourth-leg is simply given a command of 0. In case of other types of modulation, the zero-vector is changed in the fourth-leg, and consequently the voltage commands of the other three legs are also changed accordingly. This gives the possibility of easily implementing various modulation methods in the 4-leg converter by just changing the injected zero-vector.

Table 2.3: Comparison between different control strategies

Control Strategy	Advantages	Disadvantages
PQ Theory	• Intuitive control based on sequence decomposition. • Computationally easier to implement.	• Distorted voltage can cause distorted currents. • Necessity of a PLL.
Current-based control	• Controls current effectively even with distorted voltage. • Synchronisation using zero-crossing voltage detector is possible [28].	• Powers may not properly be compensated in unbalanced voltage conditions.
CPT-based control	• The balanced, unbalanced and void components are completely orthogonal. • Accurate control of each component can be achieved even under distorted supply conditions.	• The algorithm is computationally intensive. • Use of Band-Pass filters makes it sensitive to frequency variations.

- In the case of a split DC-Link as presented in Section 2.2.3, the neutral leg control is completely decoupled from the control of the other three legs. Thus, any form of control can be implemented independent of the actual control of the converter, such that the neutral current flows through this leg. However, for other types of modulation, where the zero-vector needs to be modified, this configuration also relies on the fact that both the phase-current controller and the neutral current controller commands need to be modified accordingly. [32].

2.4.5. Capacity Allocation for Compensation

In the Three-Phase Three Wire (3P-3W) system, the converter's total capacity is distributed for active and reactive power compensation [23]. However, in the 3P-4W system, the capacity after active and reactive power compensation can be used for higher-capacity unbalance compensation by neutral current regulation [33]. Thus, based on this, a dynamic saturation limiter for the various controllers is shown in [33]. Based on the priorities and system conditions, the neutral current limit can

be dynamically changed leading to higher-capacity unbalance compensation.

This dynamic allocation is especially important in the cases of battery storage or DERs connected to the DC-bus. The use of such algorithms can help maximise the capacity utilisation of the converter.

2.4.6. Virtual Synchronous Generator (VSG)-based Control

Liu *et al.* presented an interesting approach for the control of a Four-Leg converter as a Virtual Synchronous Generator (VSG) in [34]. This involves the use of DERs and battery storage on the DC-link side. The VSG aims to replicate the operation of a synchronous generator and thus, the concept of virtual inertia is shown in [34]. This control strategy helps in both grid-connected as well as islanded mode, where the system can power the loads independently. The use of such a system can help in realising a flexible device for both, the integration of DERs as well as improving the Power Quality in the distribution grids.

2.5. Conclusion

The problem of phase-unbalance in the LV distribution grids was explored from the literature. The possibility of using a power-electronic based converter to compensate this unbalance is explored. Various topologies and their respective advantages and disadvantages are discussed. Subsequently, a few control topologies are presented and the possibility of controlling the neutral current by using a four-leg converter is also discussed.

The proliferation of Energy storage systems and DERs with integrated inverters are on the rise. There is a necessity to design the converter to be as flexible as possible and potentially use the integrated inverter without additional investment. The four-leg topology with split capacitor presented in Fig. 2.4 can be used effectively in this case, where the neutral and three-phase current control are completely decoupled. This topology offers the possibility of a cost-effective method of controlling the unbalance in 3P-4W systems.

3

Mathematical Modelling of the Converter

As discussed in Chapter 2, the converter acts in a current-injection mode and compensates the phase-current unbalance in the loads. In this thesis, we study three configurations of the converter: The three-leg converter with split capacitor (3L), the four-leg converter with split capacitor (4L-SC) and the four-leg converter (4L). All these configurations have identical phase configurations. They differ in the control of neutral current processed by the converter. In the three-leg configuration, the capacitor carries the neutral current whereas, in the four-leg configuration, the fourth-leg carries the low-frequency neutral current.

3.1. Neutral-current in a 3P-4W system

In a 3P-4W system, the neutral current is given by the vector sum of the phase currents:

$$I_N = I_A + I_B + I_C \tag{3.1}$$

where I_A, I_B and I_C are the phase currents.

Depending on the magnitude and phase of the unbalanced phase currents, the magnitude of neutral current varies. Some operating conditions are shown below with the magnitude of neutral currents. This is also verified with a PLECS simulation, with a three-leg converter operating in islanded operating condition. A schematic of this set-up is shown in Fig. 3.1. The converter can compensate both active and reactive power unbalance. The neutral current for operation in various power unbalance compensation scenarios are presented below.

3.1.1. Active-Power Compensation

The conditions for exclusive active-power compensation are given below:

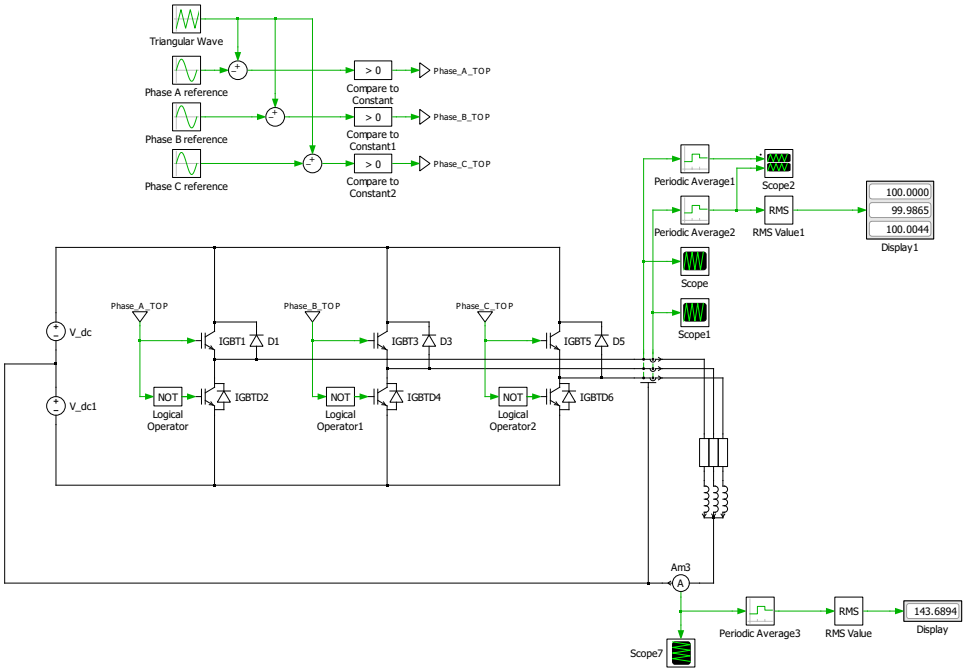


Figure 3.1: PLECS Simulation of the three-leg converter in islanded mode

- The three phase-currents have a phase-difference of 120° with respect to each other.
- The magnitude of Phase C current is taken to be 100 A, whereas the currents of Phase A and B are varied.

Based on these conditions, the magnitude of neutral current is shown in Fig. 3.2. As can be observed from Fig. 3.2, the maximum possible value of neutral current is found to be 100 A. Some specific points of interest are taken and the values from the PLECS simulation are observed and shown in Table 3.1.

Table 3.1: Neutral Current - Active Power Compensation

I_A(A)	I_B(A)	I_C(A)	I_N(A)
5.26	89.47	100.00	**89.94**
47.37	21.05	100.00	**69.63**
73.68	42.11	100.00	**50.21**

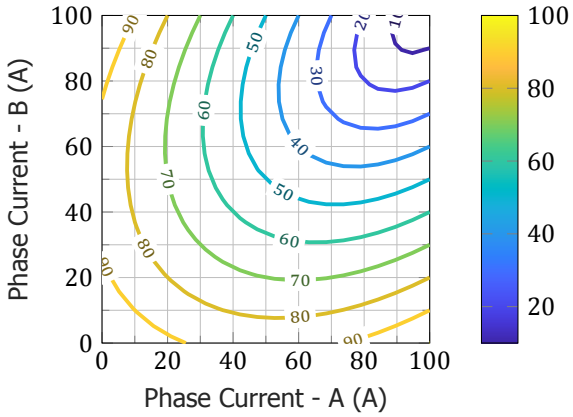


Figure 3.2: Magnitude of Neutral Current - Active Power Compensation

3.1.2. Reactive-Power Compensation

The converter compensates reactive power exclusively when the magnitudes of the phase-currents are equal, but do not operate at unity power factor. One phase is maintained at unity power factor, whereas two conditions of lag & lag and lead & lag are tested.

3.1.2.1. Lag and Lag compensation

The conditions for this test are given below:

- The magnitudes of all three phase-currents are 100 A.
- Phase-A is operated at unity power factor.
- Phase-B is operated from 0 to 1 lagging power factor.
- Phase-C is operated from 0 to 1 lagging power factor.

Based on these conditions, the magnitude of neutral current is shown in Fig. 3.3. As can be observed from Fig. 3.3, the maximum neutral current is almost 150 A. Some specific points of interest are taken and the values from the PLECS simulation are observed and shown in Table 3.2.

Table 3.2: Neutral Current - Reactive Power Compensation (lag and lag)

I_A, I_B, I_C(A)	PF_B(lag)	PF_C(lag)	I_N(A)
100.00	0.11	0.47	**139.77**
100.00	0.47	0.11	**101.85**
100.00	0.95	0.47	**79.80**
100.00	0.47	0.95	**102.95**

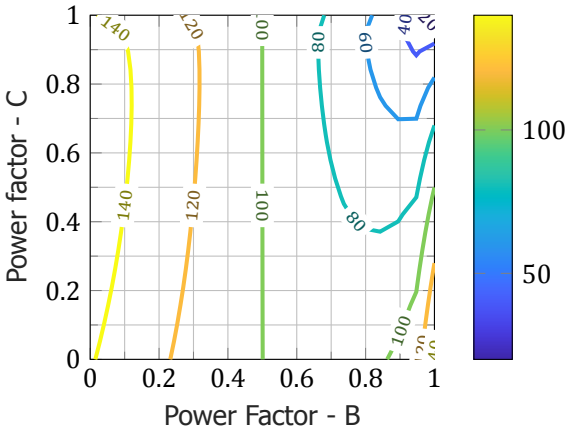


Figure 3.3: Magnitude of Neutral Current - Reactive Power Compensation (lag and lag)

3.1.2.2. Lead and Lag compensation

The conditions for this test are given below:

- The magnitudes of all three phase-currents are varied equally from 0-100 A.
- Phase-A is operated at unity power factor.
- Phase-B is operated from 0 to 1 leading power factor.
- Phase-C is operated from 0 to 1 lagging power factor.
- Both Phase-B and Phase-C are operated at the same power factor in lead and lag configuration respectively.

Based on these conditions, the magnitude of neutral current is shown in Fig. 3.4. As can be observed from Fig. 3.4, the maximum neutral current is almost 250 A. Some specific points of interest are taken and the values from the PLECS simulation are observed and shown in Table 3.3.

Table 3.3: Neutral Current - Reactive Power Compensation (lead and lag)

I_A, I_B, I_C(A)	PF	I_N(A)
21.05	0.26	**50.69**
57.89	0.11	**152.41**
94.74	0.68	**149.59**

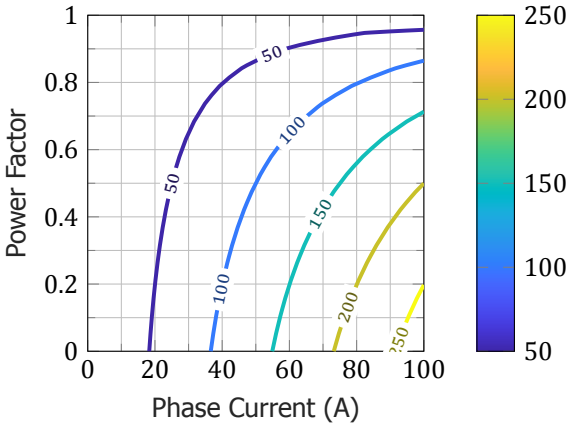


Figure 3.4: Magnitude of Neutral Current - Reactive Power Compensation (lead and lag)

3.1.3. Active & Reactive Power Compensation

The converter compensates both the active and reactive power unbalance when the magnitudes of phase-currents are not maintained equal to each other, and the phases are not operated at unity power factor. In this case as well, the magnitude of neutral current varies when the phases are operated in lead & lag as well as the lag & lag condition. These conditions are shown below.

3.1.3.1. Lag and Lag compensation

The conditions for this test are given below:

- Phase-A is maintained at zero current.
- Phase-B and C are operated at 100 A current.
- Phase-B is operated from 0 to 1 lagging power factor.
- Phase-C is operated from 0 to 1 lagging power factor.

Based on these conditions, the magnitude of neutral current is shown in Fig. 3.5. As can be observed from Fig. 3.5, the maximum neutral current is almost 200 A. Some specific points of interest are taken and the values from the PLECS simulation are observed and shown in Table 3.4.

3.1.3.2. Lead and Lag compensation

The conditions for this test are given below:

- Phase-A is maintained at zero current.
- Phase-B and C are operated at 100 A current.

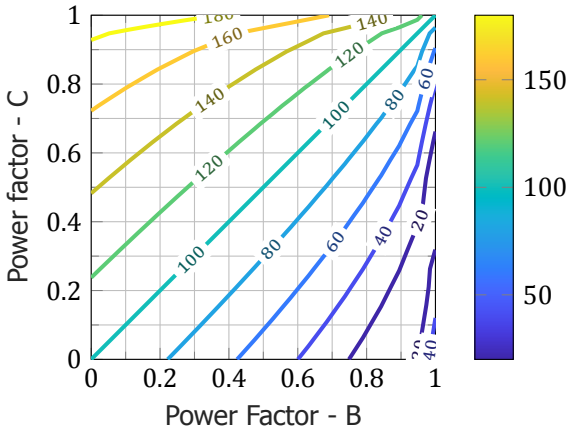


Figure 3.5: Magnitude of Neutral Current - Active & Reactive Power Compensation (lag and lag)

Table 3.4: Neutral Current - Active & Reactive Power Compensation (lag and lag)

I_A(A)	I_B, I_C(A)	PF_B(lag)	PF_C(lag)	I_N(A)
0.00	100.00	0.16	0.16	**100.00**
0.00	100.00	0.05	0.52	**139.85**
0.00	100.00	0.42	0.95	**160.18**
0.00	100.00	0.52	0.05	**53.89**
0.00	100.00	0.95	0.42	**23.67**

- Phase-B is operated from 0 to 1 leading power factor.
- Phase-C is operated from 0 to 1 lagging power factor.

Based on these conditions, the magnitude of neutral current is shown in Fig. 3.6. As can be observed from Fig. 3.6, the maximum neutral current is almost 200 A. Some specific points of interest are taken and the values from the PLECS simulation are observed and shown in Table 3.5.

3.1.4. Neutral Current compensation limits

Based on the above calculated neutral current magnitudes for different operating conditions, it can be observed that the neutral current strongly has a dependence on the magnitude and phase-difference between the phase currents. These operating conditions help define compensation limits of the neutral current by the converter. This is important to ensure reliable operation of the converter in a specified operating range.

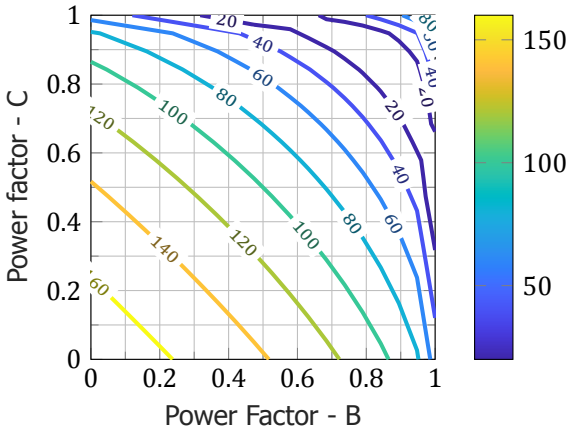


Figure 3.6: Magnitude of Neutral Current - Active & Reactive Power Compensation (lead and lag)

Table 3.5: Neutral Current - Active & Reactive Power Compensation (lead and lag)

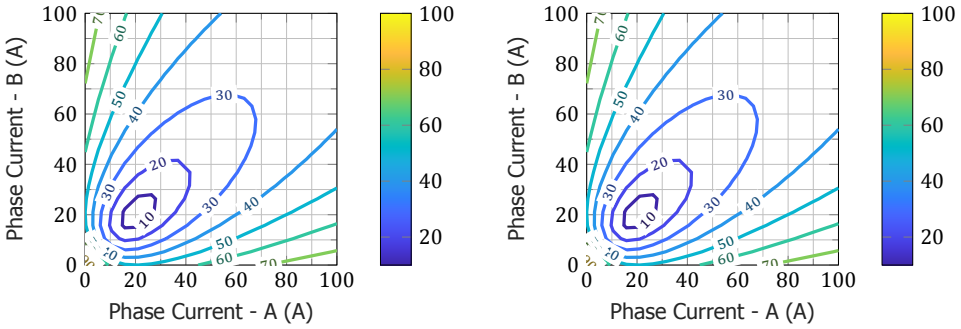
I_A(A)	I_B, I_C(A)	PF_B(lead)	PF_C(lag)	I_N(A)
0.00	100.00	0.16	0.37	**141.10**
0.00	100.00	0.37	0.16	**140.50**
0.00	100.00	0.47	0.84	**59.08**
0.00	100.00	0.84	0.47	**59.08**

3.2. Magnitude of Unbalance

In the previous section, the magnitude of neutral current for varying cases were discussed. In this section, based on (2.4) and (2.5), the unbalance magnitude for all the cases discussed above are shown. This helps understand the severity of unbalance for various operating conditions. Figs. 3.7 to 3.11 show the Negative-sequence and Zero-sequence unbalance magnitude for these cases.

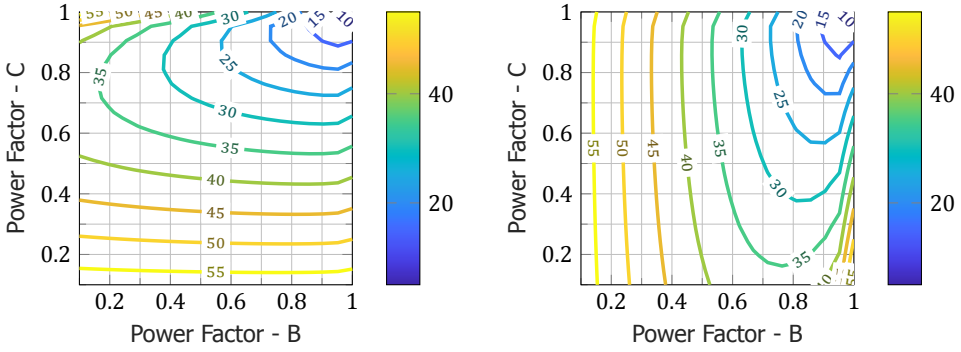
3.3. DC-Link Current

In a balanced scenario, the DC-link current is composed of only the positive-sequence component and thus, only the high-frequency switching ripple is present in the DC-side current. However, considering the unbalance scenario, the current is composed of additional components which affect the design of the DC-link. Both the average and Root Mean Square (RMS) current value are affected in this scenario. These quantities are derived in this section building on the procedure presented by Pei *et al.* in [35]. It is important to note that this derivation derives the expression of DC-link current based on carrier switching frequency, and thus, higher-order switching harmonics are not considered.



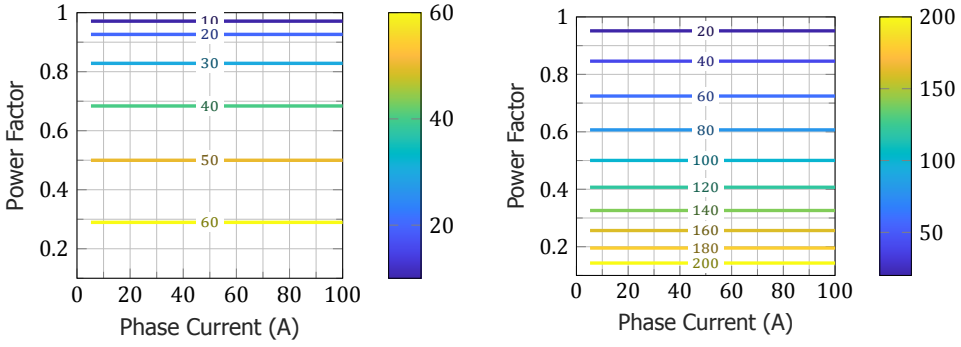
(a) Negative-Sequence **(b)** Zero-Sequence

Figure 3.7: Unbalance Magnitude - Active Power Compensation



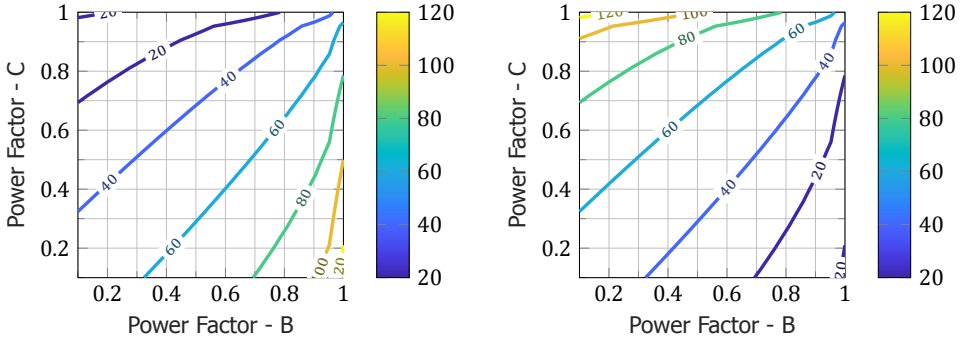
(a) Negative-Sequence **(b)** Zero-Sequence

Figure 3.8: Unbalance Magnitude - Reactive Power Compensation (lag and lag)



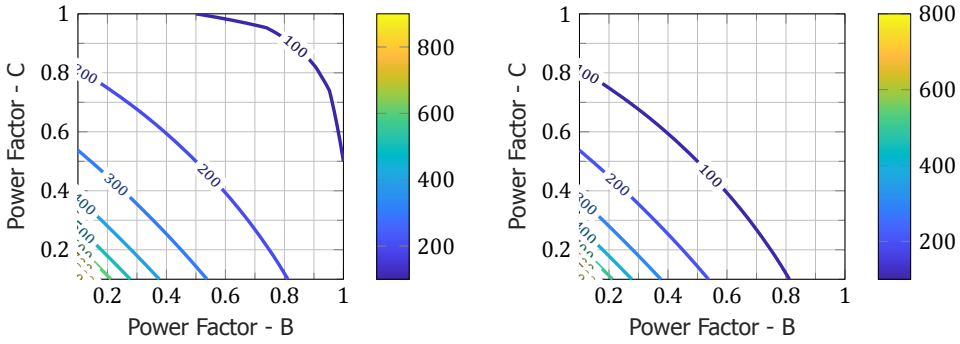
(a) Negative-Sequence **(b)** Zero-Sequence

Figure 3.9: Unbalance Magnitude - Reactive Power Compensation (lead and lag)



(a) Negative-Sequence **(b)** Zero-Sequence

Figure 3.10: Unbalance Magnitude - - Active & Reactive Power Compensation (lag and lag)



(a) Negative-Sequence **(b)** Zero-Sequence

Figure 3.11: Unbalance Magnitude - - Active & Reactive Power Compensation (lead and lag)

Consider the three-phase current, which can be decomposed into their respective symmetrical components as shown in (3.2):

$$\begin{aligned} I_A &= I_1 \sin(\omega t - \phi_1) + I_2 \sin(\omega t - \phi_2) + I_0 \sin(\omega t - \phi_0) \\ I_B &= I_1 \sin(\omega t - \phi_1 - 2\pi/3) + I_2 \sin(\omega t - \phi_2 + 2\pi/3) + I_0 \sin(\omega t - \phi_0) \\ I_C &= I_1 \sin(\omega t - \phi_1 + 2\pi/3) + I_2 \sin(\omega t - \phi_2 - 2\pi/3) + I_0 \sin(\omega t - \phi_0) \end{aligned} \tag{3.2}$$

where I_1, I_2, I_0 are the positive, negative & zero-sequence currents and ϕ_1, ϕ_2, ϕ_0 are the phase-angle differences of the positive, negative and zero-sequence currents with the voltage reference vector.

A balanced voltage reference is assumed to calculate the DC-link current. Fig. 3.12 show the different intervals A-F which represent the change in voltage sequence of the input reference signals. In each carrier period of the PWM signal, the reference signal varies at a much lower frequency and is assumed to be constant. The switching waveforms and the respective DC-link currents are shown in Fig. 3.13. Based on Fig. 3.13, the timing of each state can be derived. As an example, the timings for interval A in Fig. 3.13a are derived in (3.3) [35]:

$$\begin{aligned} T_0 &= \frac{T_s}{4}\Big(1 - m_a \sin(\omega t) - m_a v_z\Big) \\ T_1 &= \frac{T_s}{4} m_a \Big(\sin(\omega t) - \sin(\omega t + 2\pi/3)\Big) \\ T_2 &= \frac{T_s}{4} m_a \Big(\sin(\omega t + 2\pi/3) - \sin(\omega t - 2\pi/3)\Big) \\ T_3 &= \frac{T_s}{4}\Big(1 + m_a \sin(\omega t - 2\pi/3) + m_a v_z\Big) \end{aligned} \tag{3.3}$$

where T_s is the time-period of one carrier wave, m_a is the modulation index and v_z is an additional signal injected into the three-phase reference signals. The injected component v_z varies depending on the type of modulation used. For SPWM, $v_z = 0$. The modulation index, m_a, assuming balanced three-phase voltage is defined as follows:

$$m_a = \frac{2 \cdot |V_{ABC}|}{V_{DC}} \tag{3.4}$$

where $|V_{ABC}|$ is the magnitude of the balanced converter voltage and V_{DC} is the DC-link voltage. Based on the above-mentioned conditions, the average value and the harmonic RMS component of the DC-link current are derived below.

3.3.1. Average of the DC-Link current

The average value of the DC-link current in one period of the carrier wave in interval A is shown in (3.5):

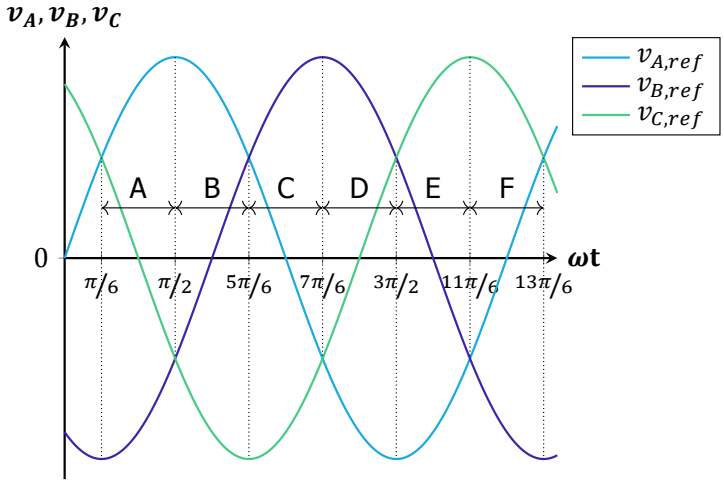


Figure 3.12: Three-phase voltage reference signals

$$\begin{aligned} I_{DC_{avg,car}} &= \frac{1}{T_s}\int_{t_0}^{t_8} i_{DC}\mathrm{d}t = \frac{2T_1}{T_s}I_A + \frac{2T_2}{T_s}(I_A + I_C) + \frac{2T_3}{T_s}I_N \\ &= \frac{3m_a I_1}{4}\cos\phi_1 - \frac{3m_a I_2}{4}\cos(2\omega t - \phi_2) - \frac{I_0}{2}\sin(\omega t - \phi_0) \end{aligned} \tag{3.5}$$

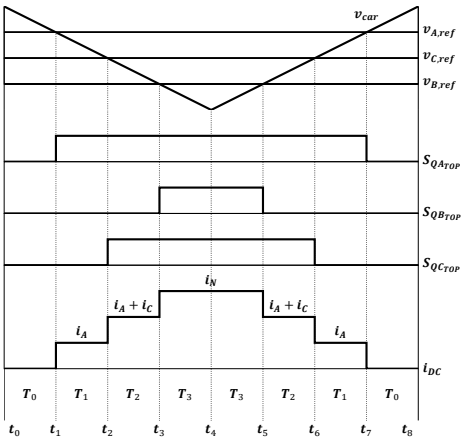
From (3.5), it can be seen that the average DC-link current also has a dependence on the negative-sequence and zero-sequence component in one carrier time period. This average is the same for each carrier period in all intervals from Period A to F. Thus, the average DC-link current for one fundamental period of the converter is given by (3.6):

$$I_{DC_{avg}} = \frac{1}{2\pi}\int_0^{2\pi} I_{DC_{avg,car}}\mathrm{d}\omega t = \frac{3m_a I_1}{4}\cos\phi_1 \tag{3.6}$$

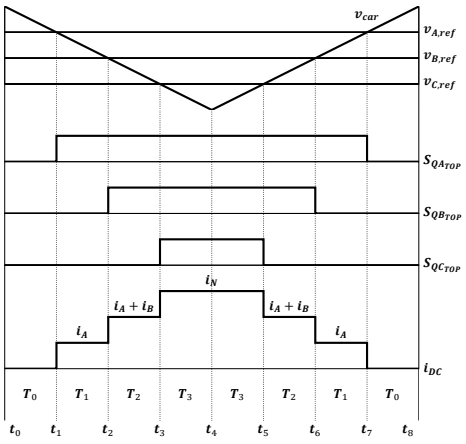
3.3.2. Harmonic RMS current

The Mean Square (MS) value of the DC-link current for one carrier period is calculated as follows. This is done as shown in (3.7) for interval A:

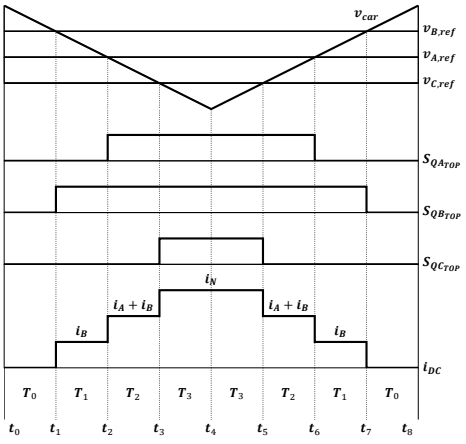
$$\begin{aligned} I_{DC_{ms,carA}} &= \frac{1}{T_s}\int_{t_0}^{t_8} i_{DC}^2\mathrm{d}t \\ &= \frac{2T_1}{T_s}I_A^2 + \frac{2T_2}{T_s}(I_A + I_C)^2 + \frac{2T_3}{T_s}I_N^2 \end{aligned} \tag{3.7}$$



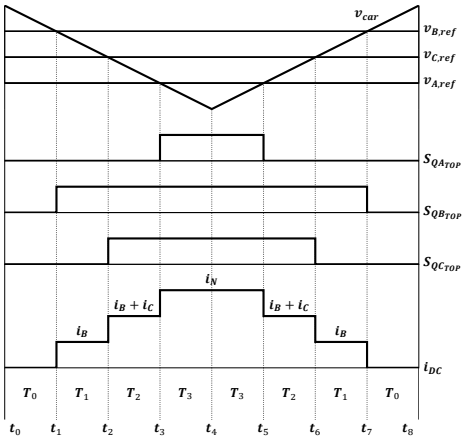
(a) Interval A



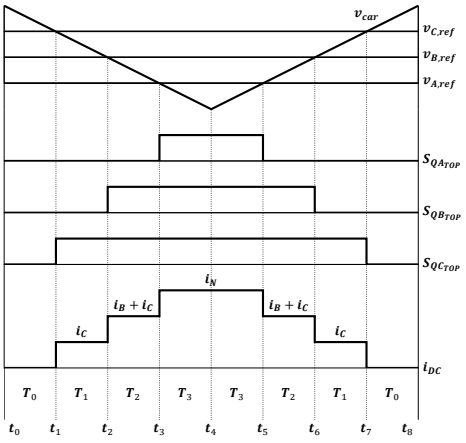
(b) Interval B



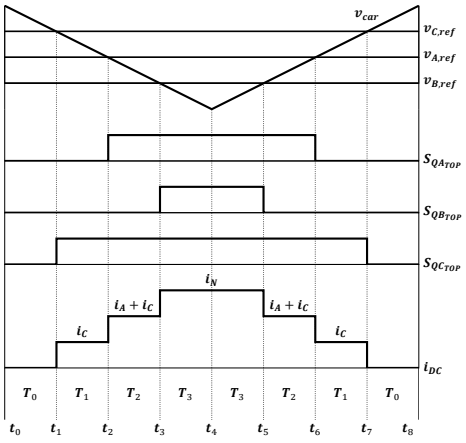
(c) Interval C



(d) Interval D



(e) Interval E



(f) Interval F

Figure 3.13: Switching signals over one carrier period for intervals A-F

Similarly, the MS values of the DC-current in one carrier period in intervals B to F can also be calculated.

The total MS current over one fundamental period is calculated using the RMS values from intervals A to F which was done using MATLAB Symbolic Toolbox. The final expression of MS current over one fundamental time period is given in (3.8):

$$\begin{aligned} I_{DC_{ms}} &= \frac{1}{2\pi}\Bigg[\int_{\pi/6}^{\pi/2} I_{DC_{ms,carA}} + \int_{\pi/2}^{5\pi/6} I_{DC_{ms,carB}} + \int_{5\pi/6}^{7\pi/6} I_{DC_{ms,carC}} \\ &\quad + \int_{7\pi/6}^{3\pi/2} I_{DC_{ms,carD}} + \int_{3\pi/2}^{11\pi/6} I_{DC_{ms,carE}} + \int_{11\pi/6}^{\pi/6} I_{DC_{ms,carF}}\Bigg] \\ &= \frac{\sqrt{3}}{4\pi}\cdot\Bigg[\left(3+2\cos\left(2\phi_1\right)\right) m_a I_1^2 + 3 m_a I_2^2 \\ &\quad + 3\left(\sqrt{3}\pi - 2m_a\right) I_0^2 - 2m_a \cos\left(\phi_2+\phi_0\right) I_2 I_0\Bigg] \end{aligned} \tag{3.8}$$

Based on the total MS current through the DC link, the harmonic RMS current can be calculated by (3.9) [35]:

$$\tilde{I}_{DC_{rms}} = \sqrt{I_{DC_{ms}} - I_{DC_{avg}}^2} \tag{3.9}$$

By substituting (3.6) and (3.8) into (3.9), the harmonic RMS current can be calculated by (3.10):

$$\begin{aligned} \tilde{I}_{DC_{rms}}^2 &= \frac{\sqrt{3}}{16\pi}\cdot\Bigg[\left(4+\left(16-3\sqrt{3}\pi m_a\right) m_a \cos^2\phi_1\right) I_1^2 + 12 m_a I_2^2 \\ &\quad + 12\left(\sqrt{3}\pi - 2m_a\right) I_0^2 - 8 m_a \cos\left(\phi_2+\phi_0\right) I_2 I_0\Bigg] \end{aligned} \tag{3.10}$$

3.4. Capacitance Requirement for the DC Link

Depending on the configuration of the converter chosen, the DC-link capacitance requirement changes. This is shown for the three-leg and four-leg topologies as follows.

3.4.1. Zero-Sequence current requirement

In the three-leg converter, the neutral current flows through the middle of the two DC-link capacitors. The individual capacitors are rated to be $2C_{DC}$ since they are in series. Since the neutral current flows through the mid-point, the two DC-link capacitors are in parallel with respect to each other giving an equivalent of $4C_{DC}$. The neutral current is related to the zero-sequence by (3.11):

$$I_N = 3I_0 = 3|I_0|\cos(\omega t + \phi_0) \tag{3.11}$$

where I_0 is the zero-sequence current, ϕ_0 is the phase-angle difference of the zero-sequence current. The voltage-ripple in the DC-link based on the capacitance is given by (3.12) [17]:

$$\begin{aligned} 3|I_0| &= 4C_{DC_0}\frac{\Delta V_{DC}}{\omega/2} \\ C_{DC(min)_0} &= \frac{3|I_0|}{2\omega\Delta V_{DC}} \end{aligned} \tag{3.12}$$

3.4.2. Negative-sequence current requirement

The power due to the negative-sequence current influences the size of the DC-link capacitor in both the three-leg and four-leg converters. The peak-to-peak energy ripple is given by (3.13):

$$\Delta E_{pp} = \frac{3V_m|I_2|}{2\omega} \tag{3.13}$$

where V_m is the peak of the AC voltage and $|I_2|$ is the magnitude of the negative-sequence current. In the DC-link, the peak-to-peak energy ripple is given by (3.14):

$$\Delta E_{pp} = \frac{1}{2}C_{DC}(V_{DC} + \Delta V_{DC})^2 - \frac{1}{2}C_{DC}(V_{DC} - \Delta V_{DC})^2 = 2C_{DC}V_{DC}\Delta V_{DC} \tag{3.14}$$

From (3.13) and (3.14), the minimum DC-link capacitance is given by (3.15) [17]:

$$C_{DC(min)_n} = \frac{3V_m|I_2|}{4\omega V_{DC}\Delta V_{DC}} \tag{3.15}$$

where V_{DC} is the DC-link voltage and ΔV_{DC} is the DC-link voltage ripple.

The capacitance of the three-leg converter is designed based on both the negative and zero-sequence currents. For the four-leg converter, the capacitor is designed based on only the negative-sequence current, since the neutral current flows through the fourth leg.

3.5. Current Rating of the switches - SPWM

The conduction loss in bipolar semiconductor devices is a function of both the average and RMS current as given in (3.16):

$$P_C = v \cdot I_{avg} + r_{on} \cdot I_{rms}^2 \tag{3.16}$$

where v is the PN-junction forward-voltage, r_{on} is the device on-state resistance, I_{avg} is the average current and I_{rms} is the RMS current.

The duty cycle of the switches in a grid connected inverter, operating with SPWM is given by (3.17):

$$\begin{aligned} D_u(\omega t) &= \frac{1}{2} + \frac{m}{2}\sin(\omega t) \\ D_b(\omega t) &= 1 - D_u(\omega t) \end{aligned} \tag{3.17}$$

where D_u & D_b are the duty cycles of the top and bottom switches respectively and m is the modulation index.

The current in one-phase of the converter is represented by (3.18):

$$I = |I|\sin(\omega t - \phi) \tag{3.18}$$

where ϕ is the phase difference between the phase-voltage and the phase-current.

The average current through the IGBT is found by integrating the top-switch duty-cycle and the phase current during the positive-half cycle of the current waveform as shown in (3.19):

$$\begin{aligned} I_{avg(IGBT)} &= \frac{1}{2\pi}\int_{\phi}^{\pi+\phi} D_u(\omega t)\cdot I(\omega t)\cdot \mathrm{d}\omega t \\ I_{avg(IGBT)} &= |I|\cdot\frac{(4 + m\pi\cos\phi)}{8\pi} \end{aligned} \tag{3.19}$$

Similarly, the RMS current through the IGBT is given by (3.20):

$$\begin{aligned} I_{rms(IGBT)} &= \sqrt{\frac{1}{2\pi}\int_{\phi}^{\pi+\phi} D_u(\omega t)\cdot I^2(\omega t)\cdot \mathrm{d}\omega t} \\ I_{rms(IGBT)} &= \frac{|I|}{2}\sqrt{\frac{3\pi + 8m\cos\phi}{6\pi}} \end{aligned} \tag{3.20}$$

The average current through the diode is found by integrating the bottom-switch duty-cycle and the phase current during the positive-half cycle of the current waveform as shown in (3.21):

$$\begin{aligned} I_{avg(diode)} &= \frac{1}{2\pi}\int_{\phi}^{\pi+\phi} D_b(\omega t)\cdot I(\omega t)\cdot \mathrm{d}\omega t \\ I_{avg(diode)} &= |I|\cdot\frac{(4 - m\pi\cos\phi)}{8\pi} \end{aligned} \tag{3.21}$$

Similarly, the RMS current through the diode is given by (3.22):

$$I_{rms(diode)} = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\pi+\phi} D_b(\omega t)\cdot I^2(\omega t)\cdot \mathrm{d}\omega t}$$
$$I_{rms(diode)} = \frac{|I|}{2}\sqrt{\frac{3\pi - 8m\cos\phi}{6\pi}} \tag{3.22}$$

3.6. Sizing of DC-Link Capacitance

As derived in Section 3.1, the neutral current can have a magnitude of three times the phase current. The converter capacity for different configurations of the converter based on the neutral current magnitude is summarised below.

- In the 3L configuration, the DC-link capacitance is a function of both the negative and zero-sequence components of currents, which can be derived following (3.12) and (3.14). Therefore there is a linear relationship between DC-link capacitor size and neutral current magnitude as shown in Fig. 3.14.
- In the 4L configuration, the zero-sequence current only can flow through the fourth leg. Thus, the capacitance is only rated for the negative-sequence current, and for higher neutral currents, the fourth-leg needs to have a higher current rating than the phase-legs as shown in Fig. 3.14.
- In the 4L-SC configuration, the zero-sequence current is controlled by the neutral current controller. Thus, if the neutral leg is rated equal to the phase-leg, for higher neutral currents, it can be redirected through the DC-link capacitance, provided enough capacitance is provided as shown in Fig. 3.15.

3.7. Conclusion

In this chapter, the mathematical modelling of the converter was dealt with. Initially, the magnitude of unbalance in the grid, based on operating conditions and the corresponding neutral current in the system were derived and presented. Subsequently, the DC-link harmonic RMS current expression was derived and an expression was derived involving the Negative-sequence ripple which has a frequency twice that of the grid frequency and the Zero-sequence ripple, which has the same frequency as the grid frequency. Based on this, the design of the capacitance and sizing of the DC-link can be done. Finally, the expressions of current through the switches were also presented, which can help estimate losses mathematically. These expressions can be verified by simulation and experimental testing of the converter.

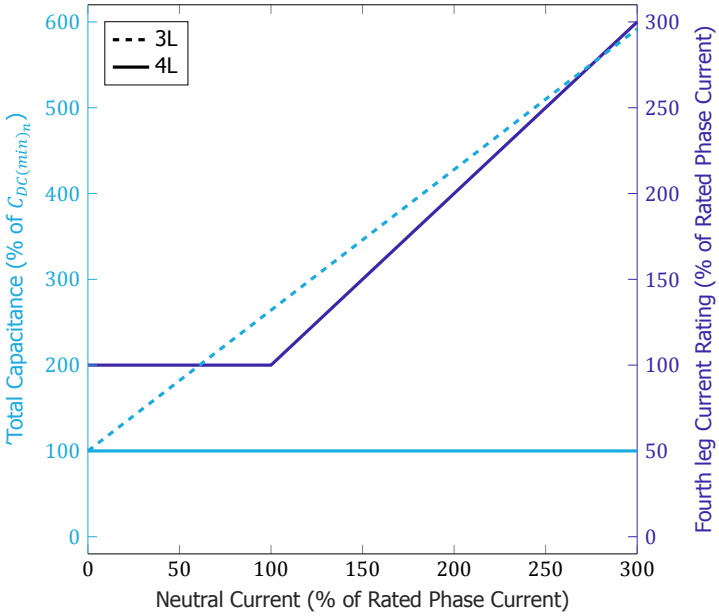


Figure 3.14: Capacitance and fourth-leg current rating for the 3L & 4L configuration

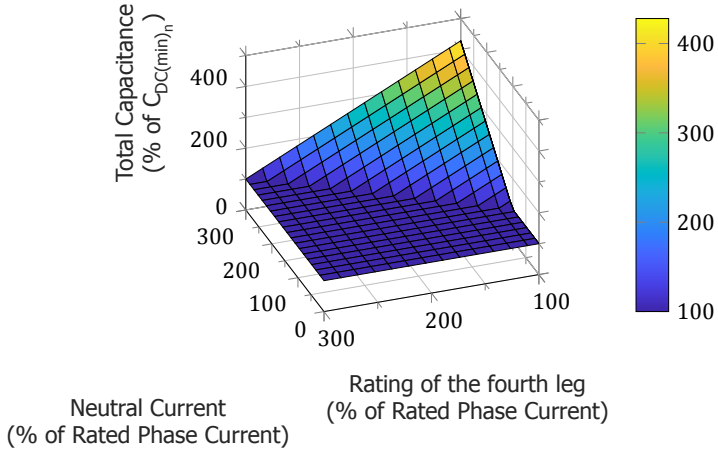


Figure 3.15: Capacitance requirement and fourth-leg current rating for 4L-SC Configuration

4

Control Strategy

The converter considered for this application is the basic 2-level converter with different configurations for the neutral current. The difference between the 3L, 4L and 4L-SC were covered in detail in Chapter 2. The configurations considered are presented in Fig. 4.1. The only difference is the DC-link and the neutral connection.

In this chapter, the design of the control strategy, for both the three-leg and four-leg configurations are explored.

4.1. Average equivalent circuit and dynamic equations

Based on Fig. 4.2, the average equivalent circuit of the converter is derived. This average equivalent circuit helps deriving the dynamic equations which determine the operation of the converter.

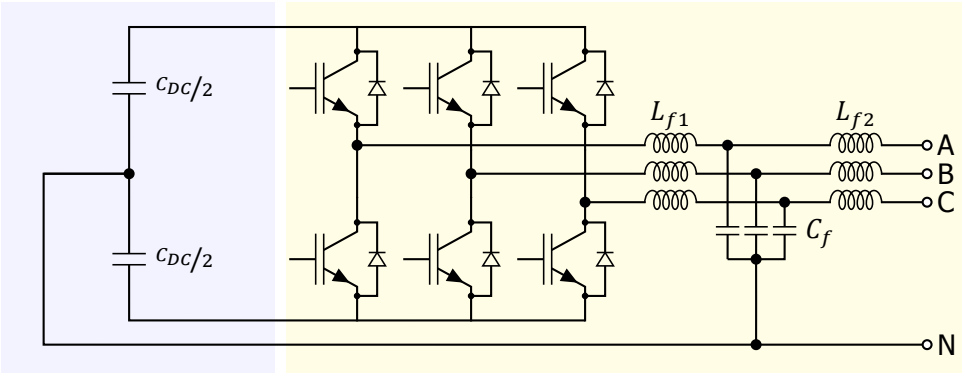
The average equivalent circuit of the converter is derived at fundamental frequency, considering the switching frequency is much higher. This model can be derived in both the stationary (abc) reference frame and the synchronous ($dq0$) reference frame.

4.1.1. Stationary Reference Frame

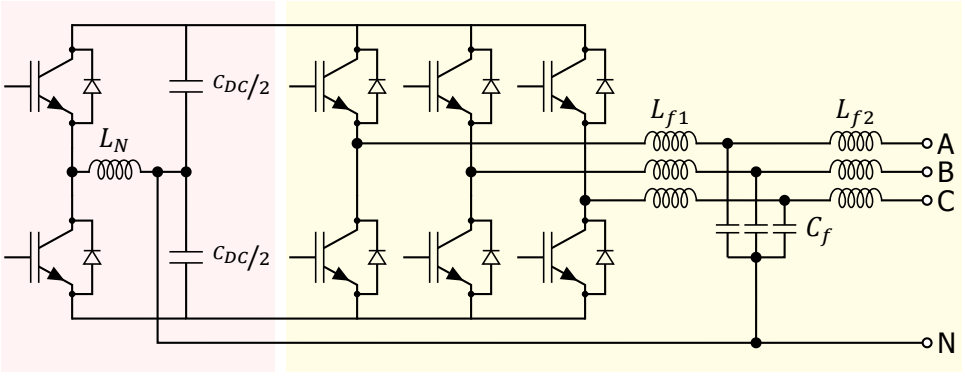
In the stationary reference frame, the per-phase average-equivalent circuit is given in Fig. 4.3.

From Fig. 4.3, dynamic equations of the converter are obtained as shown in (4.1) to (4.4) [36]:

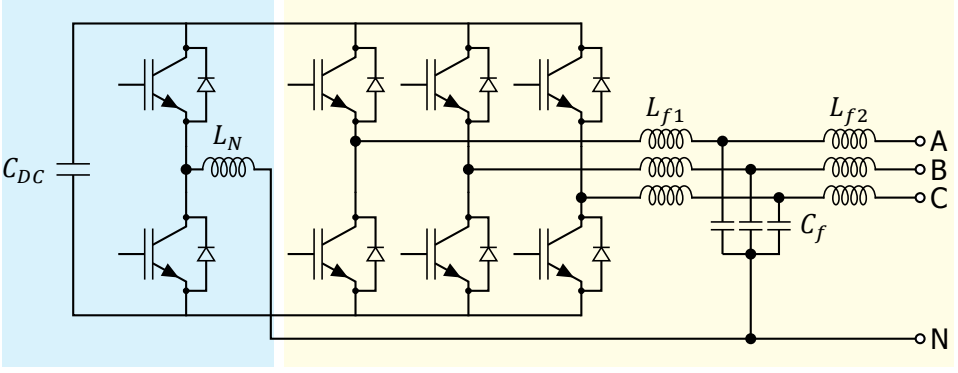
$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{dt}}I_{f_{ABC}} = \frac{D_{ABC}}{L_f}V_{DC} - \frac{R_f}{L_f}I_{f_{ABC}} - \frac{R_d}{L_f}(I_{f_{ABC}} - I_{g_{ABC}}) \\ - \frac{1}{L_f}V_{C_{f,ABC}} + \frac{L_{Nf}}{L_f}\frac{\mathrm{d}}{\mathrm{dt}}I_{Nf} + \frac{R_{Nf}}{L_f}I_{Nf}\end{aligned} \tag{4.1}$$



(a) 3L



(b) 4L-SC



(c) 4L

Figure 4.1: The three configurations of the converter

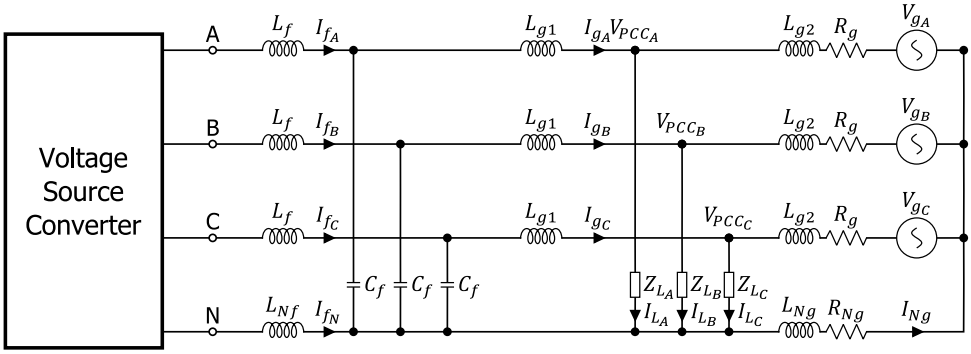


Figure 4.2: Grid-connected Voltage Source converter with LCL filter

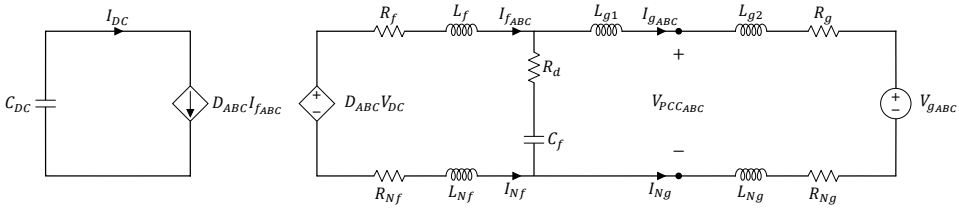


Figure 4.3: Per-phase average-equivalent circuit of the converter

$$\frac{\mathrm{d}}{\mathrm{d}t}I_{g_{ABC}} = \frac{1}{L_g}V_{C_{f,ABC}} - \frac{R_g}{L_g}I_{g_{ABC}} + \frac{R_d}{L_g}(I_{f_{ABC}} - I_{g_{ABC}}) - \frac{1}{L_g}V_{g_{ABC}} + \frac{L_{Ng}}{L_g}\frac{\mathrm{d}}{\mathrm{d}t}I_{Ng} + \frac{R_g}{L_{Ng}}I_{Ng} \tag{4.2}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{C_{f,ABC}} = \frac{1}{C_f}(I_{f_{ABC}} - I_{g_{ABC}}) \tag{4.3}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{DC} = -\frac{1}{C_{DC}}D_{ABC}^{T}I_{f_{ABC}} \tag{4.4}$$

where:

$$I_{f_{ABC}} = \begin{bmatrix} I_{f_A} & I_{f_B} & I_{f_C} \end{bmatrix}^T$$
$$I_{g_{ABC}} = \begin{bmatrix} I_{g_A} & I_{g_B} & I_{g_C} \end{bmatrix}^T$$
$$V_{g_{ABC}} = \begin{bmatrix} V_{g_A} & V_{g_B} & V_{g_C} \end{bmatrix}^T$$
$$V_{C_{f,ABC}} = \begin{bmatrix} V_{C_{f,A}} & V_{C_{f,B}} & V_{C_{f,C}} \end{bmatrix}^T$$
$$D_{ABC} = \begin{bmatrix} D_A & D_B & D_C \end{bmatrix}^T$$

4.1.2. Synchronous Reference Frame

In the synchronous reference frame, the equivalent-circuit is given in Fig. 4.4.

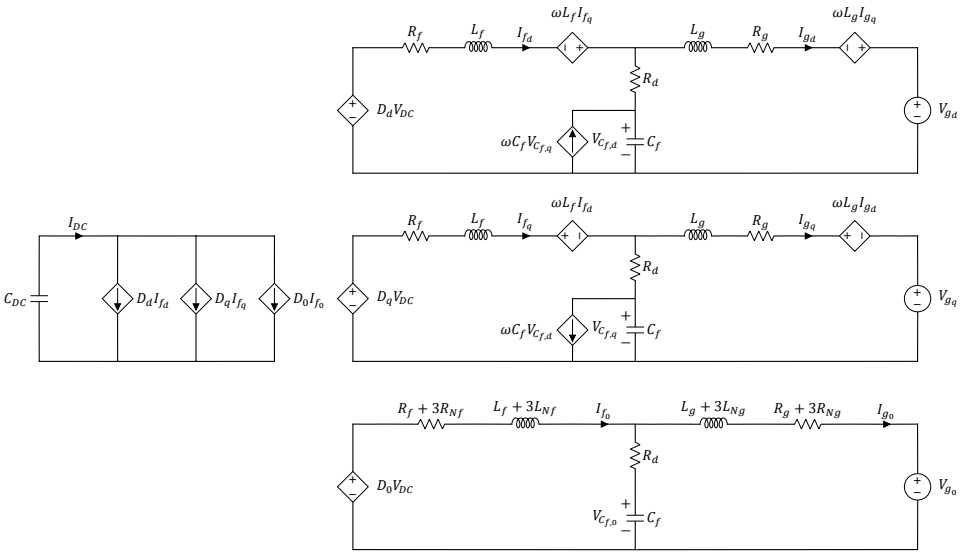


Figure 4.4: Average-equivalent circuit of the converter in $dq0$ reference frame

From Fig. 4.4, dynamic equations of the converter are obtained as shown in (4.5) to (4.8) [36]:

$$\frac{\mathrm{d}}{\mathrm{d}t}I_{f_{dq0}} = G_{L_f}V_{DC}D_{dq0} - G_{R_f}I_{f_{dq0}} - G_{L_g}R_d(I_{f_{dq0}} - I_{g_{dq0}}) - G_{L_f}V_{C_{f,dq0}} + \omega I'_{f_{dq0}} \tag{4.5}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}I_{g_{dq0}} = G_{L_g}V_{C_{f,dq0}} - G_{R_g}I_{g_{dq0}} + G_{L_g}R_d(I_{f_{dq0}} - I_{g_{dq0}}) - G_{L_g}V_{g_{dq0}} + \omega I'_{g_{dq0}} \tag{4.6}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{C_{f,dq0}} = \frac{1}{C_f}(I_{f_{dq0}} - I_{g_{dq0}}) + \omega V'_{C_{f,dq0}} \tag{4.7}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{DC} = -\frac{1}{C_{DC}}D^T_{dq0}I_{f_{dq0}} \tag{4.8}$$

where:

$$
\begin{aligned}
I_{f_{dq0}} &= \begin{bmatrix} I_{f_d} & I_{f_q} & I_{f_0} \end{bmatrix}^T \\
I'_{f_{dq0}} &= \begin{bmatrix} I_{f_q} & -I_{f_d} & 0 \end{bmatrix}^T \\
I_{g_{dq0}} &= \begin{bmatrix} I_{g_d} & I_{g_q} & I_{g_0} \end{bmatrix}^T \\
I'_{g_{dq0}} &= \begin{bmatrix} I_{g_q} & -I_{g_d} & 0 \end{bmatrix}^T \\
V_{g_{dq0}} &= \begin{bmatrix} V_{g_d} & V_{g_q} & V_{g_0} \end{bmatrix}^T \\
V_{C_{f,dq0}} &= \begin{bmatrix} V_{C_{f,d}} & V_{C_{f,q}} & V_{C_{f,0}} \end{bmatrix}^T \\
V'_{C_{f,dq0}} &= \begin{bmatrix} V_{C_{f,q}} & -V_{C_{f,d}} & 0 \end{bmatrix}^T \\
D_{dq0} &= \begin{bmatrix} D_d & D_q & D_0 \end{bmatrix}^T
\end{aligned}
$$

$$
G_{L_f} = \begin{bmatrix} \frac{1}{L_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f + 3L_{Nf}} \end{bmatrix}
$$

$$
G_{R_f} = \begin{bmatrix} \frac{R_f}{L_f} & 0 & 0 \\ 0 & \frac{R_f}{L_f} & 0 \\ 0 & 0 & \frac{R_f + 3R_{Nf}}{L_f + 3L_{Nf}} \end{bmatrix}
$$

$$
G_{L_g} = \begin{bmatrix} \frac{1}{L_g} & 0 & 0 \\ 0 & \frac{1}{L_g} & 0 \\ 0 & 0 & \frac{1}{L_g + 3L_{Ng}} \end{bmatrix}
$$

$$
G_{R_g} = \begin{bmatrix} \frac{R_g}{L_g} & 0 & 0 \\ 0 & \frac{R_g}{L_g} & 0 \\ 0 & 0 & \frac{R_g + 3R_{Ng}}{L_g + 3L_{Ng}} \end{bmatrix}
$$

4.2. Control of the converter

This converter is designed to control the grid current in a 3P-4W system. This would mean that, under balanced Point of Common Coupling (PCC) voltage, it works as an ideal Power Redistributor. Under unbalanced PCC voltage, the line currents would still be appropriately compensated. However, the power may not be fully compensated due to the unbalanced voltages. This is chosen since:

- The upstream PCC voltages in a Power System are generally balanced with slight unbalances, which should not affect the operation of the converter.
- The current compensation ensures that a balanced sinusoidal current is drawn from the grid, which can be advantageous from the grid operator point-of-view.

Based on the above chosen current control strategy, the control of the converter involves the following:

1. Current Controller
2. DC-Link Voltage Controller
3. Neutral Current Controller

The current and DC-link voltage controller design is the same for both the three-leg and four-leg configurations. The neutral current control is where the strategy changes depending on converter configuration. The overall control scheme is presented in Fig. 4.5.

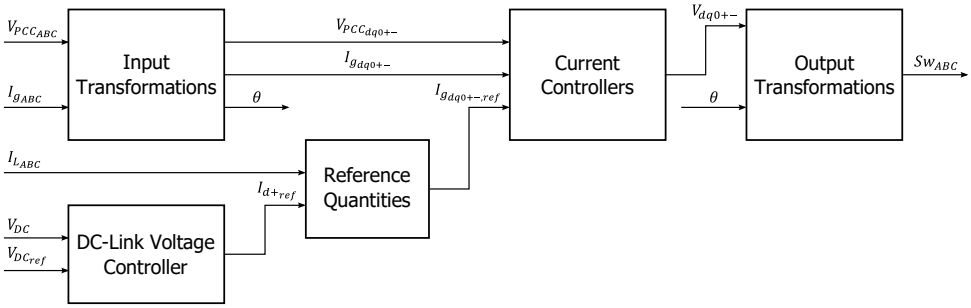


Figure 4.5: Overall Control Scheme

4.2.1. Current Controller

The control of the current is done in the double-synchronous reference frame to compensate the positive and negative-sequence components of currents separately and accurately.

4.2.1.1. Double Synchronous Frame Transformation

The controller input quantities in the abc reference frame are transformed to the rotating $dq0$ reference frame. The control of positive and negative sequence components require two reference frames which rotate at the fundamental frequency but in the opposite direction relative to each other. This is achieved by the use of a PLL, which generates the reference angle for the synchronous reference frame. The negative of the angle generated by this PLL is given as reference for the negative-sequence reference frame [37]. Based on this, the input and output quantities transformation between abc and $dq0$ quantities are carried out respectively as shown in Fig. 4.6.

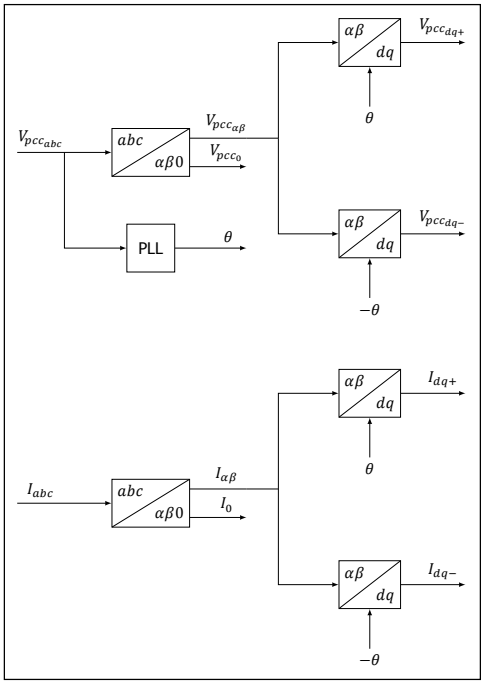
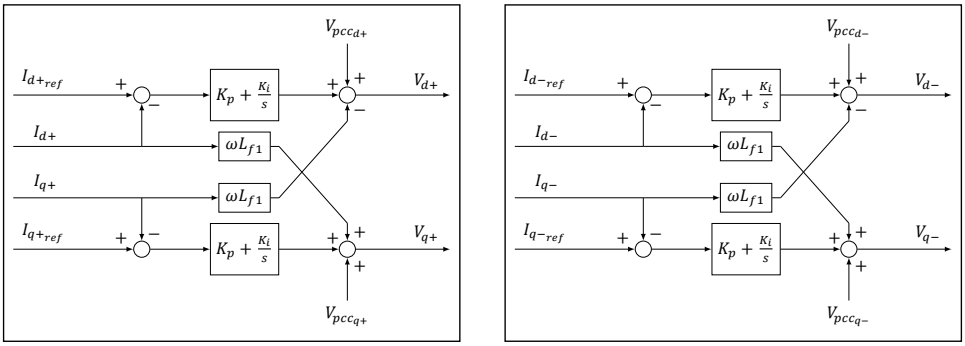


Figure 4.6: abc to $dq0$ transformation of input quantities

4.2.1.2. Positive and Negative-Sequence Current Controller

In the respective $dq0$ reference frames, the positive and negative-sequence components of currents appear as DC quantities with a 100 Hz ripple. The ripple is caused due to the presence of negative-sequence components in the positive-sequence rotating reference frame and vice versa. Since the control quantity is DC quantities, a simple PI controller can be used. In addition to the PI control, feed-forward is added for the PCC voltage. Additionally, the decoupling of the inductor currents in the dq reference frame is also compensated as a feed-forward. This implementation of current controller is shown in Fig. 4.7.



(a) Positive-Sequence **(b)** Negative-Sequence

Figure 4.7: Double Synchronous Reference Frame Current Controllers

4.2.1.3. Zero-Sequence Current Controller

The zero-sequence current is controlled by using a simple PI controller as well. This controls the amount of neutral current compensated by the converter. Since a PI controller can have steady-state error at non-DC frequencies, the controller can be tuned for higher gain at necessary frequency to compensate for the error and higher-order harmonics if necessary. The implementation is shown in Fig. 4.8.

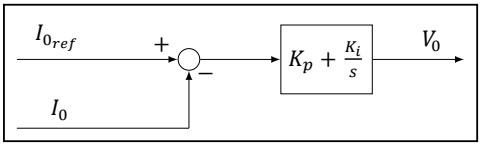


Figure 4.8: Zero-Sequence Current Controller

4.2.1.4. Converter Modulation

The output of the three current-controllers are the converter voltage references which need to be produced by the converter. Thus, the outputs are converted to the stationary reference frame, and added together to get the converter voltage reference. This is then modulated, to provide the firing pulses to the gate drivers of the Voltage Source Converter (VSC). This output transformation is shown in Fig. 4.9.

4.2.2. DC-Link Voltage Control

The overall DC-link voltage is controlled by controlling the active-power transfer. Considering the sine-based Park transformation used, the active power transfer in case of balanced voltage at the PCC is controlled by controlling I_{d+}. Thus, the DC-link voltage is controlled using a PI controller, and it's output is used as the reference for the positive-sequence direct-axis current. This is implemented as shown in Fig. 4.10. It is to be noted, that in the application considered, there is

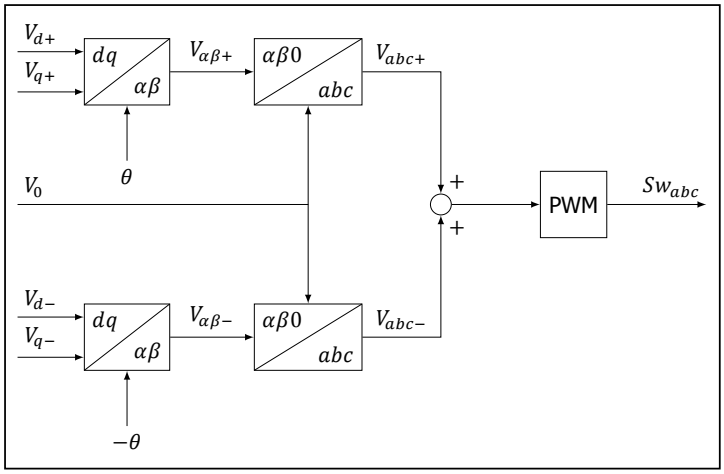


Figure 4.9: Output Transformation

no active-power exchange between the DC-link and the grid. However, this can be additionally added in by simply controlling the positive-sequence direct-axis current.

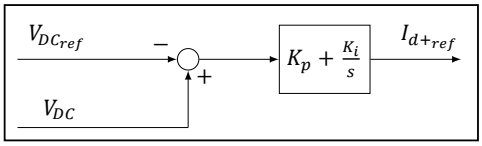


Figure 4.10: DC-Link Voltage Controller

4.2.3. Control of Neutral Current

The neutral current control varies between the configuration of converter considered. In the 3L configuration, the neutral current flows through the DC-Link capacitance. However, in the 4L and 4L-SC configuration, the fourth-leg is modulated such that the neutral current flows through the fourth-leg. The control of all these configurations are explored in this section. In the split-capacitor topologies, the voltages across the upper and lower capacitor need to be maintained constant and exactly half of each other on average. In the non-split version, only a single voltage controller is necessary, and the neutral point is controlled directly by the fourth leg.

4.2.3.1. 3L Configuration

In the three-leg configuration, since the neutral current flows through the capacitor, the voltages across the upper and lower capacitor cannot exactly be maintained constant. There will be a ripple in the voltage difference, which essentially allows

for the flow of the neutral current through the capacitors. There are two ways in which the control can be done.

- The overall DC-link voltage is controlled with one DC-link voltage controller as mentioned in Section 4.2.2. In this method, the neutral current controller, would control the difference of voltage between the upper and lower capacitors.
- The voltages across upper and lower capacitors are controlled separately essentially, splitting the DC-link voltage control mentioned in Section 4.2.2 into two parts.

In this design, the second control method is chosen for the ease of implementation, considering the same PI control is used for both voltage controllers. The implementation is done as per Fig. 4.11.

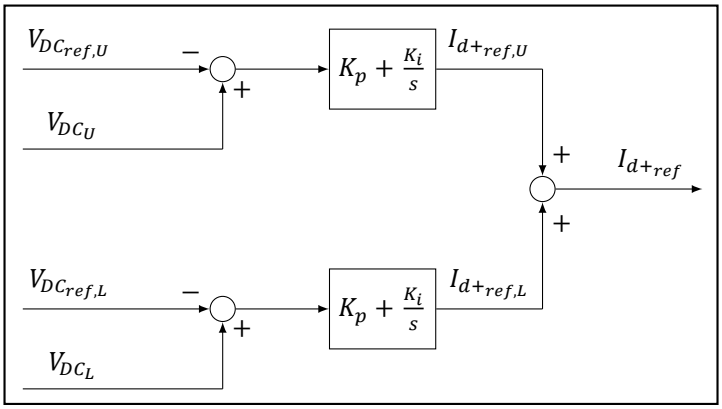


Figure 4.11: Voltage Control in 3-Leg configuration

4.2.3.2. 4L-SC Configuration

In the 4L-SC configuration, the neutral voltage is controlled by the fourth leg. The neutral current flowing through the fourth leg can be controlled by controlling the voltage across the neutral inductor L_N. The major advantage of this approach is the fact the system neutral is maintained almost constant with the mid-point of the DC-link capacitance. This ensures a stable system. The control of the fourth-leg is done with two current control loops.

- An inner current control loop, which controls the capacitor current, i_C. This current should be almost zero, to ensure the neutral current passes through the fourth-leg and not the capacitor.
- An outer voltage-error control loop which ensures that the voltage difference between the upper and lower capacitor is controlled to be almost zero.

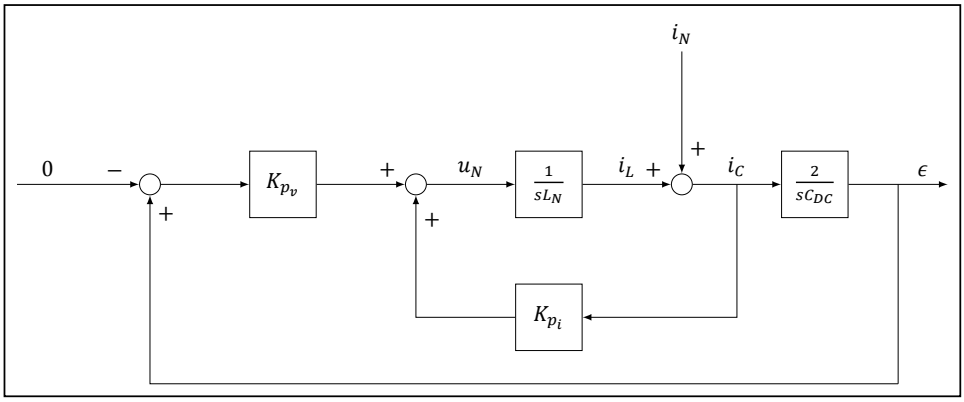


Figure 4.12: Control of the 4th Leg

The realisation of this control scheme is shown in Fig. 4.12. In this control scheme, the controller gains are set as per the procedure laid out in [38]. The strategy is based on the assumption that the inductor and capacitances are ideal, and thus, the control can be achieved by just using a Proportional Controller. If necessary, any steady-state error can be corrected by implementing an Integral controller in addition. The gain of the inner current-loop, is set based on (4.9).

$$K_{p_i} = \omega_c L_N \tag{4.9}$$

where ω_c is the control bandwidth, which needs to be lower than the switching frequency. The proportional gain of the outer voltage-loop is set based on (4.10):

$$K_{p_v} = \frac{\omega_c^2 L_N C_{DC}}{2} \tag{4.10}$$

Based on this, the neutral current is redirected through the fourth leg of the converter as opposed to the DC-link capacitance.

4.2.4. 4L Configuration

In the configuration where the capacitor is not split, the system neutral point is directly controlled by controlling the fourth-leg. Thus, for simple SPWM based control of the converter, a constant reference of 0 is provided.

The above-mentioned control strategy will help control the operation of the converter. The advantage of the mentioned control scheme is the completely independent Positive, Negative and Zero-sequence current control.

4.3. Current Controller Frequency Response

Based on the above mentioned strategy, the current control frequency response and stability needs to be verified. This is done based on bode analysis of the converter. For this, initially, the transfer function is formulated based on the converter

parameters and then the stability analysis on open-loop and closed-loop response is checked.

4.3.1. Converter Parameters - Simulation

A simulation model is built in PLECS. The converter parameters are as follows:

Parameter	Symbol	Value
PCC Phase Voltage (RMS)	V_{pcc}	230 V
Converter Phase Current	I_f	20 A
DC-Link Voltage	V_{DC}	800 V
DC-Link capacitance	C_{DC}	53.3 mF
Switching frequency	f_{sw}	11 kHz
LCL Filter - Converter-side Inductance	L_{f1}	897 μH
LCL Filter - Grid-side Inductance	L_{f2}	135 μH
LCL Filter - Capacitance	C_f	753 nF

Table 4.1: Converter Parameters

Based on the above converters, the transfer functions are formulated and henceforth, the frequency domain analysis is carried out.

4.3.2. Transfer Function of VSC with LCL Filter

The transfer function governing the LCL filter is:

$$G_{LCL}(s) = \frac{I_g(s)}{V_{VSC}(s)} = \frac{1}{s^3 L_{f1} L_{f2} C_f + s(L_{f1} + L_{f2})} \tag{4.11}$$

In addition, the transfer function of the PWM converter is just a time delay due to the sampling. In case of symmetrical sampling, this delay is 1.5 times the switching time-period. This delay is represented by:

$$G_{VSC}(s) = \frac{V_{VSC}(s)}{V_{ref}(s)} = e^{-1.5 T_s s} \tag{4.12}$$

where T_s is the switching time period. The open-loop transfer function of the system is given by:

$$G_{OL}(s) = G_{LCL}(s) \cdot G_{VSC}(s) \tag{4.13}$$

Based on (4.13), the bode plot of the converter is plotted in Fig. 4.13.
From Fig. 4.13, the open-loop stability margins are obtained as follows:

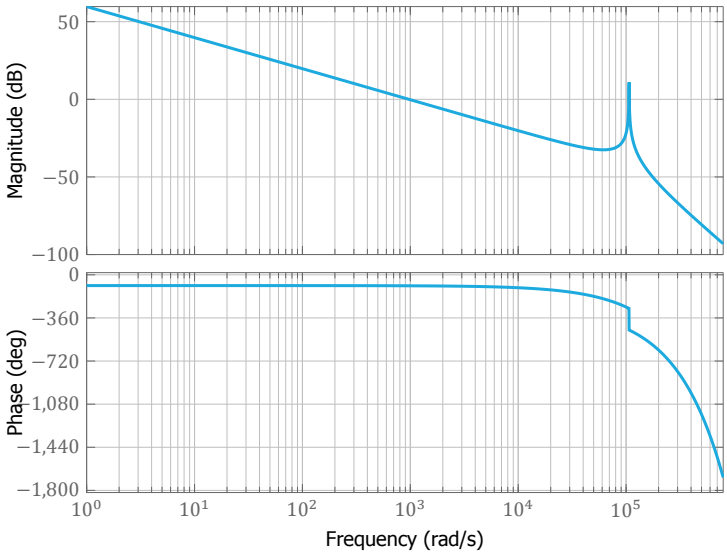


Figure 4.13: Open-Loop Response

Table 4.2: Open-Loop Stability Margins

Parameter	Value	Frequency
Gain Margin	40.3 dB	50,238 rad/s
Phase Margin	78°	10,702 rad/s

From the stability margins, it can be seen that the chosen LCL filter, operated with a converter at the chosen switching frequency is a stable system. Based on the plant model in (4.13), the closed-loop control stability can be verified by multiplying the controller gains with the plant model.

4.3.3. PI Current Controller

The PI-controller is used to control the Positive and Negative-sequence currents in their respective synchronous reference frames. The controller gain for a PI-controller is:

$$G_{PI}(s) = \frac{V_{ref}(s)}{I_g(s)} = K_{p_i} + \frac{K_{i_i}}{s} \tag{4.14}$$

where K_{p_i} is the proportional gain and K_{i_i} is the integral gain of the PI current controller. The controller gains for this converter is obtained through MATLAB PID Tuner as follows:

Table 4.3: PI Current Controller Gains

Parameter	Symbol	Value
Proportional Gain	K_{p_i}	13.937
Integral Gain	K_{i_i}	1012.5

Combining (4.13) and (4.14), the overall closed-loop control transfer function is given by,

$$G_{CL_{PI}}(s) = G_{PI}(s) \cdot G_{LCL}(s) \cdot G_{VSC}(s) \tag{4.15}$$

Based on (4.15), the bode plot of the closed-loop current controlled converter is plotted in Fig. 4.14.

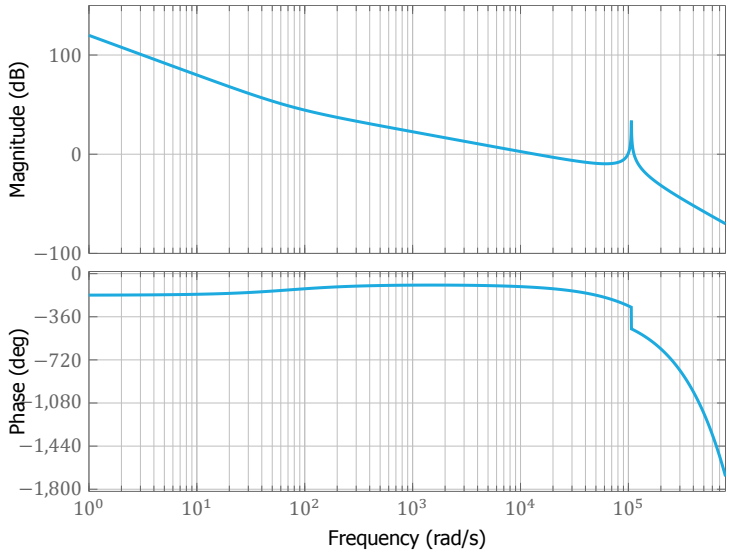


Figure 4.14: Closed-Loop Response - PI Controller

From Fig. 4.14, the closed-loop stability margins are obtained as follows:

Table 4.4: Closed-Loop Stability Margins - PI Controller

Parameter	Value	Frequency
Gain Margin	2.89 dB	50,219 rad/s
Phase Margin	65°	13,737 rad/s

From the stability margins, it can be seen that the current controller is stable. Thus, this configuration of PI current controller is used for the simulation.

Based on the above-mentioned stability analysis, it can be seen that the controllers are optimally tuned to have highest gain at their respective operating points. In the case of the PI-controller, the maximum gain is necessary for the DC quantities, and it is important that the reference signals do not have the 100 Hz component, which could be filtered out using a Low-Pass Filter (LPF). If necessary, additional compensation can be added especially to the zero-sequence controller, by tuning it to operate at specific resonant frequencies. This can help compensate for specific harmonics as and when necessary.

4.4. Conclusion

In this chapter, control strategy for controlling a power redistributor was discussed. The converter control was achieved in the double synchronous reference frame, and thus, the control of the sequence components of current was achieved by the use of PI controllers. The controller stability was also checked and verified for the given operating point. In addition, for the three different configurations, the DC-link voltage control method, as well as control of the fourth leg for the 4L-SC and 4L configurations were also presented.

5

Simulation of the Model

The configurations of the converter discussed, and the above-mentioned control strategy need to be tested. This is done by simulating the overall circuit in PLECS. PLECS is chosen considering the closed-loop control and electrical modelling can be done simultaneously, and in addition, the losses in the switches can also be directly estimated by the use of the device models from the manufacturer. This helps to simplify the estimation of the semiconductor losses in the converter.

This chapter will cover the development of the PLECS model, testing the converter at various operating points and plots of how the converter conditions the grid current.

5.1. 3L Configuration

Initially, the three-leg configuration of the converter is considered. The main circuit diagram is shown in Fig. 5.1.

From Fig. 5.1, the following are the major points of interest:

- The ideal AC grid is connected to the PCC through a Grid Impedance. In this model, the Grid Impedance is taken to be very small to simulate a strong grid : R_g = 0.1 Ω and L_g = 100 µH.
- The VSC is connected to the PCC through the LCL filter.
- The unbalanced loads are connected to the PCC with a neutral return point back to the AC grid as well as the VSC.
- A heat sink is placed under the VSC to set the ambient temperature at 40 °C. This is for more accurate loss modelling of the switches.
- The switches used are the C3M0120090J [39] and its thermal characteristics are loaded into the PLECS model. This switch is chosen considering the SiC technology, which allows for higher switching frequency operation and low

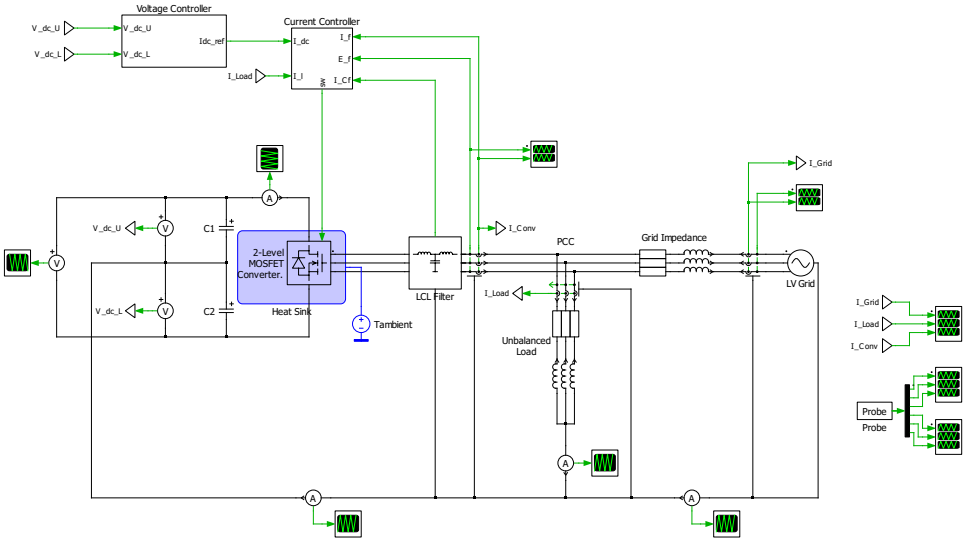


Figure 5.1: The Three-Leg Configuration of Power Redistributor - PLECS Model

on-state resistance. This allows for significantly low-losses for the converter's rated voltage and current.

The current controller is set-up as per the control loops specified in Section 4.2.1. The only difference is the use of LPFs in the measurement transformation, to ensure the Positive and Negative-sequence components are provided as DC to the controllers in their respective synchronous reference frames. This is because the reference values are measured load currents which have both Positive and Negative sequence components. For example, in the measurements for the positive-sequence components, the measurement transformation is done as shown in Fig. 5.2.

5.1.1. Grid Current Compensation

The power redistribution works by compensating the following components:

- Reactive component of Positive-sequence current.
- Active and Reactive components of Negative-sequence current.
- Active and Reactive components of Zero-sequence currents.

From the above, the active power transfer between the DC-link and the AC grid is zero. To represent the compensation, one operating point is chosen for representing the operation of the converter:

- Phase A : 6.67 A at unity PF
- Phase B : 13.33 A at 0.68 leading PF

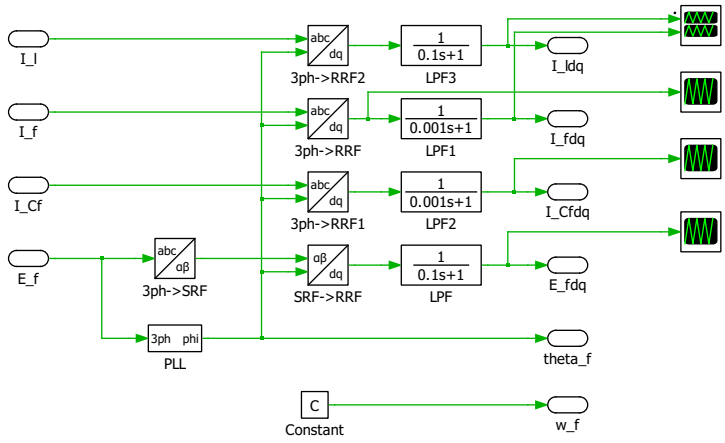


Figure 5.2: Measurement transformation with filters

5

- Phase C : 20 A at 0.68 lagging PF

The converter operation is shown in Fig. 5.3 where it can be observed that the unbalanced phase currents are balanced once the converter compensates the sequence components.

5.1.2. Unbalance Compensation

The converter's primary functionality is to compensate the unbalance in the grid current. The magnitude of unbalance based on sequence components was presented in (2.4) and (2.5). Based on this, the magnitude of unbalance before and after the compensation is tabulated in Table 5.1.

5.1.3. DC-Link Current

The DC-link current consists of additional 50 Hz and 100 Hz harmonic components due to the presence of Zero-sequence and Negative-sequence components respectively. This is derived as per (3.8) and (3.9), and the same can be verified by the simulation as well. The DC-link current for the chosen operating point is shown in Fig. 5.4. From the waveform in Fig. 5.4, by Fourier analysis, the frequency spectrum of the waveform can be obtained. As discussed in Section 3.3, the positive-sequence component of the current will be at the switching frequency due to no active power transfer to/from the DC-link, whereas, the Negative and zero-sequence components will be a low-frequency harmonic of 100 Hz and 50 Hz respectively. Thus, the frequency spectrum up to 500 Hz of this waveform is plotted in Fig. 5.5. From Fig. 5.5, it can be observed that only the 50 Hz and 100 Hz components are present significantly in the low-frequency spectrum corresponding to the Zero-sequence and Negative-sequence components respectively. The DC-link current harmonic RMS and the 50 Hz and 100 Hz components for various operating points are shown in Table 5.2.

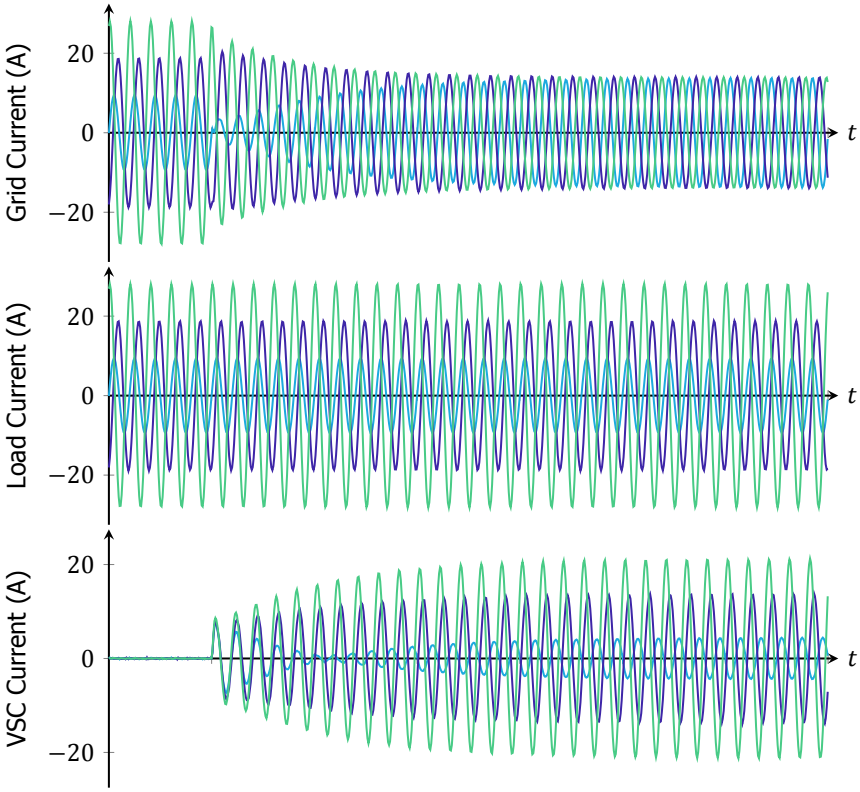


Figure 5.3: Grid Current Compensation by the Converter

Table 5.1: Magnitude of Unbalance before and after compensation

Load Current			**Unbalance$_n$(%)**		**Unbalance$_0$(%)**	
I_A(A)	I_B(A)	I_C(A)	**Before**	**After**	**Before**	**After**
1.05	17.89	20.00	46	0.24	46	0.25
9.47	4.21	20.00	41	0.12	41	0.27
14.74	8.42	20.00	23	0.25	23	0.09
I_A, I_B, I_C(A)	PF_B	PF_C	**Before**	**After**	**Before**	**After**
4.21	0.26	-0.26	61	0.14	158	1.21
11.58	0.11	-0.11	68	0.32	216	1.30
18.95	0.68	-0.68	40	0.13	67	0.44
20.00	-0.11	-0.47	42	0.15	57	0.67
20.00	-0.47	-0.11	57	0.14	42	0.53
20.00	-0.95	-0.47	38	0.24	30	0.28
20.00	-0.47	-0.95	30	0.27	38	0.34

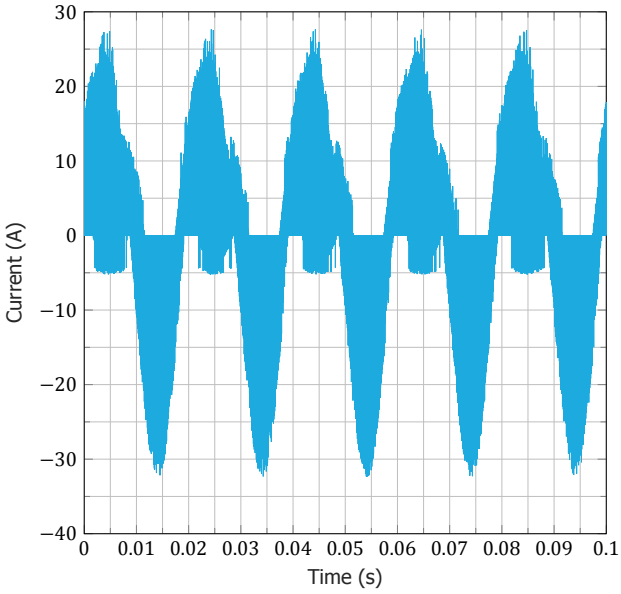


Figure 5.4: DC-Link Current Waveform

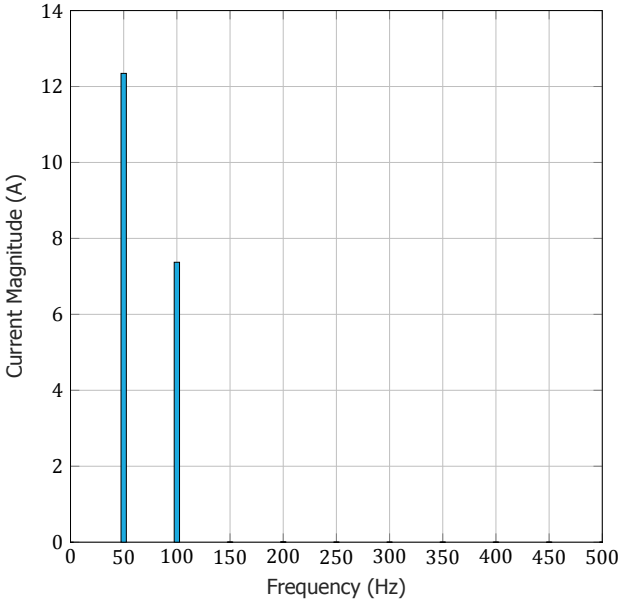


Figure 5.5: DC-Link Current Frequency Spectrum

Table 5.2: DC-Link Current Harmonic Components

Load Current			DC-Link Harmonics		
I_A(A)	I_B(A)	I_C(A)	$\tilde{I}_{DC_{rms}}$(A)	$I_{DC_{50}}$(A)	$I_{DC_{100}}$(A)
1.05	17.89	20.00	11.04	8.95	3.60
9.47	4.21	20.00	8.61	6.93	2.80
14.74	8.42	20.00	6.27	4.99	2.01
I_A, I_B, I_C(A)	PF_B	PF_C	$\tilde{I}_{DC_{rms}}$(A)	$I_{DC_{50}}$(A)	$I_{DC_{100}}$(A)
4.21	0.26	-0.26	6.39	5.07	0.80
11.58	0.11	-0.11	18.55	15.13	1.93
18.95	0.68	-0.68	19.03	14.87	3.59
20.00	-0.11	-0.47	18.52	13.92	4.19
20.00	-0.47	-0.11	15.66	10.14	5.80
20.00	-0.95	-0.47	11.92	7.93	4.21
20.00	-0.47	-0.95	13.69	10.23	3.26

The values of DC-link harmonics by PLECS simulation is compared with the mathematical model derived in Section 3.3. It was observed that the maximum errors were as per Table 5.3.

Table 5.3: Error in estimation of DC-Link Harmonics based on (3.10)

Parameter	$\tilde{I}_{DC_{rms}}$(A)	$I_{DC_{50}}$(A)	$I_{DC_{100}}$(A)
Error	0.41%	0.41%	0.86%

The errors are found to be less than 1% and thus, the mathematical model is validated.

5.1.4. THD

The THD of the grid-current due to the converter compensation is measured at the grid-side. This is done to ensure that the converter does not inject harmonics of it's own into the power system to ensure high power quality in the grid. The average THD measured in the three-phase grid current is tabulated in Table 5.4.

From Table 5.4, it can be observed that the current harmonics are well under control for this operating region. If necessary, in a real-world scenario, since the converter is essentially operating in a current-control mode, observed harmonics can also be compensated using the converter by tuning the converter to reject the particular higher-order harmonics.

5.1.5. Semiconductor Losses

The losses in the converter are measured by considering the C3M0120090J switch by CREE [39]. The MOSFET model is loaded into PLECS, and the individual switch

Table 5.4: THD in Grid Current

I_A(A)	I_B(A)	I_C(A)	**THD (%)**
1.05	17.89	20.00	0.48
9.47	4.21	20.00	0.48
14.74	8.42	20.00	0.31
I_A, I_B, I_C(A)	PF_B	PF_C	**THD (%)**
4.21	0.26	-0.26	2.46
11.58	0.11	-0.11	1.00
18.95	0.68	-0.68	0.40
20.00	-0.11	-0.47	0.67
20.00	-0.47	-0.11	0.81
20.00	-0.95	-0.47	0.45
20.00	-0.47	-0.95	0.39

losses are measured. In this section, a loss (%) is presented, which is defined as follows:

$$\text{Loss (\%)} = \frac{\text{Losses in the Switches}}{\text{Total Load Power}} \tag{5.1}$$

This gives an idea as to how much power loss is there as a function of the total power in the system. For the 3-leg configuration, the Loss (%) is tabulated in Table 5.5. Based on the loss (%), it is seen that unless there is a high-level of

Table 5.5: Loss (%) in 3-Leg Configuration

I_A(A)	I_B(A)	I_C(A)	**Loss (%)**
1.05	17.89	20.00	0.29
9.47	4.21	20.00	0.22
14.74	8.42	20.00	0.11
I_A, I_B, I_C(A)	PF_B	PF_C	**Loss (%)**
4.21	0.26	-0.26	0.30
11.58	0.11	-0.11	0.48
18.95	0.68	-0.68	0.34
20.00	-0.11	-0.47	0.62
20.00	-0.47	-0.11	0.62
20.00	-0.95	-0.47	0.32
20.00	-0.47	-0.95	0.32

unbalance, the converter losses are within 1% of the grid power.

5.1.6. Loss of a Phase

If there is a fault on one of the phases, the converter can still compensate the power in the other two phases, and make sure a balanced 3-phase current is drawn from the grid. To show this, the converter is operated in the following conditions:

- Phase A : 0 A
- Phase B : 20 A at 0.68 leading PF
- Phase C : 20 A at 0.68 lagging PF

This is shown in Fig. 5.6. It can be observed that the converter compensates the loss of phase appropriately in the grid-side, and ensures a three-phase balanced current is drawn from the grid. Thus, this converter helps improve the reliability of the system as well by compensating the loss of phase appropriately.

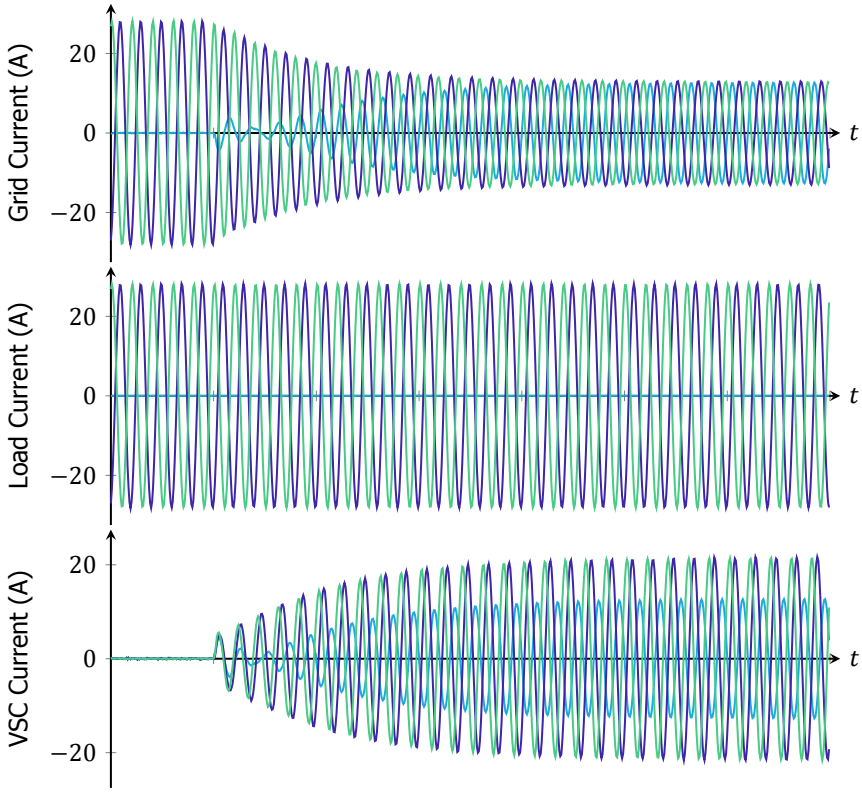


Figure 5.6: Grid Current Compensation by the Converter during Loss of a Phase

5.1.7. Observations

Thus, the three-leg converter compensates the three-phase power in the system. Various parameters were taken and considered under different operating conditions.

It is found that the converter can compensate reliably under normal operating conditions as well as during extreme conditions such as the loss of a phase. Due to the use of a PI controller in the Zero-sequence current controller, there may be a small steady-state error. This can be eliminated, and additional harmonic compensation can also be achieved by tuning the current controllers to specific resonant frequencies to ensure better compensation.

5.2. Four-Leg Configuration

The four-leg configuration is an extension to the three-leg configuration discussed in Section 5.1. The only addition is the fourth-leg which can be connected in two ways as discussed before. The THD is similar for both configurations, since the current controller and the LCL filter in use are the same. The only changes from the three-leg configuration are:

- DC-Link current
- Semiconductor loss
- Neutral-Leg Control

5.2.1. DC-Link Current

Since the neutral-leg carries the Zero-sequence component, the DC-link current should only consist of the Negative-sequence component of current as low-frequency harmonic. The DC-Link current in the 4-leg converter consists of only the Negative-sequence component. Thus, the waveform is different as it only consists of a primary 100 Hz ripple. The waveform of the DC-link current in the 4L configuration is shown in Fig. 5.7.

From Fig. 5.7, the frequency spectrum of the current waveform can be derived. The low-frequency spectrum of this DC-link current is shown in Fig. 5.8. From Fig. 5.8, it can be observed that the main low-frequency ripple is at 100 Hz, corresponding to the Negative-sequence component of current. The Zero-sequence component is fully eliminated in the 4L configuration, and is redirected through the fourth-leg, which carries the neutral current. However, in the 4L-SC configuration, the amount of zero-sequence component passing through the neutral leg is controlled by the neutral-leg controller. Due to the presence of this additional controller, there may be steady-state error and thus, a small 50 Hz component might be introduced in the DC-link of the 4L-SC configuration.

In the four-leg configuration, due to the zero-sequence component being redirected, there are significant higher-order harmonics at the switching frequency, due to which the RMS value as calculated in (3.10) does not hold true anymore. This equation only considers the fundamental switching frequency, and does not consider the higher-order harmonics.

5.2.2. Semiconductor Loss

Due to the presence of the fourth-leg, the losses are significantly higher as compared to the three-leg configuration. Considering the fact that, neutral current

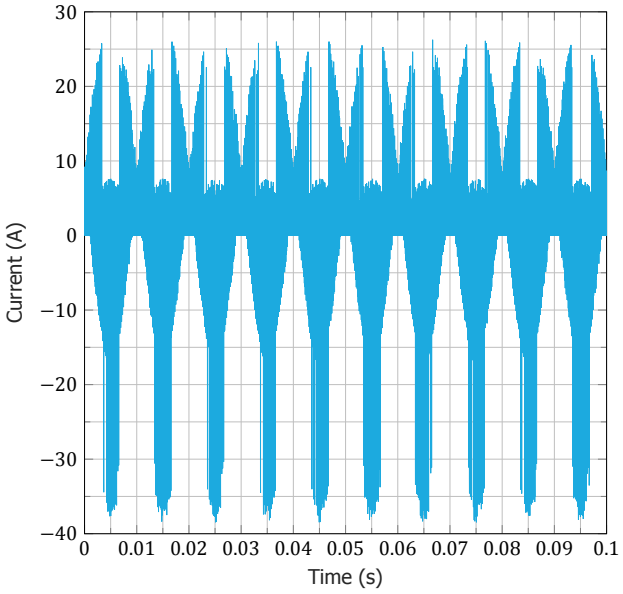


Figure 5.7: DC-Link Current Waveform - Four Leg

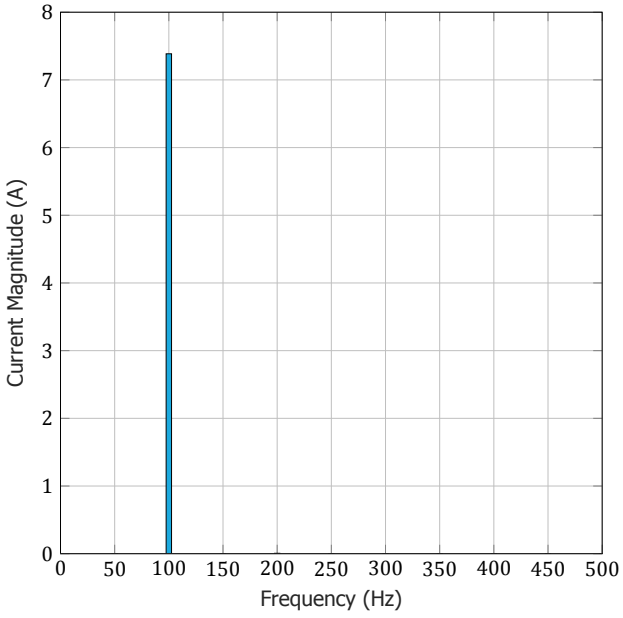


Figure 5.8: DC-Link Current (Low) Frequency Spectrum - Four Leg

can be up to 3 times the magnitude of phase current, the losses are also much higher than in other phase-legs. The loss(%) as presented in Section 5.1.5 is also calculated for the four-leg configuration and tabulated in Table 5.6.

Table 5.6: Loss (%) in 4-Leg Configurations

I_A(A)	I_B(A)	I_C(A)	**Loss (%) - 4L-SC**	**Loss (%) - 4L**
1.05	17.89	20.00	0.74	0.66
9.47	4.21	20.00	0.54	0.50
14.74	8.42	20.00	0.25	0.23
I_A, I_B, I_C(A)	PF_B	PF_C	**Loss (%) - 4L-SC**	**Loss (%) - 4L**
4.21	0.26	-0.26	0.79	0.74
11.58	0.11	-0.11	1.95	1.67
18.95	0.68	-0.68	1.20	1.04
20.00	-0.11	-0.47	1.34	1.20
20.00	-0.47	-0.11	0.99	0.93
20.00	-0.95	-0.47	0.55	0.51
20.00	-0.47	-0.95	0.69	0.63

From Table 5.6, it can be observed that the losses in the 4-leg configuration is significantly higher than that of the 3-leg configuration. This is because, the neutral current magnitude is quite large in comparison with the individual phase currents. In addition, this MOSFET is rated only for 20 A, but however, as shown in Section 3.1, the neutral current can be higher than even individual phase current. Thus, the simulation might over-estimate losses because the switches are not rated for such high current. However, the conclusion that losses are much higher still holds true, since the loss in the four-leg converter is always higher, even when the neutral current is within limits.

5.2.3. Neutral-Leg Controller

In the 4L-SC configuration, the neutral-leg controller essentially redirects the zero-sequence component of current through the neutral-leg by controlling the voltage across the neutral inductor L_N. The neutral inductor size, determines the amount of current ripple as well as DC-link voltage utilisation for the inductor. Thus, a tradeoff needs to be done in the selection of this inductor. In this converter, a neutral inductor of 1 mH is chosen. The operation of this controller in the 4L-SC topology can give a control over the amount of zero-sequence current passing through the neutral leg. This topology has an advantage that the converter can stil compensate for higher limits, even if the neutral leg is not designed to carry the higher neutral current if the DC-link has sufficient capacity.

5.3. Observations

All the three configurations of the converters are operated at the same points, compensating the same magnitude of unbalance. With these the following key points are observed.

- All the configurations do the main function of unbalance compensation in the grid. The THD, the unbalance compensation magnitude are all found to be similar for both the configurations.
- The DC-link current in the 4-leg configuration does not have the 50 Hz harmonic ripple, since the neutral current is redirected into the fourth-leg. Thus, the DC-link ripple in the 4-leg configuration is much lower than that of the 3-leg configuration. However, the fourth-leg controls the neutral point, and thus, some noise may be injected into the DC-link, which depends on the size of the neutral inductance in case of the 4L-SC configuration.
- The losses in the 4-leg configuration are significantly higher than that of the 3-leg configuration. This is essentially due to the fact that, in unbalanced conditions, the neutral current magnitude rises quite rapidly, and can even be up to 3 times the phase-current. This is the reason losses are high in the 4-leg configuration.
- The neutral point in the 4L configuration is subject to high EMC, and this can be observed from the neutral current of the converter in this configuration.

6

Conclusion

The concept of Phase Unbalance has long-existed in the Power System. With the proliferation of DERs and energy storage, this problem becomes a key point of focus. This thesis dealt with one of the methods of dealing with this problem, a Power Redistributor. In this thesis, the following research on a power redistributor was conducted.

- **Chapter 1** gave an introduction to the research topic, some background motivation and methods to tackle the phase-unbalance problem in LV distribution grids.
- **Chapter 2** gave a detailed analysis and working of a Power Redistributor device. The mathematical decomposition of unbalance was introduced, various topologies of the converter, and possible control strategies of the converter were explored in this chapter.
- **Chapter 3** dealt with the mathematical modelling of a converter. In this chapter, the major contribution was the DC-Link current ripple derivation which was dealt with in detail. In addition, operating limits of the converter, switch rating and capacitance derivation were dealt with in this chapter.
- **Chapter 4** dealt with the detailed design of the control loops used for the converter. The stability of the converter was also explored in this chapter.
- **Chapter 5** dealt with the simulation model of the converter and the various topologies under consideration. The topologies were compared on various chosen parameters by operating under different conditions, and the mathematical model of the converter was also verified.

This thesis aimed at answering the following research questions which are discussed below:

1. **What are the possible configurations of a converter suited for the realisation of a power redistributor for use in the LV distribution grids?**

   The various possible configurations such as two-level three-leg, two-level four-leg with and without split capacitor were discussed. Various advantages and disadvantages of these configurations, and their design were dealt with throughout the thesis.

2. **How does the sizing of the DC-link capacity change based on the configuration of converter selected?**

   The DC-link capacity requirement changes based on the configuration chosen. For the three-leg converter, the whole zero-sequence current flows through the DC-link and thus, should be rated as such. Whereas for the four-leg full capacitor configuration, zero-sequence current flows only through the fourth-leg and thus, its rating is variable based on the magnitude of unbalance compensation. For the four-leg split capacitor configuration, part of the zero-sequence current can be controlled to flow through the fourth leg and the rest can be redirected through the DC-link. This can thus, present interesting scenarios on which converter is chosen based on the end-user requirement.

3. **What are the different methods of controlling this converter and its implementation?**

   Various control methods based on PQ theory, CPT based control, and current control were introduced. Due to it's simplicity and the fact that the current compensation is essential to ensure reliable sinusoidal current supply to the loads, current control is chosen. The implementation of the control based on double-synchronous reference frame for the individual control of positive, negative and zero-sequence components of the currents was demonstrated.

6.1. Discussion

Considering the above-done research, a few relevant points of discussion were found in thesis and are listed below.

1. The literature review was key to identifying suitable toplogies of the converter to be used in a Power Redistributor application. The use of a simple 2-level converter helps in maintaining modularity and simplicity of the converter. The use of an additional fourth leg, as presented in the 4L-SC configuration, makes the system flexible.

2. The use of a current-controlled strategy helps compensate the grid-currents rather than the three-phase power in the system. This helps in controlling the THD of the currents which flow to sensitive loads, thus, improving performance of equipment. Based on the observed harmonics in the system, specific harmonic compensation can be achieved by adding resonant controllers tuned to the particular frequency to eliminate said harmonic.

3. The mathematical model of the converter derived in Chapter 3 helps in sizing of converter components accurately. For the DC-link, previous literature has only focused on contribution of negative-sequence component to the DC-link ripple. In this thesis, an expression involving both negative and zero-sequence components of the converter is derived, and validated by simulations. This can help in accurate sizing of the DC-link.

4. The control strategy used in this thesis was based on the Double Synchronous reference frame. Considering the main purpose of this converter is to compensate unbalance, this is important, considering the positive, negative and zero-sequence components can be compensated and controlled individually in their respective reference frames. This helps in accurate and modular control of all of these components as necessary.

5. The different configurations of the converter i.e. 3L, 4L-SC and 4L were compared under various parameters. Each converter has their own strengths and weaknesses and it is important to identify the application and power level of use of these converters before their implementation.

6.2. Future Scope of Work

This thesis provided a comprehensive introduction to the phase-unbalance and the design of a power redistributor device. However, the design presented here is fundamental and a lot of improvements can be made. Some of the recommendations of future work based on this work are presented below.

1. The current work has only involved simulation of this converter. A hardware implementation can help verify actual problems related to the grid, and the operation of the converter can be verified in a realistic environment. A converter for this purpose has already been designed and is shown in Fig. 6.1.

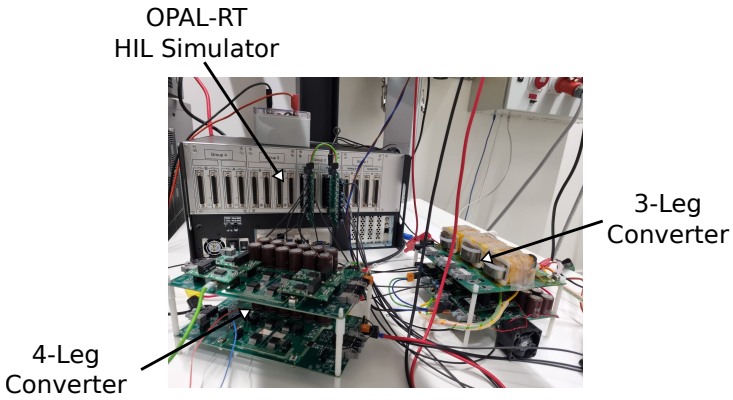


Figure 6.1: Hardware Setup showing both three-leg and four-leg configurations

2. The design parameters of the converter based on magnitude of power unbalance could be an interesting problem to solve.

3. The control of the converter was based on a current-control scheme. However, various other control schemes based on CPT and Power balance were not considered, and these could be explored, to allow for more flexible and accurate control of the power.

4. The modulation of the converter chosen was simple SPWM. However, various other modulation techniques can be tested, and their use in unbalance systems could be explored. This could help improve the efficiency of a converter operating in an unbalanced system.

5. The traditional 4L-SC configuration normally cannot have the improved DC-link utilisation possible in the 4L configuration by injecting a third-harmonic zero-vector. However, Liang *et al.* presents a method of improving the DC-link capacity, but however, the neutral-leg decoupling advantage is lost [32]. This could be an interesting method of improving the DC-link utilisation of a 4L-SC configuration converter.

6. In the 4L configuration, the presence of a full DC-link presents an opportunity to redirect the negative-sequence ripple of DC-link current into one of the legs of the converter or onto a 5^{th} leg. This is called active power decoupling and Zhou *et al.* have presented a detailed method of implementation of this strategy in [40]. This could help eliminate all the low-frequency harmonics in the DC-link.

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