High-Performance Phase-Locked Loops for Quantum Computing Applications

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High-Performance Phase-Locked Loops for Quantum Computing Applications

Jiang GONG

High-Performance Phase-Locked Loops for Quantum Computing Applications

Dissertation

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To my lovely grandparents

"A journey of a thousand miles begins with a single step."

Lao Tzu

Contents

Chapter

1

Introduction

This is an introductory chapter of the thesis. The main goal of this chapter is to justify the need of cryogenic CMOS (cryo-CMOS) circuits and systems, particularly a cryo-CMOS phase-locked loop (PLL), for quantum computing applications. In Section 1.1, we first elaborate on the conventional applications and general design challenges of frequency synthesizers and declare that the main application of developed PLLs is quantum computing. In Section 1.2, we introduce the necessary background information on quantum computing and justify the need for a cryo-CMOS PLL for quantum computing applications. This helps to develop the thesis in the following chapters. In Section 1.3, we discuss state-of-the-art PLL architectures and their strengths and limitations. Moreover, the key objectives, structure, and research contributions of this thesis are concluded in Section 1.4 and Section 1.5.

1.1 Frequency Synthesis: Applications and Challenges

Frequency synthesis has widespread applications by providing clocks for data converters, generating local oscillator (LO) signals for wireless transceivers, and performing frequency and phase modulation. For instance, a low-jitter and low-spur clock is demanded in high-performance data converters to avoid compromising the sampling performance [1, 2]. In addition, in both wireless and wireline transceivers, the limited available bandwidth in communication channels requires efficient modulation schemes, demanding ultra-low-jitter clocks as well [1–3]. Furthermore, in a micro-electromechanical system (MEMS) based oscillator, a high-performance frequency synthesizer is typically required to compensate for frequency deviation in the MEMS resonator due to temperature variation [4]. In particular, a frequency synthesizer is in great demand for emerging applications, such as quantum computing [5].

Both the phase-locked loop (PLL) and the direct digital frequency synthesis (DDS) could be used to generate the high-frequency clock signal. A key advantage of a DDS system is that its output frequency and phase can be rapidly manipulated through a digital processor control. However, the high-resolution digital-to-analog converter (DAC) and low-pass filter following the digital processor are expensive to build and consume excessive power at high frequencies. Hence, the DDS solution is not acceptable and practical for major radio-frequency (RF) applications. A dominant method of implementing frequency synthesis is by a PLL [6]. A PLL compares the output phase of an oscillator with the phase of a stable external reference signal. As the oscillator's frequency drifts, the PLL generates a control signal to the oscillator and corrects the oscillator's frequency in a negative feedback manner. Compared with a DDS, a PLL is much cheaper to build and consumes less power, at the cost of lower switching speed due to the feedback control.

In macro-cellular base stations and satellite communication systems, an RF sampling analog-to-digital converter (ADC) is typically used to directly digitize received wideband (e.g., in a gigahertz frequency range) signals [7]. Compared to the heterodyne architecture, this approach can significantly reduce the system's complexity and cost while offering more frequency agility. Furthermore, the RF sampling approach enables more digital integration, which is used for a low-power, multi-gigabit serial interface and on-chip digital-

down conversion (DDC). Hence, this leads to a very size- and power-efficient digital interconnect between the data converter and digital processor. However, in an RF ADC, the clock jitter is one of the major concerns, as it changes sampling moments and creates sampling errors. The resulting signal-to-noise ratio (SNR) of an ADC due to jitter could be expressed as [8]

$$\mathrm{SNR} = 20\log_{10}\left(\frac{1}{2\pi f_{\mathrm{sig}}\sigma_{\mathrm{jit}}}\right), \tag{1.1}$$

where $\mathrm{f_{sig}}$ is the input signal frequency and σ_{jit} is the clock's RMS jitter. For a given SNR requirement, the linear dependence of jitter to the input signal frequency in high-speed and high-resolution ADC designs presents difficult challenges. For instance, less than 20-fs jitter is allowed on the sampling clock of a 10-bit 10-GHz ADC. On the other hand, spurs on the sampling clock can shift sampling moments in a deterministic fashion, introducing sampling errors as well. The resulting ADC output exhibits spurious tones and limits the spurious-free dynamic range (SFDR) of the converter to

$$\mathrm{SFDR} = -\mathrm{Spur_{clk}} + 20\log_{10}\left(\frac{\mathrm{f_{clk}}}{\mathrm{f_{sig}}}\right), \tag{1.2}$$

where $\mathrm{Spur_{clk}}$ is the spur of the clock and $\mathrm{f_{clk}}$ is the sampling frequency [9]. This indicates that the clock spurs requirements can be very challenging for high SFDR applications as well. For example, the clock spur must be below -80 dBc for applications requiring 90 dB SFDR.

To improve the mobile experience and develop new technologies (e.g., vehicle-to-everything and machine-type communications), the next-generation communication standard is expected to provide higher data rates, lower latency, and improved link robustness. For example, compared to fourth-generation long-term evolution (4G LTE), the fifth generation (5G) increases peak data rates to 10 Gb/s, and connection density to 1 million devices/km^2, while reducing the latency to one-tenth [3]. To achieve such a superior wireless link, complex modulation schemes are typically required. For instance, 256 quadrature amplitude modulation (QAM) is used in 5G radios operating at around 30 GHz, leading to a tolerable EVM of -36 dBc due to LO's jitter [10].

The resulting PLL's jitter requirement can be derived by [11]:

$$\sigma_{\text{jit}} = \frac{\sqrt{10^{\text{EVM}/10}}}{2\pi \text{f}_{\text{clk}}}. \tag{1.3}$$

Thus, less than 84-fs of jitter is allowed for the PLL if the EVM is dominated by the PLL. In practice, the required jitter is much more stringent when other error sources are considered. Moreover, based on Eq. (1.3), the required RMS jitter becomes much lower at higher frequency bands. For instance, the PLL should deliver less than 50-fs jitter at the 47-GHz band.

Due to the increasing demand in high-performance computing, networking, communications, and most recently from machine learning (ML), deep learning (DL), and artificial intelligence (AI), wireline data links have reached a tremendous data rate of 224 Gb/s by using the Pulse Amplitude Modulation 4-level (PAM4) signaling [12, 13]. On the transmit (TX) side, the random and deterministic jitters generated by the PLL directly corrupt the transmitted data. Notice that the symbol period is as low as 10 ps in a 224 Gb/s PAM4 wireline TX. To minimize the horizontal eye closure at the TX output, the TX PLL should introduce a jitter of less than 100 fs. On the receive (RX) path, almost all of the high-speed PAM4 RX front end adopts the ADC-based architecture for digital equalization. A 6-bit or 7-bit ADC is typically used in the RX [14–16]. This translates to a jitter requirement of below 20 fs.

Apart from the stringent jitter and spur requirements, for multi-standard devices such as wireless and wireline transceivers, a PLL with an octave frequency-tuning range (FTR) is desired such that a single-core synthesizer can support multi-band operation [17–28]. This tends to degrade the PLL's jitter performance due to higher phase noise in a wide FTR oscillator. Moreover, low power consumption is necessary to increase the battery life of portal devices.

In conclusion, high-performance PLLs are widely used in many applications. The goal of this thesis is to address the clock generation problems and propose integer-N PLL architectures that reliably achieve low jitter with a low power consumption over a wide temperature range. Moreover, low-noise and wide FTR oscillators are investigated as well. The techniques we proposed in this thesis are general and essential for room-temperature applications. Nevertheless, in this thesis, the developed PLLs and oscillators mainly target quantum computing applications. Before diving into the detailed PLL specifications

and design considerations, the necessary background information for quantum computing will be first introduced in the next section.

1.2 Cryo-CMOS PLL for Quantum Computing

Quantum computers hold the promise to solve particular problems that are intractable even for today's most powerful supercomputers [29–31]. For example, quantum computers can efficiently simulate highly-entangled quantum systems [31–33]. This could potentially help to accelerate the design of new catalysts that improve the efficiency of nitrogen fixation or carbon capture into fertilizers, room-temperature superconductors that lead to more effective power transmission, or improved collection of solar energy [31]. In addition, quantum computers could also solve classical problems faster, such as searching in large datasets using Grover's algorithm [34] and factorizing large integers into prime numbers using Shor's algorithm [35]. Consequently, the capability of solving currently intractable problems and significantly accelerating certain computations of quantum computers are believed to represent a game changer that has the potential to revolutionize entire industries. Hence, since the initial proposal by Richard Feynman, quantum computers have gained widespread interest in both academia and industry over the last few decades.

To reach such remarkable goals, a quantum computer operates by processing the information stored in quantum bits (qubits). In this thesis, solid-state qubit topologies such as spin qubits and transmons are considered, as they promise scalability due to their small form factor and fabrication process [36,37]. A qubit is a two-level quantum mechanical system whose instantaneous state can be described as a superposition of its two basis states (denoted as $|0\rangle$ and $|1\rangle$). A single-qubit state thus can be mathematically expressed as:

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,, \tag{1.4}$$

where α and β are complex coefficients and should satisfy $|\alpha|^2+|\beta|^2 = 1$. As depicted in Fig. 1.1, any single-qubit state $|\psi\rangle$ can be pictorially presented by a three-dimensional unit vector on the Bloch sphere.

Apart from the superposition, another distinct property of qubits (compared to classical bits) is entanglement or the inseparability of the state of two or more qubits [32]. Classical bits are typically isolated from each other

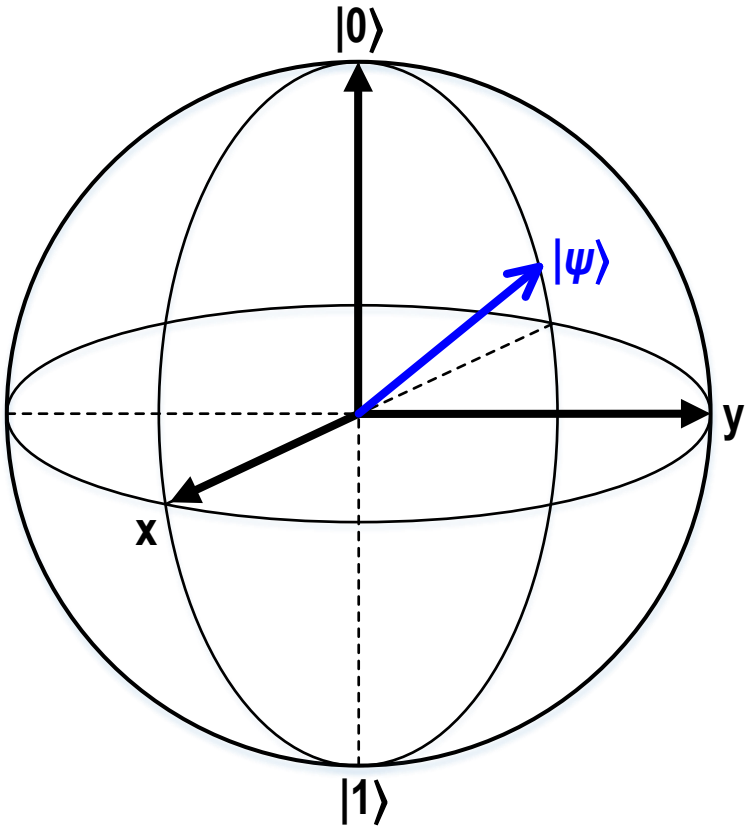

Figure 1.1: Bloch sphere representation of a single-qubit state.

as crosstalk could adversely affect the performance of one bit due to unwanted noise coupling from the other bits. However, when many qubits are coupled or entangled, their behaviors are correlated i.e., any change in the state of one qubit affects the state of other qubits in a well-controlled fashion.

In a similar fashion to running classic algorithms, which requires operations on classic bits, the execution of quantum algorithms involves operations on qubits. This is typically accomplished by acquiring/applying high-frequency, high-accuracy, and low-noise signals from/to the qubit electrodes [29]. Performing a logic operation on a single qubit is equivalent to performing a rotation of the block vector in the Bloch sphere [38]. The accuracy of such a rotation is typically characterized by the fidelity (F), which is limited by both the qubit itself and the applied control signals [39]. Due to the qubit's implementation non-idealities, a state-of-the-art fidelity is reported to be around 99.9%, which is too low to be useful in practical quantum computing applications [39]. Therefore, by encoding the state of a single logical qubit in many physical qubits, quantum-error correction schemes have been developed so as to detect and correct the errors of the logic qubit [40]. The resulting

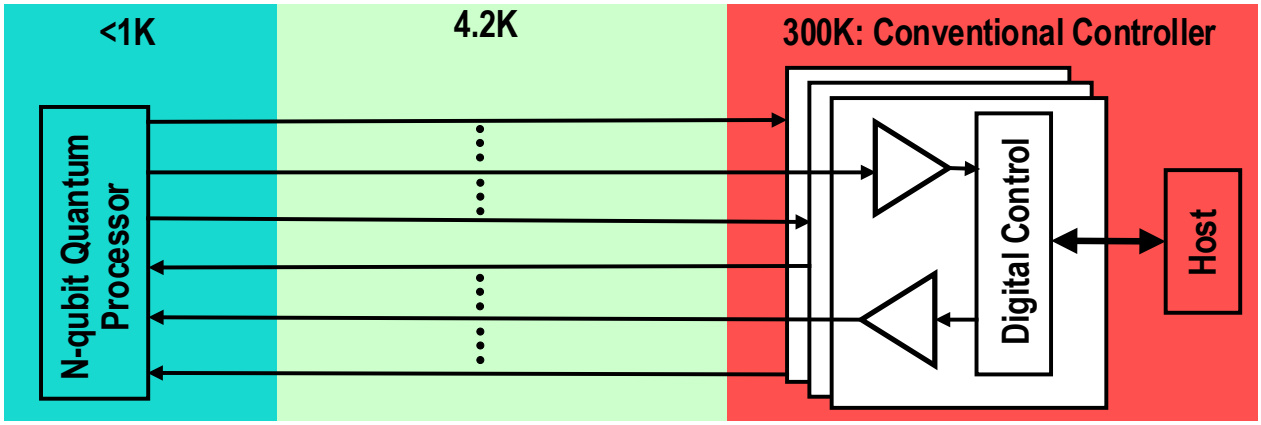

Figure 1.2: Simplified block diagram of a room-temperature instrument-based controller.

fidelity of a single logical qubit after the error correction can be high enough for practical quantum computing applications.

Nevertheless, more than 100 logical qubits would be required for the simplest nontrivial problem (e.g., quantum chemistry) [41]. More than 1000 physical qubits are required to implement a single logical qubit with a sufficiently low error rate by using the best-known qubits and algorithms to date [40]. This requirement translates into the need for thousands or millions of physical qubits, which advocates scalability for the qubit-control system.

However, as shown in Fig. 1.2, current spin qubits and transmons operate at temperatures well below 1 K inside a dilution refrigerator, while the readout/control electronics are typically implemented with commercial instruments operating at room temperature (RT), which are hardwired from/to qubits. Although this brute-force approach proves to be successful in few-qubits (<100) systems, it creates scalability and performance issues due to the impractical cabling, thermal loading, and large form factor as the qubit number grows. Hence, this approach is not practical for a large-scale quantum computer that requires millions of qubits to run a quantum algorithm.

To overcome the cabling bottleneck, as depicted in Fig. 1.3, a fully-integrated cryogenic CMOS (cryo-CMOS) control system is proposed to operate close to the qubits at 1-4.2 K [5]. This intermediate approach could support up to 1000 qubits due to the relatively high cooling power of the refrigerator at 1-4.2 K (i.e., a power consumption of ∼1 mW per qubit for the qubit controller), and hence dramatically reduces the required complex interconnections between the cryogenic refrigerator and the room temperature electronics. Eventually, the cryo-CMOS controller could be co-integrated with advanced “hot” qubits

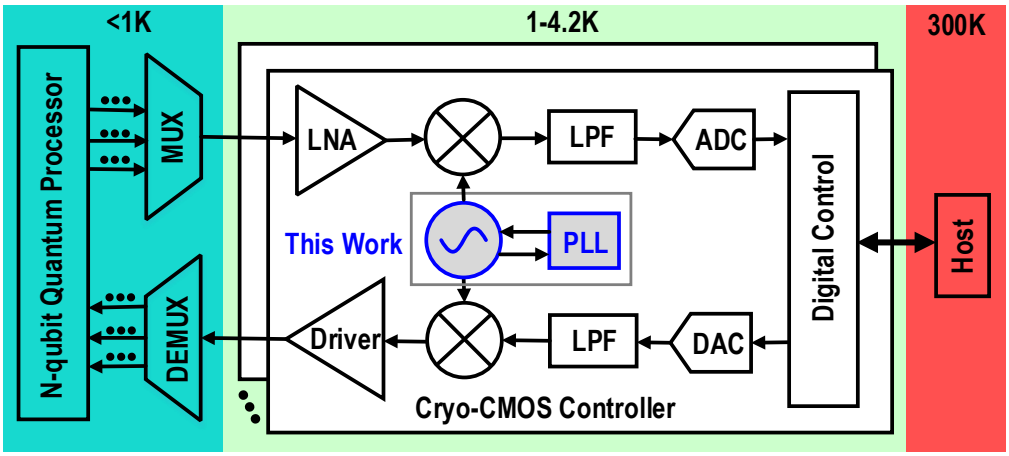

Figure 1.3: Simplified block diagram of a cryo-CMOS controller interfacing a quantum processor [5].

operating at ∼1 K [42] on the same die or package, thus eliminating the wiring issue and offering a compact solution towards the realization of large-scale quantum computers. To this end, developing building blocks for quantum computing applications at cryogenic temperatures (i.e., 1-4.2 K) has been an active field of research over the last few years [43–69].

Although a cryo-CMOS receiver for the gate-based RF readout of spin qubits [61], and cryo-CMOS burst generators for the control of superconducting and spin qubits [62,63,70] are presented, they rely on an off-chip local oscillator (LO) operating at room temperature to down/up-convert the desired signals. This requires a complex, high-frequency, and high-power LO distribution network (∼7 mW in [63]), thus limiting the system form factor and worsening the LO leakage at the controller output. Consequently, as shown in Fig. 1.3, it is beneficial to generate the LO at cryogenic temperatures (CT) as well. And recent cryo-CMOS qubit controllers typically integrate several on-chip PLLs [64, 66, 71, 72]. In [64, 66], two cryo-CMOS digital PLLs were used to generate LO for the controller of superconducting qubits. In [67], an analog charge-pump PLL was integrated into a cryo-CMOS receiver for scalable multiplexed readout of silicon-based semiconductor spin qubits/quantum dots. However, those designs consume high power (i.e., 12.5 mW in [64, 66] and 35 mW in [67]). Besides, they exhibit poor in-band phase noise at cryogenic temperatures and might not meet the stringent specifications required for quantum computing applications.

Apart from the fully-integrated PLLs, the performance of standalone voltage-controlled oscillators (VCOs) is reported at 4.2 K as well [48–51, 65,

73]. In [48], a cryo-CMOS class $F_{2,3}$ LC-tank VCO was first reported with extensive characterization. In [65], a cryogenic SiGe BiCMOS hybrid Class B/C mode-switching VCO was presented to reduce the phase noise in the flicker region. However, there is still a lack of systematic study of LO design for quantum computing applications. Notice that the cryo-CMOS controller presented in Fig. 1.3 shows close similarities with conventional RF wireless transceivers. As discussed in Section 1.1, the PLL performance for wireless applications is typically determined by the error vector magnitude (EVM). To determine the PLL requirements, this dissertation derives PLL specifications for quantum computing applications. It will be shown soon that the required PLL specifications (e.g., phase noise, integrated jitter, reference spur, and power consumption) are stringent for quantum computing applications. Based on the PLL specifications, this dissertation complements the prior art by proposing appropriate PLL architectures for quantum computing applications. In the next section, state-of-the-art PLL architectures will be reviewed. This includes a brief discussion of charge-pump PLL, digital PLL, injection-locked oscillator, sub-sampling PLL, and sampling PLL.

1.3 Review of the Prior Art PLLs

An analog charge-pump PLL (CPPLL) is most widely used to synthesize high-purity clock signals due to its simplicity and robustness [74]. Fig. 1.4 (a) shows the simplified block diagram of a CPPLL. Recently, a CPPLL achieved an excellent RMS jitter of 54 fs [17]. Yet, a high-frequency reference clock of 500 MHz was used to suppress the in-band phase noise of the PLL building's blocks. The generation of 500-MHz frequency from a low-frequency reference < 100 MHz is nontrivial.[1] Besides, the power consumption was relatively high (45 mW) in order to reduce the noise of the charge pump and phase frequency detector. It is worth mentioning that an analog CPPLL suffers from other design issues as well. On the one hand, the area of the loop filter might be impractically large, especially when a narrow loop bandwidth is required (e.g., a few kHz). In addition, the charge-pump current mismatch causes a voltage

[1] In the final cryo-CMOS controller, the common reference signal would be derived from an off-chip quartz crystal resonator operating at 4.2 K. An on-chip sustaining amplifier will be used to compensate for the resonator loss for the stable oscillation. A crystal resonator with a frequency higher than 100 MHz might not be commercially available.

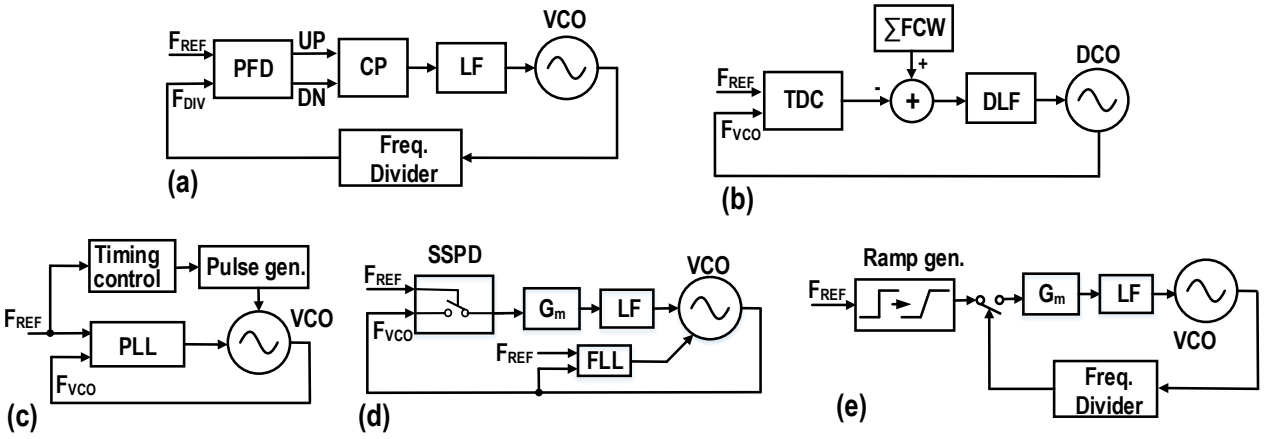

Figure 1.4: Simplified block diagram of the (a) CPPLL, (b) DPLL, (c) ILO, (d) SSPLL, and (e) SPLL.

ripple on the VCO tuning voltage, degrading spur performance.

To solve the above-mentioned issues, a digital PLL (DPLL) eliminates the charge pump and phase frequency detector and hence their noise [see Fig. 1.4 (b)]. And its loop filter being digital scales down with new process nodes [75]. However, the quantization noise of a time-to-digital converter (TDC) and a digitally controlled oscillator (DCO) typically limits the DPLL's jitter performance. Recently, DPLLs using the stochastic flash TDC [76] and bang-bang phase detector [77] achieved a jitter value of 50 fs, closing the performance gap between analog PLLs. However, an impractically high-frequency reference clock (∼500 MHz) was still used to reduce the impact of quantization noise on the jitter. In addition, the power consumption was still quite high (i.e., 56 mW in [76] and 19.8 mW in [77]).

An injection-locked oscillator (ILO) can achieve excellent jitter performance with low power by periodically replacing the noisy edge with a clean edge of the reference [78–83]. Fig. 1.4 (c) shows the simplified block diagram of an ILO. The power consumption of this architecture can be very low due to the elimination of both PLL's loop components and feedback divider. In [84], the presented ILO achieved a jitter value of 70 fs while consuming merely 0.2 mW power. However, the jitter performance of an ILO is very sensitive to process-voltage-temperature (PVT) variations. To address this problem, recent ILOs are typically equipped with dedicated on-chip background calibration circuits (e.g., an auxiliary PLL), complicating the design. Moreover, due to the direct reference injection, an ILO typically suffers from large reference spurs (i.e., >-60 dBc) [78–83, 85] even for lower-GHz carriers. The spur level becomes

higher than -50 dBc when synthesizing a carrier higher than 8 GHz [86, 87]

Sub-sampling PLLs (SSPLLs) are promising solutions to reliably synthesize low-jitter clocks [88–96]. As shown in Fig. 1.4 (d), SSPLLs obviate the need for a feedback frequency divider as well. The jitter and power associated with it are thus eliminated. Moreover, by directly sampling the fast edges produced by the voltage-controlled oscillator (VCO), this method achieves a high phase-detection gain and hence a low contribution of the phase detector and loop components to the total phase noise. Due to these reasons, the SSPLL presented in [97] achieves 54 fs jitter while consuming only 6.5 mW. However, an SSPLL has its limitations as well. One of the drawbacks is that the monotonic input range of a sub-sampling phase detector is only $\pm 0.5\pi$ VCO phase. This can potentially cause an SSPLL to lose lock if there is some sudden interference on the power supply and ground of the VCO and reference path. Hence, a frequency-tracking loop is typically required in the background, consuming a considerable amount of power [97].

A sampling PLL (SPLL) can be used to solve the SSPLL's limited input range problem [98, 99]. In an SPLL, either the reference clock or the feedback clock is used to generate a ramping voltage through a ramp generator [98–103], which is then sampled at a rate of the reference frequency. Depending on the slew rate of the voltage ramp, the monotonic range of an SPLL can be enlarged to $\pm 0.5 T_{REF}$, where T_{REF} is the reference period. However, the increase in the detection range sacrifices the phase-detection gain, resulting in high in-band phase noise. For example, in [98], while the SPLL demonstrated robust locking performance, the achieved jitter was above 110 fs due to reduced phase-detection gain ($\sim$0.02 V/rad). On the other hand, in [103], the phase-detection gain was improved to $\sim$40 V/rad by increasing the slope of the ramp voltage. The resulting SPLL achieved 20 fs jitter, at the cost of the reduced linear range. In addition, due to the VCO's narrow frequency tuning range, only a single frequency can be covered in [103]. Moreover, the SPLL might not generate target frequency over process variations.

1.4 Thesis Objective and Outline

As mentioned in Section 1.1, the major goal of this thesis is to propose integer-N PLL architectures that reliably achieve low jitter with a low power

consumption over a wide temperature range. Moreover, low-noise and wide frequency-tuning-range VCOs are investigated as well. The techniques developed in this thesis are general and can be used for a wide range of applications. Nevertheless, the developed PLLs and VCOs mainly target emerging quantum computing applications.

At the beginning of this Ph.D. work, it is not clear what are the specifications of PLLs as the quantum computing application is a relatively new field. In Chapter 2, the VCO and PLL specifications are firstly derived based on the control fidelity for a single-qubit operation. The specifications obtained in this chapter are used as the guideline for designing VCOs and PLLs in the following chapters. Notice that PLLs and VCOs for quantum computing applications need to operate at ambient temperatures as low as 4.2 K. However, there is a lack of both active and passive device models at those temperatures. Chapter 3 briefly summarizes both active and passive device behaviors at cryogenic temperatures based on the literature. A simplified device model based on Veriloga is introduced to predict the PLL performance at cryogenic temperatures.

At the beginning of this Ph.D. work, it was found that an *LC* VCO shows a surprisingly high flicker phase noise corner at 4.2 K when compared to 300 K. It is thus interesting to understand the phase noise mechanism of an *LC* VCO and solve the high flicker phase noise corner issue by circuit techniques at 4.2 K. To this end, Chapter 4 introduces a low-noise cryo-CMOS *LC* oscillator in a 40-nm bulk CMOS process. A digital calibration loop is presented to automatically adjust the configuration of the differential-mode and common-mode capacitor banks of an oscillator to ensure that the oscillator always operates near its optimum performance at 4.2 K. To reveal the substantial gap between the theoretical predictions and measurement results at cryogenic temperatures, a new phase noise expression for RF oscillators is derived by considering the shot-noise effect. The proposed cryo-CMOS *LC* oscillator meets the stringent specifications required by a qubit controller.

While the oscillator in Chapter 4 shows good phase noise at 4.2 K, it cannot be directly used for a cryo-CMOS controller due to its frequency drift over time. A PLL should be used to lock the oscillator phase to an external stable reference for long-term stability. Moreover, the phase noise of an oscillator is high-pass shaped by a PLL. Hence, a wide bandwidth PLL can be used

to solve the flicker phase noise corner issue. Yet, the in-band phase noise due to PLL's loop components must be minimized. In Chapter 5, a wide bandwidth charge-domain sub-sampling PLL is introduced in a 40-nm bulk CMOS process. The main idea is to exploit the windowed-current-integration mechanism in the PLL's phase-detection circuit. This allows for achieving a high phase-detection gain for the PLL while simultaneously minimizing the duty cycle of the reference clock and transistor dimension of the phase detector. As a result, the proposed PLL simultaneously delivers low in-band phase noise, low RMS jitter, and low reference spur while consuming low power. Furthermore, a low-power frequency-tracking loop without using RF dividers is also introduced to lock the PLL robustly when the VCO faces a sudden frequency disturbance. This PLL can be used for various applications such as high-speed data converters, wireline transceivers, and so on. Moreover, the PLL is also fully functional at 4.2 K and hence can be used for quantum computing applications.

Although the PLL presented in the previous chapter shows good phase noise performance over a wide temperature range, its minimum achievable spur performance is limited due to the phase detector's intrinsic nonideality. In Chapter 6, by considering the benefits and challenges of cryogenic operation, a dedicated analog PLL structure is employed so as to maintain high performance from 300 K to 4.2 K. This PLL is optimized for quantum computing applications. It incorporates a new charge-sampling phase detector based on the operation of a dynamic amplifier, which achieves low reference spur thanks to its minimized periodic disturbances on the VCO control. In addition, the phase-detection gain is very high and hence the PLL achieves very low in-band phase noise. The measured phase noise at 4.2 K is analyzed in depth. The proposed cryo-CMOS PLL meets the performance requirements for the qubit control.

While the oscillators and PLLs presented in previous chapters show low phase noise at 4.2 K, they exhibit a narrow frequency tuning range and have limited applications. Chapter 7 introduces an octave-frequency-tuning and low-jitter PLL operating at 4.2 K in a 22-nm FinFET CMOS process. The PLL features a dynamic-amplifier-based phase detector for low-jitter performance. The tuning range of the PLL is enhanced by a compact dual-core triple-mode VCO. Due to its wide frequency-tuning range, this PLL can be used to address

both spin qubits and transmons.

Finally, Chapter 8 concludes this dissertation and presents several suggestions for future developments.

1.5 Original Contributions

The original contributions to the body of knowledge of the Solid-State Circuits community and the quantum computing community are listed as follows:

- Deriving the PLL specifications based on the control fidelity for a single-qubit operation for quantum computing applications [chapter 2];
- Introducing a common-mode resonance calibration technique to automatically optimize the phase noise of an LC oscillator [chapter 4];
- Proposing a low-jitter and low-spur PLL: charge-sampling PLL (CSPLL) [chapter 5];
- Comprehensive phase noise, reference spur, and stability analysis of the CSPLL [chapter 5]
- Introducing the first cryo-CMOS PLL operating at 4.2 K [chapter 6];
- Maintaining PLL performance over a large temperature range from 4.2 K to 300 K [chapter 6];
- Introducing a compact and low-jitter octave-frequency-tuning PLL [chapter 7];

Chapter

2

PLL Specifications for Quantum Computing Applications

In Chapter 1, we have shown that it is beneficial to place a phase-locked loop (PLL) at cryogenic temperatures operating in close vicinity to the qubits for a scalable quantum computer. As the performance of quantum processors improves, non-idealities in the PLL can become the performance bottleneck for the whole quantum computer. To prevent such a limitation, this chapter presents a systematic study of the impact of the PLL's non-ideal effects on qubit fidelity[1]. In Section 2.1, the basic knowledge of qubit states manipulation is presented. Section 2.2 quantifies how much fidelity would degrade due to the phase noise of a PLL or an oscillator. The requirements on PLL's spur and frequency inaccuracy for a given fidelity are elaborated in Section 2.3 and Section 2.4, respectively. Section 2.5 discusses the PLL's tuning range requirement for quantum computing applications, and Section 2.6 concludes this chapter.

[1]This chapter is extracted from the author's previous publications [69, 104].

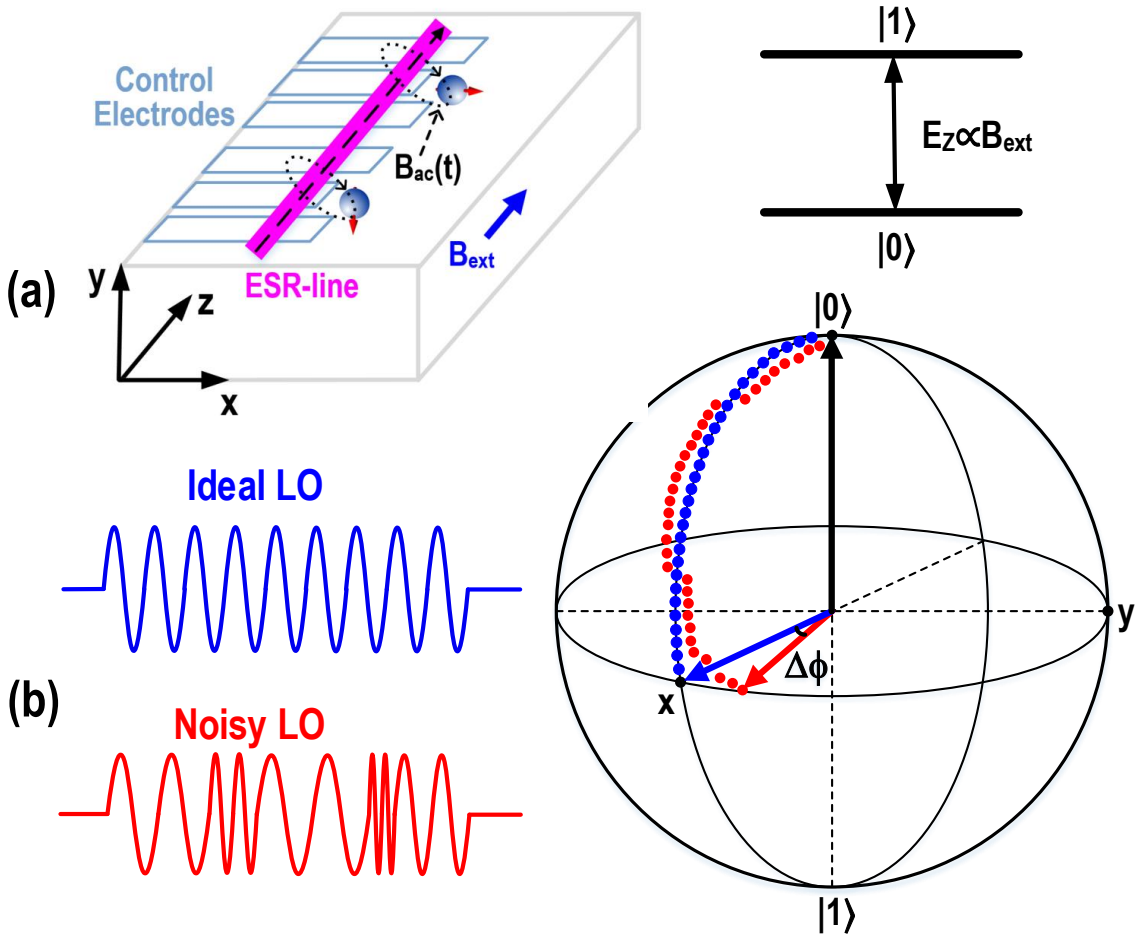

Figure 2.1: (a) A generic sketch of a spin qubit quantum processor comprising qubits encoded in the spin of electrons trapped in quantum dots and (b) an illustration of LO's frequency noise effect on the qubit control.

2.1 Manipulation of Qubit States

A quantum computer operates by processing the information stored in qubits. A qubit is a two-level quantum mechanical system whose instantaneous state can be described as a superposition of its two basis states (denoted as $|0\rangle$ and $|1\rangle$). Any single-qubit state $|\psi\rangle$ can be pictorially presented by a three-dimensional unit vector on the Bloch sphere. The temporal evolution of the qubit state can be described by a unitary propagator U(t), which transforms an initial state $|\psi(0)\rangle$ to a desired state $|\psi(t)\rangle = \mathrm{U(t)}\,|\psi(0)\rangle$. The state evolution corresponds to a vector rotation on the Bloch sphere and the propagator satisfies the Schrodinger equation:

$$i\frac{\mathrm{dU(t)}}{\mathrm{dt}} = \mathrm{H(t)U(t)}, \tag{2.1}$$

where H(t) is the Hamiltonian operator.

Fig. 2.1 (a) shows a generic sketch of a spin-qubit quantum processor comprising qubits encoded in the spin of electrons trapped in quantum dots. Under a strong external static magnetic field (B_{ext}), an energy difference (E_Z) proportional to B_{ext} between electrons with spin up and down is induced.

Suppose that only the B_{ext} is applied. The Hamiltonian in the lab frame is a constant [38]: $H(t) = -\omega_0\sigma_z/2 = -\gamma_e|B_{ext}|\sigma_z/2$, where ω_0 is the qubit resonant frequency (i.e., Larmor frequency), σ_z is the z-component of Pauli spin operators[1], and γ_e is the gyromagnetic ratio of electron ($\sim$28 GHz/T in silicon). ω_0 is around 10-20 GHz for spin qubits and 4-8 GHz for transmons [36, 37]. (2.1) could be solved as $U(t) = \exp(i\omega_0\sigma_z t/2)$, indicating that the spin rotates around the z-axis in the Block sphere at a rate of ω_0 with the application of B_{ext}. However, such a rotation is very fast and is limited to the z-axis only.

To rotate around all of the axes with a manageable speed, $|\psi\rangle$ are typically manipulated through the local application of a weak oscillating magnetic field [$B_{ac}(t)$] oriented perpendicularly to B_{ext}, produced by an on-chip electron spin resonance (ESR) line. Suppose that $B_{ac}(t)$ equals $(2/\gamma_e)\omega_R\cos(\omega_{LO}(t)t + \phi)$, where ω_R ($= 2\pi f_R$) is the qubit operation speed and $\omega_{LO}(t)$ is the LO's instantaneous frequency [105]. The resulting Hamiltonian in the lab frame has the following form:

$$H(t) = -\omega_0\frac{\sigma_z}{2} + \omega_R\cos(\omega_{LO}t + \phi)\frac{\sigma_x}{2}, \tag{2.2}$$

which is explicitly time-dependent and eludes itself from an analytical solution. However, it is possible to transform this Hamiltonian into a rotating frame with a frequency of ω_{LO} around the z-axis [38, 39, 105, 106]. The resulting Hamiltonian in the rotating frame at frequency $\omega_0$can be estimated by [105]:

$$H_{rot}(t) \approx (\omega_{LO} - \omega_0)\frac{\sigma_z}{2} + \omega_R(\cos(\phi)\frac{\sigma_x}{2} - \sin(\phi)\frac{\sigma_y}{2}), \tag{2.3}$$

which is time-independent. Thus, (2.1) can be solved to find the control propagator in the rotating frame:

$$U_{rot}(t) = \exp(-iH_{rot}t). \tag{2.4}$$

[1]The Pauli spin operators are expressed by three complex matrices (σ_x, σ_y, and σ_z) and are given by: $\sigma_x = \begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}, \sigma_y = \begin{bmatrix}0 & -i\\ i & 0\end{bmatrix}, \sigma_z = \begin{bmatrix}1 & 0\\ 0 & -1\end{bmatrix}$.

If ω_{LO} is precisely set to ω_0, the z-component of the Hamiltonian in (2.4) is eliminated, and the spin rotates around the x/y axis under the application of $B_{ac}(t)$ [see blue plots in Fig. 2.1 (b)]. The magnitude of $B_{ac}(t)$ determines the rotation speed (ω_R), which is typically above 100 kHz. A higher ω_R is desired because qubit operations are faster and qubits are less sensitive to dephasing-induced errors, leading to a higher intrinsic qubit fidelity. The rotation axis (x/y) can be controlled by updating the phase ϕ of $B_{ac}(t)$ [i.e., 0° or 90°]. Both the amplitude and duration (τ) of $B_{ac}(t)$ can be exploited to control the rotation angle (i.e., $\theta = \omega_R \tau$). However, if there is an instantaneous frequency mismatch between ω_{LO} and ω_0 due to LO's frequency noise (FN), the z-component of the Hamiltonian in (2.4) is not zero. Consequently, apart from undergoing the desired rotation around the x/y axis, the spin also suffers from an undesired rotation around the z-axis, thus introducing control errors [see red plots in Fig. 2.1 (b)].

2.2 Fidelity due to LO's Phase Noise

To quantify the accuracy of a single-qubit operation introduced by the non-idealities of $B_{ac}(t)$, the gate fidelity F is typically used as the metric that characterizes the agreement between the intended rotation [$U_{ideal}(\tau)$] and the real rotation [$U_{real}(\tau)$] over a time interval (0, τ) [107]:

$$F = \frac{1}{4} \cdot |Tr[U_{ideal}{}^{\dagger}(\tau) \cdot U_{real}(\tau)]|^2, \tag{2.5}$$

where "Tr" and "†" represent the trace and conjugate transpose of a matrix, respectively. Due to LO's frequency noise FN [$\Delta\omega(t)$], (2.3) could be rewritten as the sum of a noisy and noise-free Hamiltonian [$H_{noise}(t)$ and $H_{ideal}(t)$]:

$$\begin{aligned} H_{real}(t) &= \Delta\omega(t)\frac{\sigma_z}{2} + \omega_R(\cos(\phi)\frac{\sigma_x}{2} - \sin(\phi)\frac{\sigma_y}{2}) \\ &= H_{noise}(t) + H_{ideal}(t). \end{aligned} \tag{2.6}$$

Since $\Delta\omega(t)$ is random and time-dependent, it is not possible to derive a closed-form expression for $U_{real}(\tau)$, as the Hamiltonian will not commute with itself at different times. Nevertheless, in first-order approximation, the expected fidelity due to the general noise $S(\omega)$ of $B_{ac}(t)$ can be calculated in

the frequency domain and estimated by [106]:

$$\mathrm{F} \approx 1 - \frac{1}{2\pi} \sum_{\mathrm{i,j,k=x,y,z}} \int_{-\infty}^{+\infty} \mathrm{S_{ij}}(\omega) \frac{\mathrm{M_{jk}}(\omega) \mathrm{M_{ik}}^{*}(\omega)}{\omega^2} \mathrm{d}\omega. \tag{2.7}$$

$\mathrm{M_{jk}}(\omega)$ represent the elements of the control matrix in the frequency domain and only depend on the noise-free control propagator $[\mathrm{U_{ideal}(t)} = \exp(-i\mathrm{H_{ideal}(t)t})]$ as:

$$\mathrm{M_{ij}}(\omega) = \frac{-i\omega}{2} \int_0^{\tau} \mathrm{Tr}[\mathrm{U_{ideal}^{\dagger}}(\mathrm{t}) \sigma_{\mathrm{i}} \mathrm{U_{ideal}}(\mathrm{t}) \sigma_{\mathrm{j}}] \cdot \mathrm{e}^{i\omega \mathrm{t}} \mathrm{dt}. \tag{2.8}$$

Suppose that only the LO's frequency noise is considered. In (2.7), the index i and j equal z, and the noise expression is

$$\mathrm{S_{zz}}(\omega) = \frac{1}{4} \cdot \mathrm{S_F}(\omega) = \frac{1}{4} \cdot \mathcal{L}_{\phi}(\omega) \cdot \omega^2, \tag{2.9}$$

where $\mathrm{S_F}$ and $\mathcal{L}_{\phi}(\omega)$ are the frequency-domain FN and PN, respectively [105]. Consequently, the fidelity introduced by LO's FN can be expressed as

$$\mathrm{F} = 1 - \frac{1}{2\pi} \int_{-\infty}^{+\infty} \frac{S_{\mathrm{F}}(\omega)}{{\omega_{\mathrm{R}}}^2} \cdot \frac{(\alpha^2+1)[1-\cos(\theta)\cos(\theta\alpha)] - 2\alpha\sin(\theta)\sin(\theta\alpha)}{2(\alpha^2-1)^2} \mathrm{d}\omega, \tag{2.10}$$

where $\alpha = \omega/\omega_{\mathrm{R}}$. By referring the angular frequency to the regular frequency for simplicity, (2.10) can be rewritten as

$$\mathrm{F} = 1 - \int_0^{+\infty} 2 \cdot \frac{\mathcal{L}_{\phi}(f) \cdot f^2}{{f_{\mathrm{R}}}^2} \cdot |\mathrm{H_{LO}}(f)|^2 \mathrm{d}f, \tag{2.11}$$

where $\mathrm{H_{LO}}(f)$ can be interpreted as a qubit filter function. By considering a worst-case rotation angle of π, the squared magnitude of $\mathrm{H_{LO}}(f)$ is

$$|\mathrm{H_{LO}}(f)|^2 = \frac{[1+\cos(\alpha\pi)] \cdot (1+\alpha^2)}{2\left(1-\alpha^2\right)^2}. \tag{2.12}$$

Fig. 2.2 (a) depicts $|\mathrm{H_{LO}}(f)|^2$ versus the frequency offset with various qubit rotation speed. $|\mathrm{H_{LO}}(f)|^2$ shows a first-order low-pass response with a DC gain of 1 and a 3-dB bandwidth of $1.9\mathrm{f_R}$, and exhibits high-frequency notches. This indicates that a qubit has a different sensitivity to LO's phase noise at different frequency offsets and the choice of rotation speed has a substantial

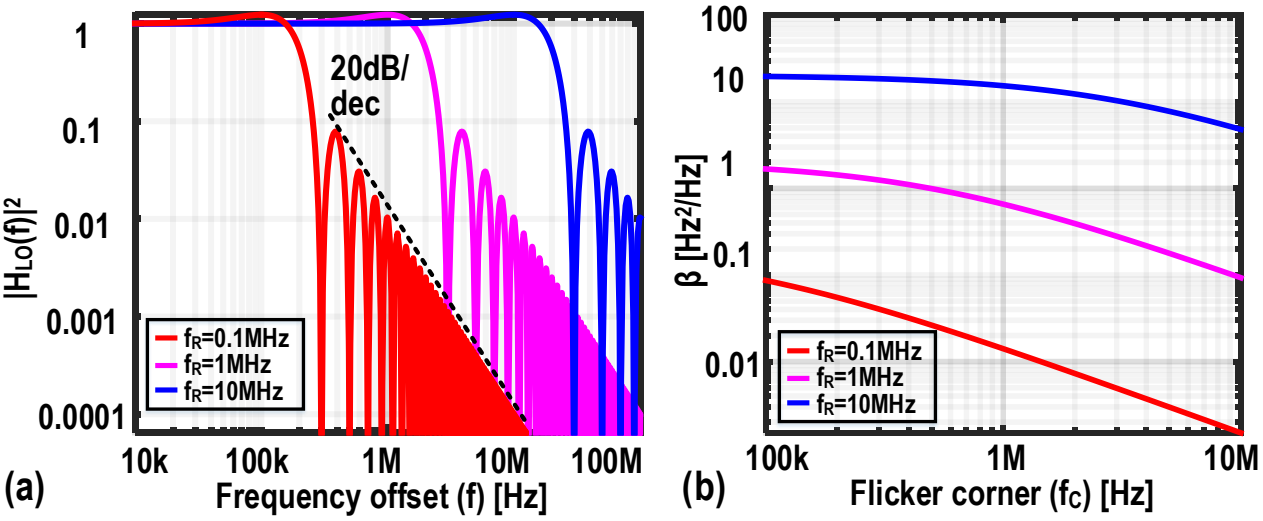

Figure 2.2: (a) $|H_{LO}(f)|^2$ versus the frequency offset and (b) β versus f_C by considering a control fidelity of a 99.999% and various qubit rotation speeds.

impact on the control fidelity.

Equations (2.11) and (2.12) illustrate the LO's phase noise ($\mathcal{L}_\phi(f)$) impact on the system performance (i.e., F). For a given phase noise profile, system engineers could quickly determine the LO's impact on the control fidelity. On the other hand, for circuit designers, it is helpful to get LO specifications based on a given fidelity requirement.

2.2.1 Oscillator's Phase Noise Specifications

For the sake of benchmarking oscillators for quantum computing applications, it is instrumental to derive an oscillator's phase noise specifications. Suppose that the phase noise of an oscillator can be expressed as

$$\mathcal{L}_\phi(\Delta f) = \frac{\beta}{f^2} + \frac{\beta \cdot f_C}{f^3}, \tag{2.13}$$

where β[1] in Hz^2/Hz determines the phase noise in the thermal region and f_C represents the flicker corner. By substituting (2.12) and (2.13) into (2.11), the infidelity for a typical f_R and f_C higher than 0.1 MHz could be solved numerically and may be estimated by

$$\beta \approx \frac{1}{1-F} \cdot \left(\frac{\pi^2}{2f_R} + \frac{16 f_C}{{f_R}^2} \cdot \frac{(1+0.3f_N)^4}{1.6+(1+0.3f_N)^4}\right), \tag{2.14}$$

[1] β has the same unit as the power spectral density of frequency noise.

where f_N is the qubit rotation speed normalized to 1 MHz (i.e., f_N=f_R/1MHz). Notice that a larger f_R is desired as the qubit operation is faster. Nevertheless, a larger f_R necessitates the use of microwave bursts with a larger amplitude and shorter duration for a given rotation angle. When a shorter duration is used, the control noise is only mildly averaged out, and hence the qubit is more sensitive to the high-frequency noise [see Fig. 2.2 (a)]. At first glance, it might conclude that a smaller f_R should be used to relax the oscillator's phase noise requirement. However, a larger amplitude also enhances the power of the microwave bursts to a qubit, leading to a $1/f_R^2$ factor in (2.11). Consequently, although a smaller f_R is beneficial for reducing the noise bandwidth, a higher f_R is desired to relax the required phase noise of an oscillator, as indicated by (2.14).

For fault-tolerant operations, a qubit fidelity larger than 99.9% is typically required. Therefore, the oscillator targets a fidelity of 99.999% to avoid limiting the inherent fidelity of a qubit. By considering those factors, Fig. 2.2 (b) depicts the theoretical β as a function of f_C for a 99.999% fidelity. As expected, a higher f_R relaxes the required PN. In addition, for each f_R, a higher f_C would require a smaller β and hence lower phase noise in the thermal-noise region. For instance, as can be gathered from Fig. 2.2 (b), if f_C is degraded from 1 MHz to 10 MHz for a 1-MHz f_R, the required phase noise in the thermal noise region is >8 dB lower so as to maintain the same fidelity, thus increasing the oscillator's power consumption by >7×. Consequently, an oscillator with a low f_C is crucial to relaxing its power consumption. By considering a state-of-the-art f_R of 1 MHz and an f_C of 3 MHz, the resulting PN at a 10 MHz offset should be below -145.5 dBc/Hz[1].

2.2.2 PLL's Phase Noise Specifications

Having derived the oscillator's phase noise specifications, the PLL's specifications for quantum computing applications will be derived in this subsection. For the sake of simplicity, a type-I PLL is considered here. Suppose that

[1]If this oscillator is placed inside a PLL, the PN specifications of the oscillator are relaxed due to the PLL's filtering effect.

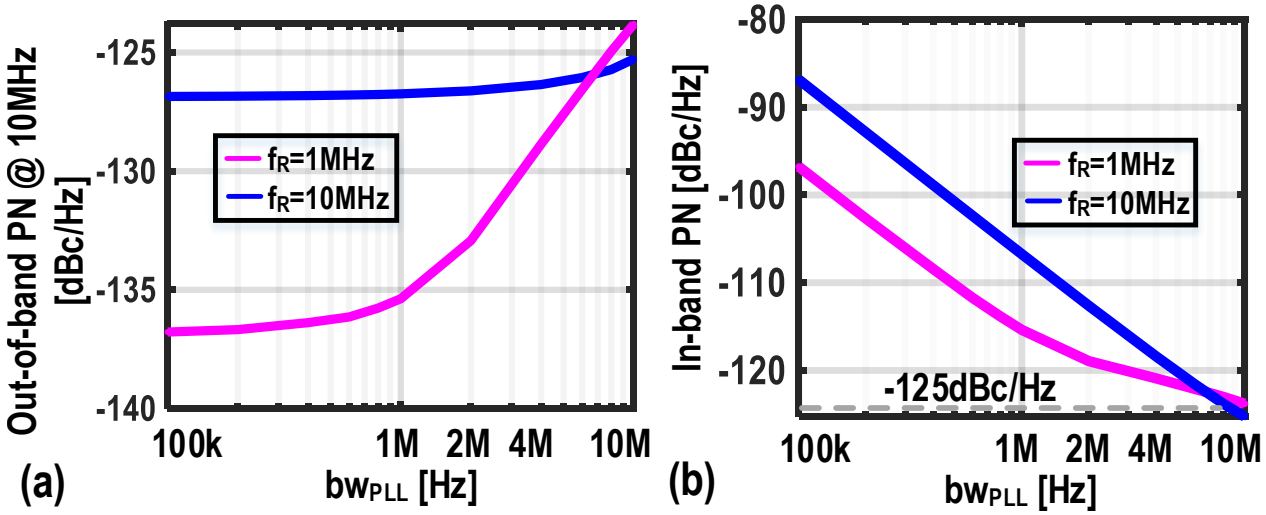

Figure 2.3: Theoretically required (a) out-of-band PN at a 10 MHz offset and (b) in-band PN versus $\mathrm{bw_{PLL}}$ by considering a control fidelity of 99.999% and qubit rotation speed of 1 MHz and 10 MHz.

PLL's phase noise has the following form:

$$\mathcal{L}_\phi(f) = \begin{cases} \beta/\mathrm{bw_{PLL}}^2, & f \leq \mathrm{bw_{PLL}} \\ \beta/f^2, & f \geq \mathrm{bw_{PLL}}, \end{cases} \tag{2.15}$$

where β is a constant coefficient in $\mathrm{Hz^2/Hz}$ and $\mathrm{bw_{PLL}}$ is the PLL bandwidth. (2.15) neglects the flicker noise of the entire PLL[1] and assumes that the in-band PN of the PLL ($\beta/\mathrm{bw_{PLL}^2}$) is flat and the out-of-band phase noise ($\beta/\mathrm{f^2}$) is dominated by the VCO. By substituting (2.12) and (2.15) into (2.11), the infidelity for a typical qubit rotation speed higher than 0.1 MHz could be solved numerically and may be estimated by

$$1 - \mathrm{F} \approx \frac{1.6\pi\beta}{f_\mathrm{R}} \cdot \frac{1}{1 + 0.5(\mathrm{bw_{PLL}}/\mathrm{f_R})^{1.6}}. \tag{2.16}$$

For fault-tolerant operations, a qubit infidelity well below 0.1% is typically required [108]. Therefore, the PLL targets an infidelity of 0.001% to avoid limiting the inherent fidelity of a qubit. The qubit rotation speed is currently ~1 MHz and will be extended to 10 MHz in the future [108]. A higher rotation speed is desired as the qubit gate operation is faster. Based on those considerations, Fig. 2.3 (a) and (b) respectively depict the theoretically

[1]When the flicker noise is included, the accurate infidelity could be obtained by simulation based on (2.11).

required out-of-band phase noise at a 10 MHz offset and in-band phase noise as a function of bw_{PLL} for a 99.999% fidelity. Since the power consumption of a high-performance PLL is typically dominated by the VCO, it is thus beneficial to reduce the VCO's power consumption by increasing the out-of-band phase noise, which could be realized by using a larger bw_{PLL} [see Fig. 2.3 (a)]. However, as depicted in Fig. 2.3 (b), a larger bw_{PLL} would require a more stringent in-band phase noise, demanding lower phase noise contributed by the PLL reference clock buffer and loop components. By considering an f_R of 1 MHz[1] and a reference frequency (F_{REF}) of 100 MHz, a bw_{PLL} of 4 MHz is selected to relax the VCO phase noise requirement. Further increasing bw_{PLL} would degrade the PLL stability and spurious performance, and require a tougher in-band phase noise. The resulting in-band phase noise, phase noise at a 10 MHz offset, and RMS jitter should be below -121 dBc/Hz, -129 dBc/Hz, and 60 fs when synthesizing a 10-GHz carrier.

2.3 Reference Spur Specification

To facilitate scalability and manipulate more qubits, frequency division multiplexing (FDM) could be used, where multiple qubits share a single microwave control line. However, a PLL typically generates spurious tones, which could be at the resonant frequencies of unaddressed qubits. Due to those spurious tones, the states of unaddressed qubits would also experience undesired rotations, degrading the fidelity. The infidelity due to S_{REF} is [108]:

$$1 - F = \frac{\pi^2}{4} \cdot 10^{S_{REF}/10}. \tag{2.17}$$

This translates to a -54-dBc S_{REF} requirement when a 99.999% fidelity is targeted.

2.4 Frequency Inaccuracy Specification

Apart from the frequency noise, the deterministic frequency inaccuracy (f_{err}) between the applied microwave burst and qubit resonant frequency also

[1] An f_R of 1 MHz is targeted as the required β and β/bw_{PLL}^2 are more stringent given a realistic bw_{PLL}.

degrades the fidelity. For a θ of π, the infidelity incurred due to f_{err} is [39]:

$$1 - F = \frac{f_{err}^2}{f_R^2}. \tag{2.18}$$

Considering an infidelity of 0.001% and a qubit rotation speed of 1 MHz, the required frequency inaccuracy f_{err} should be below 3 kHz. At first glance, a fractional-N PLL might be required to achieve the required f_{err}. However, it is challenging to design a low-jitter fractional-N PLL with low power consumption. Instead, a power-efficient approach would be to use an individual Numerically Controlled Oscillator (NCO) to synthesize the required *fractional* frequency of each qubit [29]. Consequently, a single power-efficient integer-N PLL can be used to upconvert the qubits' baseband signals and address multiple qubits simultaneously.

2.5 Tuning Range Specification

Qubit state manipulation and readout require the generation and acquisition of microwave bursts. For the manipulation of a single transmons qubit, 4–8-GHz bursts of ∼50-ns duration are typically applied [37]. On the other hand, ∼1-μs bursts in a frequency range of 10-20-GHz are typically applied for the manipulation of a single spin qubit [36]. To offer system-level flexibility and ensure scalability, the PLL should be tunable in a wide frequency range, e.g., 9-to-21 GHz for spin qubits, assuming enough margin to adapt to PVT variations. A divide-by-2 or divide-by-3 circuit could be used to generate the required frequencies for transmons.

2.6 Conclusion

In this chapter, the VCO and PLL specifications are firstly derived based on the control fidelity for a single-qubit operation. The specifications obtained in this chapter are instrumental and will be used as the guideline for designing VCOs and PLLs in the following chapters.

Chapter

3

Device Modeling for Cryogenic Circuit Design

Chapter 2 showed that the specifications of a cryo-CMOS phase-locked loop (PLL) for scalable quantum computers are challenging. Moreover, the design of such a PLL requires the characterization and modeling of active and passive devices operating at cryogenic temperatures. In this chapter, both active and passive device behaviors at cryogenic temperatures are briefly summarized. A simplified transistor model based on Veriloga is introduced to predict the PLL performance at cryogenic temperatures. This chapter comprises four sections. In Section 3.1, the characteristics of active devices at cryogenic temperatures are elaborated. Section 3.2 discusses the cryogenic behaviors of passive devices. In Section 3.3, a modified noise model of the transistor is developed by considering the shot-noise effect at cryogenic temperatures. Finally, Section 3.5 concludes this chapter.

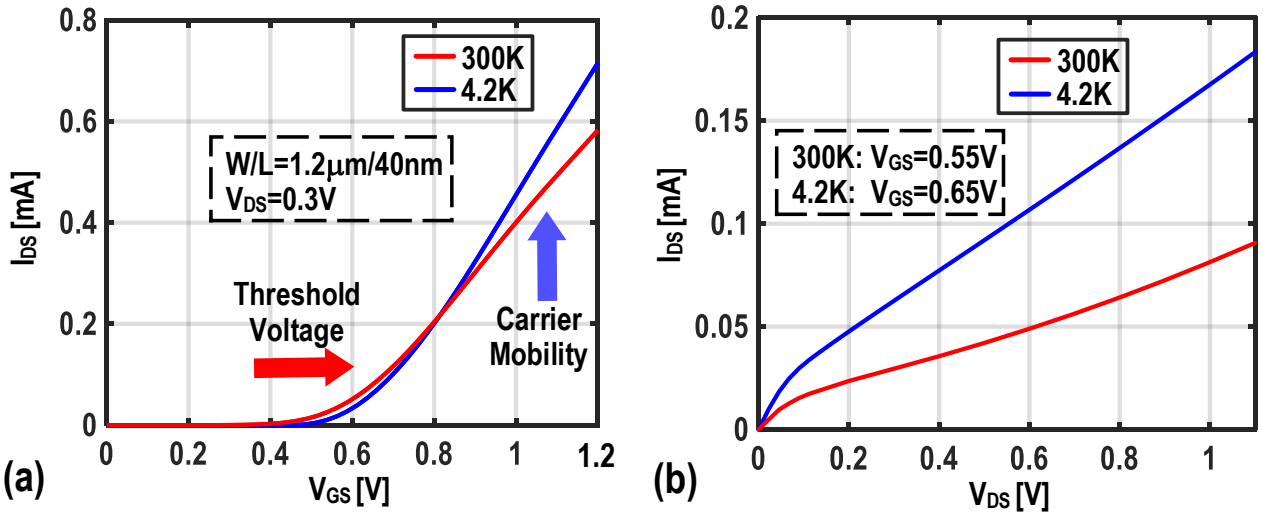

Figure 3.1: Measured (a) I_{DS} verus V_{GS} and (b) I_{DS} verus V_{DS} of an NMOS transistor (W/L=1.2μm/40nm) fabricated in a 40-nm bulk CMOS.

3.1 Active Devices

Standard foundry process development kits (PDK) do not offer device models for cryogenic temperatures. Therefore, since the inceptive proposal of cryo-CMOS circuits and systems for quantum computing applications, significant effort has been made in the past few years to characterize and model CMOS transistors operating at cryogenic temperatures in various technology nodes [109–115]. This section reviews the cryogenic characteristics of devices from prior-art data, which helps to build a simplified device model to facilitate the PLL design.

Due to the Fermi-Dirac scaling and bandgap widening [111, 112, 116], compared with room temperature, the measured threshold voltage of transistors (V_{TH}) increases by ∼100 mV for 40-nm bulk CMOS transistors at 4.2 K. The increased V_{TH} limits the voltage headroom of cascode-based circuit topologies, presenting a challenge to meet linearity and swing requirements. Besides, the mobility of both electrons and holes substantially increases due to the reduced phonon scattering at cryogenic temperatures [112]. As a result, as shown in Fig. 3.1 (a), due to the increase in V_{TH} and mobility at 4.2 K, the measured drain current (I_{DS}) of an NMOS transistor increases for a larger gate-to-source voltage (V_{GS}) and decreases for a smaller V_{GS}. Consequently, although the on-resistance of a transmission gate at cryogenic temperatures reduces when the input voltage is close to the supply or ground level, it can increase by more than two orders of magnitude when the input voltage is near the middle of the

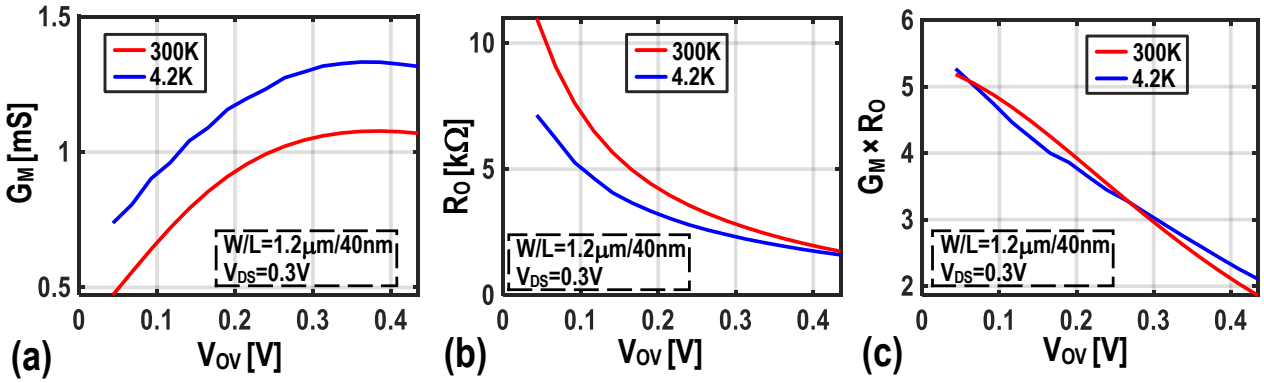

Figure 3.2: Simulated (a) G_M, (b) R_O, and (c) $G_M \times R_O$ versus V_{OV} of a common-source amplifier operating at 300 K and 4.2 K.

supply voltage. This could lead to severe problems in a sampling circuit [58].

Fig. 3.1 (b) depicts the measured drain current (I_{DS}) versus drain-to-source voltage (V_{DS}) characteristics under the same overdrive voltage ($V_{OV} = V_{GS} - V_{TH}$) of ∼200 mV at both 300 K and 4.2 K. Due to the increase in the carrier mobility at 4.2 K, the transistor exhibits an increase in both the current driving capability and output conductance. Based on the measured drain current versus gate-source and drain-source voltage (i.e., Fig. 3.1), a look-up-table-based Verilog-A model was built to capture the DC behavior of transistors[1]. This model helps to predict the phase-detection gain and other PLL loop parameters at 4.2 K through transient and DC simulations. It is also helpful for other circuits, such as voltage regulators, bandgap references, and ring oscillators. According to the developed Verilog-A model, Fig. 3.2 (a)-(c) respectively depict the simulated transconductance (G_M), output resistance (R_O), and intrinsic gain ($G_M \times R_O$) of a common-source amplifier operating at both 300 K and 4.2 K. Compared with 300 K, although the simulated G_M increases, the output resistance reduces, leading to a minor change in the intrinsic gain.

The statistical behaviors of transistors at cryogenic temperatures were studied in [116, 117]. The drain-current mismatch of transistors could be expressed as:

$$\sigma^2_{\Delta I_{DS}/\bar{I}_{DS}} = \sigma^2_{\Delta\beta/\bar{\beta}} + \left(\frac{G_M}{\bar{I}_{DS}}\right)^2 \cdot \sigma^2_{\Delta V_{TH}}, \tag{3.1}$$

where σ is the standard deviation operator and β is the current factor [118]. The threshold-voltage and current-factor variability can be described by $\sigma^2_{\Delta\beta/\bar{\beta}} =$

[1] See Appendix A.1.

$A_\beta/\sqrt{WL}$ and $\sigma^2_{\Delta V_{TH}} = A_{VTH}/\sqrt{WL}$ [119]. Compared with room temperature, A_β and A_{VTH} respectively increase by 78% and 22% at 4.2 K [116]. This implies that transistors exhibit a much large current mismatch at 4.2 K. Therefore, the matching performance of a current mirror, a current-steering DAC, and a charge pump is severely degraded at cryogenic temperatures.

There is a lack of literature on characterizing AC parameters of bulk-CMOS transistors operating at cryogenic temperatures. Based on the small-signal characterization of a 32-nm SOI CMOS presented in [120], it can be concluded that the gate capacitances (i.e. C_{GS} and C_{GD}) exhibit a negligible change from 293 K to 6 K. An increase in transconductance while a minor change in gate capacitances leads to an increase in device transit frequency.

At cryogenic temperatures, the self-heating of transistors cannot be ignored, as the junction temperature of devices can be easily much higher than the ambient temperature. [113] showed that an NMOS transistor with a dimension of 12 μm/40 nm can raise its junction temperature from 4.2 K to more than 50 K when dissipating 6.5 mW. Therefore, a designer should pre-calculate the junction temperature of critical transistors in noise-sensitive circuits for selected device dimensions, and further optimize the design if the junction temperature is too high.

3.2 Passive Devices

The characterization and modeling of passive devices are presented in [121]. This section summarizes the main findings for the sake of convenience. The quality factor of a spiral inductor at lower frequencies is limited by the metal resistance. It is proportional to the operation frequency. Compared with room temperature, the metal resistance reduces by $\sim 5\times$ at 4.2 K [121]. Hence, the measured quality factor of a spiral inductor at lower frequencies improves by $\sim 5\times$ [121]. As the frequency increases, skin effect cannot be ignored. The quality factor increases slowly when the frequency increases. Since the skin resistance improves by only 2.26×, the peak quality factor improvement at 4.2 K is limited to ∼2.5× [121]. Nevertheless, the inductance and capacitance change marginally (∼5%) from RT to 4.2 K [121]. Those variations were accounted for by increasing the conductivity of metals (5×) and the substrate resistivity (800×) in both the EM and parasitic extraction

tools, which were used to predict the VCO performance at 4.2 K. While the sheet resistance of the unsilicided polysilicon resistor is fairly constant over temperature, the silicided counterpart exhibits ∼2.5× resistance reduction from RT to 4.2 K. Hence, the passive loop filter of an analog PLL can be designed to be relatively immune to temperature variations by adopting MOM capacitors and unsilicided polysilicon resistors.

3.3 Noise Modeling

The previous literature on noise modeling of transistors operating at 4.2 K is scarcely available. In [120], a systematic study of the white-noise performance of 32-nm SOI MOS transistors has been carried out down to 6 K and results imply that the measured white noise does not scale as temperature. In this section, a modified noise model of transistors is proposed to better predict the noise performance at 4.2 K.

The channel noise of a long-channel MOS transistor is typically modeled by

$$S_{n,ch}(f) = 4KT_{ch}\gamma g_{ds0}, \tag{3.2}$$

where T_{ch} is the channel temperature, γ is the noise coefficient, and g_{ds0} is the channel conductance under 0-V drain-source voltage. When this transistor is biased in the saturation region, (3.2) can be rewritten as

$$S_{n,ch}(f) = 4KT_{ch}\gamma g_{m}, \tag{3.3}$$

where g_m is the transcondutance. Compared with 300 K, one would expect an 18.5-dB noise reduction at 4.2 K. This contradicts the measurement results presented in [120], which shows ∼10-dB improvement.

Notice that (3.3) assumes that the channel noise is thermal noise and proportional to T_{ch}. This is based on the assumption that carriers in the channel undergo scattering collisions, exchange energy with the lattice, and reach thermal equilibrium with the environment. These assumptions are valid for long-channel devices as the mean-free-path of carriers (∼100 nm) is much shorter than the channel length. However, if a short-channel device is required (e.g., L<100 nm) to optimize speed and to minimize parasitic capacitance, the assumptions underlying (3.3) are invalid since most carriers undergo little

scattering collisions, the carriers in the channel do not have sufficient time to reach thermal equilibrium, and carrier behavior tends more toward the shot noise [122–125]. Therefore, the channel's white noise is not entirely thermal noise and can be empirically modeled by [126]:

$$\overline{i_{n,ch}^2(t)} = 4KT_{ch}g_m(t) \cdot \xi \cdot (1-\nu)^2 + 2qI_D(t) \cdot \nu^2, \tag{3.4}$$

where ξ is the noise coefficient, and ν^2 is the Fano factor and a function of the channel length. ν reaches 0 in a long-channel device, and the resulting channel noise is dominated by the thermal noise. On the other hand, it approaches 1 in a short-channel device, and the channel noise tends to be shot noise. For a 40-nm channel-length transistor, ∼25% of the total channel noise is contributed by the shot noise at 300 K [122]. Since the shot noise weakly depends on the temperature, it could set a bottleneck for the noise reduction at 4.2 K. Based (3.4), the "white_noise" function built in Verilog-A[1] was used to model the power spectrum density of both the thermal noise and shot noise transistors at 4.2 K.

The flicker noise power spectral density of a transistor can be modeled by

$$\overline{i_{n,fl}^2(t)} = \frac{K_P}{WLC_{ox}} \cdot \frac{1}{f} \cdot g_m^2(t), \tag{3.5}$$

where K_P is a process-dependent constant, W and L are core transistors' width and length, respectively, and C_{ox} is an oxide capacitance per area [127]. Unlike the thermal noise, there is no indication of any temperature-dependent mechanism for flicker noise if a constant g_m is used over temperatures [114,115].

3.4 Cryogenic Effects on Cryo-CMOS PLL Design

While the reduction of the thermal noise and increase in the quality factor help to improve the phase noise of an *LC* oscillator operating at 4.2 K, the improvement is not substantial and is limited to ∼10 dB [48]. Notice that, based on the discussion in the previous chapter, the PLL must deliver a phase noise below -129 dBc/Hz at 10-MHz for a carrier frequency ranging from 10 GHz to 20 GHz. This is demanding even though the phase noise reduction

[1] See Appendix A.1.

at 4.2 K is considered. Moreover, a reference spur below -54-dBc must be guaranteed for the qubit frequency division multiplexing, which is challenging even at 300 K. Unfortunately, there is no indication that the spur improves at 4.2 K. Moreover, the *LC* oscillator flicker corner is expected to increase at 4.2 K, requiring a wider PLL bandwidth to relax the oscillator phase noise. This tends to degrade the reference spur performance at 4.2 K.

3.5 Conclusion

Transistors exhibit large deviations in their parameters, such as higher threshold voltage, higher mobility, and worse mismatch when operating at 4.2 K [111, 112, 116]. Moreover, the channel noise of a short-channel device is dominated by shot noise. Therefore, a Verilog-A based model was built to facilitate the design of active circuits at 4.2 K. The inductor shows a $\sim$2.5$\times$ increase in quality factor and there are minor changes in the inductance and MOM capacitance values at 4.2 K. These variations can be replicated in EM simulations by manipulating the resistivity of metals and substrate. This enables, in combination with active device models, the reliable design of cryogenic PLLs.

Chapter

4

A Cryo-CMOS Oscillator with an Automatic Common-Mode Resonance Calibration

In the previous chapter, the characteristics of on-chip active and passive devices operating at cryogenic temperatures are elaborated, and a simplified device model was developed. This chapter presents a cryo-CMOS LC oscillator for quantum computing applications[1]. An oscillator is the heart of a frequency synthesizer and its phase noise performance is very critical for the fidelity introduced by a qubit controller. As a proof of concept, a 5-GHz oscillation frequency is targeted as both transmons and spin qubits can be addressed when a frequency doubler and triple are used.

To reveal the substantial gap between the theoretical predictions and measurement results at cryogenic temperatures, a new phase noise expression for an oscillator is derived based on the presented device model. To reach the optimum performance of an LC oscillator, a common-mode (CM) resonance technique is implemented. Additionally, this chapter presents a digital calibration loop to adjust the CM frequency automatically at 4.2 K,

[1]This chapter has been published in the Systems I: Regular Papers [69].

reducing the oscillator's phase noise and thus improving the control fidelity. The calibration technique reduces the flicker corner of the oscillator over a wide temperature range ($10\times$ and $8\times$ reduction at 300 K and 4.2 K, respectively). At 4.2 K, our 0.15-mm^2 oscillator consumes a 5-mW power and achieves a PN of -153.8 dBc/Hz at a 10 MHz offset, corresponding to a 200-dB FOM. The calibration circuits consume only a 0.4-mW power and 0.01-mm^2 area.

4.1 Introduction

As mentioned in Chapter 1, a local oscillator operating at cryogenic temperatures (CT) is required to down/up-convert the desired signals. However, designing a cryo-CMOS oscillator presents several challenges. Firstly, low phase noise (PN) is required to ensure that the oscillator does not limit the overall fidelity of a quantum computer (see Chapter 2). Secondly, the oscillator must operate at CT, where devices exhibit large temperature-induced variations of the parameters and no mature device models are available. Finally, as the cryogenic refrigerator has a limited cooling power, a low power consumption (P_{DC}) is required. Although standalone LC oscillators operating down to 4.2 K are presented in [48,49,51,65,128], only the cryogenic LC oscillators in [48,51] are implemented in a standard CMOS process. Yet, the oscillator presented in [51] had poor phase noise, failing to meet the stringent specifications required for a quantum computer. On the other hand, the oscillator's PN at lower frequency offsets in [48] is severely compromised at 4.2 K, complicating cryo-CMOS PLL designs for quantum computing applications.

In the last few years, several flicker PN reduction techniques have been proposed at RT: 1) inserting resistances in series to the drain of oscillation sustaining devices [129]; 2) narrowing down the conduction angle of oscillation sustaining devices [130,131]; 3) shifting the phase of the gate voltage against the drain voltage by tuning the capacitance ratio of the gate and drain capacitors in a transformer-based complementary oscillator [132]. Nevertheless, adding drain resistors degrades an oscillator's PN in the 20 dB/decade region with low supply and high current consumption. Besides, narrowing down the conduction angle needs careful consideration of the oscillation startup. Finally, the gate–drain phase shift reduces the passive voltage gain from the drain to gate, and degrades an oscillator's PN in the 20 dB/decade region.

The PN performance of an LC oscillator can be enhanced by adjusting the common-mode frequency of the circuit (F_{CM}) to be at twice the oscillation frequency (F_O). When such a technique is correctly employed, the Q-degradation due to the triode operation of the differential pair is alleviated, and the flicker noise up-conversion to PN is also ideally eliminated [133]. Initially, this condition was satisfied by a separately tuned common-mode (CM) tank [134–136]. Yet, the requirement for an extra inductor incurs an area penalty, and the

need to tune it limits the frequency-tuning range. By introducing a single-end capacitor bank in the main tank, the authors of [127, 133, 137–139] also fulfilled the CM resonance condition by accurately modeling the CM inductance and manually controlling the ratio of single-ended to differential-mode (DM) capacitance without the use of tail inductor. However, in the presence of PVT variations, the parasitic capacitance of the oscillator's core devices and the switches in the capacitor banks changes dramatically, shifting the expected F_{CM}. Consequently, even at RT, some mechanisms should be added to adjust the DM and CM capacitor banks such that the oscillator operates near its optimum performance. This issue is even more prominent at CT, since the silicon substrate becomes highly resistive due to carrier freeze-out in the substrate, reducing the parasitic capacitance to ground up to 3.6× [121]. The resulting F_{CM} is expected to change dramatically, degrading PN at 4.2 K [48].

In this chapter, we propose a digital calibration loop, which automatically adjusts the configuration of the DM and CM capacitor banks to ensure that the oscillator always operates near its optimum performance at 4.2 K. This chapter is organized as follows. By considering the shot-noise effect for short channel devices in Section 4.2, a new PN expression for an oscillator is derived. Section 4.3 presents the proposed CM resonance calibration technique and details the circuit implementation and design considerations for the cryogenic operation. The measurement results and conclusions are presented in Section 4.4 and Section 4.5, respectively.

4.2 Phase Noise Analysis

Based on the analysis presented in Chapter 2, both the oscillator's PN in the thermal noise region and its flicker PN corner f_C are critical to avoid limiting the qubits' intrinsic fidelity. Fig. 4.1 (a) shows the schematic of a class-D/F_2 oscillator adopted in our design to satisfy these criteria simultaneously. Two sets of capacitors (C_C and C_D) are used to adjust the fundamental and second harmonic resonance of the oscillator, respectively. Due to the auxiliary CM resonance at $2F_O$, this topology reaches within 3 dB of the theoretical PN limit of an ideal cross-coupled *LC* oscillator for a given power consumption (P_{DC}) [133]. Meanwhile, the flicker noise up-conversion of the differential pair transistors ($M_{1,2}$) to PN is also reduced due to the symmetry of oscillation

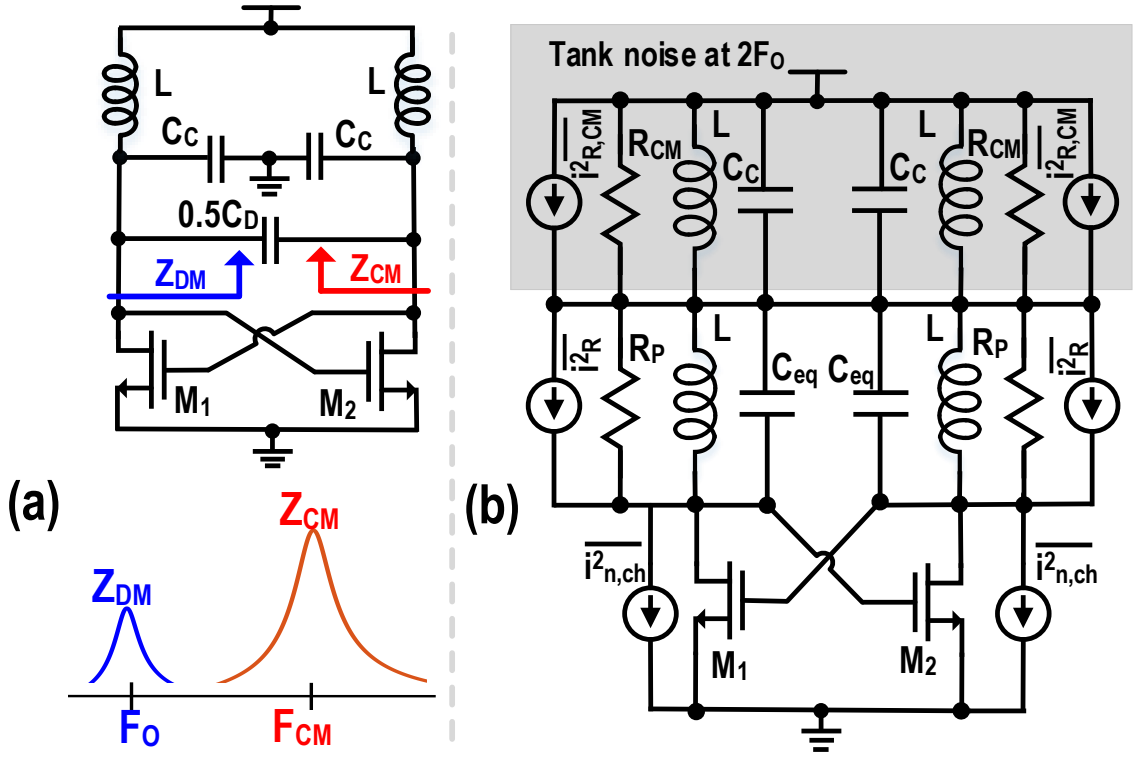

Figure 4.1: (a) A class-D/F_2 oscillator's schematic and tank impedance, and (b) its corresponding noise sources.

waveforms, thus lowering f_C significantly. Since the oscillator must operate at CT, it is instrumental in understanding its PN behavior at those temperatures as well. However, the conventional PN analysis is insufficient to quantify the difference between the theoretical and measured PN at CT. To this end, a new PN expression for short-channel devices is derived in this section by considering the shot-noise effect.

4.2.1 Limitation of Conventional PN Analysis

Assume that the channel's current noise generated by a MOS transistor is proportional to its transconductance (g_m) according to the following equation [140]

$$\overline{i^2_{n,ch}(t)} = 4KT_{ch}\gamma g_m(t)^1, \tag{4.1}$$

with K Boltzmann's constant, T_{ch} the channel temperature, and γ the noise coefficient. The PN expression for the oscillator can be found in previous

[1] This equation was introduced in Chapter 2 and is rewritten here for convenience.

works [140–142] and is rewritten as

$$\mathcal{L}(f) = 10\log_{10}\left(\frac{KT_R}{2R_P C_{eq}^2 V_{osc}^2} \cdot \frac{1}{(2\pi f)^2} \cdot \left(1 + \gamma \cdot \frac{T_{ch}}{T_R}\right)\right), \tag{4.2}$$

with R_P the equivalent tank parallel resistance, C_{eq} the equivalent tank parallel capacitance, V_{osc} the single-ended oscillation amplitude, and T_R the absolute temperature of the *LC* tank. By analyzing the variation of temperature-dependent terms in (4.2), the PN at 4.2 K could be partially understood according to the measured characteristics of devices from the target 40-nm CMOS process.

Compared with 300 K, one would expect an ∼18-dB PN reduction by assuming $T_R = T_{ch} = 4.2$ K, as predicted by (4.2). In addition, the measured ON-resistance of a transistor reduces by ∼2.5× due to the enhanced carrier mobility [111, 112, 143], and the measured quality factor of a spiral inductor exhibits up to a ∼2.5× increase due to both the higher substrate resistivity and metal conductivity at 4.2 K [121]. Consequently, the tank quality factor and R_P are expected to increase by ∼2.5×, thus reducing PN by ∼4 dB. Suppose that the oscillator is operating in the voltage-limited region at both 300 K and 4.2 K. Then, V_{osc} is expected to be fairly constant. Since the measured capacitance of a MOM capacitor (typically used in *LC* tank) changes only ∼5% from 300 K to 4.2 K [121], C_{eq} is not expected to vary significantly. Therefore, the estimated PN improvement of an oscillator is ∼22 dB. This contradicts with the measurement results presented in [48, 50, 51, 55], which show a maximum 12-dB PN reduction when differential pair transistors are implemented by short-channel devices. Such a performance gap between the theoretical analysis and measurement results requires an alternative method of analyzing PN at 4.2 K.

The above analysis assumes $T_R = T_{ch} = 4.2$ K. In practice, the self-heating of devices could raise T_R and T_{ch} much higher than 4.2 K. For instance, by dissipating a 2-mW P_{DC}, a transistor measuring 12 μm/40 nm could exhibit a T_{ch} of ∼44 K due to the self-heating at 4.2 K [113]. However, considering the device dimensions (i.e., 64 μm/270 nm and 135 μm/40 nm) and P_{DC} (i.e., 12 mW and 5 mW) of two published cryo-CMOS oscillators in [48, 50] respectively, the T_{ch} in prior-art designs is estimated to be below 8 K. Besides, T_R is estimated to be ∼4.2 K due to the proper thermalization of the *LC* tank, as typically

implemented by ultra-thick and wide metals to reduce the loss. Consequently, compared with 300 K, the estimated PN reduction of an oscillator is ∼19 dB even by considering the self-heating effect, which is 7 dB higher compared with measurement results [48, 50, 51, 55].

(4.1) assumes that the channel noise is thermal noise and proportional to T_{ch}. As mentioned in Chapter 3, this assumption is not valid for a short-channel device (e.g., L<100 nm) since most carriers do not have sufficient time to reach thermal equilibrium. The total channel noise contains a large portion of temperature-independent shot noise and should be modeled by [126]:

$$\overline{i_{n,ch}^2(t)} = 4KT_{ch}g_m(t) \cdot \xi \cdot (1-\nu)^2 + 2qI_D(t) \cdot \nu^2, \tag{4.3}$$

where ξ is the noise coefficient, and ν^2 is the Fano factor and a function of the channel length. ν reaches 0 in a long-channel device, and the resulting channel noise is dominated by the thermal noise. On the other hand, it approaches 1 in a short-channel device, and the channel noise tends to be shot noise. For a 40-nm channel-length transistor, ∼25% of the total channel noise is contributed by the shot noise at 300 K [122]. Since the shot noise weakly depends on the temperature, it could set a bottleneck for the PN reduction at 4.2 K.

4.2.2 PN Analysis by Considering Shot Noise

In this section, the conversion of the circuit noise to the oscillator's PN will be investigated. According to the linear time-variant model [144], the PN of an oscillator is expressed as

$$\mathcal{L}(f) = 10\log_{10}\left(\frac{\sum_j N_{L,j}}{2 \cdot C_{eq}^2 \cdot V_{osc}^2 \cdot (2\pi f)^2}\right). \tag{4.4}$$

$N_{L,j}$ is the effective current noise ($\overline{i_{n,j}^2}$) generated by the j-th device and is given by

$$N_{L,j} = \sum_{k=0}^{\infty} \overline{i_{n,j,k}^2} \cdot \frac{c_k^2}{2}, \tag{4.5}$$

where $\overline{i_{n,j,k}^2}$ is the current noise at frequencies of $kF_O \pm f$, and c_k is the k-th harmonic's amplitude of the impulse sensitivity function (ISF). $\overline{i_{n,j}^2}$ includes the noise due to resonant tank losses and the channel noise of the active

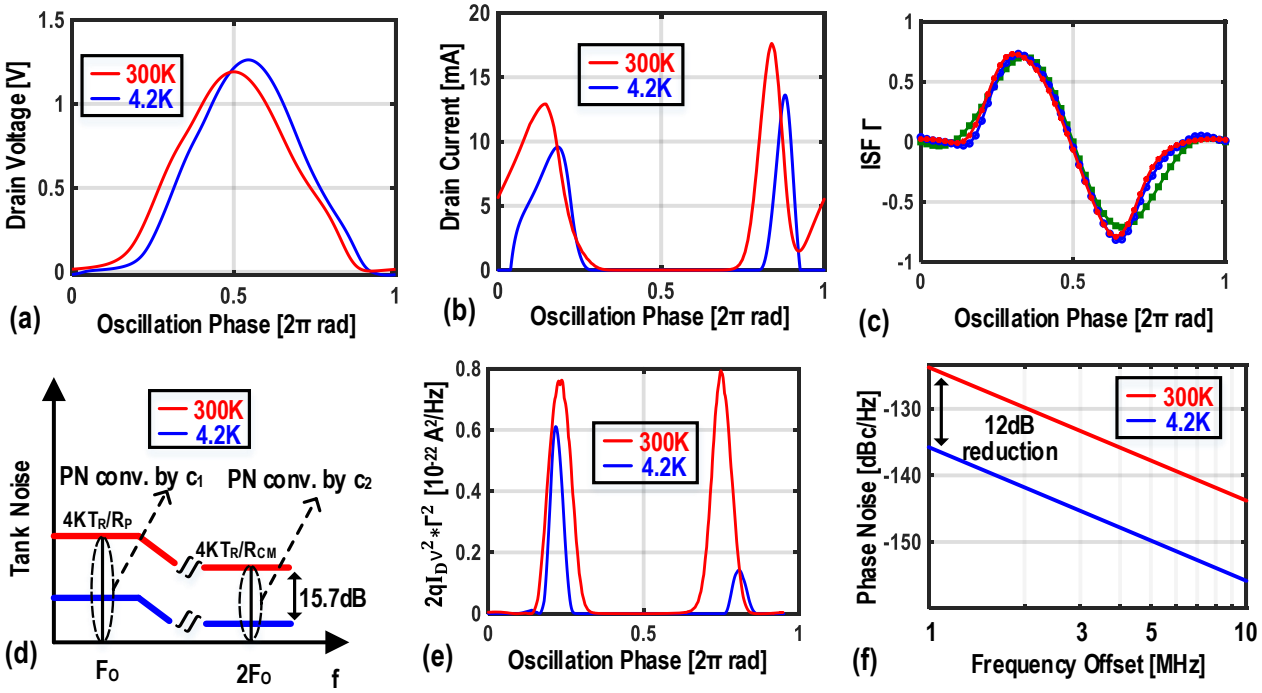

Figure 4.2: Simulated (a) drain voltage and (b) drain current of M_1, and (c) ISF function; (d) illustration of the tank noise conversion to PN; (e) simulated effective current noise due to shot noise of $M_{1,2}$;(f) simulated PN at 300 K and 4.2 K.

devices. Note that there are two resonances (i.e., ∼5/10 GHz) in the tank. The mechanism of how the two resonant peaks affect the PN will be firstly investigated. The PN contributed by the $M_{1,2}$ will be discussed later.

Fig. 4.1 (b) illustrates the major noise sources of a class-D/F_2 oscillator, including the noise of the *LC* tank and differential pair transistors $M_{1,2}$. R_P and R_{CM} are used to model the tank losses at the fundamental and second-harmonic frequencies, respectively. In general, the ISF is related to the shape of the oscillator's waveform [144]. Due to the waveform clipping of a class-D/F_2 oscillator, it could be empirically estimated by

$$\Gamma(t) \approx \frac{1}{2} \cdot (\sin(2\pi F_O t) - m \cdot \sin(4\pi F_O t)), \tag{4.6}$$

where m is a constant (∼$2/\pi$) and depends slightly on the tank quality factor, based on simulations.

4.2.2.1 Noise of the Tank

Since the noise of R_P at frequencies far away from the fundamental is highly attenuated by the *LC* tank, based on (4.5), the conversion from R_P's

noise to PN is then governed by c_1. Hence, the effective noise due to R_P could be found as

$$N_{L,R_P} = 2 \cdot \frac{4KT_R}{R_P} \cdot \frac{1}{2 \cdot 4} = \frac{KT_R}{R_P}. \tag{4.7}$$

The tank also largely filters the R_{CM} noise at frequencies far from the second harmonic. According to (4.5), the conversion from R_{CM}'s noise to PN is based on c_2. The effective noise due to R_{CM} thus could be be expressed as

$$N_{L,R_{CM}} = 2 \cdot \frac{4KT_R}{R_{CM}} \cdot \frac{m^2}{2 \cdot 4} = \frac{m^2 KT_R}{R_{CM}}. \tag{4.8}$$

4.2.2.2 Noise of the $M_{1,2}$

Unlike the noise generated by the tank, the noise of $M_{1,2}$ is cyclostationary due to the periodic time-varying nature of the $g_m(t)$ and $I_D(t)$. Based on the Parseval's theory, (4.5) could be rewritten as

$$N_{L,j} = \int_0^{T_{osc}} \frac{\Gamma^2(t)}{T_{osc}} \cdot \overline{i_{n,j}^2(t)} \cdot dt. \tag{4.9}$$

Since the drain current $I_D(t)$ is periodic, it can be expanded in Fourier series as

$$I_D(t) = I_0 \cdot (1 + \sum_{p=1}^{+\infty} \eta_p \cos(2\pi p F_O t + \Phi_p)). \tag{4.10}$$

Assume that Φ_p is zero for the worst-case scenario. By substituting (4.6), (4.10), and the second term of (4.3) into (4.9), the effective noise due to the shot noise of $M_{1,2}$ could be estimated by

$$N_{L,shot} \approx \frac{q\nu^2 I_0}{2} \cdot (1 + m^2 - m\eta_1 - \frac{\eta_2}{2} + m\eta_3 - \frac{m^2\eta_4}{2}). \tag{4.11}$$

Similarly, the effective noise due to the thermal noise of $M_{1,2}$ can be found by substituting (4.6) and the first term of (4.3) into (4.9)

$$N_{L,the} = 2 \cdot \int_0^{T_{osc}} \frac{\Gamma^2(t)}{T_{osc}} \cdot 4KT_{ch}\xi g_m(t) \cdot (1-\nu)^2 \cdot dt \approx \frac{KT_{ch}}{R_P} \cdot \xi \cdot (1-\nu)^2. \tag{4.12}$$

Table 4.1: Calculated and simulated PN contribution at 5 GHz.

PN results @ a 1MHz frequency offset	Noise Sources @ 300K				Noise Sources @ 4.2K			
	Tank	Shot	Thermal	Total	Tank	Shot	Thermal	Total
Cal. based on (4)-(13)	-127.0	-127.8	-128.5	-123.0	-147.5	-134.5	-149.1	-134.2
Cal. based on Fig. 2	-126.9	-129.5	-129.3	-123.6	-147.3	-136.5	-151.0	-136.0
Sim. in Spectre RF™	-127.1	-129.3	-129.7	-123.8	-147.6	-136.2	-151.3	-135.8

4.2.2.3 PN Expression

The complete PN expression can be estimated by substituting (4.7), (4.8), (4.11), and (4.12) into (4.4).

$$\mathcal{L}(f) \approx 10\log_{10}\left(\frac{N_{L,R_P} + N_{L,R_{CM}} + N_{L,shot} + N_{L,the}}{2 \cdot C_{eq}^2 \cdot V_{osc}^2 \cdot (2\pi f)^2}\right). \tag{4.13}$$

Based on transient simulations, Fig. 4.2 (a) and (b) depict the simulated drain voltage and drain current of M_1 over one oscillation period at both 300 K and 4.2 K under a 0.5-V supply. $M_{1,2}$ are based on a look-up-table-based Verilog-A model built from the measured drain current versus gate-source and drain-source voltage[1]. In addition, based on (4.3), the channel white noise is also included in this model[2] to simulate the phase noise at the 20dB/decade region. The inductor is based on a lumped-element model, whose parameters are modified to account for the temperature variation [121]. Compared with 300 K, while the oscillator consumes less current due to the increase of threshold voltage of transistors at 4.2 K, it exhibits a slightly higher oscillation swing due to a 2.5× higher tank quality factor. As expected, as shown in Fig. 4.2 (c), the simulated ISF function from the transient simulation is relatively immune to temperature variations as the oscillation waveforms show similar shapes.

Assumes that $\xi \cdot (1-\nu)^2 = 1$ and $\nu^2 = 0.5$ for a 40-nm channel length transistor. This ensures that the shot noise of $M_{1,2}$ in saturation region contributes to 25% of the total simulated channel noise, which is in line with the study in [122]. In addition, by considering the self-heating effect (i.e.,

[1]This is because the foundry PDK does not support device models at cryogenic temperatures.

[2]The "white_noise" function built-in Verilog-A is used to model the power spectrum density of both the thermal noise and shot noise of $M_{1,2}$ [i.e., (4.3)]. Then, conventional PSS/PNOISE simulations in Spectre RF™ are used to predict the oscillator's phase noise at 4.2 K.

$T_R = T_{ch} = 8\,K$), Fig. 4.2 (d) illustrates the mechanism of the tank's thermal noise conversion to PN, where c_1 and c_2 determine the conversion of the noise of the R_P and R_{CM}, respectively. Thanks to the T_R reduction, the effective noise due to the tank's thermal noise is significantly reduced. However, the effective noise due to $M_{1,2}$'s shot noise is only minorly reduced [see Fig. 4.2 (e)]. Consequently, as shown in Fig. 4.2 (f), compared with 300 K, the PN at 4.2 K only improves by 12 dB, limited by the shot noise. Table 4.1 summarizes the simulated and calculated PN contributions at both 300 K and 4.2 K due to the tank's thermal noise and $M_{1,2}$'s thermal noise and shot noise. The presented theory matches well with simulation results. Notice that the shot noise and thermal noise show a similar contribution to the PN even at 300 K. By moving to 4.2 K, the shot noise contributes more than 90% of the total PN due to the substantial reduction of the thermal noise. This implies that the shot noise must be carefully modeled for cryogenic designs.

4.2.3 PN Consideration in the Flicker Region

Unlike the thermal noise, there is no indication of any temperature-dependent mechanism for flicker noise if a constant g_m is used over temperatures [114, 115]. Since the ISF is relatively immune to temperature variations [see Fig. 4.2 (c)], the PN of an oscillator in the flicker region is not expected to change significantly at CT. Consequently, the flicker PN corner of an oscillator f_C raises mainly due to the PN reduction in the thermal noise region at CT. Fortunately, the flicker noise up-conversion can be significantly suppressed by the selected oscillator topology.

4.3 Class D/F_2 Oscillator with Common-mode resonance calibration

The class-D/F_2 oscillator has been designed for operation at both 300 K and 4.2 K. Performance targets have been set at 4.2 K for the control electronics of a quantum computer, while the room-temperature operation has been used for convenient circuit validation and debugging. As mentioned earlier, the oscillator's parasitic single-ended capacitance (C_P) is subject to PVT variations. The resulting CM frequency F_{CM} can change dramatically and

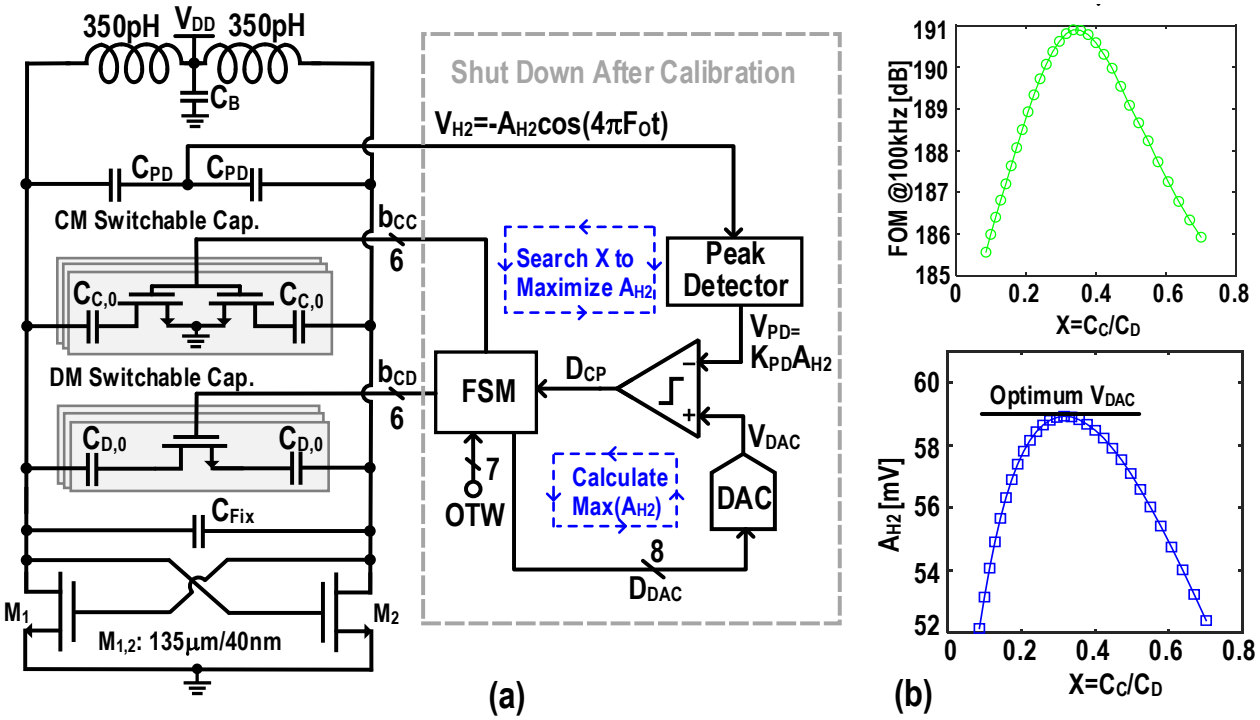

Figure 4.3: (a) Block diagram of the calibration loop with the schematic of a class-D/F$_2$ oscillator; (b) simulated FOM and A$_{H2}$ versus X.

hence deviate from 2F$_O$, thus degrading the PN performance. To resolve this issue, as depicted in Fig. 4.3, the oscillator features an automatic CM resonance calibration technique to optimize its PN over PVT variations. In this section, the implementation details of the CM resonance calibration loop and class-D/F$_2$ oscillator will be discussed by considering the effect of the cryogenic operation.

4.3.1 Class-D/F$_2$ Oscillator

As shown in Fig. 4.3 (a), the class-D/F$_2$ oscillator is implemented with a thin-oxide NMOS cross-coupled pair (M$_{1,2}$), which are sized with a minimum channel length so as to minimize C$_P$. To alleviate self-heating of the oscillator, the thermal resistance of M$_{1,2}$'s source, drain, and gate terminals are minimized in the layout by placing redundant vias. Two sets of switched capacitor banks (C$_C$ and C$_D$) are used to adjust the differential-mode and common-mode resonance of the oscillator, respectively. The implementation details of C$_C$ and C$_D$ can be found in [48]. The tank's quality factor degradation due to the switch loss of C$_C$ is very small (i.e., <10%). The control bits of C$_C$ and C$_D$ (b$_{CC}$ and b$_{CD}$) are derived from a finite-state machine (FSM). In addition, two

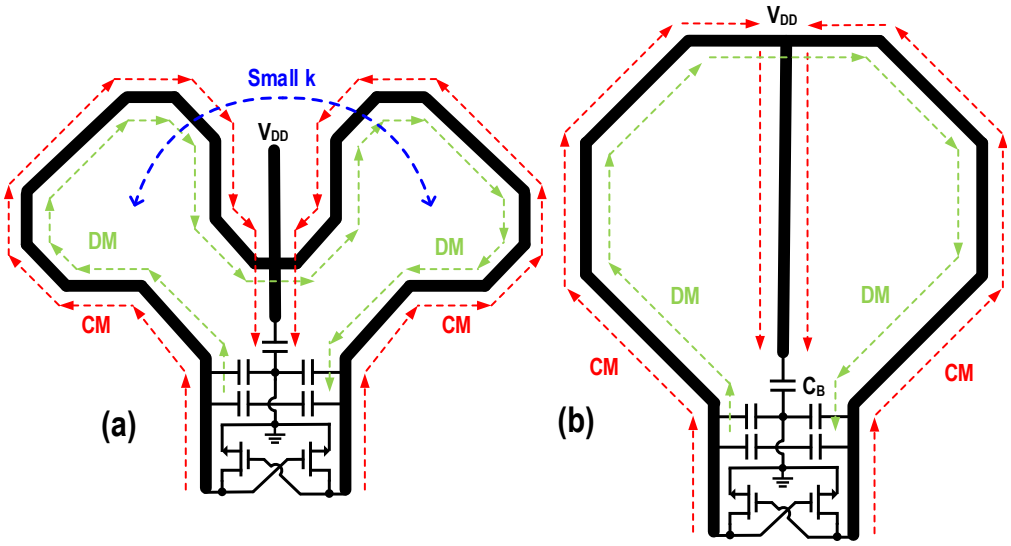

Figure 4.4: Layout view of the (a) optimized and (b) conventional inductor.

differential capacitors (C_{PD}) extract the second harmonic of the oscillation voltage A_{H2} (used for calibration). The mismatch between C_{PD} leaks the oscillator's fundamental voltage to the output, affecting the extracted A_{H2}. To achieve the required matching, each C_{PD} is implemented with a 10-fF MOM capacitor.

To satisfy the CM resonance condition, the ratio of single-ended to differential-mode capacitance ($X = C_C/C_D$) should be adjusted to (1+k)/(3-5k) [133], where k is the coupling factor between the tank inductors. However, the supply and ground routing could introduce undesired CM inductances and losses, destroying the CM resonance condition and incurring high PN [145]. To avoid this issue, an explicit CM current return path is realized by an embedded decoupling capacitor inside a transformer in [137]. On the other hand, the authors of [127, 133] employed coils with an even number of turns to ease the CM termination by ensuring the center tap close to core transistors. Moreover, k is larger than 0 so as to allow a large C_C in [127, 133]. However, to attain a low PN at a low supply voltage, the tank's DM impedance should be reduced, thus advocating for the use of a single-turn inductor. Since in that case, k becomes negative and the required C_C, which includes parasitics, reduces to impractically small values. This issue is even more severe when the CM return path is considered, which increases the CM inductance (L_{CM}) but has little effect on the DM inductance (L_{DM}). To minimize the unwanted magnetic coupling, as shown in Fig. 4.4 (a), we use two individual coils placed orthogonally to achieve $k \approx 0$. Furthermore, compared with a conventional

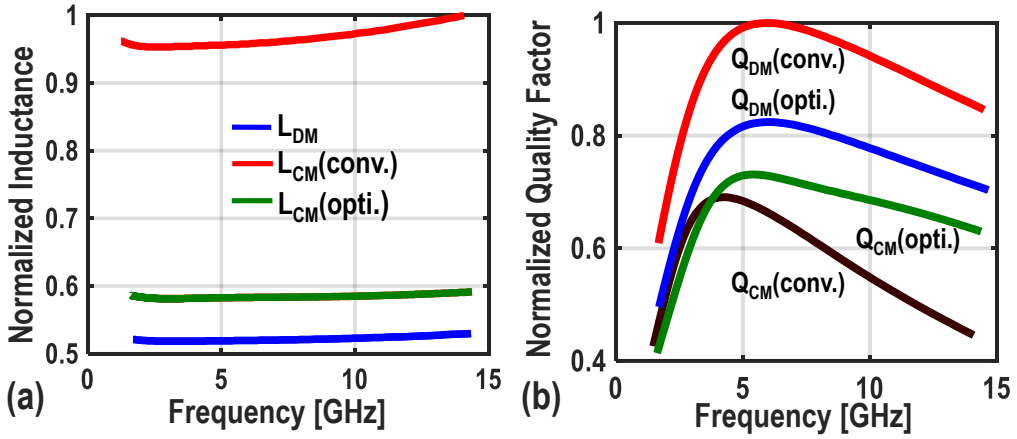

Figure 4.5: (a) Inductance and (b) quality factor comparison between the optimized and conventional inductor.

one-turn inductor as depicted in Fig. 4.4 (b)[1], the center tap of the optimized inductor is now much closer to the source of the core devices, thus alleviating parasitic L_{CM} by securing the shortest return path for the CM current. As shown in Fig. 4.5 (a), the optimized inductor shows a 1.6× lower L_{CM}. In addition, for the same inductance, the area of the proposed inductor is also ∼30% lower compared to that of the conventional spiral one. Unfortunately, as shown in Fig. 4.5 (b), the optimized inductor suffers from a slightly lower DM quality factor (Q_{DM}) due to the partial magnetic-flux cancellation inside each half inductor [146]. Nevertheless, it exhibits a higher CM quality factor (Q_{CM}) and hence a higher R_{CM}, which helps to reduce the PN in the thermal noise region based on (4.8). Notice that, without properly terminating the oscillator's second harmonic, the flicker PN corner f_C can be easily increased to ∼10 MHz at CT [65]. This translates to a stringent PN requirement in the thermal noise region [see Fig. 2.2 (b)]. Consequently, even with a slightly lower Q_{DM}, our inductor is still beneficial for cryogenic operation due to a better termination of the second harmonic.

4.3.2 Calibration Loop

As mentioned earlier, the X factor should be optimized to ensure that the oscillator operates near the optimum performance. This is evidenced in Fig. 4.3 (b), which indicates that the simulated FOM at a 100 kHz frequency offset is severely degraded when the X factor deviates from the optimum value. Consequently, some mechanisms should be added to optimize the PN. Notice

[1]The inductor shows a similarity with the transformer's primary winding presented in [137].

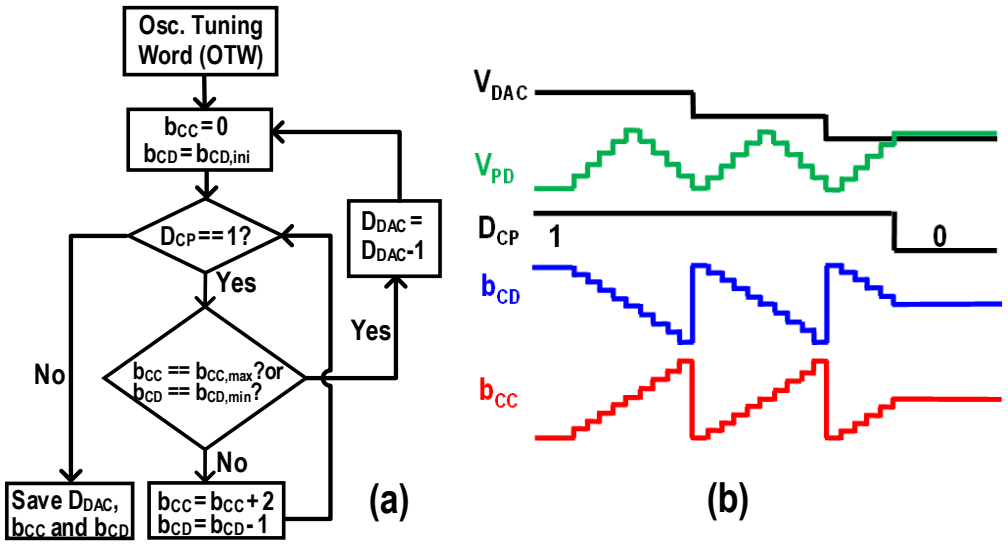

Figure 4.6: (a) Calibration flowchart and (b) conceptual waveforms during calibration.

that, due to the auxiliary CM resonance at $2F_O$, the oscillator's FOM, the tank's CM impedance, and thus the A_{H2} are virtually maximized for the same X value [see Fig. 4.3 (b)][1]. Hence, the calibration goal is to find the optimum b_{CD} and b_{CC} codes in which A_{H2} is maximized.

As shown in Fig. 4.3 (a), the calibration loop is composed of a peak detector, a comparator, a voltage DAC, and a finite state machine. At the beginning of the calibration, the CM capacitor bank is kept off, while b_{CD} is set to reach the desired frequency, resulting in the lowest possible X. The second harmonic of the oscillation voltage is extracted at the common node of differential capacitors C_{PD}. A peak detector with a gain of K_{PD} then produces a DC voltage (V_{PD}) proportional to A_{H2}. V_{PD} is compared with the output of the 8-bit DAC (V_{DAC}), and the result is fed to the finite-state machine (FSM).

For now, suppose that V_{DAC} is set exactly to the maximum V_{PD} ($=K_{PD} \cdot A_{H2,max}$). Initially, X is set at its minimum, and the tank configuration is not optimum; thus $V_{PD} < V_{DAC}$ and comparator output (D_{CP}) is one. Consequently, the FSM increases X via reducing b_{CD} by 1 LSB and increasing b_{CC} by 2 LSBs. In this way, the tank's total capacitance (C_C+C_D) and thus F_O remain almost constant during the calibration. This procedure continues until V_{PD}-V_{DAC} and D_{CP} become zero, indicating that the current b_{CD} and b_{CC} states are near the optimum.

The maximum V_{PD}, and hence the required V_{DAC}, depend on PVT, tank's

[1]Since the higher-order even harmonics are not terminated in this design, the maximum FOM and A_{H2} occur at slightly different X.

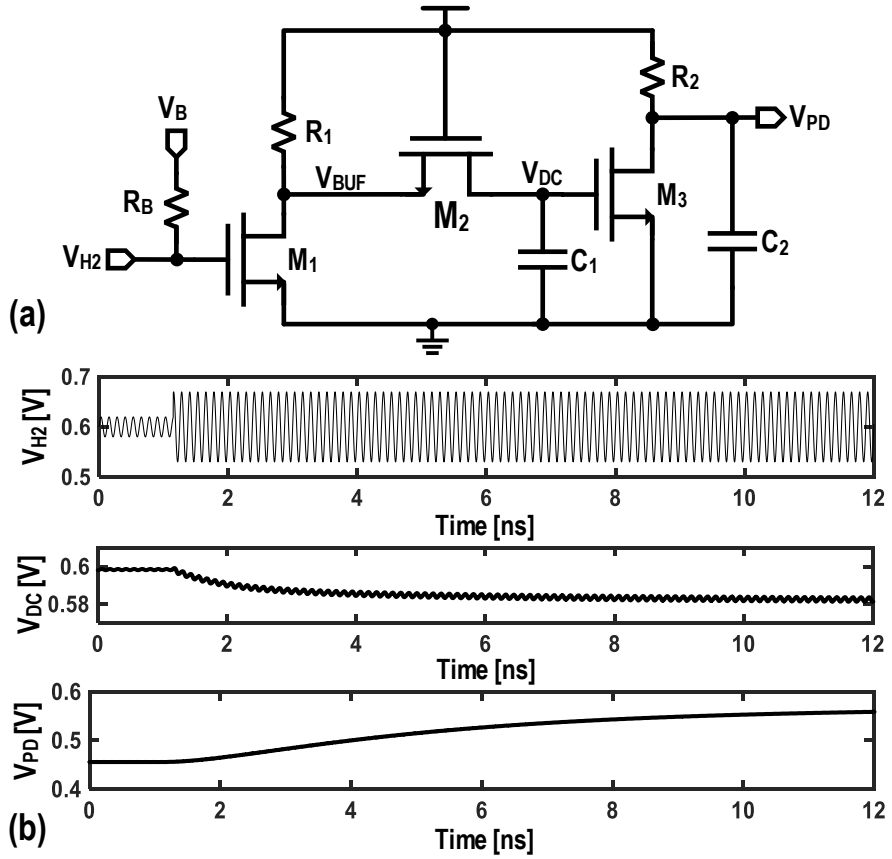

Figure 4.7: (a) Peak detector schematic and (b) simulated transient response of the peak detector at 300 K.

CM quality factor (Q_{CM}), and F_O. Therefore, a second loop is added to adjust V_{DAC} accordingly. Initially, V_{DAC} is intentionally set to a voltage level that is safely higher than the maximum possible V_{PD}. Hence, D_{CP} is always 1, resulting in X being swept from its minimum to maximum. The FSM then lowers down V_{DAC} by 1 LSB and resets X to its minimum possible value again. This process is repeated until D_{CP} becomes zero for the first time. At this point, the DAC and b_{CD} and b_{CC} states are frozen. The calibration circuit is then shut down to save power. The flowchart and conceptual waveforms of the calibration loop are shown in Fig. 4.6 (a) and (b), respectively.

4.3.3 Peak Detector

The schematic of the peak detector is shown in Fig. 4.7 (a). A common-source buffer is used to isolate the oscillator from the detector's switching activities. The biasing resistor of the buffer (R_B) is implemented with a 10-kΩ

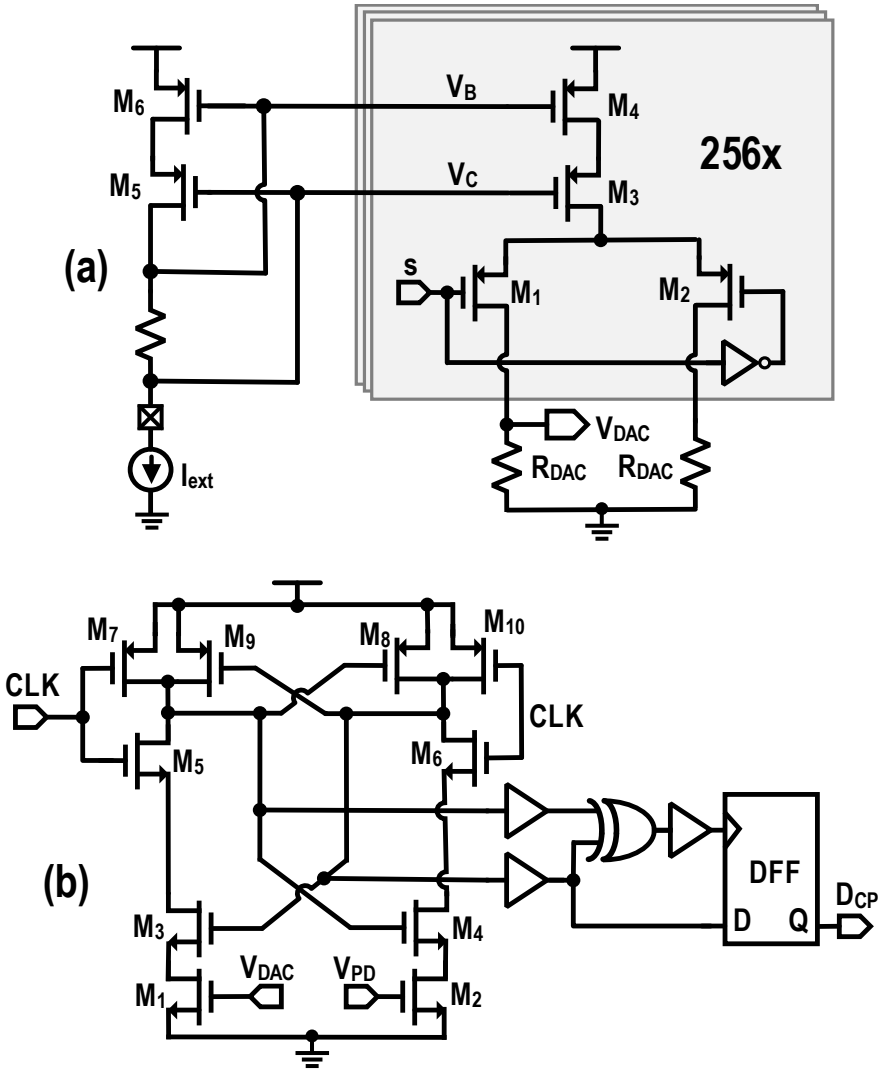

Figure 4.8: Schematics of the (a) DAC and (b) comparator.

unsilicided polysilicon[1] to minimize the tank's CM quality factor degradation. The biasing voltage V_B is derived from a current mirror[2]. The output of the buffer (V_{BUFF}) is then connected to the detector core, consisting of an NMOS transistor (M_2) and a capacitor (C_1) [147]. The voltage drop on the buffer load resistance (R_1) is designed to be about the threshold voltage of M_2. Hence, M_2 acts as a diode and only turns on in the negative half cycle of the buffer's output (V_{BUFF}). During this phase, M_2 ON-resistance and C_1 form a low-pass filter to extract the average value of V_{BUFF} negative cycle, leading to a peak detection gain of $\sim 1/\pi$. Since the fundamental tone of V_{BUFF} is at $2F_O$ ($\sim$10 GHz), M_2 and C_1 are sized to achieve a few hundreds of MHz corner frequency to provide enough attenuation for V_{BUFF} high-frequency

[1]The measured resistance of the unsilicided polysilicon is relatively immune to temperature.
[2]It is not shown in Fig. 4.7 (a).

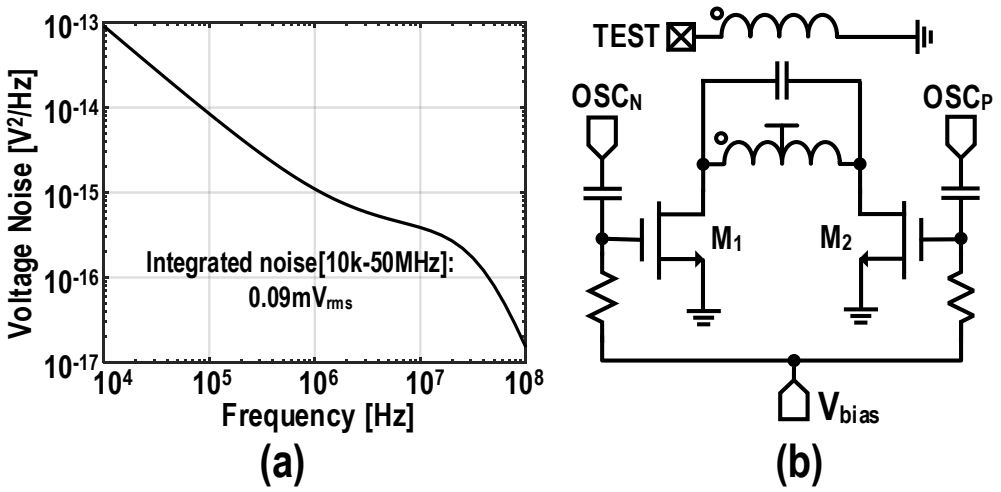

Figure 4.9: (a) Simulated noise of the calibration loop referred to the input of the peak detector at 300 K and (b) schematic of the test buffer.

components and to guarantee the loop settling within ∼20 ns, as shown in Fig.4.7 (b). Another amplifier (M_3 and R_2) further boosts the desired signal to relax the requirements on the DAC resolution and the comparator noise. K_{PD} of the entire peak detection block is ∼6.

4.3.4 DAC, Comparator, and VCO Buffer

Fig. 4.8 (a) shows the schematic of the voltage DAC, which consists of 256 unary cascode current sources with a unit current of 0.7 μA to satisfy the dynamic range, resolution, and speed requirements. The resistive components of the DAC (R_{DAC}) are implemented by unsilicided polysilicons as they are relatively immune to temperature variations. A constant-current biasing scheme is adopted to generate required bias voltages (V_B and V_C) for the cascode transistors, which circumvents the potential start-up issue at CT[1]. The linearity of the DAC is expected to become worse due to the higher mismatch of transistors at 4.2 K [113]. Nevertheless, the calibration results would not be affected provided that the DAC is monotonic, which is guaranteed by the unary structure. The simulated settling time of the DAC is within 10 ns at 300 K, and is expected to decrease at 4.2 K due to the reduction of the ground capacitance. The simulated RMS voltage noise is ∼200 μ V at 300 K, which is expected to decrease below 100 μV at CT.

Fig. 4.8 (b) shows the schematic of the voltage comparator, which comprises

[1]A constant-g_m biasing circuit was found to fail in start-up at 4.2 K.

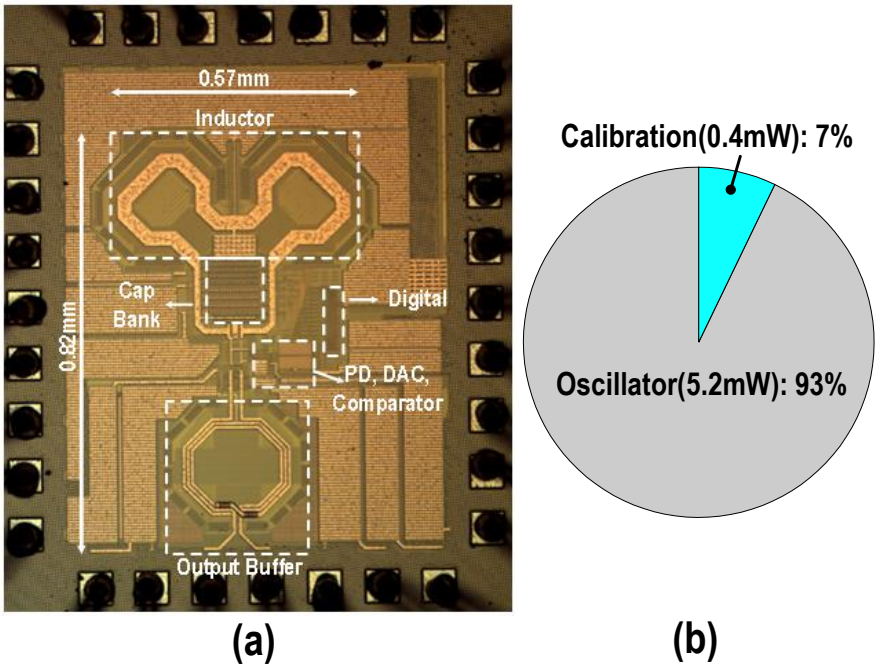

Figure 4.10: (a) Chip micrograph and (b) measured power breakdown at 4.2 K.

a StrongARM latch and a resampling stage. This topology is chosen to minimize the kickback noise as the input pairs ($M_{1,2}$) are clocked through the drain path rather than the source path [148]. The comparator's offset shifts the DAC control code at the optimum point, which consumes some dynamic range of the DAC. Nevertheless, it does not affect calibration results since the DAC is designed with a sufficient dynamic range. A resample stage is adopted to preserve compared results when the CLK is low, and to synchronize the comparator output with the digital clock. Fig. 4.9 (a) shows the simulated noise of the calibration loop referred to the input of the peak detector at 300 K. The integrated voltage noise is $\sim 90\,\mu V$, ensuring that the calibrated PN is within 1 dB of the optimum, as can be gathered from Fig. 4.3 (b).

Fig. 4.9 (b) shows the schematic of the VCO buffer, which is an AC-coupled common-source amplifier with a transformer load. The buffer is designed with a sufficiently large swing to drive the long cable of the cryogenic measurement setup and the instrument. The biasing resistor is implemented with unsilicided polysilicon ($\sim 30\,\mathrm{k}\Omega$) to avoid the reduction of the VCO's tank quality factor. Since the buffer consumes a high P_{DC}, it can increase the temperature of the VCO core, degrading PN. For example, at an ambient temperature of 4.2 K, the substrate heating was observed to be more than 50 K and 7 K, when respectively measured at distance of 0 μm and 15 μm from a heater dissipating

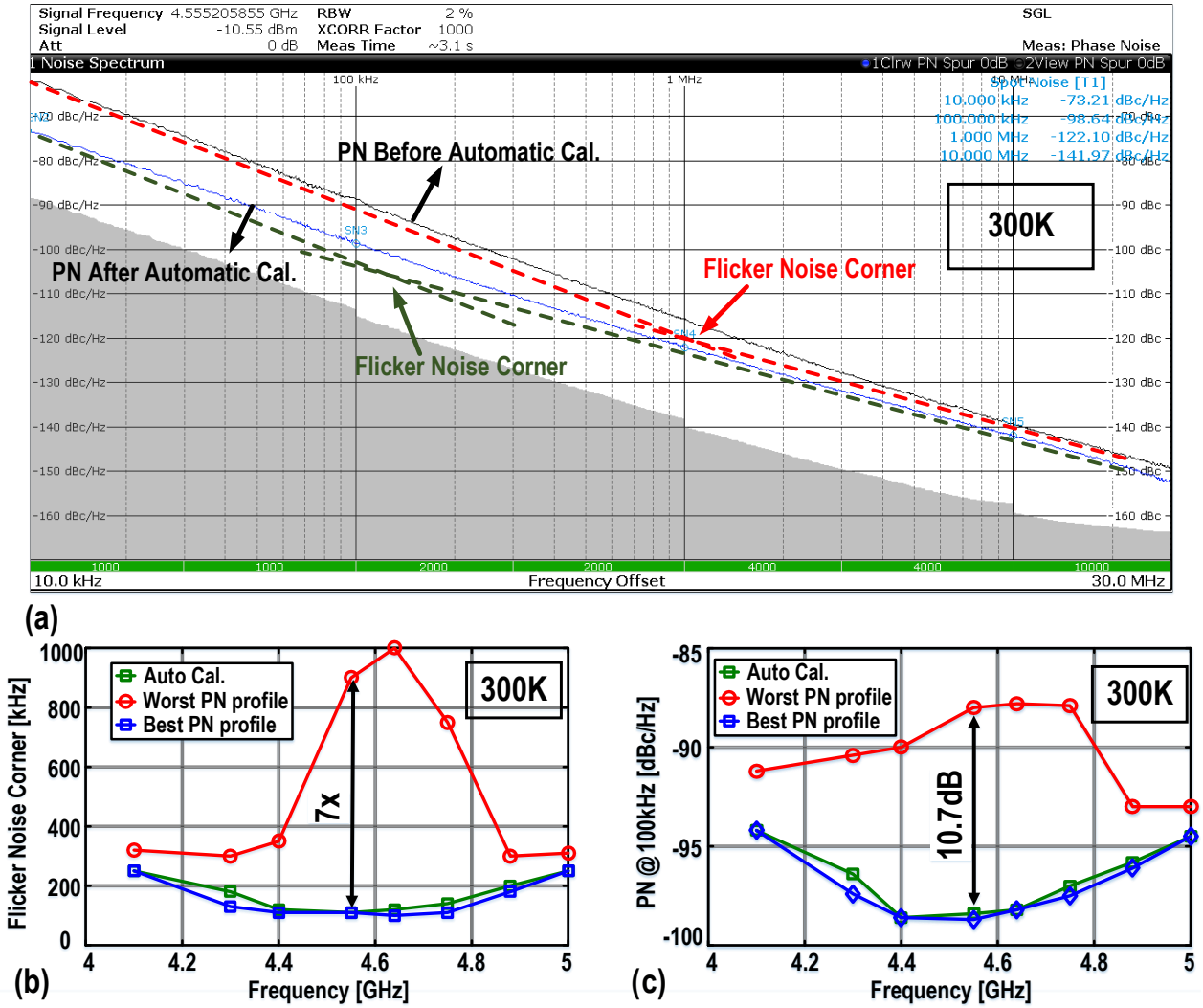

Figure 4.11: (a) Measured PN profiles before and after automatic calibration at 4.56 GHz; Measured (b) flicker noise corner and (c) PN at a 100 kHz offset over its tuning range for the worst, best, and calibrated at 300 K.

6.5 mW [113]. To mitigate this issue, the buffer is placed physically far away ($\sim 100\,\mu$m) from the VCO in the layout.

4.4 Measurement Results

The oscillator with the proposed CM resonance calibration technique is implemented in a standard 40-nm bulk CMOS process. Fig. 4.10 (a) and (b) respectively show the chip micrograph and measured power breakdown at 4.2 K. The core area of the chip is 0.15 mm^2, in which the calibration circuits occupy $\sim$0.01 mm^2. The oscillator has been wire-bonded on a printed circuit board (PCB) for room temperature and cryogenic measurements. To characterize its

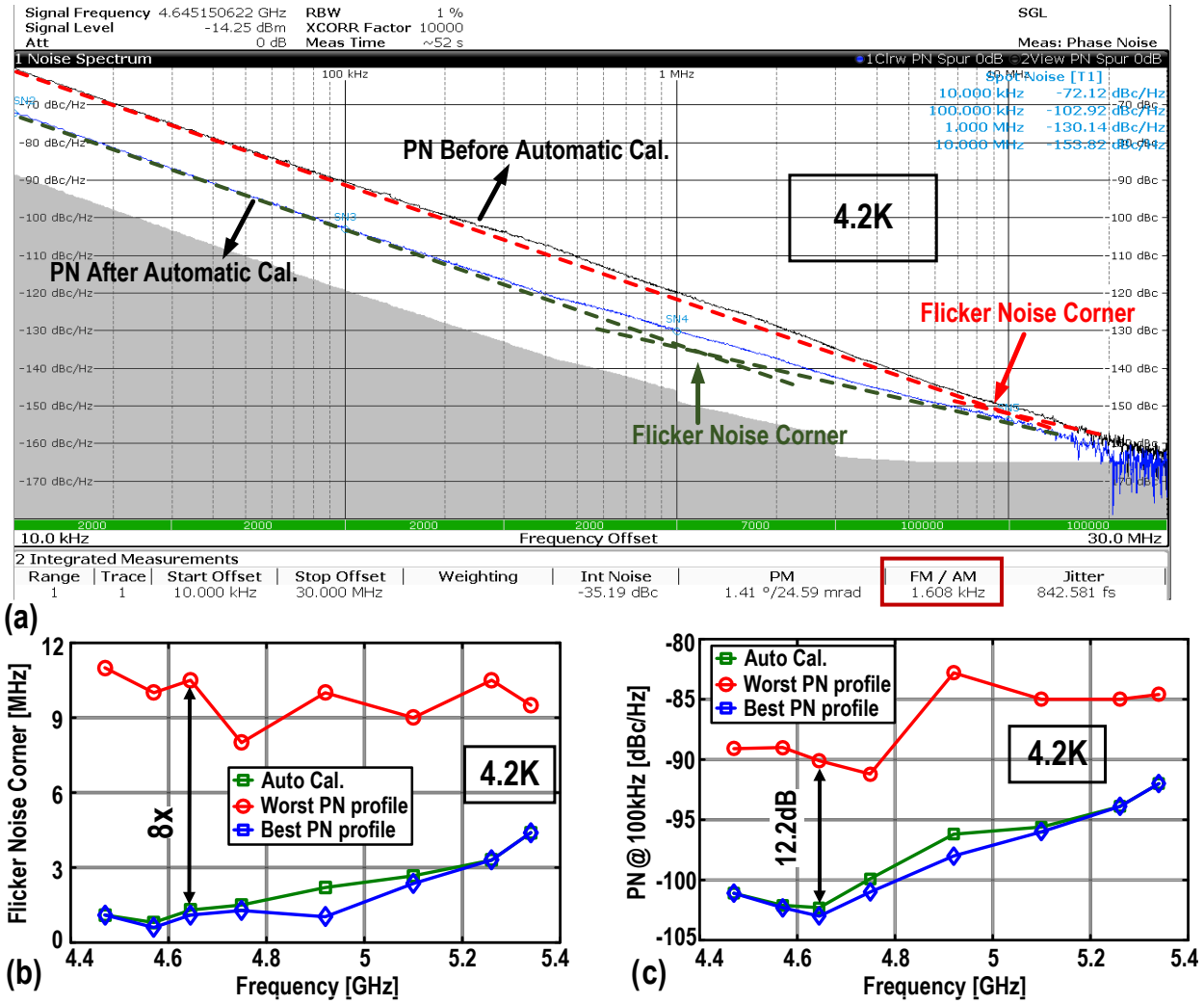

Figure 4.12: (a) Measured PN profiles before and after automatic calibration at 4.56 GHz; Measured (b) flicker noise corner and (c) PN at a 100 kHz offset over its tuning range for the worst, best, and calibrated at 4.2 K.

performance at 4.2 K, the PCB was mounted at one end of a dipstick, which immersed the oscillator sample into the liquid helium [48]. The oscillator's PN has been measured from an R&S FSWP8 phase noise measurement setup. A signal generator with a nominal frequency of 50-MHz is used to provide the clock for calibration. At 300 K, the oscillator consumes 4.3 mW from a 0.5-V supply. By cooling the chip to 4.2 K, it consumes 5.2 mW (excluding 0.4 mW of the calibration loop) from a 0.6-V supply. The oscillator can cover an output frequency range of 4.1–5 GHz and 4.4–5.3 GHz at 300 K and 4.2 K, respectively. The increased output frequency at 4.2 K is mainly due to the reduction of the parasitic ground capacitance to the substrate. The oscillator's frequency change is not a concern as the output frequency can be precisely set by a PLL.

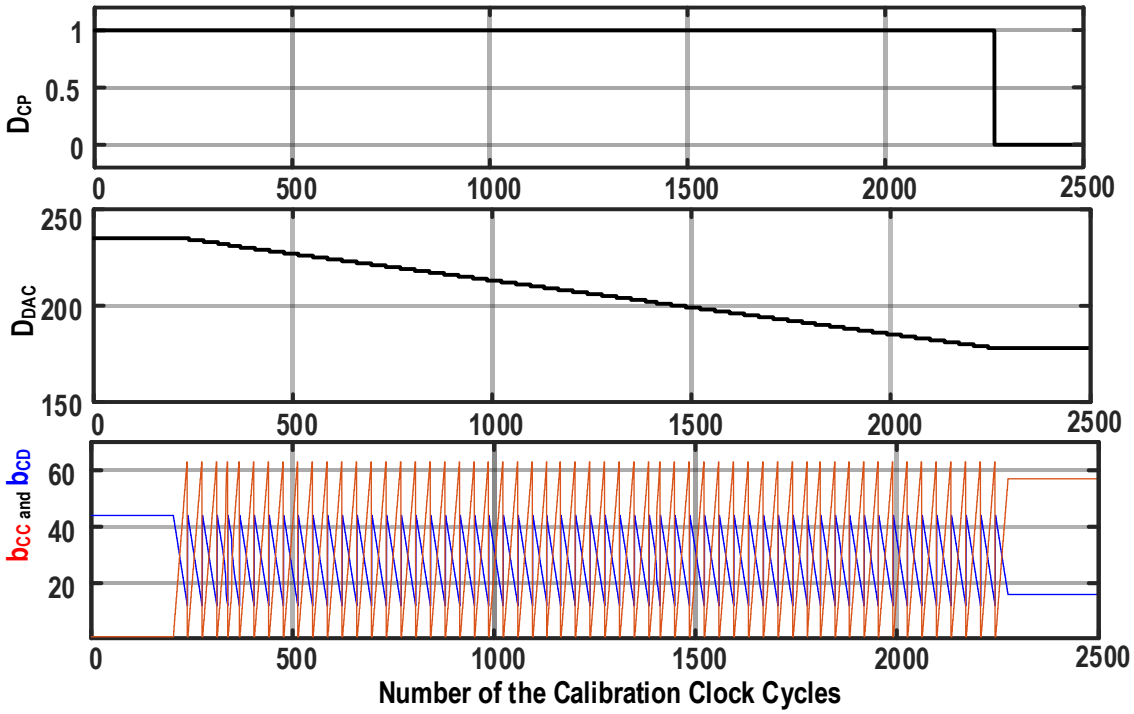

Figure 4.13: Measured settling behavior of the calibration loop at 4.2 K.

The oscillator's PN is measured over all possible b_{CC} and b_{CD} states while disabling the calibration to find the best and worst PN profiles over the tuning range at 300 K. The calibration loop is then activated to investigate the effectiveness of the proposed technique. Fig. 4.11 (a) shows the measured PN profiles before and after automatic calibration at 4.56 GHz. The calibration loop successfully finds the optimum b_{CC} and b_{CD} codes, suppressing the oscillator's PN from -87.9 dBc/Hz to -98.6 dBc/Hz at a 100 kHz offset. It also reduces the flicker PN corner from 1 MHz to 130 kHz at 300 K. Fig. 4.11 (b) and (c) respectively depict the measured flicker PN corner and PN at a 100 kHz offset of the oscillator over the tuning range. The calibrated results follow the optimum ones in most cases.

The oscillator's PN has been measured at 4.2 K as well. Fig. 4.12 (a) depicts the measured PN profiles before and after automatic calibration at 4.65 GHz. The calibration is capable of reducing the oscillator's PN from -90.7 dBc/Hz to -102.9 dBc/Hz at a 100 kHz offset. Moreover, Fig. 4.12 (b) and (c) respectively depict the measured flicker PN corner and PN at a 100 kHz offset of the oscillator over the tuning range, indicating the robustness of the calibration at 4.2 K. After the automatic CM resonance calibration, a PN of -153.8 dBc/Hz at a 10 MHz offset (i.e., β=0.041 Hz^2/Hz) and a flicker PN corner f_C of 1.3 MHz are achieved. This translates to an estimated fidelity of 99.999% for an f_R

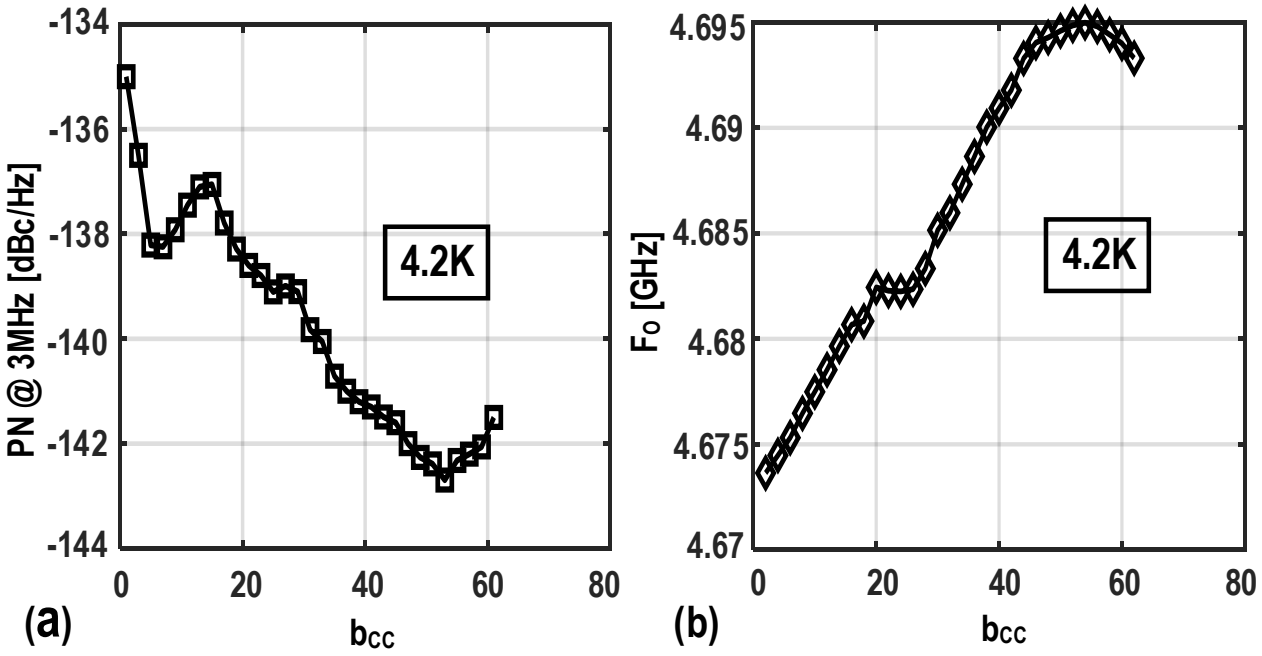

Figure 4.14: Measured (a) PN at a 3 MHz offset and (b) oscillator frequency by increasing b_{CC} by 2 LSBs and reducing b_{CD} by 1 LSB at 4.2 K.

higher than 0.25 MHz, thus satisfying the requirements of LO generation for quantum computing applications. Compared with 300 K, the normalized PN[1] reduction at a 100 kHz offset is $\sim$2 dB ($\sim$3.7 dB) before (after) the automatic calibration. Those results suggest that the absolute flicker noise of transistors is not a strong function of temperature. Moreover, the normalized PN reduction at a 10 MHz offset is $\sim$11 dB, which is in line with our analysis presented in Section 4.2.

Fig. 4.13 shows the measured settling of the calibration loop. For this measurement, instead of using the regular 50 MHz clock frequency, a very low-speed clock (0.5 kHz) is used for the calibration loop to allow monitoring of the comparator output D_{CP}, DAC code D_{DAC}, and b_{CC} and b_{CD} states during the calibration via an SPI link[2]. Initially, the DAC code voltage is too high and D_{CP} is 1. This results in b_{CC} being swept from its minimum to maximum and b_{CD} being swept from its maximum to minimum. Then, the DAC output code is gradually reduced by 1 LSB to search the maximum peak detector voltage V_{PD}. Once D_{CP} becomes 0 for the first time, the D_{DAC}, b_{CC}, and b_{CD} are frozen. The calibration loop successfully settles from an

[1]This normalization takes the power consumption into account for a fair comparison.

[2]In this chip, due to the speed limitation of the SPI link and long cables, we cannot directly monitor D_{CP}, D_{DAC}, b_{CC} and b_{CD} states during the calibration if the regular 50 MHz clock frequency is used.

initial setting ($b_{CC} = 1$, $b_{CD} = 44$) to the optimized b_{CC} and b_{CD} states within 2500 clock cycles. Consequently, the estimated calibration time is less than 50 μs during the nominal operation. Fig. 4.14 shows the measured oscillation frequency (F_O) and PN versus b_{CC} while sweeping X=C_C/C_D at 4.2 K. At each sweep step, b_{CC} is increased by 2 LSBs and b_{CD} is reduced by 1 LSB. In this way, F_O remains almost constant during the calibration. When this technique is employed in a PLL, F_O is first roughly adjusted by the coarse frequency selector, this calibration is then run to find the optimum X, and finally, the PLL locks to the desired frequency by using a tracking bank.

Table 4.2 compares the performance of the presented oscillator with the state-of-the-art. The achieved FOM of this work at RT is limited by the low supply voltage and by the lower tank's quality factor, due to the use of a smaller single-turn inductor and a larger capacitor bank [see Fig. 4.10]. However, our work is the only one offering automatic CM resonance calibration, while requiring a negligible area overhead ($\sim$0.01 mm^2).

Thanks to the calibration loop and the optimization of the inductor layout, this work achieves a 200-dB FOM in the thermal noise region at 4.2 K and meets the PN specification required for the control electronics of a scalable quantum computer. In addition, our cryo-CMOS oscillator reaches the performance of a recent SiGe HBT design in [65]. Moreover, it also shows more than 5-dB FOM improvement in the flicker noise region, compared with the cryogenic oscillator in [48, 51, 55]. The proposed technique will potentially enable the realization of cryogenic low-power, low-jitter frequency synthesizers required for the control of quantum computers.

4.5 Conclusion

A cryo-CMOS LC oscillator for the qubit control is presented. A new PN expression is derived by considering the shot-noise effect to explain the difference between the theoretical predictions and measurement results at CT. The implemented oscillator features an automatic CM resonance calibration technique to reduce its PN. At 4.2 K, the oscillator achieves -153.8-dBc/Hz PN at a 10 MHz offset and 1.3-MHz flicker PN corner, while consuming only 5.2 mW at 4.2 K. Such a performance is sufficient to achieve a fidelity of 99.999% for an f_R higher than 0.25 MHz, thus meeting the stringent requirements of a

qubit controller.

Table 4.2: Table of comparison with prior art.

	This Work		A. Ruffino ISSCC'2021	Y. Peng ISSCC'2022		J. Gong CICC'2021	B. Patra JSSC'2018	F. Pepe ISSCC'2015	A. Franceschin B. ISSCC'2015	J. Du JSSC'2015	K. Hoshino ISSCC'2018
Osc. Topology	NMOS CM Resonance Class-D/F_2		CMOS Push-Pull LC-Tank VCO	Hybrid Class B/C Mode-Switching VCO		CMOS Class-B VCO	NMOS CM Resonance Class-$F_{2,3}$	NMOS CM Resonance Class-$F_{2,3}$	NMOS Implicit CM Resonance	NMOS $2f_{LO}$ Tail Tuning	CMOS DM Resonance Inverse Class-F
Temperature [K]	300	4.2	4.2	295	3.5	4.2	4.2	300	300	300	300
Frequency [GHz]	4.73	4.65	12.7	15.3	15.9*	10.8	6.3	7	3.3	8.4	4.51
Supply Voltage [V]	0.5	0.6	NA	1.35	1.4	1.1	1	1	0.9	1.5	0.6
Tuning Range	4.1-5 (19.8%)	4.4-5.3 (18.6%)	NA	13.4~17.0 (23.7%)	13.9~18.1 (25.5%)	9.4-11.6 (21%)	5.8-7.3 (25%)	5.4-7 (25%)	2.85-3.37 (27.2%)	7.4-8.4 (12.7%)	3.49-4.51 (25.5%)
Power [mW]	4.3	5.3	4.38	3.55	3.08	1.7	12	10	6.8	20	1.14
PN [dBc/Hz] @100kHz/1MHz/ 10MHz	-99.0/ -122.4/ -143.0	-102.9/ -130.2/ -153.8	-87.4 -114.5 -136.2	-88.5*/ -112*/ -132.6*	-93.1*/ -119.9*/ -141.7*	-83 -113 -138	-94/ -120/ -149	-102.1/ -124.5/ -144.5	-106*/ -129.5*/ -150.2*	-88*/ -118*/ -146.8	-98.5/ -123.7*/ -143.7
FOM** [dB] @100kHz/1MHz/ 10MHz	186.2/ 189.6/ 190.2	189/ 196.3/ 200	183.1/ 190.2/ 191.2	186.1/ 189.9/ 190.3	191.3/ 198.7/ 201.1	183.7 193.7 196.4	179.2/ 185/ 194	188.9/ 191.4/ 191.4	188/ 191.5/ 192.2	173.5/ 183.5/ 192.3	191/ 196.2/ 196.2
Flicker Corner [kHz]	180	1300	800	55-145	165-497	4000	5700	130	200	600	300
Technology	40nm CMOS		40nm CMOS	130nm SiGe HBT		40nm CMOS	40nm CMOS	40nm CMOS	28nm CMOS	55nm CMOS	65nm CMOS
Oscillator Area [mm^2]	0.14		NA	0.05		0.1*	0.13	0.13	0.19	0.17	0.14
Calibration Area [mm^2]	0.01		NA	NA		NA	NA	NA	NA	NA	NA
Inductor	One Turn		2 Inductors	2 Inductors		One Turn	1:2 XFMR	1:2 XFMR	Two Turns	One turn+tail Ind.	2:4 XFMR
CM Resonance Cali.	Auto		NA	NA		NA	Manual	Manual	Manual	NA	Manual

*Estimated from the measured phase noise plot of the oscillator **FOM=$|PN(f)|+20\log10(F_O/f)-10\log10(P_{DC}/1mW)$

Chapter

5

A Low-Jitter and Low-Spur Charge-Sampling PLL

In the previous chapter, a low-phase-noise cryo-CMOS oscillator is introduced. Nevertheless, that oscillator can not be directly used as a local oscillator for quantum computing applications since its frequency suffers from drift over time. In this chapter, a complete PLL is presented, which is locked to a stable reference and operates reliably over a wide temperature range from 300 K to 4.2 K[1]. The goal of this chapter is to introduce a low-jitter, low-spur, and low-power phase-locked loop (PLL) for both conventional applications and emerging applications such as quantum computing.

A charge-domain sub-sampling phase detector (CSPD) is introduced to achieve a high phase-detection gain and to reduce the PLL in-band phase noise. Even without employing any power-hungry isolation buffers, the proposed CSPD dramatically suppresses the reference spurs by both minimizing the modulated capacitance seen by the VCO tank and by reducing the duty cycle of the sampling clock. A 50 μW RF-dividerless frequency-tracking loop is also introduced to lock the PLL robustly when the VCO faces a sudden

[1]This chapter has been published in the IEEE Journal of Solid-State Circuits [149].

frequency disturbance. Fabricated in a 40-nm CMOS process, the prototype PLL occupies a core area of 0.13 mm^2 and synthesizes 9.6-to-12 GHz tones using a 100 MHz reference. At 11.2 GHz, it achieves a reference spur of -77.3 dBc and an RMS jitter of 48.6 fs while consuming 5 mW. When the PLL operates at 4.2 K, it achieves 37.2 fs RMS jitter, 76.8 dBc reference spur and consumes 3 mW power.

5.1 Introduction

Phase-locked Loops (PLLs) with high spectral purity are in great demand for high-performance data converters, optical communication links, wireline, and wireless transceivers. In quantum computing applications, a cryogenic high-performance PLL is required for a qubit controller, as mentioned in Chapter 2. Consequently, it is desired that a single PLL can operate over a wide temperature range (e.g., from 300 K to 4.2 K) to target all those applications. However, this imposes stringent requirements on the PLL's power consumption (P_{DC}), phase noise (PN), RMS jitter, and reference spur (S_{REF}). In the last decade, significant effort has been made to improve PLLs' spectral purity and power-efficiency [17, 55, 77–80, 84, 85, 88–99, 101, 149–158].

A divider-less sub-sampling PLL (SSPLL) based on voltage sampling can achieve low jitter while dissipating low power, as it eliminates the noise of the feedback divider and suppresses the noise of the charge pump and phase detector (PD) thanks to its high phase-detection gain (K_{PD}) [88–97]. Unfortunately, the direct sampling of the voltage-controlled oscillator (VCO) voltage by a low-frequency reference clock (REF) can introduce a high S_{REF} due to the periodic tank-capacitance perturbation, reference clock feedthrough, and charge injection from the sampling switch to the VCO. The periodic switching of the sampling capacitor modulates the VCO's frequency, F_{VCO}, in a similar fashion to the case of binary frequency shift keying (BFSK), which creates a spur at the reference frequency (F_{REF}) given by

$$S_{REF-BFSK} = 20 \cdot \log_{10}\left[\sin(\pi \cdot D_{REF}) \cdot \frac{N}{2\pi} \cdot \frac{C_{MOD}}{C_{TANK}}\right], \tag{5.1}$$

where D_{REF} is the reference clock duty cycle, N is the PLL frequency multiplication factor, C_{MOD} is the modulated capacitance seen by the VCO tank, and C_{TANK} is the total tank capacitance [89]. S_{REF} can be improved by directly decreasing the sampling capacitor (C_S) [89] to reduce C_{MOD}. However, a small C_S degrades the in-band PN due to the sampling noise, diminishing the benefit of a sub-sampling PD. Hence, a dummy sampler was added in [93] such that the VCO could see a small C_{MOD}. Yet, this approach suffers from the mismatch between these two sampling capacitors, thus limiting S_{REF} to -56 dBc for a 2.2 GHz carrier.

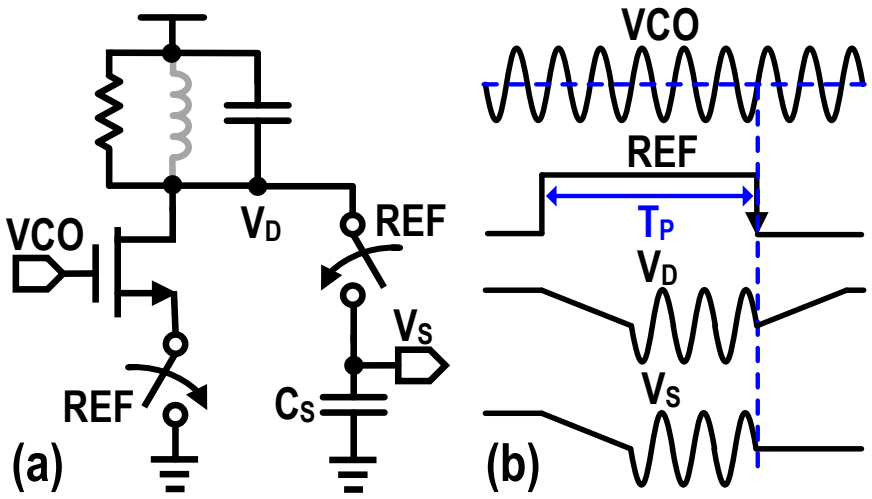

Figure 5.1: (a) Schematic and (b) conceptual waveforms of a voltage-sampling phase detector using a power-gated isolation buffer.

Consequently, to target a low S_{REF} (e.g., <-70 dBc) through lowering C_{MOD}, an isolation buffer with either inductive or resistive load is typically employed between VCO and sampler [89, 151]. However, the buffer operates at F_{VCO}, resulting in a substantial penalty in the PLL's area, P_{DC}, and jitter. Moreover, the rise and fall time of the signal at the sampler input may be reduced, shrinking the linear phase-detection range of the PD. Hence, a power-hungry slope generator is added in [89, 151] to realize a triangular-like waveform for the sampler.

Power-gated operation of the isolation buffer, as shown in Fig. 5.1 (a), reduces D_{REF}, thus alleviating S_{REF} and P_{DC} overhead [90, 91]. However, the REF pulse width (T_P) cannot be shorter than a few cycles (e.g., 5-10) of the VCO period (T_{VCO}) to ensure that the resonant buffer reaches its steady-state amplitude before the sampling instants. In the case of the resistive buffer, the common-mode (CM) settling time sets the shortest possible T_P, thus limiting S_{REF} and P_{DC} improvement. Moreover, to provide a low-noise signal amplification at F_{VCO}, the buffer's transistors must be wide enough to draw a relatively large current during the ON-state. Due to the use of wide transistors, the buffer's input capacitance significantly changes when the devices enter saturation from the cut-off region and vice versa. Therefore, the VCO experiences a large C_{MOD}, thus limiting the PLL spur performance. Besides, the clock feedthrough and charge injection issues still exist through the large gate parasitic capacitance of the isolation buffer. Consequently, due to the constraints on the minimum achievable C_{MOD} and D_{REF}, even by using

a gated isolation buffer in [91], the S_{REF} and FOM are still limited to -67 dBc and -256 dB at 2.4 GHz carrier frequency, respectively.

To improve on those limitations, we propose a charge-sampling PLL (CSPLL), firstly introduced in [150], whose phase-detection mechanism is based on a windowed current integration. Without exploiting any isolation buffers, the proposed CSPLL achieves -77 dBc S_{REF} by simultaneously minimizing C_{MOD} and D_{REF}. It also offers a high K_{PD} even without requiring an RF bandwidth at the sampler output, resulting in -259 dB jitter-power FOM. Furthermore, a highly-digital frequency-tracking loop (FTL) without the use of any RF dividers is proposed to guarantee PLL's robust operation.

This chapter is organized as follows. Section 5.2 focuses on the detailed theoretical analysis and design considerations of the charge-sampling phase detector. Section 5.3 describes the complete CSPLL architecture and FTL operation. The circuit implementation of critical building blocks of the CSPLL is shown in Section 4.3. Section 4.4 presents measurement results, while Section 4.5 wraps up the chapter with conclusions.

5.2 Charge-Sampling Phase Detector

5.2.1 Voltage Sampling versus Charge Sampling

Voltage-sampling phase detectors (VSPD) capture the instantaneous input voltage when the sampling switch is turned OFF [see Fig. 5.1 (b)]. Their ideal locking point is when the VCO zero-crossings occur at the REF falling edge [88]. The VSPD phase-detection gain is directly proportional to the voltage swing at the sampler's output, thus demanding a high power consumption for both the isolation buffer and the sampling circuit for realizing an RF bandwidth close to F_{VCO}. On the other hand, charge sampling is based on *integrating* an input current on a capacitor over a fixed time window and taking the resulting voltage as the sampler output. It is a well-known technique to reduce the sampling error caused by the clock jitter in high-speed sample-and-hold amplifiers [159, 160]. It is also widely used in software-defined radio receivers due to its built-in anti-aliasing and reconfigurability [161–164]. However, the interesting properties of the charge-sampling concept have not yet been exploited in PLL design. This paper shows that the fundamental differences in the voltage sampling and charge sampling operation profoundly impact the

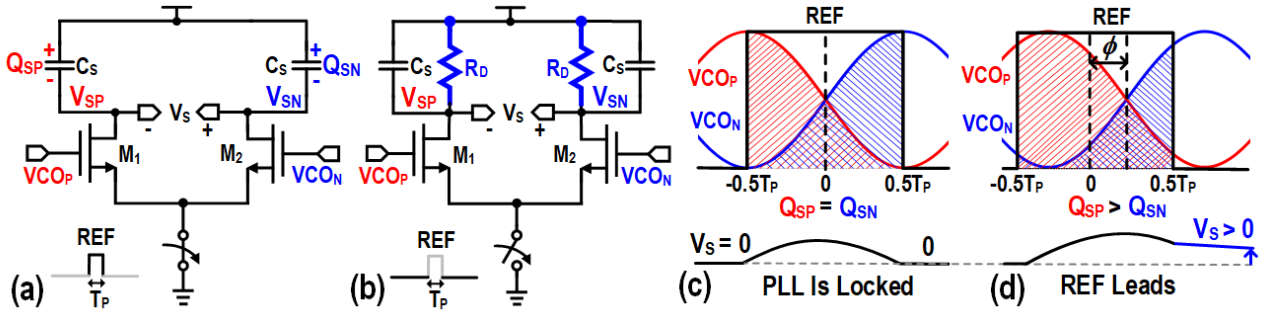

Figure 5.2: Simplified schematic of the proposed CSPD when REF is (a) high and (b) low; its conceptual waveforms (c) without and (d) with a phase error.

PLL performance in terms of locking point, K_{PD}, S_{REF}, PN, and P_{DC}.

5.2.2 Locking Point

Fig. 5.2 shows the schematic and conceptual waveforms of a charge-sampling phase detector (CSPD). The transconductors ($M_{1,2}$) convert the VCO's output voltage VCO_P-$VCO_N = 2A_{VCO}\cdot\sin(\omega_{VCO}t+\phi)$ into a differential RF current, realizing a charge difference on C_S when REF is high. If the VCO zero-crossings occur at the center of the REF pulse, $M_{1,2}$ charge C_S during the first half of the REF pulse (i.e., from -0.5 T_P to 0), and discharge C_S during the second half of the REF pulse (i.e., from 0 to 0.5 T_P). Consequently, the sampled net charge difference $Q_S = (Q_{SP}$-$Q_{SN})$ is zero, which is represented by the equaled shaded blue and red areas in Fig. 5.2 (c). Hence, the sampled differential voltage V_S (=V_{SN}-V_{SP}) remains zero after the phase comparison, corresponding to the ideal locking condition of the PLL. If there is any phase error (ϕ), the CSPD converts it into a non-zero Q_S and V_S, as shown in Fig. 5.2 (d), thus indicating that the PLL is not locked. Consequently, similarly as in sub-sampling PDs, the CSPD works without using RF dividers if $N=F_{VCO}/F_{REF}$ is an integer number.

When REF is low, V_S is *partially* discharged via load resistors (R_D) and C_S since $M_{1,2}$ are turned OFF. This peculiar discharging process is crucial for the CSPD's operation, which will be discussed in the following subsection.

5.2.3 Phase-Detection Gain

Fig. 5.3 shows the time-domain differential-mode model of the CSPD, where a periodic sampling function (p(t)) samples a continuous-time RF current $I(t) = G_M A_{VCO}\sin(\omega_{VCO}t + \phi)$. This results in a train of discrete-time narrow

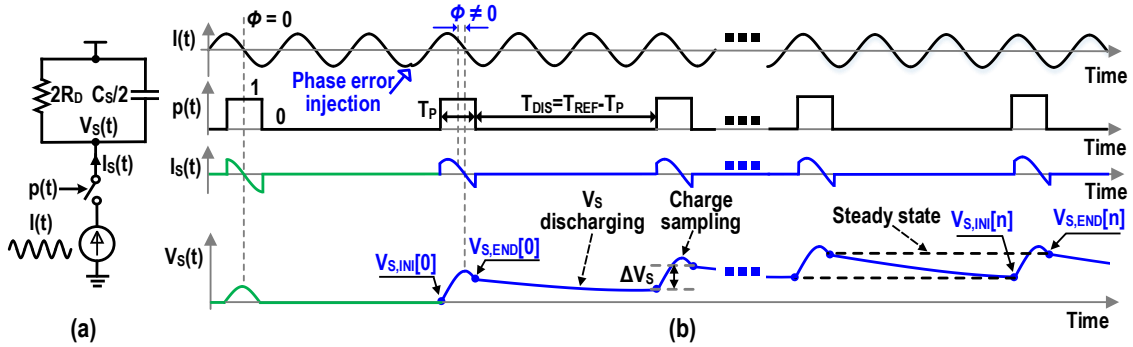

Figure 5.3: (a) Time-domain differential-mode model of the CSPD; (b) waveforms of the CSPD before and after applying a phase error to the VCO.

current pulses

$$I_S(t) = G_M A_{VCO} \sin(\omega_{VCO} t + \phi) \cdot p(t), \tag{5.2}$$

where G_M is the large-signal transconductance of $M_{1,2}$, and

$$p(t) = \begin{cases} 1, & \dfrac{-T_P}{2} + n \cdot T_{REF} \le t \le \dfrac{T_P}{2} + n \cdot T_{REF} \\ 0, & \text{otherwise.} \end{cases} \tag{5.3}$$

Due to the phase error (ϕ) between the VCO zero-crossings and middle of the REF pulse [see Fig. 5.3 (b)], V_S increases by[1]

$$\begin{aligned} \Delta V_S &= V_{S,END}[n] - V_{S,INI}[n] = \frac{2}{C_S} \int_{-0.5T_P}^{0.5T_P} I_S(t) dt \\ &= \frac{4 G_M A_{VCO}}{\omega_{VCO} C_S} \cdot \sin(0.5 \omega_{VCO} T_P) \cdot \sin(\phi) \end{aligned} \tag{5.4}$$

during each phase comparison, where $V_{S,INI}[n]$ and $V_{S,END}[n]$ represent the voltages of V_S at the beginning and end of the charge sampling, respectively, at the n^{th} reference clock cycle. Following the phase comparison, p(t) becomes 0 for a duration of T_{DIS}=T_{REF}-T_P. $V_{S,END}[n]$ is exponentially discharged through R_D and C_S, and brings $V_{S,INI}$ to

$$V_{S,INI}[n+1] = V_{S,END}[n] \cdot \exp^{-k} \tag{5.5}$$

[1]Here, we assume $1/(C_S \omega_{VCO}) \ll R_D$. And it will be shown later that this assumption is valid for a CSPD.

at the next cycle, where k is defined as $T_{DIS}/(R_D C_S)$. By combining Eqs (5.4) and (5.5), $V_{S,END}[n]$ can be calculated as

$$V_{S,END}[n] = \Delta V_S \sum_{k=0}^{n-1} \exp^{-n \cdot k}, \tag{5.6}$$

and it reaches a steady-state value given by $V_{S,END}[n]|_{st} = \Delta V_S/(1 - \exp^{-k})$.

The unique discharging process of V_S is critical for the proper operation of a CSPD. Let us consider two extreme cases here. In the first one, k approaches 0 by removing R_D. Therefore, the sampled charge is accumulated, and CSPD resembles an ideal integrator, exhibiting a pole at DC and causing instability issues in the PLL. In the second case, if k is chosen to be $\sim$N by picking a small R_D and C_S, which is a typical case in a VSPD using a power-gated isolation buffer [90, 91], the detected V_S will rapidly return to zero, thus destroying the PD's memory and requiring a hold switch at the sampler output. In this design, k is designed to be $\sim$0.4, so as to satisfy the PLL's required phase margin and simultaneously guarantee the PD's charge-sampling operation. As a result, CSPD resembles a leaky phase integrator with a pole location determined by k. We will discuss this further in Section 5.3.

In the steady-state, V_S becomes a periodic function of T_{REF}, and its average value can be estimated by[1] K_{PD} is then defined as $\overline{V_S}/\phi$ and can be calculated by

$$K_{PD} = \frac{2 G_M A_{VCO} R_D}{N\pi} \cdot \sin(0.5\omega_{VCO} T_P) \cdot \frac{\sin(\phi)}{\phi}. \tag{5.7}$$

We can inspect the validity of the above equation by using an alternative method. The phase error modifies the shape of the sampled current pulses [see Fig. 5.3 (b)], and creates a non-zero DC current ($\overline{I_S}$). Notice that $\overline{I_S}$ must flow into the resistive load R_D, thus creating a DC voltage given by

$$\begin{aligned} \overline{V_S} &= \frac{2R_D}{T_{REF}} \cdot \int_{-0.5T_P}^{T_{REF}-0.5T_P} G_M A_{VCO} \sin(\omega t + \phi) dt \\ &= \frac{2 G_M A_{VCO} R_D}{N\pi} \cdot \sin(0.5\omega_{VCO} T_P) \cdot \sin(\phi). \end{aligned} \tag{5.8}$$

Interestingly, K_{PD} is not a function of C_S. This indicates that an arbitrarily large C_S can be used without sacrificing K_{PD}. The complete phase-detection

[1] This approximation is valid since $T_P \ll T_{DIS}$ in a CSPD.

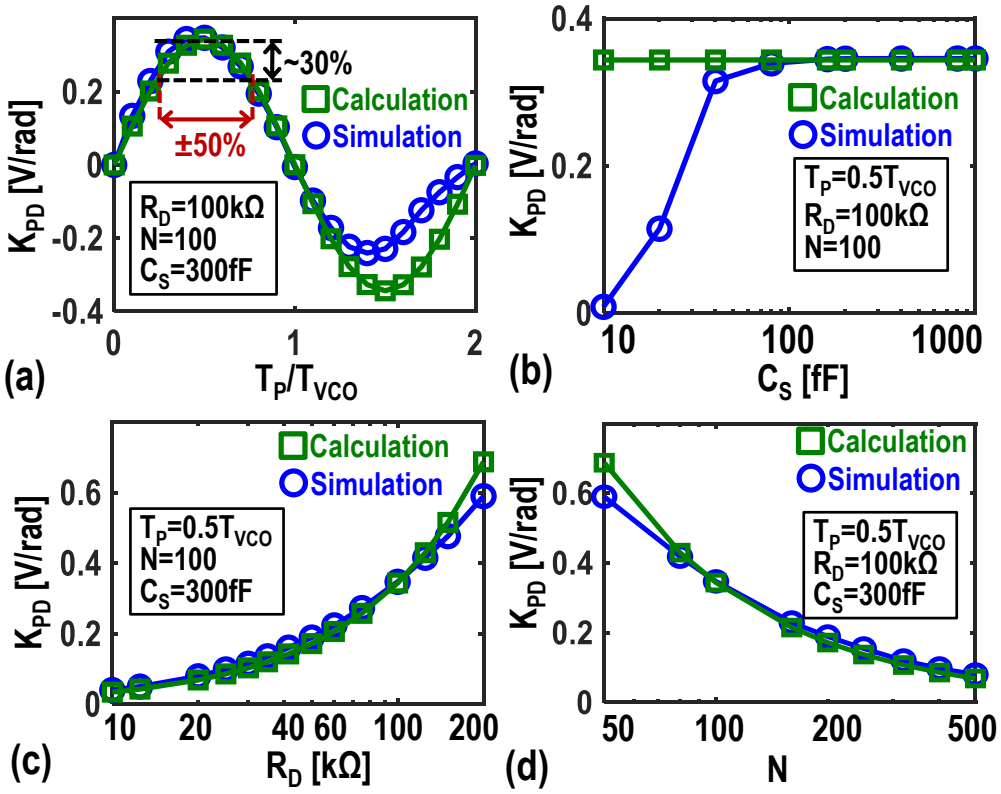

Figure 5.4: Simulated and calculated K_{PD} as a function of (a) T_p, (b) C_S, (c) R_D, and (d) N.

gain by considering the PD delay can be estimated by $K_{PD}(s) \approx K_{PD}/(1 + s \cdot R_D C_S)$.

Notice that, unlike a VSPD, K_{PD} of a CSPD is a function of both T_P and N. At first glance, it seems that the K_{PD} of a CSPD with the $N\pi$ factor in the denominator is much smaller than that of a VSPD (i.e., $K_{PDVS} \approx 2G_M A_{VCO} R_D$). However, the reduction of K_{PD} by $N\pi$ can be easily compensated by choosing a large R_D. Note that the finite output impedance of $M_{1,2}$ (r_{ds}) has a marginal impact on K_{PD}, as long as $1/(\omega_{VCO} C_S) \ll r_{ds}$. This condition can be easily satisfied in a CSPD by choosing a large C_S. Hence, without compromising K_{PD}, a minimum channel length device can be used for $M_{1,2}$ to minimize C_{MOD} and to improve S_{REF}. In contrast to the CSPD, r_{ds} significantly reduces K_{PDVS} in deep-submicron technologies due to short-channel effects, enforcing the use of long channel length devices, and thus degrading S_{REF}.

Due to the integration operation, K_{PD} is a periodic function of T_P, and reaches its maximum at T_P=0.5 T_{VCO}. Using $T_P \gg 0.5\, T_{VCO}$ does not improve K_{PD} but degrades the reference spur. Notice that, due to the sinusoidal dependency of K_{PD} to T_P, a ±50% variation of T_P around its optimum point only reduces K_{PD} by 30%, suggesting that CSPD is robust against PVT variations.

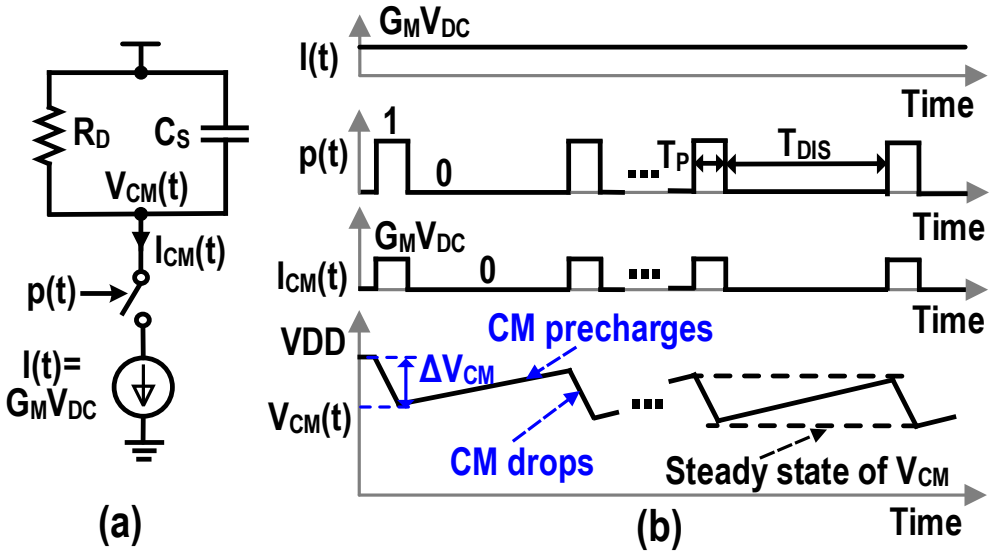

Figure 5.5: (a) Time-domain common-mode model of the CSPD; (b) common-mode waveforms of the CSPD.

In this design, a K_{PD} of $\sim$0.35 V/rad is achieved by choosing $R_D = 100\,k\Omega$, $(W/L)_{1,2} = 2\,\mu m/40\,nm$, $G_M = 1.2\,mS$, and $N = 100$. Note that the achieved gain is sufficiently high to suppress the noise of PLL loop components. Further increasing K_{PD} would require a pulser circuit to reduce the loop gain [88], complicating the design. Fig. 5.4 shows the simulated and calculated K_{PD} versus various parameters of the CSPD. Although there are some deviations especially if a large T_P and a small C_S are used, simulations match the presented theory very well. The discrepancies will be justified in the next subsection by investigating the CM behavior of the CSPD.

5.2.4 Common-Mode Settling

Fig. 5.5 shows the time-domain CM model and waveforms of the CSPD, where the sampling function p(t) is used to sample a constant current. Consequently, a train of current pulses with a fixed amplitude of $G_M V_{DC}$ and a duration of T_P is pumped into the R_D and C_S irrespective of the phase error, where V_{DC} is $M_{1,2}$ gate-source bias voltage. This results in a CM voltage drop of $\Delta V_{CM} = G_M V_{DC} T_P / C_S$ when p(t) is 1 (i.e., during the phase comparison). When p(t) is 0, the output CM voltage (V_{CM}) is exponentially precharged to a high level such that $M_{1,2}$ can be turned on very fast (i.e., <15 ps), only limited by the on-resistance and parasitic capacitance of the tail switch. Note that CSPD CM settles to its steady-state right after the power-up and follows

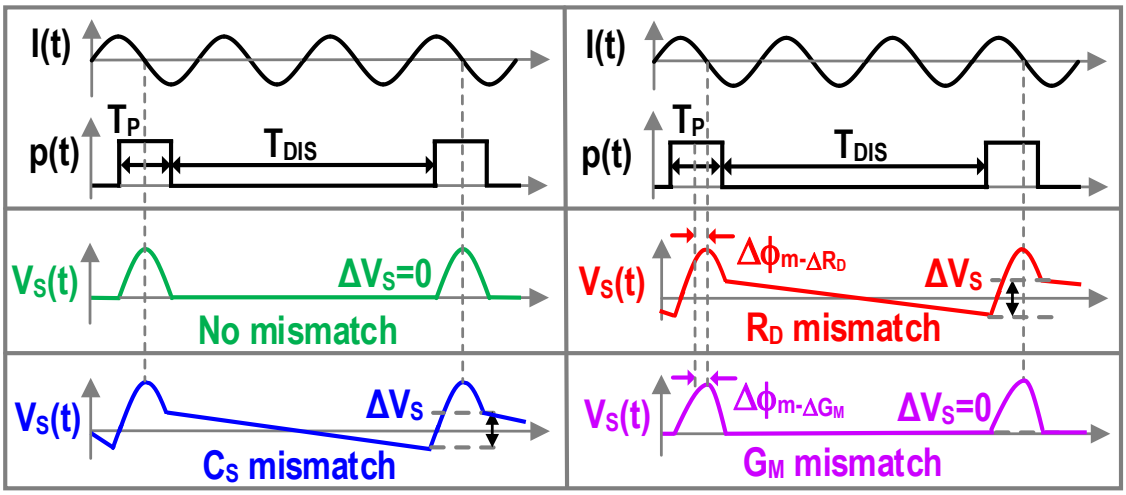

Figure 5.6: Conceptual waveforms of the CSPD due to C_S, R_D, and transistor mismatch.

the same pattern regardless of the phase error variations.

K_{PD} could be potentially compromised if $M_{1,2}$ enter the triode region, as shown in Fig. 5.4 (a) and (b), where the simulated K_{PD} deviates from its theoretical value if a larger T_P or a smaller C_S is used. Therefore, a large C_S and very narrow pulse width for the REF *must* be utilized to maintain a high output CM voltage and keep $M_{1,2}$ in saturation during each phase comparison[1]. The current consumption of the CSPD is obtained by averaging the CM current over one reference period,

$$\overline{I_{CM}} = \frac{2}{T_{REF}} \int_{-\frac{T_P}{2}}^{T_{REF}-\frac{T_P}{2}} G_M V_{DC} dt = \frac{2 G_M V_{DC} T_P}{T_{REF}}. \tag{5.9}$$

By considering $V_{DC} = 0.6\,V$, $(W/L)_{1,2} = 2\,\mu m/40\,nm$, and $T_P = 0.3 T_{VCO}$, the CSPD consumes less than $5\,\mu A$. Consequently, a low power consumption, and a high K_{PD} can be simultaneously achieved by having a small T_P (e.g., $0.3\,T_{VCO}$) in the proposed CSPD. On the contrary, to deliver a maximum voltage gain, a VSPD needs a large T_P for proper CM settling of its gated isolation buffer, thus degrading both power consumption and S_{REF}.

[1]Interestingly, in contrast to a VSPD, a proper CSPD design always favors a small T_P and a large C_S.

5.2.5 Mismatch Analysis

5.2.5.1 C_S Mismatch

As discussed earlier, since the averaged differential output of CSPD ($\overline{V_S}$) is not a function of C_S, the locking point and K_{PD} are also not sensitive to the mismatch between the sampling capacitors (ΔC_S). However, due to ΔC_S, even when the phase error is zero, the CSPD's differential output in steady-state experiences a voltage jump (ΔV_S) during each phase comparison followed by an exponential voltage change over the discharging phase [see the blue curve in Fig. 5.6]. This results in a sawtooth ripple in V_S, whose fundamental amplitude is given by

$$A_{rip-\Delta C_S} \approx \frac{\Delta C_S}{C_S} \cdot \frac{\Delta V_{CM}}{\pi}. \tag{5.10}$$

The effect of this sawtooth-like ripple on the reference spur will be discussed further in Section 5.3.

5.2.5.2 R_D Mismatch

If the VCO zero-crossings occur at the center of the REF pulse, then a non-zero $\overline{V_S}$ ($= G_M V_{DC} \Delta R_D T_P / T_{REF}$) will be created due to the mismatch between the CSPD load resistors (ΔR_D), indicating that the PLL is not locked. The loop must therefore develop a phase offset of

$$\Delta\phi_{m-\Delta R_D} \approx \frac{\Delta R_D}{R_D} \cdot \frac{N\pi T_P}{2\sin(0.5\omega_{VCO} T_P) T_{REF}}, \tag{5.11}$$

to compensate for ΔR_D and realize $\overline{V_S} = 0$ in the locked state. Even considering a pessimistic $\Delta R_D / R_D = 10\%$, $\Delta\phi_{m-\Delta R_D}$ would be $< 4^\circ$ with almost no penalty on K_{PD}. Nevertheless, due to this offset, a sawtooth ripple will show up in V_S again [see the red curve in Fig. 5.6], whose fundamental amplitude can be found by

$$A_{rip-\Delta R_D} \approx 4 G_M A_{VCO} \cdot \sin(\Delta\phi_{m-\Delta R_D}) \cdot \frac{\sin(0.5\omega_{VCO} T_P)}{\pi \omega_{VCO} C_S}. \tag{5.12}$$

The impact of this ripple on S_{REF} will be quantified in Section 5.3.

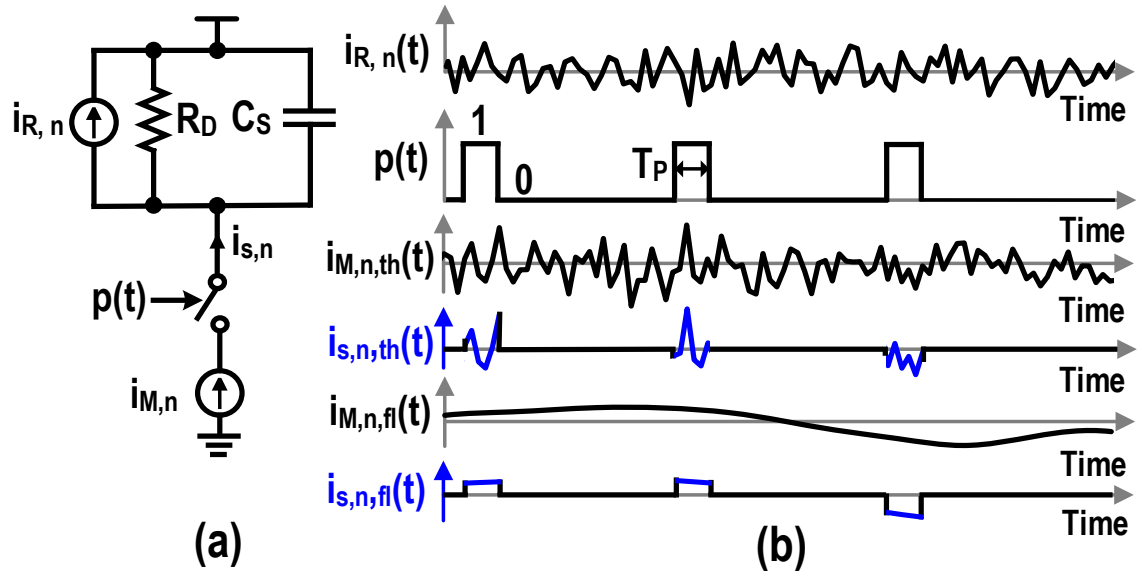

Figure 5.7: (a) Half-circuit noise model and (b) time-domain noise waveforms of the CSPD.

5.2.5.3 $M_{1,2}$ Mismatch

Similar to R_D mismatch, the loop must create a phase offset to compensate for the mismatch between the transconductance of the transistors (ΔG_M), as shown in Fig. 5.6. The phase offset can be estimated by

$$\Delta\phi_{m-\Delta G_M} \approx \frac{\Delta G_M}{G_M} \cdot \frac{N\pi T_P}{2\sin(0.5\omega_{VCO}T_P)T_{REF}}. \tag{5.13}$$

By considering $\Delta G_M/G_M = 50\%$, $\Delta\phi_{m-\Delta G_M}$ is $\sim$16.9°, degrading K_{PD} by only $\sim$0.4 dB. Fortunately, since C_S and R_D are matched, there is no sawtooth ripple in V_S at the steady-state [see the pink curve in Fig. 5.6]; hence S_{REF} is not affected by ΔG_M.

5.2.6 Phase-Noise Analysis

5.2.6.1 Noise of R_D

Since R_D is always connected to the CSPD output, the effective power spectral density (PSD) of its noise current can be simply expressed as $\overline{i^2_{s,R,n}}/\Delta f = 4KT/R_D$. Note that this expression slightly overestimates R_D noise when transferred to the CSPD output, as its noise current partially flows to the ground due to the finite r_{ds} of $M_{1,2}$.

5.2.6.2 Thermal Noise of $M_{1,2}$

As shown in Fig. 5.7, $M_{1,2}$ contribute noise only when the REF is high by injecting a train of narrow noise-current pulses ($i_{s,n}(t) = i_{M,n}(t) \cdot p(t)$) into R_D and C_S. Suppose that $i_{M,n}(t)$ contains only thermal noise ($i_{M,n,th}(t)$) with a variance of $i^2_{M,n,th}$. The resulting $i_{s,n}(t)$ is a white and cyclostationary process, and its auto-correlation function can be expressed as

$$R_{i_{s,n}}(t, t+\tau) = i^2_{M,n,th} \cdot \delta(\tau) \cdot p(t+\tau) \cdot p(t), \tag{5.14}$$

which is a function of both t and the lag τ. The $i_{s,n}(t)$ PSD is obtained by averaging $R_{i_{s,n}}(t, t+\tau)$ over one reference period and taking the Fourier transformation; and it is given by

$$\frac{\overline{i^2_{s,n,th}}}{\Delta f} = \int_{-\infty}^{+\infty} \exp^{-j2\pi f\tau} \int_{-\frac{T_P}{2}}^{T_{REF}-\frac{T_P}{2}} \frac{R_{i_{s,n}}(t, t+\tau)}{T_{REF}} dt d\tau = i^2_{M,n,th} \cdot \frac{T_P}{T_{REF}}. \tag{5.15}$$

As expected, a smaller T_P also reduces $M_{1,2}$ contribution to the PLL total PN.

5.2.6.3 Flicker Noise of $M_{1,2}$

Since the flicker noise of $M_{1,2}$ ($i_{M,n,fl}(t)$) is a slow process, and varies little during the charge-sampling window, it can be assumed that its time average determines the root mean square of the flicker fluctuations [165]. Consequently, the output flicker noise current can be modeled as an impulse train with a height of $T_P/T_{REF} \cdot i_{M,n,fl}(t)$ sampled at the reference frequency.

$$i_{s,n,fl}(t) = \frac{T_P}{T_{REF}} \cdot \sum_{k=0}^{n} \left(i_{M,n,fl}(t) \cdot \delta(t - k \cdot T_{REF}) \right). \tag{5.16}$$

Its PSD at low frequencies can be estimated by

$$\frac{\overline{i^2_{s,n,fl}}}{\Delta f} = \frac{T_P^2}{T_{REF}^2} \cdot \frac{\overline{i^2_{M,n,fl}}}{\Delta f}, \tag{5.17}$$

where $\overline{i^2_{M,n,fl}}/\Delta f$ is the power spectral density of $M_{1,2}$ flicker noise. Note that the spectrum of the flicker noise current at the CSPD output consists of sampled replicas appearing at integer multiples of F_{REF}, which are sufficiently suppressed by the large time constant of $R_D C_S$.

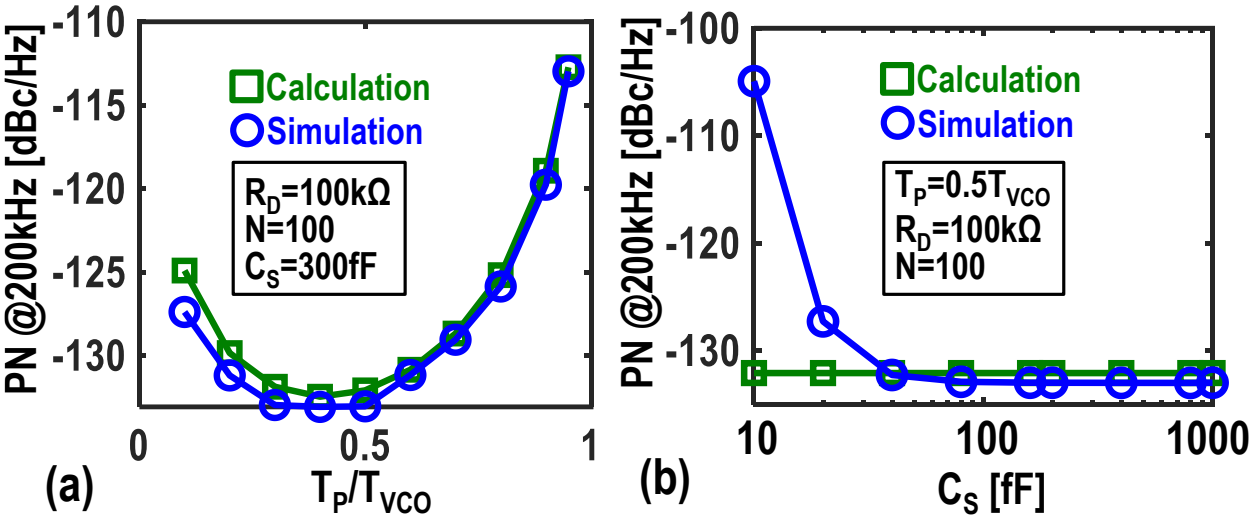

Figure 5.8: Simulated and calculated PN at 200 kHz offset from a 10 GHz carrier as a function of (a) T_P and (b) C_S due to CSPD only.

5.2.6.4 In-band PN due to CSPD

The in-band phase noise is obtained by considering the noise contributions of R_D, and $M_{1,2}$ at the CSPD output, and referring the resulting voltage noise to the input of CSPD.

$$\mathcal{L}_{\text{CSPD}} = 2 \cdot \left(\frac{\overline{i^2_{\text{s,R,n}}}}{\Delta f} + \frac{\overline{i^2_{\text{s,n,th}}}}{\Delta f} + \frac{\overline{i^2_{\text{s,n,fl}}}}{\Delta f}\right) \cdot \frac{R_D^2}{K_{PD}^2}. \tag{5.18}$$

Notice that, in contrast to a VSPD, the theoretical phase noise of a CSPD is not a function of C_S. Fig. 5.8 depicts the simulated and calculated in-band PN at 200 kHz offset from a 10 GHz carrier due to both the flicker and thermal noise of CSPD (but excluding any other noise sources) when R_D=100 kΩ and $(W/L)_{1,2}$=2 μm/40 nm. The simulation results are in good agreement with the presented calculations if C_S is not chosen too small, which is anyway outside the optimum range. If a very small C_S is used, the simulated PN is much higher than the theoretical value due to the reduced K_{PD} caused by V_{CM} drop. However, if a larger C_S is used, the simulated in-band PN is very weakly related to C_S, as expected. This is very different from a VSPD, where a large C_S is essential to reduce the KT/C noise.

As shown in Fig. 5.8 (a), the CSPD displays a minimum in-band PN (<-133 dBc/Hz) when T_P reaches ~0.5 T_{VCO}.While $M_{1,2}$ flicker noise corner is very high (i.e., ~60 MHz) due to their small dimensions, the charge-sampling suppresses the flicker noise much more than the thermal counterpart [compare

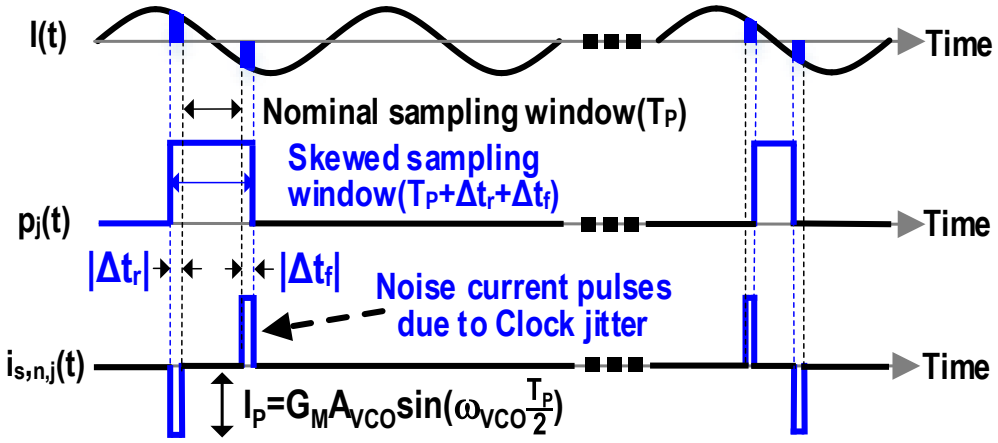

Figure 5.9: Sampling error due to the REF jitter.

(5.15) with (5.17)]. As a result, the R_D thermal noise, the $M_{1,2}$ thermal noise, and the $M_{1,2}$ flicker noise contribute almost equally to the total PN at 200 kHz offset. A larger T_P degrades both the K_{PD} and voltage noise contributed by $M_{1,2}$, worsening the in-band PN. Although a smaller T_P reduces the PN originated from the flicker noise of $M_{1,2}$, it degrades in-band PN due to the reduced K_{PD}. Nevertheless, choosing a T_P between $0.2\,T_{VCO}$ and $0.6\,T_{VCO}$ maintains the PN within 3 dB of the optimum performance.

5.2.6.5 PN due to Clock Jitter

The jitter of the reference clock alters the moment when $M_{1,2}$ are both turned ON and OFF, thus randomly changing the sampling function ($p_j(t)$), as shown in Fig. 5.9. The resultant sampling error ($i_{s,n,j}(t)$) contains two noise current pulses with a fixed amplitude of $I_P = G_M A_{VCO} \sin(\omega_{VCO} \frac{T_P}{2})$ and variable widths of $|\Delta t_r|$ and $|\Delta t_f|$ over one reference period, where Δt_r and Δt_f are the clock jitter of the REF rising edge and falling edge, respectively. Since Δt_r and Δt_f are very small, $i_{s,n,j}(t)$ can be represented as the sum of two impulse trains sampling at the reference frequency,

$$i_{s,n,j}(t) = \sum_{k=0}^{n} \frac{I_P \cdot \Delta t_r[k]}{T_{REF}} \cdot \delta\left(t - (\frac{-T_P}{2} + k \cdot T_{REF})\right) + \sum_{k=0}^{n} \frac{I_P \cdot \Delta t_f[k]}{T_{REF}} \cdot \delta\left(t - (\frac{T_P}{2} + k \cdot T_{REF})\right). \quad (5.19)$$

If Δt_r and Δt_f are *uncorrelated* but with the same variance, $i_{s,n,j}(t)$ power spectral density can be estimated by

$$\frac{\overline{i_{s,n,j}^2}}{\Delta f} = \frac{{I_P}^2}{T_{REF}^2}\left(\mathrm{psd}(\Delta t_r) + \mathrm{psd}(\Delta t_f)\right) = \frac{I_P^2}{2\pi^2}\cdot\mathcal{L}_j(f), \tag{5.20}$$

where $\mathcal{L}_j(f)$ is the PN at the rising edge and falling edge of the reference clock. The in-band PN of the PLL due to the uncorrelated jitter can be derived as

$$\mathcal{L}_{pll,j}(f) = \frac{\overline{i_{s,n,j}^2}}{\Delta f}\cdot\frac{(2R_D)^2}{K_{PD}^2} = \frac{N^2}{2}\mathcal{L}_j(f). \tag{5.21}$$

Consequently, in a CSPD, the *uncorrelated* noise of the rising and falling edges of REF is only multiplied by $N^2/2$ when transferred to the PLL output, alleviating the noise requirement of the pulse generator. On the contrary, this noise is still multiplied by N^2 for a VSPD in [90, 91]. However, similar to a VSPD, the *correlated* noise generated by the off-chip crystal and on-chip reference buffer is still multiplied by N^2 when transferred to the PLL output.

5.3 Charge-Sampling Phase-Locked Loop

Fig. 5.10 (a) shows the block diagram of the proposed type-II charge-sampling PLL (CSPLL) with a frequency-tracking loop (FTL) operating in the background. A reference buffer and a pulse generator are used to generate a narrow pulse signal (REF) from an off-chip sine reference. The CSPD converts the phase error between the VCO and REF into a differential voltage, V_S. A fully differential V/I stage then rejects the CM ripples on the CSPD output and converts its desired differential-mode signal into a current, which is further filtered by the loop filter (composed of R, C, and C_1) to generate a fine-tuning voltage V_P ($=V_{P+}$-V_{P-}) for the VCO. Note that there is no isolation buffer between the VCO and CSPD so as to verify the inherent low-spur performance of the CSPD. There is still a need for a VCO buffer in a practical system to drive the corresponding load (e.g., an IF mixer or a divider). If the CSPD is driven by the VCO buffer, even a lower reference spur could be obtained. However, this results in poor isolation between the CSPD and IF mixer or divider, leading to unpredictable noise coupling.

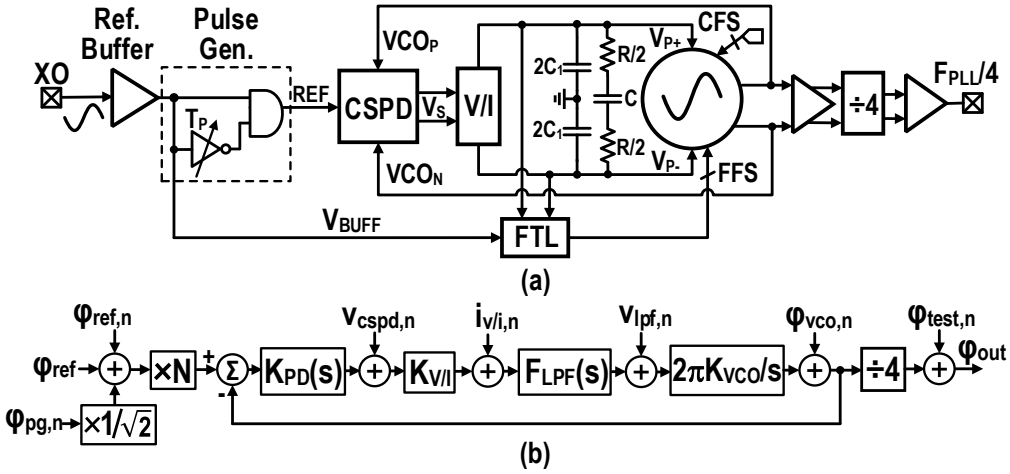

Figure 5.10: (a) Block diagram of the proposed CSPLL with an RF-dividerless FTL; (b) linear phase-domain model of the CSPLL.

5.3.1 Phase-Domain Model

Fig. 5.10 (b) illustrates the linear phase-domain model for the proposed CSPLL, where $K_{V/I}$ is the transconductance of the V/I stage, and $F_{LPF}(s)$ represents the transfer function of the loop filter. This model is accurate as long as the PLL bandwidth is much smaller than F_{REF}. Like an SSPLL, there is no divide-by-N in the feedback path, and a virtual frequency multiplier "$\times$N" is added to the reference path due to the sub-sampling process. However, a factor of $1/\sqrt{2}$ is used for the pulse generator noise to capture the charge-sampling process, as discussed in Section 5.2. The closed-loop transfer function of the CSPLL can be found as

$$H_{cl}(s) = \frac{H_{ol}(s)}{1 + H_{ol}(s)}, \tag{5.22}$$

where $H_{ol}(s)$ is the open-loop transfer function and can be expressed as

$$\begin{aligned} H_{ol}(s) &= K_{PD}(s) \cdot K_{V/I} \cdot F_{LPF}(s) \cdot \frac{2ßK_{VCO}}{s} \\ &= \frac{2ß \cdot K_{PD}}{1 + s \cdot R_D C_S} \cdot K_{V/I} \cdot (R + \frac{1}{s \cdot C}) || \frac{1}{s \cdot C_1} \cdot \frac{K_{VCO}}{s}. \end{aligned} \tag{5.23}$$

Here, we ignored the sinc-type low-pass filtering response of $K_{PD}(s)$ introduced by the windowed current integration since T_P is very small compared to T_{REF}.

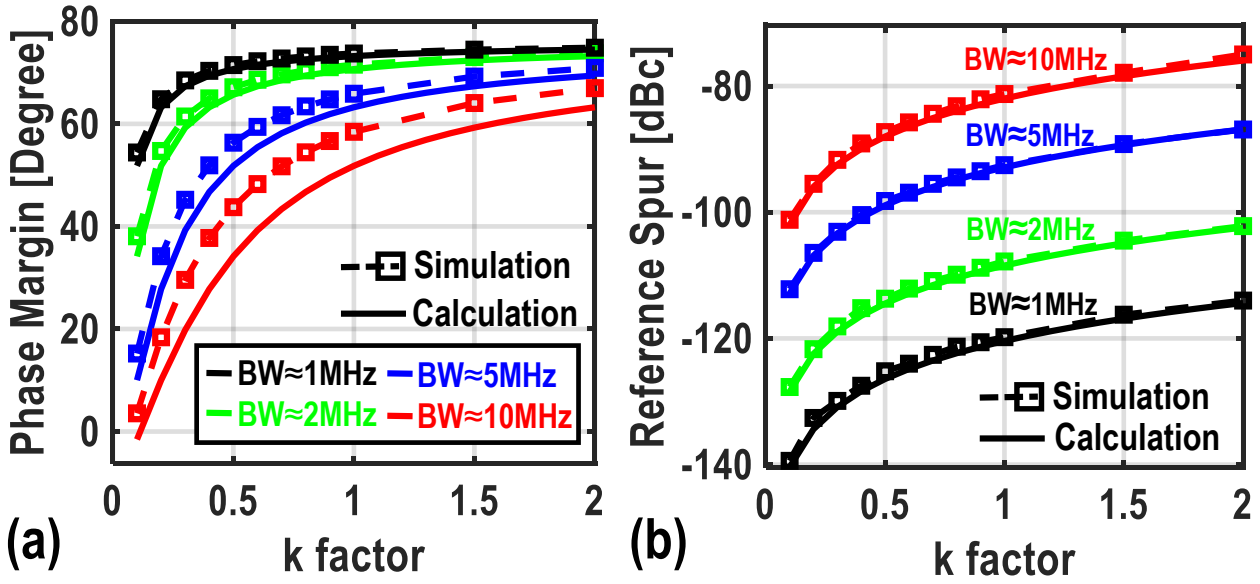

Figure 5.11: Simulated and calculated (a) phase margin and (b) reference spur due to differential-mode ripple versus the k factor.

5.3.1.1 Phase Margin Analysis

By considering the presented phase-domain model, the phase margin of CSPLL can be estimated as

$$\mathrm{PM} \approx \tan^{-1}(\omega_u \mathrm{RC}) - \tan^{-1}(\omega_u \mathrm{RC_1}) - \tan^{-1}(\omega_u \mathrm{R_D C_S}), \tag{5.24}$$

where ω_u is the frequency in which $|\mathrm{H_{ol}(s)}| = 1$. Since $\mathrm{k} \approx \mathrm{T_{REF}}/(\mathrm{R_D C_S})$, we can rearrange this equation as

$$\mathrm{PM} \approx \tan^{-1}(\omega_u \mathrm{RC}) - \tan^{-1}(\omega_u \mathrm{RC_1}) - \tan^{-1}\left(\frac{\omega_u \mathrm{T_{REF}}}{\mathrm{k}}\right). \tag{5.25}$$

Note that there is also a delay between the CSPD differential output and VCO waveforms due to the current integration. Nevertheless, the resulting phase delay is ignored in the phase margin calculations as it is $< \tan^{-1}(2\pi \mathrm{F_{REF}} \mathrm{T_P}/2) \approx 0.1^\circ$ in a realistic design. Due to the extra pole introduced by CSPD, $\mathrm{C_1}$ should be much smaller than that in a conventional loop filter ($\sim 0.015\times$C in this design) to minimize PM degradation. By ignoring the pole introduced by CSPD ($-1/\mathrm{R_D C_S}$), we can approximate ω_u as

$$\omega_u \approx \omega_n \cdot \sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}}, \tag{5.26}$$

where ω_n ($=\sqrt{K_{PD}K_{V/I}K_{VCO}/C}$) and ζ ($=0.5RC\omega_n$) are the natural frequency and the damping factor, respectively. Given a certain damping factor and PLL bandwidth (BW)[1], one can calculate C, and R to find the phase margin. Fig. 5.11 (a) shows the simulated and calculated phase margin versus k factor for various BW settings with $\zeta = 1.5$, where the discrepancy at high BW is due to the neglected pole of CSPD in estimating ω_u. A large k factor improves the system phase margin, especially for large PLL bandwidths. However, to ensure a proper charge-sampling operation without sacrificing K_{PD}, the k factor must be smaller than 2. By choosing k factor between 0.4 and 2, PM varies between 51.9° and 70.9° for a bandwidth of 5 MHz.

5.3.2 Spur due to Charge Sampling

In this subsection, the reference spur due to CSPD's non-idealities will be discussed and quantified.

5.3.2.1 Spur due to BFSK Effect

Due to the windowed current integration, the CSPD can operate with a small T_P. In addition, the transconductors ($M_{1,2}$) of CSPD can be sized very small without sacrificing in-band PN due to the CSPD's high K_{PD} and short T_P. Those lead to a substantial spur reduction due to the BFSK effect as predicted by (5.1). Based on design parameters (i.e., $C_{MODE} \approx 0.3\,fF$, $D_{REF} = 0.003$, and $C_{TANK} = 650\,fF$), $S_{REF-BFSK}$ is -83 dBc, where C_{MOD} is mainly originated from the gate-source capacitance (C_{gs}) variation of $M_{1,2}$ due to the REF switching.

Apart from the spur due to the BFSK effect, unlike a conventional SSPLL in [89], a CSPLL contains other spur mechanisms which disturb the VCO through its tuning voltage. In other words, there is a trade-off between the maximum bandwidth and minimal reference spur level. Nevertheless, it will be shown in the following subsection that the spur level due to those mechanisms is much lower than $S_{REF-BFSK}$.

5.3.2.2 Spur due to Differential-Mode Ripple

Unfortunately, as can be gathered from Fig. 5.3 (b), the differential output of CSPD (V_S) experiences a ripple with a worst-case peak value of

[1]BW can be estimated by $\sqrt{2\zeta^2+1+\sqrt{(2\zeta^2+1)^2+1}}\cdot\omega_n/(2\pi)$.

$2G_M A_{VCO}/(\omega_{VCO} C_S)$ during each phase comparison even if the PLL is locked. This ripple is first attenuated by the loop filter, then upconverted to spurious tones around the carrier. However, since C_S does not affect K_{PD}, the V_S ripple can be easily suppressed by increasing C_S as long as the PLL phase margin is satisfied. Therefore, the output voltage swing of the CSPD can be very small (i.e., <100 mV) in the lock state, which is also beneficial to reduce the spur due to the charge kickback.

The fundamental component of this differential ripple at F_{REF} can be estimated as $A_{drip} \approx 4G_M A_{VCO}/(N\pi\omega_{VCO} C_S)$. The resulting spur level can be estimated by

$$S_{REF-drip} \approx 20 \cdot \log_{10}\left(\frac{A_{drip} \cdot K_{V/I} R K_{VCO}}{2F_{REF}\sqrt{1+(2\pi F_{REF} R C_1)^2}}\right). \tag{5.27}$$

Based on the expression of A_{drip}, K_{PD}, and k, $S_{REF-drip}$ can be rearranged as

$$S_{REF-drip} \approx 20 \cdot \log_{10}\left(\frac{k \cdot K_{PD} K_{V/I} R K_{VCO}}{\omega_{VCO}\sqrt{1+(2\pi F_{REF} R C_1)^2}}\right). \tag{5.28}$$

Fig. 5.11 (b) shows the simulated and calculated spur level due to the differential-mode ripple versus the k factor for various BW settings. By choosing $k = 0.4$, the resulting spur level is below -100.4 dBc for a 5 MHz BW, which is marginal compared with the spur due to BFSK effect.

5.3.2.3 Spur due to Common-Mode Ripple

In addition, the output of CSPD also contains a common-mode (CM) ripple [see Fig. 5.5], with a very large amplitude of $\sim\Delta V_{CM}/\pi$ at F_{REF}. Firstly, this ripple can be converted to a differential one by the V/I, and results in a spur level estimated by

$$S_{REF-crip1} \approx 20 \cdot \log_{10}\left(\frac{G_M V_{DC} T_P}{C_S \pi} \cdot A_{CM-DM} \cdot \frac{K_{VCO}}{2F_{REF}}\right), \tag{5.29}$$

where A_{CM-DM} is the common-mode-to-differential-mode gain of the V/I at F_{REF}. Secondly, the CM ripple is attenuated by the V/I, and then appears at the input of the VCO. It will also introduce a spur due to the finite CM

rejection of VCO. The resulting spur level can be estimated as

$$S_{REF-crip2} \approx 20 \cdot \log_{10}\left(\frac{G_M V_{DC} T_P}{C_S \pi} \cdot \frac{A_{CM}}{CMR} \cdot \frac{K_{VCO}}{2F_{REF}}\right), \tag{5.30}$$

where A_{CM} is the common-mode gain of the V/I, and CMR is the common-mode rejection ratio of the VCO. By considering $K_{VCO} = 50\,\text{MHz/V}$, T_P=30 ps, and $C_S = 250\,\text{fF}$ (or $k = 0.4$), A_{CM-DM} and A_{CM}/CMR must be below -47 dB so as to suppress $S_{REF-crip1,2}$ below $-90\,\text{dBc}$, which can be satisfied by a proper design.

5.3.2.4 Spur due to C_S and R_D Mismatch

As discussed in section 5.2, the mismatch of C_S and R_D also creates a differential ripple at the CSPD output [see Fig. 5.6]. The resulting spur level can be estimated by

$$S_{REF-ms} \approx 20 \cdot \log_{10}\left(\frac{A_{rip-ms} \cdot K_{V/I} R K_{VCO}}{2F_{REF}\sqrt{1 + (2\pi F_{REF} R C_1)^2}}\right). \tag{5.31}$$

A_{rip-ms} is the ripple amplitude due to mismatch (i.e., $A_{rip-\Delta C_S}$ or $A_{rip-\Delta R_D}$). By considering a moderate C_S or R_D matching (e.g., $\Delta C_S/C_S = \Delta R_D/R_D = 1\%$), the resulting spur level is below -105 dBc for a 5 MHz BW.

5.3.3 Frequency Locking

Like a VSPD, the CSPD also has a limited lock-in range and one cannot distinguish between the desired N^{th} harmonic and other harmonics of F_{REF}. To avoid locking to a wrong harmonic, [88–93, 97] employed an RF divider-based FTL to bring the VCO frequency within the SSPLL's lock-in range. In the locked condition, the same FTL is also used to correct the frequency error (F_{ERR}) introduced by the sudden frequency disturbance on the VCO. However, when the PLL is locked, the maximum F_{ERR} due to voltage and temperature variations or power leakage from other chip components is in the order of tens of MHz[1]. Consequently, it is not wise to use a full range FTL as its high-frequency divider consumes substantial power consumption. We address

[1]The measured VCO frequency of this work is within ±27 MHz over a VCO supply variation of 100 mV and a temperature variation of 160°C.

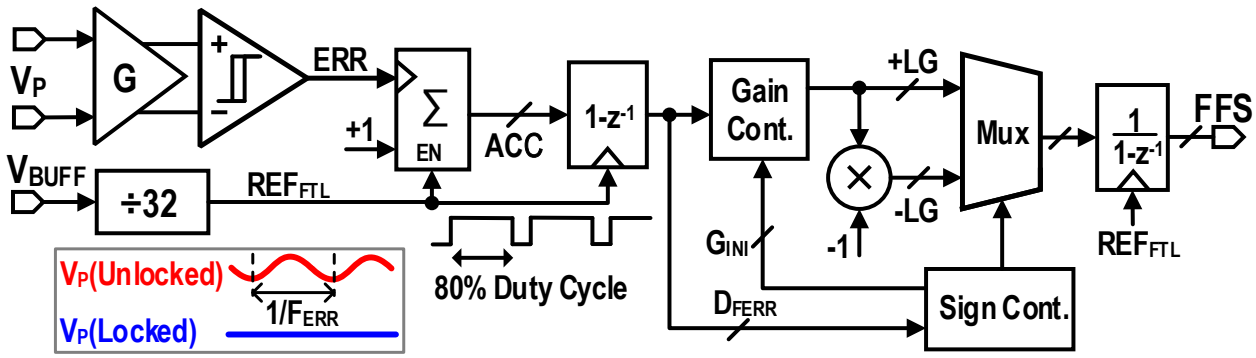

Figure 5.12: Block diagram of the frequency-tracking loop.

this issue by introducing a power-efficient FTL that does not rely on any power-hungry RF dividers and can be implemented chiefly by digital blocks, as can be gathered from Fig. 5.12.

Due to the removal of the RF divider, the lock-in range of the proposed FTL is limited to $\pm 0.5 F_{REF}$ (e.g., ± 50 MHz). Hence, the VCO's frequency must be initially calibrated within $\pm 0.5 F_{REF}$ of the desired frequency. This is done offline by adjusting the coarse switchable capacitor at power ON. In a future design, a conventional FTL as in [88–93, 97] can be used to automatically tune the VCO frequency. Once F_{ERR} is within $\pm 0.5 F_{REF}$, our proposed FTL takes over and the RF divider-based FTL is shut down to save power consumption.

Now suppose that the VCO experiences a frequency disturbance during the CSPLL's nominal operation. If F_{ERR} is within the lock-in range (e.g., $\sim$5 MHz), it can be corrected by the CSPLL. However, if F_{ERR} exceeds the lock-in range, it causes a lock failure of the CSPLL. An aliasing signal with an amplitude of $\sim$20-to-40 mV and an F_{ERR} of $|N \times F_{REF} - F_{VCO}|$ will appear at the CSPD output [166, 167]. Instead of using the divided RF clock, the proposed FTL relies on this aliasing signal to initiate the feedback and calculate the frequency error. An amplifier and a Schmitt trigger are employed to convert this aliasing signal to a digital bitstream (ERR). A ÷32 frequency divider generates the FTL master clock (REF_{FTL}) from the reference. To ensure that the following digital logics are synchronized with REF_{FTL}, the number of ERR rising edges is firstly accumulated only when the REF_{FTL} is high. Then a differentiator clocked by REF_{FTL} is used to obtain the digital representation of the frequency error (D_{FERR}). As a result, the ratio of REF_{FTL} frequency to its duty cycle determines the minimum detectable F_{ERR}, which must be smaller than CSPLL lock-in range to ensure a seamless frequency locking operation.

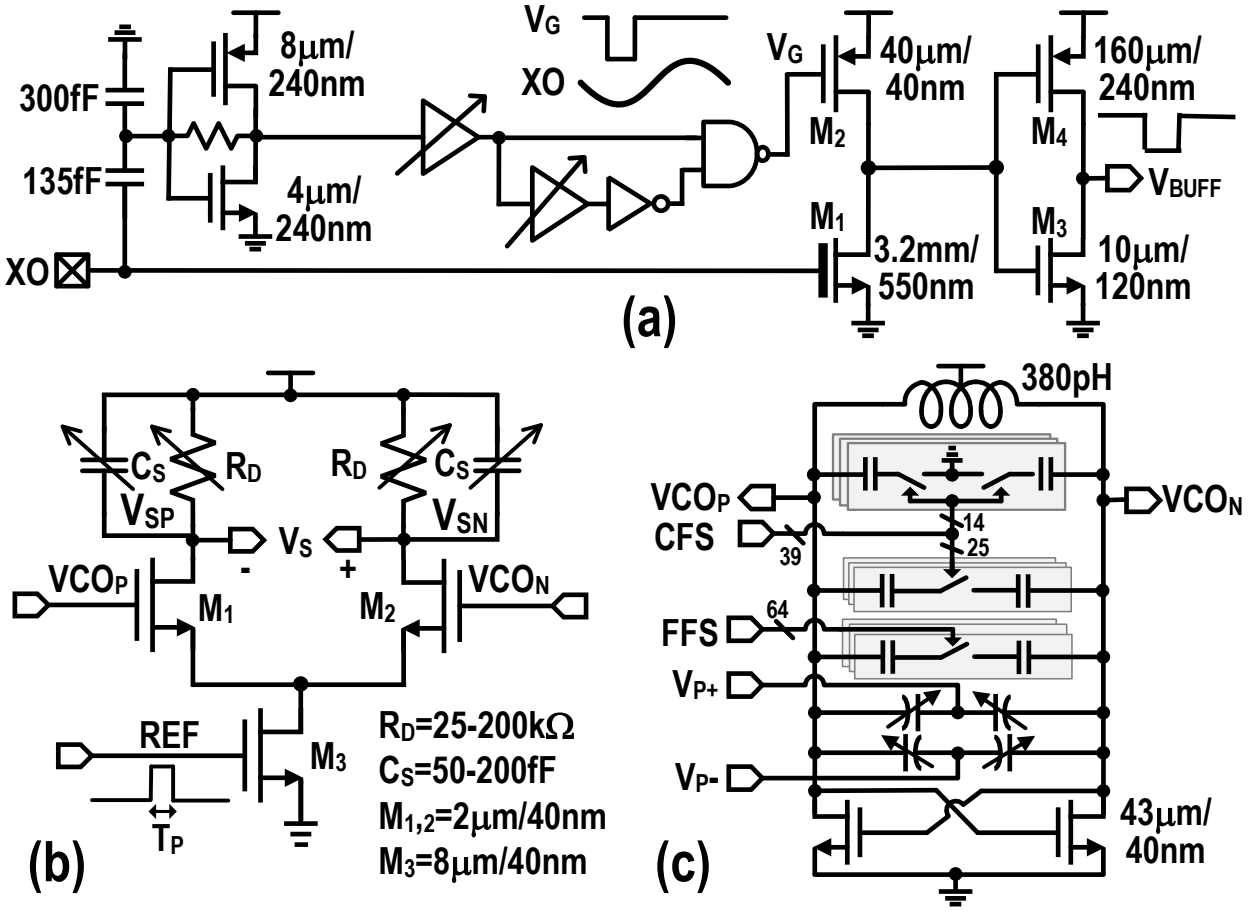

Figure 5.13: Schematics of the (a) reference buffer, (b) CSPD, and (c) VCO.

FTL should first determine the F_{ERR} sign since the aliasing signal does not provide that information. Consequently, FTL is initially set to decrease the F_{VCO} once the detected D_{FERR} is larger than a programmable threshold. Depending on whether D_{FERR} is decreasing or increasing, the initial loop sign is kept or flipped. To speed up the frequency locking process, FTL loop gain (LG) can be adaptively controlled based on the D_{FERR} value. Once FTL brings F_{VCO} into the PLL's lock-in range, the CSPLL rapidly locks the VCO phase to REF, forcing a nearly constant V_P. Hence, ERR stops toggling due to the insufficient input swing and low gain of the amplifier at frequencies below the PLL's lock-in range, eliminating the power of the digital logic. To avoid a false unlock detection, the noise of the amplifier is optimized such that it does not trigger the FTL when the CSPLL is locked.

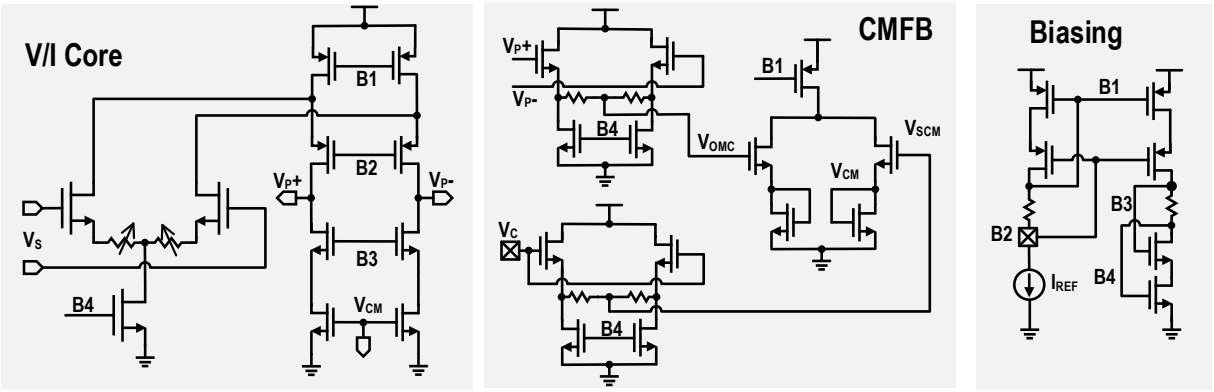

Figure 5.14: Schematics of the V/I.

5.4 Circuits Implementation

5.4.1 Reference Buffer and Pulse Generator

Fig. 5.13 (a) shows the reference buffer schematic adapted from [93]. The main transistor (M_1) is a thick-oxide device to allow a higher input swing, and is sized large and wide (3.2 mm/550 nm) to achieve a low PN floor (<-168 dBc/Hz). The gate terminal of the PMOS transistor (M_2) is driven by a pulse signal, V_G, derived from the delayed reference clock edge. In this way, the short-circuit current of M_1 and M_2 is minimized since M_2 is OFF when M_1 conducts current. The rising edge of the reference buffer then drives the pulse generator (PG) to realize the required CSPLL reference, whose pulse width ($\sim$35-to-55 ps) can be adjusted by a 4-bit switched-capacitor bank. While the simulated pulse width of PG varies $\sim\pm$50% over PVT variations, the maximum PD gain degradation is limited to 30%.

5.4.2 Phase Detector, V/I, and Loop Filter

Fig. 5.13 (b) shows the CSPD schematic, whose phase-detection gain can be changed ($\sim$0.1-0.6 V/rad) by a 7-bit resistor. Moreover, a 4-bit switched capacitor is added to adjust the CSPD output CM voltage (e.g., >500mV) over PVT variations. The resistor is implemented by unsilicided polysilicon resistor and the capacitor is implemented by metal-oxide-metal (MOM) capacitor as their values are relatively immune to temperature variations. The VCO output directly drives the CSPD without any isolation buffers to eliminate their power consumption and noise. As shown in Fig. 5.14, the V/I

is based on a fully-differential folded-cascode operational transconductance amplifier whose transconductance can be tuned by a 4-bit source-degenerated unsilicided polysilicon resistor. Thanks to the achieved high K_{PD}, even by consuming a negligible power (i.e., <20 μW), the simulated in-band PN due to the V/I thermal noise is extremely low (i.e., <-148 dBc/Hz). 1000 monte carlo simulations suggest thatA_{CM-DM} and A_{CM} are below -63 dB and -32 dB, respectively. The total capacitance of the loop filter is only 20.7 pF due to the fully-differential structure, optimized K_{PD}, and wide PLL bandwidth. The compensation resistance of the loop filter can be adjusted by a 4-bit unsilicided polysilicon resistor to regulate the bandwidth and damping factor of the PLL.

5.4.3 VCO

As shown in Fig. 5.13 (c), the VCO employs an NMOS-only cross-coupled pair with a single-turn inductor to achieve a low PN. The implicit common-mode resonance technique is used to reduce PN further [50, 127, 168]. To cover a wide tuning range with a small K_{VCO}, a combination of discrete tuning by switched-capacitor banks and continuous tuning by accumulation-mode MOS varactors [169] is adopted. The control of the varactors is fully-differential [92] to reject any CM ripples originated from the heavily-switched reference path with CMR >15 dB according to post-layout simulations.

5.5 Layout Consideration

In order to further minimize reference spurs due to the reference switching noise, the ground of the VCO, VCO test buffer, and loop filter is shared but is isolated from the ground of the reference buffer, pulse generator, CSPD, V/I, and FTL. In addition, the reference buffer, pulse generator, CSPD, V/I, and FTL are placed inside a deep N well (DNW). Moreover, the reference buffer is placed far away from the VCO inductor in the layout to minimize the crosstalk. The reference clock and pulse generator traces in the layout are carefully shielded and iterated to greatly mitigate crosstalk based on the post-layout simulation results. The VCO cross-couple pair is placed inside the DNW and a guard ring is used to hinder any clock bouncing locally. The VCO supply uses a standalone off-chip regulator, which is separated from the reference buffer and CSPD supply. The output of the VCO is routed differentially to

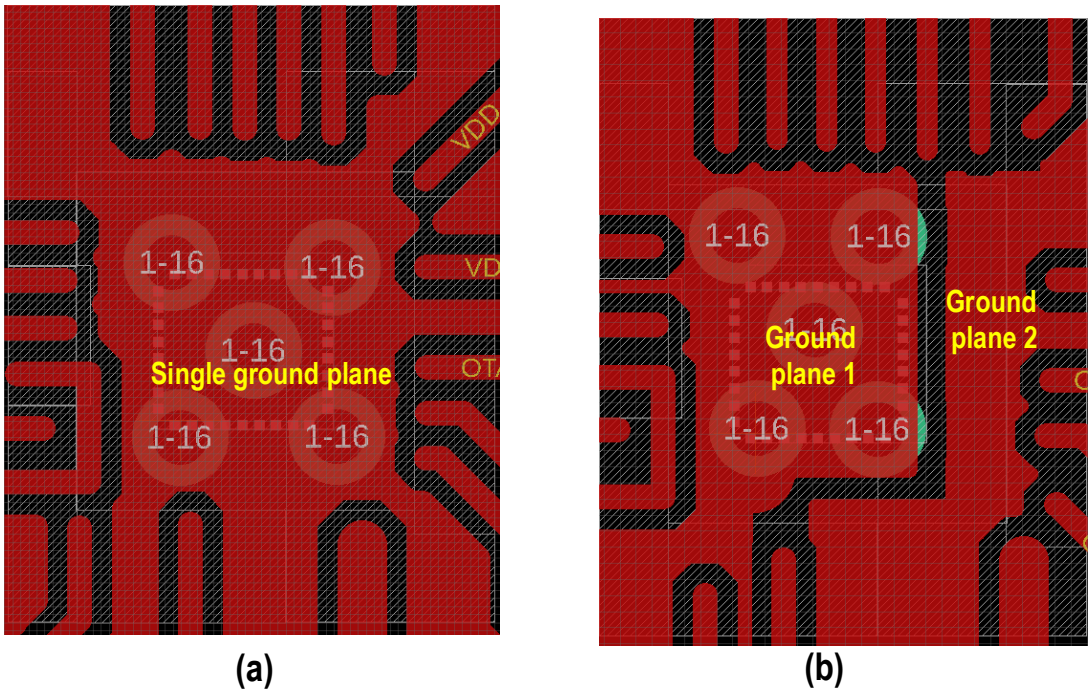

Figure 5.15: Layout of the PCB with (a) a single ground plane and (b) two separate ground planes.

the test divider to minimize the common-mode noise disturbance. A native layer (NTN) is added underneath the VCO inductor to minimize the noise coupling from the substrate.

The PCB layout is also carefully designed to minimize the crosstalk due to the non-zero impedance of the ground plane. In the original PCB design, as shown in Fig.5.15 (a), one single ground plane was used. The CSPLL chip grounds are directly down-bonded to such a ground plane. However, the measured spur level is higher compared with simulations, where the PCB ground is assumed as an ideal conductor. This is because that the ground plane has a non-zero inductance, resulting in poor isolation between the VCO and reference buffer. In the revised PCB design, as shown in Fig.5.15 (b), the VCO and test divider share one ground plane and the reference buffer, pulse generator, CSPD, V/I, and FTL share another ground plane. Two separate ground planes help to reduce local ground bounce due to the reference switching, improving spur performance by more than 10 dB based on measurements. Those two ground planes are merely connected near their corresponding power supplies to minimize unwanted couplings.

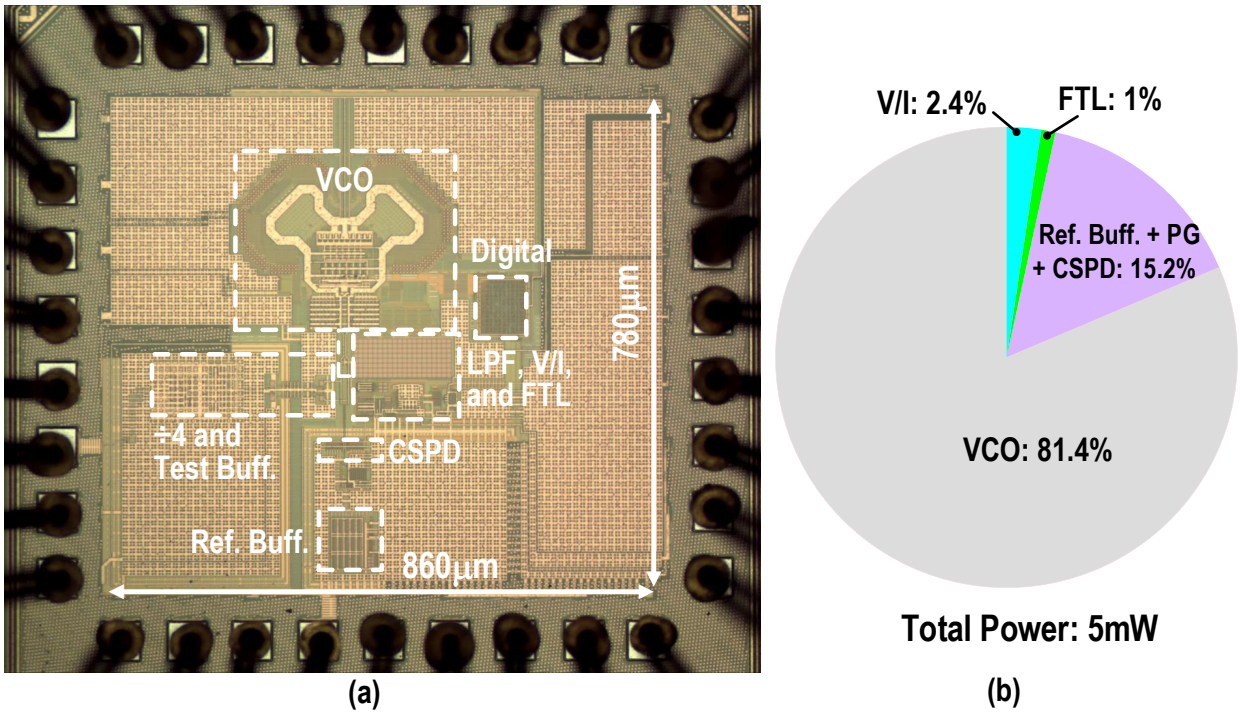

Figure 5.16: (a) Chip micrograph and (b) measured power breakdown.

5.6 Measurement Results

The CSPLL was fabricated in a standard 40-nm bulk CMOS and the core circuit occupies 0.13 mm^2, as shown in Fig. 5.16 (a). The PLL is powered by 0.6-V, and 1.1-V supplies. The 0.6-V supply is used for the VCO to satisfy time-dependent dielectric breakdown (TDDB) requirements for thin-oxide transistors, thus securing PLL's long-term reliability [170]. In a future design, thick-oxide devices can be used in the VCO such that the entire PLL can operate under a single power supply. This would not compromise the PLL phase noise and jitter performance but would slightly degrade VCO's tuning range. Alternatively, a complementary VCO can be used without sacrificing the tuning range and jitter performance. The entire PLL (excluding the test divider and buffer but including the reference buffer) dissipates 5 mW, and its power breakdown is shown in Fig. 5.16 (b). The test buffer between the VCO and divider consumes 2.1 mW. The FTL consumes 50 μW in total, of which the amplifier, the digital logic, and the reference clock divider consume 39 μW, 8 μW, 3 μW, respectively. The power and area overhead of the CSPD and FTL are negligible compared to the VCO.

The reference clock is derived from an off-chip high-quality VLCU-Type

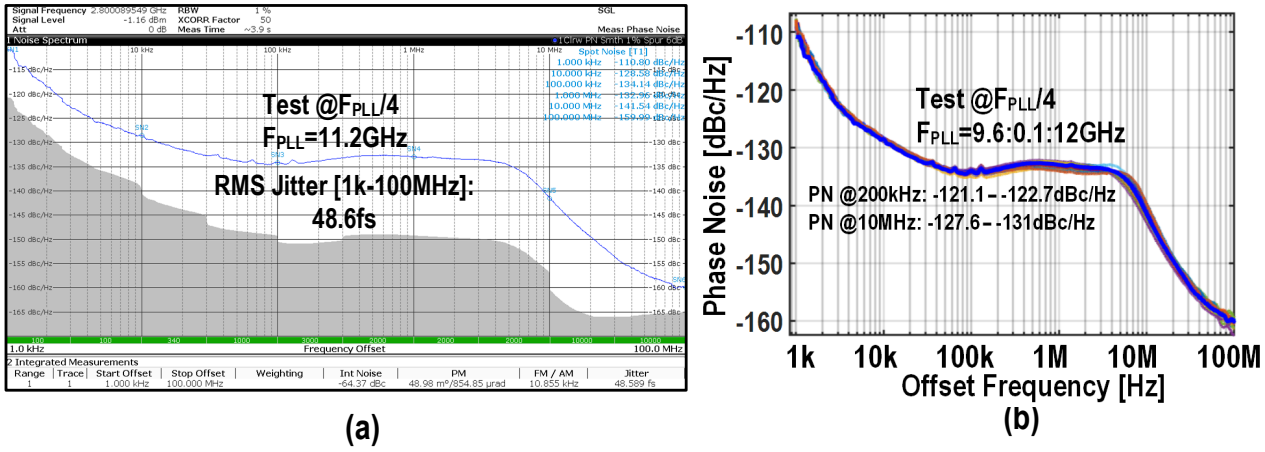

Figure 5.17: (a) Measured PN at 11.2 GHz after an on-chip divide-by-4; (b) measured PN for all integer channels.

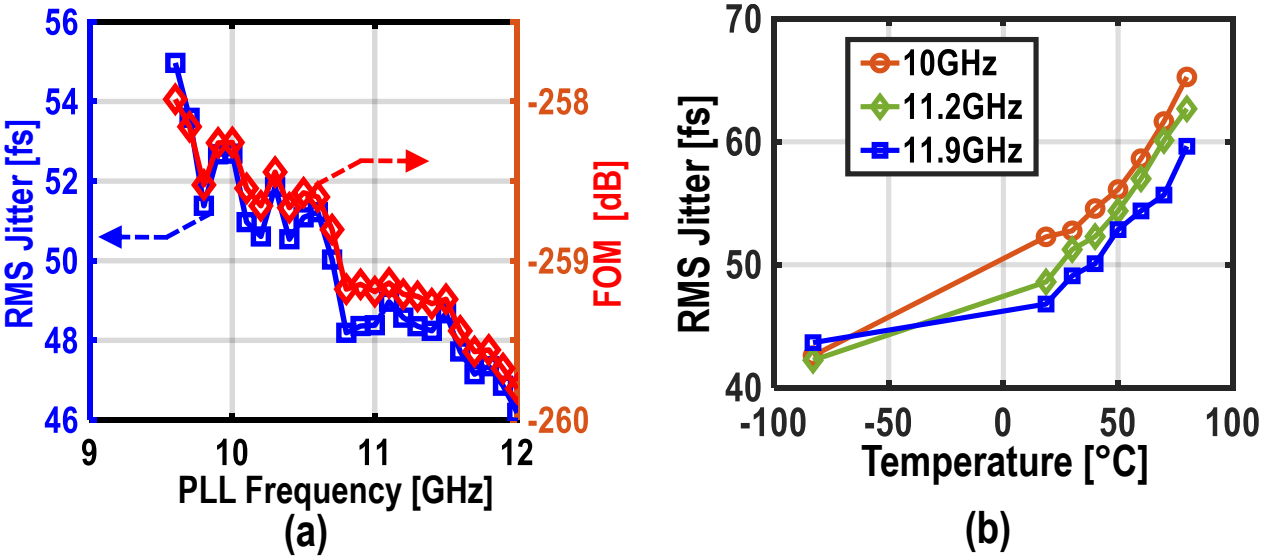

Figure 5.18: (a) Measured RMS jitter and FOM versus PLL tuning range; (b) measured RMS jitter versus temperature.

series crystal oscillator offered by Taitien. Fig. 5.17 (a) shows the measured PN plot at a PLL frequency (F_{PLL}) of 11.2 GHz after an on-chip divide-by-4. The RMS jitter is 48.6 fs (integrated from 1 kHz to 100 MHz but excluding reference spurs). To optimize the jitter performance at this frequency, T_P tuning code was adjusted to achieve the highest K_{PD}, and the PLL bandwidth was digitally regulated at ~6 MHz by adjusting the resistance of the loop filter, the transconductance of the V/I converter, and the R_D of the CSPD. The measured PN, RMS jitter, and FOM plots covering the PLL's tuning range (i.e., 9.6-12 GHz) are shown in Fig. 5.17 (b) and Fig. 5.18 (a). The in-band PN, RMS jitter, and FOM are better than -121 dBc/Hz, 55 fs, and -258 dB, respectively. As shown in Fig. 5.18 (b), the CSPLL appropriately works over a

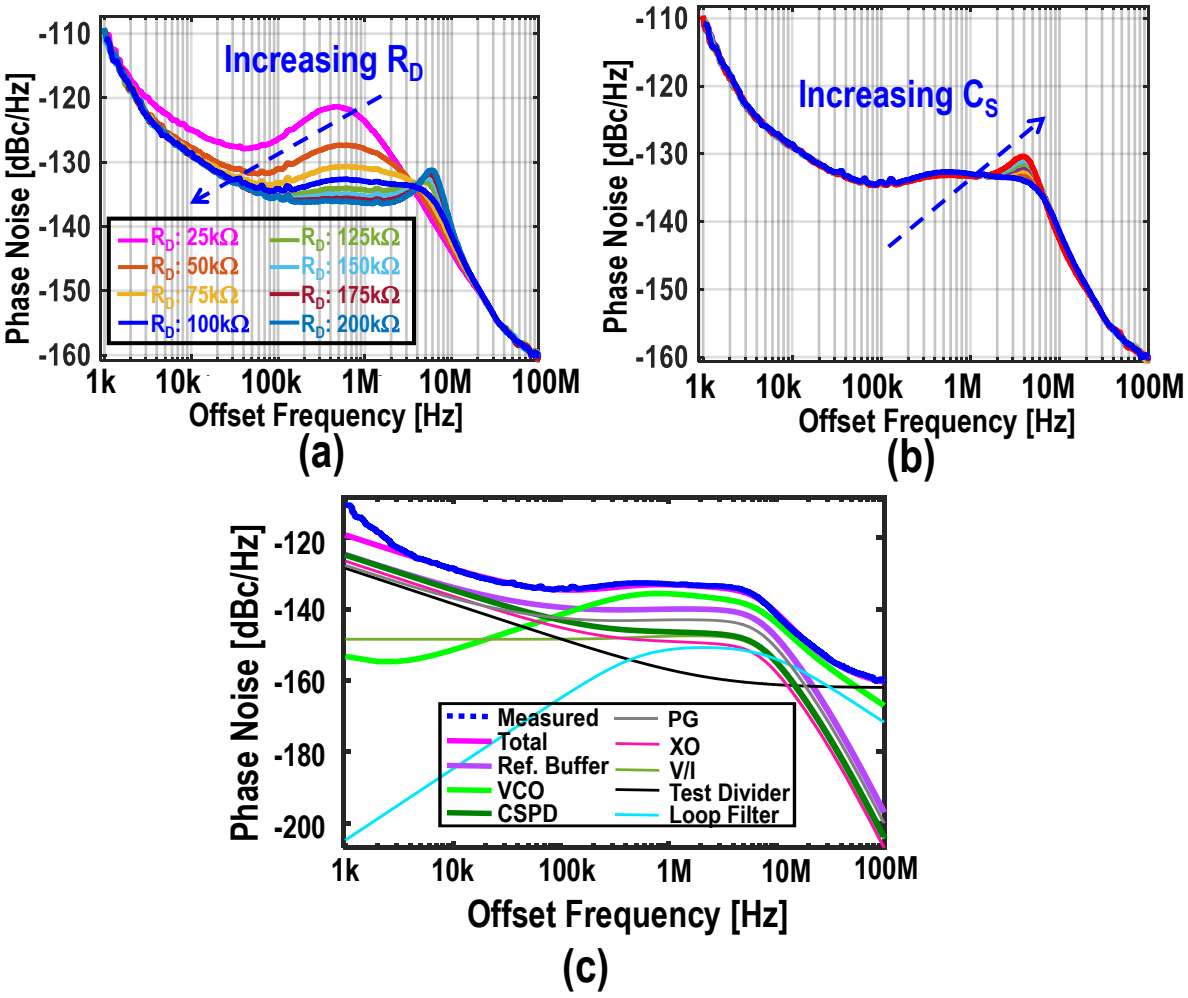

Figure 5.19: Measured PN for different values of (a) R_D and (b) C_S; (c) simulated PN contribution of different PLL blocks with the measured PN performance.

wide temperature range (i.e., from -80°C to +80°C), but its integrated jitter increases to 65 fs at 80°C. Notice that all of the above measurements were carried out under the same loop parameters setting[1], indicating the robustness of the design.

Fig. 5.19 (a) shows the measured PN plots for different R_D values. As predicted by (5.7), by enlarging R_D, K_{PD} increases, and the in-band PN at 200 kHz is monotonically reduced. Furthermore, for small R_D values, the CSPLL bandwidth is not wide enough to sufficiently attenuate the VCO PN. As the PLL loop bandwidth is widened by increasing R_D, the VCO PN is suppressed and the reference buffer eventually dominates the in-band PN. However, increasing R_D or C_S beyond their practical useful range introduces

[1]Unless otherwise specified, we fixed the loop parameters setting for all of the remaining measurements in this paper.

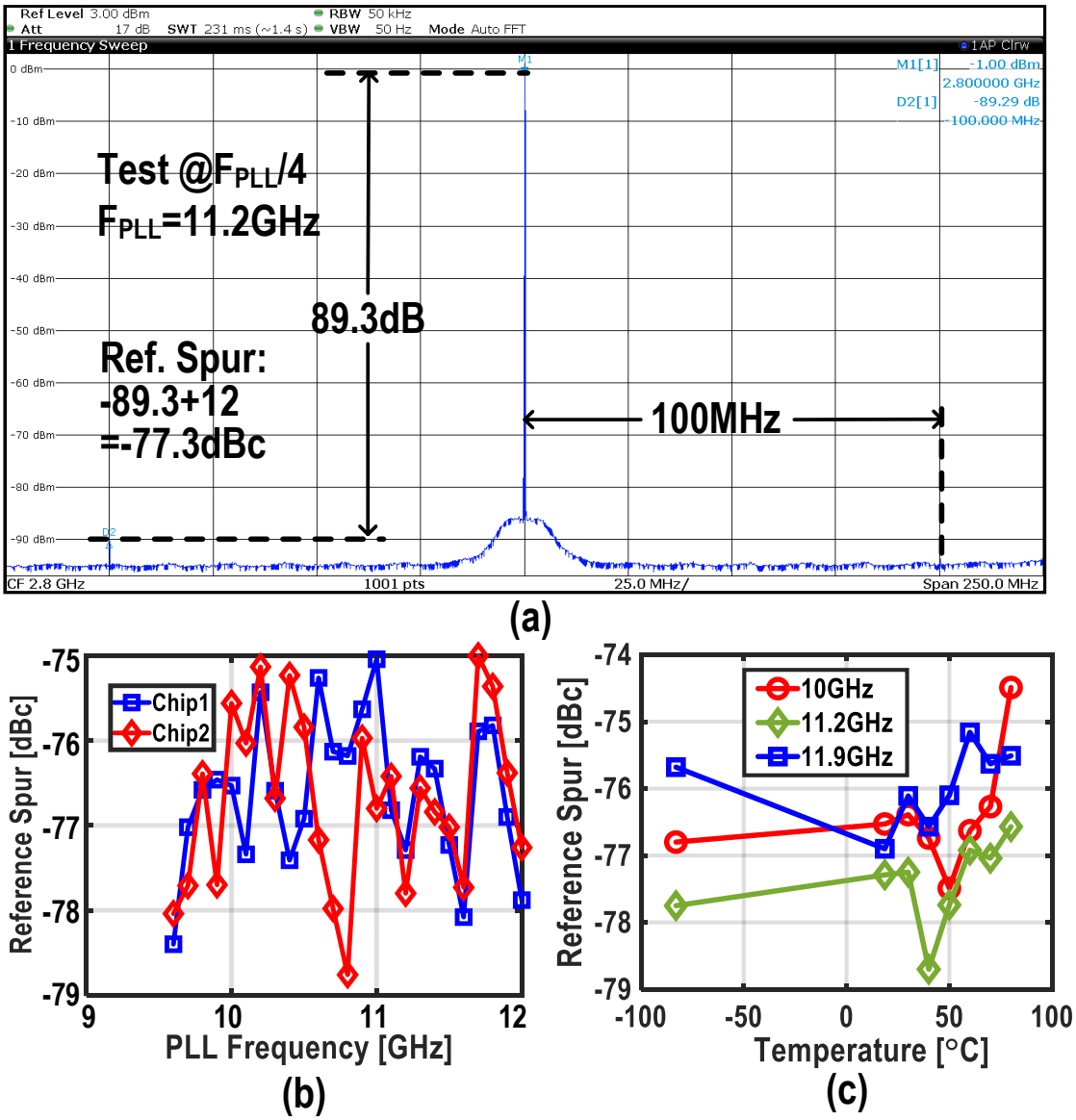

Figure 5.20: (a) Measured CSPLL spectrum after an on-chip divide-by-4; measured reference spur versus (b) PLL tuning range and (c) temperature.

peaking on the measured PN plots [see Fig. 5.19 (a) and (b)] due to the reduced phase margin. Changing T_P control code only marginally affects the measured PN performance due to the sine characteristics of K_{PD} [see Fig. 5.4 (a)] and the limited T_P tuning range of the pulse generator. To verify the phase-domain model presented in Section 5.3, the measured reference and free-running VCO PN, in addition to simulated loop parameters of the CSPLL, were used to calculate the closed-loop PN, and compare it to the measured result, as shown in Fig. 5.19 (c). The measured PN in blue matches very well with the predicted PN in pink. The discrepancy between two curves at 1 kHz–to–4 kHz frequency offsets mainly originates from the neglected supply noise in the phase-domain

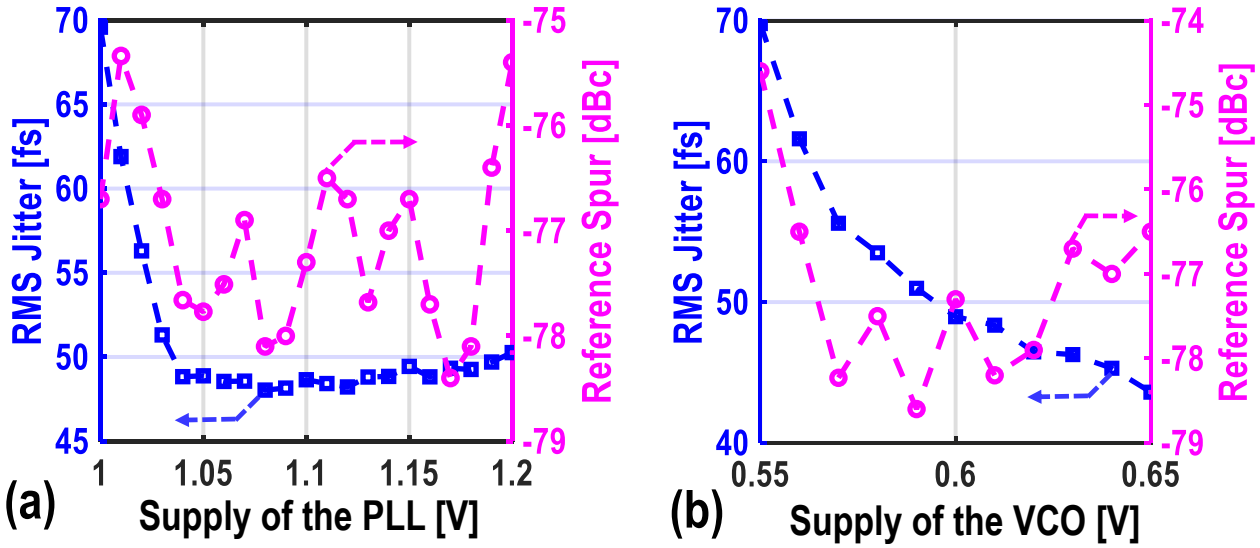

Figure 5.21: Measured RMS jitter and reference spur versus the power supply of the (a) PLL and (b) VCO at 11.2 GHz.

analysis.

Fig. 5.20 (a) shows the measured spectrum at the divide-by-4 output. The measured reference spur is -89.3 dBc at the divider output, translating to -77.3 dBc when referred to F_{PLL}. Since the measured spur level is ∼25 dB lower than the integrated PN (∼-52 dBc), the impact of reference spur on RMS jitter is marginal. The measured reference spur for two wire-bonded samples is <-74 dBc over the tuning range, and varies <3 dB over temperatures, as shown in Fig. 5.20 (b) and (c). The measured spur level varies <0.7 dB by sweeping C_S control code, indicating that the voltage ripple on V_S and the mismatch between CSPD components have a minor impact on reference spur. In addition, the measured spur level is also weakly related to T_P control word, and is ∼5 dB higher than the theoretical prediction given by (5.1). The dominated spur mechanism of the CSPLL is charge injection and clock feedthrough according to simulations. Compared with the CSPLL originally presented in [150], the spur performance is improved by modifying the PCB layout, and reducing the PCB ground bounces originated from the high current spike of the reference pin. In the modified PCB, the reference ground and VCO ground are merely connected near their corresponding power supplies to minimize unwanted couplings.

Fig. 5.21 shows the measured RMS jitter and reference spur versus the power supply of the PLL and VCO at 11.2 GHz. The RMS jitter varies <4 fs when the PLL supply was swept from 1.04 to 1.2 V. However, it degrades

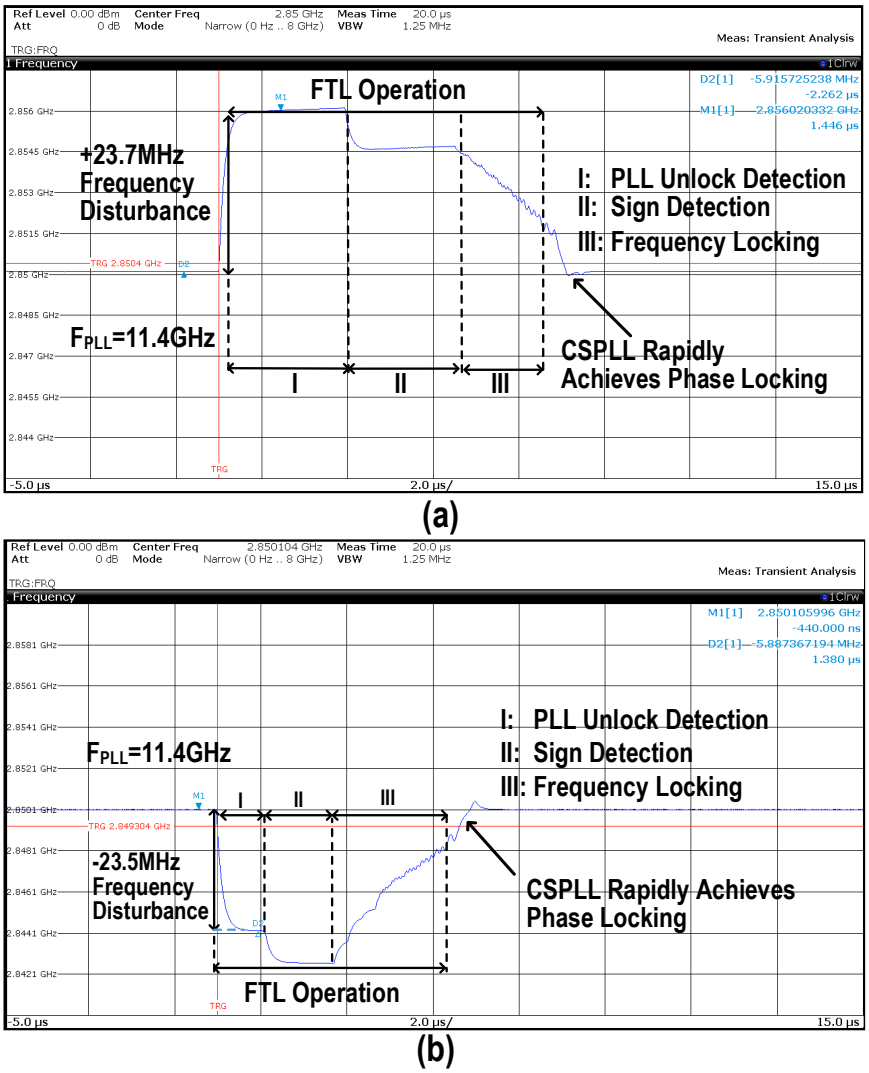

Figure 5.22: Measured FTL transient response to (a) a positive frequency disturbance and (b) a negative frequency disturbance.

to 70 fs under a 1 V supply mainly due to the higher PN contribution of the reference buffer. As the oscillation swing increases by raising VCO's supply voltage, both VCO phase noise and K_{PD} are improved, leading to a lower RMS jitter. The measured reference spur is still $<$ -74 dBc over a wide supply variation.

Fig. 5.22 shows the measured transient response of the FTL to a positive or negative frequency disturbance injected to the VCO by intentionally changing the VCO control code. In both cases, the FTL successfully detects the frequency error and relocks the VCO within 10 μs thanks to the implemented adaptive gain adjustment technique.

For completeness, the CSPLL was characterized at 4.2 K as well. A setup similar to [48] was used to immerse the PLL sample into the liquid helium.

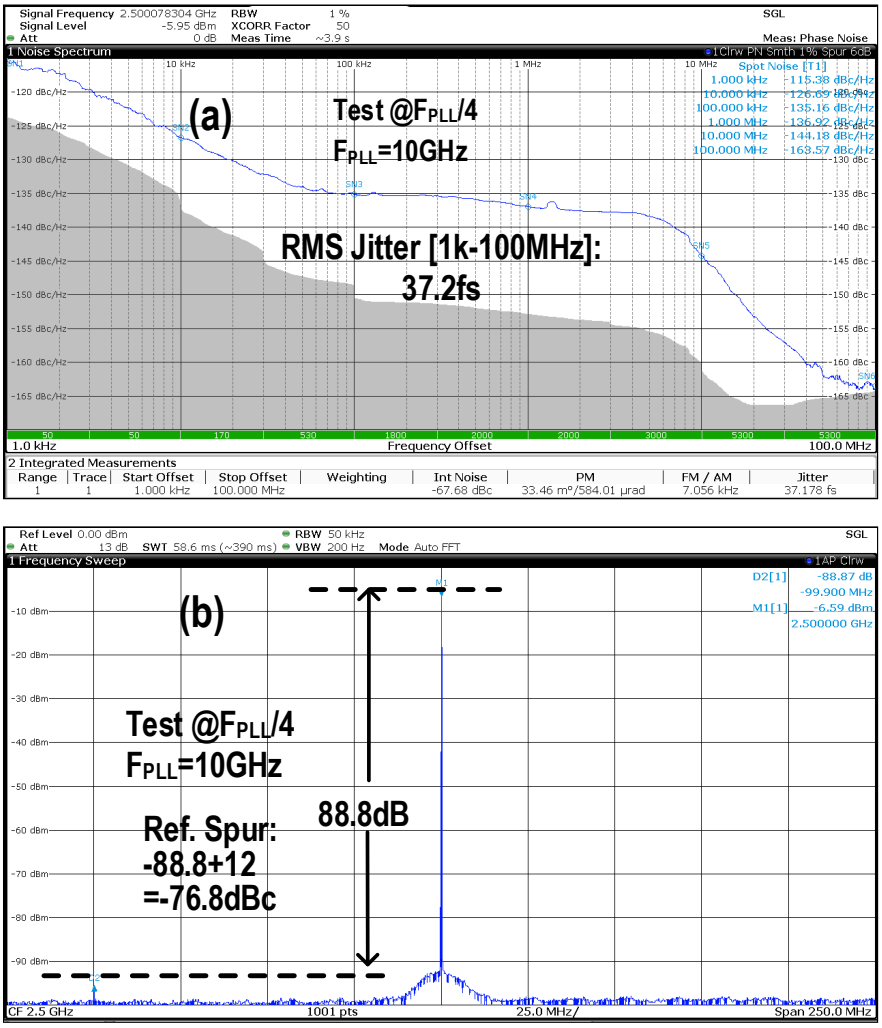

Figure 5.23: Measured CSPLL (a) phase noise and (b) spectrum after an on-chip divide-by-4 at 4.2 K.

Compared to room-temperature measurements, the CSPLL was re-optimized in order to deliver low-jitter performance at 4.2 K. The CSPLL consumes ∼3 mW power at 4.2 K. Figure 5.23 (a) and (b) respectively depict the measured phase noise and spectrum of the CSPLL after an on-chip divide-by-4 at 4.2 K, where the CSPLL was running at 10 GHz. Compared with 300 K, the measured RMS jitter reduces from 48.6 fs to 37.2 fs thanks to the channel noise reduction at 4.2 K. The measured reference spur is -88.8 dBc at the test divider output, translating to -76.8 dBc when referred to the PLL frequency. Those results indicate that the proposed CSPLL can deliver low-jitter and low-spur performance over a wide temperature range.

Table 5.1 summarizes the CSPLL performance and compares it with the state-of-the-art with a frequency-tuning range (FTR) higher than 3%. Thanks to the proposed CSPD and low-power FTL, the proposed CSPLL shows the

lowest reference spur, lowest jitter, best FOM, and a 2.5 dB improvement in FOM_N. While the SSPLL in [153] achieved a comparable reference spur level, an area-hungry VCO isolation buffer with an inductive load was used. The CSPLL also occupies the smallest area compared to other type-II PLLs. In addition, the proposed CSPLL can deliver high performance at 4.2 K as well.

5.7 Conclusion

We presented a charge-sampling PLL (CSPLL) and analyzed in-depth its transient response, phase-detection gain, reference spur, and phase noise performance. Thanks to its high phase-detection gain and excellent isolation between the VCO and the sampling capacitor, the PLL can simultaneously achieve an ultra-low-RMS jitter and an outstanding reference spur with a large frequency multiplication factor. Moreover, a power-efficient highly-digital frequency-tracking loop is introduced to lock the CSPLL robustly when the VCO faces a sudden frequency disturbance. Measurement results show that the CSPLL achieves 48.6 fs RMS jitter and -77.3 dBc reference spur at an 11.2 GHz carrier frequency while consuming 5 mW. This corresponds to the best-reported jitter-power FOM and reference spur performance. Moreover, cryogenic measurement results indicate that the proposed CSPLL can deliver high performance at 4.2 K as well.

Table 5.1: Comparison table with state-of-the-art LC-based Integer-N PLLs with FTR Larger than 2.5%.

	This Work	Z. Zhang JSSC'20	Z. Yang ISSCC'19	Y. Lim, ISSCC'20	D. Lee JSSC'20	A. Sharkia JSSC'18	J. Sharma JSSC'19	J. Kim ISSCC'19	D. Turker ISSCC'18	H. Zhang VLSI'19
PLL Architecture	**Type-II CSPLL**	Type-II SSPLL	Type-II iSSPLL	Type-II SSPLL	Type-II SSPLL	Type-I SSPLL	Type-II RSPLL	Type-II SSPLL	Type-II CPPLL	Type-II ILCM
Power Supply [V]	**1.1/0.6**	0.65	1/0.55	NA	1	0.8	1.2/0.5	NA	NA	NA/0.14
F_{REF} [MHz]	**100**	200	103	50	100	100	50	100	500	100
F_{PLL} [GHz] FTR [GHz]	**11.2 9.6-12 (22.2%)**	14 12-16 (28.6%)	26.4 25.4-29.5 (14.9%)	13.05 12-14.5 (18.9%)	2.4 NA (NA)	5 4.6-5.6 (19.6%)	2.55 2.05-2.55 (21.7%)	3.8 3.3-4.3 (26.3%)	12.5 7.4-14 (61.7%)	2.4 2.2-2.6 (16.7%)
PLL Bandwidth [MHz]	**~6**	~7	~4	~3	~0.6	~6	~1	~3	~3	~10
S_{REF} [dBc]	**-77.3**	-64.6	-63	-75	-67	-64.1	-63	-75	-75	-66.5 $
***S_{REF_Nor} [dBc]**	**-77.3**	-66.5	-70.4	-76.3	-53.6	-57.1	-50.1	-65.6	-76	-53.1
RMS Jitter, σ_{rms} [fs] [Int. Bandwidth]	**48.6 [1k-100MHz]**	56.4 [1k-100MHz]	71 [1k-100M]	83 [1k-100M]	161 [10k-100M]	162.2 [10k-100MHz]	110 [10k-100M]	72 [1k-30MHz]	53.6 [10k-10M]	298 [0.1k-100M]
P_{DC} [mW]	**5**	7.2	15.3 ^	6.7	0.9 #	1.1	3.7	19.1	45	0.17 #
P_{DC} of Iso. Buffer [mW]	**0**	1.4	0.56	~1.5	0	0.15	~0.4	~7	NA	0
Inductor Used in Iso. Buffer ?	**NO**	YES	YES	YES	NO	NO	NO	NO	NO	NO
****FOM [dB]**	**-259.2**	-256.4	-251.1	-253	-256.3	-255.4	-253.5	-250.1	-248.9	-258.2
*****FOM_N [dB]**	**-279.7**	-274.9	-275.4	-277.2	-269.8	-272.4	-270.6	-265.8	-262.8	-272
Core Area [mm²]	**0.13**	0.234	0.24	0.23	0.42	0.01	0.36	0.21	0.35	0.25
Process [nm]	**40**	40	65	65	65	65	65	65	16	65

*$S_{REF\_Nor} = S_{REF}+20*\log_{10}(11.2GHz/ F_{PLL})$ **$FOM = 20*\log_{10}(\sigma_{rms}/1s)+10*\log_{10}(P_{DC}/1mW)$ ***$FOM_N = FOM+10*\log_{10}(1/N)$ defined in K. M. Megawer ISSCC'2018
^Reference buffer power of 5.08mW excluded #FTL power excluded or not reported $Reported value using an 800MHz reference

Chapter

6

A Cryo-CMOS Dynamic-Amplifier-Based PLL

In the previous chapter, a low-jitter and low-spur PLL based on the charge-sampling concept is presented for general applications. In this chapter, another high-performance PLL is introduced[1]. This PLL operates from 300 K to 4.2 K and is designed for the control system of scalable quantum computers. By considering the benefits and challenges of cryogenic operation, a dedicated analog PLL structure is employed so as to maintain high performance from 300 K to 4.2 K. The PLL incorporates a dynamic-amplifier-based charge-domain sub-sampling phase detector, which simultaneously achieves low phase noise and low reference spur thanks to its high phase-detection gain and minimized periodic disturbances on the VCO control. Fabricated in a 40-nm CMOS process, the PLL achieves -78.4-dBc reference spur, 75-fs RMS jitter, and 4-mW power consumption at 300 K when generating a 10-GHz carrier, leading to a -256.5-dB jitter-power FOM. At 4.2 K, the PLL synthesizes 9.4-to-11.6-GHz tones with an RMS jitter of 37 fs and a reference spur of -69 dBc while consuming 2.7 mW at 10 GHz.

[1]This chapter has been published in the IEEE Journal of Solid-State Circuits [68].

6.1 Introduction

In quantum computing applications, control and read-out of qubits require the generation and acquisition of high-frequency microwave bursts. As mentioned in Chapter 2, the application of microwave bursts for qubit control requires the generation of a carrier using a phase-locked loop (PLL) operating at 4.2 K. This chapter introduces the first cryo-CMOS PLL operating at 4.2 K. A new charge-domain sub-sampling phase detector (PD) based on the operation of a dynamic amplifier is leveraged to meet the required specifications. At 10 GHz, the cryo-CMOS PLL achieves 37-fs RMS jitter and -69-dBc S_{REF} while consuming 2.7 mW, corresponding to a PLL FOM of -264 dB.

This chapter is organized as follows. Section 6.2 discusses the most appropriate PLL structure for QC applications. In Section 6.3, the theoretical analysis and design considerations of the proposed PD are presented. Section 6.4 describes the PLL architecture, its phase-domain model, and cryogenic circuit design considerations. Finally, we present measurement results in Section 6.5 and conclude this article in Section 6.6.

6.2 Appropriate PLL Architecture for QC Applications

As mentioned in the previous Chapter 2, an integer-N PLL is required to convert the desired signals. This section will investigate the most appropriate integer-N PLL architecture for QC applications by considering the benefits and challenges of cryogenic operation.

A digital PLL [75] is less attractive at CT as the quantization noise (QN) of a time-to-digital converter (TDC), and a digitally-controlled oscillator (DCO) does not significantly scale with temperature. Firstly, the resolution of a simple TDC typically equals a gate delay, which is estimated to reduce by ∼30% from 300 K to 4.2 K [143]. The resulting in-band PN improvement is limited to 3 dB. Secondly, compared with RT, the measured inherent PN of an oscillator improves substantially (∼10 dB) at 4.2 K [48]. Yet, the measured frequency resolution of a DCO is weakly temperature-dependent. Thus, the PN introduced by the finite resolution of the DCO does not appreciably improve over temperature. Hence, the total PN of a DCO could be entirely dominated by its QN, limiting the PLL's out-of-band PN. Consequently, while

the cryo-CMOS digital PLL in [64,66] consumes 12.5 mW power, the measured RMS jitter is above 100 fs, failing to meet specifications required for quantum computing applications. While a bang-bang PLL relaxes the PD's resolution requirement [171], its locking behavior and bandwidth are strongly noise-dependent and difficult to predict at CT due to the lack of mature noise models.

An analog charge-pump PLL (CPPLL) [74] could be employed at CT due to the thermal noise reduction and the absence of QN introduced by the PD and oscillator. However, the CPPLL loop components (i.e., charge pump and divider) consume high P_{DC} and introduce high in-band PN. Hence, the cryo-CMOS CPPLL in [67] has an in-band phase noise above -100 dBc/Hz while consuming 35 mW of power. Furthermore, the mismatch of active devices becomes much worse at CT [116], which degrades the matching between the charge pump's "up" and "down" current branches, resulting in a higher S_{REF}. An injection-locked clock multiplier (ILCM) could generate a low-noise clock efficiently by eliminating the loop components. Yet, its PN and S_{REF} performance is severely degraded if the free-running frequency of the oscillator is not tuned precisely to the desired frequency over voltage and temperature variations. Hence, an ILCM must incorporate complex digital calibration [78,82,84,85], resulting in high design complexity.

Analog PLLs based on the voltage-sampling [88,90,91,97,153,172,173] or charge-sampling [149,150] concepts are more promising candidates at CT [see Fig. 6.1 (a)-(b)], as they can achieve low in-band PN due to their high phase-detection gain (K_{PD}). Nevertheless, a voltage-sampling PD (VSPD) requires an RF output bandwidth to properly track the oscillator voltage and a large sampling capacitance (C_S) to achieve a low in-band PN, thus demanding a relatively large P_{DC}. Besides, compared with RT, the on-resistance of the sampling switches ($S_{3,4}$) dramatically increases at CT as the DC voltage at the sampler output is typically designed to be near the middle of the supply voltage.

Hence, the sampler output voltage swing could be severely compromised, thus degrading K_{PD} and in-band PN. Moreover, in order not to degrade K_{PD}, the reference pulse width (T_P) should be at least a few oscillator cycles (T_{VCO}) to ensure that the VSPD output reaches its steady-state before the sampling instants. This limits the minimum achievable S_{REF} due to the oscillator's

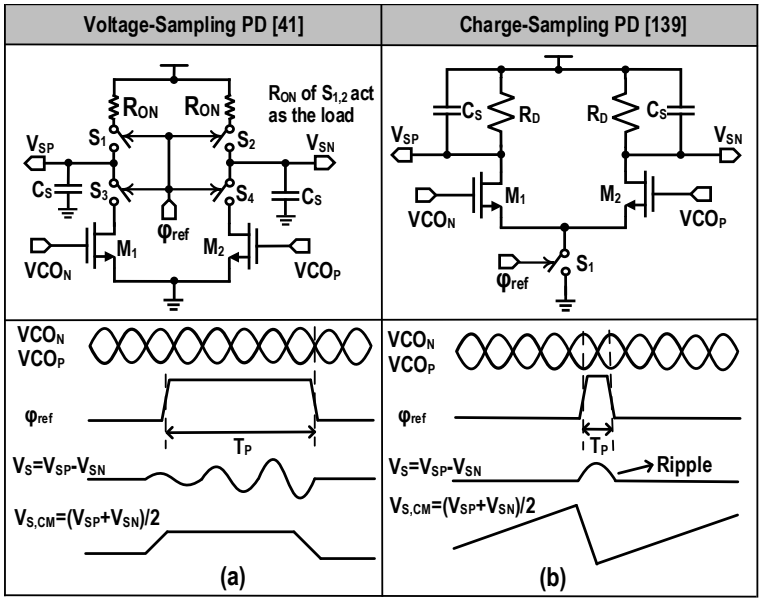

Figure 6.1: Schematics and conceptual waveforms of (a) voltage-sampling PD [90] and (b) charge-sampling PD [149].

disturbance during T_P.

The output bandwidth and T_P can be much lower in a charge-sampling PD (CSPD) introduced in [149, 150]. Nevertheless, as depicted in Fig. 6.1 (b), even in the locked condition, the differential-mode (DM) output voltage of the CSPD experiences a ripple during T_P, thus degrading the minimum achievable S_{REF}. Besides, the load resistor (R_D) and C_S should be very large to simultaneously improve K_{PD} and S_{REF}, thus compromising the PLL phase margin, especially when a wide bandwidth is used due to a considerable R_DC_S delay. Moreover, the CSPD output common-mode (CM) voltage varies significantly over one reference period (T_{REF}) [see Fig. 6.1 (b)], thus demanding a stringent requirement on the CM rejection of the next stages. To improve on those limitations, we introduce a charge-mode sub-sampling PLL that incorporates a new PD based on the operation of a dynamic amplifier.

6.3 Dynamic-Amplifier-Based Phase Detector

6.3.1 Operation

Fig. 6.2 (a)-(b) illustrate the schematic and conceptual waveforms of the dynamic-amplifier-based PD (DAPD). The circuit begins in the reset mode, with the output nodes V_{SP} and V_{SN} precharged to V_{DD} when the reset clock

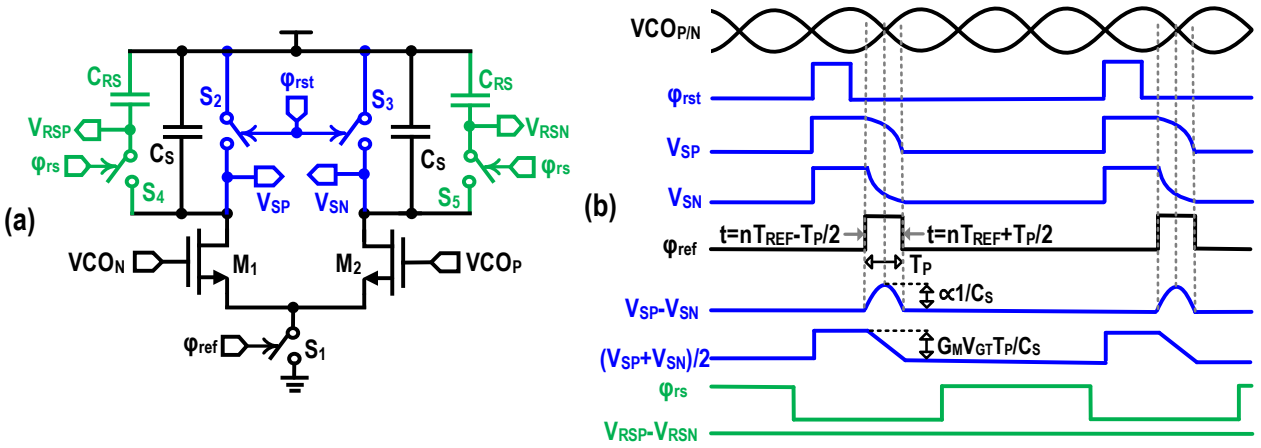

Figure 6.2: (a) Simplified schematic and (b) conceptual waveforms of a DAPD.

(φ_{rst}) is high. This aims to clear the memory of the previous operation and set a high CM voltage for the next mode. When the reference clock (φ_{ref}) goes high, the circuit enters the phase-detection mode. The transconductance devices ($\mathrm{M_{1,2}}$) are instantly turned ON, drawing a DM current of $\mathrm{G_M A_{VCO} sin(\omega_{VCO} t + \phi_e)}$ from $\mathrm{C_S}$, where $\mathrm{G_M}$ is the large-signal transconductance of $\mathrm{M_{1,2}}$ and ϕ_{e} is the instantaneous phase error between the zero-crossing of the VCO and the middle of the φ_{ref}. Notice that the on-resistance of the sampling switch $\mathrm{S_1}$ and reset switches $\mathrm{S_{2,3}}$ reduces at CT due to the large overdrive voltage. Hence, compared with a VSPD, a DAPD benefits more from the cryogenic operation. The operation of a DAPD is similar to that of a dynamic amplifier [174–176] or a charge-steering amplifier [177, 178], which has demonstrated excellent power efficiency and noise performance when used in data converters and wireline transceivers [174–178]. As will be demonstrated, the proposed DAPD can achieve low PN and high $\mathrm{K_{PD}}$ with low $\mathrm{P_{DC}}$ when incorporated into a PLL.

6.3.2 Phase-Detection Gain

During the n-th reference clock period ($\mathrm{nT_{REF}}$), the DM current of $\mathrm{M_{1,2}}$ can be modeled by

$$\mathrm{I_n(t) = G_M A_{VCO} sin(\omega_{VCO} t + \phi_e) \cdot p_0(nT_{REF} + \frac{T_P}{2} - t)}, \tag{6.1}$$

where $\mathrm{p_0(t)}$ is a deterministic sampling function, and can be expressed by a unit step function $u(\mathrm{t})$.

$$\mathrm{p_0(t) = } u(-\mathrm{t} + \mathrm{T_P}) - u(-\mathrm{t}). \tag{6.2}$$

Table 6.1: Comparison between a CSPD and a DAPD.

	CSPD	DAPD
K_{PD}	$2A_{VCO}\cdot\frac{G_M R_D}{N\pi}\cdot\sin(0.5\omega_{VCO}T_P)$	$\frac{4G_M A_{VCO}}{\omega_{VCO}C_S}\cdot\sin(0.5\omega_{VCO}T_P)$
Intrinsic Delay	$\sim 2.5T_{REF}$	$0.5TP \approx 0.25TVCO$
PN	*Not* a function of C_S	A function of C_S
S_{REF}	1, Degraded by C_S mismatch 2, High CMR of next stages required	1, *Not* degraded by C_S mismatch 2, High CMR of next stages *not* required

The sampled DM voltage at the time instant $nT_{REF}+T_P/2$ is

$$\begin{aligned} V_S(n) = V_{SP}(n) - V_{SN}(n) = \frac{2}{C_S}\int_{-\infty}^{+\infty} I_n(t)dt \\ = V_C \int_{-\infty}^{+\infty} \sin(\omega_{VCO}t + \phi_e)p_0(nT_{REF} + \frac{T_P}{2} - t)dt, \end{aligned} \tag{6.3}$$

where V_C is defined as $2G_M A_{VCO}/C_S$[1]. If ϕ_e is small, by solving the integral of (6.3), K_{PD} can be estimated by

$$K_{PD} = \frac{\overline{V_s}}{\phi_e} \approx \frac{4G_M A_{VCO}\sin(0.5\omega_{VCO}T_P)}{\omega_{VCO}C_S}. \tag{6.4}$$

K_{PD} is a periodic function of T_P, and reaches the maximum at $T_P = 0.5T_{VCO}$. Due to the sinusoidal dependence of K_{PD} to T_P, K_{PD} varies less than 30% even if T_P varies from 0.25 to 0.75 T_{VCO}. Besides, based on the measured frequency of a ring oscillator, T_P is expected to vary less than 40% from 300 K to 4.2 K [111]. Therefore, T_P may not need calibration over process, voltage, and temperature (PVT) variations. This property is similar to a CSPD in [149] due to the windowed-current integration. However, as listed in Table 6.1, K_{PD} of a DAPD is inversely proportional to C_S, which is in stark contrast to that of a CSPD in [149].

Fig. 6.3 (a) and (b) respectively show the simulated and calculated K_{PD} versus F_{VCO} and C_S by considering $(W/L)_{1,2} = 1.2\mu m/40nm$, $A_{VCO} = 0.45$ V, and $T_P = 30$ ps. Simulations closely match the presented theory if a reasonable C_S value is used. Interestingly, even with a constant T_P of 30 ps, K_{PD} varies

[1]For simplicity, the transconductance of $M_{1,2}$ is assumed to be constant.

by less than 10% when F_{VCO} changes between 5 GHz and 10 GHz. In addition, compared with 300 K, the simulated K_{PD} reduces ∼20% at 4.2 K due to the increase of threshold voltage. A small C_S is desired to achieve a high K_{PD}. However, as depicted in Fig. 6.2 (b), the CM voltage of the DAPD drops during T_P. If $M_{1,2}$ enter the triode region due to this CM drop, G_M and hence K_{PD} would be potentially compromised. As a result, the simulated K_{PD} deviates from the calculated value if a smaller C_S is used [see Fig. 6.3 (b)].

Notice that the last integral term in (6.3) results from the convolution of the sampling function and the transconductors' DM current. Hence, the complete spectrum of V_S without considering the zero-order hold could be expressed as

$$V_S(f) = V_C \sum_{k=-\infty}^{+\infty} S(f - kF_{REF}) \cdot P_0(f - kF_{REF}), \tag{6.5}$$

where $S(f)$ is the spectrum of $\sin(\omega_{VCO}t + \phi_e)$, and $P_0(f)$ is the spectrum of $p_0(t)$ [179]. Since ϕ_e is typically very small when a PLL is locked, $S(f)$ can be estimated by

$$S(f) \approx \frac{1}{2}(\Phi(f - F_{VCO}) + \Phi(f + F_{VCO})), \tag{6.6}$$

where $\Phi(f)$ is the spectrum of ϕ_e and F_{VCO} is the VCO frequency. As $P_0(f)$ is $T_P \cdot \mathrm{sinc}(\pi f T_P) e^{-i\pi f T_P}$, the spectrum of V_S is

$$V_S(f) = V_C T_P \cdot \sum_{k=-\infty}^{+\infty} ((\Phi(f - kF_{REF} - F_{VCO}) + \Phi(f - kF_{REF} + F_{VCO})) \cdot \mathrm{sinc}(\pi(f - kF_{REF})T_P) \cdot e^{-i\pi f T_P}). \tag{6.7}$$

By ignoring the high-frequency aliasing components of $\Phi(f)$, (6.7) can be estimated by

$$V_S(f) \approx V_C \Phi(f) \sum_{p=\pm 1} \frac{\sin(\pi(f + p \cdot F_{VCO})T_P)}{\pi(f + p \cdot F_{VCO})} \cdot e^{-i\pi f T_P}. \tag{6.8}$$

Consequently, the intrinsic delay of a DAPD is $T_P/2$, which is very small compared with T_{REF} and hence can be safely ignored. On the other hand, the narrow-band nature of a CSPD adds a significant loop latency due to the large $R_D C_S$ delay ($\sim 2.5 T_{REF}$ in [149]), degrading the PLL phase margin.

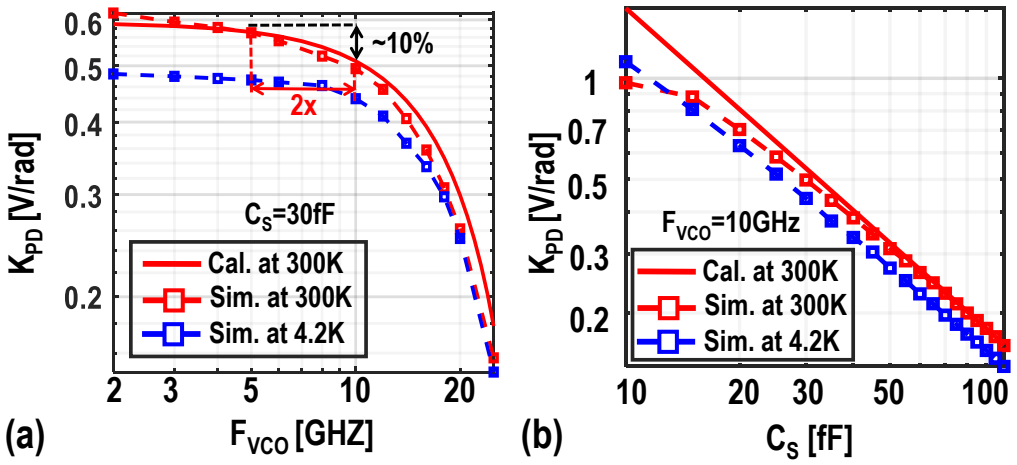

Figure 6.3: Simulated and calculated K_{PD} versus (a) F_{VCO} and (b) C_S at RT.

As depicted in Fig. 6.2 (b), the DM voltage of the DAPD ($V_{SP} - V_{SN}$) experiences a voltage ripple due to the windowed-current integration, degrading S_{REF}. While a large C_S could be used to reduce this ripple, the resulting K_{PD} would be degraded. To this end, as shown in Fig. 6.2 (a), an extra stage composed of capacitors C_{RS} and switches $S_{4,5}$ is added to resample V_{SP} and V_{SN} after the phase comparison without compromising K_{PD}. The resampling also ideally eliminates the CM ripple at the DAPD output. As a result, a highly constant output voltage (V_{RSP} and V_{RSN}) can be used to control the VCO without degrading S_{REF}. While the on-resistance of switches $S_{4,5}$ does not affect K_{PD}, it could introduce a delay at CT and degrade the phase margin. This issue will be addressed in Section 6.4.

6.3.3 Transient Response of the DAPD

Fig. 6.4 shows the simulated DAPD's steady-state waveforms and transient response when a 5° input phase step is applied to the VCO at 130 ns. As expected, due to the phase error, the DM voltage at the DAPD output becomes non-zero (∼50 mV) while the CM voltage is nearly unchanged. Thanks to the resampling, both the DM and CM ripples at the DAPD output are dramatically suppressed. The small residual DM ripple at F_{VCO} is mainly due to the gate's parasitic capacitance (C_{gd}) of $M_{1,2}$, which can be sufficiently attenuated by the PLL loop filter and should not limit the S_{REF} performance. Compared with a CSPD, the simulated CM ripple of a DAPD is >10× smaller, and is only limited by the leakage of $M_{1,2}$. This significantly relaxes the CM rejection of the following stages for a given S_{REF} requirement.

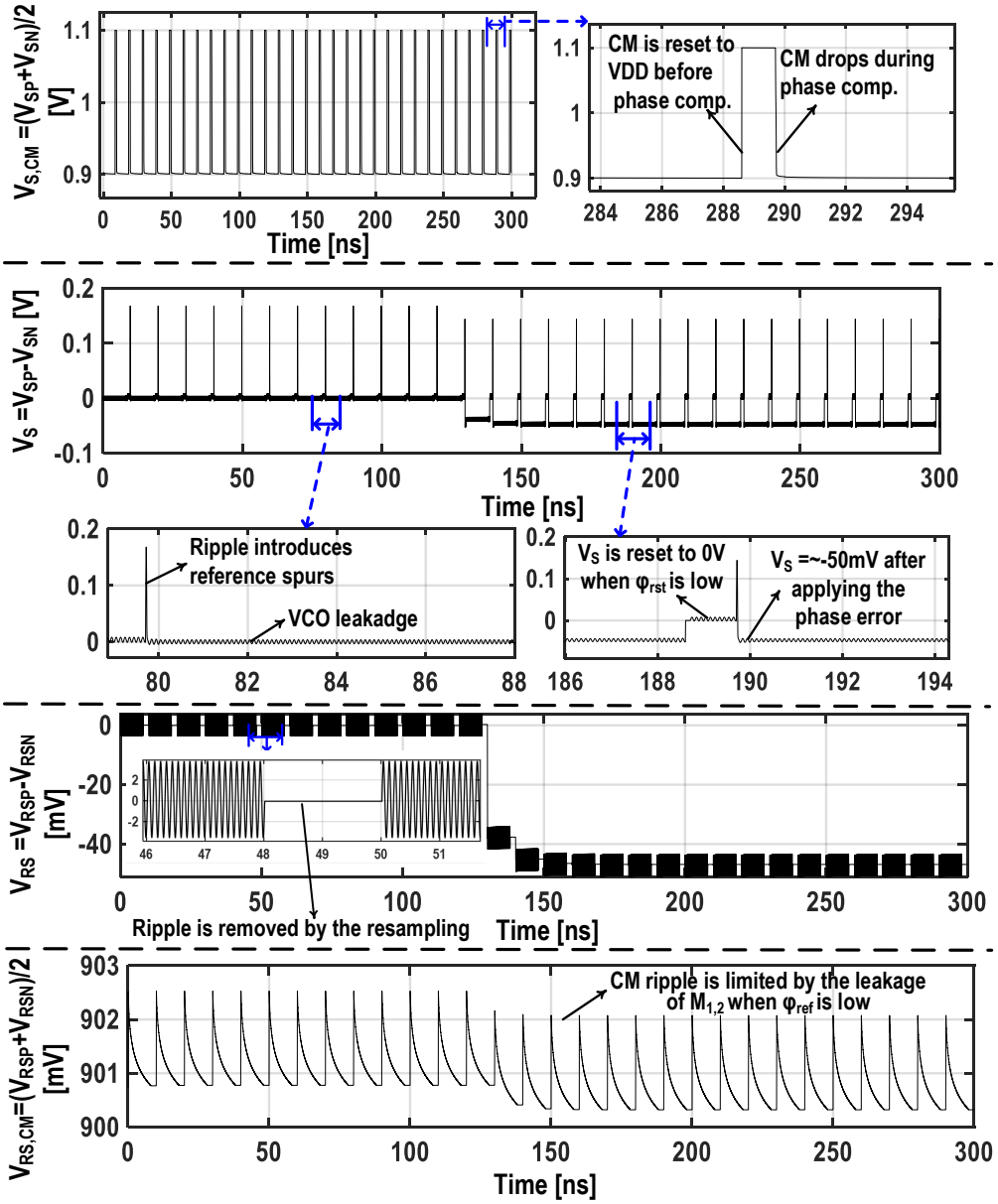

Figure 6.4: Simulated DAPD's transient response to a 5° input phase step and its steady-state waveforms at 300 K.

6.3.4 Phase-Noise Analysis

6.3.4.1 Noise of Reset Switches

When the reset switches $S_{2,3}$ are turned on, the voltage noise on C_S from the previous operation is cleared. However, the on-resistance of $S_{2,3}$ (R_{ON}) generates noise, which is held on C_S until the next reset occurs. By ignoring the pole formed by C_{RS} and $S_{4,5}$, the reset noise at the sampler output is

$$\frac{\overline{v_{n,rst}^2}}{\Delta f}(f) = \frac{2(1-\alpha)\cdot 4KTR_{ON}}{1+(2\pi f R_{ON}C_S)^2} + \frac{2\alpha^2\cdot 2KT}{C_S F_{REF}}\mathrm{sinc}\left(\frac{\alpha\pi f}{F_{REF}}\right)^2, \tag{6.9}$$

where α is the duty cycle of φ_{rst} [180]. In a DAPD, α is ∼1, and the low-frequency noise can be estimated by

$$\frac{\overline{v_{\mathrm{n,rst}}^2}}{\Delta f}(f) \approx \frac{4\mathrm{KT}}{\mathrm{C_S F_{REF}}}. \tag{6.10}$$

Notice that (6.10) slightly overestimates the reset noise held on $\mathrm{C_S}$, as part of it is discharged during the phase-detection mode due to the finite output impedance of $\mathrm{M_{1,2}}$.

6.3.4.2 Noise of Transconductors

During the phase-detection mode, $\mathrm{M_{1,2}}$ inject noise current pulses into $\mathrm{C_S}$, creating a voltage noise held there until the next reset occurs. The sampled voltage noise due to $\mathrm{M_{1,2}}$ can be expressed as

$$\frac{\overline{v_{\mathrm{n}}^2}}{\Delta f}(f) = \sum_{k=-\infty}^{+\infty} |\mathrm{H_w}(f - \mathrm{k}\cdot\mathrm{F_{REF}})|^2 \cdot \mathrm{S_i}(f - \mathrm{k}\cdot\mathrm{F_{REF}}), \tag{6.11}$$

where $\mathrm{H_w}(f)$ is the transfer function of the windowed-current integration process, and $\mathrm{S_i}(f)$ is the power spectral density (psd) of the devices' current noise [181]. $\mathrm{H_w}(f)$ can be found as

$$\mathrm{H_w}(f) = \frac{1}{\mathrm{C_S}} \cdot \mathrm{T_P} \cdot \mathrm{sinc}(\pi f \mathrm{T_P}). \tag{6.12}$$

Suppose that $\mathrm{M_{1,2}}$ only generate white noise (e.g., thermal noise and shot noise). The low-frequency noise can be found by calculating the running sum of (5.6), and can be estimated by

$$\frac{\overline{v_{\mathrm{n,white}}^2}}{\Delta f}(f) \approx 2 \cdot \frac{\overline{i_{\mathrm{n,white}}^2}}{\Delta f} \cdot \frac{1}{\mathrm{C_S^2}} \cdot \frac{\mathrm{T_P}}{\mathrm{F_{REF}}}, \tag{6.13}$$

where $\overline{i_{\mathrm{n,white}}^2}/\Delta f$ is the psd of $\mathrm{M_{1,2}}$'s white noise and can be found from (3.4). If $\mathrm{M_{1,2}}$ contain only flicker noise with a psd of $\overline{i_{\mathrm{n,fl}}^2}/\Delta f$, the running sum of (6.11) gives

$$\frac{\overline{v_{\mathrm{n,fl}}^2}}{\Delta f}(f) \approx 2 \cdot \frac{\overline{i_{\mathrm{n,fl}}^2}}{\Delta f} \cdot \frac{1}{\mathrm{C_S^2}} \cdot \frac{\mathrm{T_P}}{\mathrm{F_{REF}}} \cdot \frac{\mathrm{T_P}}{\mathrm{T_{REF}}} = 2 \cdot \frac{\overline{i_{\mathrm{n,fl}}^2}}{\Delta f} \cdot \frac{\mathrm{T_P^2}}{\mathrm{C_S^2}}. \tag{6.14}$$

6.3.4.3 Noise of Other Components

Compared with $M_{1,2}$ noise, the noise of the tail switch S_1 can be safely ignored since the on-resistance of S_1 is designed to be $\ll 1/G_M$ to ensure a fast turn ON of $M_{1,2}$. The resampling switches $S_{4,5}$ also generate noise, and the resulting voltage noise at the DAPD output can be estimated as $4KT/(C_{RS}F_{REF})$. A large C_{RS} can be used to reduce the resampling noise without affecting K_{PD}. However, C_S and C_{RS} form a discrete-time low pass filter, degrading the phase margin if C_{RS} is too large. This issue will be resolved in Section 6.4.

6.3.4.4 In-band PN due to DAPD

The in-band PN due to DAPD ($\mathcal{L}_{DAPD}$) is obtained by referring the sampled voltage noise to the input of the DAPD.

$$\mathcal{L}_{DAPD} \approx \frac{(4KTC_S + \overline{\frac{i^2_{n,white}}{\Delta f}} \cdot 2T_P + \overline{\frac{i^2_{n,fl}}{\Delta f}} \cdot 2F_{REF}T_P^2)}{F_{REF}C_S^2K_{PD}^2}. \tag{6.15}$$

Since K_{PD} is proportional to $1/C_S$, the reset noise contribution to $\mathcal{L}_{DAPD}$ is proportional to C_S, indicating that a small C_S helps to improve the in-band PN. By contrast, the in-band PN of a CSPD is not a function of C_S [149]. Hence, a very large C_S is typically used to reduce the DM ripple in a CSPD [149]. Fig. 6.5 (a) and (b) respectively depict the simulated and calculated $\mathcal{L}_{DAPD}$ versus C_S and T_P at a 300 kHz offset from a 10 GHz carrier when $(W/L)_{1,2} = 1.2\mu m/40nm$. Simulations match very well with the presented theory. As expected, $\mathcal{L}_{DAPD}$ is dominated by the reset noise if a large C_S is used since $\mathcal{L}_{DAPD}$ contributed by both the flicker and thermal noise of $M_{1,2}$ is not a function of C_S. In addition, by varying T_P, the individual contribution of each noise source to $\mathcal{L}_{DAPD}$ also varies. Nevertheless, $\mathcal{L}_{DAPD}$ is still below -130 dBc/Hz and varies less than 2 dB when T_P is within 0.2-to-0.5 T_{VCO}.

Fig. 6.5 (c) and (d) show the simulated $\mathcal{L}_{DAPD}$ at 4.2 K due to DAPD's white noise[1] versus C_S and T_P, respectively. Thanks to the temperature reduction, the PN contributed by the thermal noise of reset switches and $M_{1,2}$ is reduced dramatically. However, the temperature-independent shot noise

[1]The flicker noise is not included in those simulations due to the lack of device model.

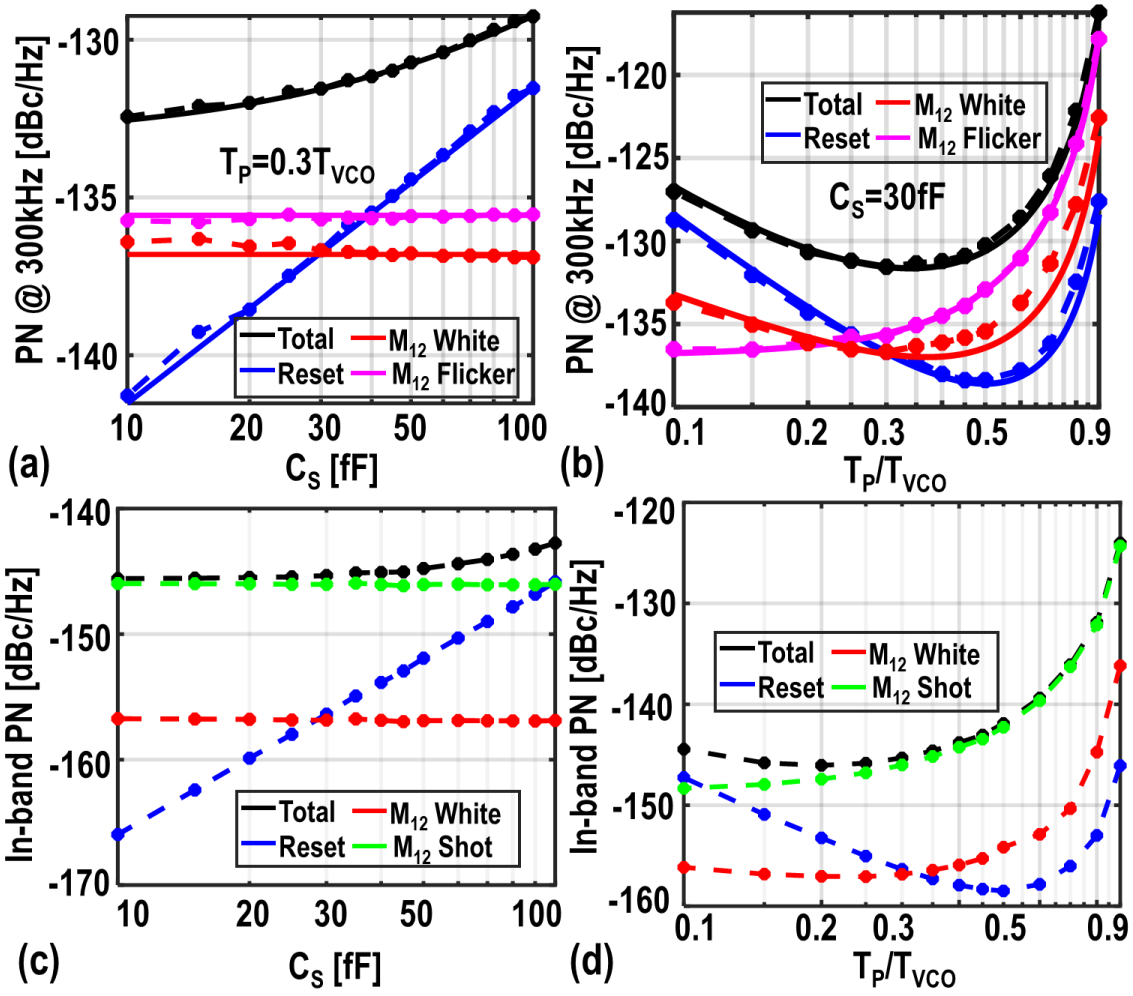

Figure 6.5: Simulated and calculated PN at a 300 kHz offset from a 10 GHz carrier versus (a) C_S and (b) T_P at 300 K; simulated in-band PN due to DAPD's white noise versus (c) C_S and (d) T_P at 4.2 K.

limits the final PN improvement to ∼10 dB[1].

6.3.5 Mismatch and P_{DC} Analysis

The DAPD components are subject to a large mismatch due to the use of small device sizes. If the VCO zero-crossings still occur at the center of the φ_{ref} pulse, then a non-zero V_S will be created due to the mismatch of C_S and G_M. This implies that the PLL is not locked. Hence, the PLL must develop a static phase offset to equalize V_{SP} and V_{SN} by shifting the locking point away from the ideal point. After the resampling, V_{RSP} and V_{RSN} are still ideally constant. Hence, the mismatch of DAPD components do not degrade

[1]If the flicker noise is considered to be temperature-independent in the process we used, the final PN improvement is estimated to be within 6 dB.

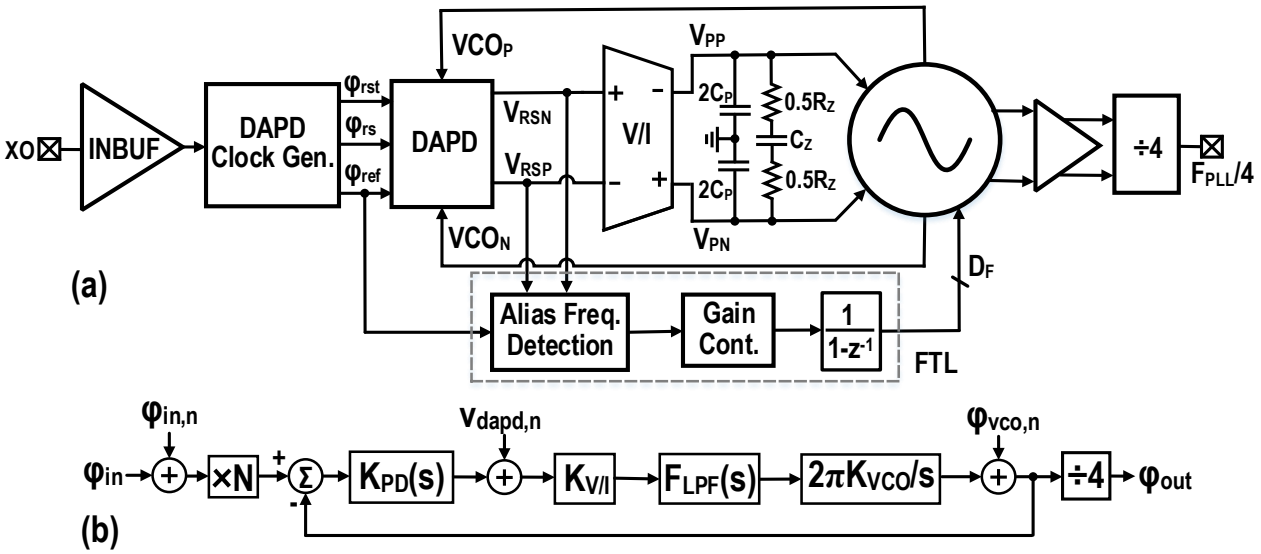

Figure 6.6: (a) Block diagram and (b) phase-domain model of the cryo-CMOS analog DAPLL with noise sources of interest.

S_{REF}. On the contrary, the C_S mismatch in a CSPD [149] does not change the locking point but increases S_{REF}.

The DAPD mainly dissipates dynamic current when charging C_S during φ_{rst}. The P_{DC} of the DAPD core could be estimated by

$$P_{DC,DAPD} \approx 2 \cdot C_S \cdot F_{REF} \cdot \frac{G_M V_{GT} T_P}{C_S} \cdot V_{DD}, \tag{6.16}$$

where V_{GT} is the overdrive voltage of $M_{1,2}$. The resulting P_{DC} is less than 2μW by considering $F_{REF} = 100\,\text{MHz}$ and $V_{GT} = 0.25\,\text{V}$.

6.4 Cryo-CMOS Analog DAPLL

6.4.1 System Overview

The block diagram of the proposed cryo-CMOS dynamic-amplifier-based sub-sampling PLL (DAPLL) is shown in Fig. 6.6 (a). An input buffer (INBUF) is used to reshape the external 100-MHz sinusoidal reference clock into a steep square wave. The required clock pulses (φ_{rst}, φ_{rs}, and φ_{ref}) for a proper operation of the DAPD are derived from a clock generation circuit. The DAPD directly senses the phase error between the VCO and φ_{ref} without any isolation buffers, and outputs a very stable voltage. A fully-differential V/I stage (based on a folded-cascode operational transconductance amplifier) and a passive

loop filter are then used to generate a tuning voltage for the fine frequency control. An on-chip divide-by-4 circuit based on the static current-mode-logic (CML) latch is designed to ease the cryogenic measurements.

To avoid locking to a wrong harmonic, the VCO's frequency is manually tuned within $\pm 0.5 F_{REF}$ of the desired frequency at power ON. Afterward, the VCO's frequency is kept close to the lock-in range of the PLL by a frequency-tracking loop (FTL) similar to that in [150], which is running in the background to correct the frequency error introduced by a sudden frequency disturbance on the VCO.

As shown in Fig. 6.6 (b), a linear phase-domain model of the DAPLL is developed to predict the loop dynamics and PN performance at 4.2 K. Here, $F_{LPF}(s)$ and K_{VCO} respectively represent the transfer function (TF) of the loop filter and VCO tuning gain. A damping factor of ∼1.6 is selected in this design to guarantee the PLL's stability at CT. By considering the zero-order hold effect and ignoring the sinc-type response introduced by the windowed-current integration, the s-domain K_{PD} can be estimated by

$$K_{PD}(s) \approx K_{PD} \cdot \frac{1 - e^{-sT_{REF}}}{sT_{REF}}. \tag{6.17}$$

6.4.2 Dynamic-Amplifier-Based Phase Detector

The periodic switching of C_{RS} in Fig. 6.2 injects charge to the VCO through the C_{gd} of $M_{1,2}$, degrading S_{REF}. As depicted in Fig. 6.7 (a), a two-stage cascaded DA is thus employed before the resampling stage to achieve better isolation between the VCO and C_{RS}. The S_{REF} due to φ_{rst} switching can be minimized by narrowing down the duty cycle of φ_{rst}. To accommodate the transconductance variation of M_{1-4} at 4.2 K, K_{PD} can be digitally regulated by sampling capacitors C_{S1} and C_{S2}. $M_{1,2}$ are sized with a minimum channel length and a small width to reduce the modulated capacitance seen by the VCO tank and optimize S_{REF}. A high K_{PD} of the first stage DA (∼0.6 V/rad) ensures that the in-band PN contributed by $M_{1,2}$ is very low [see (5.18)]. However, such a high K_{PD} introduces a large loop gain for the PLL. Hence, the resulting loop is difficult to stabilize without using a large loop filter capacitor. To this end, the second stage is sized with a low gain by choosing a large C_{S2} to optimize the overall K_{PD}. A large C_{S2} also helps to preserve

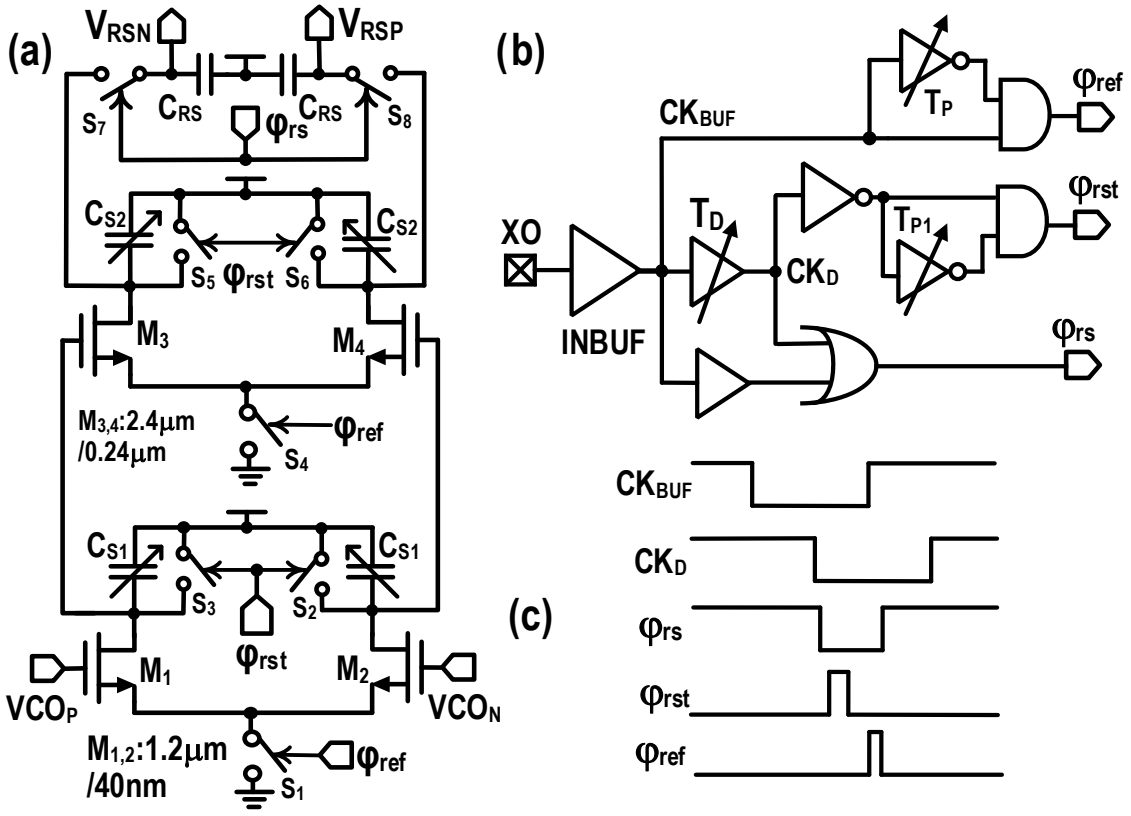

Figure 6.7: Schematics of the (a) DAPD and (b) its clock generation; (c) timing diagram of the DAPD

a high common-mode voltage at the second-stage DA output. Hence, the resampling switches $S_{7,8}$ can have enough voltage headroom, thus leading to low on-resistance at CT. Due to the good isolation offered by $M_{1,2}$ between the VCO and second stage DA, $M_{3,4}$ are up-sized with a channel length of 240 nm to reduce their shot noise and flicker noise at CT without penalizing S_{REF}.

Notice that the charge transfer between C_{S2} and C_{RS} forms a discrete-time low-pass filter. Thus, C_{RS} should be minimized to preserve a high phase margin of the PLL. Fortunately, by choosing $C_{RS} = C_{S2}/4$, the resulting phase margin degradation is within 14° for a 4-MHz PLL bandwidth. Thanks to the high gain of the first stage, the simulated noise contribution due to resampling switches $S_{7,8}$ at 300 K is less than 10% of the total noise. At 300 K, the simulated PN floor due to DAPD is -128 dBc/Hz when referred to a 10-GHz carrier, in which the first and second stage DA shows a similar contribution. By considering $T_{ch} = 4.2$ K due to the DAPD's low P_{DC} ($<10\,\mu$W), the estimated PN floor is expected to be ∼-137 dBc/Hz, dominated by the first stage DA's shot noise.

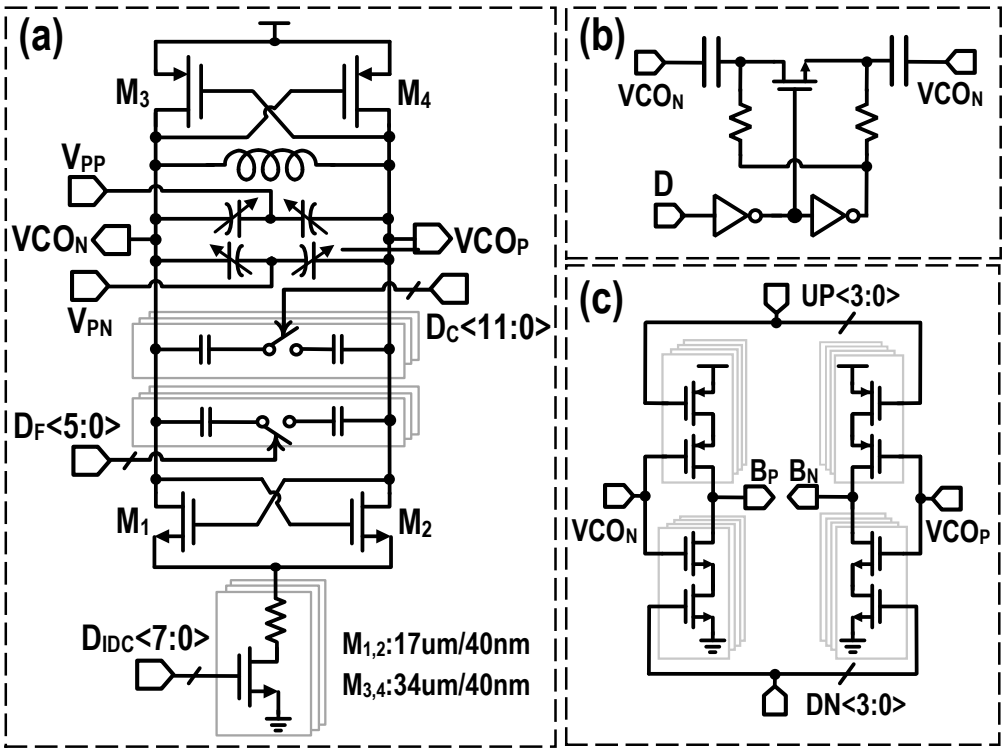

Figure 6.8: Schematics of the (a) VCO, (b) VCO capacitor bank unit, and (c) VCO buffer.

6.4.3 DAPD Clock Generation

Fig. 6.7 (b) and (c) show the schematic and timing diagram of the DAPD clock generation, respectively. Notice that, in theory, the DAPD output is only determined by φ_{ref}. The clock jitter of φ_{rst} and φ_{rs} thus has a minor impact on DAPD's PN. Therefore, the clock generation circuits of φ_{rst} and φ_{rs} can be designed with low power. φ_{ref} is generated by a pulse generator, which is derived from the rising edge of the buffered XO output. At RT, the simulated PN floor of the INBUF is -161 dBc/Hz. By considering $T_{\mathrm{ch}} = 4.2\,\mathrm{K}$, the PN floor is dominated by the shot noise and is limited to -167 dBc/Hz. Compared with RT, T_{P} is expected to reduce by ∼30% at 4.2 K, degrading K_{PD} moderately by <10%. To generate φ_{rst} and φ_{rs}, an intermediate clock (CK_{D}) is generated by delaying CK_{BUF} through a digitally-controlled delay line. Its delay (T_{D}) can be tuned from 0.6 to 3 ns to ensure that the required clock pulses can be reliably generated under PVT variations. φ_{rst}, derived from the falling edge of CK_{D}, is generated by a second pulse generator. Finally, the falling edge of CK_{D} and the rising edge of CK_{BUF} are leveraged to generate φ_{rs}.

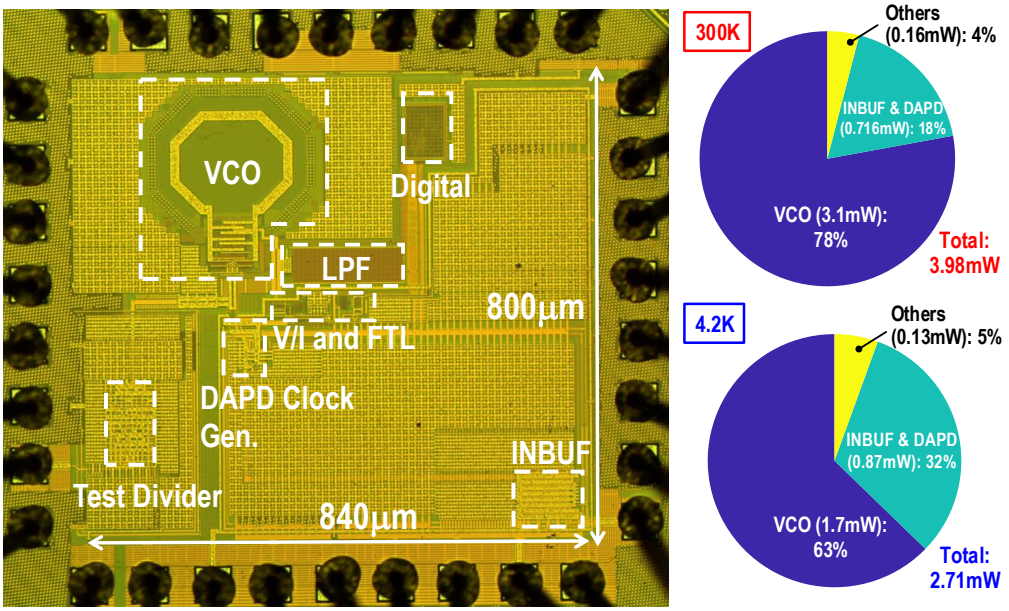

Figure 6.9: Chip micrograph and measured power breakdown of the DAPLL.

6.4.4 VCO and Its Buffer

The schematic of the LC-VCO is shown in Fig. 6.8 (a). The negative resistance is provided by a CMOS differential pair (M_{1-4}), implemented with low-threshold thin-oxide devices. The excess gain (G_X) of the VCO is designed to be ~ 3 to ensure a robust start-up at RT. However, due to the significant increase of the tank's quality factor and transconductance at 4.2 K, the conversion of M_{1-4}'s device flicker noise to PN can be severely degraded due to the increased G_X [182]. An 8-bit digitally controlled tail-resistor bank is thus used to optimize G_X and PN at 4.2 K. This resistor bank also helps to adjust the VCO swing and thus optimize K_{PD} over the PLL tuning range. In a future design, an amplitude calibration technique [183] could be used to stabilize the VCO swing across the band of operation without incurring extra P_{DC}. Due to the dramatic reduction of the PN in the thermal region and limited improvement of the PN in the flicker region, the VCO would exhibit a very high flicker corner (e.g., a few MHz) at 4.2 K. Yet, the flicker-corner issue could be partially mitigated by using a large DAPLL loop bandwidth. The VCO can be fine-tuned by two differential accumulation-mode varactors, and its coarse frequency tuning is realized by a switched capacitor bank, whose unit cell schematic is shown in Fig. 6.8 (b). A DC-coupled VCO buffer is used to drive the test divider as shown in Fig. 6.8 (c).

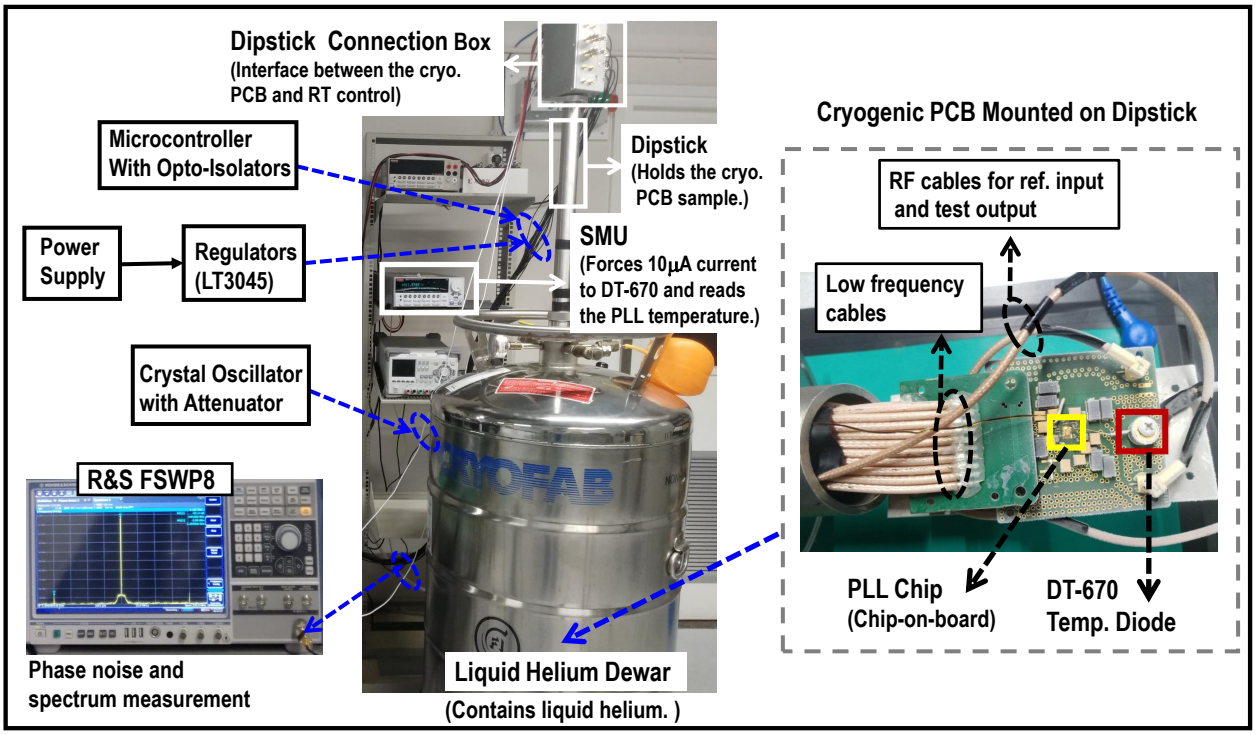

Figure 6.10: Cryogenic measurement setup.

6.5 Measurement Results

The DAPLL has been fabricated in a standard 40-nm bulk CMOS process. Fig. 5.16 shows the chip micrograph and the measured power breakdown. The core area of the chip is $\sim$0.14 mm^2. Since the divider consumes a high P_{DC} to minimize its PN and drive the long cables used in the cryogenic setup, the PLL core components could heat up beyond 100 K [113]. To mitigate this issue, the test divider is placed physically far away ($\sim 200\,\mu$m) from the PLL in the layout. The DAPLL's performance has been characterized over a wide temperature range from 300 K to 4.2 K. To measure the DAPLL's performance under cryogenic conditions, the setup shown in Fig. 6.10 was used, where a test board with a wire-bonded chip was mounted at one end of a dipstick. The DAPLL's ambient temperature (T_{am}) can be changed by adjusting the vertical position of the dipstick placed inside a helium dewar, and monitored by a temperature diode mounted on the surface of the board close to the chip. To facilitate the measurements, the 100-MHz sinusoidal reference, power supply, and biasing were placed at RT. Since the reference signal's frequency is low, the long cable used in the measurement setup has a minor impact on its swing.

As shown in Fig. 6.9, the DAPLL dissipates $\sim$4 mW (excluding the test

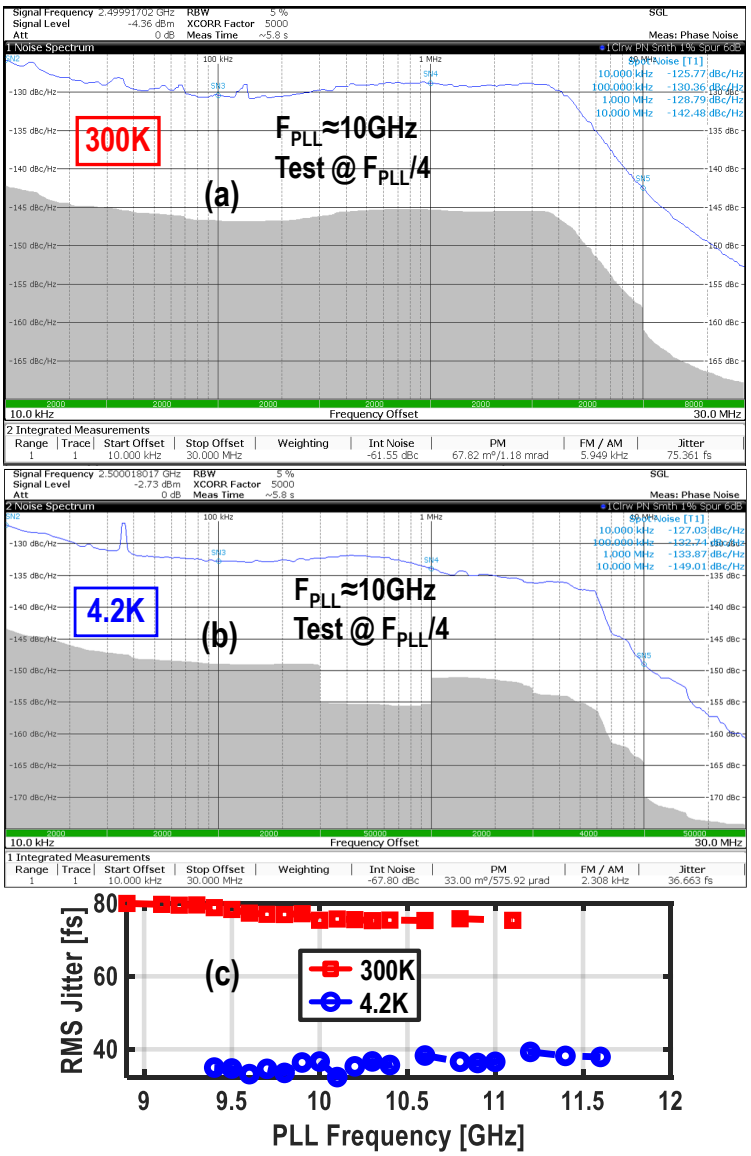

Figure 6.11: Measured PN plots at (a) 300 K and (b) 4.2 K after an on-chip divide-by-4; (c) RMS jitter at 300 K and 4.2 K over the PLL tuning range.

divider but including the on-chip input buffer) from a 1.1-V power supply at 300 K. When the chip is cooled down to 4.2 K, the P_{DC} of the DAPLL is reduced to 2.7 mW under the same supply. This is mainly because the VCO requires less current to deliver the same swing due to the increased tank quality factor at 4.2 K. The DAPLL can cover an output frequency range of 8.9–11.1 GHz and 9.4–11.6 GHz at 300 K and 4.2 K, respectively. The slightly increased output frequency at 4.2 K is mainly due to the reduction of the VCO LC tank's inductance and parasitic capacitance to the substrate.

Fig. 6.11 (a) shows the measured PN plot at 300 K from an R&S FSWP8 PN analyzer, where the PLL is running at 10 GHz. An in-band PN floor of -

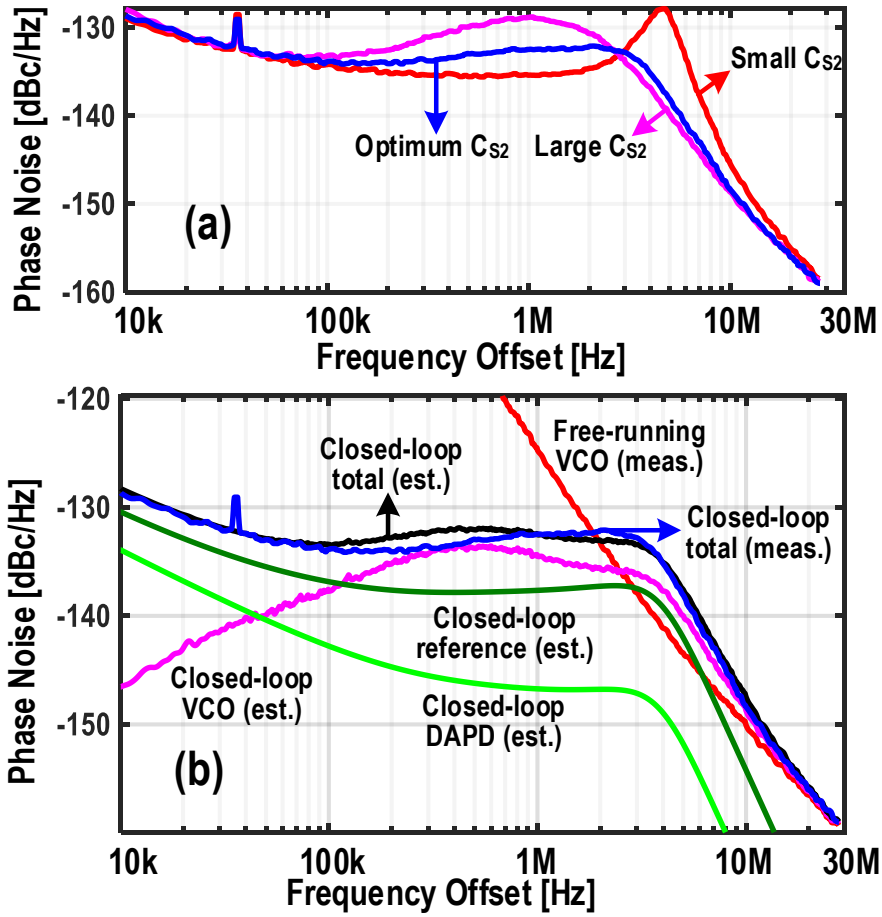

Figure 6.12: (a) Measured PN profiles by varying C_{S2} at 4.2 K and (b) estimated PN profiles in comparison with the measurement at 4.2 K.

130 dBc/Hz has been achieved at the 2.5-GHz divided output, limited by the on-chip INBUF. The measured RMS jitter and integrated phase noise (from 10 kHz to 30 MHz) excluding reference spurs are ∼75 fs and -49.5 dBc, respectively, corresponding to a PLL jitter-power FOM of -256.5 dB. Fig. 6.11 (b) shows the measured PN plot at 4.2 K after re-optimizing the loop parameters to improve the fidelity. The measured RMS jitter and integrated phase noise are dramatically reduced to 37 fs and -55.8 dBc, respectively. The estimated control fidelity is 99.9994% (99.9998%) for a 1-MHz (10-MHz) f_R, thus satisfying the requirements of LO generation for QC applications. Fig. 6.11 (c) shows the measured RMS jitter over the tuning range at 4.2 K and 300 K. In each measurement point, the VCO's frequency was initially calibrated within the PLL's locking range by adjusting the VCO's switched capacitor at power ON. Then, the PLL locks the phase of the VCO to the reference. Compared with 300 K, the measured RMS jitter improves nearly by 2× due to the noise reduction at 4.2 K.

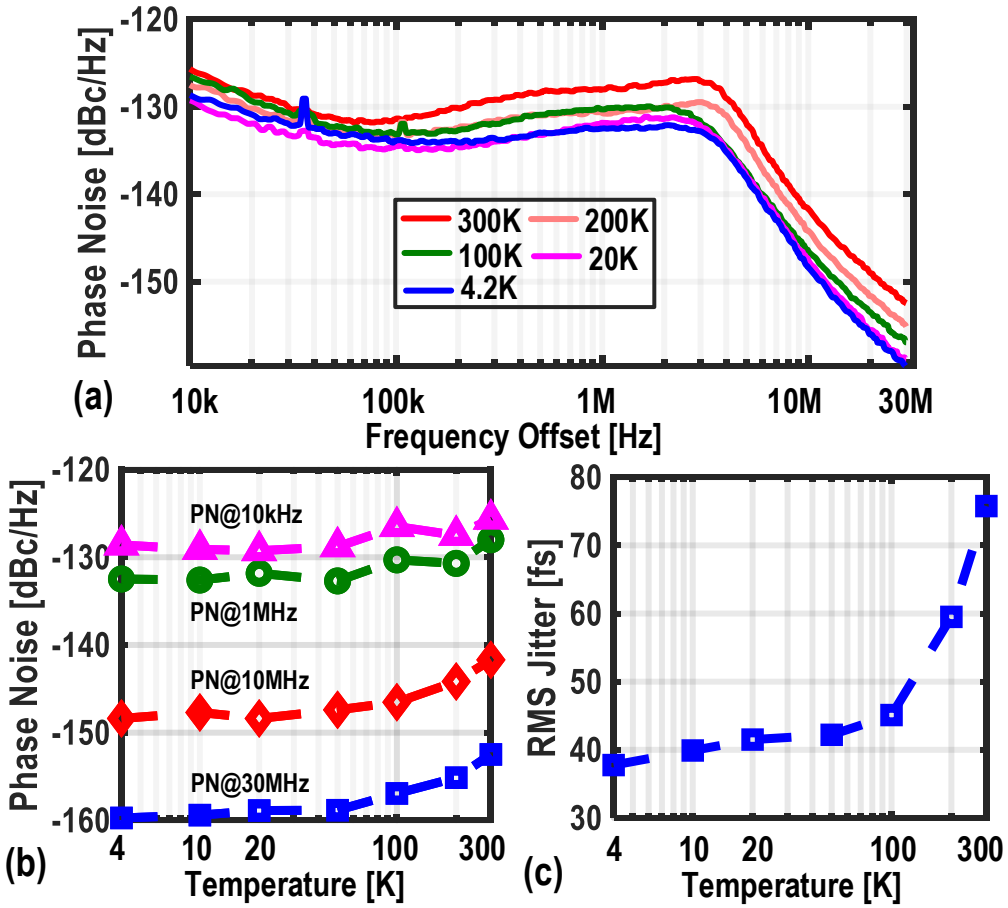

Figure 6.13: (a) Measured PN profiles, (b) spot noise, and (c) RMS jitter over the temperature.

Fig. 6.12 (a) depicts three measured PN plots based on different C_{S2} settings while keeping other loop parameters fixed at 4.2 K, where the PLL is running at 10.8 GHz. As expected, the K_{PD} and hence the PLL loop gain become too large when a very small C_{S2} is used, resulting in a wide loop bandwidth and jitter peaking. However, when a very large C_{S2} is used, K_{PD} and the PLL loop gain are reduced, leading to less filtering of the VCO's PN due to a narrow bandwidth. Based on the phase-domain model and the estimated PN of the DAPD and INBUF discussed in Section 6.4, the model-predicted PN is compared with a measured PN profile at 4.2 K [see Fig. 6.12 (b)]. The measured output PN in blue matches well with the estimated noise profile in black. Below 100 kHz, the in-band PN is dominated by the flicker noise of the input buffer. From 100 kHz to 4 MHz, the in-band PN is limited by the filtered flicker PN of the VCO and shot PN of the input buffer. The flicker PN of the VCO could be better suppressed by the PLL if a lower damping factor was selected, at the cost of worse loop stability.

Fig. 6.13 (a) and (b) respectively show the measured PN profiles and

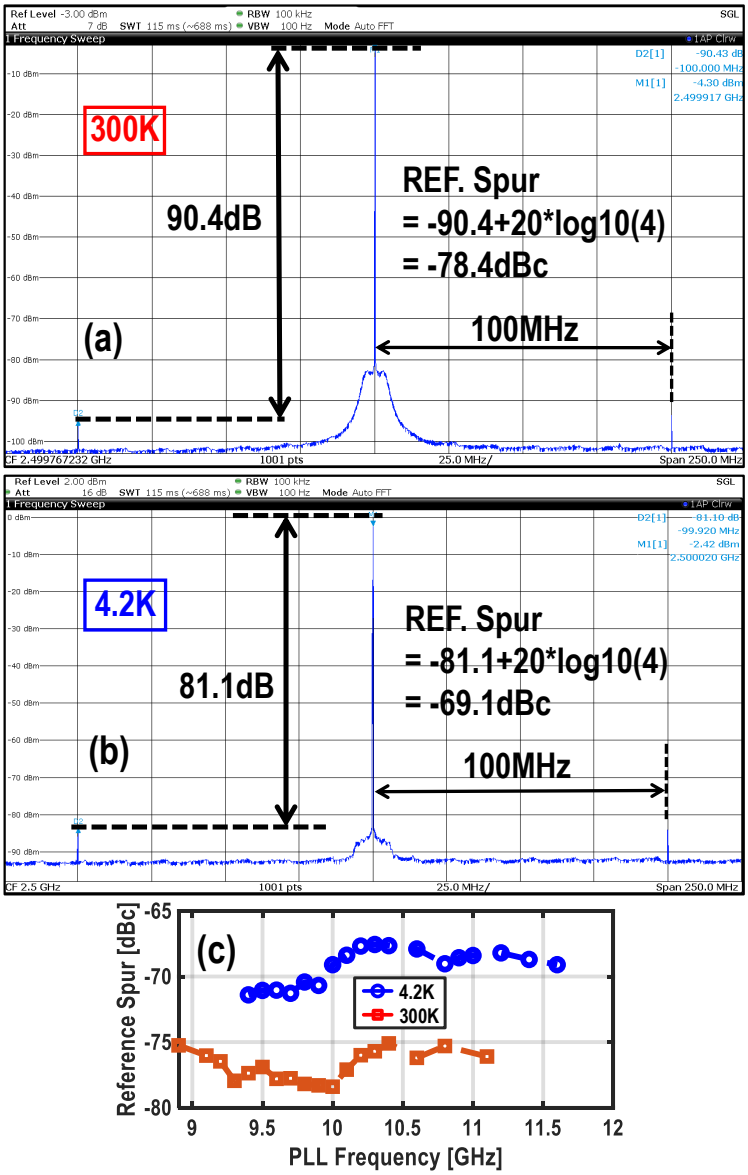

Figure 6.14: Measured spectrum at (a) 300 K and (b) 4.2 K after an on-chip divide-by-4; (c) S_{REF} at 300 K and 4.2 K over the PLL tuning range.

spot noise over T_{am} after re-optimizing the jitter performance. The PN at 10 MHz and 30 MHz offsets improve substantially (∼5 dB) from 300 K to 100 K. However, it reduces moderately (<3 dB) by further going from 100 K to 4.2 K. This is because, above 100 K, self-heating of the VCO can be safely ignored as the increase of channel temperature (ΔT_{ch}) is expected to be within $0.1\times T_{am}$ (i.e., $T_{ch} \approx T_{am}$) [113]. Hence, the measured PN in the VCO's thermal region improves significantly due to reduced channel noise and increased quality factor. Below 100 K, the VCO suffers from severe self-heating, resulting in $T_{ch} \gg T_{am}$ [113]. In addition, as thermal noise reduces, the shot noise cannot be ignored. The combination of self-heating and shot noise results in a minor

PN improvement below 100 K. Moreover, the measured PN at a 10 kHz offset improves merely ∼3 dB from 300 K to 4.2 K. This is likely due to the fact that the PN in the flicker region of the input buffer is not a strong function of T_{ch}. Furthermore, the improvement of PN at a 1 MHz offset is ∼5 dB from 300 K to 4.2 K, limited by both the shot and flicker noise of the VCO. Consequently, while the measured RMS jitter improves significantly from 75 fs to 45 fs by going from 300 K to 100 K, the jitter improvement is limited to merely 1.5 dB when T_{am} is further reduced from 100 K to 4.2 K [see Fig. 6.13 (c)].

Fig 6.14 (a) and (b) respectively show the measured spectrum at 300 K and 4.2 K, where the DAPLL was running at 10 GHz for both temperatures. At 300 K, the measured S_{REF} at the divide-by-4 output is -90.4 dBc, which increases to -78.4 dBc when referred to the 10-GHz PLL frequency. The measured S_{REF} becomes -69 dBc at 4.2 K, probably due to cryogenic measurement constraints (e.g., coupling between dense cables). While the measured S_{REF} is degraded at 4.2 K, the target specification of -54 dBc is satisfied with >10 dB margin over the PLL tuning range as shown in Fig 6.14 (c). The measured reference spur (< -67.5 dBc) is well below the integrated phase noise (∼ -55.8 dBc), which degrades the RMS jitter by < 1.5 fs.

Table 6.2 compares the performance of the presented DAPLL with the state-of-the-art. At 300 K, the FOM and S_{REF} achieved in this work are very competitive. By moving to 4.2 K, our FOM improves by ∼8 dB, outperforming the room temperature prior art. Compared with the cryo-CMOS PLL presented in [66], our FOM improves by more than 15 dB. Moreover, this work is the first cryo-CMOS PLL operating at 4.2 K, and meets the specification requirements of LO generation for QC applications.

6.6 Conclusion

A cryo-CMOS PLL for qubit control is presented. An analog charge-domain sub-sampling PLL structure is selected to benefit more from noise reduction from 300 K to 4.2 K. A DAPD is proposed to simultaneously achieve low spur and low jitter. The K_{PD} and PN of the DAPD are analyzed in depth. Design considerations of the PLL for cryogenic operation are also analyzed. At 300 K, the PLL achieves 75-fs RMS jitter and 4-mW P_{DC} at 10 GHz, leading to a -256.5-dB PLL jitter-power FOM, while maintaining

-78.4-dBc S_{REF}. At 4.2 K, the PLL achieves an RMS jitter of 37 fs and an S_{REF} of -69 dBc, while consuming 2.7 mW. The proposed cryo-CMOS PLL meets the performance requirements for the qubit control, which marks a major step toward a fully-integrated qubit controller.

Table 6.2: Comparison with state-of-the-art.

	This Work		**K. Kang JSSC'22**	**T. Liu TCAS-I'17**	**J.-H. Seol JSSC'21**	**J. Gong JSSC'21**	**Z. Zhang JSSC'20**	**D.-G. Lee JSSC'20**	**M. Mercandelli ISSCC'20**	**A. Santiccioli ISSCC'20**	**H. Zhang VLSI'19**
PLL Architecture	**DAPLL**		DPLL	Charge-Pump PLL	Reference Oversamp. PLL	Charge-Sampling PLL	Sub-Sampling PLL	Sub-Sampling PLL	Sampling PLL	Bang-Bang PLL	Injection-Locked PLL
Power Supply [V]	**1.1**		1.05	1.2	NA	1.1/0.6	0.65	1	0.9	0.9	**0.14
Temperature [K]	**4.2**	**300**	3.5	77	300	300	300	300	300	300	300
F_{REF} [MHz]	**100**		500	NA	200	100	200	100	500	500	100
F_{PLL} [GHz] **FTR [GHz]**	**10** **9.4-11.6**	**10** **8.9-11.1**	12.16 9-13	2.5 2.22-3.6	4 (NA)	11.2 9.8-12.2	14 12-16	2.4 NA	12.5 11.9-14.1	13.5 12.8-15.2	2.4 2.2-2.6
REF. Spur [dBc]	**-69.1**	**-78.4**	NA	NA	-78.1	-77.3	-64.6	-67	-73.5	-80.1	-66.5
RMS Jitter, σ_j [fs] **[Int. Bandwidth]**	**36.7** **[10k-30MHz]**	**75.3** **[10k-30MHz]**	115 [100Hz-20MHz]	420 NA	67.1 [10k-100M]	48.6 [1k-100MHz]	56.4 [1k-100MHz]	161 [10k-100M]	***51.7 [1k-100MHz]	***58.9 [1k-100MHz]	298 [0.1k-100M]
Power, P_{DC} [mW]	**2.7**	**4**	12.5	8.5	5.2	5	7.2	0.9	18	19.8	0.17
***FOM [dB]**	**-264.4**	**-256.5**	-247.8	-238.3	-256.3	-259.2	-256.4	-256.3	-253.2	-251.6	-258.2
Core Area [mm^2]	**0.14**		0.068	0.08	0.17	0.13	0.234	0.42	0.16	0.17	0.23
Process [nm]	**40**		40	65	28	40	40	65	28	28	65

*FOM = $20*\log_{10}(\sigma_j/1s) + 10*\log_{10}(P_{DC}/1mW)$ ** For the VCO only (supply of the rest circuit is not reported.) ***Jitter of a fractional-N PLL (measured in an integer-N channel)

Chapter

7

An Octave PLL with a Dual-Core Triple-Mode VCO

Chapters 5 and 6 introduced two cryo-CMOS phase-locked loops (PLLs) with a narrow frequency-tuning range (FTR). However, in order to directly support both spin qubits and superconducting qubits, it is desired that a single PLL can cover an octave FTR. This chapter presents a wide FTR and low-jitter PLL by utilizing a compact dual-core triple-mode voltage-controlled oscillator (VCO) and a dynamic-amplifier-based phase detector (DAPD)[1].

Fabricated in a 22-nm FinFET CMOS process, the PLL covers an FTR of 7.1-16.8 GHz and achieves better than 80-fs RMS jitter across the whole FTR at 300 K. Compared with the prior art VCOs at a similar frequency range, this work improves the area normalized figure of merit (FOM_A) by > 3.3 dB without sacrificing the tuning-range normalized figure of merit (FOM_T). Thanks to the proposed compact and low-power triple-mode VCO, our octave FTR PLL achieves the best figure of merit (FOM), occupies the smallest area, and uses the lowest reference frequency. By moving to 4.2 K, the PLL covers an FTR of 7.4-17.8 GHz and achieves an RMS jitter of less than 50 fs.

[1]Part of this chapter has been published in the 2022 IEEE International Solid-State Circuits Conference (ISSCC) [184].

7.1 Introduction

Modern multi-standard communication devices require a single PLL covering an octave frequency-tuning range (FTR) to minimize the cost and offer a flexible system design. In wireless transceivers, the pursuit of higher-order modulations to improve data rates and channel capacity sets increasingly stringent jitter requirements for PLLs, e.g., lower than 80-fs RMS jitter for 5G applications (see Chapter 1). Moreover, due to large out-of-band blockers, the phase noise (PN) requirements of the VCO are demanding due to reciprocal mixing. In qubit controllers of quantum computers, a cryo-CMOS PLL with low PN and a wide FTR is necessary to address various types of qubits, such as 10-20-GHz spin qubits and 4-8-GHz transmons. Apart from the FTR and PN requirements, the power consumption of this PLL must be low due to the limited cooling power of the refrigerator. In addition, the PLL's silicon area is preferred to be small for a low cost. However, there is a lack of PLLs that simultaneously meet these requirements. Consequently, this chapter focuses on developing an octave FTR, low-jitter, and area-efficient PLL operating over a wide temperature range (i.e., 4.2-300 K) for various applications, such as quantum computing, wireless/wireline transceivers, and data converter systems with programmable sampling clock frequencies.

In a high-performance and wide FTR PLL, the noise contribution of every component to the total PN should be minimized. Recent advances in PLL architectures (e.g., sub-sampling PLLs, sampling PLLs, and injection-locked PLLs) tend to make the noise of PLL's loop components, such as phase detector, loop filter, and feedback frequency divider, negligible [55, 78–80, 84, 85, 88–94, 97–99, 101, 149–152, 154, 156, 158]. The in-band PN of a PLL can be eventually limited by the external reference and its on-chip input buffer. Moreover, the jitter contributed by the input reference buffer can be designed small with a manageable power budget. Hence, eventually, the in-band PN is set by the external reference, which cannot be improved further. To optimize the jitter, the PLL loop bandwidth should be adjusted so that the VCO PN and the reference PN contribute approximately equally. Considering a fixed PN profile of the reference, the intrinsic VCO PN is very critical to reduce the PLL's output-of-band PN for a low-jitter design. While a ring oscillator offers a wide FTR with a compact chip area, its PN is poor and its maximum

operating frequency is limited. Hence, an *LC* VCO with a wide FTR is more suitable for a low-jitter, wide FTR and high-frequency PLL.

The oscillation frequency of an *LC* VCO can be expressed by

$$\mathrm{F_{OSC}} = \frac{1}{2\pi\sqrt{\mathrm{L_{eff}C_{eff}}}}, \tag{7.1}$$

where $\mathrm{L_{eff}}$ and $\mathrm{C_{eff}}$ represent the effective inductance and capacitance of the tank, respectively. Therefore, to target a wide FTR, $\mathrm{L_{eff}}$ and $\mathrm{C_{eff}}$ can be adjusted by switching a capacitor, an inductor, or a transformer. However, the switch used for frequency tuning contains parasitic capacitances ($\mathrm{C_{off}}$) in the OFF state, which limits the maximum oscillation frequency. Hence, a small switch (with small $\mathrm{C_{off}}$) is desired to avoid limiting the FTR, thus degrading the tank Q factor due to the loss of the switch. On the other hand, the PN of an *LC* VCO at a frequency offset of f can be found as

$$\mathcal{L}(f) \approx 10\log_{10}\left(\frac{\mathrm{F_N \cdot K \cdot T_{ch}}}{2 \cdot \mathrm{Q}^2 \cdot \alpha_\mathrm{I} \cdot \alpha_\mathrm{V}} \cdot \left(\frac{\mathrm{F_{OSC}}}{f}\right)^2\right), \tag{7.2}$$

with $\mathrm{F_N}$ the effective noise factor, K Boltzmann's constant, $\mathrm{T_{ch}}$ the channel temperature, α_I the current efficiency, and α_V the voltage efficiency [185]. α_I and α_V are fixed for a given VCO topology. Hence, the most straightforward method to achieve low PN is to increase the tank's Q factor, which contradicts the switch requirement for wide FTR. Consequently, it is challenging to simultaneously obtain a wide FTR and low PN due to the limited Q of the tuning capacitors and switched inductors/transformers.

To expand the FTR without degrading the tank's Q factor, multiple VCOs oscillating at different frequencies could be used and each VCO is enabled at a time. Nevertheless, integrating several VCOs into a single PLL has some limitations, such as increased die area, complicated multiplexing functions, and layout difficulty. Moreover, the PN of a single-core VCO is limited.

In recent years, multi-core mode-switching VCOs are widely used to mitigate the trade-off between the FTR and PN with a relatively small chip footprint. The PN improves linearly by in-phase coupling of N identical VCOs, and the resonant-mode switching enhances the VCO FTR without degrading the tank Q factor as no RF current ideally flows through lossy mode-selection switches. As an example, Fig. 7.1 (a) shows the schematic of a

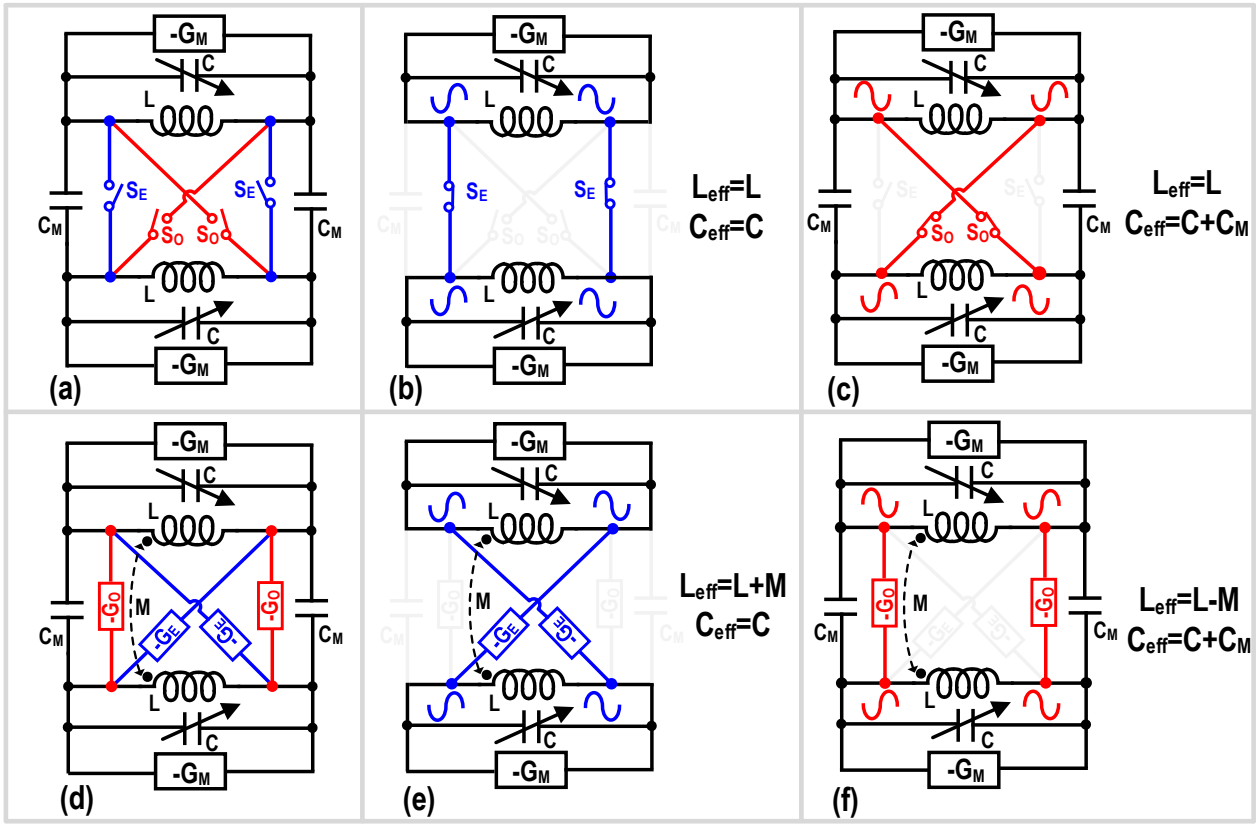

Figure 7.1: (a) Schematic and (b)-(c) detailed operation of a capacitive mode-switching VCO [28]; (d) Schematic and (e)-(f) detailed operation of a resonant mode-switching VCO [27]

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capacitive mode-switching VCO, which couples two identical VCOs through capacitors (C_M) and the mode-selection switches (S_O and S_E) [28]. As depicted in Fig. 7.1 (b)-(c), C_M can either experience a common-mode oscillation voltage (even mode) or a differential-mode oscillation voltage (odd mode) by changing the coupling polarity of C_M through S_O and S_E. The effective tank capacitance C_{eff} thus does not include C_M in the even mode but incorporates it in the odd mode. Hence, two different C_{eff} values can be synthesized to realize a dual-mode operation.

Fig. 7.1 (d) shows the schematic of a resonant mode-switching VCO, where both the tank's capacitive and inductive components can be switched [27]. By changing the coupling polarity of the two identical VCOs through the mode-selection switches (S_O and S_E) and negative transconductors (G_O and G_E), as shown in Fig. 7.1 (e)-(f), two effective tank capacitances and inductances can be synthesized to realize a dual-mode operation. In both designs, the dual-core structure theoretically reduces PN by 3 dB. In addition, the dual-mode mode-switching technique allows each mode to cover only 50% of the total

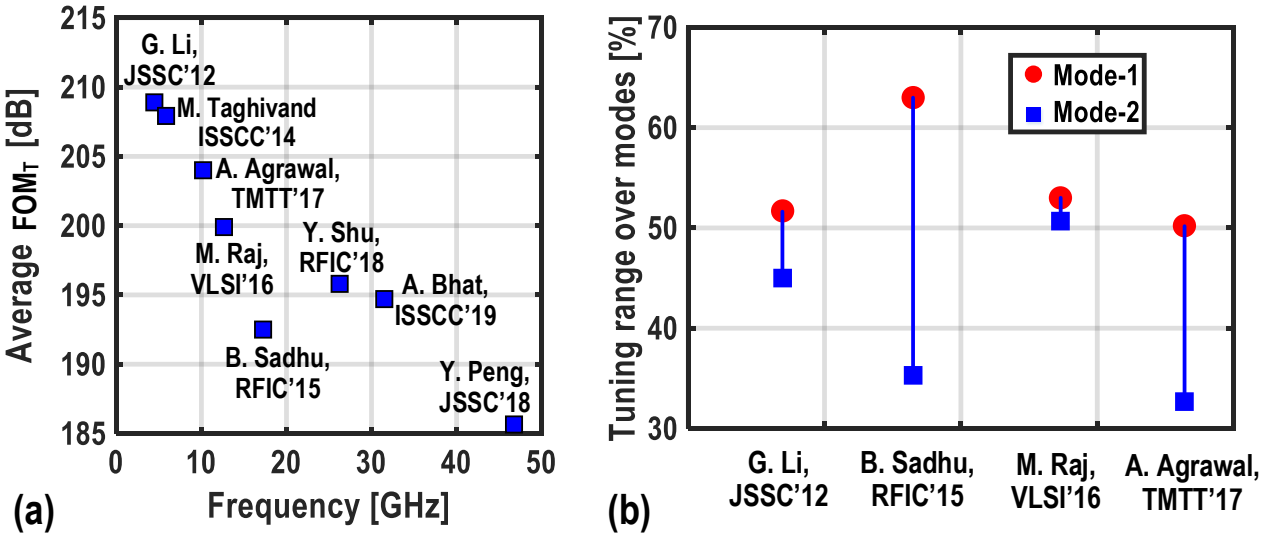

Figure 7.2: (a) Averaged FOM_T versus the oscillation frequency F_{OSC} of the prior-art dual-mode VCOs; (b) FTR of two operation modes in octave FTR VCOs.

FTR. This allows larger switches for the switched capacitor bank, leading to a higher Q and hence lower PN. Moreover, the mode-selection switches S_O and S_E ideally do not degrade PN as they conduct zero current due to a common-mode oscillation across these switches.

Fig. 7.2 (a) depicts the averaged tuning-range normalized figure of merit (FOM_T) versus the oscillation frequency F_{OSC} of the prior-art dual-mode VCOs. It suggests that the FOM_T is severely degraded as the F_{OSC} increases. Notice that the Q factor of a switched capacitor is

$$Q_{sw} = \frac{1}{2\pi R_{sw} F_{OSC} C_{eff}}, \tag{7.3}$$

where R_{sw} is the switch on-resistance. Suppose that the oscillation frequency is doubled by halving both the C_{eff} and L_{eff}. To maintain the same FTR, C_{off} must be halved by reducing the switch size, resulting in doubling R_{sw} and halving Q_{sw}. Consequently, due to the limitation of Q_{sw}, achieving a high FOM_T at higher frequencies is challenging. Moreover, Fig. 7.2 (b) shows the FTR of two operation modes in octave FTR VCOs, indicating that more than 50% FTR is still required in one resonant mode so as to cover process, voltage, and temperature (PVT) variations. Therefore, dual-mode design is not enough at higher frequencies, and it is still challenging for dual-mode VCOs to achieve a competitive FOM_T while covering an octave FTR at F_{OSC} above 6 GHz [22].

To enhance the oscillation mode, as shown in Fig 7.3 (a), a triple-mode VCO is realized by inserting an extra loop inductor (L_C) inside the main

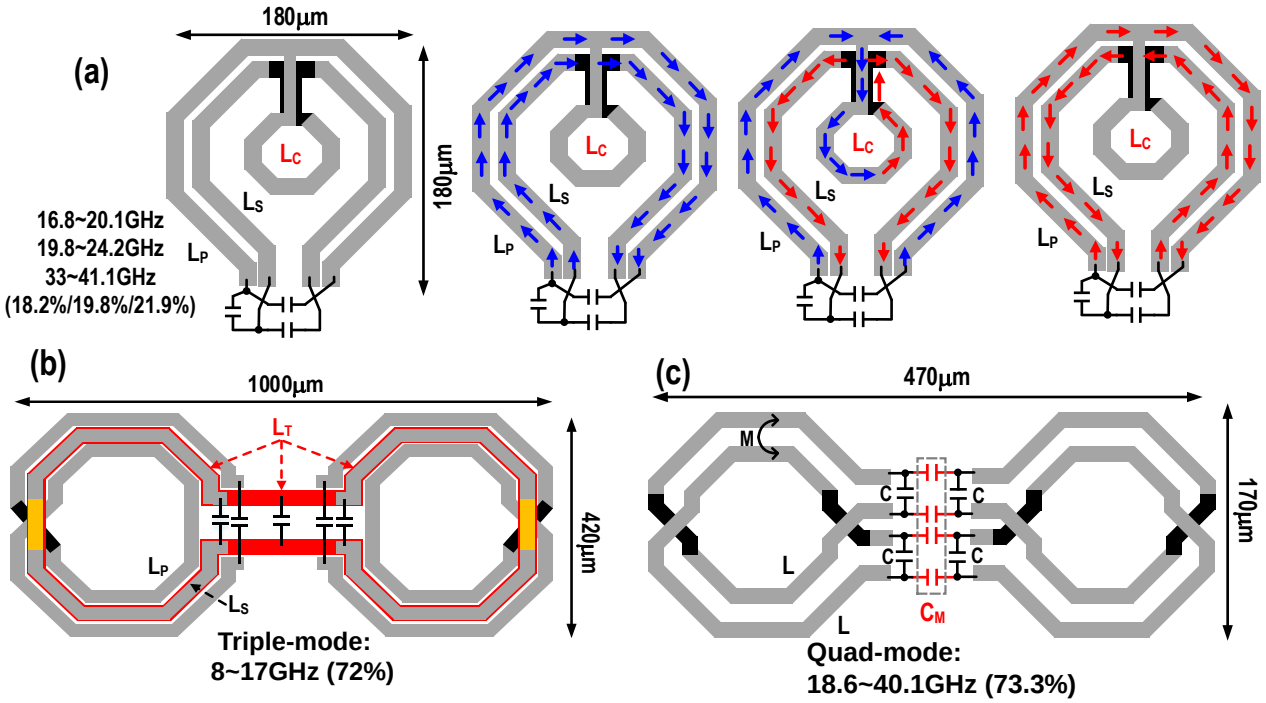

Figure 7.3: (a) Schematic and detailed operation of a triple-mode VCO [23] schematics of a (b) triple-mode [20] and (c) quad-mode [19] VCO by coupling two individual transformer-based resonators.

coupled inductors (L_P and L_S) [23]. By controlling the presence and absence of the oscillation current in the L_C and coupling directions of L_P and L_S, three effective inductance values can be synthesized. This design has a very compact chip area. However, to accommodate L_C, L_P and L_S must be strongly coupled. This leads to a substantial inductance variation over operation modes (i.e., more than 3×). Hence, a large FTR gap is measured. In addition, the tank's Q factor is severely degraded due to the strong magnetic flux cancellation.

Fig. 7.3 (b)-(c) respectively show schematics of a triple-mode and quad-mode resonator by coupling two individual transformer-based resonators [19, 20]. While both designs can continuously cover an octave FTR, they have limitations as well. On the one hand, they at least occupy twice the area of a single VCO. On the other hand, the former needs an extra third winding (L_T) in each transformer that degrades the tank's Q, while the latter uses large fixed coupling capacitors (C_M) that load the tank in two of the resonant modes, thus limiting the VCO's FTR.

Consequently, prior-art mode-switching VCOs either suffer from a severe FOM degradation [22], or FTR discontinuity [23], or a large area penalty [19, 20] as they typically occupy the footprint of two standalone oscillators. To improve on those limitations, this chapter presents a 0.049-mm^2 dual-

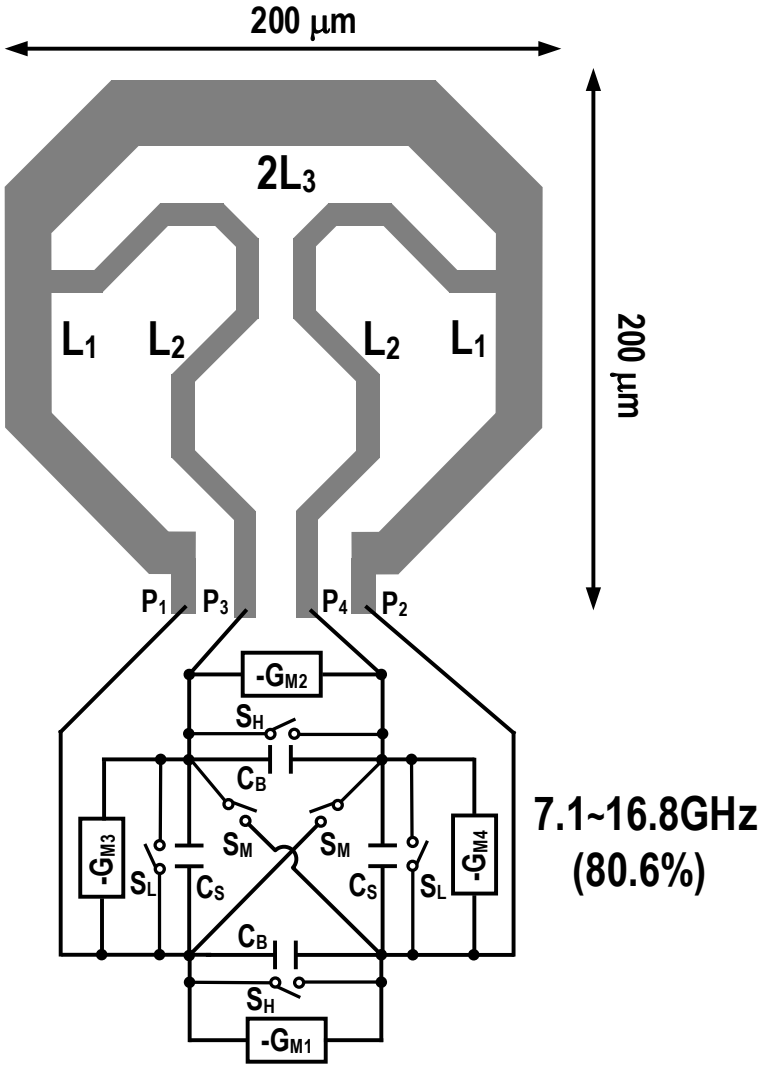

Figure 7.4: Schematic of the proposed dual-core triple-mode VCO.

core triple-mode VCO [184]. Specifically, three distinct resonant frequencies are synthesized through the constructive/destructive magnetic coupling, coil current cancellation, and inductor shortcutting of a high-Q compact 4-port tapped inductor and the capacitive mode switching. Compared with prior art at a similar F_{OSC} range at 300 K, this work improves the area-normalized figure of merit (FOM_A) by 3 dB. Our VCO is implemented within an analog dynamic-amplifier-based PLL (DAPLL). Thanks to the proposed compact and low-power triple-mode VCO, our PLL FOM advances the prior art by more than 4 dB while occupying 4× less area, and offering the highest FTR. Moreover, the DAPLL delivers high performance at 4.2 K as well. It covers a continuous FTR of 7.4-17.8 GHz and achieves an RMS jitter of less than 50 fs, representing the first cryo-CMOS PLL with an octave FTR.

This chapter is organized as follows. Section 7.2 elaborates on the operation

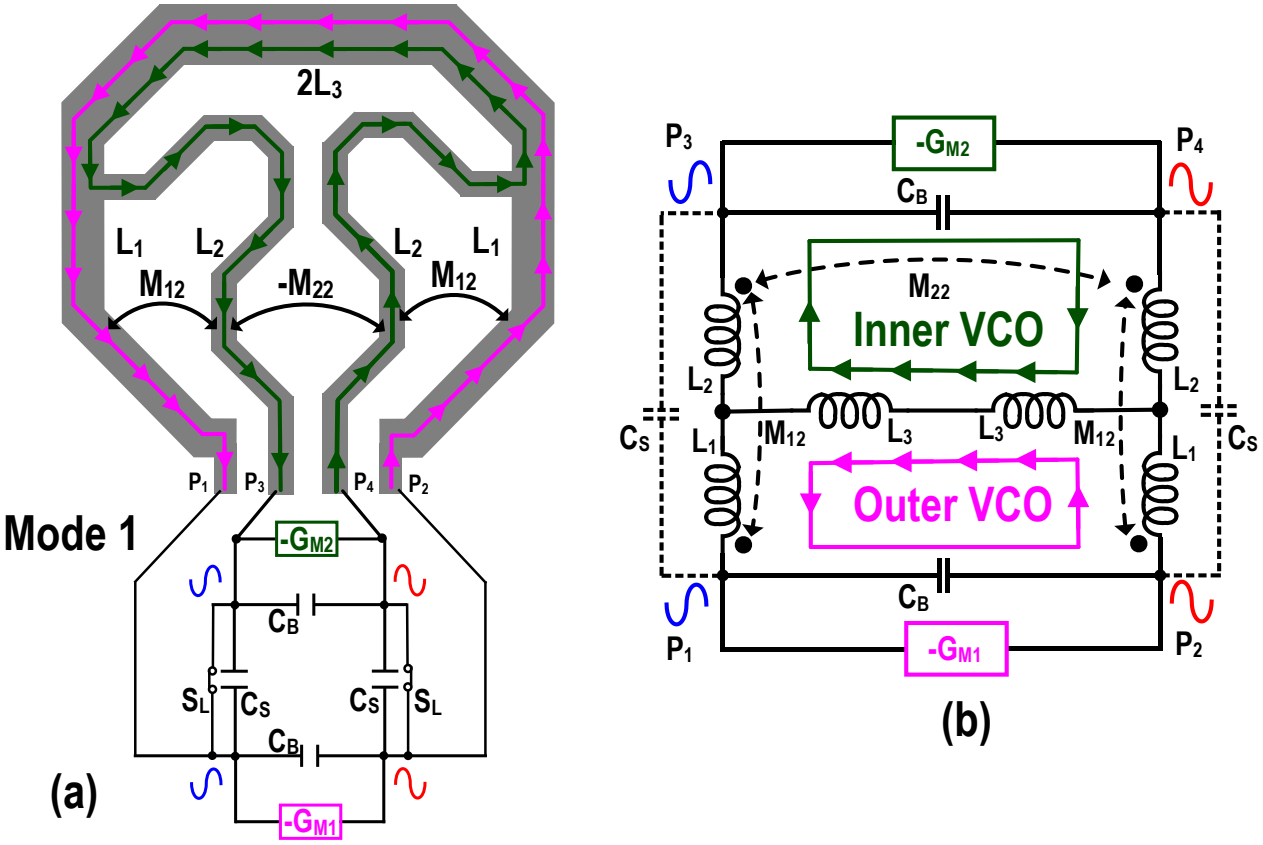

Figure 7.5: (a) Circuit configuration, oscillation voltages and currents, and (b) simplified schematic of the VCO in mode-1.

and design consideration of the proposed dual-core triple-mode VCO. The detailed circuit implementation of the VCO and DAPLL is presented in Section 7.3. Finally, Section 7.4 presents the measurement results at both 300 K and 4.2 K, while Section 7.5 wraps up this chapter with conclusions.

7.2 Proposed Dual-Core Triple-Mode VCO

Fig. 7.4 shows the schematic of the proposed dual-core triple-mode VCO, which consists of negative transconductors ($-G_{M1-4}$), mode-selection switches (S_L, S_M, and S_H), two loop-inductors, and two sets of tuning capacitors (C_B and C_S, where $C_B > C_S$). The outer and inner inductors are realized between P_1-P_2 and P_3-P_4 ports with a self-inductance of $2L_1+2L_3$ and $2L_2+2L_3$, respectively. By differential-mode or common-mode excitation of the inductors' ports through negative transconductors $-G_{M1-4}$ and mode-selection switches S_L, S_M, and S_H, three different equivalent inductances (L_{eff}) and capacitances (C_{eff}) can be realized to achieve three distinct resonant frequencies ($\omega_{1,2,3}$).

7.2.1 Low-Frequency Mode (Mode-1)

Fig. 7.5 (a) depicts the circuit configuration, oscillation voltages and currents in the low-frequency mode (mode-1). This mode is excited by closing S_L and opening $S_{M,H}$, while enabling -G_{M1} and -G_{M2} cores. As a result, two coupled VCOs employing inner and outer inductors are realized. In this mode, signals at P_1 and P_3 are in phase while showing a 180° phase difference with respect to P_2 and P_4 signals. This forces an in-phase coupling between L_1 and L_2, enhancing the magnetic flux and creating a positive mutual inductance (M_{12}). Moreover, anti-phase coupling occurs between two L_2 inductors, thus creating a negative mutual inductance of -M_{22}. Fig. 7.5 (b) shows the simplified schematic of coupled VCOs to facilitate the effective inductance and capacitance calculation in this mode. The effective inductance seen by the inner VCO can be estimated by

$$L_{eff1,in} \approx L_2 + 2L_3 + M_{12} - M_{22}, \tag{7.4}$$

and the effective inductance seen by the outer VCO can be found as

$$L_{eff1,out} \approx L_1 + 2L_3 + M_{12}. \tag{7.5}$$

Unfortunately, $L_{eff1,in}$ and $L_{eff1,out}$ are normally not equal, thus creating a frequency mismatch (ΔF) between the free-running frequencies of the two VCOs. Note that in the presence of ΔF, a current would flow through the lossy mode-selection switches S_L to balance the resonators' energy and force the VCOs to oscillate at the same frequency. Thus, those two VCOs operate off-resonance, degrading the tank's Q factor and limiting the 3-dB theoretical PN improvement due to the coupling. The degraded PN could be expressed by [186]:

$$\Delta PN \approx \frac{1}{1 - 2 \cdot \frac{R_{ON}}{R_P} \cdot Q^2 \cdot \frac{\Delta F}{F_{OSC}}}, \tag{7.6}$$

where R_{ON} is the on-resistance of S_L and R_P is the tank impedance peak at the resonant frequency.

In the ideal case, ΔF or R_{ON} is 0; there is no PN degradation. On the one hand, a large S_L with a low R_{ON} could be used to mitigate the PN degradation issue. However, the FTR would be compromised due to parasitic capacitances

of S_L in other modes. Therefore, a more practical method is to equalize the effective inductance of the two VCOs. This allows for maintaining the PN performance without using a large S_L. Thus, a high FTR can be achieved. As a consequence, L_1 is deliberately designed to be smaller than L_2, and satisfies the following relationship:

$$L_1 = L_2 - M_{22}. \tag{7.7}$$

This is realized by carefully controlling the geometry (both the length and width) of L_2 in the layout. In the design phase, several electromagnetic (EM) simulations and layout iterations were done to reach this goal.

Furthermore, the tank would not see C_S as a common-mode oscillation is realized across CS plates. The effective capacitance in this mode can be found as:

$$C_{eff1} = C_B. \tag{7.8}$$

Therefore, the resonant frequency in mode-1 can be estimated by

$$\omega_1 \approx \frac{1}{\sqrt{2(L_2 + 2L_3 + M_{12} - M_{22})C_B}}. \tag{7.9}$$

7.2.2 Middle-Frequency Mode (Mode-2)

Fig. 7.6 (a) shows the circuit configuration, oscillation voltages and currents in the middle-frequency mode (mode-2). In this mode, -G_{M1} and -G_{M2} cores are kept active, but the mode-selection switches S_M and $S_{L,H}$ are respectively closed and opened to realize a differential-mode oscillation between in-phase $P_{1,4}$ and $P_{2,3}$ signals. This forces an anti-phase magnetic coupling between L_1 and L_2 segments of inner and outer inductors. Moreover, L_3 conducts virtually zero current as the oscillation currents of the inner and outer VCOs circulate in opposite directions. Therefore, in this mode, L_3 is transparent to VCOs due to zero current in L_3. Fig. 7.6 (b) shows the simplified schematic of the VCOs in this mode. Compared with mode-1, the effective inductances of VCOs sharply dropped to

$$L_{eff2} \approx 2L_2 - 2M_{12} - 2M_{22} = 2L_1 - 2M_{12}. \tag{7.10}$$

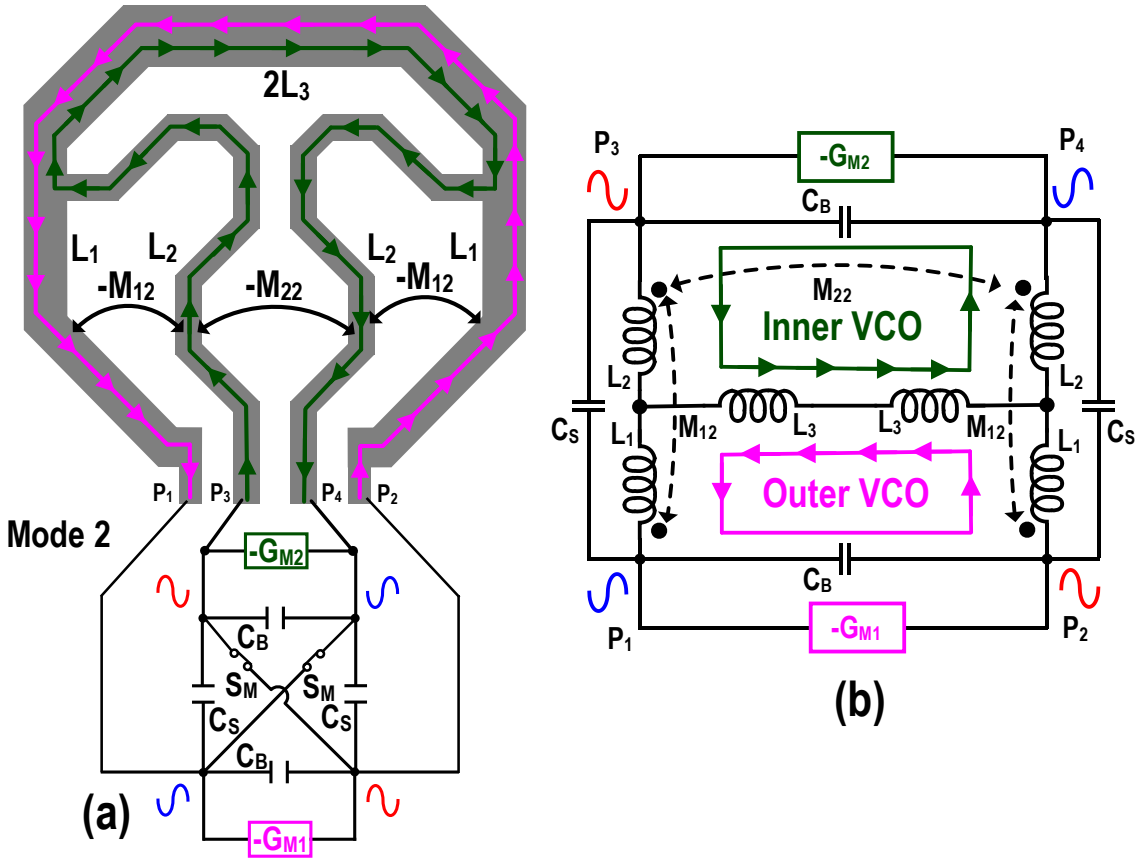

Figure 7.6: (a) Circuit configuration, oscillation voltages and currents, and (b) simplified schematic of the VCO in mode-2.

They are naturally equal since $L_1 = L_2 - M_{22}$. However, as both C_B and C_S experience a differential-mode oscillation voltage, the effective capacitance in this mode increases to $C_{eff2} = C_B + C_S$. Consequently, the resonant frequency in mode-2 can be estimated by

$$\omega_2 \approx \frac{1}{\sqrt{2(L_2 - M_{12} - M_{22})(C_B + C_S)}}. \tag{7.11}$$

Hence, the difference in both the capacitive and inductive components (i.e., $C_{eff2} - C_{eff1} = C_S$ and $L_{eff2} - L_{eff1} = -4L_3 - 4M_{12}$) are exploited to separate mode-2 from mode-1. Note that L_{eff2}/L_{eff1} reduction is designed to be much larger than C_{eff2}/C_{eff1} increase to adjust $\omega_2 \approx 1.3\omega_1$.

7.2.3 High-Frequency Mode (Mode-3)

Fig. 7.7 (a) illustrates the circuit configuration, oscillation voltages and currents in the high-frequency mode (mode-3). This mode is excited by

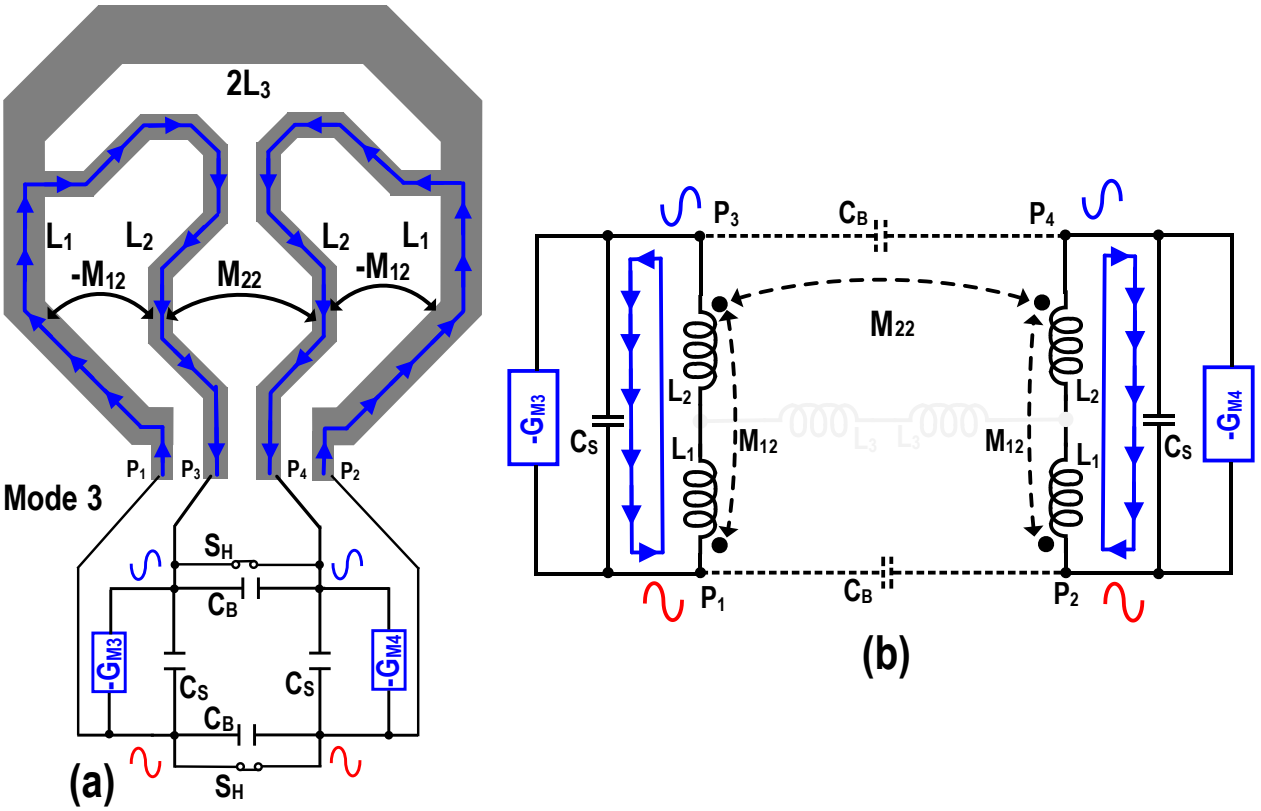

Figure 7.7: (a) Circuit configuration, oscillation voltages and currents, and (b) simplified schematic of the VCO in mode-3.

activating -G_{M3} and -G_{M4} cores, closing S_H, and opening $S_{L,M}$, as shown in Fig. 7.7 (a). In this mode, the currents of the left and right VCOs can find a shortcut and avoid flowing into L_3. Fig. 7.7 (b) shows the simplified schematic of the VCO in mode-3. The effective inductance thus could be approximated by

$$L_{eff3} \approx L_1 + L_2 - 2M_{12} + M_{22} = 2(L_1 - M_{12} + M_{22}). \tag{7.12}$$

Moreover, as a common-mode oscillation is realized across C_B plates, the effective capacitance in mode-3 is reduced to its minimum value:

$$C_{eff3} = C_S. \tag{7.13}$$

Hence, the resonant frequency in mode-3 can be estimated by

$$\omega_3 \approx \frac{1}{\sqrt{(L_1 + L_2 - 2M_{12} + M_{22})C_S}}. \tag{7.14}$$

Therefore, mode-3 is capacitively and inductively separated from other modes to place $\omega_3 \approx 1.3\omega_2$.

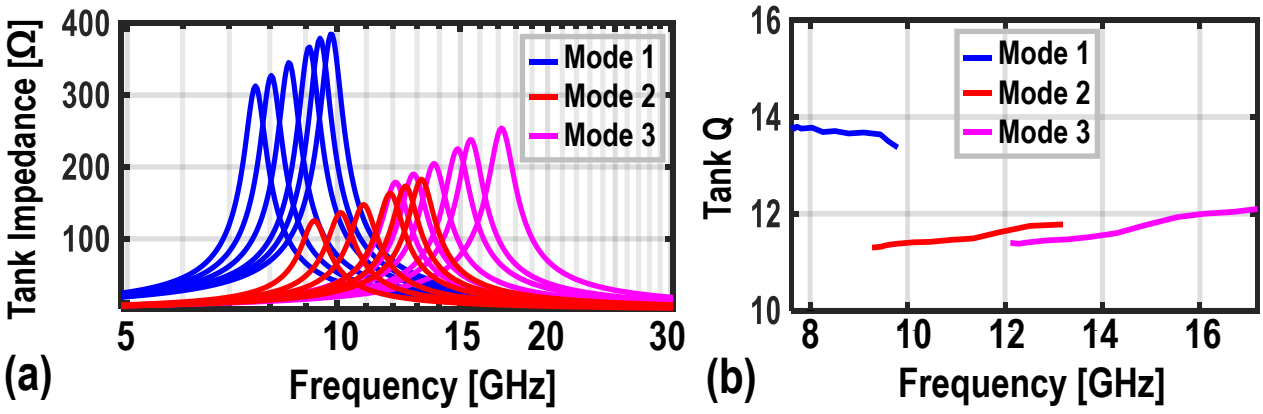

Figure 7.8: Simulated (a) tank impedance and (b) quality factor of the VCO.

7.2.4 Simulation Results of the VCO

Fig. 7.8 (a) and (b) respectively depict the simulated resonator impedance and Q factor based on the inductor's EM and $C_{B,S}$ parasitic extraction. The resonant frequency can be tuned over more than an octave frequency-tuning range with sufficient frequency overlap while going from mode-1 to mode-3, demonstrating the triple-mode operation. The tank impedance peak R_P is the largest in mode-1 due to the highest inductance in this mode. The tank's Q in mode-2 and 3 is ∼15% lower than mode-1 due to the anti-phase coupling between L_1 and L_2. Yet, the resulting FOM_T variation is within 1.5 dB. Since PN is proportional to R_P/Q^2, the lower impedance peak R_P in mode-2 and 3 (caused by the reduced L_{eff}) will partially compensate for their lower tank's Q to achieve a similar normalized PN as in mode-1. This helps a PLL to achieve a stable jitter performance over the entire tuning range. Moreover, to ensure a robust start-up over PVT variations, $-G_{M3,4}$ can be optionally enabled in mode-2, where R_P is the lowest.

7.3 Octave FTR Dynamic-Amplifier-Based PLL

7.3.1 System Overview

A dynamic-amplifier-based PLL (DAPLL) architecture is adopted in this design as it can simultaneously achieve low in-band PN, low reference spur, and low power consumption from 300 K to 4.2 K. Fig. 7.9 shows the simplified block diagram of the proposed octave FTR DAPLL. Similar to a sub-sampling PLL (SSPLL), a feedback frequency divider is not needed in a DAPLL, saving

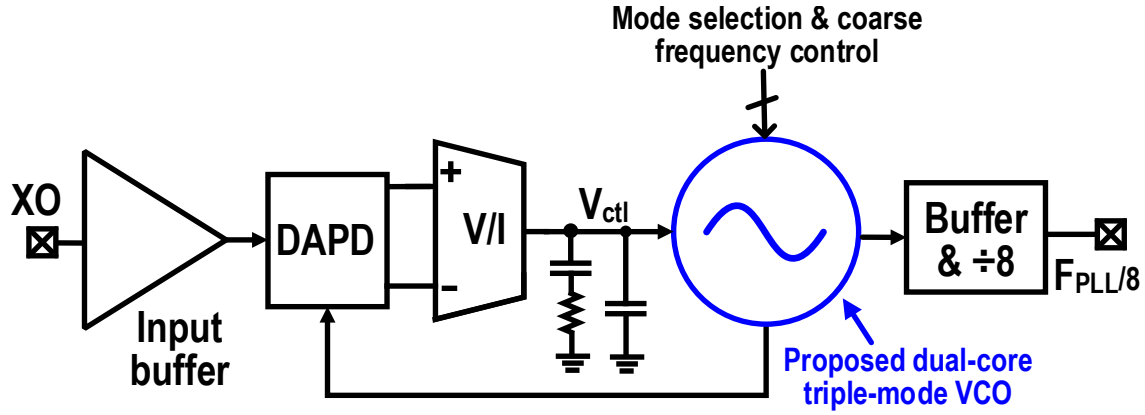

Figure 7.9: Simplified block diagram of the proposed octave FTR DAPLL.

considerable power consumption in the steady state.

The dual-core triple-mode VCO discussed in the previous section is employed to generate a wide FTR signal with low PN. To reshape the external 100-MHz sinusoidal reference clock into a steep square wave, an on-chip input buffer is used. The dynamic-amplifier-based phase detector (DAPD) directly compares the phase error between the VCO and reference without any high-frequency isolation buffers to further save power consumption. It outputs a highly stable voltage (i.e., less than 1 mV_{PP} at F_{REF}). A differential V/I stage (based on a folded-cascode operational transconductance amplifier) converts this voltage into a current. Then, a second-order passive loop filter is then used to generate a tuning voltage for the fine frequency control. In this prototype chip, an on-chip divider-by-8 circuit based on the static current-mode-logic (CML) latch is designed to ease the cryogenic measurements.

Like an SSPLL, the DAPLL also has a limited lock-in range, and one cannot distinguish between the desired N^{th} harmonic and other harmonics of the reference frequency F_{REF}. To avoid locking to a wrong harmonic, the VCO's frequency is manually tuned close to the target frequency by mode-selection circuits and switched capacitor banks. In a future design, automatic frequency-selection circuits similar to the one used in [88–93, 97] could be implemented if required.

7.3.2 VCO implementation

Fig 7.10 shows the schematic of the proposed dual-core triple-mode VCO. The four identical negative G_M cells ($-G_{M1-4}$) are implemented by CMOS differential pairs, which allows using the nominal supply voltage for the VCO.

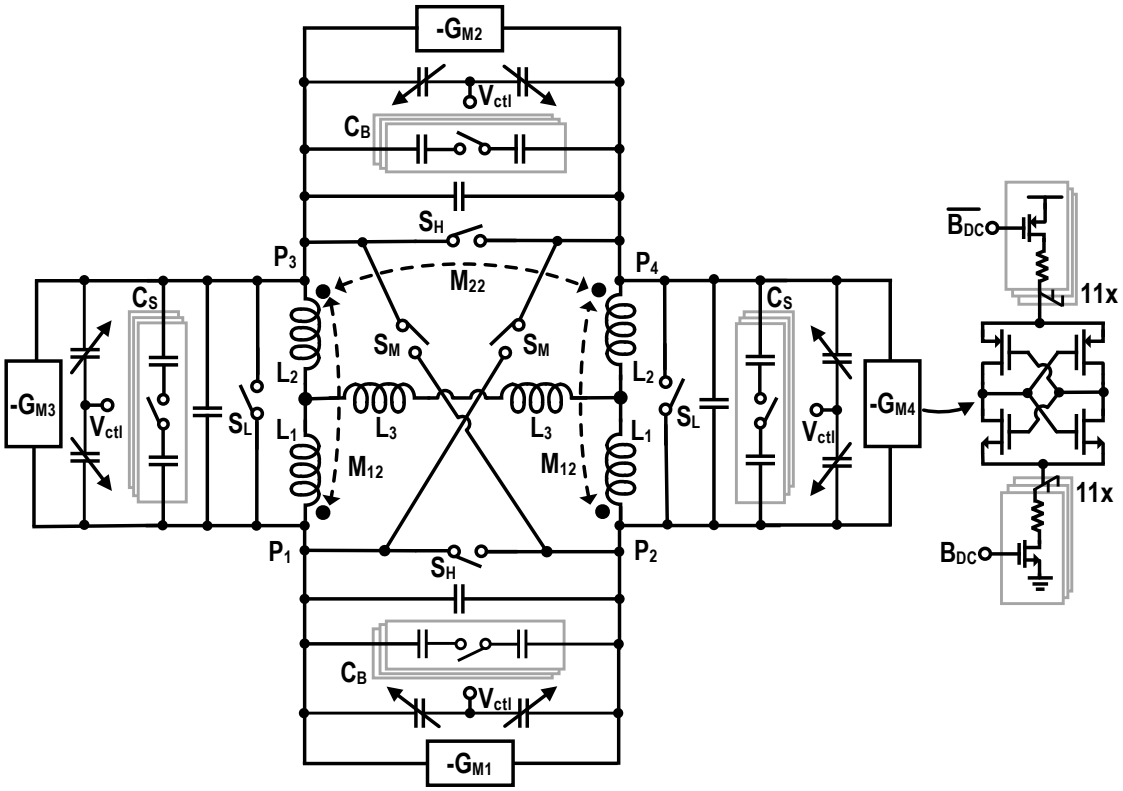

Figure 7.10: Schematic of the proposed dual-core triple-mode VCO.

Low-threshold-voltage devices are used to mitigate the headroom issue due to the threshold increase at 4.2 K. Notice that R_P varies significantly over temperatures and in different operation modes (see Fig. 7.8 (a)). To regulate the oscillation amplitude against R_P variations, 11 equally-sized switched thin-film resistors (TFRs) are added to adjust the VCO current[1]. Since the phase-detection gain (K_{PD}) is proportional to the VCO swing, this also helps to achieve a relatively constant K_{PD} over the DAPLL's tuning range, reducing the in-band phase noise variation.

The mode-selection switches S_L, S_M, and S_H are realized by plain transmission gates and sized such that their ON-resistance (R_{ON}) is low enough (i.e., R_{ON}/R_P <0.25) to minimize PN degradation when the tanks of VCOs face a pessimistic 5% mismatch. Further reducing R_{ON} would increase the switches' parasitic capacitance and limit the FTR. S_L, S_M, and S_H are implemented by low-threshold devices for low R_{ON} at 4.2 K.

For coarse frequency tuning, C_B and C_S are each realized by a small fixed capacitor in parallel with a 7-b binary switched-capacitor bank with a maximum frequency step of 60 MHz. Four varactors with an average tuning

[1]Thin-film resistors have stable resistance operating from 300 K to 4.2 K.

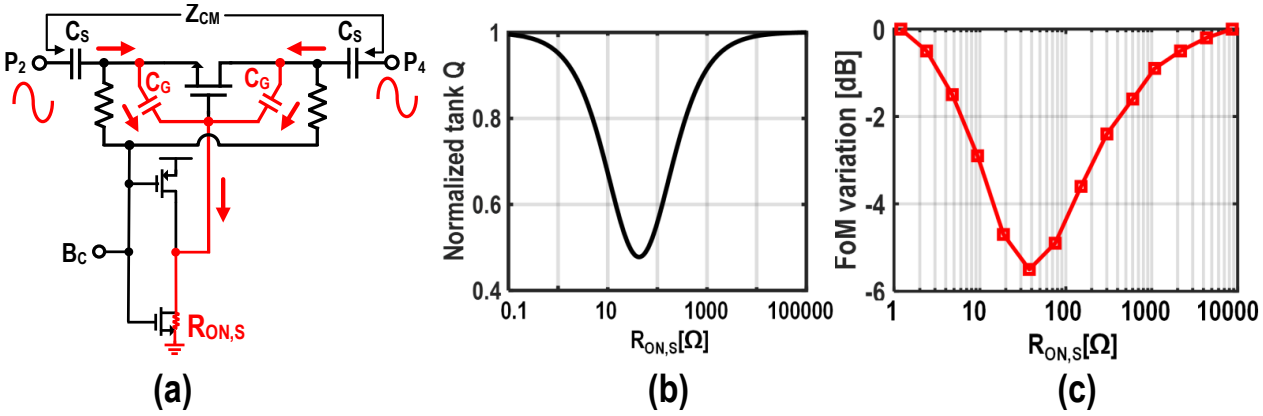

Figure 7.11: (a) Illustration of the common-mode current path with $R_{ON,S}$ in mode-1; simulated (b) normalized tank Q and (b) FOM variations as a function of $R_{ON,S}$.

gain (K_{VCO}) of 120 MHz/V are also added to C_B and C_S to achieve continuous frequency tuning.

Notice that C_S and C_B experience a CM voltage in mode-1 and 3, respectively, and should not contribute to the total tank's capacitance. However, as shown in Fig. 7.11 (a)[1], the gate capacitor of C_B/C_S bank switches (C_G) in series with the ON-resistance ($R_{ON,S}$) of the switch driver forms a return path for the tank's CM current. The resulting single-ended impedance for the tank capacitors can be estimated by

$$Z_{cap} \approx \left(\frac{1}{j \cdot 2\pi \cdot F_{OSC} \cdot C_G} + 2R_{ON,S}\right) \| \frac{1}{j \cdot 2\pi \cdot F_{OSC} \cdot 2C_B}. \tag{7.15}$$

Fig. 7.11 (b) and (c) respectively depict the simulated normalized tank Q factor and FOM as a function of $R_{ON,S}$. It indicates that the tank Q factor could be degraded by 2× and the VCO FOM can be degraded by 6 dB if $R_{ON,S}$ is not properly designed. Although the Q reduction could be minimized by lowering $R_{ON,S}$, a massive driver with a strong power/ground connection would be required, complicating the layout. Besides, as shown in Fig. 7.12 (a), the driver output would be shorted to ground due to samll $R_{ON,S}$. Therefore, the single-ended impedance for the tank capacitors can be estimated by

$$\begin{aligned} Z_{cap} &\approx \left(\frac{1}{j \cdot 2\pi \cdot F_{OSC} \cdot C_G} + \frac{1}{j \cdot 2\pi \cdot F_{OSC} \cdot C_S}\right) \| \frac{1}{j \cdot 2\pi \cdot F_{OSC} \cdot 2C_B} \\ &\approx \frac{1}{j \cdot 2\pi \cdot F_{OSC} \cdot (C_G + 2C_B)}. \end{aligned} \tag{7.16}$$

[1]Mode-1 is taken as an example for the illustration purpose.

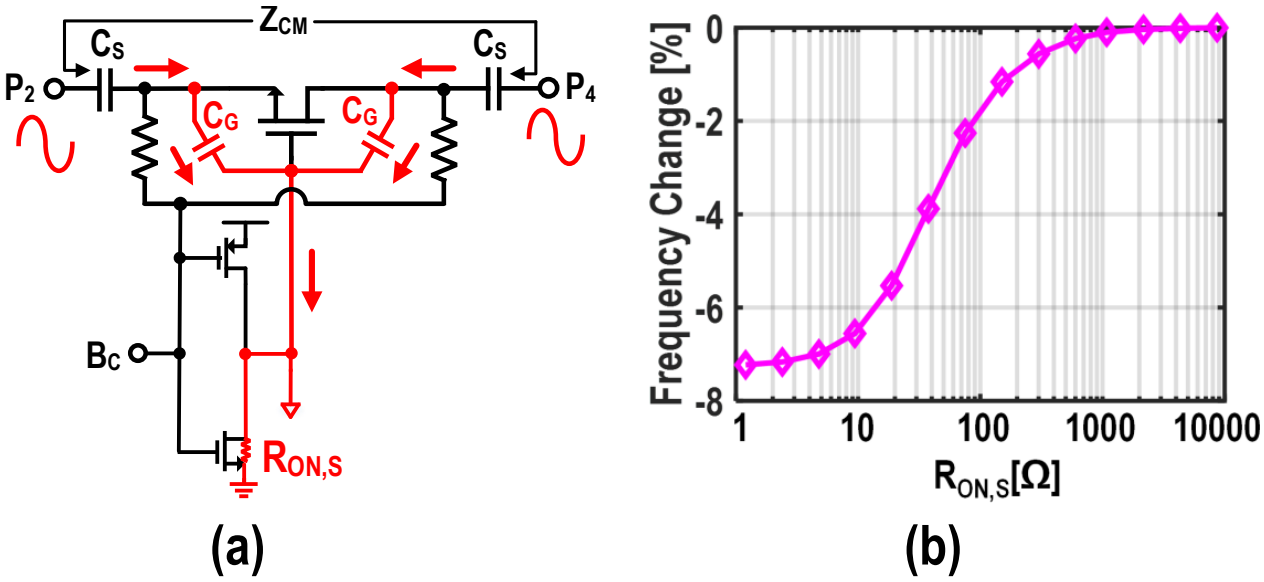

Figure 7.12: (a) Illustration of the common-mode current path with with a large switch driver in mode-1; (b) simulated frequency change as a function of $R_{ON,S}$.

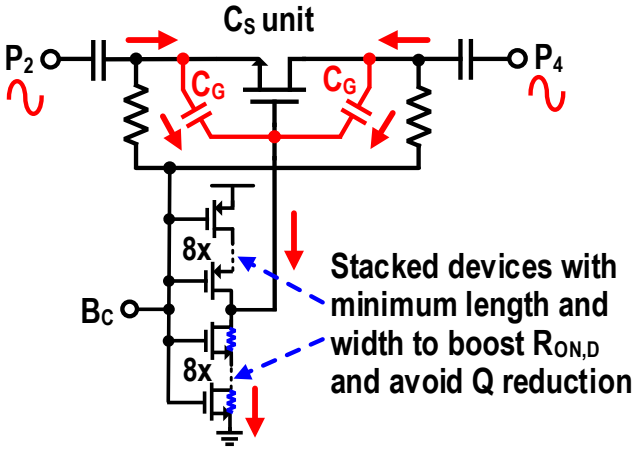

Figure 7.13: Schematic of the implemented switched capacitor unit.

Hence, C_G would be visible to the tank, thus limiting the FTR and maximum F_{OSC}. Fig. 7.12 (b) indicates that up to 7-% FTR is lost if a large switch driver with a low $R_{ON,S}$ is used. Fig. 7.13 shows the schematic of the implemented switched capacitor unit. 8 stacked devices with minimum channel length and width are used to simultaneously minimize the driver output capacitance and to increase $R_{ON,S}$, thus impeding current flow through the driver. Therefore, FTR and PN are not affected as C_G is no longer visible to the tank. As shown in Figs. 7.11 (c) and 7.12 (b), an $R_{ON,S}$ of 10 kΩ is sufficiently large for this purpose and yet low enough to ensure 500-MHz switching speed for the capacitor bank.

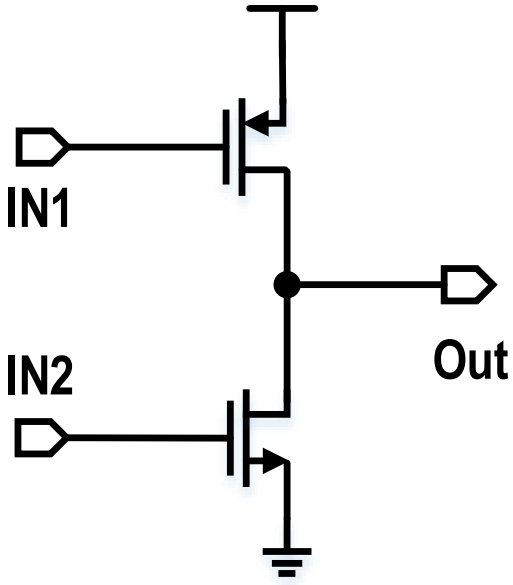

Figure 7.14: Schematic of the input reference buffer.

7.3.3 Other Circuits

As shown in Fig 7.14, the input reference buffer is based on a simple inverter. The NMOS transistor of the inverter is sized very large to create a low PN falling edge, while the small PMOS is used to pull up the output node. The gate biasing for both NMOS and PMOS can be adjusted to reduce the short-circuit current. Thick-oxide devices with a long channel length are used for the inverter to reduce the shot noise at 4.2 K. At 300 K, the input buffer consumes ∼0.9-mW power to achieve a PN floor below -170 dBc/Hz when referred to a 100-MHz carrier.

The dynamic-amplifier-based phase detector (DAPD) is adapted from the one presented in Chapter 6. Its phase-detection gain can be adjusted from 0.05-1 rad/V, which is enough to cover PVT variations. Due to the DAPD's advantage, it achieves less than -175 dBc/Hz PN floor with a power consumption below 20 μW. Thanks to the DAPD's high-phase detection, the following V/I stage contributes less than 5% to the total in-band PN while consuming less than 50 μW power. Both the transconductance of the V/I and the loop filter's compensation resistor can be digitally adjusted for the DAPLL bandwidth control.

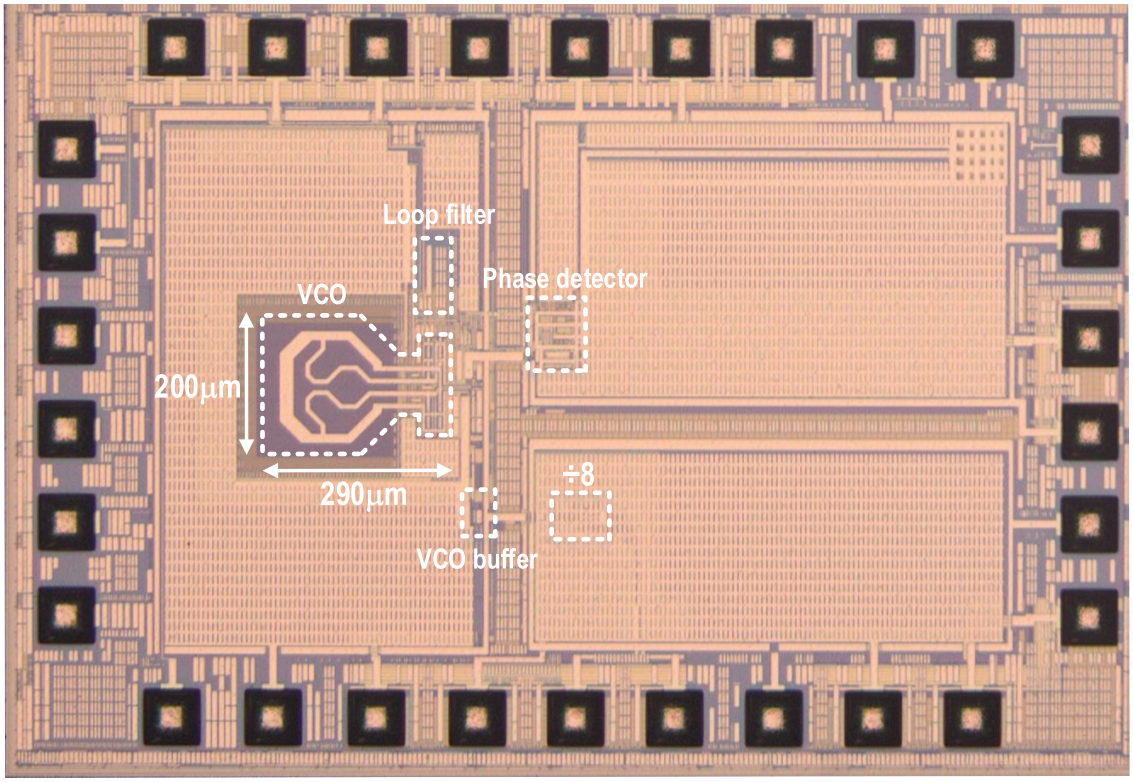

Figure 7.15: Chip micrograph of the DAPLL with a dual-core triple-mode VCO.

7.4 Measurement Results

The proposed dual-core triple-mode VCO, implemented within an analog dynamic-amplifier-based PLL (DAPLL), was fabricated in a 22-nm FinFET CMOS. The chip micrograph is shown in Fig. 7.15. The DAPLL occupies a core area of 0.078 mm^2, and the VCO occupies 0.049 mm^2. Thanks to the small area of the VCO, the DAPLL has a compact chip footprint. As mentioned earlier, an on-chip divider-by-8 is used to ease the measurements. This divider is designed very low noise to minimize its impact on the DAPLL performance. Hence, its power consumption is very high (>50 mW), which creates severe self-heating at 4.2 K. To mitigate this issue, the test divider and the DAPLL are placed physically far away from each other in the layout.

7.4.1 Measurement Results at 300 K

The VCO consumes 5.5 to 13.5 mW (5.5 to 6 mW in mode-1, 11.3 to 13.5 mW in mode-2, and 6.5 to 6.8 mW in mode-3) from a 1.1 V supply. The measured power consumption is the highest in mode-2, which is expected since the R_P is lowest in this mode. The DAPLL's power consumption is 6.5

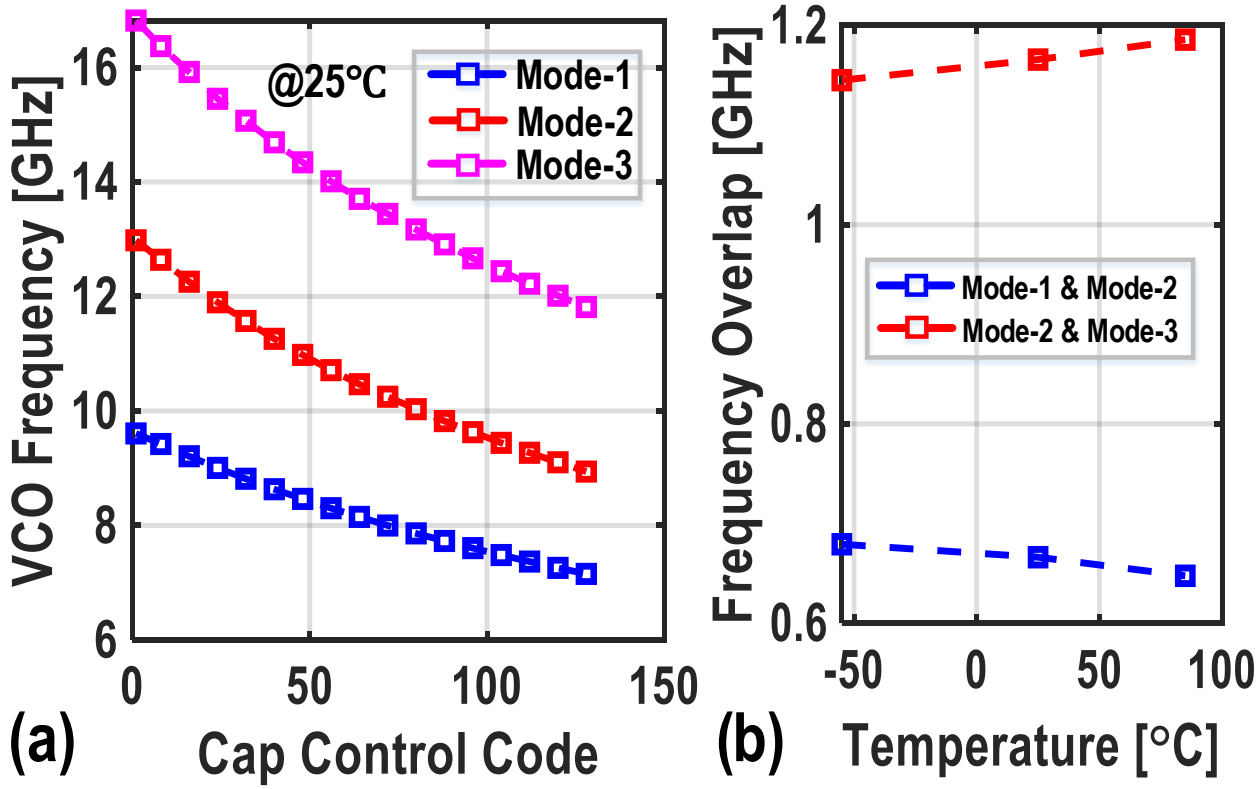

Figure 7.16: Measured (a) frequency-tuning curves and (b) frequency overlap between adjacent modes over temperature at 300 K.

to 14.5 mW and is dominated by the VCO, which is necessary to achieve an ultra-low jitter for a wide FTR PLL.

The performance of the free-running VCO is first measured from an R&S FSWP8 PN analyzer in an open-loop configuration. As shown in Fig. 7.16 (a), the VCO shows a triple-mode operation by covering 7.1-9.6 GHz (29.9%), 8.9-13 GHz (37.4%), and 11.8-16.8 GHz (34.9%) at 25°C. Moreover, from -55°C to 85°C, a continuous FTR of 80.6% with more than 0.65 GHz frequency overlap between adjacent modes is achieved [see Fig. 7.16 (b)]. Those results suggest that the VCO has a continuous FTR over a wide temperature.

Fig. 7.17 (a)-(c) present the measured PN profiles in three operation modes at the test divider-by-8 output. During those measurements, the resistors implemented in $-G_{M1-4}$ are adjusted to optimize the VCO performance. The restored PN[1] at 7.15 GHz, 10.79 GHz, and 16.81 GHz are -137.9 dBc/Hz, -135.5 dBc/Hz, and -128.7 dBc/Hz, respectively, at a 10-MHz offset. Hence, the normalized PN to a 10-GHz carrier is -135.0 dBc/Hz, -136.1 dBc/Hz, and -133.3 dBc/Hz, which is within a 3-dB variation.

[1]The measured PN is added by 18 dB due to the divider by 8.

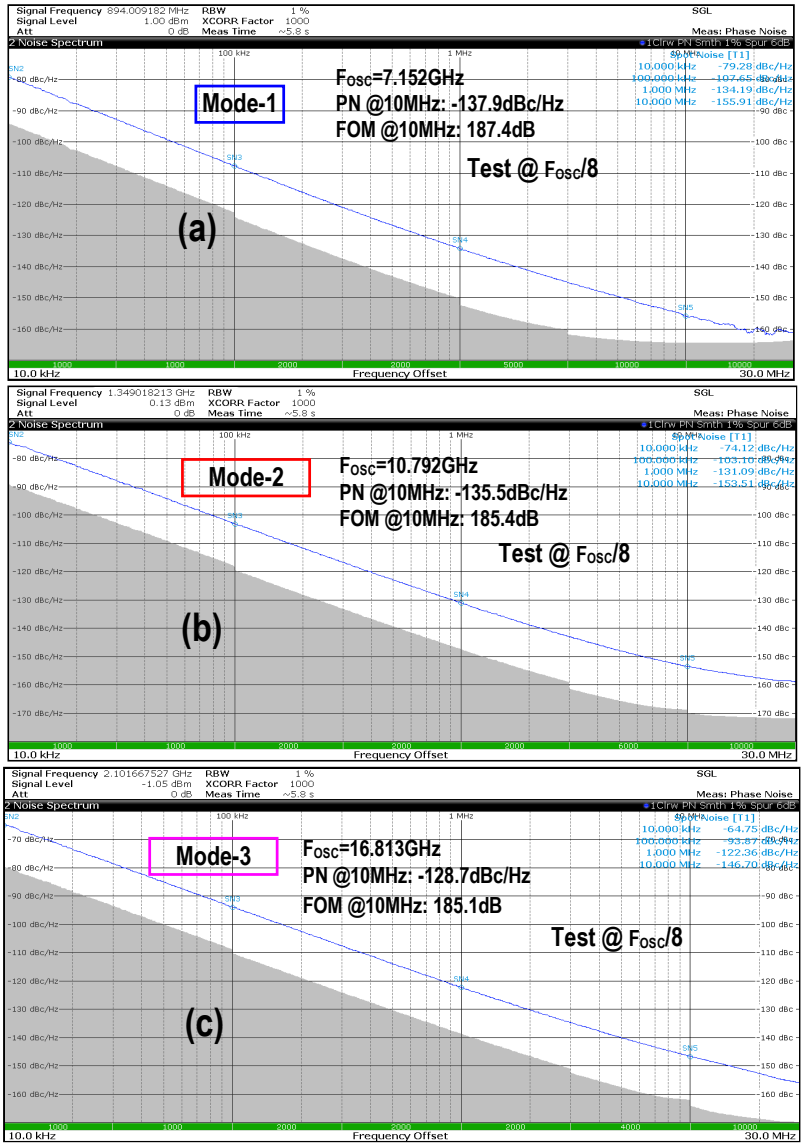

Figure 7.17: (a)-(c) Measured VCO phase noise in three operation modes.

Fig. 7.18 (a) and (b) respectively show measured PN and FOM and FOM_T at a 10-MHz offset in different operation modes over temperature. The measured FOM in mode-1 is ∼2 dB higher than that in mode-2 and mode-3, which is compliant with the simulated tank Q factor shown in Fig. 7.8. As shown in Fig. 7.18 (a), the PN is measured in different operation modes at a 10 MHz offset over temperature. The measured PN variation over a 140°C temperature range is less than 3.6 dB at a similar F_{OSC}. Furthermore, the normalized PN variation is within 3 dB over the entire FTR, suggesting that the VCO can deliver stable performance over operation modes. Thanks to the enhanced $R_{ON,S}$, as shown in Fig. 7.18 (c)-(d), changing C_S (C_B) in mode-1

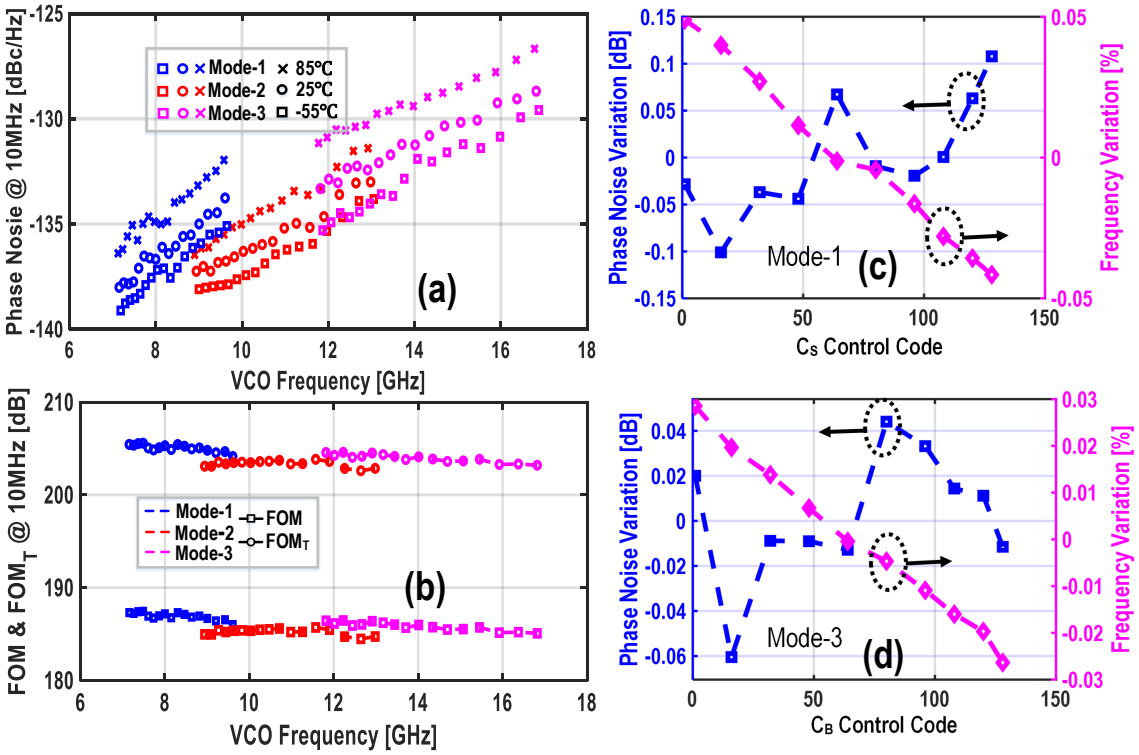

Figure 7.18: Measured (a) PN and (b) FOM and FOM_T at a 10-MHz offset versus the VCO frequency over temperature; (c)-(d) Measured phase noise and frequency variations by changing C_S (C_B) in mode-1 (mode-3).

(mode-3) has a negligible impact on the measured PN (<0.3 dB) and F_{OSC} (<0.1%).

The closed-loop PN was measured as well. An external 100-MHz clock is used as the DAPLL's reference. Fig. 7.19 (a)-(c) respectively show the measured PN plot in three operation modes at 300 K, where the PLL is running at 7.2 GHz, 12 GHz, and 16 GHz. An in-band PN floor below -115 dBc/Hz has been achieved when referred to a 10-GHz carrier, which is mainly limited by the on-chip input buffer[1]. The measured RMS jitter (from 10 kHz to 30 MHz), excluding reference spurs, is below 80 fs in those frequencies, corresponding to a PLL jitter-power FOM of better than -252 dB. Due to the VCO's negligible FOM variations, the measured RMS jitter of the PLL is almost constant and remains <80 fs over different operation modes. Finally, the measured worst-case reference spur over the three operation modes is below -63 dBc.

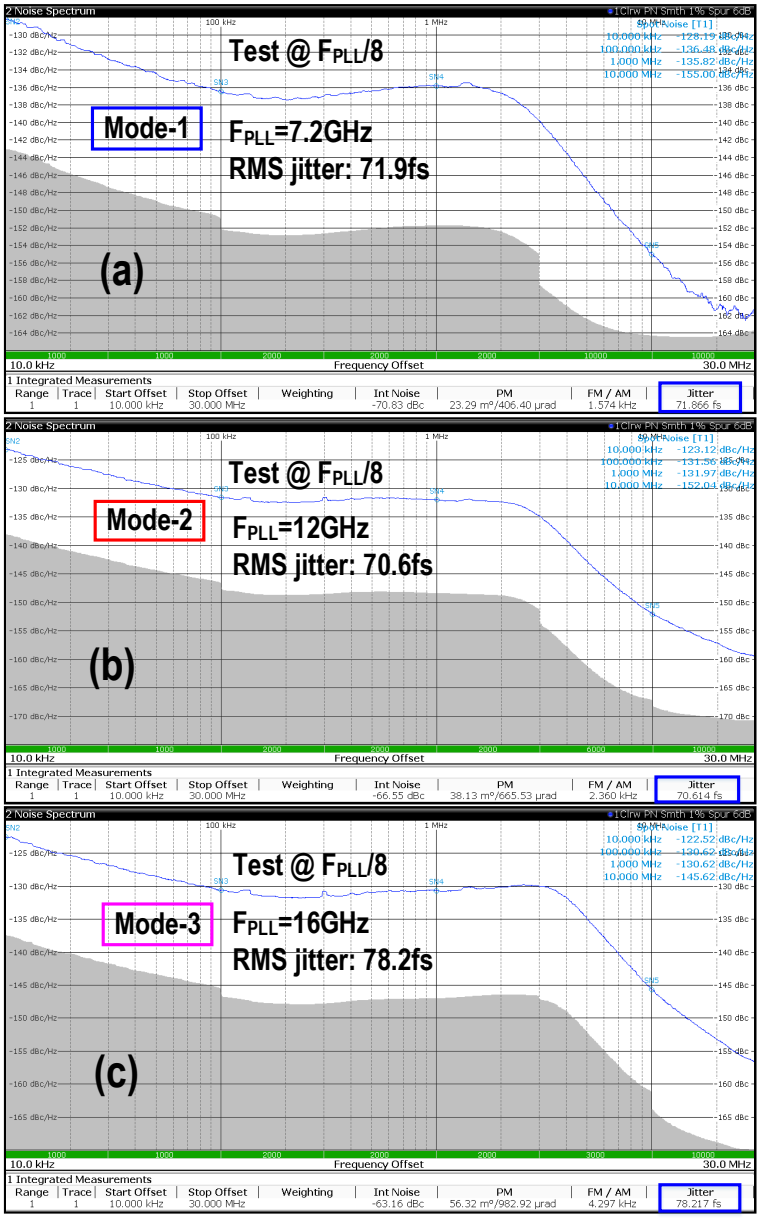

Figure 7.19: (a)-(c) Measured PLL phase noise in three operation modes at 300 K.

7.4.2 Measurement Results at 4.2 K

The performance of both the dual-core triple-mode VCO and DAPLL was measured at 4.2 K as well. To reach this temperature, a dipstick setup was used, which immersed the DAPLL die into the liquid helium (see Chapter 6). The VCO is still functional at this temperature and shows a triple-mode operation by covering 7.44-10.15 GHz (30.8%), 9.3-13.58 GHz (37.4%), and 12.39-17.88 GHz (36.3%) at 4.2 K. This translates to a continuous FTR of 82.5%,

[1]We suspect that the input reference buffer's noise is higher than expected due to underestimated layout parasitics.

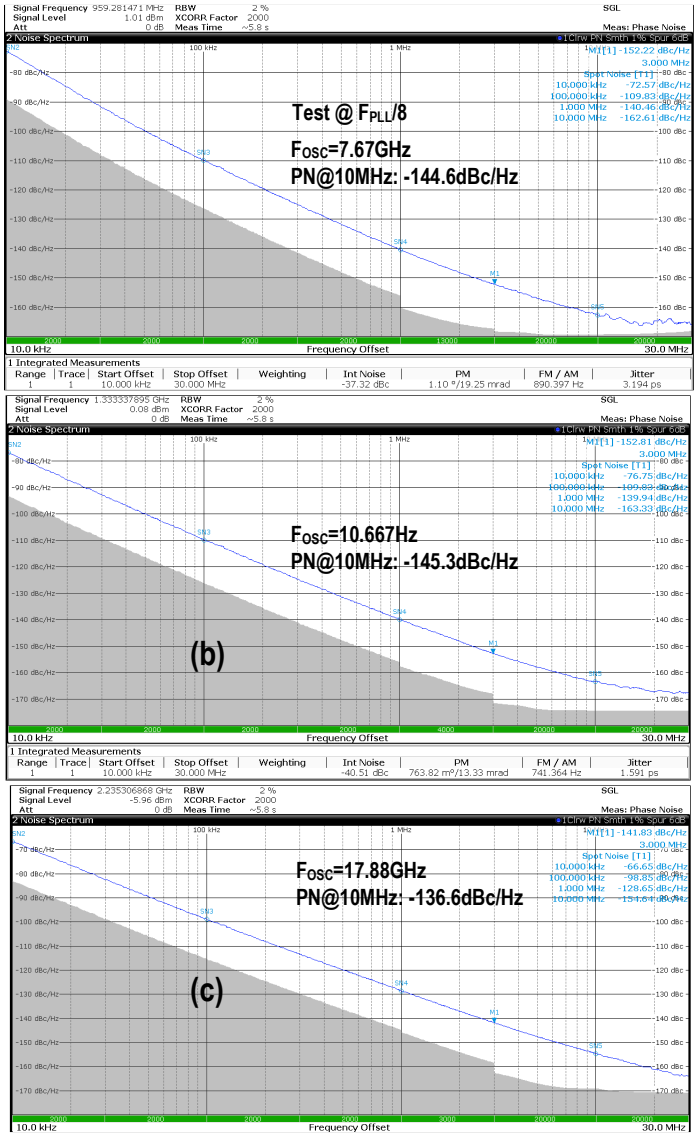

Figure 7.20: (a)-(c) Measured VCO phase noise in three operation modes at 4.2 K.

which is close to the room-temperature results (80.5%). In addition, more than 0.85 GHz frequency overlap between adjacent modes is achieved. Moreover, the measured maximum and minimum VCO frequency in each mode is around 5 % higher compared to 300 K. This indicates that the inductor's inductance is reduced as the capacitance of the metal capacitor slightly increases at 4.2 K. The VCO consumes 3.5 to 9.9 mW (3.5 to 3.7 mW in mode-1, 7.4 to 9.9 mW in mode-2, and 5.1 to 9.9 mW in mode-3) from a 1.1 V supply. At 4.2 K, the measured power consumption is lower compared with 300 K due to the higher Q factor of the resonator.

Fig. 7.20 (a)-(c) present the measured PN plots in three operation modes at 4.2 K. The restored PN at 7.67 GHz, 10.67 GHz, and 17.88 GHz are -

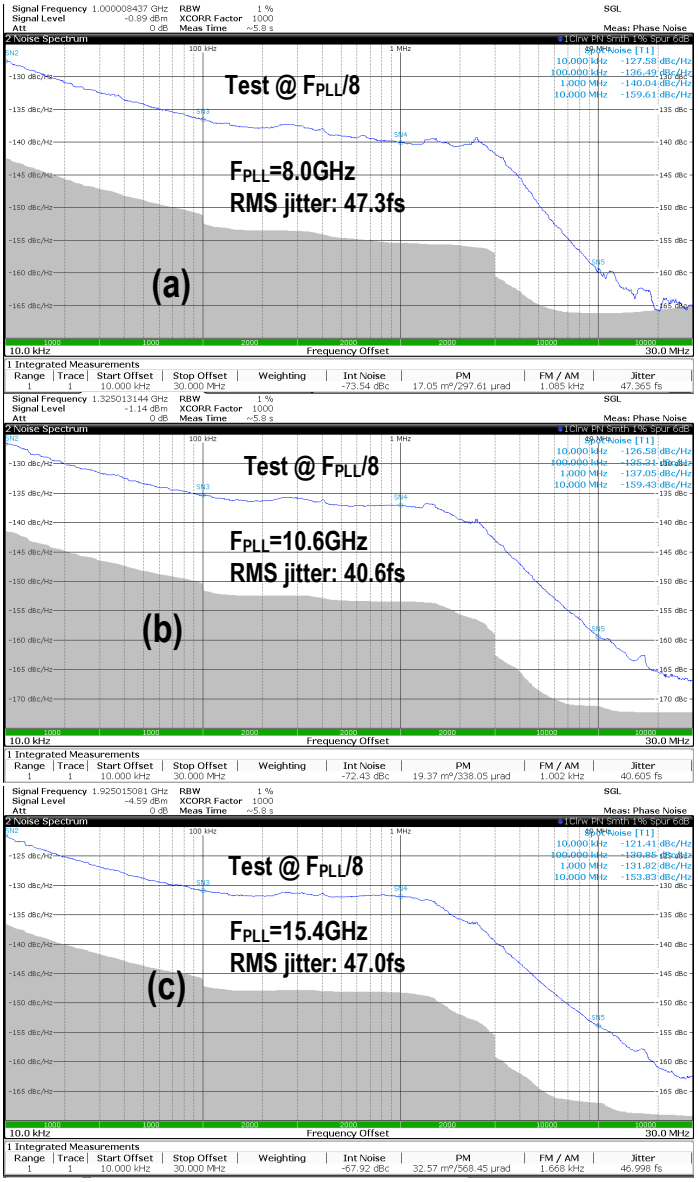

Figure 7.21: (a)-(c) Measured PLL phase noise in three operation modes at 4.2 K.

144.6 dBc/Hz, -145.3 dBc/Hz, and -136.6 dBc/Hz, respectively, at a 10-MHz offset. The normalized PN to a 10-GHz carrier is -142.2, -145.8, and -141.6 dBc/Hz, which is ∼7-9 dB lower compared with 300 K. The measured PN variations match the theory presented in Chapter 4, indicating that the shot noise cannot be ignored at 4.2 K.

The closed-loop PN was measured at 4.2 K as well. The external 100-MHz clock is placed at room temperature to ease the measurement. Fig. 7.21 (a)-(c) respectively show the measured PN plots over the three operation modes, where the PLL is running at 8 GHz, 10.6 GHz, and 15.4 GHz. An in-band PN floor of below -120 dBc/Hz has been achieved when referred to a 10-GHz carrier, which is ∼5 dB lower compared with room-temperature results. The

Table 7.1: Comparison with state-of-the-art.

	This Work	M. Raj VLSI'16	O. El-Aassar JSSC'21	A. Agrawal TMTT'17	W. Deng CICC'21	Y. Shu ISSCC'20
VCO Topology	**Dual-core Triple-mode**	Single-core Dual-mode	Dual-core Triple-mode	Single-core Dual-mode	Dual-core Quad-mode	Quad-core Quad-mode
Supply [V]	**1.1**	0.8	0.45/0.9***	0.45~0.6	NA	0.95
Frequency [GHz]	**7.1~16.8**	7~18.3	8~17	6.39~14	8.2~21.5	18.6~40.1
Tuning Range [%]	**80.6**	89.3	72	74.6	89.6	73.2
Power [mW]	**5.5~13.5***	4.4~3	17^~33^^	2.2~10.3	4~6	9~15
PN @10MHz [dBc/Hz]	**-137.9~-128.7**	-131.8**~-119**	-143.1^~-134.7^^	-137.7~-130.3	-129~-120	-130.3~-122.7
PN @10MHz [dBc/Hz] (normalized to 1GHz)	**-155~-153.2**	-148.8~-144.2	-163.8~-155.8	-153.8~-153.2	-147.3~-146.7	-156~-154.7
Average FOM / FOM Variation @10MHz [dB]	**186.3 187.6~185.1**	180.9 182.3~179.5	186.15 191.65~180.65	187 188~186	179 181~177	184.65 186.3~183
Average FOM_T / FOM_T Variation @10MHz [dB]	**204.4 205.7~203.2**	199.9 201.3~198.5	203.3 208.8~197.8	204 205~203	198.5 201~196	201.95 203.6~200.3
Average FOM_A / FOM_A Variation @10MHz [dB]	**199.4 200.7~198.2**	196.1 197.5~194.7	190.2 195.7~184.7	196 197~195	183 185~181	195.65 197.3~194
Technology	**22nm FinFET**	16nm FinFET	22nm FDSOI	65nm CMOS	65nm CMOS	40nm CMOS
Core Area [mm^2]	**0.049**	0.03	0.39	0.126	0.4	0.08

*6-5.5mW (mode-1), 13.5-11.3mW (mode-2), and 6.8-6.5mW (mode-3) **Estimated from plots ***0.9V Forward body biasing voltage used in switched capacitors ^Reported value @11.02GHz ^^Reported value @11.4GHz
$FOM=|PN(\Delta f)|+20\log10(F_{OSC}/\Delta f)-10\log10(P_{DC}/1mW)$
$FOM_T=FOM+20\log10(FTR/10)$
$FOM_A=FOM+10\log10(1mm^2/A)$ defined in [B. Soltanian, JSSC'07]

measured RMS jitter (from 10 kHz to 30 MHz), excluding reference spurs, is below ∼50 fs over the operation modes. Due to the VCO's negligible FOM variations, the measured RMS jitter of the PLL is almost constant as well over different operation modes at 4.2 K. The measured worst-case reference spur over the three operation modes is below -66 dBc, which is sufficient for quantum computing applications.

7.4.3 Comparison with Prior Art

Table 7.1 summarizes the performance of the proposed VCO and compares it with previously published works at similar frequencies at 300 K[1]. Only the

[1]To the best of the author's knowledge, there is no octave FTR VCO and PLL operating at 4.2 K. Hence, for a fair comparison, only the room-temperature designs are compared.

Table 7.2: Comparison with state-of-the-art.

	This Work	M. Raj VLSI'17	D. Turker ISSCC'18	Y. Wang JSSC'23
PLL Architecture	**Integer N, DAPLL**	**Integer N, Sampling PLL**	**Integer N, Charge-Pump PLL**	**Integer N, Sub-Sampling PLL**
Power Supply [V]	**1.1**	0.9/1.8	NA	0.7/1.1
Reference Freq. [MHz]	**100**	450	500	100
FTR [GHz]	**7.1-16.8 (80.6%)**	9-18 (66.7%)	7.4-14 (61.7%)	7.9-14.3 (57.7%)
Test Frequency [GHz]	**16**	18	12.5	12.2
PN @ 100kHz/1MHz (normalized to 1GHz)	**-136.6/-136.6**	-129.2/-132.4 (@200kHz)	-135.9/-139.1	-134.1/-134.1
RMS Jitter, σ_{rms} [fs] [Int. Bandwidth]	**78.2 (69~79)* [10k-30MHz]**	164 [1k-100MHz]	53.6 [10k-10M]	77 (77.0~84.6) [1k-30MHz]
Power, P_{DC} [mW]	**7.6** (6.5~14.5)**	29.2	45	14.1~17.2
^FoM$_{PLL}$ [dB]	**-253.3 (-254.5~-252)**	-241	-248.9	-249.4~-250.5
^^FoM$_N$ [dB]	**-275.3 (-272.6~-275.8)**	-257	-262	-271~-271.4***
Core Area [mm^2]	**0.078**	0.39	0.35	0.18
Process [nm]	**22nm FinFET**	**16nm FinFET**	**16nm FinFET**	**40nm CMOS**

*Over the entire frequency tuning range **Include the power consumption of the input buffer *** Estimated from plots

^FoM$_{PLL}$ = 20*log$_{10}$(σ_{rms}/1s)+10*log$_{10}$(P_{DC}/1mW) ^^FoM$_N$ = FoM$_{PLL}$ +10*log$_{10}$(F_{REF}/F_{PLL})

dual-mode VCO in [22] occupies a smaller area, but with >4 dB worse FOM_T. Although [20] achieves a better maximum FOM_T, it occupies ∼8× larger area and its performance drops by >10 dB over the FTR. Without sacrificing FOM_T, our triple-mode VCO achieves the best reported FOM_A of 200.7 dB, thus improving prior art by 3 dB.

Table 7.2 shows the performance summary of the DAPLL and compares it with the state of the prior art wide tuning range PLLs. Thanks to the proposed compact and low-power triple-mode VCO, our octave FTR PLL FOM (FOM_N) advances the prior art by more than 3.5 dB (∼4 dB) while occupying 2× less area, and offering the highest frequency tuning range.

7.5 Conclusion

In this chapter, we presented a dual-core triple-mode LC VCO with a wide frequency tuning range. The triple-mode operation is realized by a high-Q compact 4-port tapped inductor in combination with the capacitive

mode switching. The mode-switching network does not conduct current in three operation modes, and hence small switches are used to optimize the tuning range. The oscillation frequency and operation conditions of the VCO are analyzed in depth. Meanwhile, by using a small switch driver for the capacitor bank, the frequency tuning range and phase noise performances can be preserved. Fabricated in a 22-nm FinFET CMOS process, the 0.049 mm^2 VCO exhibits an 80.6% frequency tuning range from 7.1 to 16.8 GHz, and achieves a state-of-the-art FOM_T of 204.4 dB at a 10-MHz offset at 300 K. The peak FOM_A of this design is 200.7 dB, outperforming the prior art by >3 dB at similar frequencies. Thanks to the proposed low-noise dual-core triple-mode VCO, the DAPLL can deliver less than 80 fs RMS jitter over the entire tuning range at 300 K. Moreover, both the VCO and DAPLL function at 4.2 K and deliver high performance.

Chapter

Conclusion

In previous chapters, we have introduced several high-performance phase-locked loops (PLLs) and oscillators which operate over a wide temperature range. The detailed theoretical analysis is provided as well. This chapter is the last chapter of this thesis. Chapter 8.1 summarizes the thesis, and it also repeats the accomplishments achieved throughout this thesis. Finally, Chapter 8.2 provides some suggestions and recommendations for future improvements to this research work.

8.1 Research Overview

Quantum computers have gained widespread interest from both industry and academia in the last decade as they are very promising for solving problems intractable by classical computers. However, there is a limited number of qubits in current quantum processors, which impedes the practical applications of a quantum computer. To increase the number of qubits and scale up a quantum computer, a classical electronic interface is required to control and read out the quantum processor operating at cryogenic temperatures. A high-performance phase-locked loop (PLL) is a critical component in such an interface (Chapter 1).

Since the quantum computing application is a new field, the impact of the PLL's performance on the system performance is not clear at the beginning of this Ph.D. work. In Chapter 2, the VCO and PLL specifications are first derived, which are based on the control fidelity for a single-qubit operation. The specifications obtained in this chapter are used as the basis for designing oscillators and PLLs in the following chapters. In addition, to meet the PLL specifications at cryogenic temperatures for quantum applications, it is essential to have device models at those temperatures. In Chapter 3, the existing literature on cryogenic device behaviors is first discussed, and a simplified device model was then developed to predict the circuit's behavior at 4.2 K. The simplified device model helps to analyze and design circuits in the following chapters.

Chapter 4 introduces a low-phase-noise cryogenic CMOS (cryo-CMOS) oscillator for the control electronics of quantum computers in a 40-nm bulk CMOS process. An oscillator is a critical component of a cryo-CMOS frequency synthesizer. It generates the RF signal and limits the PLL's out-of-band phase noise. However, based on the characterization results of an oscillator [48], it was found that the flicker phase noise corner of an oscillator at 4.2 K is severely degraded when compared with 300 K. Hence, the goal of this chapter is to investigate an oscillator with both low flicker phase noise corner and low phase noise. A digital calibration loop is presented to automatically adjust the configuration of the differential-mode and common-mode capacitor banks of an oscillator to ensure that the oscillator always operates near its optimum performance at 4.2 K. This calibration loop is general and can be used in other

applications requiring low phase noise. Based on the device model developed in Chapter 3, design considerations for the cryogenic temperature operation of both the oscillator and calibration circuits are proposed and analyzed. Moreover, the phase noise performance of a cryo-CMOS *LC* oscillator is studied in detail. We point out that the phase noise of an *LC* oscillator operating at 4.2 K is limited by temperature-independent shot noise.

Unfortunately, the oscillator presented in Chapter 4 exhibits frequency drift over time due to its open-loop nature. Hence, it cannot be directly used in a qubit controller. In Chapter 5, a complete PLL is presented. By locking the oscillator to an external stable reference, this PLL can achieve long-term frequency stability. While the PLL is designed and optimized for conventional high-performance applications, it also demonstrates its functionality at 4.2 K and hence can be used for quantum computing applications. The flicker phase noise issue of an oscillator is tackled by a wide bandwidth PLL in this chapter. Hence, the phase noise of the PLL loop components must be minimized. To achieve high performance, the windowed-current-integration mechanism is exploited in the PLL's phase-detection circuit. As a result, the PLL achieves a high phase-detection gain and simultaneously minimizes the duty cycle of the reference clock and transistor dimension of the phase detector. Consequently, the proposed PLL simultaneously demonstrates low in-band phase noise, low RMS jitter, and low reference spur while consuming low power. In order to lock the PLL robustly in case the VCO faces a sudden frequency disturbance, a low-power frequency-tracking loop without requiring an RF divider is further introduced. Measurement results suggest that the proposed PLL delivers high performance from 300 K down to 4.2 K.

Although the PLL presented in the previous chapter demonstrates low jitter and low spur, there is a limit on the minimum spur it can achieve due to the phase detector's output ripple. In Chapter 6, the first cryogenic PLL operating at 4.2 K is demonstrated in a 40-nm bulk CMOS process. This PLL targets quantum computing applications and is optimized for cryogenic operations by using the device model developed in Chapter 3. It incorporates a dynamic-amplifier-based phase detector for cryogenic operation. Thanks to the phase detector's high phase-detection gain, the proposed PLL achieves low in-band phase noise. It also achieves low spur due to minimized periodic disturbances on the VCO control. The PLL presented in this chapter meets

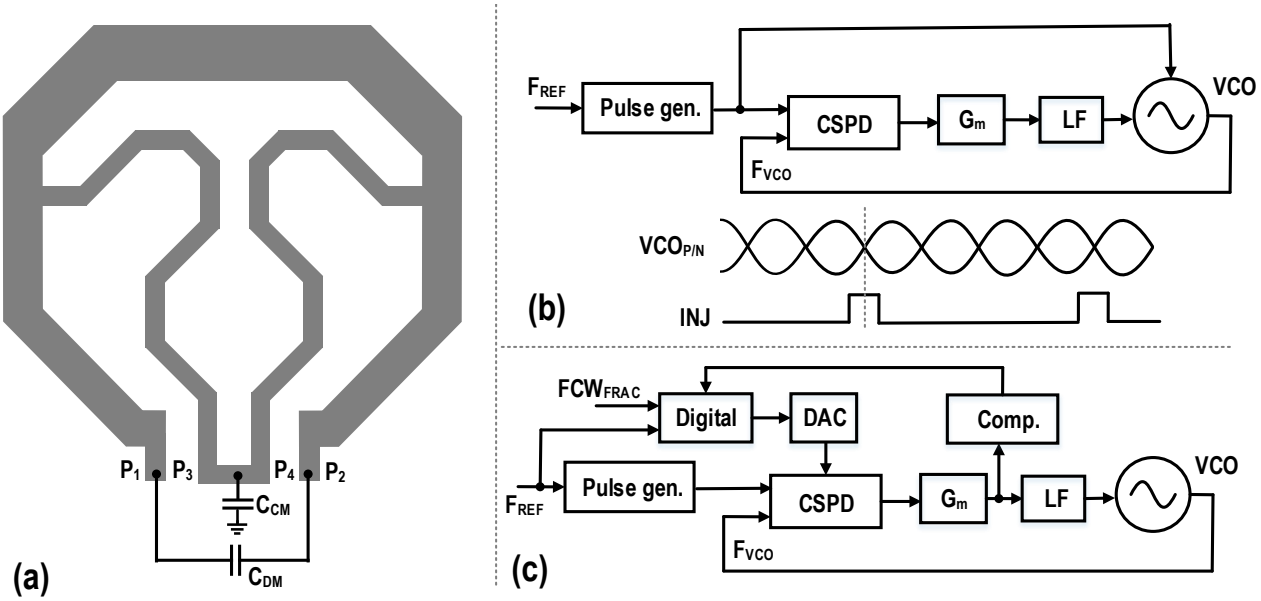

Figure 8.1: (a) Layout of the improved common-mode resonance oscillator;(b) block diagram of an injection-locked *LC* oscillator with the charge-sampling PLL as a background frequency-tracking loop; (c) block diagram of a fractional-N charge-sampling PLL.

the performance requirements for the qubit control, which marks a major step toward a fully-integrated qubit controller.

While the PLLs presented in previous chapters exhibit high performance over a wide temperature range, they have a limited frequency tuning range. It is highly desirable for a PLL which covers a wide frequency tuning range so as to target different types of qubits. Chapter 7 introduces a wide-tuning-range analog PLL in a 22-nm FinFET CMOS process. The tuning range of the PLL is extended by a dual-core triple-mode VCO. Specifically, three distinct resonant frequencies of the VCO are synthesized through the constructive/destructive magnetic coupling, coil current cancellation, and inductor shortcutting of a high-Q compact 4-port tapped inductor and the capacitive mode-switching. The PLL achieves the state-of-the-art FOM with a compact area and operates from 300 K to 4.2 K.

8.2 Some Suggestions for Future Developments

While this work presents the first step toward a fully-integrated cryogenic synthesizer that can be used in future fault-tolerant quantum computers, a few suggestions for future work are listed below:

- In Chapters 4 and 5, an inductor with a special shape is optimized to terminate the second-harmonic current of the oscillator properly. However, compared with a conventional single-turn inductor, the differential-mode quality factor of the optimized inductor is lower due to the small dimension of the sub-inductors. In a future design, a conventional single-turn inductor with a high differential-mode quality factor could still be used to conduct the fundamental current. Besides, the second-harmonic current could be terminated by two extra inductor legs, which are symmetrically placed inside the single-turn inductor. As shown in Fig. 8.1 (a), the proposed tapped inductor in Chapter 7 could be modified for this purpose.

- In oscillators using common-mode resonance techniques, the large single-ended capacitors from the parasitic capacitances limit the common-mode frequency, resulting in a common-mode frequency lower than the second harmonic frequency. I would suggest reducing the switch driver size for switched capacitors to impede common-mode current flowing to the parasitic capacitances. A similar method is proposed to avoid frequency tuning range reduction and phase noise degradation in an octave VCO in Chapter 7.

- At cryogenic temperatures, the phase noise of an oscillator is limited by shot noise. Consequently, the negative trans-conductance transistors should be implemented by long-channel devices to better enjoy phase noise reduction at 4.2 K. Without compromising the frequency-tuning range, the fixed capacitance of the oscillator should be reduced accordingly to accommodate the increased parasitic capacitances.

- In a conventional injection-locked LC oscillator (ILO), the injection timing must be calibrated in the background for stable jitter and spur performance. The ideal locking point of the proposed charge-sampling PLL is the same as an ILO (i.e., the reference pulse occurs at the middle of the VCO waveforms). Consequently, as shown in Fig. 8.1 (b), the charge-sampling PLL could be used as a background frequency-tracking loop in an injection-locked LC oscillator. The injection timing is automatically adjusted by the PLL over PVT variations and the complex injection timing calibration can be eliminated.

- In massive production, phase-detection gain should be characterized as part of the PLL bandwidth trimming over process variations. The phase-detection gain of the proposed phase detectors in Chapters 5 and 6 is highly dependent on the output common-mode voltage. Therefore, the output common-mode voltage of the phase detectors can be used as a sensing signal to calibrate the phase-detection gain.

- Due to the integration nature of proposed phase detectors in Chapters 5 and 6, the RF input ports (i.e., OSC_N and OSC_P in Fig. 5.2 and Fig. 6.2) can be driven by a square wave. Compared with a sine wave VCO, a wider linear range of the phase-detection characteristics can be realized, which preserves high phase-detection gain over a large input phase range. As shown in Fig. 8.1 (c), a voltage digital-to-analog converter (DAC) placed at the output of the phase detector could be used to cancel the phase error due to the fractional-N operation. A conventional digital-to-time converter (DTC) is eliminated in this topology as it contributes to high in-band phase noise.

- The maximum lock-in range of the presented frequency-tracking loop (FTL) in Chapter 5 is limited to $\pm F_{REF}/2$ as the clock frequency of the FTL is F_{REF}. In a future design, multiple reference clocks with different frequencies could be exploited to unambiguously calculate the frequency error for the FTL to realize an automatic coarse frequency tuning.

- The VCO contributes up to 80% of the total power of a charge-sampling PLL at room temperature, while the measured FOM of the VCO is limited to 187 dB. To push the PLL FOM further, it is thus beneficial to reduce the VCO power consumption while simultaneously maintaining its phase noise performance by using a more efficient VCO structure (e.g., common-mode resonance VCO with a tail inductor [135]) or reducing the VCO's frequency-tuning range.

Appendix

Appendix

A.1 Transistor Model

```
`include "constants.vams"
`include "disciplines.vams"
module nmos_model(d,g,s,b);
inout d,g,s,b;
electrical d,g,s,b;
real Ids1,Ids2,Ids;
real gm_cal ;
real Cdd,Css,Cgg;
real Qg=0,Qd=0,Qs=0;
parameter real W = 1200n;
parameter real L = 40n;
string Ws = "1200";
string Ls = "40";
string path = "/users/coolgrouplib/common_libs/
tsmc_N40_tbl_jiang/nmos_model/idc_save.tbl";
parameter string interpolation_mode = "1CL,1CL";
```

```
analog begin
    @(initial_step) begin
                case(W*1G)
                        1200:Ws="1200";
                        2000:Ws="2000";
                endcase
                case(L*1G)
                        40:Ls="40";
                        100:Ls="100";
                        240:Ls="240";
                        2000:Ls="2000";
                endcase
        // create caps
        Css = 0.000  * W * L;
        Cdd = 0.0000 * W * L;
        Cgg = 0.00   * W * L;
    end // initial step
        gm_cal = ddt(I(d,s))/ddt(V(g,s));
    if(V(d,s)>0)begin // d > s
  Ids1=$table_model(V(g,s), V(d,s),path,interpolation_mode);
        Ids=Ids1;      end
    else begin // s > d
 Ids2=$table_model(V(g,d), V(s,d),path,interpolation_mode);
 Ids=Ids2;      end
 I(d,s) <+ Ids+1*white_noise(2*`P_Q*0.5*Ids)+
 1*white_noise(4*`P_K*$temperature*1*gm_cal);
V(b) <+  gm_cal;
Qg = Cgg*V(g);
I(g) <+ ddt(Qg);
Qd = Cdd*V(d);
I(d) <+ ddt(Qd);
Qs = Css*V(s);
I(s) <+ ddt(Qs);
end
endmodule
```

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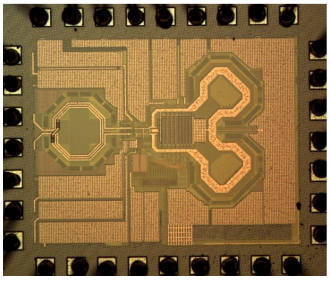
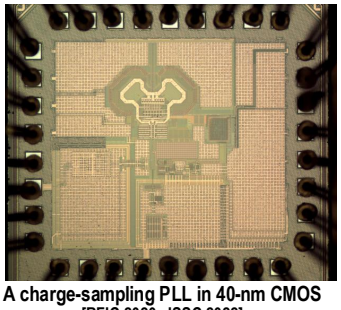
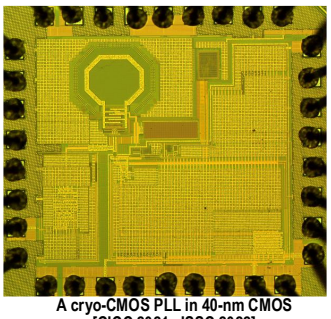
Chip Micrograph Gallery



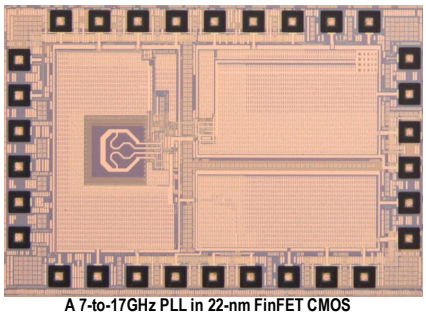
A 4-to-5GHz cryo-CMOS VCO in 40-nm CMOS
[ISSCC 2020, TCAS1 2022]



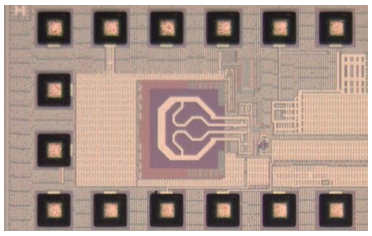
A charge-sampling PLL in 40-nm CMOS
[RFIC 2020, JSSC 2022]



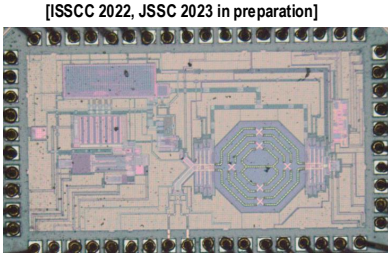
A cryo-CMOS PLL in 40-nm CMOS
[CICC 2021, JSSC 2022]



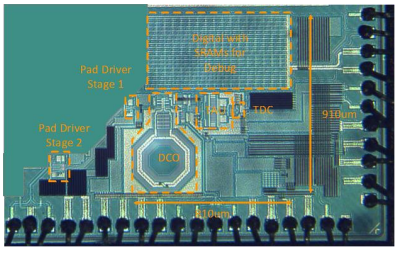
A 7-to-17GHz PLL in 22-nm FinFET CMOS
[ISSCC 2022, JSSC 2023 in preparation]



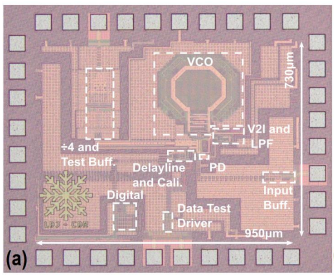
A 7-to-17GHz IQPLL in 22-nm FinFET CMOS



Supply insensitive digital PLL in 40-nm CMOS
[JSSC 2022] (with Yue Chen)



A low-spur DPLL based on Time-Mode Arithmetic Unit
[ISSCC 2022, JSSC 2022] (with Zhong Gao)



A cryo-CMOS charge-sampling CDR in 40-nm CMOS
[IMS 2023] (with Lennart de Jong)

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Jiang Gong (Student Member, IEEE) received a B.Sc. degree in Electrical and Electronic Engineering with distinction in 2015 from Jilin University, Changchun, China. He received an M.Sc. degree (cum laude) in Microelectronics from Delft University of Technology, Delft, the Netherlands, in November 2017, where he is currently pursuing the Ph.D. degree. In May 2022, he joined SiTime Netherlands as a senior analog/mixed-signal integrated circuit designer, focusing on phase-locked loop design for precision timing applications. His current research includes high-spectral-purity and wide-tuning-range frequency synthesizers, high-speed data converters, and high-precision analog design for wireless, wireline, and quantum computing applications.

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