Modulation of a Bidirectional DC-AC Converter for an AC Grid Interface in Bipolar DC Microgrids

by

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to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Thursday August 24, 2023 at 9:00 AM.

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Abstract

As renewable energy sources and DC energy storage continue to increase in modern power systems, the power electronic converters required to interface them with existing power grids are also rapidly increasing. This is resulting in increasing amounts of the total power exchanged on the grids being converted between DC and AC. Additionally, the majority of today's grid loads ultimately convert their input power to some form of DC whether they are connected to an AC or DC grid. Therefore, the concept of DC grids is becoming more attractive for applications such as DC distribution systems and electric vehicle charging stations. However, the existing AC grids will continue to play a fundamental role in the power infrastructure. Therefore, it is, important to consider how LVDC distribution grids will be connected to, and exhange power with, the AC grid. A transformerless interface between LVDC distribution grids and the LV AC grid via a power electronic converter is an attractive option in terms of size and cost reduction. However, the challenge of ground leakage current is a major challenge for such an interface.

This thesis assesses the different possible three-phase DC-AC converter topologies for a transformerless interface between a bipolar DC microgrid and the LV AC grid. The DC-AC converter modulation is explored to understand the challenges of ground leakage current and determine the feasibility of a transformerless interface. A detailed analysis of the common-mode voltage, common-mode impedance and resulting circulating currents in a grid-tied DC-AC converter is performed. The effect of this circulating current on AC grid protection equipment is considered.

A survey of converter modulation methods for common-mode reduction and DC bus voltage balancing is conducted. Simulations are used to verify the performance of the different modulation methods in terms of common-mode reduction and DC balancing capabilities in the bipolar DC grid. A new modulation method is proposed for simultaneously mitigating ground leakage current and providing DC voltage balancing. The limitations of this method are analyzed and simulations are performed to evaluate its effectiveness. The developed modulation method is also shown to eliminate the low-frequency voltage ripple in the DC bus caused by the conventional modulation methods. An experimental hardware prototype DC-AC converter is designed and built for testing the different modulation methods. Finally, recommendations for future work are made.

Acknowledgement

I would like to express my sincerest gratitude to the many people who support me throughout the journey of this thesis work. I would not have been able to complete this journey without your tireless and steadfast encouragement, guidance, patience and love.

First and foremost, tremendous thanks goes to my incredible family who supported me from the start of this journey abroad for my graduate studies, as well as from long before. To my parents and sister, your support of me throughout all my years of education and career has been such a source of joy during peaceful times, and a beacon of hope and reassurance during the more challenging periods. I cannot thank you enough and I am extremely grateful to have you in my life.

To my friends and colleagues at TU Delft, thank you for undertaking this challenging academic program with me. You have given me new perspectives on many aspects of life, both professional and personal, that I will carry with me for the rest of mine. You helped me to grow and push the boundaries of my abilities, and you made me feel at home so far away from home. Thank you for all the great memories.

A very special thank you is owed to Dr. Laurens Mackay and Ir. Gerasimos Maroulis for the opportunity to work on this thesis project. Your advisement and supervision throughout the thesis has been extremely valuable. I have learned a great deal from you during this thesis and I look forward to our continued work together at DC Opportunities.

I would like to extend a special thank you to Dr. Zian Qin and Ir. Sachin Yadav from the TU Delft DCE&S department. The discussions and feedback you provided were invaluable and contributed greatly to the thesis work. I would also like to thank Prof. Pavol Bauer and Dr. Aleksandra Lekic for serving on my thesis committee and providing their evaluation of my work.

Last and far from least, I would like to express my deepest gratitude to my girlfriend, Sara, who came on this journey abroad to the Netherlands with me. You have been with me through each moment, good and bad. You have embraced this chaotic period of our lives and given me unending love and encouragement through all of my doubts and hesitations. I am extremely fortunate and grateful to have a partner as amazing as you.

Kyle McNeil
Delft, August 2023

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List of Abbreviations

2-L	Two-Level
3HRE	Third Harmonic Ripple Elimination
3-L	Three-Level
3-ϕ	Three-Phase
AC	Alternating Current
ANPC	Active Neutral-Point Clamped
CHB	Cascaded H-Bridge
DC	Direct Current
DPWM	Discontinuous Pulse-Width Modulation
EMC	Electromagnetic compatability
ESS	Energy Storage System
EV	Electric Vehicle
FC	Flying Capacitor
FFT	Fast Fourier Transform
GTO	Gate Turn-off Thyristor
IC	Interleaved Carrier
IGBT	Insulated Gate Bipolar Transistor
LF	Low-Frequency
LV	Low Voltage
LVDC	Low Voltage Direct Current
M^2ZV	Two medium vector - one zero vector
MCU	Microcontroller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
NPC	Neutral-Point Clamped
NTV	Nearest Three Vector
PCB	Printed Circuit Board
PD	Phase Disposition
PE	Protective Earth
PF	Power Factor
POD	Phase Opposition Disposition
PSC	Phase-Shifted Carrier
PV	Photovoltaic
PWM	Pulse Width Modulation
RCD	Residual Current Detector
RZV	Redundant Zero Vector
SiC	Silicon Carbide
SMD	Surface Mount Device
SPCMB	Switching Period Common-Mode Balancing
SPWM	Sinusoidal Pulse-Width Modulation
SVM	Space-Vector Modulation

THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
WBG	Wide-bandgap

List of Symbols

α	Stationary reference frame horizontal axis
β	Stationary reference frame vertical axis
C_b	DC bus lower capacitance
C_{DC-GND}	DC grounding capacitance
C_{DC-BUS}	DC bus capacitance
C_f	LCL filter capacitance
C_{iw}	Inter-winding capacitance
C_{par}	Parasitic capacitance
C_t	DC bus upper capacitance
DC_N	Bipolar grid neutral conductor
Δs	DC bus voltage imbalance control variable
ϵ	DC load ratio
F_f	RCD frequency factor
f_{grid}	AC grid frequency
f_{sw}	Switching frequency
I_{cm}	Common-mode current
I_{cm-Cf}	LCL filter capacitance common-mode current
I_{gl}	Ground leakage current
i_{np}	DC neutral-point current
i_ϕ	Phase current
I_{th}	RCD tripping threshold current limit
j	Complex unit
L_{CMC}	Common-mode choke inductance
L_{grid}	Grid inductance
L_N	Bipolar grid negative conductor
L_P	Bipolar grid positive conductor
m_a	(Amplitude) modulation index
N	Number of converter levels
NP	DC neutral-point
ϕ	Relative phase angle
θ	Instantaneous phase angle
P_b	Split DC bus lower load
$P_{inverter}$	Inverter active power
P_t	Split DC bus upper load
$Q_{inverter}$	Inverter reactive power
R_{damp}	Damping resistance
S_{sw}	Number of valid converter switching states
$SV_{cmv-bal}$	Small state vector common-mode volt-second balance
t_d	Dead-time
T_{fund}	Fundamental period
T_{sw}	Switching period

$\bar{V}$	Voltage space vector
$\bar{V_{ref}}$	Voltage reference space vector
V_b	Split DC bus lower voltage
V_N	Bipolar DC grid negative pole voltage
V_P	Bipolar DC grid positive pole voltage
V_t	Split DC bus upper voltage
$V_{AC-grid}$	AC grid voltage
V_{cm}	Common-mode voltage
V_{cm-vs}	Common-mode voltage volt-second balance
V_{DC}	DC bus voltage
V_m	AC voltage amplitude
$V^+_{DC-grid}$	Bipolar grid positive pole voltage
$V^-_{DC-grid}$	Bipolar grid negative pole voltage
ω	fundamental frequency
Z_{cm}	Common-mode impedance
$Z^+_{DC-grid}$	Bipolar grid positive pole impedance
$Z^-_{DC-grid}$	Bipolar grid negative pole impedance

Chapter 1: Introduction

With the increasing proliferation of renewable energy sources and DC energy storage in modern power systems, the power electronic converters required to interface them with existing power grids are also rapidly increasing [1] [2]. This is resulting in increasing amounts of the total power exchanged on the grids being converted between DC and AC. Additionally, the majority of today's grid loads ultimately convert their input power to some form of DC whether they are connected to an AC or DC grid [3]. Therefore, the concept of DC grids is becoming more attractive for applications such as DC distribution systems and electric vehicle charging stations. In such applications, DC grids have the potential to eliminate/simplify power conversion steps, thereby increasing power system efficiency and reducing costs. DC grids also enable renewable energy resources such as photovoltaic (PV) solar and wind energy, as well as DC energy storage systems (ESSs), to be more directly integrated into power distribution systems [4]. DC grids further simplify the integration of distributed energy resources and energy storage because they eliminate the need for phase synchronization and reactive power control that is crucial in AC grids, reducing the control complexity and power quality requirements of the interfacing power electronic converters [5].

Compared with traditional AC power grids, DC grids are much less well-established in the modern era of electrical power systems. However, in recent years, efforts have been made towards the development of DC grid standards, namely for low-voltage (LV) DC distribution grids. The European Union's Directive 2014/35/EU establishes the voltage range for LVDC systems as 75 to 1500 V. The Netherlands is the first country to publish a national standard (practice directive) for the design and installation of LVDC and combined LVDC and AC systems with the NPR 9090:2018 [6]. This standard specifies the voltage range for LVDC distribution grid systems as 350 V to 1400 V and establishes a DC grid grounding specification for safety and protections. Efforts have also been made by the International Electrotechnical Commission (IEC) to establish standardization for LVDC power system installations [7]. The development of these standards bodes well for more DC distribution systems in the future.

There are two main architectures currently considered for DC distribution grids: unipolar (also known as monopolar) and bipolar [8]. The unipolar DC grid architecture consists of two conductors with one DC voltage established between them. Grid sources and loads are connected between the two conductors. The bipolar DC grid architecture consists of three conductors: a positive rail conductor, negative rail conductor and neutral conductor. One DC voltage is established between the positive and negative rails. The neutral conductor voltage is then nominally maintained halfway between the positive and negative rail voltages, resulting in two DC voltages to which sources and loads can be connected. While implementation and regulation of the unipolar architecture is generally less complex, the bipolar architecture enables increased grid flexibility, stability and fault tolerance. Additionally, the bipolar architecture can reduce the voltage conversion required for a wider range of source and load voltages due to the two available voltage levels, thereby, increasing the efficiency of the power electronic converters in the DC grid system. These advantages in the bipolar architecture have resulted in increased interest from research in recent years. Accordingly, this work focuses on the application of a bidirectional DC-AC power converter as an interface be-

tween a bipolar DC microgrid and the LV AC power grid.

The bipolar DC grid has the potential to increase the overall stability and resilience of modern power grid systems, and to make the integration of distributed energy resources into the power infrastructure more seamless. However, the existing AC grids will, of course, continue to play a fundamental role in the power infrastructure. Therefore, it is, important to consider how LVDC distribution grids will be connected to, and exhange power with, the AC grid. This work investigates some of the potential challenges to connecting the two types of grids and develops a solution for a specific use-case of a bipolar DC microgrid.

1.1 Bipolar DC Microgrid System

As previously explained, the bipolar DC grid architecture consists of a positive, negative and neutral conductor, and has two different voltage levels. The emerging LVDC grid standards are moving towards a standard LVDC bipolar grid nominal voltage of ±700 V which will be considered in this work. This equates to a nominal voltage of 700 V between each DC rail and the neutral conductor, and a nominal voltage of 1400 V between the two DC rails. The general structure of this bipolar grid is shown in Figure 1.1 with the positive, negative and neutral conductors denoted as L_P, L_N and DC_N, respectively. The bipolar DC grid use-case considered here is comprised of a PV array connected to the grid through maximum power point tracking (MPPT) DC-DC converters, battery energy storage, and DC loads. The DC loads on the grid can consist of lighting and electric vehicle (EV) chargers, for example, in the case of a PV-covered parking lot. As per the emerging LVDC grid standards, capacitive grounding is considered for the bipolar DC grid, where capacitors are placed between DC_N and protective earth (PE) at various grounding points in the grid. This enables transient AC components in the DC grid neutral voltage to be grounded while still maintaining electrical isolation between the conductors and PE.

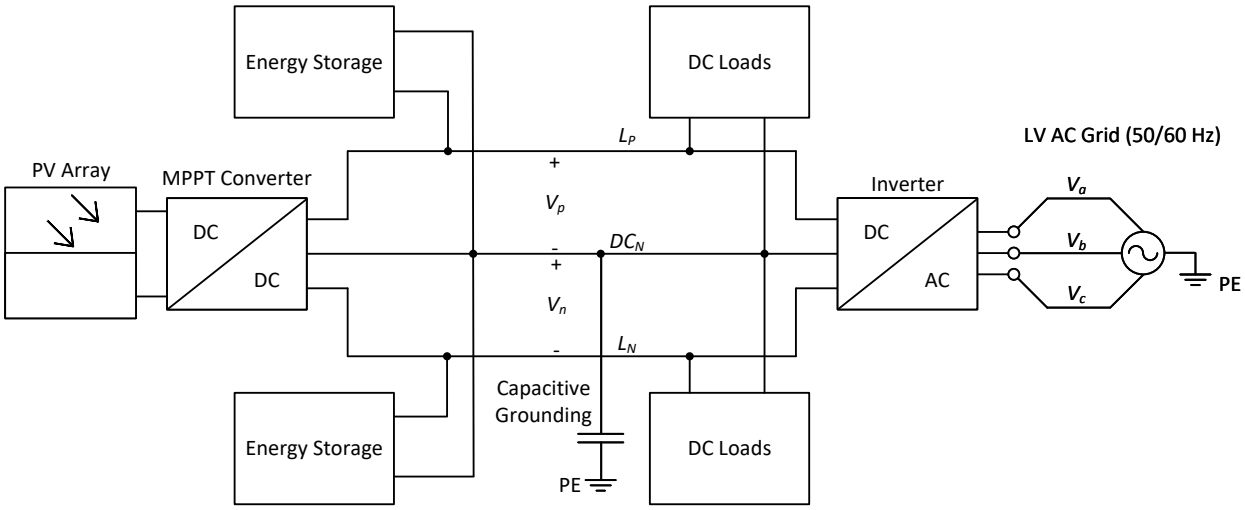


Figure 1.1: General architecture of bipolar DC grid with LVAC grid interface converter

1.2 Transformerless LVAC Grid Interface

In AC grid-connected DC-AC inverter applications, such as in PV arrays, there is often a low-frequency (LF) transformer between the inverter and the AC grid [9] [10]. The LF transformer provides galvanic isolation between the inverter and AC grid, as shown in Figure 1.2. Having galvanic isolation between the inverter and AC grid prevents ground leakage currents from flowing between the AC grid neutral-point and the inverter DC bus terminals due to the common-mode

voltage (V_{cm}) that results from the inverter modulation switching. In the case of an inverter connected to a PV array, these currents will flow between PE and the terminals of the PV panels by way of the parasitic capacitance, C_{par}, between the panels and the earth [11]. If there is a connection of the AC grid neutral-point to PE at a point up the line from the inverter connection, such as at a wye-connected distribution transformer, ground leakage current, I_{gl}, can flow between the AC grid neutral point and the inverter DC bus terminals, as shown in Figure 1.3.

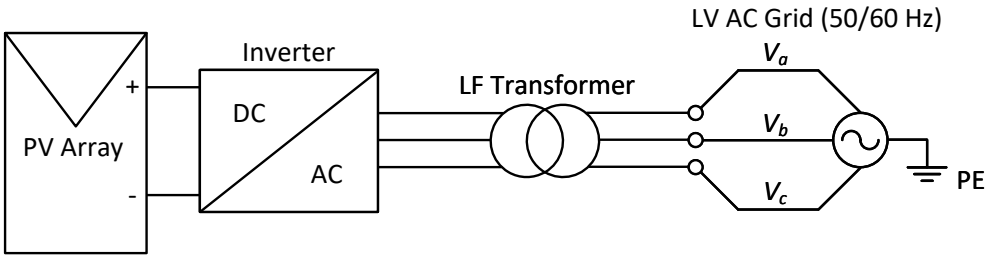


Figure 1.2: Grid-connected inverter with LF transformer interface

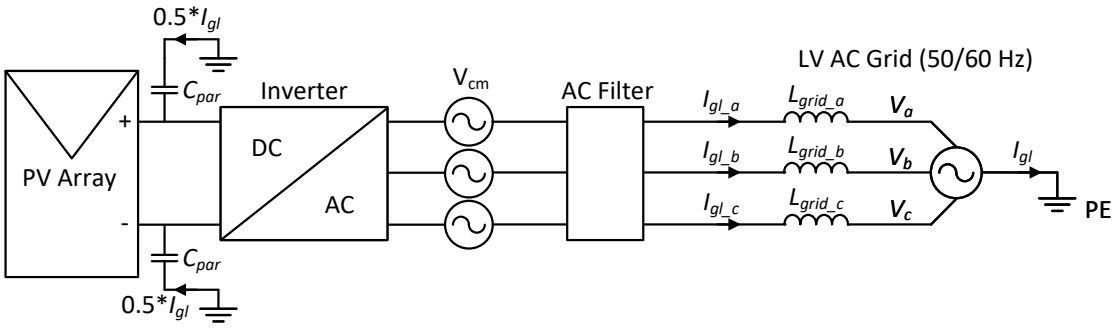


Figure 1.3: Ground leakage current in PV array due to PV inverter common-mode voltage

These ground leakage currents can interfere with protection equipment, such as residual current detectors (RCDs), installed between the inverter and any AC grid neutral-point PE connections. This is because the RCDs are designed to detect net current flowing in the three phases of the AC grid that does not return on a neutral conductor. Such current must flow to ground and typically indicates a ground fault. A ground fault can be caused by a person, animal or object coming into contact with the grid voltage while touching the ground, or an insulation failure in a conductor. The purpose of an RCD is to "trip" and open the grid circuit when ground leakage current is detected in order to isolate the fault. However, RCDs are not designed to distinguish ground leakage current caused by a ground fault versus the V_{cm} of a grid-connected power converter. Therefore, this V_{cm} and the resulting ground leakage current can cause the RCDs to trip even when no ground fault is present, preventing proper operation of the grid and the installed protection devices.

A LF transformer prevents ground leakage currents due to inverter V_{cm} because it presents a very high capacitive impedance to the V_{cm} component of the inverter output voltage. However, LF transformers are relatively large and expensive and, therefore, increase the overall size and cost of an inverter grid connection. A common alternative is to place an isolated DC-DC converter between the inverter and the DC source [9] [10] [12]. This configuration is shown in Figure 1.4. The isolated DC-DC converter provides galvanic isolation with a high-frequency transformer which reduces the transformer size and cost while still preventing ground leakage currents from flowing into the AC grid. However, this configuration results in an additional power conversion step, resulting in higher system cost and complexity, and lower system efficiency, compared to a non-isolated (transformerless) connection of the inverter to the AC grid, shown in Figure 1.5. As the

use of DC-AC power electronics converters to interface renewable energy resources and DC energy storage systems to the AC grid increases, reducing the size, cost and complexity of these interfaces by having transformerless connections will be highly beneficial.

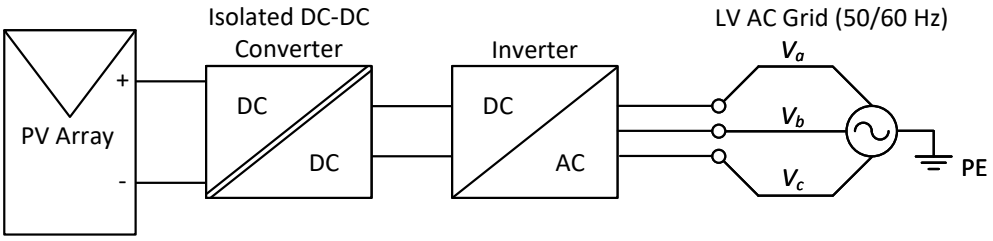


Figure 1.4: Galvanic isolation using isolated DC-DC converter in grid-connected PV array system

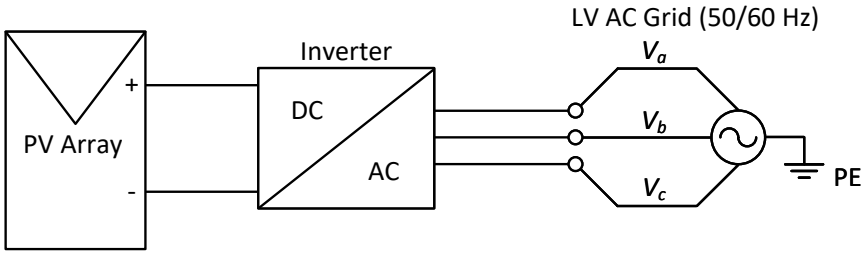


Figure 1.5: Transformerless grid-connected PV inverter

1.3 Three-Level Bidirectional Inverter Topology Comparison

In a conventional two-level (2-L) three-phase (3-ϕ) voltage source inverter (VSI) topology, shown in Figure 1.6, the power switching devices must be capable of blocking the full DC bus voltage, V_{DC}, at the DC-side of the inverter. In the case of the considered bipolar DC grid, this voltage is nominally 1400 V and can fluctuate as high as 1500 V per the existing LVDC grid standards. Considering a 20% margin between the device rated voltage and the maximum voltage at the device power terminals, switching devices with a voltage rating of at least 1875 V would be required in the two-level topology. This requirement of the 2-L topology eliminates the possibility of using wide-bandgap (WBG) Silicon Carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) which have become commercially available, in recent years, at voltage levels of 1000, 1200 and 1700 V. The WBG devices have significantly lower switching losses compared to equivalent conventional Silicon-based MOSFETs and insulated gate bipolar trasistors (IGBTs), enabling higher converter performance in efficiency and power density [13] [14] [15].

Due to the bipolar DC grid architecture and voltage levels, several multi-level 3-ϕ VSI topologies were considered in order to enable the use of 1200 or 1000 V SiC MOSFETs for the inverter switching devices. The multi-level topologies also produce less harmonics in their output voltages compared to the two-level topology due to the higher number of output voltage levels that can be generated [16] [17]. While this feature is not rigorously analyzed in this work, it is an important general consideration in many inverter applications.

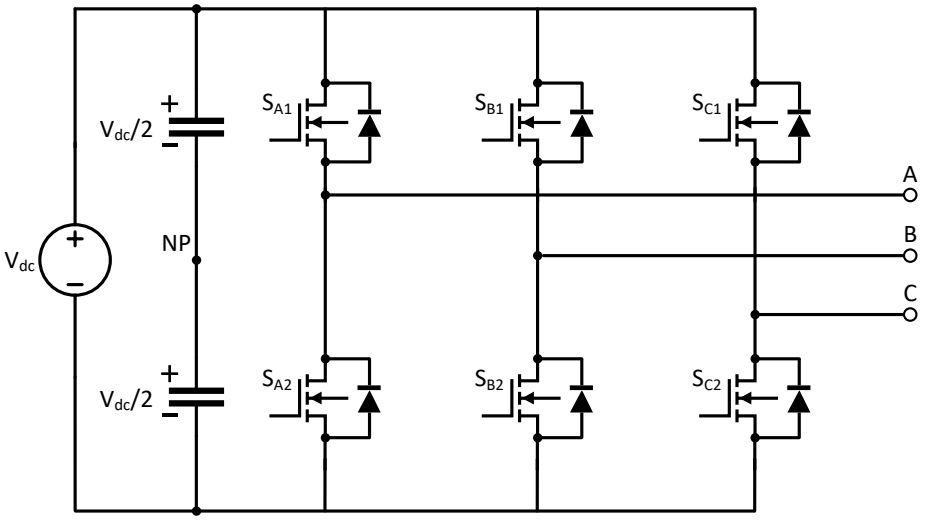


Figure 1.6: Two-level voltage source inverter

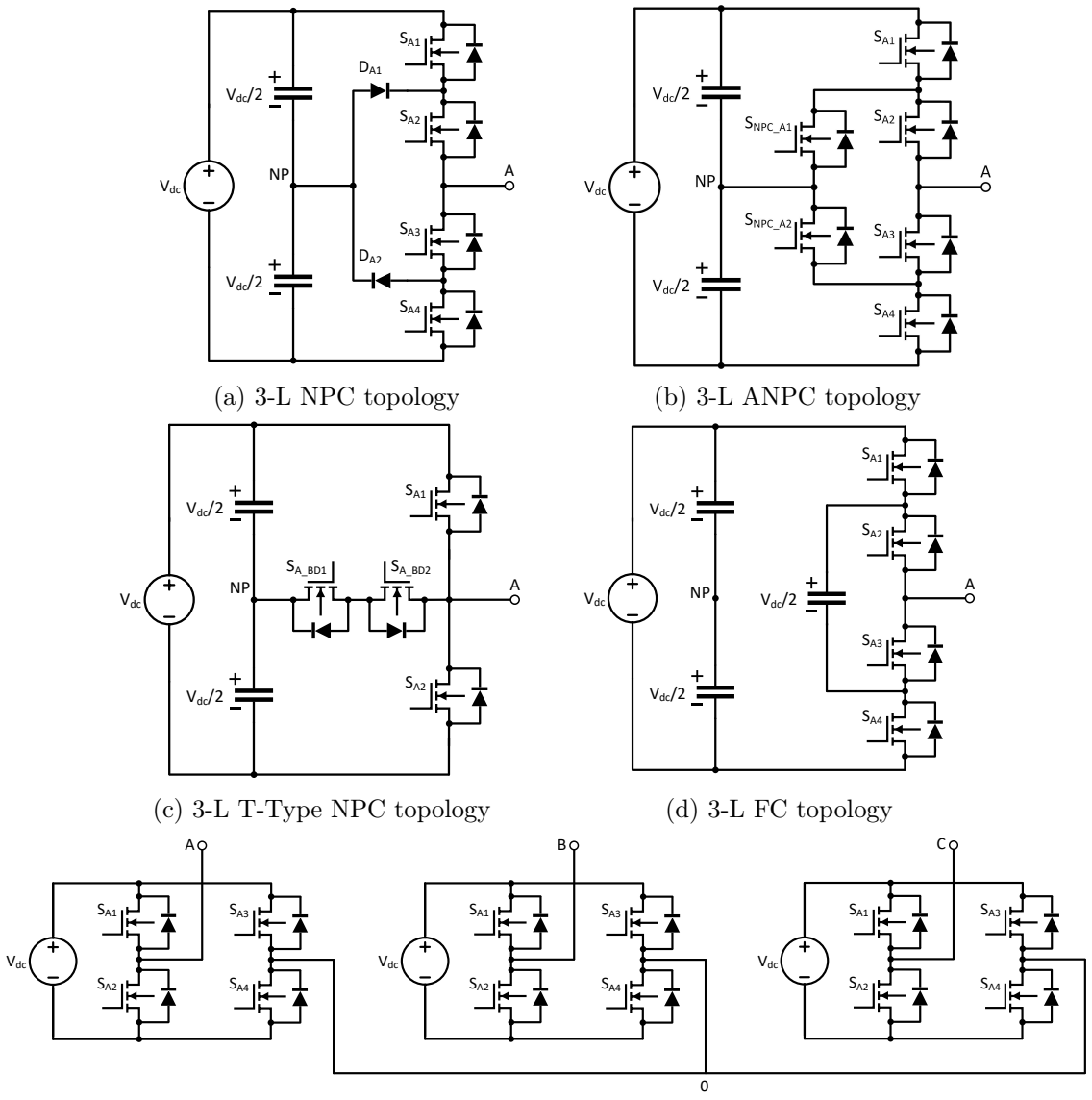
The considered multi-level topologies are listed in Table 1.3 and their architectures are shown in Figure 1.7. A single phase leg of each topology is shown in Figure 1.7, except for the cascaded h-bridge (CHB) topology. The three-level (3-L) neutral-point-clamped (NPC) topology, first proposed in [18] and shown in Figure 1.7(a), consists of four switching devices and two diodes per phase leg. Each switching device and diode must only block half of V_{dc} making this topology advantageous for higher DC voltage levels. The main drawbacks of this topology are problems balancing the DC bus capacitor voltages and uneven loss distribution in the four semiconductor switches of each phase leg [19]. However, methods for balancing the DC bus have been established. Additionally, it is well suited for the bipolar DC microgrid application because it enables a connection of the converter to the DC neutral point, *NP*. As will be discussed in Chapter 4, this connection is important for the DC-AC converter to provide balancing capabilities for the bipolar DC grid itself. A variant of the NPC topology is the active NPC (ANPC) topology, shown in Figure1.7(b), in which the clamping diodes are replaced with active switches, enabling control of where the neutral point current in each phase leg flows [20].

The 3-L T-Type NPC topology, shown in Figure 1.7(c), achieves the same number of output voltage levels as the NPC and ANPC topologies and eliminates the clamping diodes required in the NPC topology. However, the top and bottom switching devices, S_{A1} and S_{A2}, must block V_{dc}. The 3-L flying capacitor (FC) topology, shown in Figure 1.7(d), also achieves the same number of output levels as the NPC and ANPC topologies. Instead of clamping diodes, it utilizes a capacitor connected between the drain-source connections of the top two switches and bottom two switches. The capacitor voltage is maintained at a voltage of $\frac{1}{2}V_{dc}$ to ensure that each of the switches only blocks half of the DC bus voltage. However, this topology cannot achieve a connection to the DC bus neutral-point and, therefore, cannot provide active voltage balancing for the DC bus.

The CHB topology, shown in Figure 1.7(e), also achieves three output voltage levels with two additional voltage levels for each additional stage of CHBs, and does not require clamping diodes like in the NPC topology. However, the CHB topology requires an isolated DC source for each stage of CHBs and, therefore, cannot be directly connected to L_P, L_N and DC_N of the bipolar DC microgrid system like the NPC, ANPC and T-Type topologies.

Table 1.3: Considered Three-Level Bidirectional DC-AC Converter Topologies

Topology	**Max. Switch Blocking Voltage**	**Neutral-Point Connection**
NPC	$\frac{V_{dc}}{2}$	Yes
ANPC	$\frac{V_{dc}}{2}$	Yes
T-Type NPC	V_{dc}	Yes
FC	$\frac{V_{dc}}{2}$	No
CHB	$\frac{V_{dc}}{2}$ (five-level)	No



(a) 3-L NPC topology

(b) 3-L ANPC topology

(c) 3-L T-Type NPC topology

(d) 3-L FC topology

(e) 3-L CHB topology (three-phases shown)

Figure 1.7: Considered three-level bidirectional DC-AC converter topologies

The NPC topology was selected for this application because it is the only topology of those considered, in addition to the ANPC topology, which ensures each switching device blocks $\frac{1}{2}V_{dc}$ and a connection to the bipolar DC microgrid can be made to provide DC grid voltage balancing. The schematic of the NPC converter connected between the bipolar DC microgrid and the LV AC grid

with a transformerless connection is shown in Figure 1.8. This work does not consider the loss distribution in the converter phase leg switches so the ANPC topology is not considered.

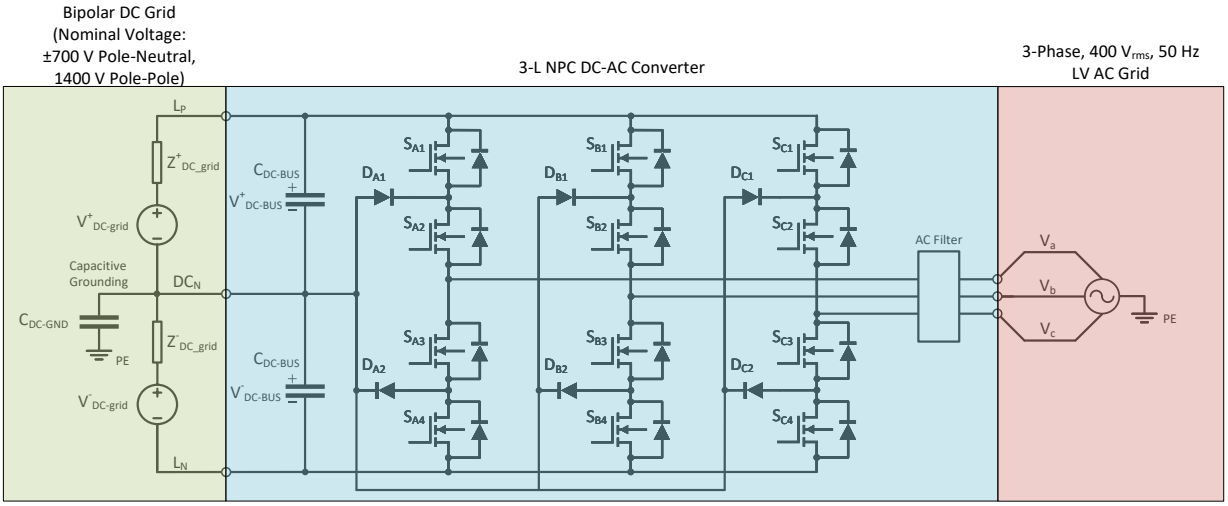


Figure 1.8: Schematic of NPC converter connected between bipolar DC microgrid and LV AC grid

1.4 Research Questions

The objective of this thesis is to develop modulation methods for the 3-L 3-ϕ NPC DC-AC converter for reducing or eliminating the ground leakage currents caused by the converter in order to make a transformerless connection of a bipolar DC microgrid system to the LV AC grid feasible. DC pole balancing in the bipolar DC microgrid system is essential to its operation. Therefore, it is desired for the developed modulation method to allow for the converter to simultaneously provide DC pole balancing and reduce/eliminate ground leakage currents. Thus, the research questions addressed in this thesis are the following:

1. What are the existing modulation methods for reducing/eliminating common-mode current in the 3-L 3-ϕ NPC DC-AC converter?
2. What are the existing modulation methods for active DC bus voltage balancing in the 3-L 3-ϕ NPC DC-AC converter?
3. Can the AC grid-connected 3-L 3-ϕ NPC DC-AC converter be modulated such that it can simultaneously keep ground leakage currents below protection equipment tripping thresholds and provide active DC pole voltage balancing?

1.5 Overview of Chapters

The thesis consists of six chapters and an overview of each chapter is given below.

- Chapter 1 provides background information on the project and bipolar DC microgrid systems, develops the general motivation for the research and introduces the main challenges associated with the research objectives. It also introduces the 3-L NPC DC-AC converter topology and explains why it was selected for this research.
- Chapter 2 introduces the fundamental concepts of the two main modulation methods used in DC-AC converters. It sets the framework for sinusoidal pulse-width modulation (SPWM)

and space vector modulation (SVM) with which the approach and results of Chapters 3, 4 and 5 will be discussed.

- Chapter 3 presents the analysis of common-mode voltage and the resulting common-mode current in a grid-connected 3-L NPC converter. It also gives an overview of the issue ground leakage current presents for protection devices in AC systems. A survey and analysis of the existing methods for reducing/eliminating common-mode current is provided. Finally, a modulation method for reducing ground leakage current caused by the grid-connected 3-L NPC converter is proposed and simulation results are presented.

- Chapter 4 presents the analysis of DC bus voltage balancing in the 3-L NPC converter and bipolar DC microgrid systems. An overview of the existing modulation methods for balancing the DC bus voltages in the 3-L NPC is given. This overview includes methods that are designed to achieve both DC bus voltage balancing and common-mode current reduction. Finally, a modulation method for simultaneously providing active DC pole voltage balancing and keeping ground leakage current below the tripping thresholds of the AC protection devices is proposed and simulation results are presented.

- Chapter 5 presents the 3-L NPC converter hardware prototype designed for experimental demonstration in this research. The experimental results of the NPC converter operating unloaded at low DC bus voltage are presented to demonstrate some of the modulation methods. Suggestions for future testing are made.

- Chapter 6 summarizes the thesis research and presents the final conclusions on the findings. Suggestions for future research and analysis are also provided.

Chapter 2: Overview of Pulse-Width Modulation

Pulse-width modulation (PWM) is one of the most prevalent methods for controlling the switches of modern voltage source DC-AC converters, as well as numerous other types of power converters and amplifier systems, in order to synthesize the desired output voltages and currents. The theory and practical implementation of PWM for power converters has been built up and firmly established for more than six decades and will continue to form the basis by which a large portion of power converters are operated for the foreseeable future [21]. This chapter presents an overview of the fundamental concepts of PWM and provides a framework with which the 3-L 3-ϕ NPC converter modulation will be discussed in the subsequent chapters. The overview focuses on the two main types of PWM used in DC-AC converters.

2.1 Carrier-Based Sinusoidal Pulse-Width Modulation

The first type of PWM for DC-AC converters analyzed in this work is carrier-based sinusoidal PWM (SPWM). Carrier-based SPWM is one of the most commonly implemented modulation methods for DC-AC converters. For the 2-L 3-ϕ inverter shown in Figure 1.6, SPWM is generally implemented by generating sinusoidal phase reference waveforms with the inverter modulation circuitry and comparing them with a triangular or sawtooth carrier waveform to generate the modulator pulses. The carrier waveform frequency determines the switching frequency, f_{sw}, of the converter. The 3-ϕ reference waveforms and a triangular carrier waveform are shown in Figure 2.1. The modulator output of a phase is set to 1 if the phase reference waveform is greater than the carrier waveform and 0 if the phase reference waveform is less than the carrier waveform. The modulator pulse generation for the phase A reference waveform is shown in Figure 2.2. These pulses are then used to generate the on/off signals for the control pins of the converter switches. Table 2.1 lists the switch states of the 2-L 3-ϕ inverter corresponding to the modulator output for phase A. The same is applied for phases B and C, resulting in the synthesis of sinusoidal 3-ϕ voltages at the inverter output. The output voltages also contain a f_{sw} component in their frequency composition due to the PWM. A low-pass filter is placed at the inverter output to attenuate the output voltage f_{sw} component and achieve a sinusoidal AC output.

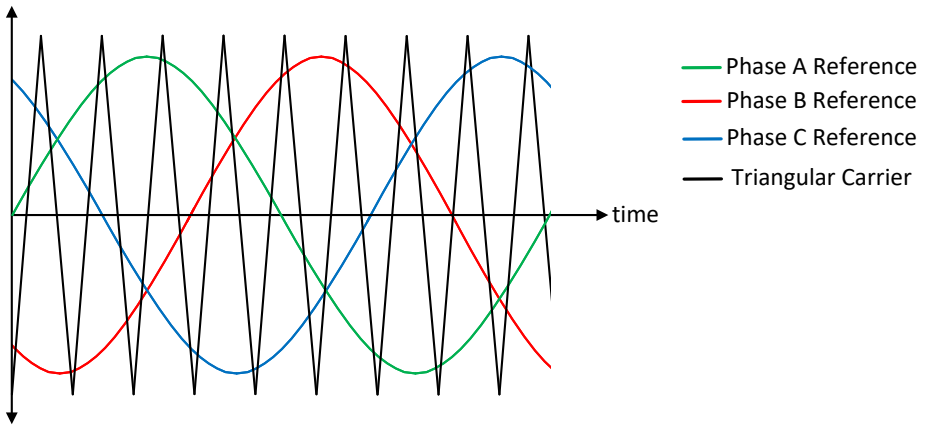


Figure 2.1: Two-level three-phase carrier-based SPWM reference and triangular carrier waveforms

Table 2.1: Two-Level Three-Phase Inverter Phase A Modulator Output and Switching States

Modulator Output (Phase A)	**S_{A1} State**	**S_{A2} State**
0	OFF	ON
1	ON	OFF

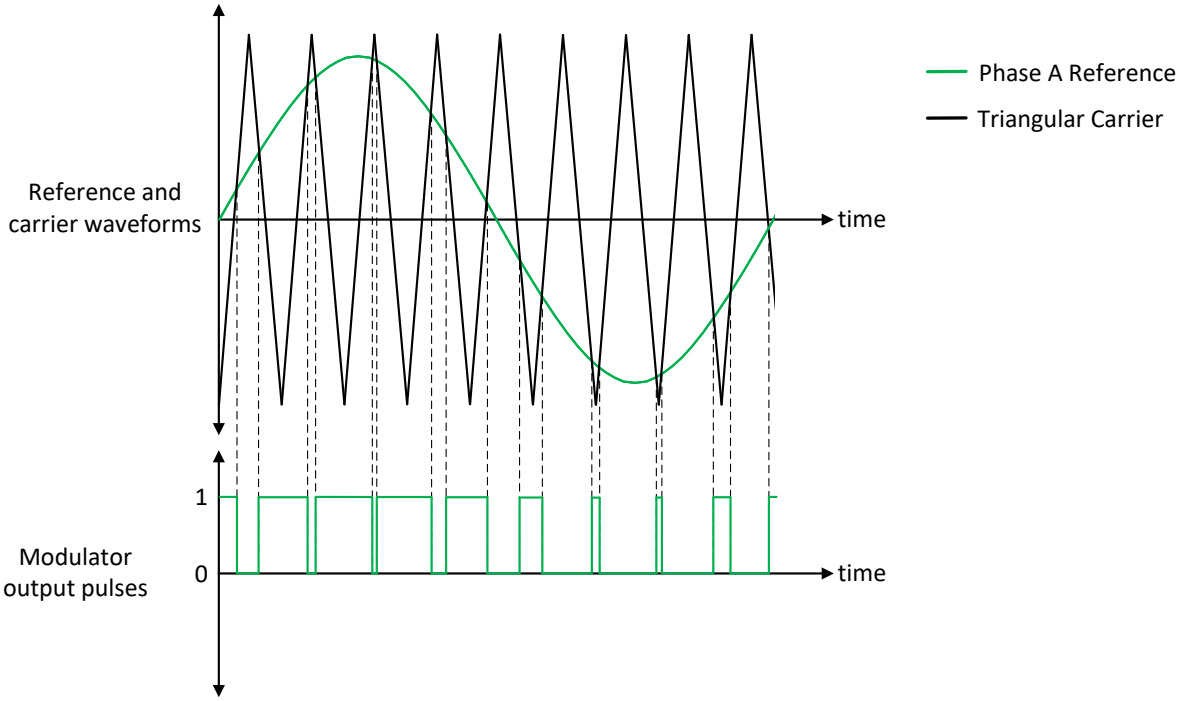
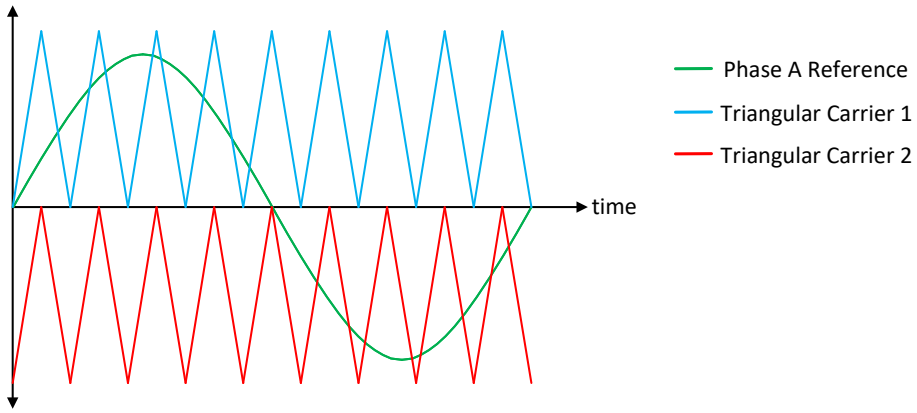


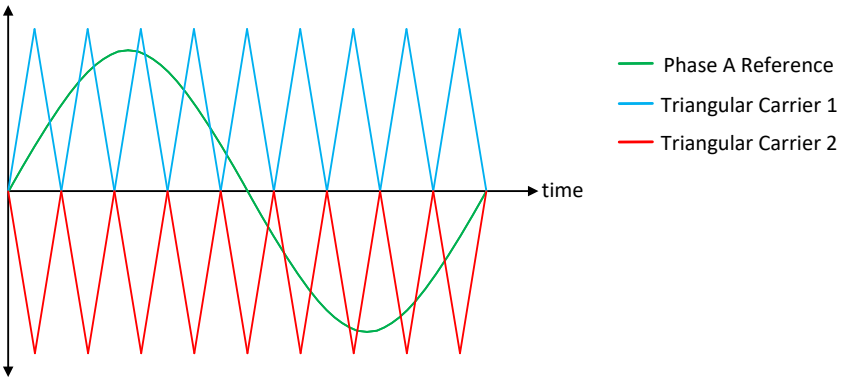
Figure 2.2: Two-level three-phase carrier-based SPWM phase A modulator output pulses

Carrier-based SPWM can be extended to 3-L inverters by adding an additional carrier waveform. A variety of 3-L SPWM types can be realized by level-shifting or phase-shifting the two carrier waveforms with respect to one another. In 3-L phase disposition (PD) SPWM, the carrier waveforms are in phase and level-shifted, as shown in Figure 2.3(a). In 3-L phase opposition disposition (POD) SPWM, the carrier waveforms are level-shifted as in PD SPWM and they are also phase-shifted by

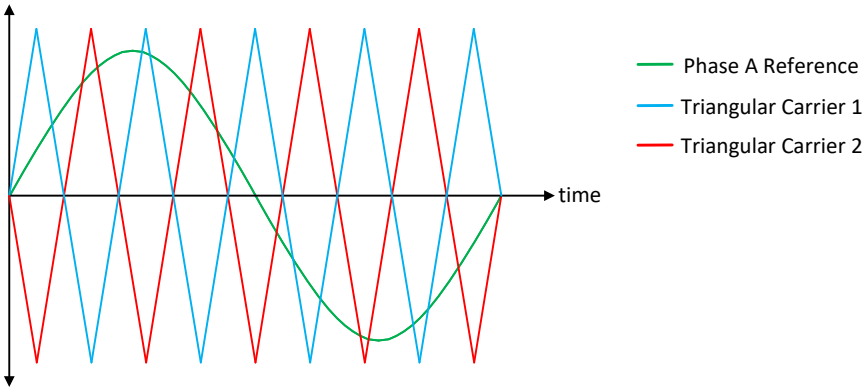
180°, as shown in Figure 2.3(b). In 3-L phase-shifted carrier (PSC) SPWM, there is no level-shift between the two carrier waveforms and they are phase-shifted by 180°, as shown in Figure 2.3(c).



(a) Three-level PD SPWM phase A reference and carriers



(b) Three-level POD SPWM phase A reference and carriers



(c) Three-level PSC SPWM phase A reference and carriers

Figure 2.3: Three-level carrier-based SPWM types

Similar to 2-L SPWM, each phase reference is compared with the carrier waveforms to generate the modulator output. However, each phase of the 3-L converter has three possible switching states compared to only two in 2-L SPWM. Therefore, the modulator output of a phase is set to 1 if the phase reference waveform is greater than both carrier waveforms, 0 if the phase reference waveform is less than one carrier waveform and greater than the other, and -1 if the phase reference waveform is less than both carrier waveforms. The 3-L modulator pulse generation for the phase A reference waveform with PD SPWM is shown in Figure 2.4. These pulses are then used to generate the on/off signals for the control pins of the converter switches similar to 2-L SPWM. Table 2.2 lists the switch states of the 3-L 3-ϕ NPC inverter corresponding to the modulator output for phase A.

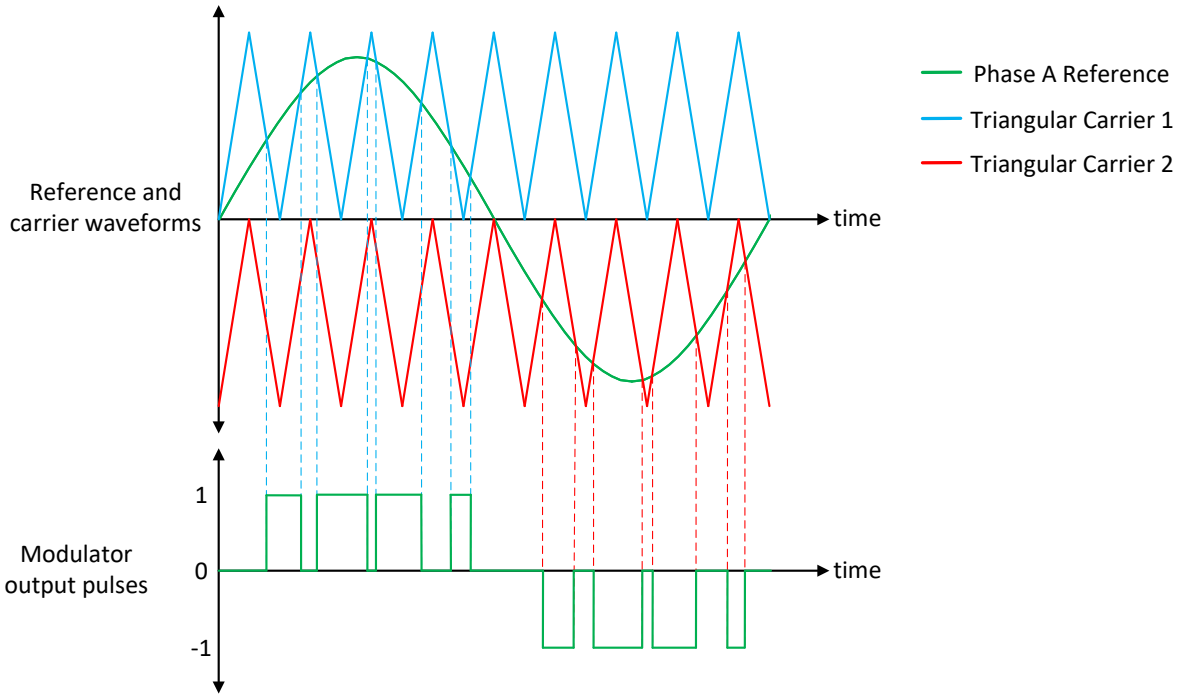


Figure 2.4: Three-level three-phase carrier-based PD SPWM phase A modulator output pulses

Table 2.2: Three-Level Three-Phase NPC Inverter Phase A Modulator Output and Switching States

Modulator Output (Phase A)	**S_{A1} State**	**S_{A2} State**	**S_{A3} State**	**S_{A4} State**
0	OFF	ON	ON	OFF
1	ON	ON	OFF	OFF
-1	OFF	OFF	ON	ON

Other possible 3-L SPWM variations not shown in Figure 2.3 include interleaved carrier (IC) SPWM and variable frequency carrier (VFC) SPWM. These are excluded because this work mostly uses the space vector concept for the modulation analysis. However, simulation results for PD and POD SPWM will be shown in subsequent chapters for comparative purposes.

2.2 Space Vector Modulation

The second type of PWM for DC-AC converters analyzed in this work is space vector modulation (SVM). In 3-ϕ power systems, SVM is based on the concept of representing a 3-ϕ voltage or current from the *abc* reference frame as a space vector in the stationary (α-β) reference frame. These two reference frames are shown in Figure 2.5. A balanced sinusoidal 3-ϕ voltage is represented in the *abc* reference frame with Equation 2.1. V_m is the three-phase voltage amplitude, ω is the frequency in radians/s and ϕ is the phase angle in radians. This voltage can be converted to α-β components using Equation 2.2, known as the Clarke transform [22]. Equivalently, it can be represented in the α-β reference frame as a space vector, $\bar{V}$, using Equation 2.4. It should be noted that Equations 2.2, 2.3 and 2.4 are based on the amplitude invariant Clarke transform. There is also a power invariant Clarke transform which multiplies the transformation matrix by $\sqrt{\frac{2}{3}}$ instead of $\frac{2}{3}$.

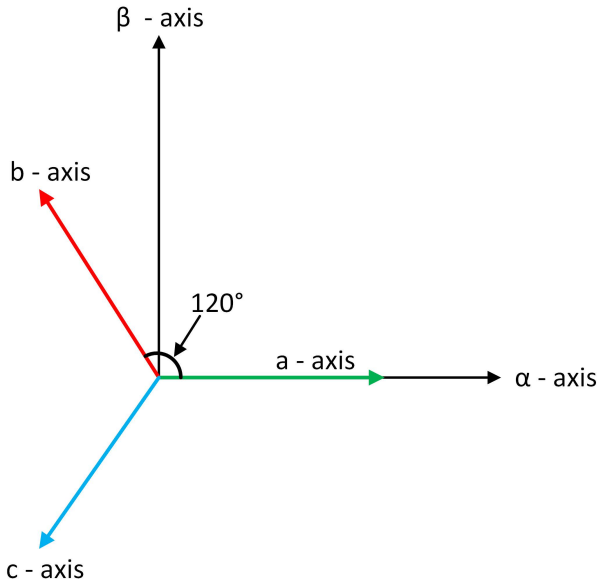


Figure 2.5: Three-phase *abc* and stationary α-β reference frames

$$\begin{aligned} v_a &= V_{\mathrm{m}} \cos(\omega t + \phi) \\ v_b &= V_{\mathrm{m}} \cos(\omega t + \phi - 2\pi/3) \\ v_c &= V_{\mathrm{m}} \cos(\omega t + \phi - 4\pi/3) \end{aligned} \tag{2.1}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.2}$$

$$\begin{aligned} v_\alpha &= \frac{2}{3} v_a - \frac{1}{3} v_b - \frac{1}{3} v_c \\ v_\beta &= \frac{\sqrt{3}}{3} v_b - \frac{\sqrt{3}}{3} v_c \\ v_0 &= \frac{1}{3} v_a + \frac{1}{3} v_b + \frac{1}{3} v_c \end{aligned} \tag{2.3}$$

$$\bar{V} = \frac{2}{3} \left(v_a + a v_b + a^2 v_c \right), \quad a = e^{j\frac{2\pi}{3}} \tag{2.4}$$

Returning to the 2-L 3-ϕ voltage source inverter of Figure 1.6, there are a total of eight valid switching states. Switching states involving both switches of a phase leg being ON are not valid because this will result in a short-circuit condition of the DC bus. Therefore, the top and bottom switches of a phase leg operate in a complementary manner where they are always in opposite states. In practice, a small delay, known as dead-time, is placed between one switch turning off and the other switch turning on. The dead-time ensures that the switches are never both in the ON-state which would result in a short-circuit current, known as shoot-through, flowing through

the switches for a small time period at the switching transition. The resulting eight valid switching states are listed in Table 2.3. The phase state 1 corresponds to the top switch, $S_{\phi 1}$, being in the ON-state and the bottom switch, $S_{\phi 2}$, being in the OFF-state. The phase state 0 corresponds to the top switch, $S_{\phi 1}$, being in the OFF-state and the bottom switch, $S_{\phi 2}$, being in the ON-state. The eight switching states of the 2-L 3-ϕ inverter can be represented as state vectors in the α-β reference frame, as shown in Figure 2.6. Six active state vectors ($\overline{V}_{1-7}$) and a zero vector ($\overline{V}_0$) with two state vector redundancies comprise the eight switching states.

Table 2.3: Two-Level Three-Phase Inverter Switching States

	Phase Leg		
Switching State	**a**	**b**	**c**
S_0	0	0	0
S_1	1	0	0
S_2	1	1	0
S_3	0	1	0
S_4	0	1	1
S_5	0	0	1
S_6	1	0	1
S_7	1	1	1

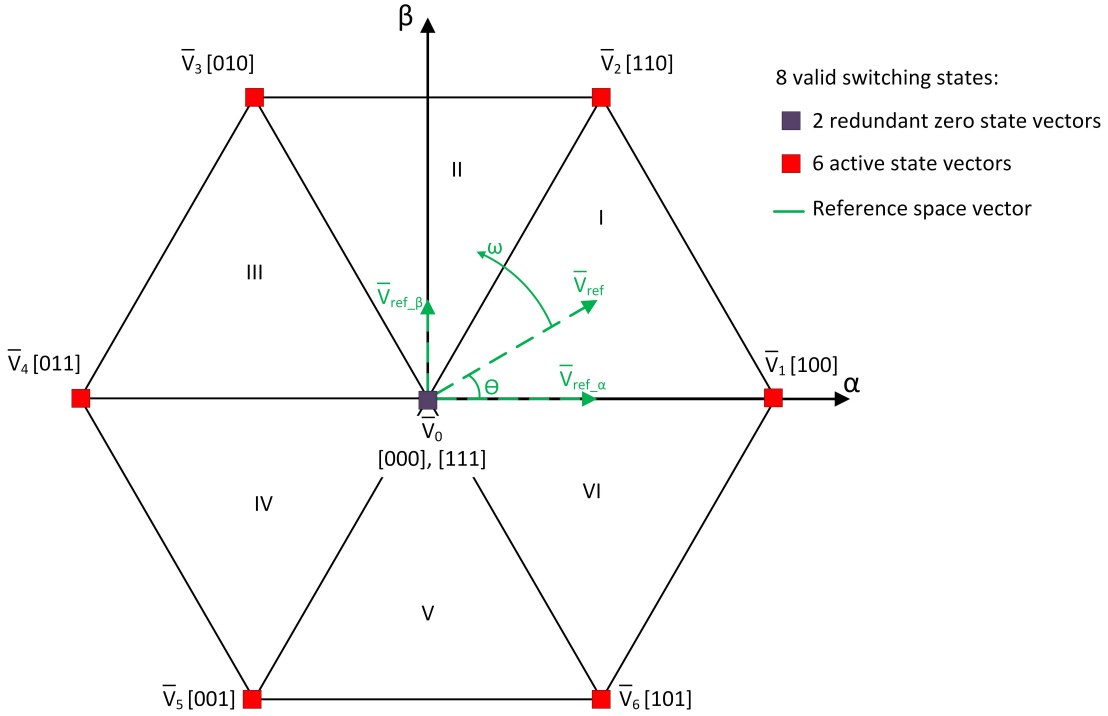


Figure 2.6: Two-level space vector hexagon

To generate a 3-ϕ sinusoidal output voltage with SVM, the output reference voltage is transformed to a space vector, $\overline{V}_{ref}$, in the α-β reference frame as shown in Figure 2.6 and then synthesized with the available converter states by dwelling on the corresponding states for specific amounts of time within each converter switching period, T_{sw}. The reference voltage space vector rotates in the α-β reference frame at the fundamental frequency, ω, and its instantaneous angle with respect to

the α-axis is denoted θ. If the converter switching frequency, f_{sw}, is sufficiently high compared to ω, the space vector is approximately stationary throughout T_{sw} and the sinusoidal output voltage can be synthesized with high quality. As shown in Figure 2.6, a hexagon is formed by connecting the active state vectors and the hexagon is divided into six triangular sectors (I-VI) that each occupy 60°of the reference voltage fundamental cycle, T_{fund}. T_{fund} is given by Equation 2.5

$$T_{fund} = \frac{2\pi}{\omega} \tag{2.5}$$

The most commonly implemented type of 2-L SVM is symmetric nearest-three-vector (NTV) SVM. In symmetric NTV SVM, the three converter state vectors (zero vector and two active vectors) forming the sector triangle in which $\overline{V}_{ref}$ lies are used to synthesize the output voltage. For example, in Sector I, $\overline{V}_{ref}$ can be represented over T_{sw} by Equation 2.6 where $\frac{T_1}{T_{sw}}$, $\frac{T_2}{T_{sw}}$ and $\frac{T_0}{T_{sw}}$ are the portions of T_{sw} for which the converter dwells on $\overline{V}_1$, $\overline{V}_2$ and $\overline{V}_0$, respectively. Thereby, T_1, T_2 and T_0 are denoted the dwell times of $\overline{V}_1$, $\overline{V}_2$ and $\overline{V}_0$, respectively.

$$\bar{V}_{ref} = \frac{T_1}{T_{sw}}\bar{V}_1 + \frac{T_2}{T_{sw}}\bar{V}_2 + \frac{T_0}{T_{sw}}\bar{V}_0 \tag{2.6}$$

$\overline{V}_0$ has zero voltage magnitude and has no effect on the angle of the synthesized vector. It is simply used to fill the portion of T_{sw} not occupied by the active vectors in order to realize the desired vector amplitude. Therefore, Equation 2.6 can be rewritten as shown in Equation 2.7. By converting Equation 2.7 from polar to rectangular form, the α and β components of $\overline{V}_{ref}$ can be written in terms of the dwell times as shown in Equations 2.8 and 2.9, respectively. Equation 2.9 can be simplified to Equation 2.10 which can then be used to solve for T_2, resulting in Equation 2.11.

$$\bar{V}_{ref} = \frac{T_1}{T_{sw}}\bar{V}_1 + \frac{T_2}{T_{sw}}\bar{V}_2 \tag{2.7}$$

$$V_{\text{ref\_}\alpha} = \frac{T_1}{T_{sw}} \cdot \frac{2}{3}V_{\text{dc}}\ \cos(0) + \frac{T_2}{T_{sw}} \cdot \frac{2}{3}V_{\text{dc}}\ \cos\left(\frac{\pi}{3}\right) \tag{2.8}$$

$$V_{\text{ref\_}\beta} = \frac{T_1}{T_{sw}} \cdot \frac{2}{3}V_{\text{dc}}\ \sin(0) + \frac{T_2}{T_{sw}} \cdot \frac{2}{3}V_{\text{dc}}\ \sin\left(\frac{\pi}{3}\right) \tag{2.9}$$

$$V_{\text{ref\_}\beta} = \frac{T_2}{T_{sw}} \cdot \frac{2}{3}V_{\text{dc}}\ \sin\left(\frac{\pi}{3}\right) \tag{2.10}$$

$$T_2 = \sqrt{3}\frac{V_{\text{ref\_}\beta}}{V_{dc}}T_{sw} \tag{2.11}$$

To solve for T_1, Equation 2.8 is simplified, resulting in Equation 2.12. Substituting Equation 2.11 into Equation 2.12 and simplifying results in Equation 2.13 for T_1. From Figure 2.6, $\bar{V}_{\text{ref\_}\alpha}$ and $\bar{V}_{\text{ref\_}\beta}$ are given by Equations 2.14 and 2.15, respectively.

$$V_{\text{ref\_}\alpha} = \frac{T_1}{T_{sw}} \cdot \frac{2}{3} V_{\text{dc}} + \frac{T_2}{T_{sw}} \cdot \frac{1}{3} V_{\text{dc}} \tag{2.12}$$

$$T_1 = \frac{T_{sw}}{2V_{dc}} \left[3V_{\text{ref\_}\alpha} + \sqrt{3} V_{\text{ref\_}\beta} \right] \tag{2.13}$$

$$V_{\text{ref\_}\alpha} = |\bar{V}_{\text{ref}}| \cos(\theta) \tag{2.14}$$

$$V_{\text{ref\_}\beta} = |\bar{V}_{\text{ref}}| \sin(\theta) \tag{2.15}$$

Finally, substituting Equations 2.14 and 2.15 into Equations 2.11 and 2.13, and simplifying results in Equations 2.16 and 2.17 for T_1 and T_2, respectively. T_0 is then calculated with Equation 2.18.

$$T_1 = \sqrt{3} \frac{|\bar{V}_{\text{ref}}|}{V_{dc}} T_{sw} \sin(\frac{\pi}{3} - \theta) \tag{2.16}$$

$$T_2 = \sqrt{3} \frac{|\bar{V}_{\text{ref}}|}{V_{dc}} T_{sw} \sin(\theta) \tag{2.17}$$

$$T_0 = T_{sw} - T_1 - T_2 \tag{2.18}$$

The dwell time equations can then be extended to the other five sectors of the space vector hexagon and $\overline{V}_{ref}$ can be synthesized over all of T_{fund} as long as it lies within the bounds of the hexagon. Generally, T_0 is divided equally between the two $\overline{V}_0$ redundancies. The T_{sw} vector sequence is then selected to minimize the converter switching transitions and to achieve half-wave symmetry in the output phase-to-neutral voltages over T_{fund} to eliminate even harmonic components in the output voltage. A typical vector sequence for 2-L symmetric NTV SVM is shown in Figure 2.7 for Sector I. It can be observed that each vector transition involves only one of the three phase legs changing states, thereby, minimizing the required switching transitions.

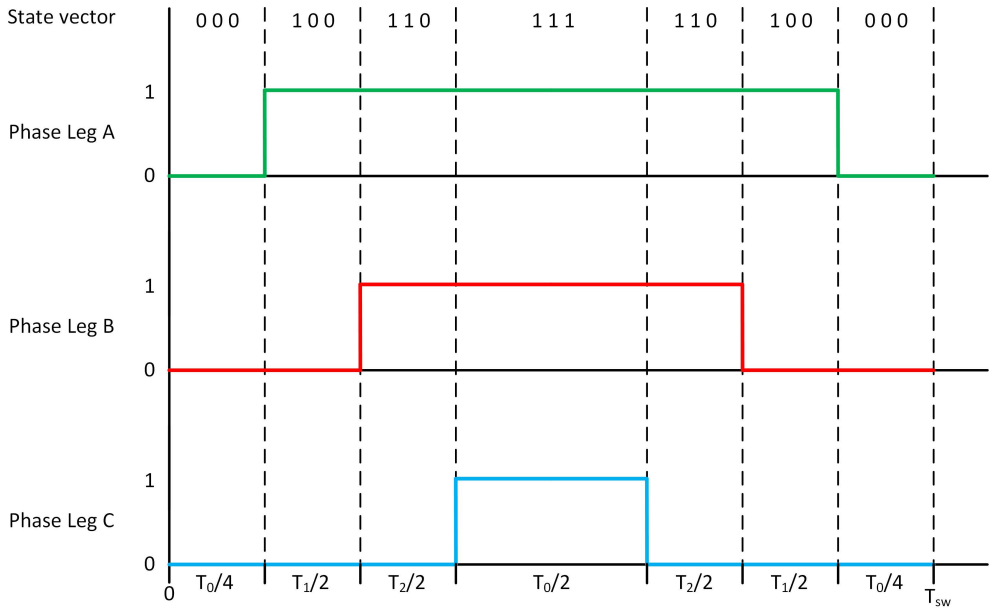


Figure 2.7: Two-level symmetric NTV SVM typical vector sequence in Sector I

The 2-L SVM concept can be extended to multi-level converters such as the 3-L NPC inverter of Figure 1.7(a). Generally, for a 3-ϕ inverter, the number of valid switching states, S_{sw}, is given as a function of the number of converter levels, N, in Equation 2.19. For the 3-L 3-ϕ NPC inverter, 0, P and N are used to denote the valid phase leg states. Table 2.4 shows the states of the NPC phase leg switches corresponding to each phase leg state. From Equation 2.19, the 3-L 3-ϕ NPC inverter has twenty-seven valid switching states which are shown in Table 2.5.

$$S_{sw} = N^3 \tag{2.19}$$

Table 2.4: Three-Level Three-Phase NPC Inverter Phase A State Switching Configurations

Phase A State	$\mathbf{S_{A1}}$	$\mathbf{S_{A2}}$	$\mathbf{S_{A3}}$	$\mathbf{S_{A4}}$
0	OFF	ON	ON	OFF
P	ON	ON	OFF	OFF
N	OFF	OFF	ON	ON

Table 2.5: Three-Level Three-Phase NPC Inverter Switching States

	Phase Leg		
Switching State	**a**	**b**	**c**
ZV_0	0	0	0
ZV_p	P	P	P
ZV_n	N	N	N
$S1_p$	P	0	0
$S1_n$	0	N	N
$S2_p$	P	P	0
$S2_n$	0	0	N
$S3_p$	0	P	0
$S3_n$	N	0	N
$S4_p$	0	P	P
$S4_n$	N	0	0
$S5_p$	0	0	P
$S5_n$	N	N	0
$S6_p$	P	0	P
$S6_n$	0	N	0
$M1$	P	0	N
$M2$	0	P	N
$M3$	N	P	0
$M4$	N	0	P
$M5$	0	N	P
$M6$	P	N	0
$L1$	P	N	N
$L2$	P	P	N
$L3$	N	P	N
$L4$	N	P	P
$L5$	N	N	P
$L6$	P	N	P

Similar to the 2-L converter states, the 3-L converter states are represented as state vectors in the α-β reference frame and form the 3-L SVM hexagon as shown in Figure 2.8. The vector names are based on their representation as state vectors where it is apparent that there is a zero vector with three redundancies, six small vectors, each with two redundancies, six medium vectors and six large vectors, as can be observed in Figure 2.8. Additionally, the six 60°sectors, I-VI, are still present as in 2-L SVM but are each divided into four regions corresponding to the nearest three state vectors. It can also be observed that the large vectors form an outer hexagon and the small vectors form an inner hexagon which will be useful for later analysis.

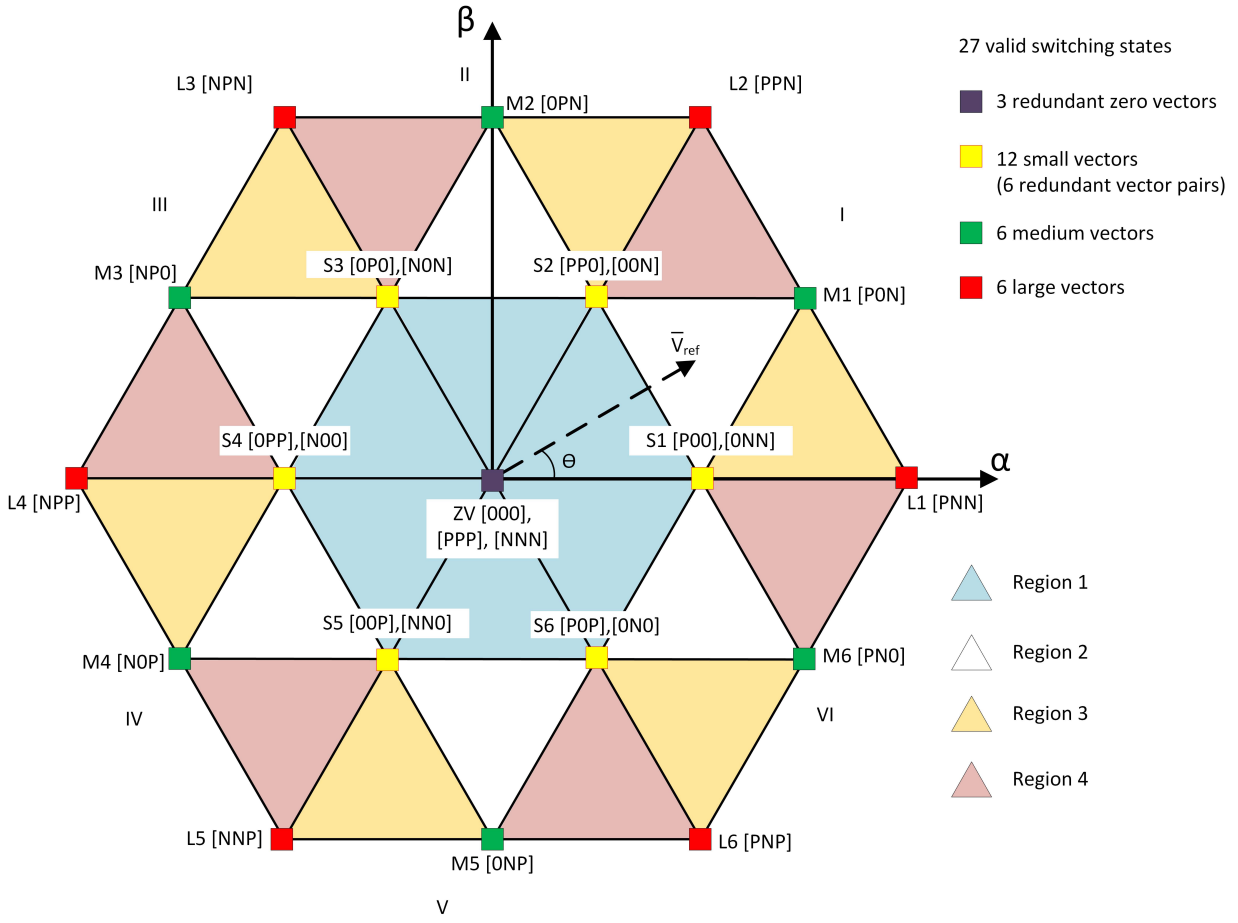


Figure 2.8: Three-level space vector hexagon

Using similar trigonometric methods as for 2-L SVM, the dwell times of three nearest vectors required to synthesize $\overline{V}_{ref}$ can be determined. The resulting dwell time equations are shown in Table 2.6 for Sector I Regions 1-4 where k is given by Equation 2.20. Similar to 2-L SVM, equivalent equations can be determined for the remaining five sectors and the rotating space vector can be synthesized throughout T_{fund} as long as it lies inside the large hexagon. For the 3-L symmetric NTV SVM, the vector sequences are determined similarly to 2-L symmetric NTV SVM. As an example, the typical vector sequence for Sector I, Region 4 is shown in Figure 2.9.

$$k = \frac{|\bar{V}_{\text{ref}}|}{V_{dc}} \tag{2.20}$$

Table 2.6: Three-Level NTV SVM Sector I Dwell Time Equations

Region	**Dwell Times**
Region 1	$T_{S1} = 2\sqrt{3}kT_{sw}\sin(\frac{\pi}{3} - \theta)$ $T_{S2} = 2\sqrt{3}kT_{sw}\sin(\theta)$ $T_{ZV} = T_{sw} - T_{S1} - T_{S2}$
Region 2	$T_{S1} = T_{sw} * \left[1 - 2\sqrt{3}k\sin(\theta)\right]$ $T_{S2} = T_{sw} * \left[1 - 2\sqrt{3}k\sin(\frac{\pi}{3} - \theta)\right]$ $T_{M1} = T_{sw} * \left[2\sqrt{3}k\sin(\frac{\pi}{3} + \theta) - 1\right]$
Region 3	$T_{L1} = T_{sw} * \left[2\sqrt{3}k\sin(\frac{\pi}{3} - \theta) - 1\right]$ $T_{M1} = 2\sqrt{3}kT_{sw}\sin(\theta)$ $T_{S1} = T_{sw} * \left[2 - 2\sqrt{3}k\sin(\frac{\pi}{3} + \theta)\right]$
Region 4	$T_{L2} = T_{sw} * \left[2\sqrt{3}k\sin(\theta) - 1\right]$ $T_{M1} = 2\sqrt{3}kT_{sw}\sin(\frac{\pi}{3} - \theta)$ $T_{S2} = T_{sw} * \left[2 - 2\sqrt{3}k\sin(\frac{\pi}{3} + \theta)\right]$

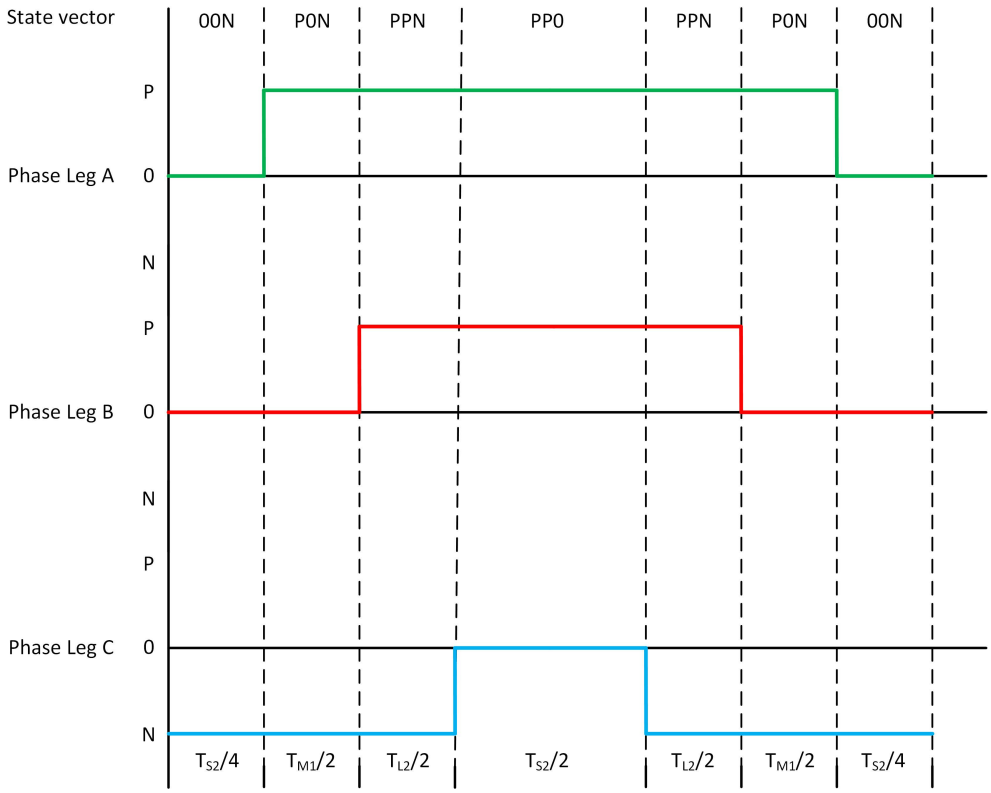


Figure 2.9: Three-level symmetric NTV SVM typical vector sequence in Sector I Region 4

It should be noted that for Regions 1 and 2, the dwell times of both small vectors can be split between the two redundancies for each vector or only one small vector's dwell time is split between its two redundancies and the other small vector allocates all of its dwell time to only one of its redundancies. This results in a 9-segment and 7-segment vector sequence, respectively.

For reference space vectors that lie beyond the boundaries of the space vector hexagon, it can be possible to synthesize them with overmodulation techniques. However, in this work, only linear modulation where the reference vector lies inside the space vector hexagon is considered. Thus, the amplitude modulation index, m_a, is given by Equation 2.21 which is valid for the amplitude invariant Clarke transform. For analysis in subsequent chapters, it is useful to show this relationship graphically on the space vector hexagon. Therefore, the 3-L SVM in Figure 2.8 is redrawn in Figure 2.10. Here, it can be seen that a reference vector with an amplitude equal to the circle inscribing the inner hexagon formed by the six small state vectors corresponds to $m_a = 1/\sqrt{3}$ or approximately 0.577. Likewise, a reference vector with an amplitude equal to the circle inscribing the hexagon formed by the six medium state vectors corresponds to $m_a = 1$. This corresponds to the m_a upper limit for carrier-based SPWM without third-harmonic injection in the linear modulation region. Finally, a reference vector with an amplitude equal to the circle inscribing the large hexagon formed by the six large state vectors corresponds to $m_a = 2/\sqrt{3}$ or approximately 1.15. This corresponds to the m_a upper limit for carrier-based SPWM with third-harmonic injection and symmetric NTV SVM in the linear modulation region. It is also useful to note that, for a balanced 3-ϕ voltage, the amplitude of the voltage space vector in the α-β reference frame is equal to the peak of the phase-to-neutral voltage in the *abc* reference frame when the amplitude invariant Clarke transform is used.

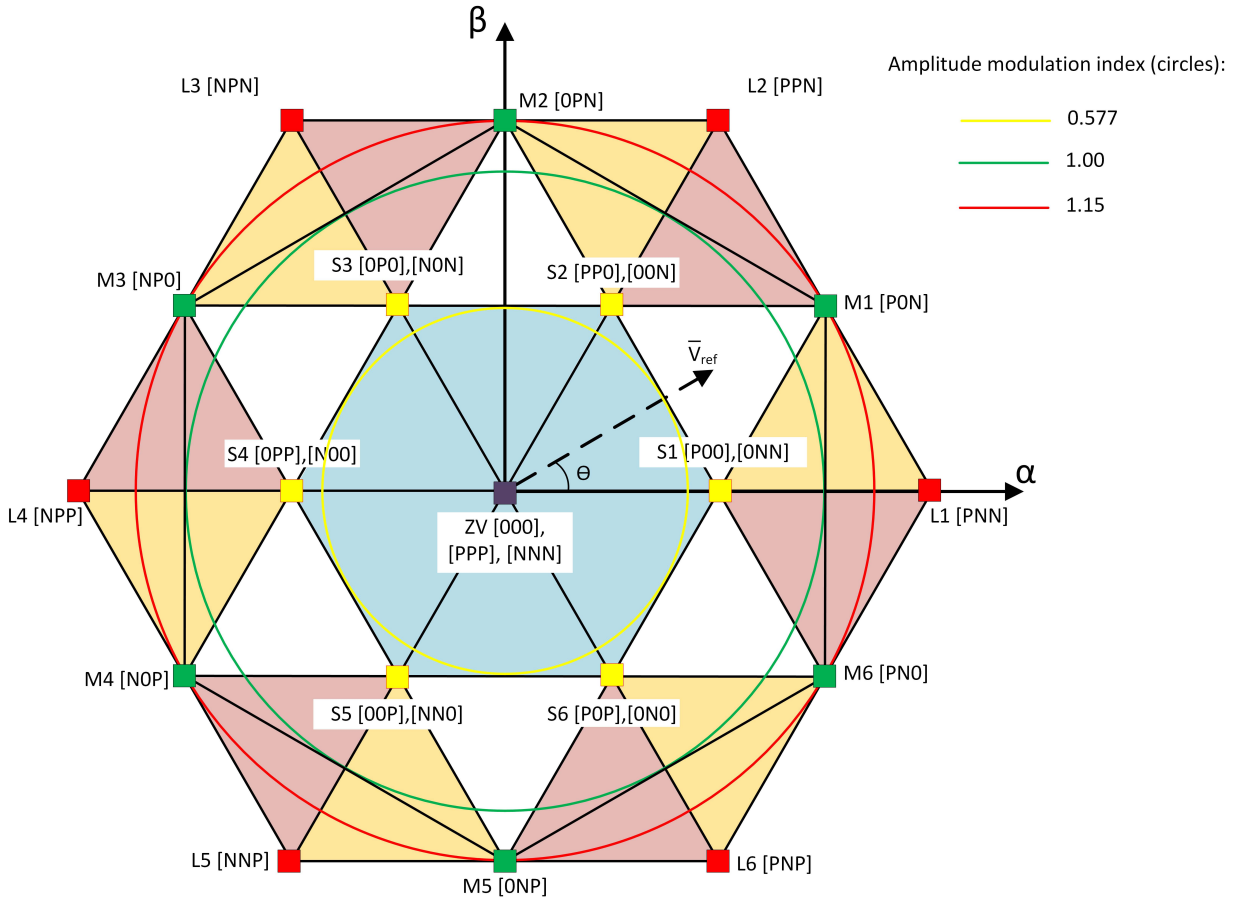
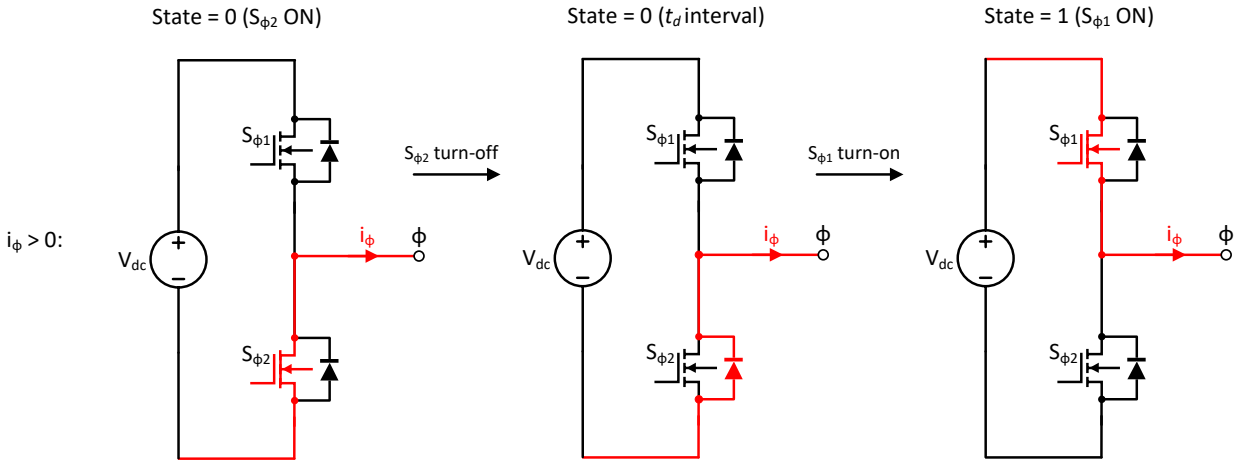


Figure 2.10: Three-level space vector hexagon with amplitude modulation index circles

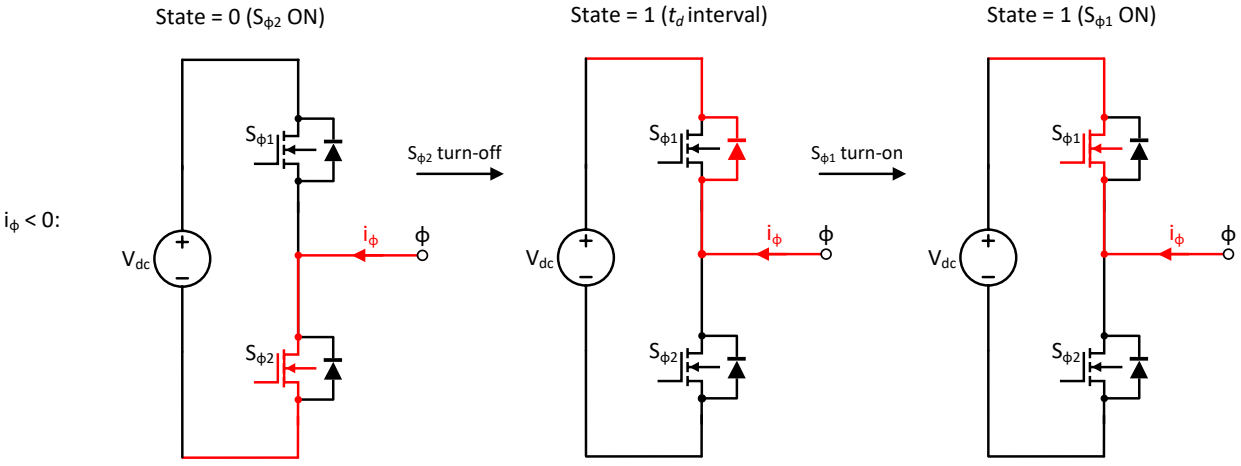
$$m_a = \frac{2|\bar{V}_{\text{ref}}|}{V_{dc}} \tag{2.21}$$

2.3 Dead-Time and Minimum Pulse-Width in PWM

As mentioned in Section 2.2, the switches of a phase leg in a 2-L DC-AC VSI operate in a complimentary manner with a small delay, called dead-time (t_d), in between one switch turning off and its complementary switch turning on. t_d is necessary to prevent shoot-through during switching transitions. t_d is also required in the 3-L NPC VSI in which $S_{\phi 1}$ is complementary to $S_{\phi 3}$ and $S_{\phi 2}$ is complementary to $S_{\phi 4}$.



(a) $i_\phi > 0$



(b) $i_\phi < 0$

Figure 2.11: Duty cycle distortion due to dead-time in half-bridge

The presence of t_d results in non-ideal effects on the converter AC output voltages and currents due to its distortion of the duty cycles of the converter phase leg states. This can be understood from Figure 2.11 in which a 2-L half-bridge is shown transitioning from State 0 to State 1. When the output phase current, i_ϕ, has positive polarity (Figure 2.11(a)), the half-bridge stays on State 0 during the t_d interval, due to the current commutation to the $S_{\phi 2}$ anti-parallel diode. However, when i_ϕ has negative polarity (Figure 2.11(b)), the current commutates to the $S_{\phi 1}$ anti-parallel

diode so the half-bridge goes to State 1 during the t_d interval. The inverse happens when the half-bridge transitions from State 1 to State 0. The net effect over a switching cycle is that the State 0 dwell time gains t_d and the State 1 dwell time loses t_d for $i_\phi > 0$ while the State 1 dwell time gains t_d and the State 0 dwell time loses t_d for $i_\phi < 0$. This results in a decrease in the half-bridge output voltage when $i_\phi > 0$ and an increase in the half-bridge output voltage when $i_\phi < 0$.

For a DC-AC converter with a sinusoidal output and a closed-loop controller with finite bandwidth, the controller will compensate for the error in the output caused by t_d. However, at the output phase current zero crossings, the polarity of the error flips and the controller will have a delayed response to the change in error polarity due to its finite bandwidth. This will result in distortions in the output phase voltages and currents at the current zero crossings, causing an increase in total harmonic distortion (THD) and grid frequency harmonics in the common-mode voltage.

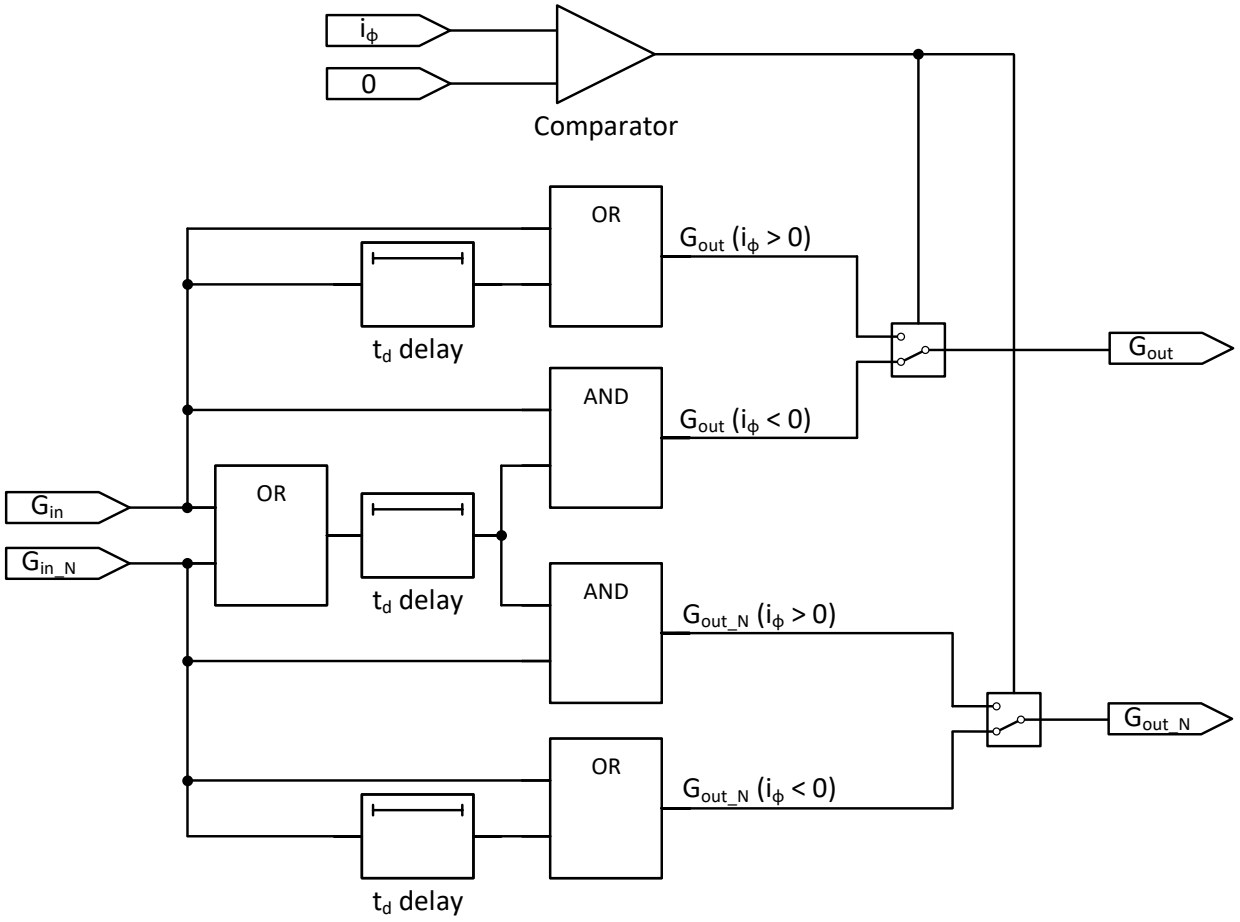


Figure 2.12: Dead-time compensator schematic

Different methods for compensating the effect of t_d on inverter output have been developed such as in [23], [24] and [25]. To mitigate the effect of t_d on the performance of the modulation methods analyzed in Chapters 3 and 4, a t_d compensator is implemented in the simulations. The t_d compensator schematic is shown in Figure 2.12 and corrects the switching device gate pulses generated by the modulator based on the respective phase current polarity. G_{in} and G_{in_N} are the uncompensated gate signal and its complementary signal. G_{out} and G_{out_N} are the gate signal and its complementary signal compensated for t_d. The compensation results in a phase delay of the converter output of t_d. However, the phase delay is very small relative to the fundamental period at 50/60 Hz with the typical dead-time range used in the considered SiC MOSFETs. This work did not implement the t_d compensator in the experimental hardware and leaves doing so to future work.

Separate from the duty cycle distortion based on phase current polarity discussed above, another non-ideality in PWM is minimum pulse-width. For carrier-based PWM methods, as the reference sine wave approaches the carrier amplitude, the pulse-width will approach zero or the carrier period, as can be observed in Figure 2.4. This will result in a switch of the respective phase leg having a near-zero duty cycle. If the duty cycle is small enough, the desired on-time of the switch will be less than t_d, in which case, the pulse will be eliminated in order to ensure t_d is still maintained. The t_d compensator of 2.12 will not prevent pulse elimination due to minimum pulse-width. However, t_d for modern IGBTs and power MOSFETs is often small enough that the effect of minimum pulse-width is negligible for converters with power levels below the MW range [21].

2.4 Chapter Summary

Chapter 2 provided an overview of carrier-based SPWM and SVM methods for 3-ϕ DC-AC converters. The implementations of both types of modulation are explained and it is shown how they are extended from a 2-L converter to the 3-L converter considered in this work. This overview serves as a framework for the analysis and discussion of the different modulation methods in Chapters 3, 4 and 5.

Additionally, the effect of dead-time and minimum pulse-width on DC-AC converter output are explained. Then, the method used to compensate for dead-time in the simulations of Chapters 3 and 4 is presented. This compensation ensures that the dead-time does not cause large distortions in the converter output voltages and currents.

Chapter 3: Ground Leakage Current in Three-Phase Inverter Systems

3.1 Three-Phase Inverter Common-Mode Voltage

As shown in Chapter 2, DC-AC converters transition through their valid switching states as they are modulated to produce the desired AC output voltages and currents. For a balanced sinusoidal 3-ϕ voltage, the sum of the instantaneous phase voltages is equal to zero throughout T_{fund}, as shown by Equation 3.1. However, for both the 2-L and 3-L converters of Figures 1.6 and 1.7, respectively, the valid converter switching states produce different values for the sum of the instantaneous voltage between each phase and the DC bus neutral-point, *NP*. This sum divided by three gives the converter output voltage component that is present in all three phase-*NP* voltages with equal amplitude, frequency and phase angle. This voltage is defined as the converter common-mode voltage, V_{cm}, and is given by Equation 3.2. The 3-L NPC topology (one phase leg) is shown again in Figure 3.1 for convenience.

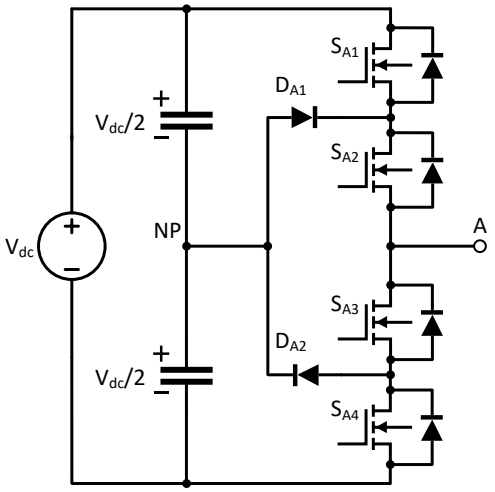


Figure 3.1: Three-level NPC topology (one phase leg)

$$v_a + v_b + v_c = 0 \tag{3.1}$$

$$V_{cm} = \frac{V_{a-NP} + V_{b-NP} + V_{c-NP}}{3} \tag{3.2}$$

For each converter switching state, the instantaneous V_{cm} is a constant DC value assuming the DC bus voltage is constant. However, as the converter transitions between switching states during operation, V_{cm} can change, resulting in AC components in V_{cm}. The values of V_{cm} for the 3-L NPC converter switching states are given in Table 3.1 and are categorized based on the different types of state vectors described for 3-L SVM in Chapter 2. The 3-L SVM hexagon is also redrawn in Figure A1 with the V_{cm} values of each state vector shown. Equivalent V_{cm} values can be derived for the 2-L SVM state vectors. As will be discussed in Section 3.2, common-mode current, I_{cm}, flowing through the converter will result from the V_{cm} produced by the converter switching if there is a path for the current to flow.

Table 3.1: Three-Level NPC State Vector Common-Mode Voltages

State Vector Category	**Switching State**	V_{cm}
Zero vectors	000	0
	PPP	$\frac{V_{dc}}{2}$
	NNN	$\frac{-V_{dc}}{2}$
Small vectors	P00, 00P, 0P0	$\frac{V_{dc}}{6}$
	PP0, P0P, 0PP	$\frac{V_{dc}}{3}$
	0NN, NN0, N0N	$\frac{-V_{dc}}{3}$
	00N, 0N0, N00	$\frac{-V_{dc}}{6}$
Medium vectors	P0N, 0PN, NP0 N0P, 0NP, PN0	0
Large vectors	PPN, NPP, PNP	$\frac{V_{dc}}{6}$
	PNN, NPN, NNP	$\frac{-V_{dc}}{6}$

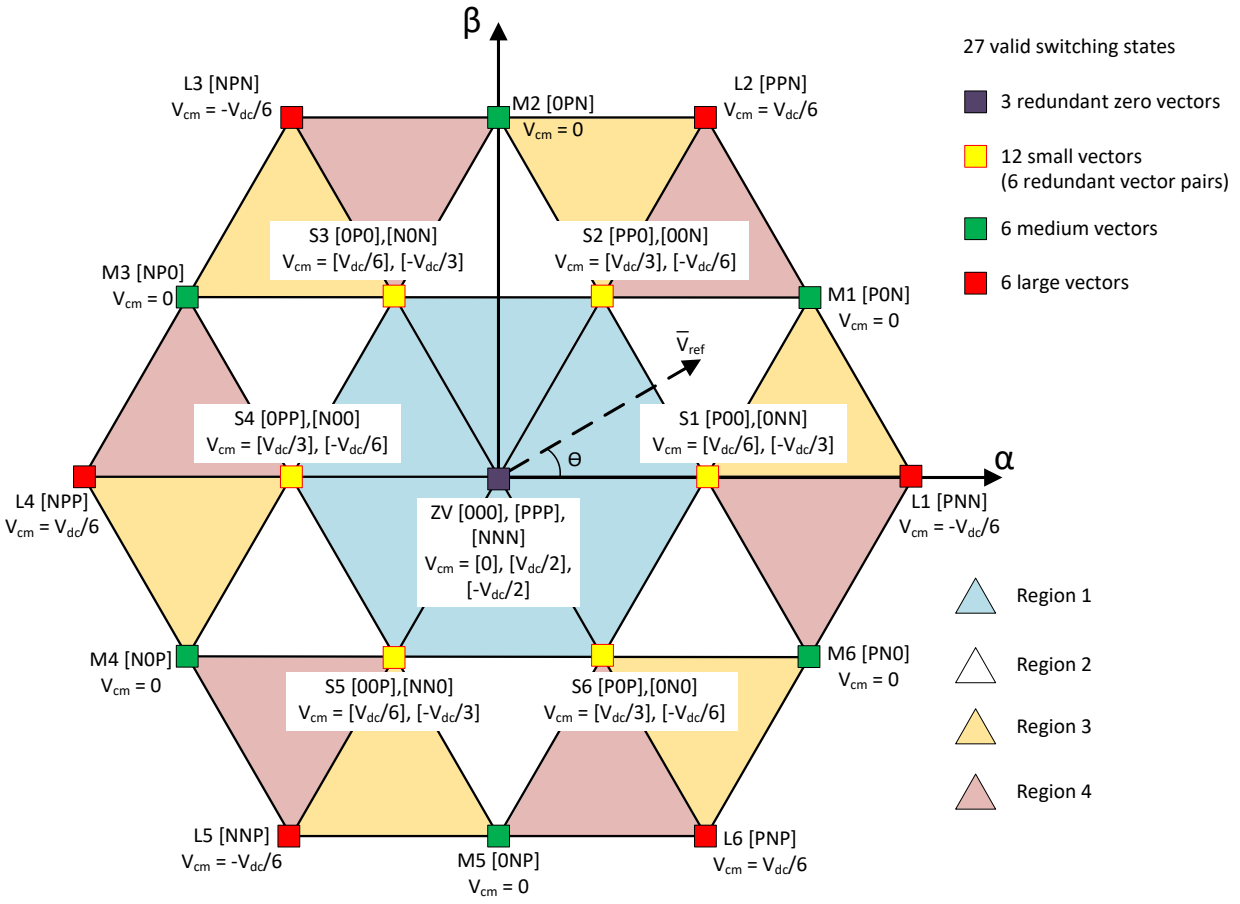


Figure 3.2: Three-level space vector hexagon with state vector common-mode voltages

3.2 Grid-Connected Inverter Common-Mode Current

As discussed in Section 3.1, a 3-ϕ grid-connected inverter produces common-mode voltage, V_{cm}, as it transitions through its switching states during operation. The resulting common-mode current, I_{cm}, depends on the common-mode impedance, Z_{cm}, of the circuit formed by the inverter, the AC grid, ground connections and the inverter's DC bus. As was introduced in Chapter 1, the main challenge of a transformerless connection of an inverter to the AC grid is the high ground leakage current, I_{gl}, which results from the lack of the transformer's high Z_{cm} and the problem it causes for protection devices in the AC grid. This section will derive Z_{cm} and demonstrate how it is fundamentally different for grid-connected inverters in PV array systems versus in the bipolar DC microgrid system of Figure 1.1. The problem for protection devices due to I_{gl} will also be presented in detail.

3.2.1 Grid-Tied Inverter Common-Mode Circuit Model

3-ϕ grid-connected voltage source inverters are typically connected to the AC grid through an LCL filter. This is a third-order filter comprised of two inductance and one capacitance as shown in Figure 3.3. In this work, the inverter switch nodes are connected to the L_1-side of the filter and the AC grid is connected to the L_2-side of the filter, as shown in Figure 3.4. The LCL filter also typically includes a common-mode choke with common-mode inductance, L_{CMC}, to attenuate the inverter I_{cm}. The common-mode choke is a multi-winding coupled inductor that ideally presents zero impedance to differential voltage components and presents an impedance given in Equation 3.3 to common-mode voltage components. In Equation 3.3, j is the complex unit and ω is the frequency of the common-mode voltage component in radians/s. Damping is typically added to the filter in

the form of either a damping resistance, R_{damp}, or active damping techniques implemented in the inverter control, to dampen the LCL filter resonance. In practice, the grid inductance, L_{grid}, is often large enough at the inverter connection point that it can be used to form the inductance of L_2 and no discrete inductor is needed for this component of the filter. For the analysis of the common-mode circuit, L_2 is considered to include the grid inductance. From Figure 3.4, it can be seen that the LCL filter will form one of the components of Z_{cm} in the grid-connected inverter system.

$$Z_{CMC} = j\omega L_{CMC} \tag{3.3}$$

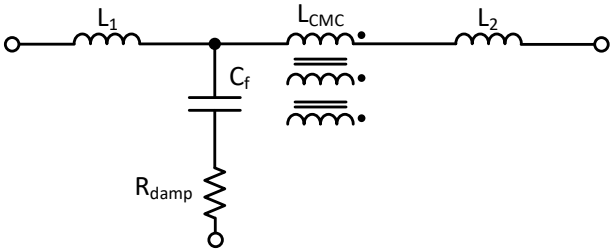


Figure 3.3: LCL filter for three-phase grid-connected DC-AC converter (one phase shown)

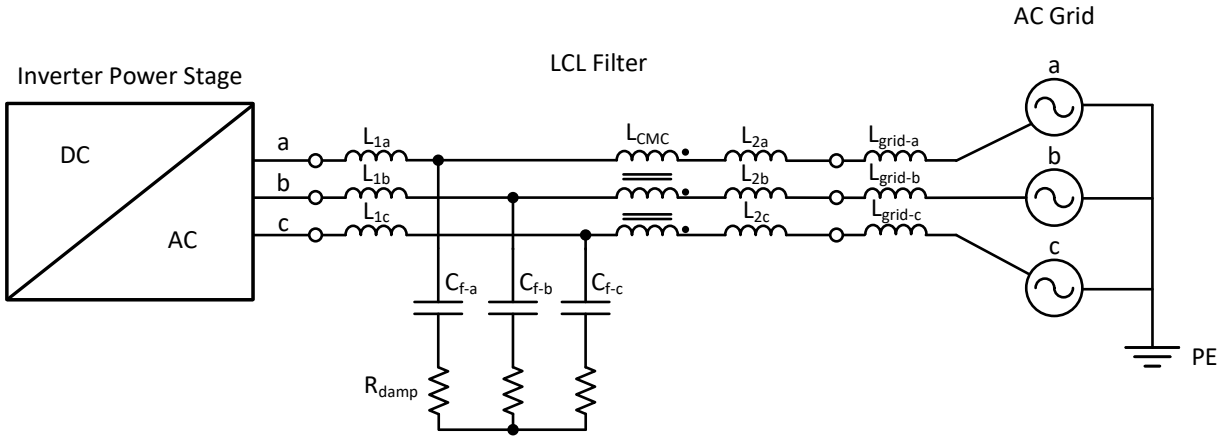


Figure 3.4: Three-phase DC-AC converter connection to AC grid with LCL filter

The other main component of Z_{cm} is the capacitance between PE and the DC bus. This was introduced in Chapter 1 for the case of a grid-connected inverter in a PV array and shown in Figure 1.3. In PV arrays, the panels are typically held inside of a metal frame which is then connected to PE. This results in a geometry of conductors and dielectrics that form a parasitic capacitance, C_{par}, between the DC terminals of the panels and PE. The value of C_{par} is, therefore, dependent on the size of the PV array and typically ranges from 100 to 200 nF per kW of installed PV power generation capacity [9] [11] [26]. Conditions such as water or salt fog on the panels due to weather also influence C_{par}.

In bipolar DC grids, a method of grounding the neutral conductor, DC_N, to PE is necessary for safe operation of the grid. Bipolar DC grids for LV distribution are still a relatively new concept and the standards for such systems are still being developed. However, multiple concepts for grounding in these systems exist [8] [27]. In this work, capacitive grounding is considered for the bipolar DC microgrid in which a capacitor is placed between DC_N and PE at each DC grounding point. This

concept is shown in Figure 1.1 of Chapter 1. Unlike in PV array systems where the capacitance between the DC terminals of the panels and PE is a parasitic one inherently formed by the geometry and material composition of the physical PV array, in the considered bipolar DC microgrid system, a capacitance, C_{DC-GND}, is intentionally placed between the neutral DC terminal and PE. Figure 3.5 shows the grid-connected inverter system considering C_{DC-GND} and the neutral-point of the LCL filter capacitors connected to DC_N.

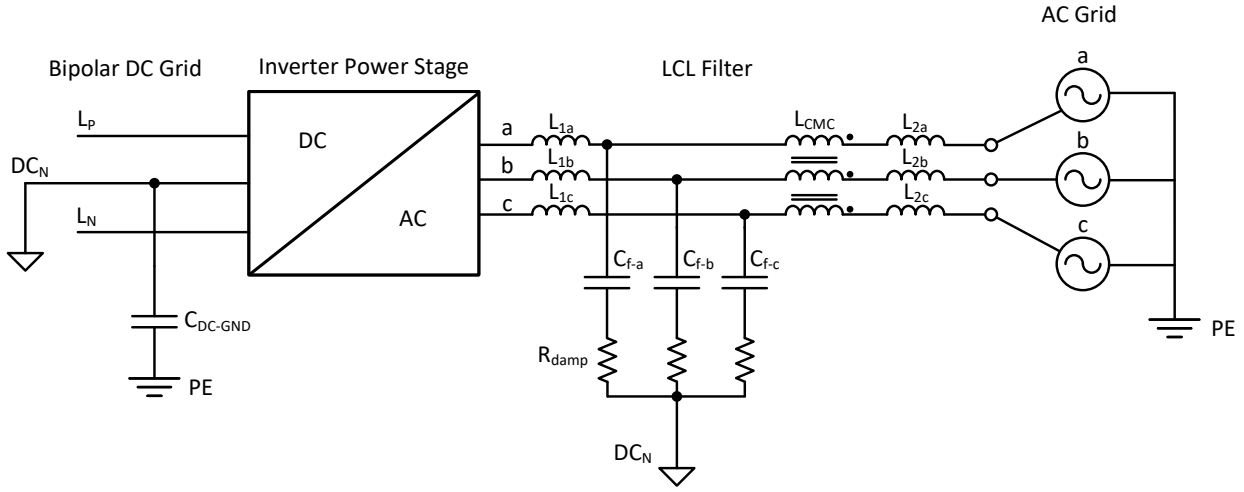


Figure 3.5: Grid-connected inverter system with LCL filter and capacitive DC grounding

From Figure 3.5, the common-mode circuit for the grid-connected inverter system can be derived as shown in Figure 3.6. It can be observed that the total common-mode current, I_{cm}, is divided between C_f and the AC grid as per Equation 3.4. Only the portion of I_{cm} flowing into the AC grid returns to DC_n through the earth and therefore, this component is defined as the ground leakage current, I_{gl}.

It should be noted that, in reality, a parasitic capacitance also exists between each switch node of the converter and PE and there is a non-zero impedance between the grounding points of the DC and AC grids. However, these components are considered negligible for the analysis conducted in this work. The switch node capacitances typically only need to be considered when analyzing the high-frequency components of the switch node voltages that result from the turn-on and turn-off events of the switching devices. Such analysis typically relates to electromagnetic compatability (EMC) of the converter and is beyond the scope of this work. Additionally, the Figure 3.6 common-mode circuit excludes the parasitics of the filter components such as the inductor inter-winding capacitances. However, these parasitics are typically small enough that their impact is negligible for this analysis. The bipolar DC grid cable impedances are also considered to be negligible here.

$$I_{cm} = I_{cm-Cf} + I_{gl} \tag{3.4}$$

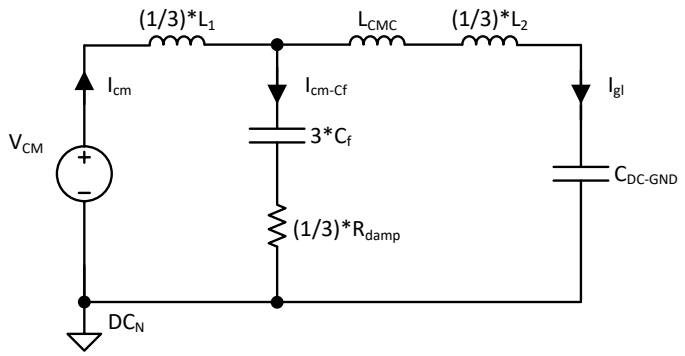


Figure 3.6: Grid-connected inverter system common-mode circuit

Table 3.2 lists the LCL filter and DC bus component values used in the simulations of this work. Figure 3.7 shows the resulting impedance plot of the common-mode circuit in the frequency range of interest. From the Z_{cm} plot, it can be seen that the common-mode circuit has three resonant frequencies. The first resonance, at approximately 650 Hz, is the series resonance of L_1, L_2 and L_{CMC} with C_{DC-GND}. The second resonance, at approximately 1.4 kHz, is the parallel resonance of L_2 and L_{CMC} with C_{DC-GND}. The third resonance, at approximately 4.3 kHz, is the series-parallel resonance of the LCL filter component common-mode values. It is evident from the impedance plot that V_{cm} frequency components close to the first and third resonances will result in relatively high I_{cm} frequency components compared to V_{cm} components with equal amplitude but at other frequencies. Equivalently, the impedance plot of the ground loop path through which I_{gl} flows is shown in Figure 3.8. This portion of the common-mode circuit only contains the 650 Hz resonance due to C_{DC-GND}. However, this demonstrates that minimizing the V_{cm} frequency components close to this resonance is generally necessary in order to minimize I_{gl}. In PV systems, the frequency of this resonance will be determined by C_{par} rather than C_{DC-GND}.

Table 3.2: LCL Filter and DC Bus Component Values

Component	**Value**	**Unit**
L_1	300	μH
L_2	100	μH
C_f	5	μF
R_{damp}	100	mΩ
L_{CMC}	1	mH
C_{DC-BUS}	390	μF
C_{DC-GND}	50	μF

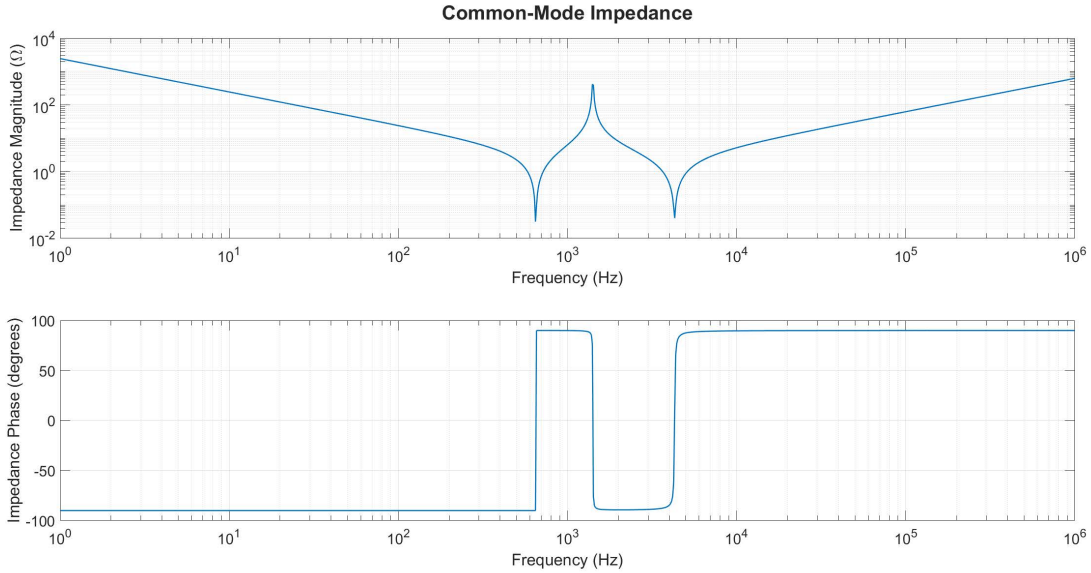


Figure 3.7: Grid-connected inverter system common-mode impedance magnitude and phase

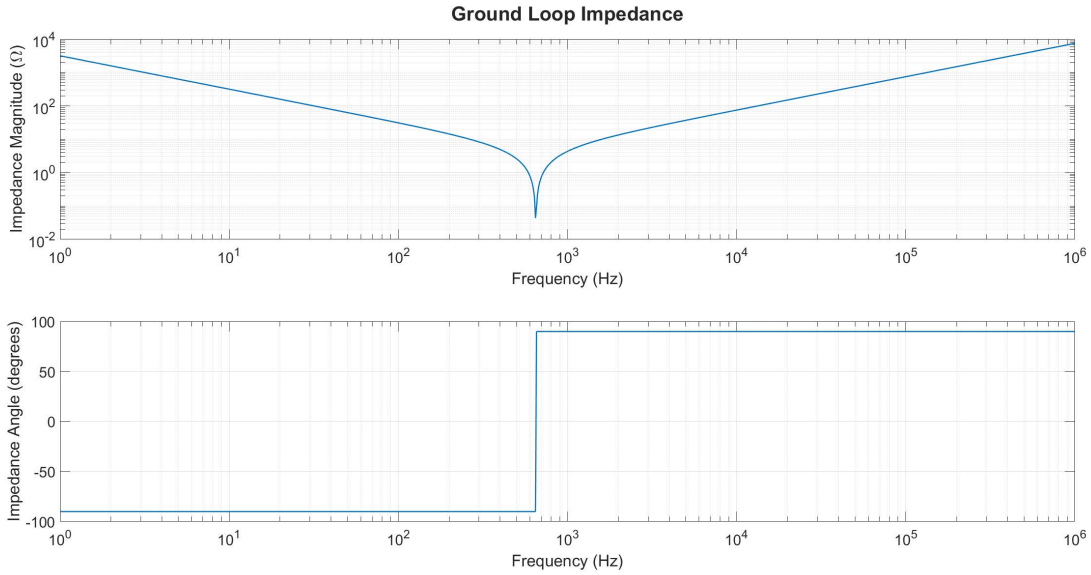


Figure 3.8: Grid-connected inverter system ground loop impedance magnitude and phase

3.2.2 Effect of Ground Leakage Current on AC Protection Devices

As introduced in Chapter 1, the main challenge of connecting a DC-AC inverter to the LV AC grid without a transformer is the resulting ground leakage current, I_{gl}, which interferes with the operation of protection equipment, namely residual current detectors (RCDs). Recalling Equation 3.1, it is seen that the instantaneous sum of balanced sinusoidal 3-ϕ voltages, and by extension, currents, is zero. This results in Equation 3.5 for balanced sinusoidal 3-ϕ currents. In 3-ϕ systems, RCDs are current sensing devices that are designed to measure the sum of the three-phase current [28]. If this sum is non-zero and not returning on a neutral-conductor, if present, it indicates the possibility of a ground fault.

$$i_a + i_b + i_c = 0 \tag{3.5}$$

The basic operation principle of a 3-ϕ RCD is illustrated in Figure 3.9. The RCD consists of a current transformer where the primary is comprised of the phase conductors (and neutral-conductor if present), and the secondary is a sensing coil. In the absence of any ground leakage current, the currents in the conductors of the current transformer primary sum to zero and no net flux is induced in the current transformer core. However, in the presence of ground leakage current, the net current in the transformer primary will no longer be zero. This will result in a non-zero net flux in the current transformer core which will induce a current in the sensing coil. If the sensing coil current is high enough, it will cause a relay to open, thereby disconnecting the circuit and isolating the ground fault from the line voltage.

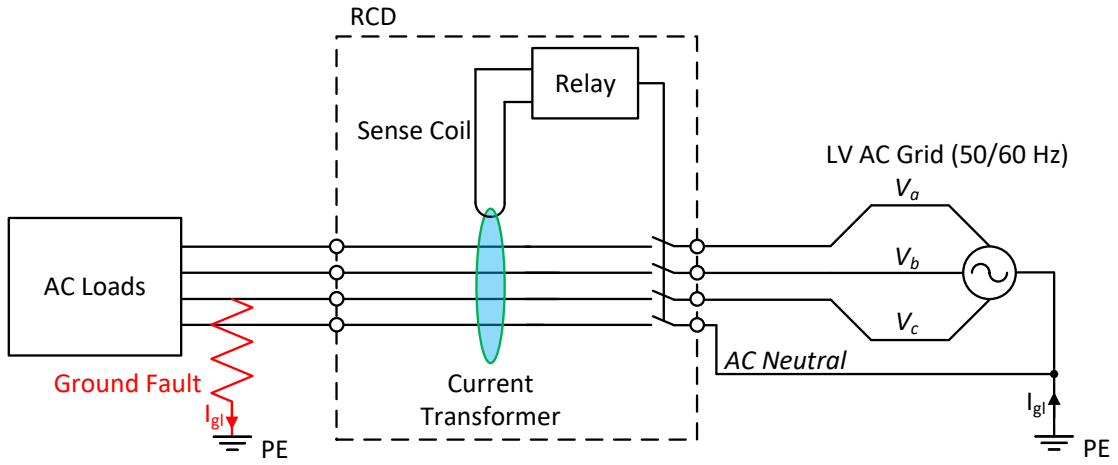
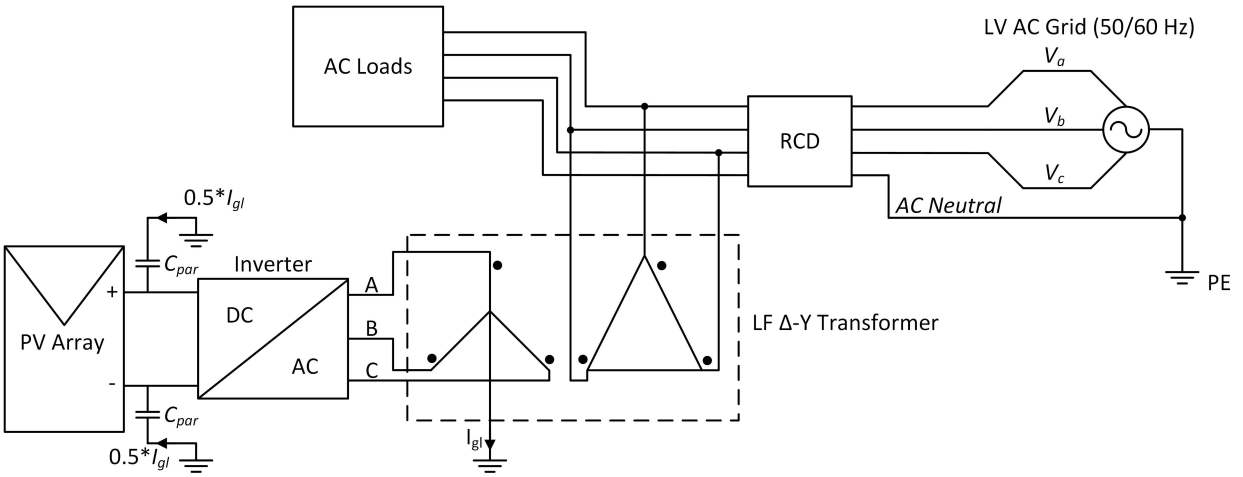


Figure 3.9: Three-phase RCD Basic Operation Principle

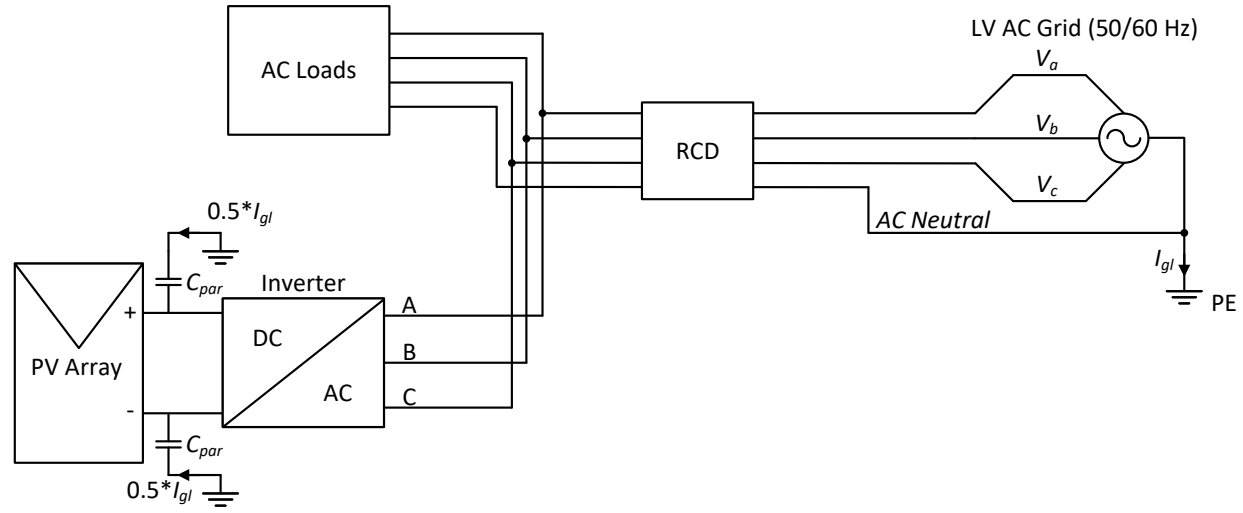
RCDs are designed to protect humans or animals, who come into contact with live conductors and create a ground fault, from harmful current flowing through the body. At 50 Hz, continuous currents greater than 30 mA and flowing for longer than 300 ms through a human body can cause ventricular fibrillation, resulting in a life-threatening situation for the person involved [29]. Therefore, the residual current tripping threshold and tripping time limits for RCDs used to protect humans are specified based on these limits in standards such as IEC 61008 [30]. At frequencies higher than 50 Hz, the risk of ventricular fibrillation in humans decreases. Therefore, standards such as IEC 60479 [31] establish a frequency factor, F_f, by which the RCD tripping threshold limit increases with frequency. Table 3.3 lists the IEC 60479 frequency factor and resulting RCD tripping threshold limit, I_{th}, for a range of frequencies above 50 Hz. It should be noted that IEC 60479 only specifies F_f for RCD tripping threshold limits up to 1 kHz. The presence of residual current frequency components greater than 1 kHz can reduce overall RCD sensitivity and result in an RCD not tripping even when the residual current exceeds I_{th} [32].

Table 3.3: IEC 60479 RCD Frequency Factors and Tripping Threshold Limits

Frequency (Hz)	F_f	I_{th} **(mA)**
50	1.0	30
100	1.5	45
200	2.0	60
300	4.5	135
400	5.8	174
500	7.0	210
600	9.2	276
700	11.2	336
800	12.3	369
900	13.3	399
1000	14.2	426



(a)



(b)

Figure 3.10: Grid-connected PV inverter with (a) LF transformer and (b) transformerless grid connection

Figure 3.10(a) and (b) illustrate why a grid-connected inverter with a transformerless connection can result in ground leakage currents that cause false tripping in RCDs. In the case of an inverter connecting a PV array to the LV AC grid, when a LF transformer is placed between the inverter and the grid, it presents a high impedance path for I_{cm} to flow into the grid. It can be observed from the transformer dot convention and Equation 3.5 that the only path for I_{cm} to flow from the LF transformer primary side to secondary side is the transformer primary-secondary inter-winding capacitance, C_{iw}. C_{iw} is a distributed capacitance that depends on the transformer insulation materials and winding geometries. However, it is typically on the order of 100 pF [9] which makes it a relatively high impedance to V_{cm} components in the line frequency range and even in the tens to hundreds of kHz. Therefore, the presence of a transformer between a grid-connected inverter and the AC grid will generally keep AC grid ground leakage current from the inverter V_{cm} negligibly low, thereby, preventing RCDs in the AC grid from false tripping. However, without the transformer, the remaining impedance for I_{cm} to flow into the AC grid is only the impedance of the inverter's AC filter, the AC grid impedance and the impedance of C_{par} in the case of a PV inverter. These impedances are much lower than C_{iw} in the relevant frequency range and I_{gl} due to the inverter V_{cm} can easily exceed the RCD tripping threshold limit.

3.3 Modulation Methods to Mitigate Common-Mode Current

It is obvious from Figure 3.6 circuit that I_{cm} can be reduced by increasing the values of the AC filter magnetics. Several approaches to reducing I_{cm} this way have been proposed [33] [34]. However, such approaches result in large and costly magnetic components. Furthermore, the effectiveness is limited for low-frequency components of I_{cm} as is demonstrated by Equation 3.3. Instead, it is preferable to develop methods of modulating the three-phase inverters to reduce I_{cm}.

Modulation methods to reduce I_{cm} in inverter systems have been researched quite extensively in an effort to enable transformerless PV inverter systems. Another motivation for minimizing inverter I_{cm} is found in motor drive applications where it can cause bearing currents and lead to premature bearing failures [35]. This motivation is an interesting and relevant one but is not analyzed in this work. There is extensive literature on I_{cm} reduction in 2-L inverter systems for both PV inverters and motor drive applications [11] [26] [36] [37] [38] [39]. The reasons for selecting the 3-L NPC inverter topology for the bipolar DC microgrid application were explained in Chapter 1. This section will give an overview of the existing methods for I_{cm} reduction in 3-L NPC inverters.

One typical approach for modulation-based I_{cm} reduction in the 3-L NPC inverter is to develop modulation methods that utilize converter state vectors with low or zero V_{cm}. For example, in PD SPWM and symmetric NTV SVM, the vectors used include the small, medium and large state vectors as well as the neutral zero state vector. As can be observed from Table 3.1 and Figure A1, this will result in V_{cm} values of 0, $\pm\frac{V_{DC}}{6}$ and $\pm\frac{V_{DC}}{3}$ throughout T_{sw}. In POD SPWM, the small vector redundancies with $V_{cm} = \pm\frac{V_{DC}}{3}$ are not utilized so the V_{cm} amplitude is reduced by 50%. Although the V_{cm} amplitude is reduced in POD SPWM, it still transitions between different V_{cm} values throughout T_{sw}, resulting in V_{cm} having AC components.

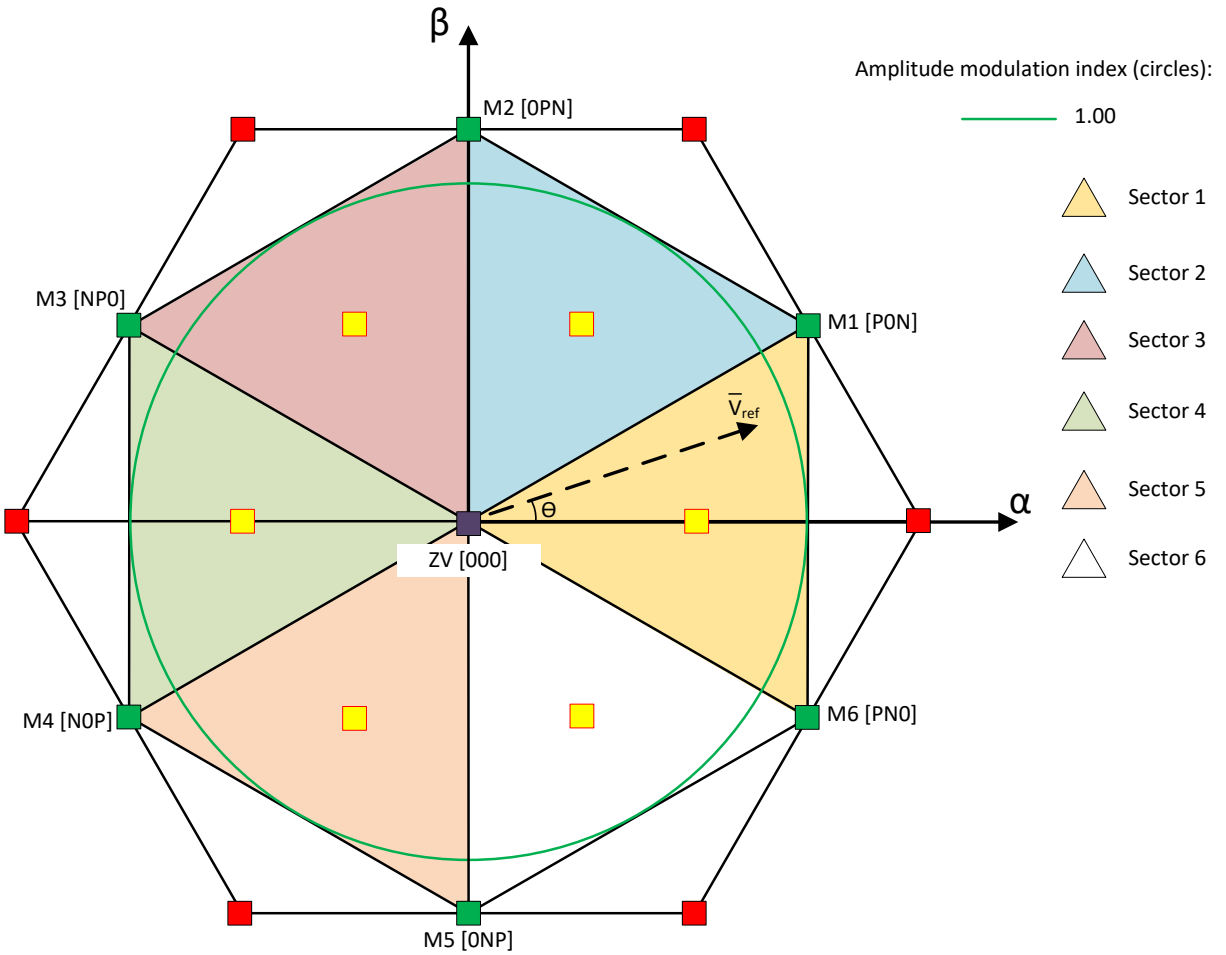


Figure 3.11: 3-L space vector hexagon illustrating M^{2}ZV SVM

A SVM method to completely eliminate V_{cm} by only using the neutral zero vector and the six medium vectors was proposed in [40]. These seven vectors all have V_{cm} equal to zero as shown in Table 3.1 and Figure A1. V_{cm} will inherently be zero if only these vectors are used and hence, I_{cm} will be zero. A carrier-based SPWM method to achieve the same result was proposed in [41] and the SVM method was analyzed in terms of I_{cm} elimination in PV systems in [10]. This method uses the 000 vector and the two nearest medium vectors in each vector sequence, and is therefore, denoted M^{2}ZV SVM. For implementing M^{2}ZV SVM, the six sectors of the space vector hexagon are shifted by 30°to correspond with the two nearest medium vectors, as shown in Figure 3.11. Figure 3.12 shows one possible M^{2}ZV SVM vector sequence for Sector I. One disadvantage of M^{2}ZV SVM is that two phase legs of the converter change state each vector transition resulting in higher switching losses per vector transition than the previously described modulation methods. M^{2}ZV SVM is limited to $m_a < 1.00$ because it does not use the large state vectors.

The modulation methods described above were simulated per the Figure 3.5 circuit and the Table 3.4 values. The resulting V_{cm}, I_{cm} and I_{gl} are shown over one T_{fund} in Figures 3.13, 3.14 and 3.15, respectively. For these results, the top and bottom C_{DC-BUS} were each modeled as an ideal voltage source at $\frac{V_{DC}}{2}$ because DC bus ripple and voltage drift were not considered for these simulations. The fast Fourier transforms (FFTs) of V_{cm}, I_{cm} and I_{gl} in the grid harmonic frequency range are shown in Figures 3.16, 3.17 and 3.18, respectively. The FFTs of V_{cm}, I_{cm} and I_{gl} at f_{sw} are shown in Figures 3.19, 3.20 and 3.21, respectively. The simulation results verify that, for POD SPWM, the V_{cm} amplitude is reduced from $\pm\frac{V_{DC}}{3}$ to $\pm\frac{V_{DC}}{6}$ compared to PD SPWM. It is also evident from the FFTs that the 650 Hz and 4.3 kHz resonances in the common-mode circuit significantly

influence the resulting I_{cm} and I_{gl} frequency component amplitudes. Even with relatively small V_{cm} frequency components close to these resonances, relatively large corresponding I_{cm} and I_{gl} frequency components result. Conversely, large V_{cm} can be generated at frequencies with high Z_{cm} without resulting in large I_{cm} and I_{gl}. This is particularly noticeable for the V_{cm} f_{sw} component generated in PD SPWM and 9-segment symmetric NTV SVM and the resulting I_{gl}. Here, the high attenuation of the inverter's LCL filter at f_{sw} is demonstrated. The results also demonstrate the inherent zero-sequence injection of symmetric NTV SVM which generates a very large third harmonic (150 Hz) V_{cm} component. This results in large I_{gl} at 150 Hz which obviously exceeds the IEC 60479 RCD tripping threshold limit for this frequency and would cause RCD false tripping.

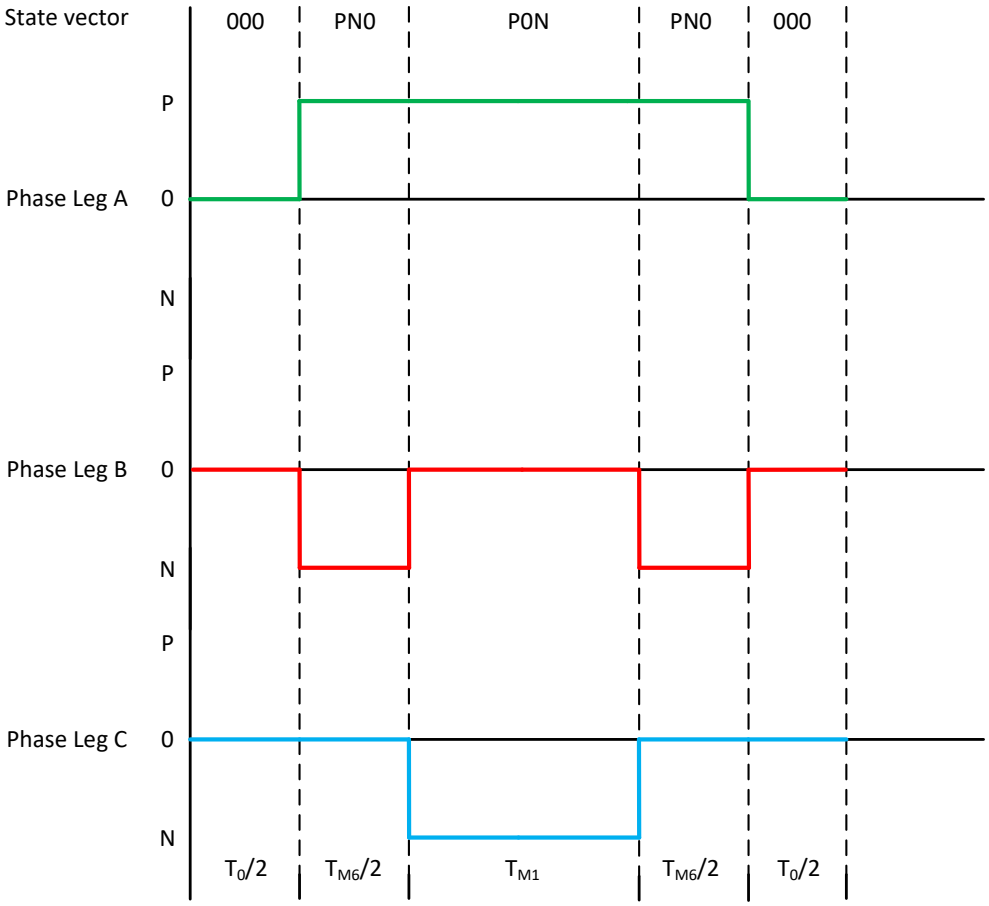
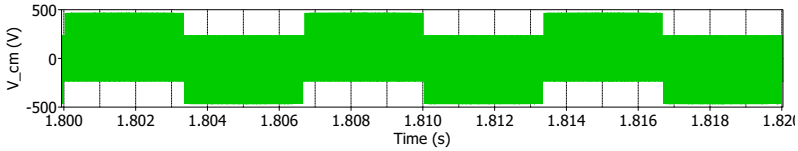


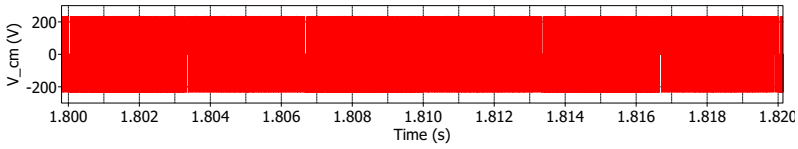
Figure 3.12: M^{2}ZV SVM Sector I vector sequence

Table 3.4: Converter and Grid Simulation Parameters

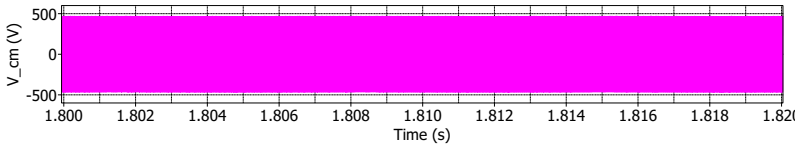
Parameter	Value	Unit
f_{sw}	50	kHz
t_d	200	ns
f_{grid}	50	Hz
V_{DC}	1400	V
$V_{AC-grid}$	400	V_{rms}
$P_{inverter}$	11	kW
$Q_{inverter}$	0	kVAR



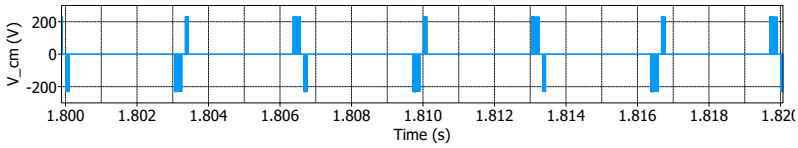
(a) PD SPWM



(b) POD SPWM

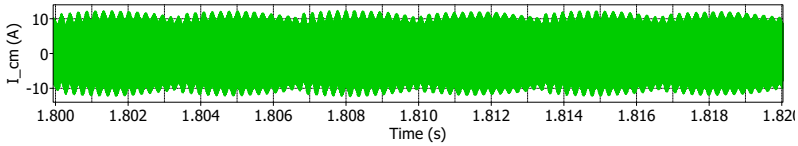


(c) 9-segment symmetric NTV SVM

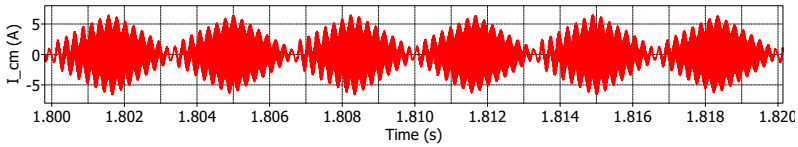


(d) M^{2}ZV SVM

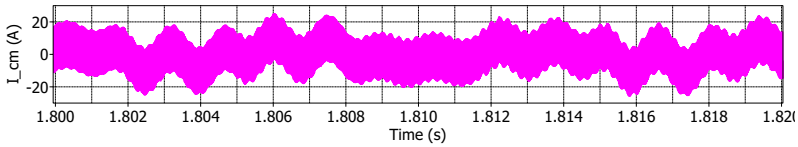
Figure 3.13: V_{cm} simulation results for PWM methods to reduce I_{cm}



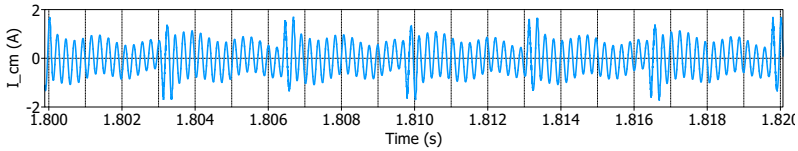
(a) PD SPWM



(b) POD SPWM

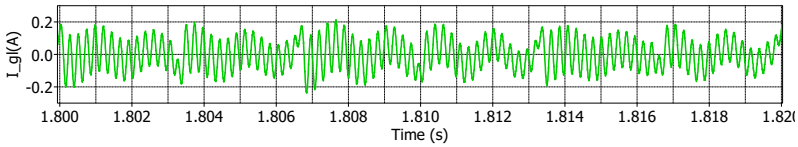


(c) 9-segment symmetric NTV SVM

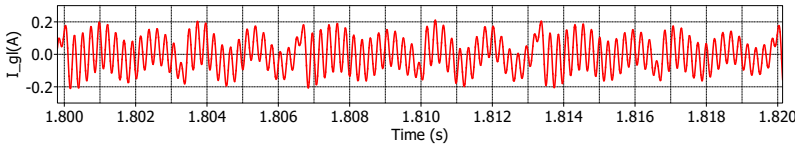


(d) M^{2}ZV SVM

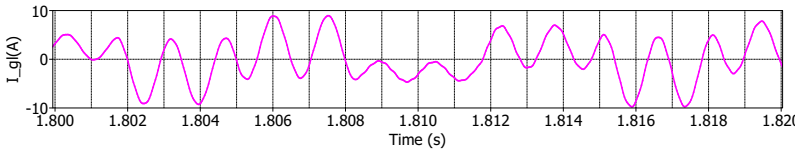
Figure 3.14: I_{cm} simulation results for PWM methods to reduce I_{cm}



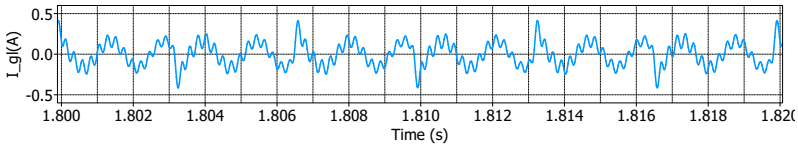
(a) PD SPWM



(b) POD SPWM

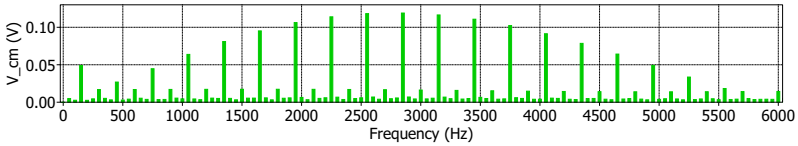


(c) 9-segment symmetric NTV SVM

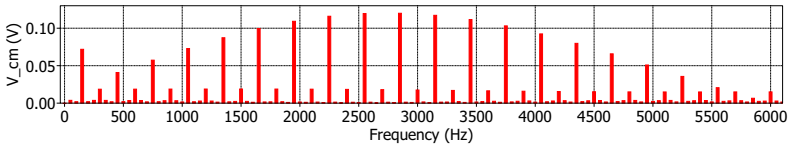


(d) M^{2}ZV SVM

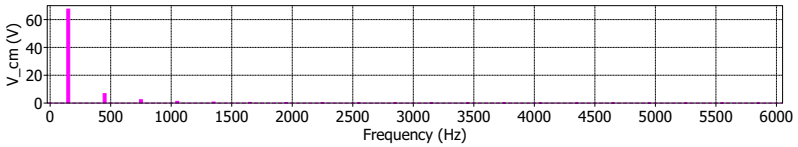
Figure 3.15: I_{gl} simulation results for PWM methods to reduce I_{cm}



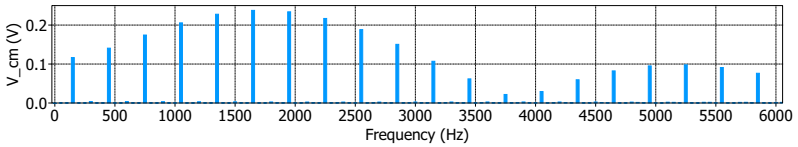
(a) PD SPWM



(b) POD SPWM

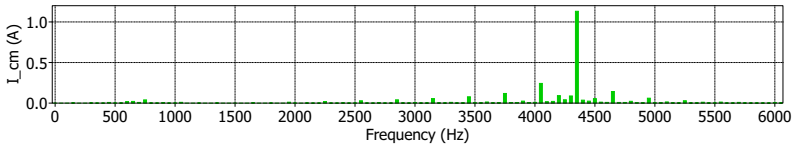


(c) 9-segment symmetric NTV SVM

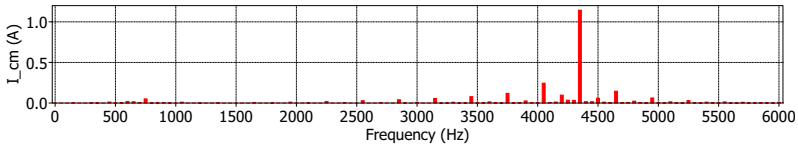


(d) M^{2}ZV SVM

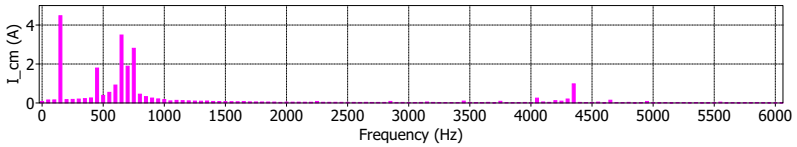
Figure 3.16: V_{cm} simulation results grid harmonic range FFT for PWM methods to reduce I_{cm}



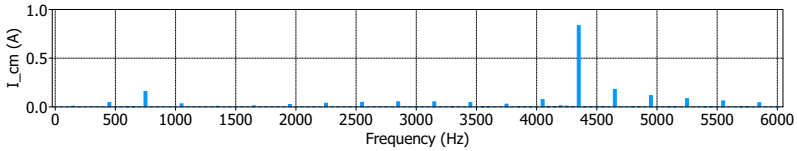
(a) PD SPWM



(b) POD SPWM

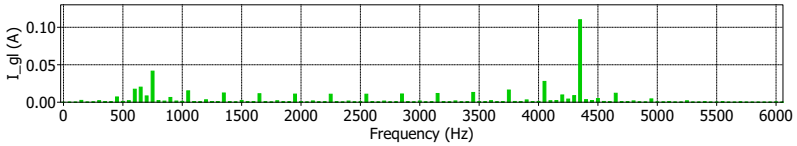


(c) 9-segment symmetric NTV SVM

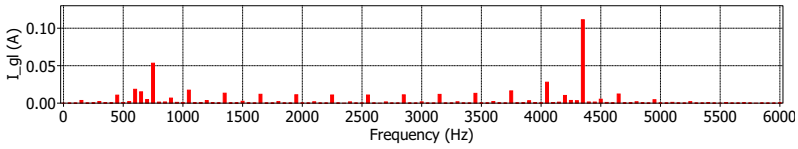


(d) M^{2}ZV SVM

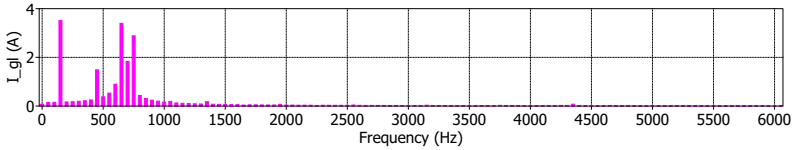
Figure 3.17: I_{cm} simulation results grid harmonic range FFT for PWM methods to reduce I_{cm}



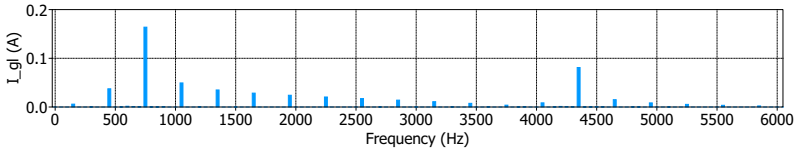
(a) PD SPWM



(b) POD SPWM

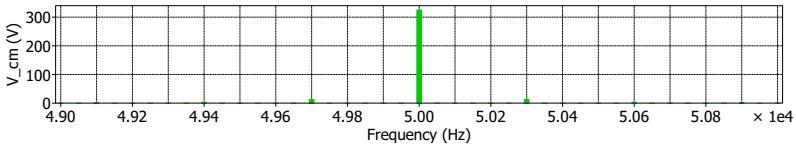


(c) 9-segment symmetric NTV SVM

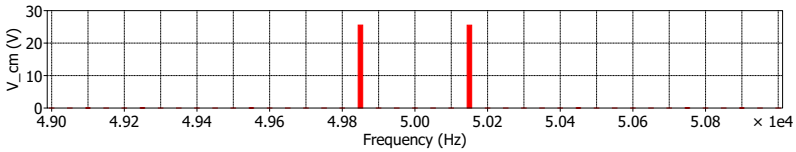


(d) M^{2}ZV SVM

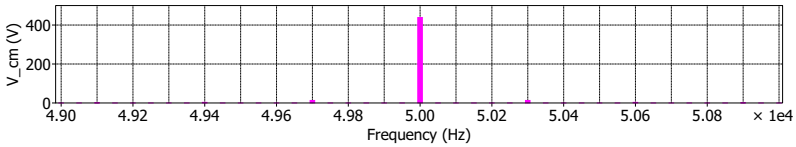
Figure 3.18: I_{gl} simulation results grid harmonic range FFT for PWM methods to reduce I_{cm}



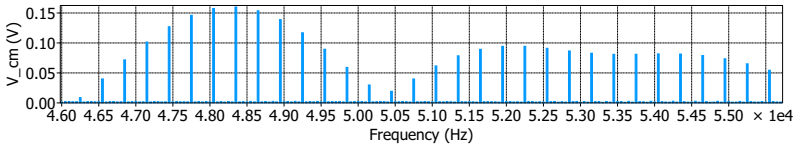
(a) PD SPWM



(b) POD SPWM

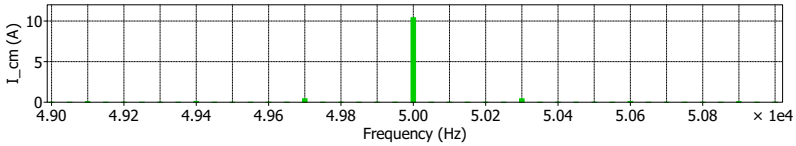


(c) 9-segment symmetric NTV SVM

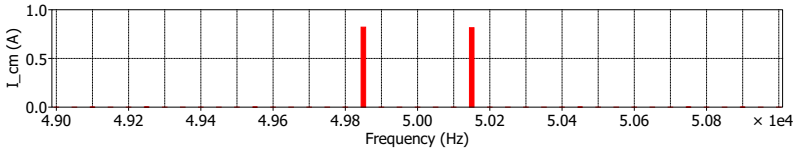


(d) M^{2}ZV SVM

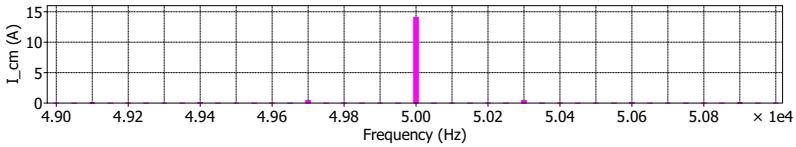
Figure 3.19: V_{cm} simulation results FFT at f_{sw} for PWM methods to reduce I_{cm}



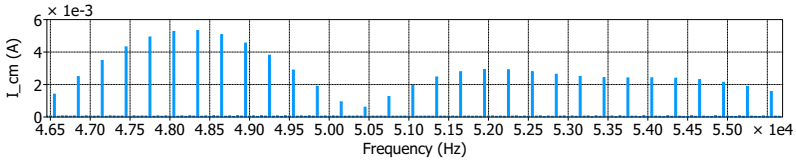
(a) PD SPWM



(b) POD SPWM

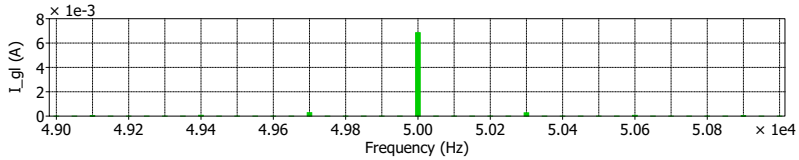


(c) 9-segment symmetric NTV SVM

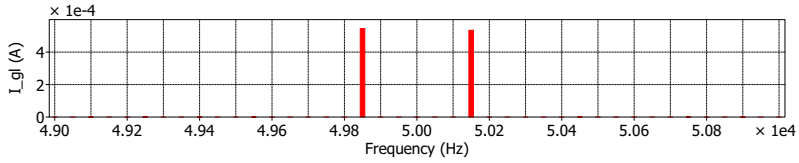


(d) M^{2}ZV SVM

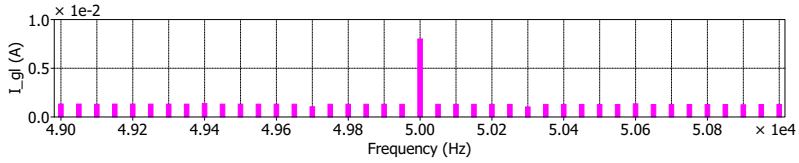
Figure 3.20: I_{cm} simulation results FFT at f_{sw} for PWM methods to reduce I_{cm}



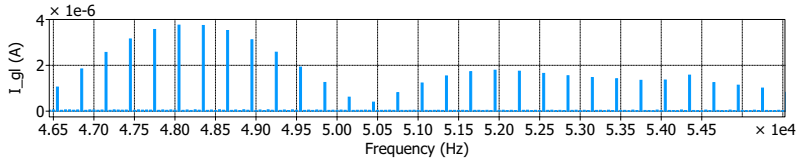
(a) PD SPWM



(b) POD SPWM



(c) 9-segment symmetric NTV SVM



(d) M^{2}ZV SVM

Figure 3.21: I_{gl} simulation results FFT at f_{sw} for PWM methods to reduce I_{cm}

The large 150 Hz V_{cm} component generated by symmetric NTV SVM is not present for the other three simulated modulation methods. In the 50 Hz to 1 kHz range, these modulation methods result in I_{gl} components that are below the Table 3.3 values. However, larger I_{gl} components result at 4.3 kHz due to the common-mode circuit resonance. As mentioned in Section 3.2.2, residual current frequency components greater than 1 kHz have been shown to reduce overall RCD sensitivity. Therefore, I_{gl} components above 1 kHz should also be minimized to prevent a dangerous situation from occurring where the RCD fails to trip even when I_{th} is exceeded.

3.4 Proposed SVM Method to Reduce Ground Leakage Current

As was shown in Section 3.3, V_{cm} frequency components at frequencies where the inverter LCL filter has high attenuation, such as f_{sw}, do not result in high I_{gl} values. Therefore, a modulation concept for a 2-L inverter was proposed in [42] that shifts the frequency composition of V_{cm} to f_{sw}. This can be achieved by ensuring that the V_{cm} volt-second balance, V_{cm-vs}, over T_{sw} is equal to zero. This is done in the 2-L inverter by redistributing the zero vector dwell time to the positive and negative zero vectors such that the total zero vector V_{cm} volt-second balance is equal in magnitude and opposite in sign to the V_{cm} volt-second balance of the two active vectors used in each switching sequence. This results in a V_{cm} waveform composed of multiple square waves with frequency, f_{sw}. The decomposition of each square wave into a Fourier series results in sinusoidal components at or above the square wave frequency. This is shown by Equation 3.6 where *f(t)* is a square wave with odd symmetry and frequency, ω, in radians/s. V_{cm-vs} for a 2-L NTV state vector sequence in Sector I is given by Equation 3.7.

$$f(t) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(n\omega t) \tag{3.6}$$

$$V_{cm-vs} = V_{cm-V1} * T_{V1} + V_{cm-V2} * T_{V2} + V_{cm-V0p} * T_{V0p} + V_{cm-V0n} * T_{V0n} \tag{3.7}$$

In this work, the concept of shifting V_{cm} to f_{sw} is extended to the 3-L NPC inverter and is denoted switching period common-mode balancing (SPCMB) SVM. In symmetric NTV SVM, the dwell time of each small state vector is typically distributed evenly between the two redundancies of that small state vector in each switching period. From Figure A1, it can be seen that there are two small vectors in each sector of the space vector hexagon. One of the small vectors has positive redundancy with V_{cm} equal to $\frac{V_{DC}}{3}$ and negative redundancy with V_{cm} equal to $\frac{-V_{DC}}{6}$. This type of small vector is denoted V_{SA} with dwell time T_{SA}. The other small vector has a positive redundancy with V_{cm} equal to $\frac{V_{DC}}{6}$ and negative redundancy with V_{cm} equal to $\frac{-V_{DC}}{3}$. This type of small vector is denoted V_{SB} with dwell time T_{SB}. This denotation is shown for Sector I in Figure 3.22.

By distributing the small vector dwell times equally to their redundancies, it is apparent that the small vector volt-second balance will be positive when T_{SA} is greater than T_{SB} and negative when T_{SB} is greater than T_{SA}. Due to the arrangement of the V_{SA} and V_{SB} state vectors in the space vector hexagon, the inequality between T_{SA} and T_{SB} alternates every 60°, resulting in V_{cm-vs} oscillating at three times f_{grid}, resulting in a large third harmonic component in V_{cm}. In SPCMB SVM, T_{SA} and T_{SB} are distributed between the V_{SA} and V_{SB} redundancies as shown in Table 3.5 for Sector I where the positive small vector redundancies are denoted with subscript p and the negative small vector redundancies are denoted with subscript n. All of the zero vector dwell time is distributed to the neutral zero vector redundancy, V_{ZV0} so it does not contribute to V_{cm-vs}. This dwell time distribution can be established for the other five sectors and results in V_{cm-vs} being equal to zero over T_{sw} which is formally defined by Equation 3.8. If Equation 3.8 is satisfied for every switching period within T_{fund} and the resulting V_{cm} waveform is half-wave symmetric within T_{sw}, V_{cm} will only contain frequency components at or above f_{sw}.

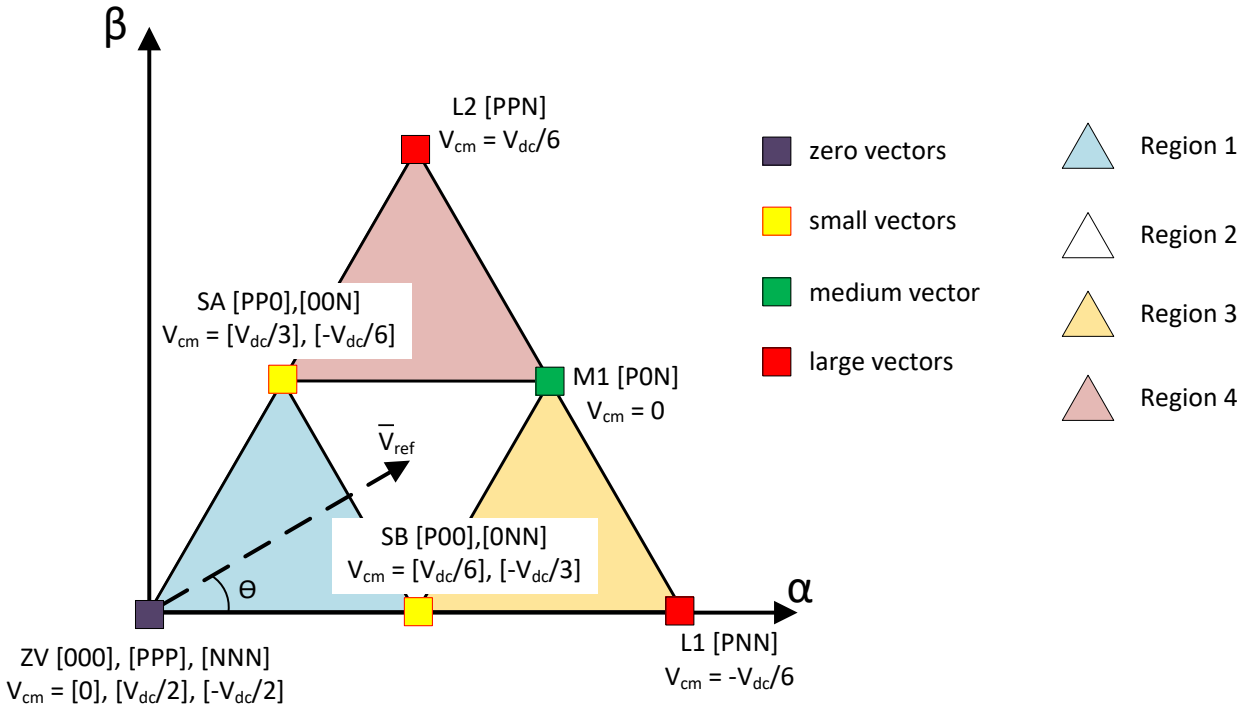


Figure 3.22: SPCMB SVM V_{SA} and V_{SB} in Sector I of 3-L space vector hexagon

Table 3.5: SPCMB SVM Small State Vector Redundancy Dwell Time Distribution in Sector I

Region	**State Vector**	Dwell Time
1	V_{SAp}	$\frac{1}{3}T_{SA}$
	V_{SAn}	$\frac{2}{3}T_{SA}$
	V_{SBp}	$\frac{2}{3}T_{SB}$
	V_{SBn}	$\frac{1}{3}T_{SB}$
	V_{ZV0}	T_{ZV}
2	V_{SAp}	$\frac{1}{3}T_{SA}$
	V_{SAn}	$\frac{2}{3}T_{SA}$
	V_{SBp}	$\frac{2}{3}T_{SB}$
	V_{SBn}	$\frac{1}{3}T_{SB}$
	V_{M1}	T_{M1}
3	V_{SBp}	$\min(T_{SB}, \frac{1}{3}T_{L1} + \frac{2}{3}T_{SB})$
	V_{SBn}	$T_{SB} - T_{SBp}$
	V_{L1}	T_{L1}
	V_{M1}	T_{M1}
4	V_{SAn}	$\min(T_{SA}, \frac{1}{3}T_{L2} + \frac{2}{3}T_{SA})$
	V_{SAp}	$T_{SA} - T_{SAn}$
	V_{L2}	T_{L2}
	V_{M1}	T_{M1}

$$\int_0^{T_{sw}} V_{cm} dt = 0 \tag{3.8}$$

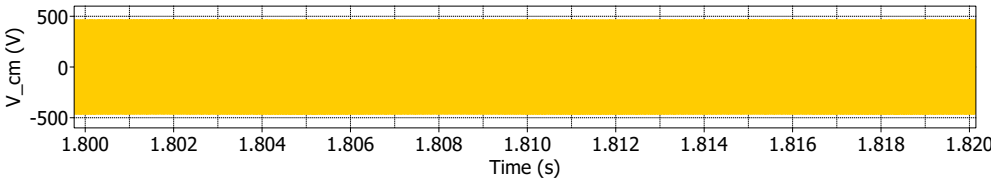
The simulation results for SPCMB, under the conditions specified in Section 3.3, are shown below. The results for V_{cm}, I_{cm} and I_{gl} are shown in Figures 3.23, 3.24 and 3.25, respectively. It can be observed in Figure 3.23 that SPCMB reduces V_{cm} in the grid harmonic frequency range and shifts it to f_{sw}. The result is a reduction of I_{cm} and I_{gl} at the 650 Hz and 4.3 kHz Z_{cm} resonances compared to PD SPWM, POD SPWM and M^{2}ZV SVM. Additionally, the I_{gl} component at f_{sw} is still relatively low despite the large V_{cm} at this frequency. Table 3.6 gives a summary of the ground leakage currents of the different modulation methods compared to the RCD tripping threshold limits, as well as the I_{gl} peak values. As can be observed, I_{gl} for each of the modulation methods is below i_{th} in the 50 Hz to 1 kHz range. However, SPCMB SVM produces significantly lower I_{gl} components close to the common-mode impedance resonance points. Additionally, the peak value of I_{gl} is 72% lower for SPCMB SVM compared to POD SPWM, the second lowest. 9-segment NTV SVM is not shown because it produces I_{gl} that is far in excess of the RCD tripping threshold limit.

SPCMB SVM uses the same state vectors as symmetric NTV SVM. Therefore, it can achieve m_a up to 1.15. However, it can be seen from Figure 3.22 that if $|\bar{V}_{\text{ref}}|$ is greater than the point halfway between SB and L1 on the α-axis, there will be portions of T_{fund} in Regions 3 and 4 where the

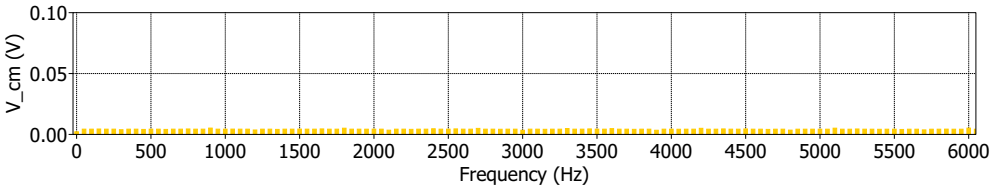
dwell time of L1 is greater than the dwell time of SB. The same applies to L2 and SA, respectively. Under this condition, Equation 3.8 cannot be satisfied because there is not sufficient small vector dwell time to redistribute in order to match the V_{cm-} volt-second balance of the respective large vector. This condition will occur for $m_a > 1.00$ and demonstrates the necessity of adding a zero sequence to the converter output voltage in order to achieve higher modulation indexes. Thus, SPCMB SVM can only satisfy Equation 3.8 and fully shift V_{cm-} to f_{sw} for $m_a < 1.00$. In theory, SPCMB SVM completely shifts V_{cm} to f_{sw}. The small components at the lower frequencies seen in the simulation results are due to the minimum pulse-width non-ideality due to dead-time, described in Chapter 2.

Table 3.6: Ground Leakage Current (I_{gl}) Performance Under Ideal DC Bus Conditions

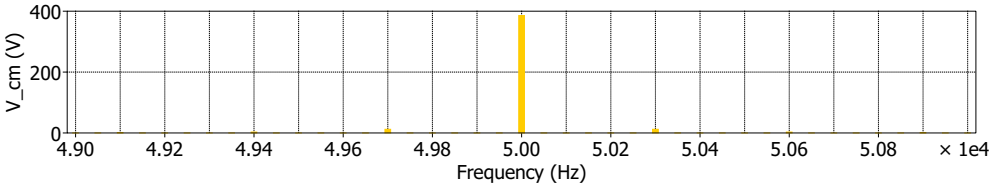
	RCD i_{th}	**PD SPWM**	**POD SPWM**	**M^{2}ZV SVM**	**SPCMB SVM**
150 Hz	57 mA	3 mA	4 mA	6 mA	0 mA
650 Hz	309 mA	20 mA	15 mA	0 mA	17 mA
750 Hz	345 mA	41 mA	53 mA	164 mA	4 mA
4.35 kHz	N/A	110 mA	111 mA	81 mA	10 mA
I_{gl} peak	N/A	214 mA	211 mA	413	59 mA



(a) V_{cm} over T_{fund}

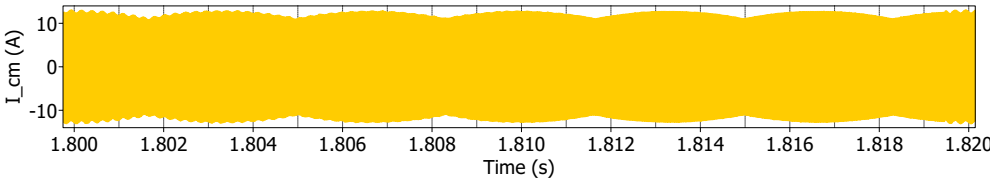


(b) V_{cm} FFT in grid harmonic range

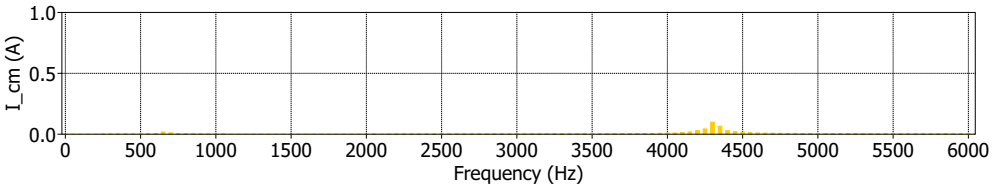


(c) V_{cm} FFT at f_{sw}

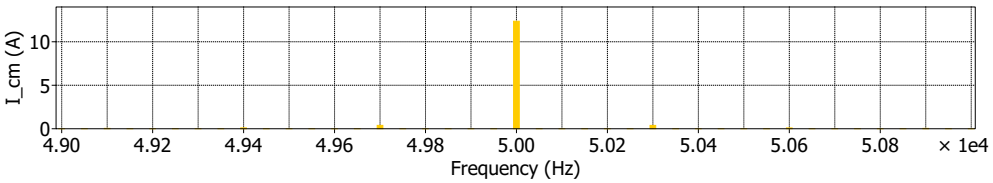
Figure 3.23: V_{cm} simulation results for SPCMB SVM



(a) I_{cm} over T_{fund}

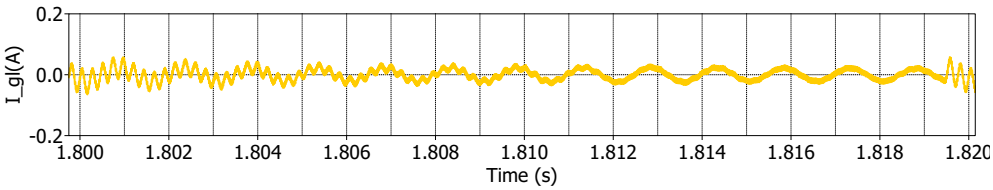


(b) I_{cm} FFT in grid harmonic range

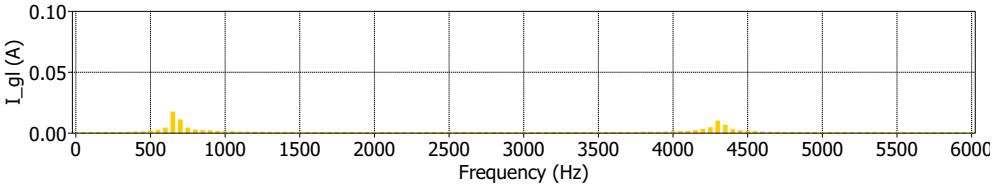


(c) I_{cm} FFT at f_{sw}

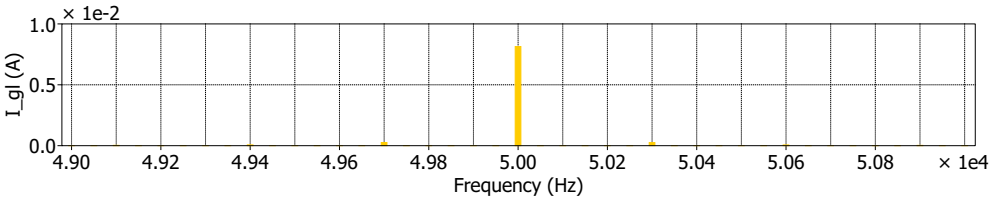
Figure 3.24: I_{cm} simulation results for SPCMB SVM



(a) I_{gl} over T_{fund}



(b) I_{gl} FFT in grid harmonic range



(c) I_{gl} FFT at f_{sw}

Figure 3.25: I_{gl} simulation results for SPCMB SVM

3.5 Chapter Summary

In this chapter, an analysis of 3-L DC-AC converter common-mode voltage was presented. Then, the common-mode impedance in a grid-tied DC-AC converter was analyzed and presented to bet-

ter understand the resulting common-mode and ground leakage currents. Next, several existing modulation methods were simulated under ideal DC bus conditions, with the DC poles modeled as voltage sources, and their common-mode performance was evaluated. Then, a SVM method that mitigates ground leakage current by shifting the frequency composition of the common-mode voltage to the switching frequency was presented and simulated. The simulation results show that this modulation method reduces the ground leakage current compared to PD SPWM and POD SPWM, which already keep this current relatively low due to no zero sequence injection. The reduction is particularly observable at the resonant points of the common-mode impedance where the resonance results in very low impedance for common-mode voltage components at those frequencies.

Chapter 4: Bipolar DC Microgrid Balancing with NPC Inverter

4.1 Load Imbalance in Bipolar DC Microgrid System

Some of the benefits of the bipolar DC microgrid architecture in comparison to the unipolar architecture were explained in Chapter 1. One of the challenges in implementing the bipolar architecture is maintaining voltage balance between the two DC poles. This can be particularly challenging because the loading of the DC poles can be unequal and unpredictable. For example, there may be an equal number of EV chargers on each DC pole of the bipolar DC microgrid in Figure 1.1. However, the number of EVs using the chargers on each DC pole at a given moment can often be unequal, resulting in a larger amount of power being drawn from one DC pole than the other. Without active balancing of the DC poles, their voltages will quickly diverge with the more loaded DC pole voltage dropping and the less loaded DC pole voltage rising. To prevent this, the DC microgrid can use one or more balancing converters. These are power electronic converters placed in the DC microgrid that redirect power from one DC pole to the other to keep their voltages balanced regardless of the load imbalance between the DC poles. Several balancing converter topologies exists but they all function on the same basic principle of imposing a DC current in the neutral conductor, DC_n, to ensure the effective load on each DC pole is equal and the voltages remain balanced [8]. Figure 4.1 shows one of the possible balancing converter topologies which is based on a bidirectional buck-boost converter. Topologies such as this can work effectively as dedicated balancing converters in bipolar DC microgrid systems. However, the need for a dedicated balancing converter increases overall system cost and complexity.

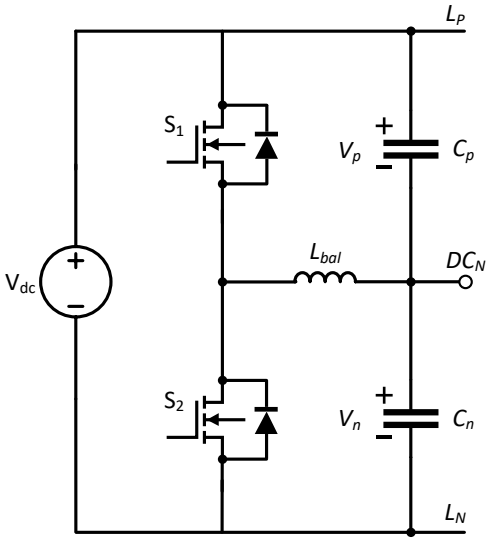


Figure 4.1: Bidirectional buck-boost balancing converter topology

The concept of using a 3-L NPC distribution converter in a bipolar DC microgrid system to provide DC pole balancing was investigated in [43] and [44]. However, these works assume a connection to the AC grid with a LF transformer and, therefore, do not consider common-mode voltage and ground leakage current issues in relation to NPC active DC balancing operation. In Section 4.2, an overview of the DC bus balancing and third harmonic ripple issues in NPC converters is given and the common approaches to solve these issue are reviewed. Section 4.5 provides a review of 3-L NPC converter modulation methods that are designed to simultaneously balanced the DC bus and reduce common-mode current, I_{cm}. Then, a modulation method is proposed to simultaneously provide active DC microgrid pole balancing with the 3-L NPC converter while balancing V_{cm} over each switching period to achieve low I_{gl} in a transformerless AC grid connection.

4.2 NPC Inverter Modulation Methods for DC Bus Balancing

The DC bus balancing issue in the 3-L NPC converter is well established in literature [45] [46]. In the NPC converter of Figure 4.2, it is essential for the DC neutral point voltage to be maintained halfway between the positive and negative DC bus terminals such that V_t and V_b are equal. If this condition is not met, the switching devices in each phase leg can be forced to block more than half of the DC bus voltage and the AC output voltages can become distorted. A comprehensive analysis from a SVM perspective was conducted in [46] where the effect of each 3-L NPC converter state vector on the DC neutral-point current, i_{np}, was established. Figure 4.3 shows how each category of state vector affects i_{np}. It can be observed that zero and large state vectors result in i_{np} equal to zero based on Equation 3.5. Thus, these state vectors have no net effect on the DC bus voltage balance. Each small and medium vector will result in one of the phase currents flowing either into or out of the DC neutral-point, *NP*. Table 4.1 lists i_{np} for each state vector. From Figure 4.3 and Table 4.1, it can be observed that p-type small state vector redundancies discharge C_t during inverter operation at power factor (PF) = 1 and charge C_t during rectifier operation at PF = -1. Likewise, n-type small state vector redundancies charge C_b during rectifier operation at PF = -1 and discharge C_b during inverter operation at PF = 1. The small vector dwell times can then be distributed to the p-type and n-type redundancies to charge/discharge C_t and C_b in order to balance the DC bus. In the carrier-based SPWM methods, the small vector dwell time redistribution is typically realized by adding a DC offset to the carrier waveforms to balance the DC bus.

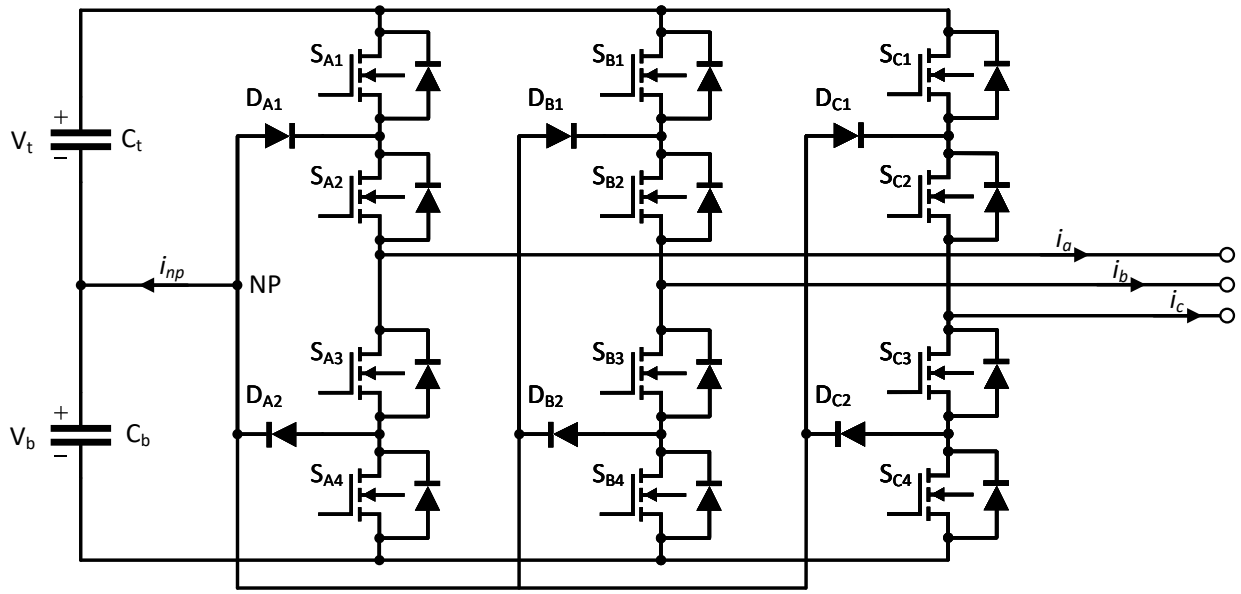
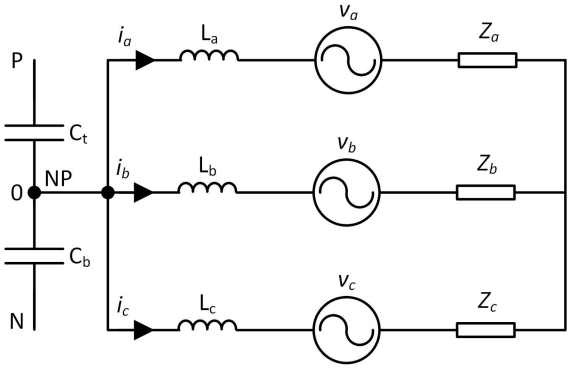
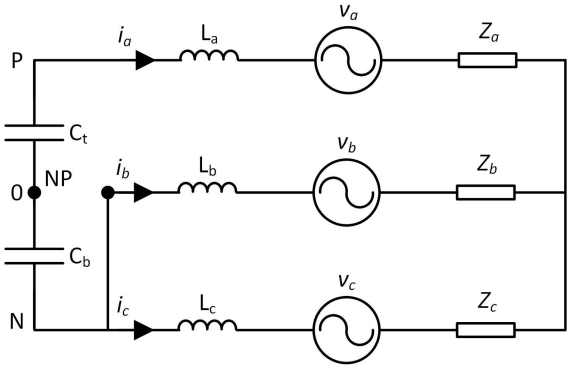


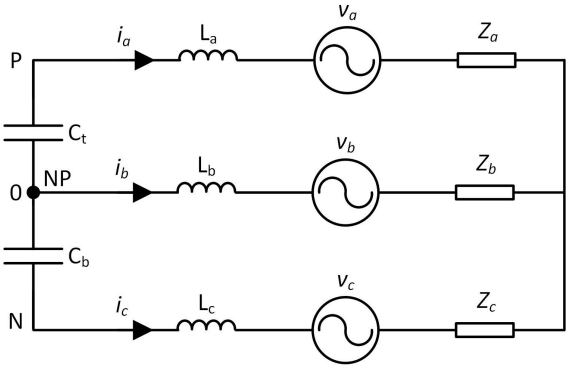
Figure 4.2: 3-L 3-ϕ NPC converter neutral point current



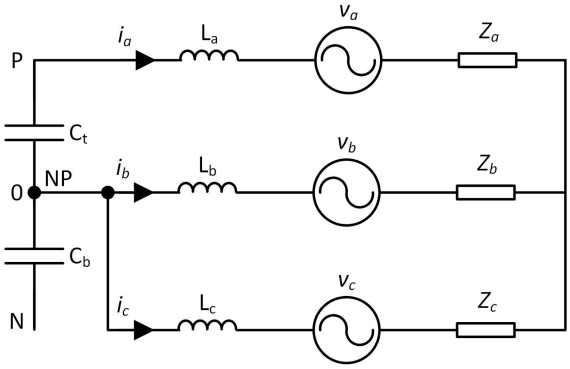
(a) Zero state vector (000)



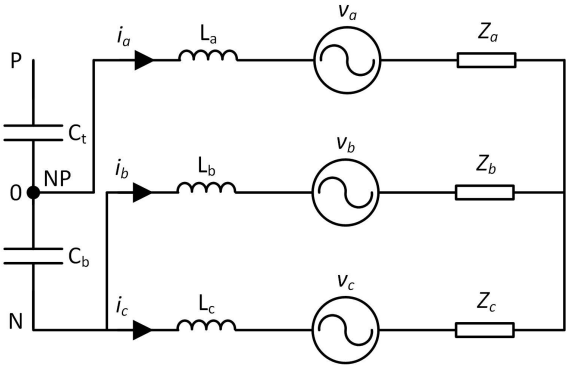
(b) Large state vector (PNN)



(c) Medium state vector (P0N)



(d) Small state vector, p-type redundancy (P00)



(e) Small state vector, n-type redundancy (0NN)

Figure 4.3: Neutral-point current for different 3-L state vector types

For a 3-L NPC converter used in traditional applications such as motor drives or static VAR compensation (SVC) systems, the converter is typically fed from a unipolar DC voltage. Capacitors are connected in series inside the converter to create the neutral-point, as shown in Figure 1.7(a). Therefore, the imbalance on the DC bus only consists of asymmetries in the NPC converter itself. However, as described in Section 4.1, the NPC converter shares the bipolar DC bus with DC sources and loads in the bipolar DC microgrid application considered in this work. These sources and loads can be unbalanced and the bipolar grid, therefore, requires active DC pole balancing. By redistributing the small state vector dwell times as previously described, the NPC converter can be modulated to provide the active DC pole balancing. The DC bus load imbalance, ϵ, is defined by Equation 4.1 where P_t and P_b are the DC loads of the top and bottom DC poles, respectively. The larger the amount of imbalance in the DC bus, the more small vector dwell time must be redistributed to compensate for the imbalance.

Table 4.1: Three-Level NPC State Vector Neutral-Point Currents

State Vector Category	**Switching State**	i_{np}
Zero vectors	000, PPP, NNN	0
Small vectors	P00, 0NN	i_a, $-i_a$
	0P0, N0N	i_b, $-i_b$
	00P, NN0	i_c, $-i_c$
	0PP, N00	$-i_a$, i_a
	P0P, 0N0	$-i_b$, i_b
	PP0, 00N	$-i_c$, i_c
Medium vectors	0PN, 0NP	$-i_a$
	P0N, N0P	$-i_b$
	PN0, NP0	$-i_c$
Large vectors	PNN, PPN, NPN, NPP, NNP, PNP	0

$$\epsilon = \frac{P_t - P_b}{P_t + P_b} \tag{4.1}$$

It was shown in [43] that there is a limitation to ϵ for which the NPC converter can maintain balanced DC pole voltages and that this limitation is a function of NPC converter modulation index, m_a. For m_a above 0.577, where $\bar{V}_{\text{ref}}$ lies in Regions 2, 3 and 4 of the space vector hexagon for some or all of T_{fund}, this limitation is due to a reduction of total small vector dwell time as m_a increases. At a given m_a above 0.577, the amount of small vector dwell time available to redistribute during T_{sw} is limited, with the remainder of T_{sw} being spent dwelling on medium and large vectors. Therefore, the limit for ϵ decreases as m_a increases. For $m_a < 0.577$, $\bar{V}_{\text{ref}}$ only lies in Region 1. Therefore, the state vectors on which power is exchanged in the DC bus are all small state vectors. In [43], a 7-segment SVM vector sequence was used in all four regions of the space vector hexagon where Regions 1 and 2 are each divided into two half regions, as shown in Figure 4.4. Under this modulation scheme, a different 7-segment vector sequence is used in each half region. [43] showed that ϵ has a constant limit for $m_a < 0.577$ with the 7-segment vector sequences. This limit results from using both redundancies of only one of the small vectors in the vector sequence within each half region. However, a 9-segment vector sequence can be implemented in Region 1 which uses both redundancies of both small vectors in each vector sequence. This enables the NPC converter to balance the DC poles at ϵ up to 1 for $m_a < 0.577$. The 9-segment and 7-segment vector sequences for Sector I, Region 1 are shown in Figures 4.5 and 4.6, respectively. The main disadvantage of the 9-segment vector sequence is the higher number of switching transitions required, resulting in higher switching losses compared to the 7-segment sequences. [43] proposes adding a fourth leg to the NPC converter to overcome the balancing limitation for $m_a > 0.577$ and $m_a < 0.577$ with the 7-segment vector sequence. The fourth leg operates as a balancing converter to maintain DC pole balancing for ϵ above the NPC converter balancing limit. However, the requirement of the fourth leg increases system cost and complexity. For the bipolar DC microgrid application where the NPC converter will always operate at $m_a < 0.577$, it makes more sense to enable balancing over the full range of ϵ by using the 9-segment vector sequence.

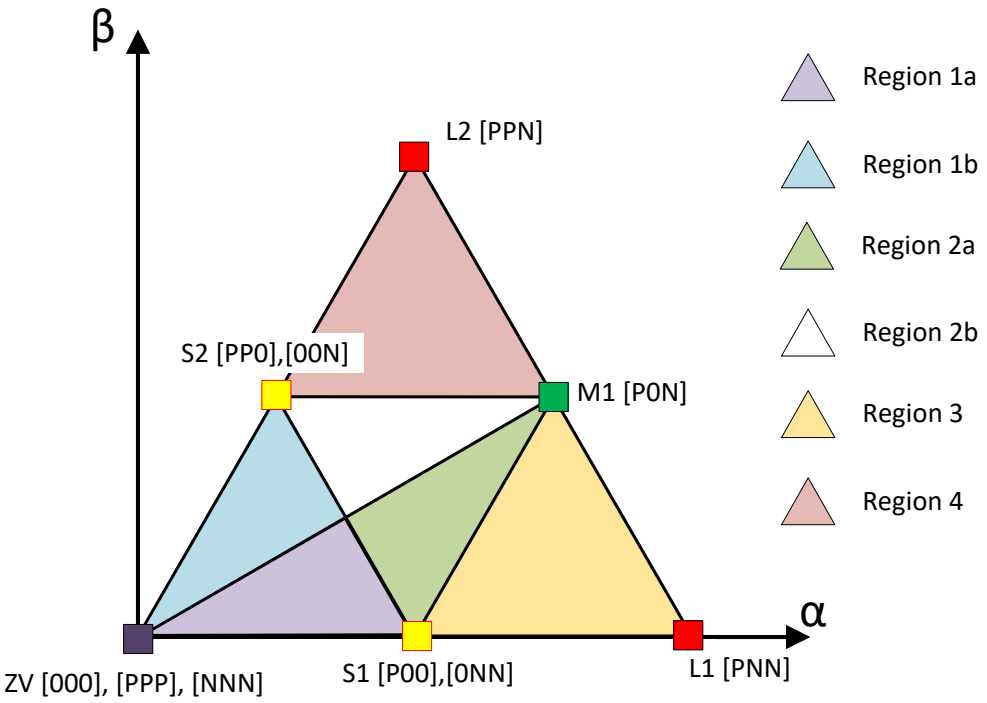


Figure 4.4: Space vector hexagon Sector I half regions

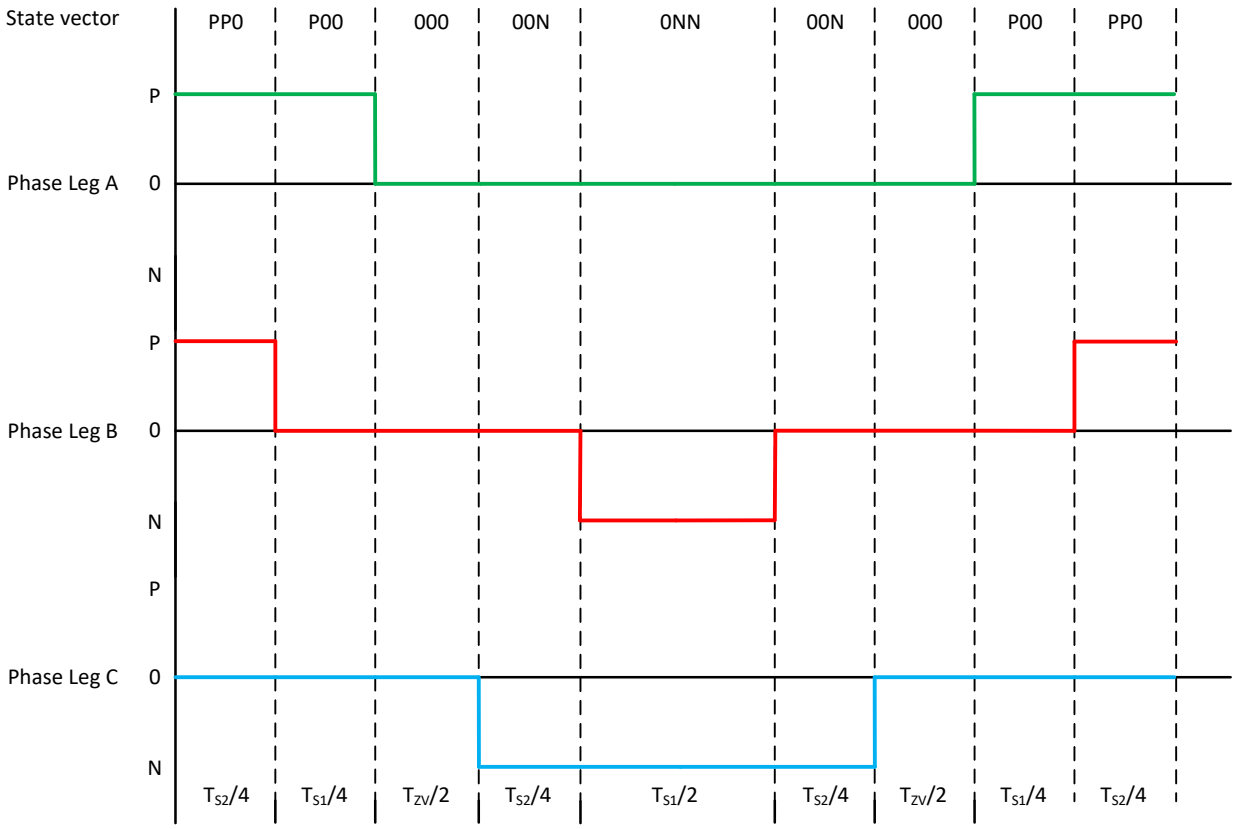
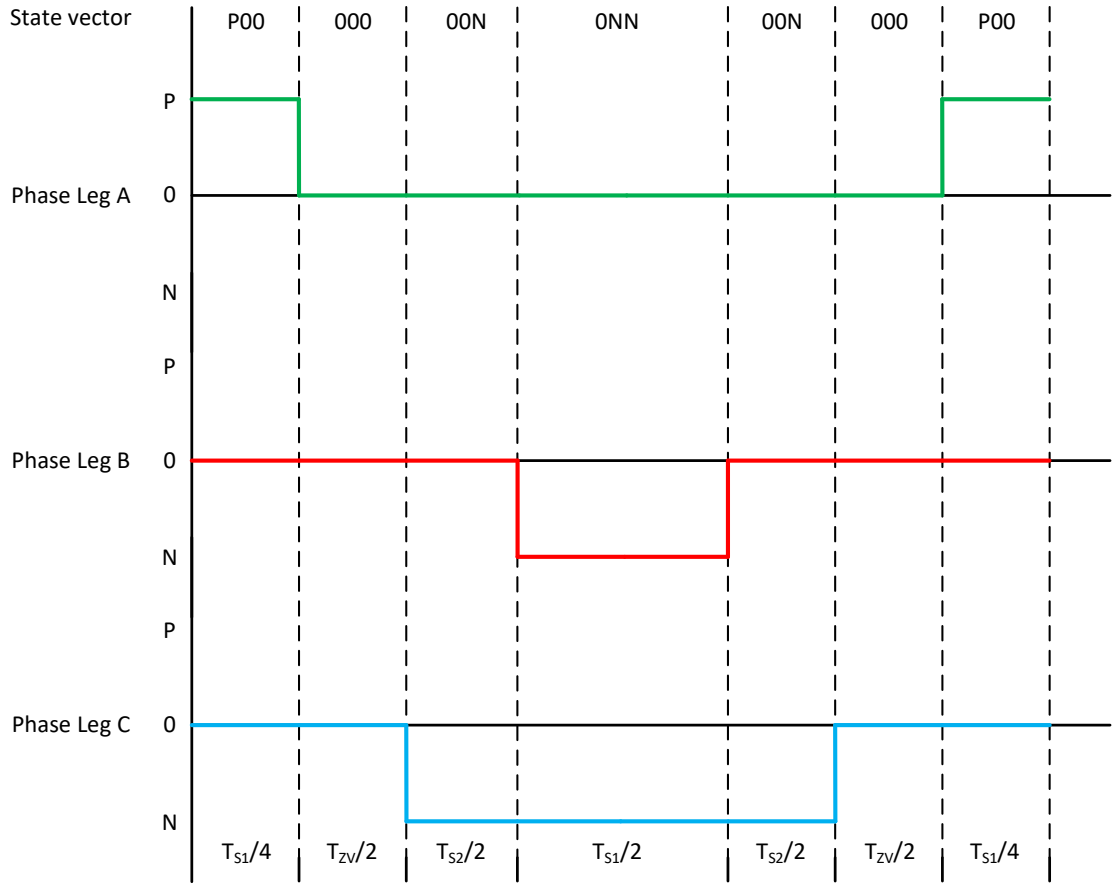
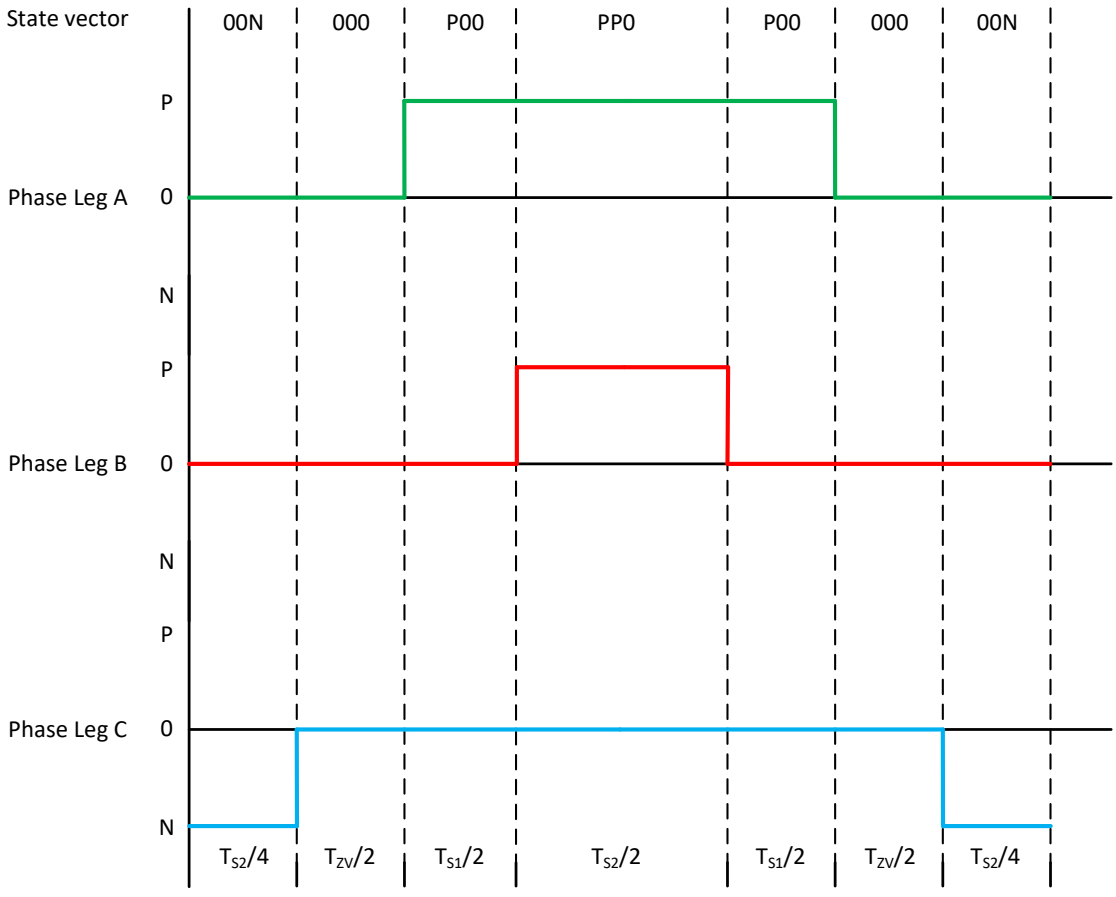


Figure 4.5: 9-segment SVM vector sequence in Sector I, Region 1



(a) Sector I, Region 1a vector sequence



(b) Sector I, Region 1b vector sequence

Figure 4.6: 7-segment SVM vector sequences in Sector I, Region 1

4.3 NPC Inverter DC Bus Third Harmonic Ripple

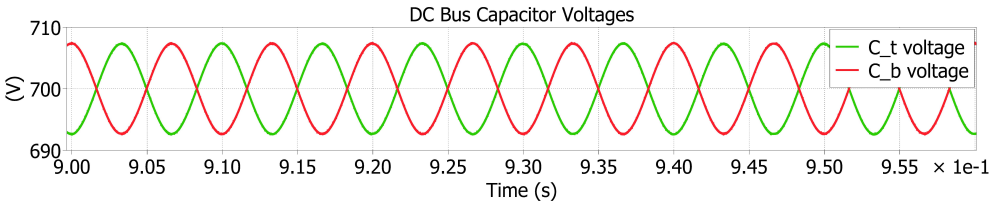
In addition to DC bus imbalance that can occur due to unbalanced DC loads, the 3-L NPC converter produces a sinusoidal ripple current in i_{np} with a frequency three times the fundamental frequency for most of the typical modulation methods. This ripple current results in a voltage ripple at the third harmonic of the fundamental frequency in the DC bus. The amplitude of the voltage ripple depends on the DC bus capacitance, converter phase current amplitudes and the fundamental frequency. The cause of the third harmonic ripple in the 3-L NPC converter is well understood [45] [46] and results from uneven use of the p-type and n-type small vectors alternating every 60°of the fundamental cycle. For example, it can be seen from Figure 4.4 and the 7-segment sequence shown in Figure 4.6(a) that when the angle of $\bar{V}_{\text{ref}}$ is close to 0°, the dwell time of V_{S2} will be close to zero. If the dwell time of V_{S1} is distributed equally between its two redundancies, the use of the p-type and n-type small vectors will be equal. However, as the angle of $\bar{V}_{\text{ref}}$ approaches 30°, the dwell time of V_{S2} will increase. While $\bar{V}_{\text{ref}}$ lies in Region 1a, only the V_{S2} n-type redundancy will be used, resulting in more small vector dwell time being distributed to n-type small vector redundancies. When $\bar{V}_{\text{ref}}$ transitions to Region 1b and the vector sequence of Figure 4.6(b), only the V_{S1} p-type small vector redundancy will be used, resulting in more small vector dwell time being distributed to p-type small vector redundancies. This inequality in dwell time distribution for p-type and n-type small vector redundancies will continue to alternate at the midpoint of each sector for the remainder of the fundamental cycle, resulting in a third harmonic oscillation in the neutral-point voltage. This same oscillation results for PD SPWM, POD SPWM and all other carrier-based modulation methods that do not inject a zero sequence voltage to compensate for it. Carrier-based SPWM modulation methods have been proposed to eliminate the third harmonic DC bus oscillation by injecting a zero sequence into the reference voltage waveforms [47] [48]. These methods achieve a similar result to the 9-segment symmetric NTV SVM sequence shown in Figure 4.5. This vector sequence ensures equal dwell time distribution to the p-type and n-type small vector redundancies throughout the complete fundamental cycle because it uses all four small vector redundancies in all of Regions 1 and 2, and distributes the dwell time of each small vector equally to its redundancies. Therefore, if $\bar{V}_{\text{ref}}$ lies only in Region 1 ($m_a < 0.577$), 9-segment symmetric NTV SVM will not produce a third harmonic ripple in the DC neutral-point voltage.

The carrier-based SPWM method with zero sequence injection to eliminate the third harmonic neutral-point ripple, proposed in [47], is denoted 3rd harmonic ripple elimination (3HRE) SPWM in this work. The neutral-point ripple simulation results for PD SPWM, POD SPWM, M^{2}ZV SVM, SPCMB SVM, 3HRE SPWM and 9-segment NTV SVM are shown in Figure 4.7. The simulation parameters and setup are the same as in Chapter 3. However, instead of ideal voltage sources, the DC bus is formed by two series capacitors, each with capacitance $C_{DC-BUS} = 390$ μF, as specified in Table 3.2. For the results shown in Figure 4.7, the DC grounding capacitor, C_{DC-GND}, is removed and the LCL filter capacitor neutral-point is left disconnected from the DC neutral-point. Therefore, there is no path for I_{cm} to flow.

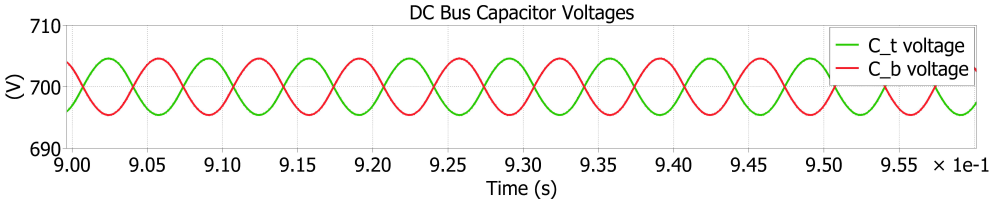
Figure 4.8 shows the neutral-point ripple simulation results with C_{DC-GND} in place and the LCL filter capacitor neutral-point connected to the DC neutral-point. As can be observed, there is a noticeable ripple for 9-segment symmetric NTV SVM which contains a large 150 Hz third harmonic component. This ripple is not caused by unequal distribution of the small state vectors but rather by the large I_{cm} that was observed in Figure 3.17(c). This demonstrates the inherent problem of eliminating both the DC bus voltage ripple and I_{gl} in the NPC converter. To eliminate the DC bus voltage ripple, a third harmonic zero sequence can be injected as in 3HRE SPWM and 9-segment symmetric NTV SVM. However, this zero sequence will result in I_{cm} and I_{gl} when there is a path for them to flow. Furthermore, because these currents flow back to the DC bus neutral-point in the case of a bipolar DC microgrid with capacitive grounding, they will cause neutral-point voltage

ripple themselves.

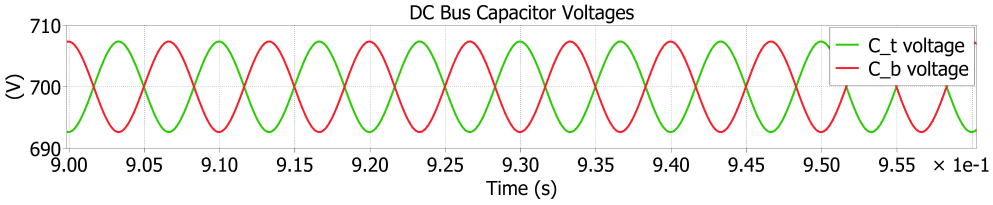
For PD SPWM, POD SPWM, M^{2}ZV SVM and SPCMB SVM, there is not a significant change in DC bus voltage ripple. This is because these modulation methods do not produce a large zero sequence at the third harmonic to begin with. The interaction of the 3HRE SPWM and 9-segment symmetric NTV SVM zero sequence components with the resonances of the common-mode circuit can be observed in the respective voltage ripples in Figure 4.8.



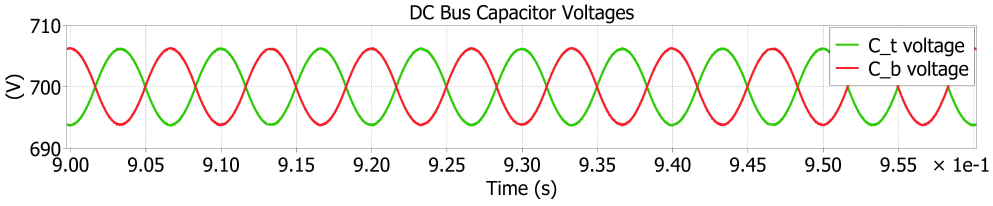
(a) PD SPWM



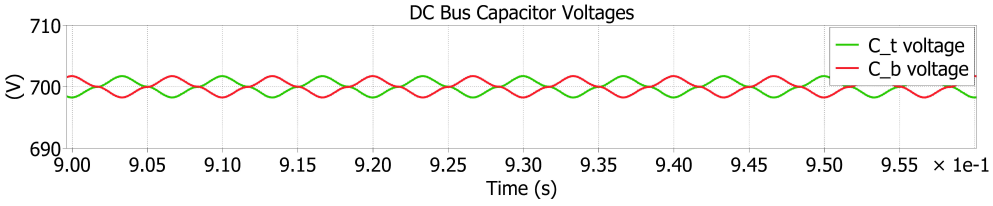
(b) POD SPWM



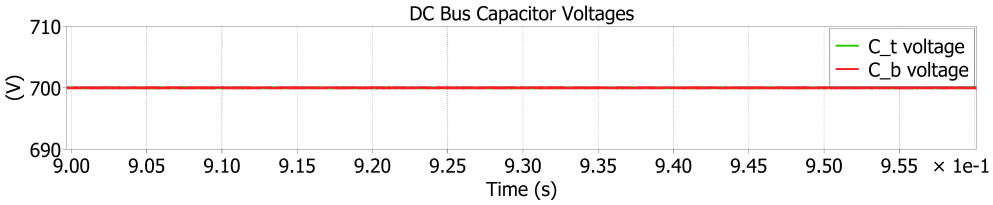
(c) M^{2}ZV SVM



(d) SPCMB SVM

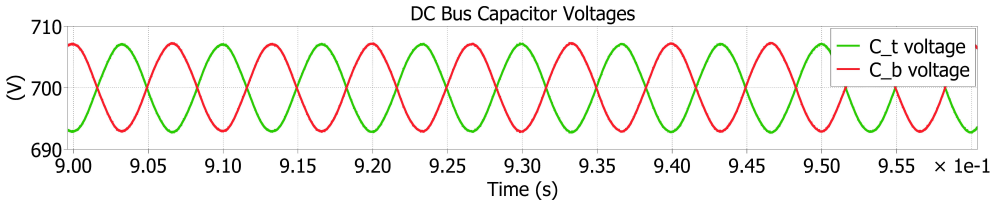


(e) 3HRE SPWM

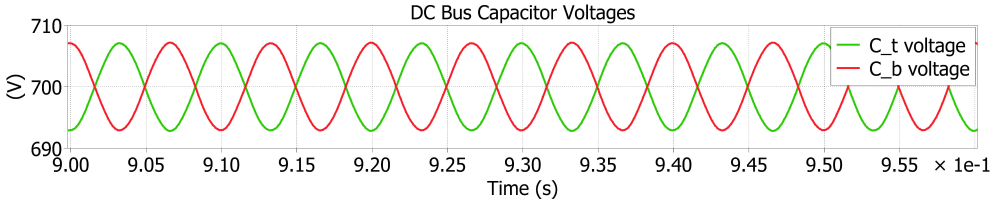


(f) 9-segment symmetric NTV SVM

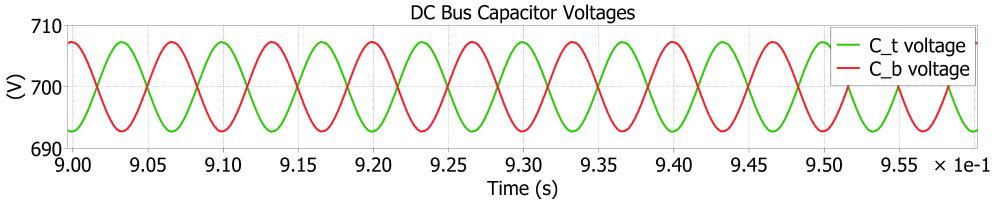
Figure 4.7: DC bus voltage ripple for different modulation methods with no path for I_{cm}



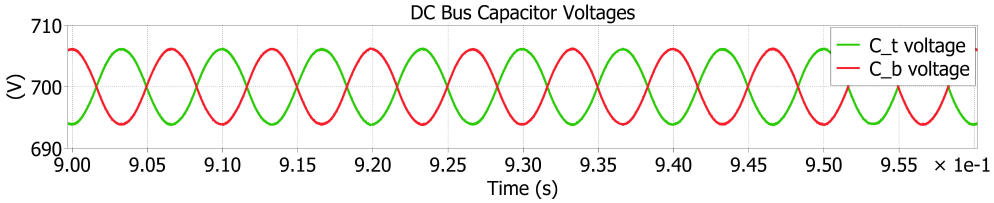
(a) PD SPWM



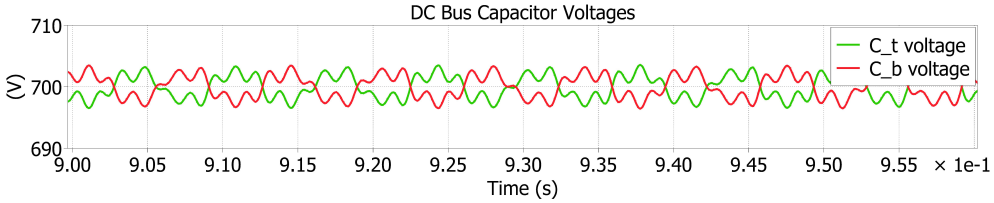
(b) POD SPWM



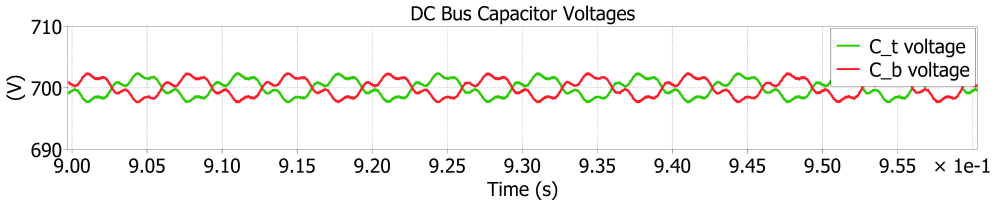
(c) M^2ZV SVM



(d) SPCMB SVM



(e) 3HRE SPWM



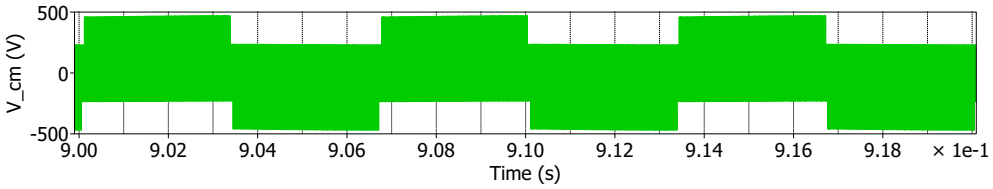
(f) 9-segment symmetric NTV SVM

Figure 4.8: DC bus voltage ripple for different modulation methods with I_{cm} path

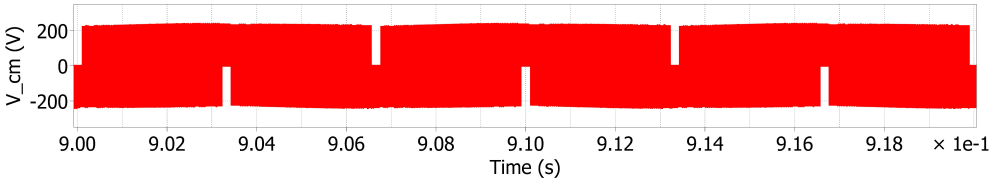
To maximize the reduction of DC bus third harmonic ripple at non-unity PF, the small state vector redundancy distribution can be coordinated with the phase current polarities, as shown in [49]. However, only the unity PF condition is considered in this work for simplicity of analysis and implementation.

The simulated common-mode performance of each modulation method with C_{DC-GND} in place and the LCL filter capacitor neutral-point connected to the DC neutral-point is shown below. The

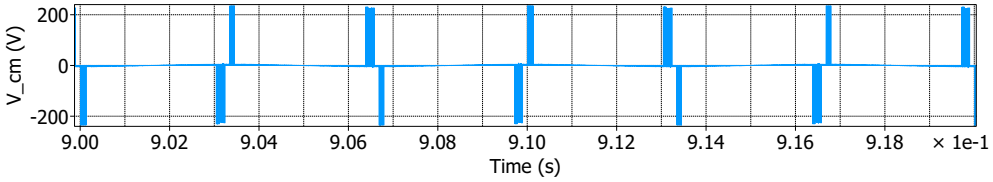
simulated V_{cm}, I_{cm} and I_{gl} for each modulation method are shown in Figures 4.9, 4.10 and 4.11, respectively. The FFTs of the simulated V_{cm}, I_{cm} and I_{gl} in the grid harmonic frequency range are shown in Figures 4.12, 4.13 and 4.14, respectively. The FFTs of the simulated V_{cm}, I_{cm} and I_{gl} at f_{sw} are shown in Figures 4.15, 4.16 and 4.17, respectively.



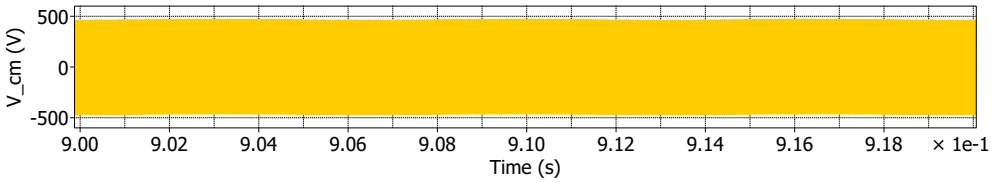
(a) PD SPWM



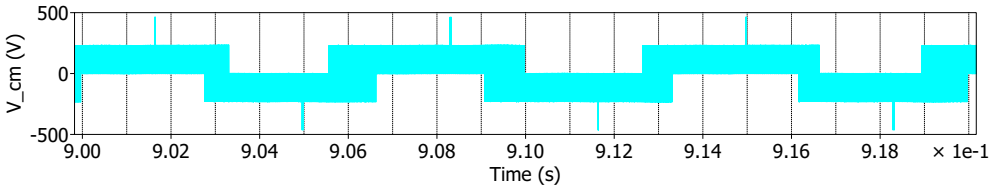
(b) POD SPWM



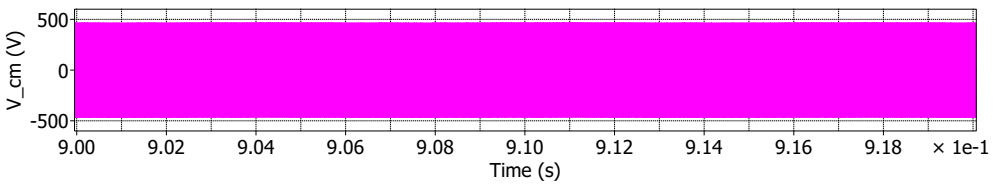
(c) M^{2}ZV SVM



(d) SPCMB SVM

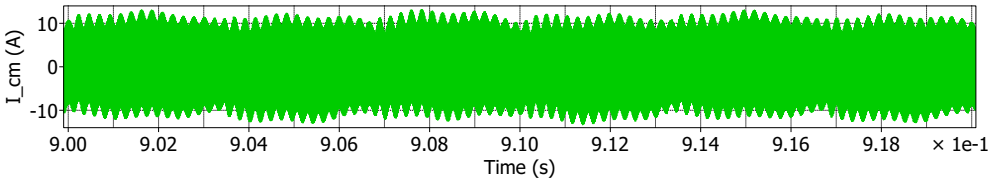


(e) 3HRE SPWM

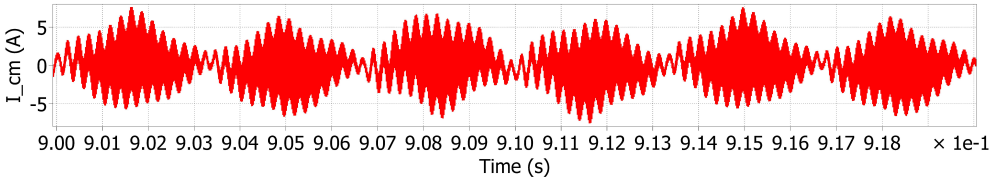


(f) 9-segment symmetric NTV SVM

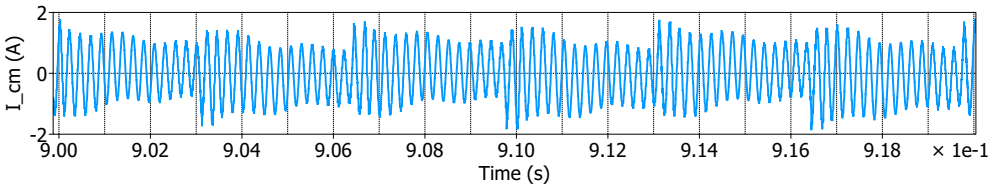
Figure 4.9: V_{cm} simulation results with series capacitors for DC bus



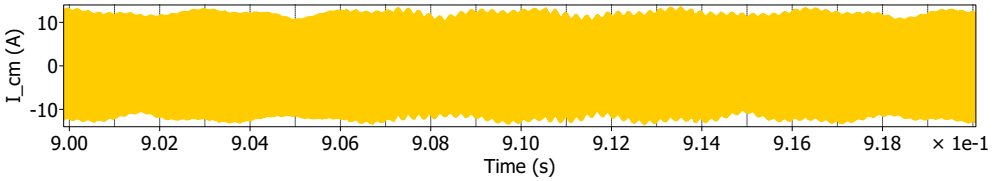
(a) PD SPWM



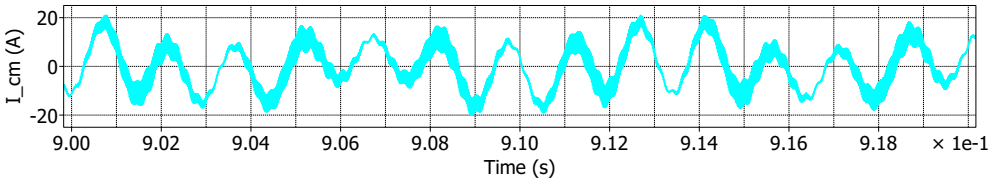
(b) POD SPWM



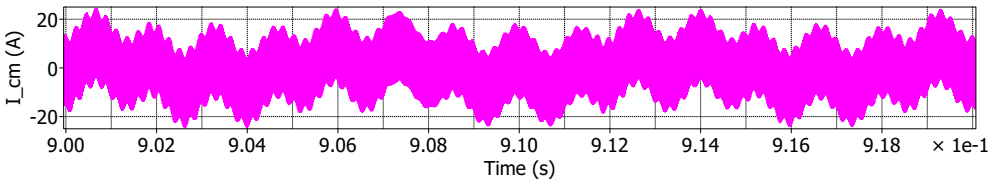
(c) M^2ZV SVM



(d) SPCMB SVM

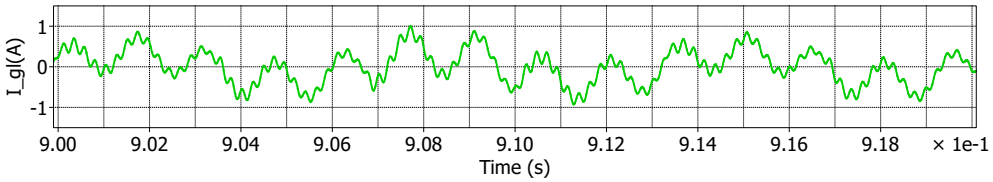


(e) 3HRE SPWM

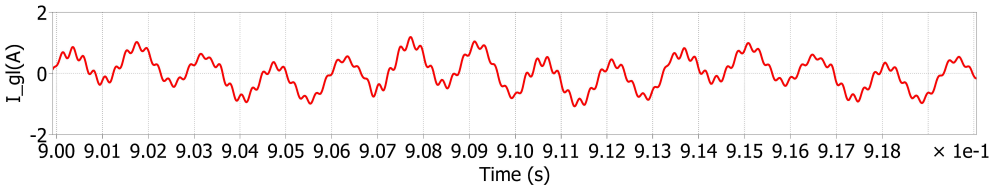


(f) 9-segment symmetric NTV SVM

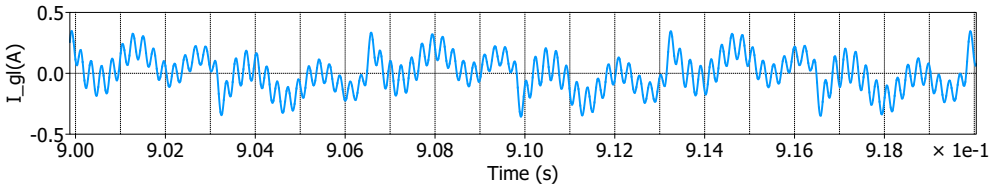
Figure 4.10: I_{cm} simulation results with series capacitors for DC bus



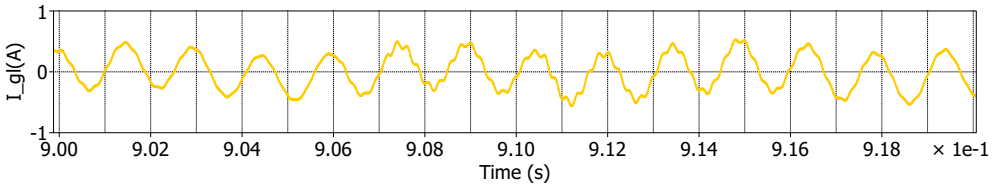
(a) PD SPWM



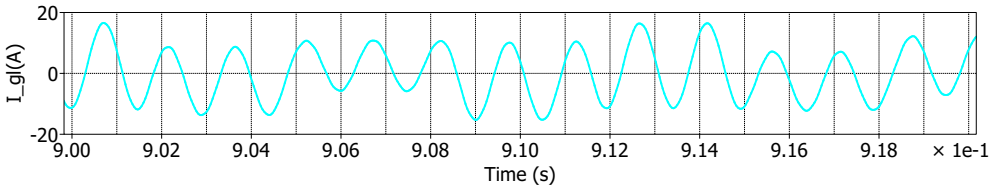
(b) POD SPWM



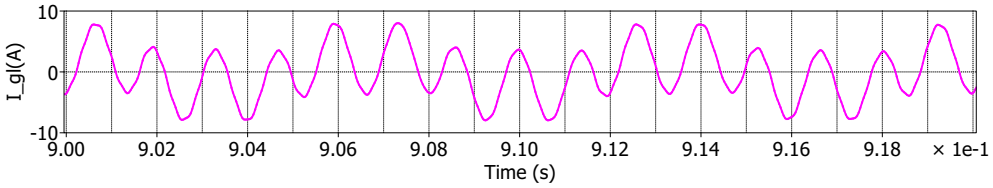
(c) M^2ZV SVM



(d) SPCMB SVM

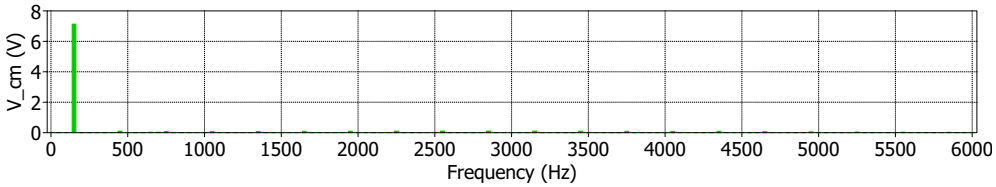


(e) 3HRE SPWM

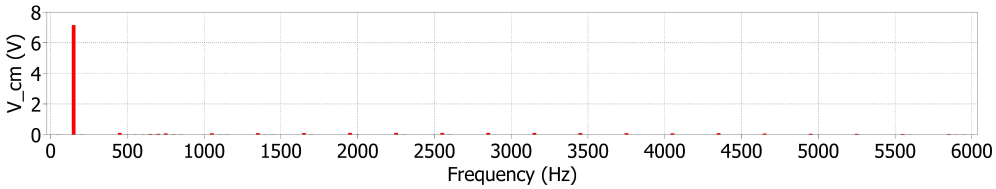


(f) 9-segment symmetric NTV SVM

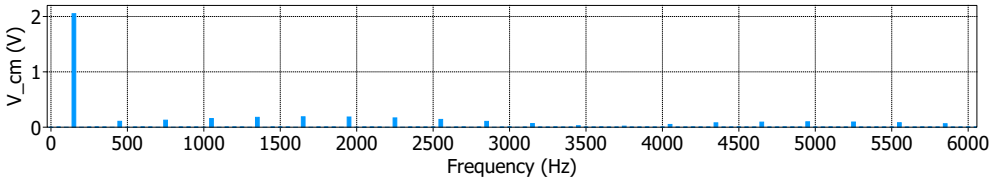
Figure 4.11: I_{gl} simulation results with series capacitors for DC bus



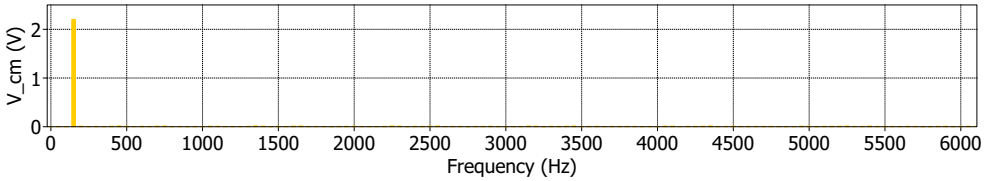
(a) PD SPWM



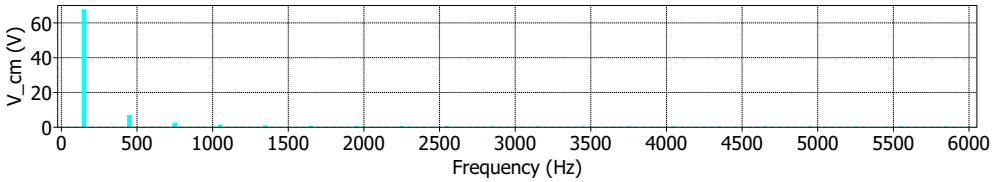
(b) POD SPWM



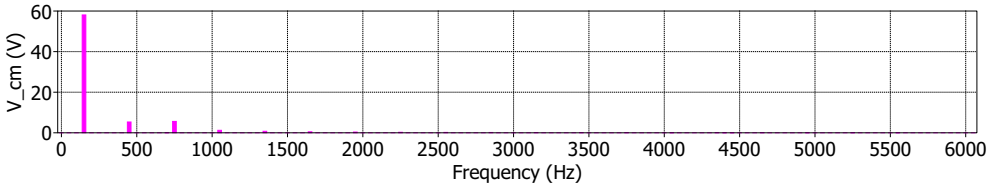
(c) M^{2}ZV SVM



(d) SPCMB SVM

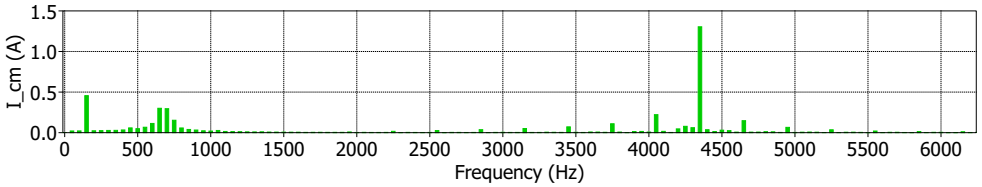


(e) 3HRE SPWM

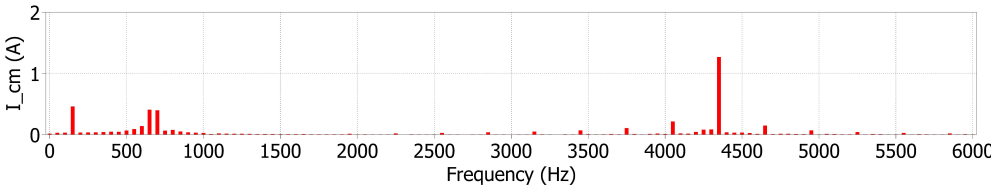


(f) 9-segment symmetric NTV SVM

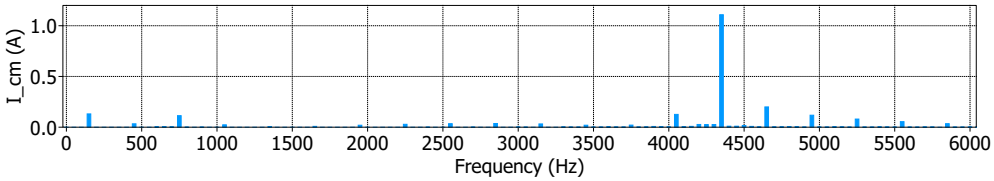
Figure 4.12: V_{cm} grid harmonic range FFT of simulation results with series capacitors for DC bus



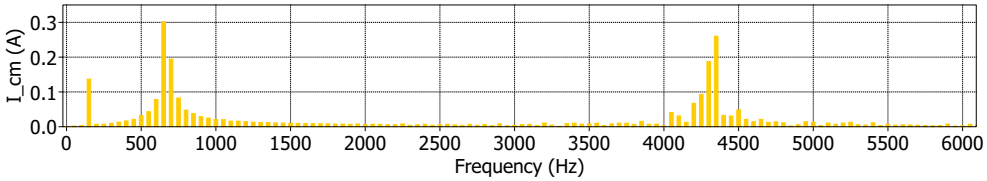
(a) PD SPWM



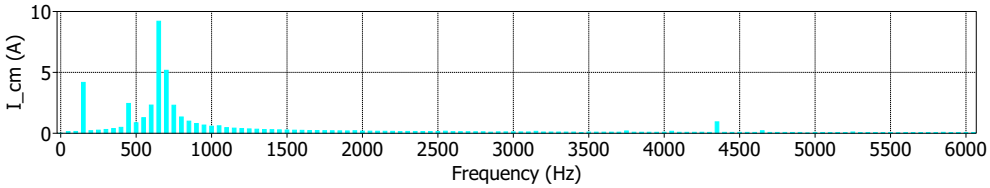
(b) POD SPWM



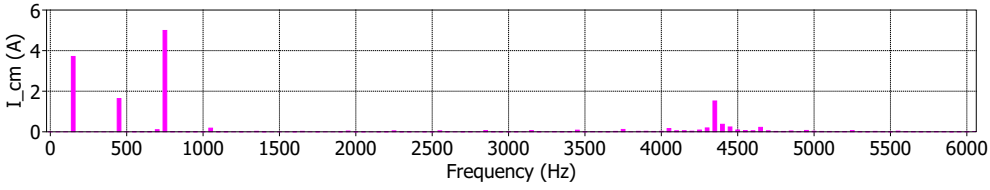
(c) M^{2}ZV SVM



(d) SPCMB SVM

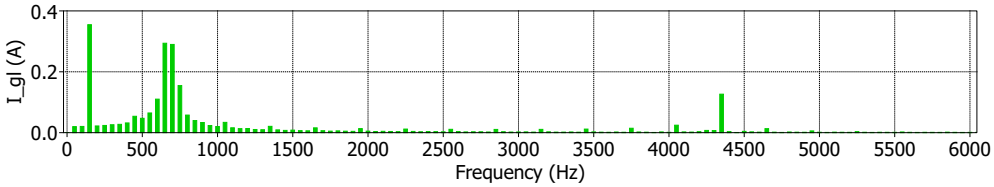


(e) 3HRE SPWM

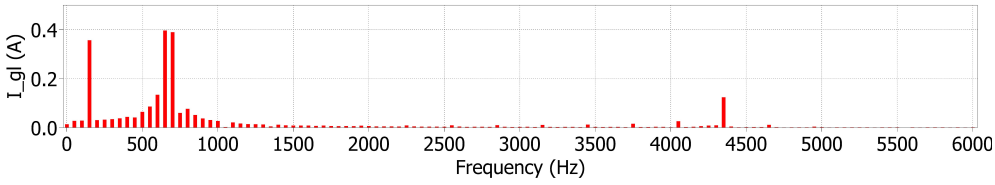


(f) 9-segment symmetric NTV SVM

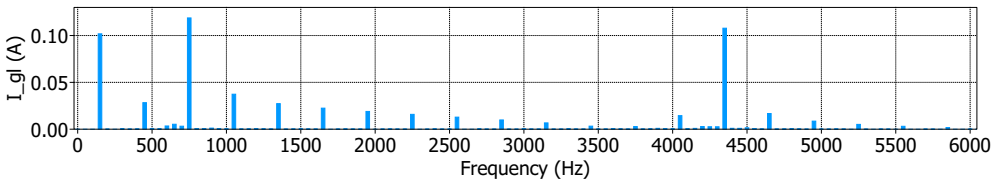
Figure 4.13: I_{cm} grid harmonic range FFT of simulation results with series capacitors for DC bus



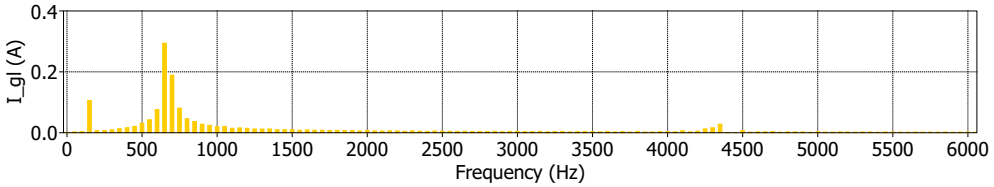
(a) PD SPWM



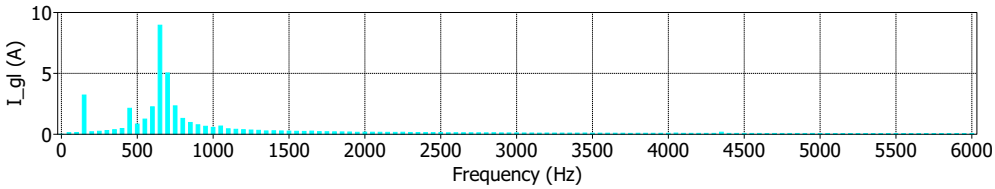
(b) POD SPWM



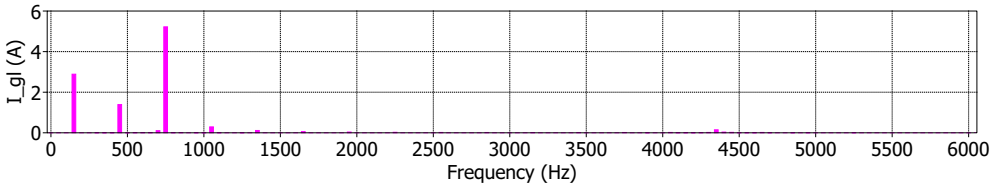
(c) M^2ZV SVM



(d) SPCMB SVM

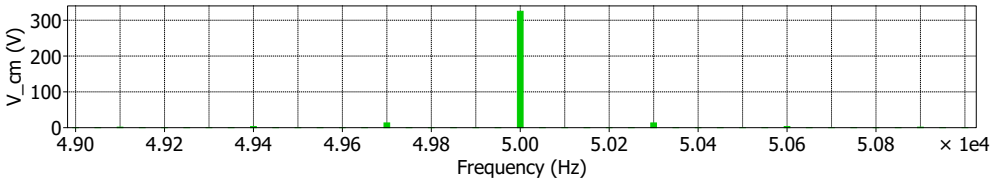


(e) 3HRE SPWM

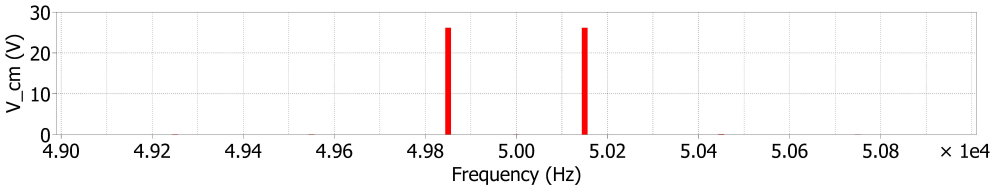


(f) 9-segment symmetric NTV SVM

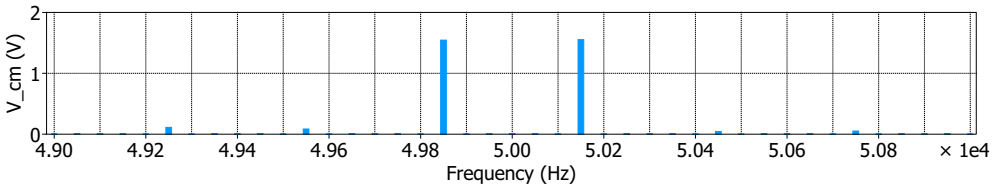
Figure 4.14: I_{gl} grid harmonic range FFT of simulation results with series capacitors for DC bus



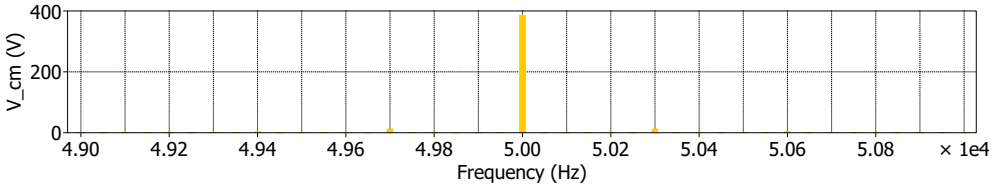
(a) PD SPWM



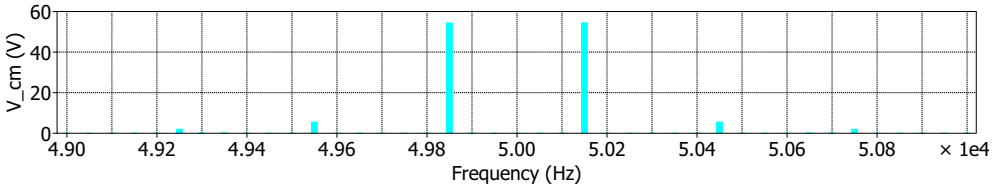
(b) POD SPWM



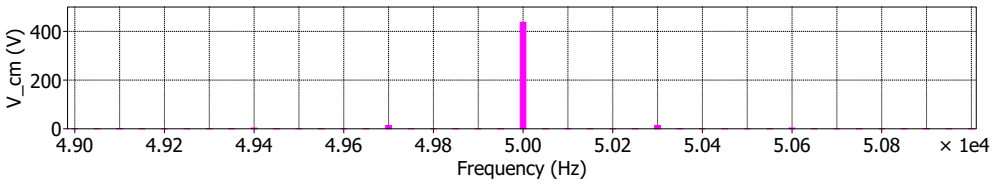
(c) M^{2}ZV SVM



(d) SPCMB SVM

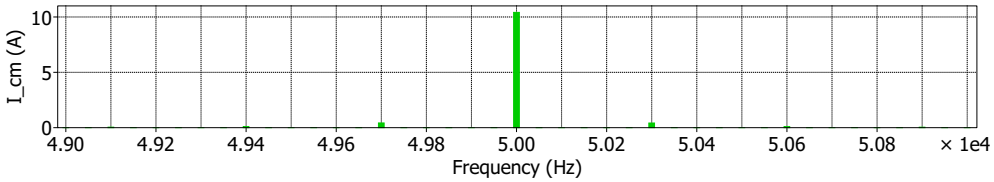


(e) 3HRE SPWM

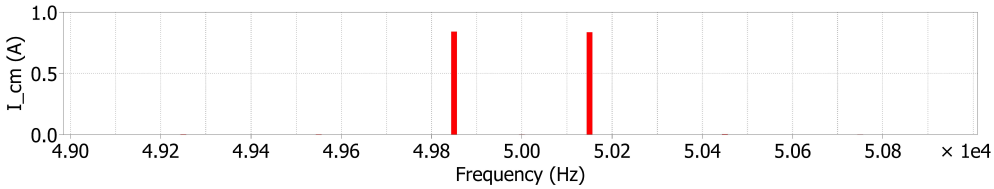


(f) 9-segment symmetric NTV SVM

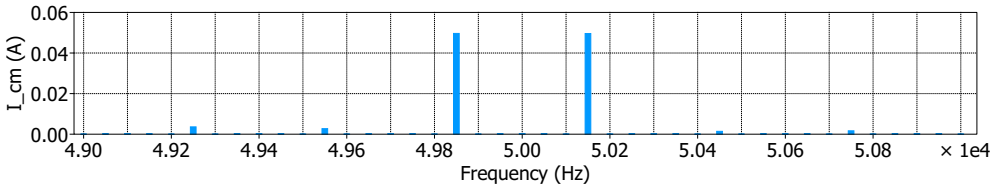
Figure 4.15: V_{cm} f_{sw} FFT of simulation results with series capacitors for DC bus



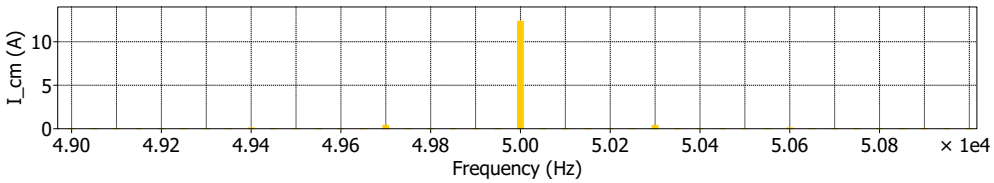
(a) PD SPWM



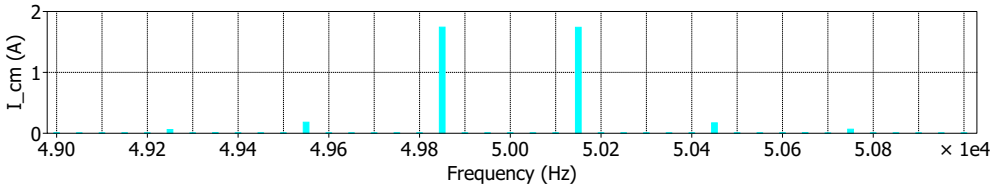
(b) POD SPWM



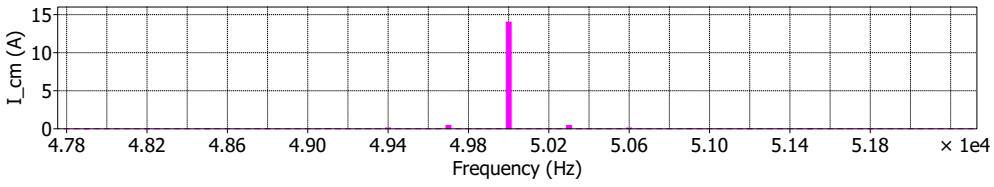
(c) M^2ZV SVM



(d) SPCMB SVM

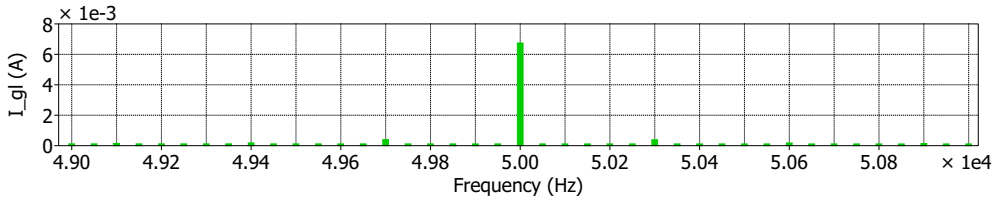


(e) 3HRE SPWM

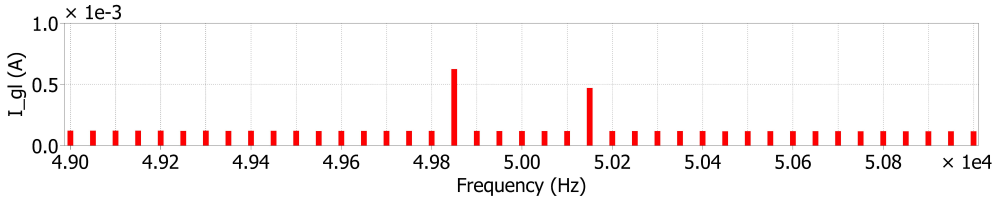


(f) 9-segment symmetric NTV SVM

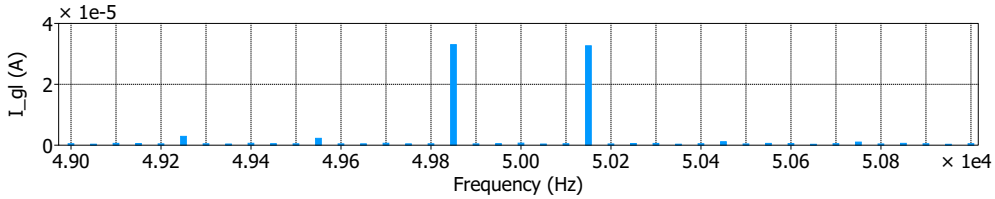
Figure 4.16: I_{cm} f_{sw} FFT of simulation results with series capacitors for DC bus



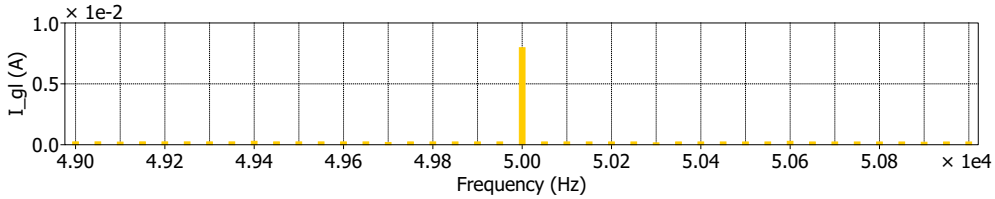
(a) PD SPWM



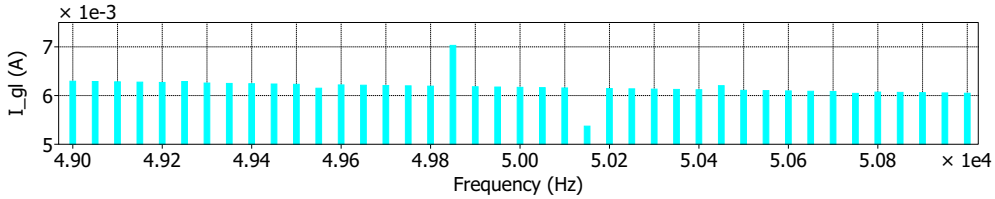
(b) POD SPWM



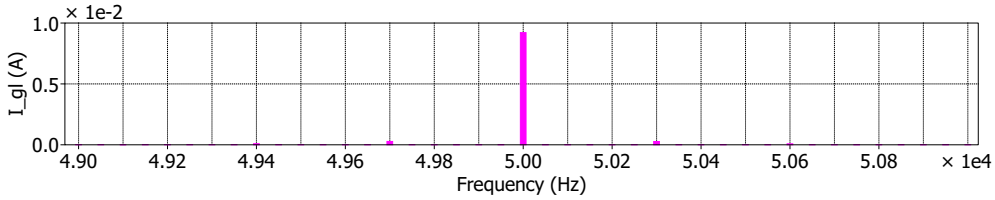
(c) M^{2}ZV SVM



(d) SPCMB SVM



(e) 3HRE SPWM



(f) 9-segment symmetric NTV SVM

Figure 4.17: I_{gl} f_{sw} FFT of simulation results with series capacitors for DC bus

As can be observed in Figure 4.14, I_{gl} for each PWM method now contains frequency components in the grid harmonic range that exceed the RCD tripping threshold limits specified in Table 3.3. Unlike for the simulation results in Chapter 3, the voltage ripple on the non-ideal DC bus produced by PD SPWM, POD SPWM, M^{2}ZV SVM and SPCMB SVM causes them to generate a much larger third harmonic in V_{cm} than they would with an ideal DC bus with no voltage ripple. This can be observed in Figure 4.12. 9-segment symmetric NTV SVM inherently produces a large third harmonic in V_{cm} and the resulting I_{cm} flowing into the DC bus neutral-point causes DC bus ripple. The same result is observable for 3HRE SPWM due to its zero sequence injection.

4.4 DC Bus Voltage Balance Controller

The above results were all obtained with no DC bus load imbalance. In the case of DC bus load imbalance, the small vectors can be redistributed to keep the DC bus voltage balanced. This is implemented by measuring the voltage difference between the two DC poles and sending this difference to a proportional integral (PI) controller that generates a DC bus imbalance variable, Δs, as proposed in [43] and shown in Figure 4.18. Δs is used to adjust the small vector redundancy dwell times in the case of SVM or offset the carriers in the case of carrier-based SPWM in order to keep the DC bus voltage balanced. The imbalance controller limits Δs between -1 and 1. These limits correspond to full redistribution of the small state vector dwell time to the p-type or n-type redundancies. At steady-state, Δs is equal to ϵ defined in Equation 4.1, assuming the DC pole voltages are equal.

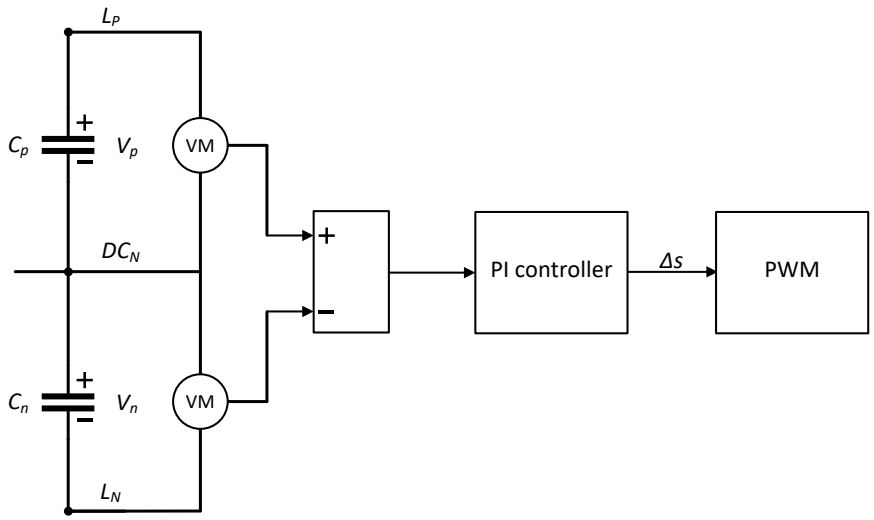


Figure 4.18: DC bus voltage balance controller

For M^{2}ZV SVM, no small vectors are used so this modulation method cannot provide active DC bus voltage balancing. For SPCMB SVM, the redistribution of the small vector dwell times means that V_{cm} cannot be balanced over T_{sw} and the condition of Equation 3.8 will not be achieved. 9-segment NTV SVM and 3HRE SPWM produce a large third harmonic zero sequence in V_{cm} so they are not feasible for mitigating I_{gl}. Under balanced conditions, PD SPWM and POD SPWM produce very small components in the grid harmonic range. However, because their carriers are offset to balance the DC bus under unbalanced conditions, these modulation methods produce a third harmonic in V_{cm} similar to 9-segment NTV SVM under unbalanced DC load conditions.

4.5 Simultaneous DC Pole Balancing and Ground Leakage Current Mitigation

There are several proposed 3-L SVM methods to simultaneously achieve DC bus balancing in 3-L converters and reduce/eliminate I_{cm}. In [50], a discontinuous PWM (DPWM) method is proposed that uses phase-shifted carriers to keep the amplitude of V_{cm} limited to $\frac{V_{DC}}{6}$. The DC bus is balanced by switching between the different DPWM schemes but the algorithm for selecting the proper scheme throughout the grid cycle is complex. In [51], the small vectors are realized utilizing virtual space vectors that have no net effect on the neutral-point voltage. By adjusting the small

vector realization between the actual small vectors and their virtual vector realizations, the DC bus can be balanced using only small vectors with $V_{cm} = \pm\frac{V_{dc}}{6}$. A SVM method is proposed in [52] that switches between using large/medium/zero state vectors and large/medium/small state vectors to balance the DC bus while maintaining $V_{cm} = \pm\frac{V_{dc}}{6}$. The magnitude of V_{cm} is reduced in the methods mentioned above but V_{cm} still oscillates between $\frac{V_{dc}}{6}$ and $-\frac{V_{dc}}{6}$ at three times the fundamental frequency which will produce I_{gl}.

A hybrid PWM method is proposed in [53] that switches between M^{2}ZV SVM and DPWM with phase-shifted carriers. When the DC bus voltage is balanced, M^{2}ZV SVM is used and when unbalance occurs, the DPWM method is selected to balance the DC bus. This method is effective in applications where the NPC inverter is fed by a unipolar DC voltage and has its own split DC bus and neutral point. However, in applications such as a bipolar DC microgrid where constant DC load imbalance can occur, the DPWM method is required under unbalanced conditions and V_{cm} will then oscillate between $\frac{V_{dc}}{6}$ and $-\frac{V_{dc}}{6}$, producing I_{gl}.

Another hybrid PWM method is proposed in [54] that uses three different SVM modes to keep V_{cm} constant during each switching period while also being able to balance the DC bus under continuous unbalance. When the DC bus voltage is balanced, M^{2}ZV SVM is used so $V_{cm} = 0$. The second sequence utilizes the p-type small vectors and keeps $V_{cm} = \frac{V_{DC}}{6}$. The third sequence utilizes the n-type small vectors and keeps $V_{cm} = -\frac{V_{DC}}{6}$. The second or third sequence can then be selected to balance the DC bus depending on which DC pole has the larger load. This method is implemented with a hysteresis based algorithm that only switches from M^{2}ZV SVM to one of the other two sequences if the DC bus voltage imbalance exceeds a certain amount. The modulator switches between M^{2}ZV SVM and one of the balancing sequences under constant DC bus imbalance resulting in periodic oscillations in V_{cm} between zero and $\pm\frac{V_{dc}}{6}$. These oscillations will result in I_{gl}. Furthermore, because the methods proposed in [53] and [54] use M^{2}ZV SVM when the DC bus is balanced, there are small grid harmonic range components in V_{cm} due to dead-time and phase current f_{sw} ripple, as was observed in Figure 3.16. In the case of the capacitive grounding in the bipolar DC microgrid, the V_{cm} components close to the common-mode circuit resonances result in large I_{gl} components, as was observed in Figure 3.18.

In order to simultaneously achieve DC bus balancing, DC bus ripple elimination and I_{gl} elimination, the SPCMB SVM method is modified so that the small vector dwell times can be redistributed to their redundancies to balance the DC bus. Then, the common-mode balancing over T_{sw}, defined by Equation 3.8, is achieved by utilizing the redundant p-type (PPP) and n-type (NNN) zero vectors. This is implemented with the state vector sequence shown in Figure 4.19 for Sector I. This state vector sequence was used in [55] to mitigate the effect of minimum pulse-width in gate turn-off thyristor (GTO) NPC inverters. However, in this work, it is used to achieve simultaneous DC bus balancing and I_{gl} elimination, and is denoted redundant zero vector (RZV) SPCMB SVM.

In RZV SPCMB SVM, the zero vector dwell time, T_{ZV}, is redistributed from the neutral zero vector redundancy (000) to the p-type redundancy if the small vector V_{cm} volt-second balance, $SV_{cmv-bal}$, is negative, and to the n-type redundancy if $SV_{cmv-bal}$ is positive. $SV_{cmv-bal}$ is given by Equation 4.2 in terms of the V_{SA}- and V_{SB}-type small vector dwell times of Table 3.5. In Equation 4.2, $SV_{cmv-bal}$ is normalized to $\frac{V_{dc}}{2}$ and the DC bus voltage is assumed to be balanced. Equation 4.3 defines the redistribution of zero vector dwell time to the p-type and n-type zero vector redundancies based on the magnitude and sign of $SV_{cmv-bal}$. Only the p-type or n-type zero vector redundancy is used within each switching period depending on the sign of $SV_{cmv-bal}$. Figure 4.20 shows the Sector I vector sequences for positive and negative $SV_{cmv-bal}$.

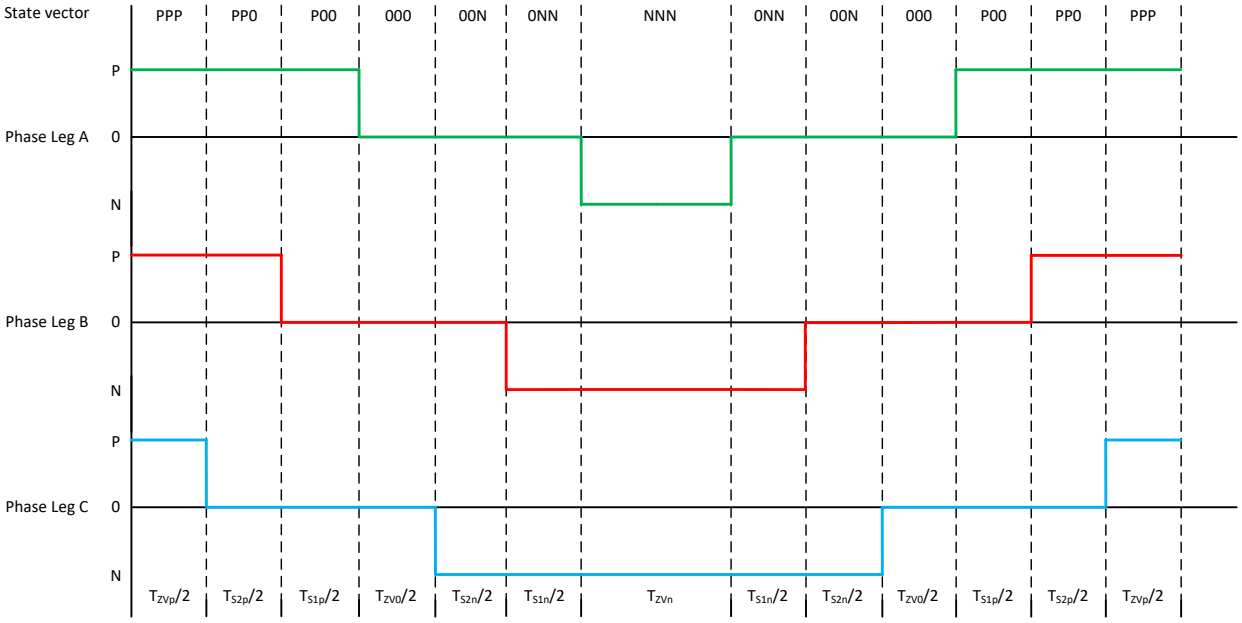
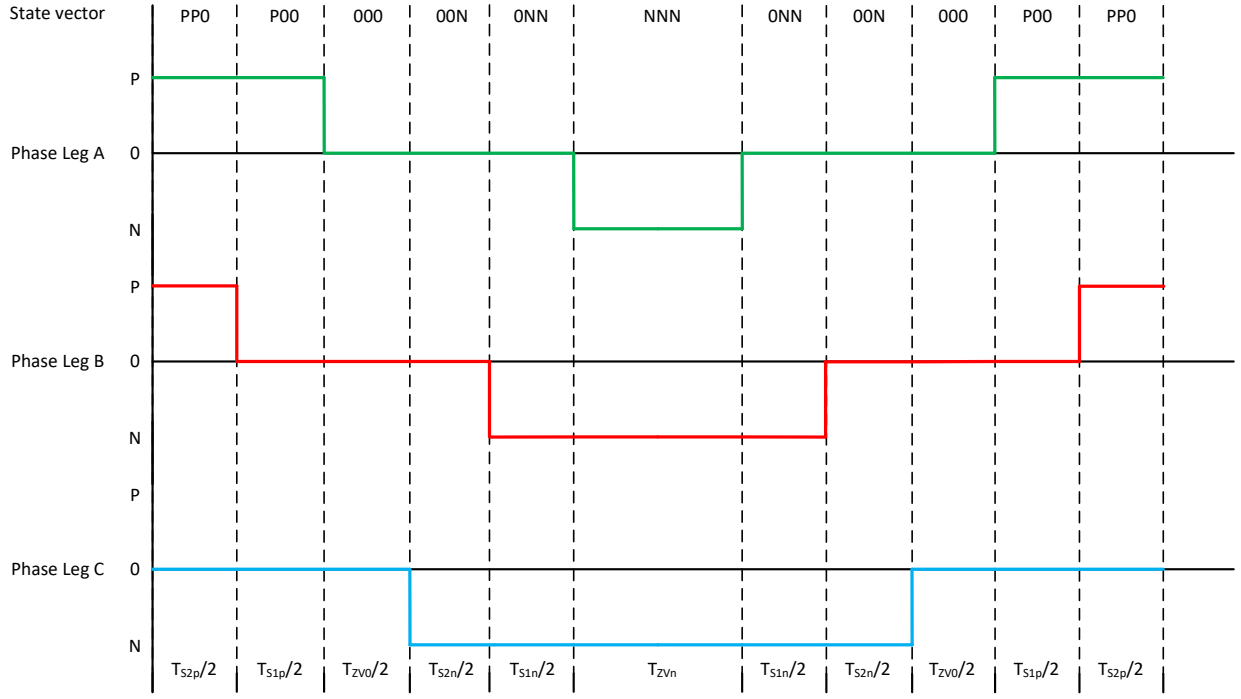


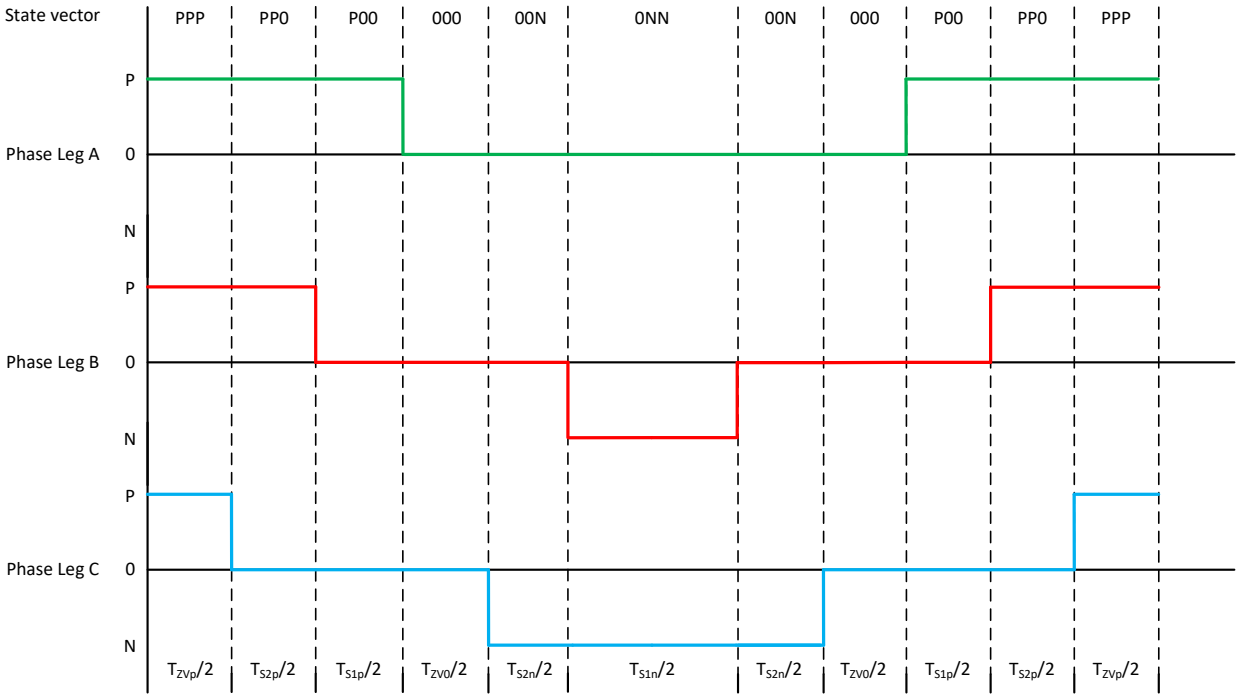
Figure 4.19: 13 segment RZV vector sequence in Sector I

$$SV_{cmv-bal} = \frac{1}{3}T_{SAp} - \frac{1}{6}T_{SAn} + \frac{1}{6}T_{SBp} - \frac{1}{3}T_{SBn} \tag{4.2}$$

$$\begin{cases} \begin{bmatrix} T_{ZVp} = min(2 * |SV_{cmv-bal}|, T_{ZV}) \\ T_{ZVn} = 0 \\ T_{ZV0} = T_{ZV} - T_{ZVp} \end{bmatrix}, & SV_{cmv-bal} < 0 \\ \begin{bmatrix} T_{ZVn} = min(2 * |SV_{cmv-bal}|, T_{ZV}) \\ T_{ZVp} = 0 \\ T_{ZV0} = T_{ZV} - T_{ZVn} \end{bmatrix}, & SV_{cmv-bal} > 0 \\ \begin{bmatrix} T_{ZVn} = 0 \\ T_{ZVp} = 0 \\ T_{ZV0} = T_{ZV} \end{bmatrix}, & SV_{cmv-bal} = 0 \end{cases} \tag{4.3}$$



(a) $SV_{cmv-bal} > 0$

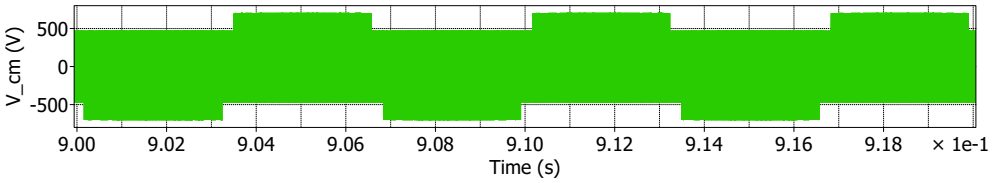


(b) $SV_{cmv-bal} < 0$

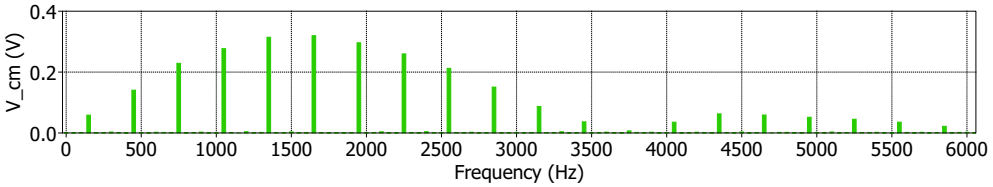
Figure 4.20: RZV SPCMB SVM vector sequences for positive and negative $SV_{cmv-bal}$ in Sector I

The simulation results for RZV SPCMB SVM are shown below. For these simulations, the NPC converter operates in the DC grid forming mode and DC loads are placed on each DC pole. Therefore, the NPC converter draws power from the AC grid as a rectifier to supply the DC loads and regulate the DC pole voltages. The same results can also be obtained for inverter operation. The results for ϵ=0 (no DC imbalance) for V_{cm}, I_{cm} and I_{gl} are shown in Figures 4.21, 4.22 and 4.23, respectively. The results for ϵ=0.35 for V_{cm}, I_{cm} and I_{gl} are shown in Figures 4.24, 4.25 and 4.26, respectively. The simulated DC bus ripples for ϵ=0 and ϵ=0.35 are shown in Figure 4.27. As can

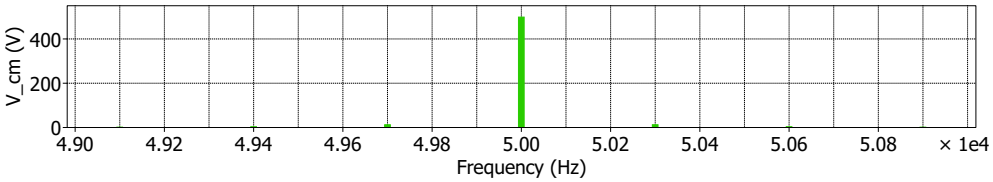
be observed, the frequency components of I_{gl} are under the RCD I_{th} values and the DC bus ripple is virtually eliminated for both ϵ=0 and ϵ=0.35.



(a) V_{cm} over T_{fund}

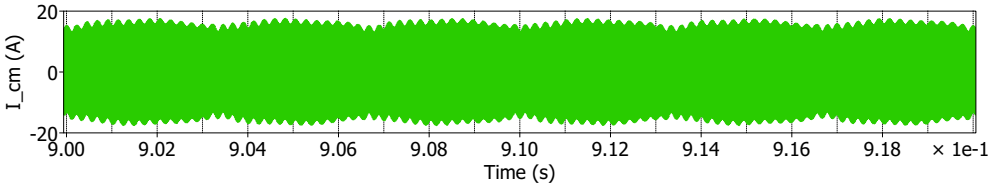


(b) V_{cm} FFT in grid harmonic range

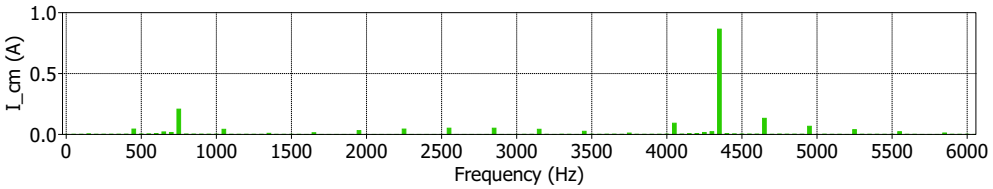


(c) V_{cm} FFT at f_{sw}

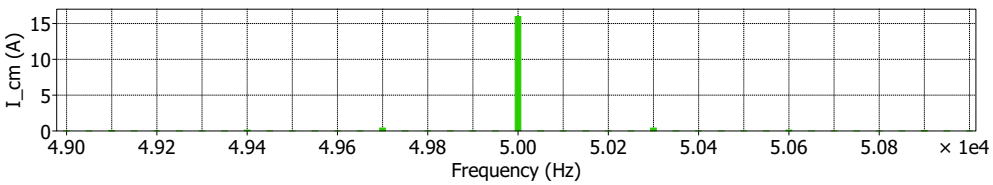
Figure 4.21: V_{cm} simulation results for RZV SPCMB SVM with ϵ=0



(a) I_{cm} over T_{fund}

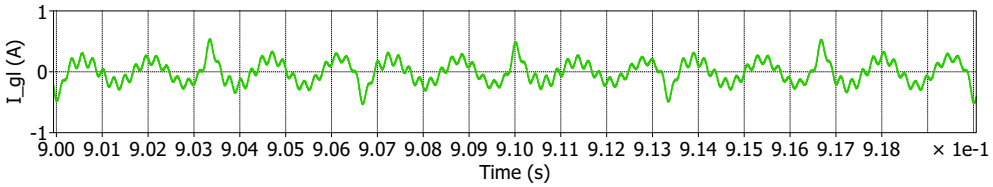


(b) I_{cm} FFT in grid harmonic range

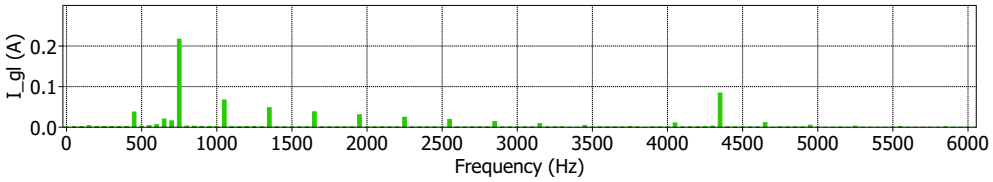


(c) I_{cm} FFT at f_{sw}

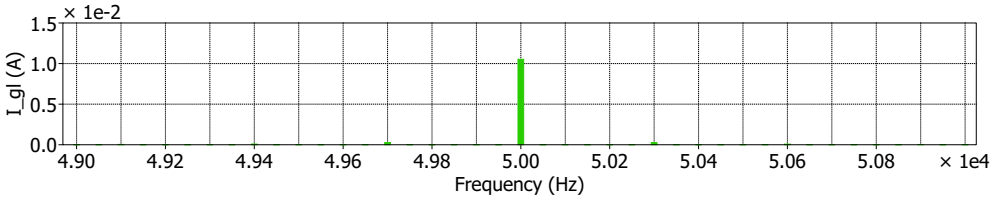
Figure 4.22: I_{cm} simulation results for RZV SPCMB SVM with ϵ=0



(a) I_{gl} over T_{fund}

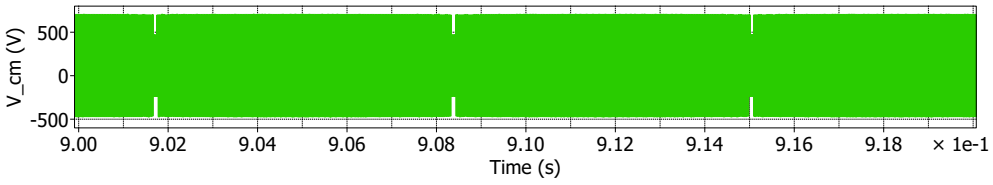


(b) I_{gl} FFT in grid harmonic range

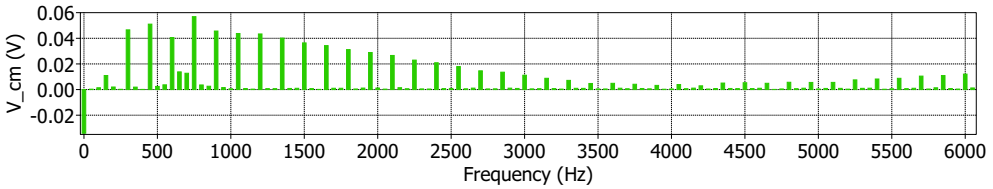


(c) I_{gl} FFT at f_{sw}

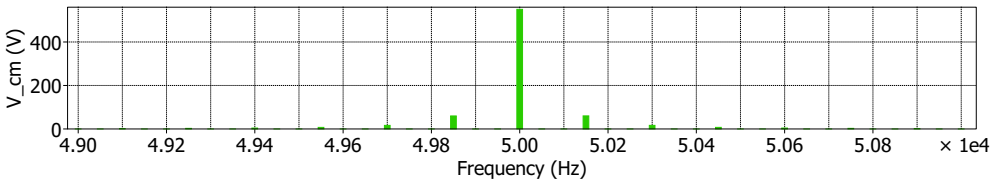
Figure 4.23: I_{gl} simulation results for RZV SPCMB SVM with ϵ=0



(a) V_{cm} over T_{fund}

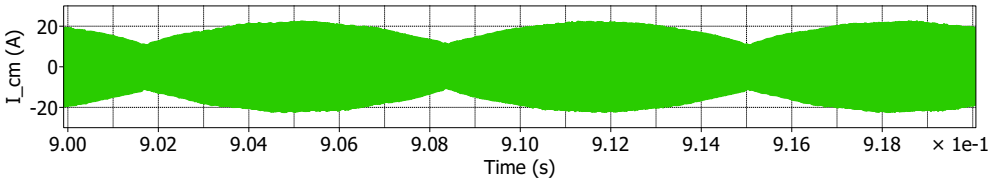


(b) V_{cm} FFT in grid harmonic range

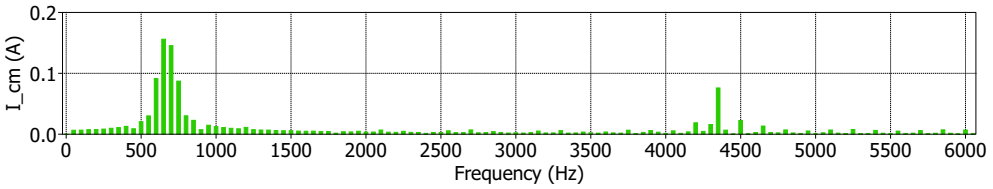


(c) V_{cm} FFT at f_{sw}

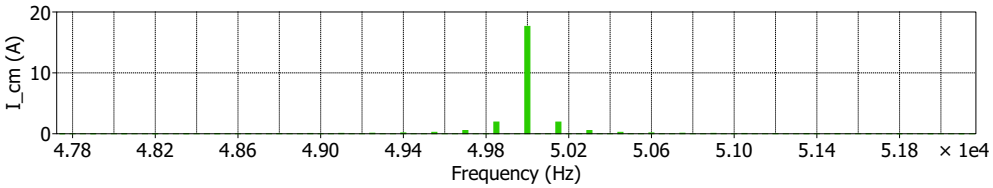
Figure 4.24: V_{cm} simulation results for RZV SPCMB SVM with ϵ=0.35



(a) I_{cm} over T_{fund}

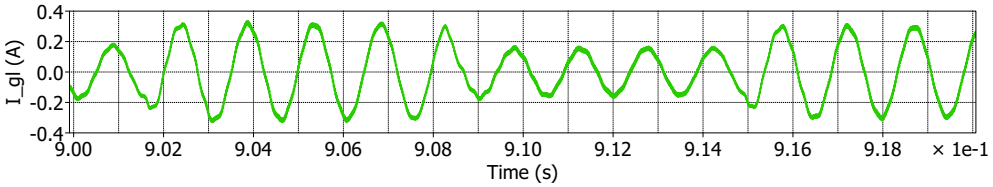


(b) I_{cm} FFT in grid harmonic range

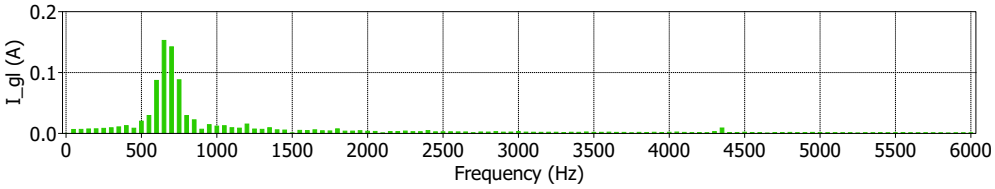


(c) I_{cm} FFT at f_{sw}

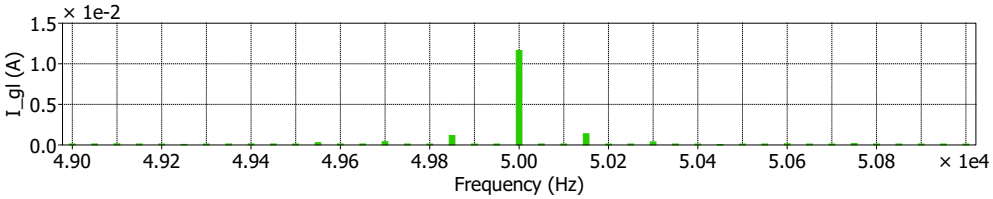
Figure 4.25: I_{cm} simulation results for RZV SPCMB SVM with ϵ=0.35



(a) I_{gl} over T_{fund}

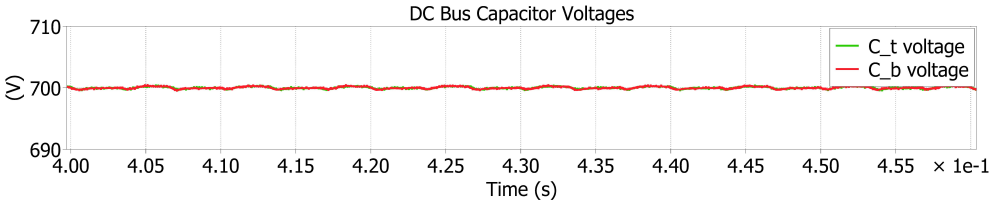


(b) I_{gl} FFT in grid harmonic range

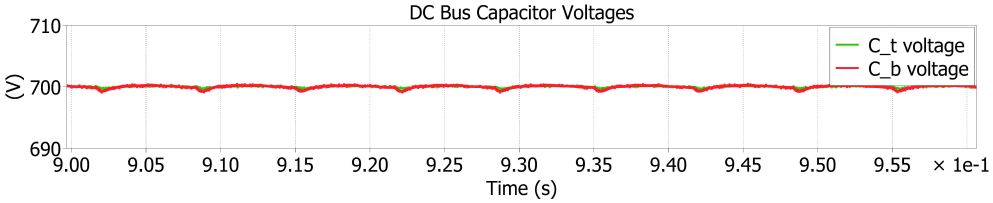


(c) I_{gl} FFT at f_{sw}

Figure 4.26: I_{gl} simulation results for RZV SPCMB SVM with ϵ=0.35



(a) $\epsilon = 0$



(b) $\epsilon = 0.35$

Figure 4.27: RZV SPCMB SVM DC bus ripple simulation results

The main disadvantages of RZV SPCMB SVM are that m_a is limited to values below 0.577 and the higher number of state vector transitions per switching period will result in higher switching loss compared to the other modulation methods analyzed in this work. However, for the DC microgrid application considered in this work, the nominal value of m_a is 0.467 and m_a does not exceed 0.561 over the full voltage ranges of both the LV AC and bipolar DC grids.

For V_{cm} to be balanced over T_{sw} in RZV SPCMB SVM, there must be enough zero vector dwell time to redistribute to the p-type or n-type zero vector redundancy to balance $SV_{cmv-bal}$. As m_a increases, T_{ZV} decreases and the amount of DC imbalance (ϵ) for which V_{cm} can be balanced over T_{sw} for the complete fundamental cycle decreases. This limit on ϵ can be derived from the dwell time and V_{cm} volt-second balance equations, and is given by Equation 4.4 as a function of m_a. The derivation is given in Appendix A. From Equation 4.4, it can be seen that V_{cm} can only be balanced over T_{sw} for $m_a < 0.571$ where ϵ is limited to 0. At this modulation index, RZV SPCMB SVM cannot balance V_{cm} over T_{sw} if there is any DC load imbalance and a third harmonic will appear in V_{cm} for non-zero values of ϵ. This limit applies given that the converter processes the full DC load.

$$\begin{cases} |\epsilon|_{max} = 1, & 0 < m_a < 0.4 \\ |\epsilon|_{max} = \frac{4-7m_a}{3m_a}, & 0.4 < m_a < 0.571 \end{cases} \tag{4.4}$$

A summary of the simulated modulation methods under non-ideal DC bus conditions is given in Table 4.2. As can be observed, each of the modulation methods now produces a 150 Hz I_{gl} component that exceeds the RCD i_{th} value. This is due to the third-harmonic voltage ripple on the DC bus. 9-segment NTV SVM and 3HRE SPWM are not shown because they produce I_{gl} that is far in excess of the RCD tripping threshold limit.

Table 4.2: I_{gl} Performance Under Non-Ideal DC Bus Conditions (C_{DC-bus} = 390 μF)

	RCD i_{th}	**PD SPWM**	**POD SPWM**	**M^{2}ZV SVM**	**SPCMB SVM**
150 Hz	57 mA	355 mA	361 mA	102 mA	106 mA
650 Hz	309 mA	294 mA	321 mA	5 mA	294 mA
750 Hz	345 mA	49 mA	139 mA	119 mA	81 mA
4.35 kHz	N/A	124 mA	131 mA	108 mA	28 mA
I_{gl} peak	N/A	1.0 A	1.0 A	346 mA	535 mA

A summary of the ground leakage current performance for RZV SPCMB SVM with balanced and unbalanced DC loads is given in Table 4.3. As can be observed, I_{gl} is below the i_{th} limits for both balanced and unbalanced DC loads.

Table 4.3: RZV SPCMB SVM I_{gl} Performance (C_{DC-bus} = 390 μF)

	RCD i_{th}	**RZV SPCMB SVM (ϵ=0)**	**RZV SPCMB SVM (ϵ=0.35)**
150 Hz	57 mA	3 mA	8 mA
650 Hz	309 mA	26 mA	153 mA
750 Hz	345 mA	217 mA	88 mA
4.35 kHz	N/A	83 mA	9 mA
I_{gl} peak	N/A	527 mA	336 mA

4.6 Chapter Summary

In this chapter, an overview of DC load imbalance in the bipolar DC microgrid is given and a survey of 3-L NPC converter modulation methods for actively balancing the DC bus voltages is conducted. Then, an analysis of the characteristic third harmonic DC bus voltage ripple that occurs in the 3-L NPC converters was made. The modulation methods of Chapter 3 are now simulated under non-ideal DC bus conditions where the DC poles are modeled as capacitors. The resulting DC bus voltage ripple resulted in a distinct third harmonic component in the common-mode voltages and caused ground leakage current to exceed the RCD tripping threshold limit at 150 Hz. This made it apparent that, in practice, the DC bus voltage ripple needs to be eliminated in order to keep the ground leakage current below the tripping thresholds. In order to actively balance the DC bus voltages and mitigate ground leakage current, a modulation method is proposed for the 3-L NPC converter that uses the redundant zero vectors to balance the common-mode voltage over a switching period. The small vector dwell-time is distributed equally to the redundancies and adjusted to compensate for DC bus load imbalance. Simulation results show that this method keeps ground leakage current below the RCD tripping threshold limits and eliminates the third harmonic ripple in the DC bus under both balanced and unbalanced DC loads. The limitations of this modulation method are also presented.

Chapter 5: NPC Inverter Hardware Implementation

A hardware prototype NPC inverter was designed and built for testing the modulation methods analyzed and developed in Chapters 3 and 4. The prototype NPC inverter is shown in Figure 5.1. The NPC inverter consists of three power stage printed circuit boards (PCBs) (one per phase) that contain the 3-L NPC half-bridges. 1000 V, 65 mΩ SiC MOSFETs and 1.2 kV SiC Schottky diodes, all in surface mount device (SMD) packages are used for the NPC switches and diodes, respectively.

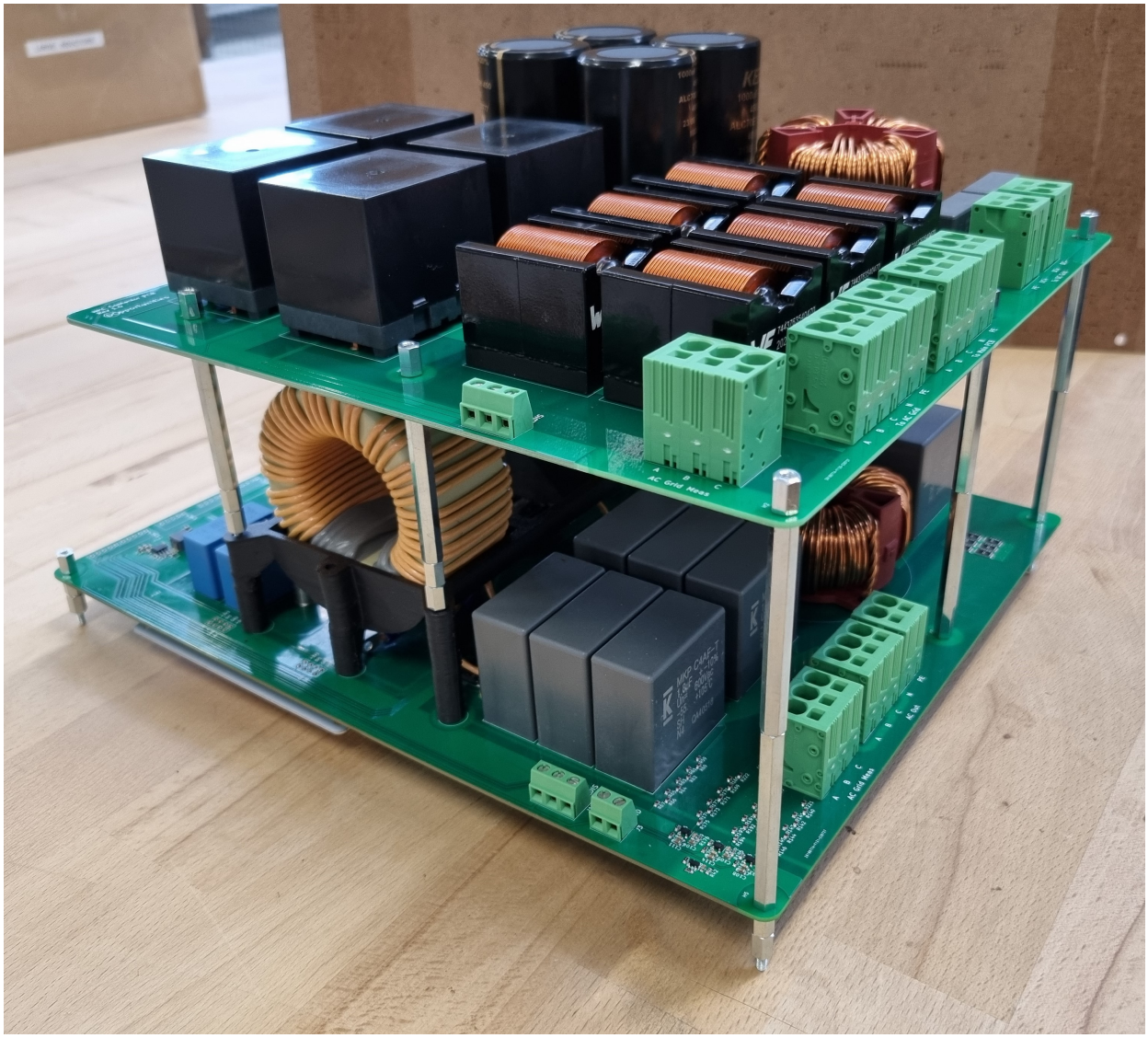


Figure 5.1: 3-L NPC converter hardware prototype

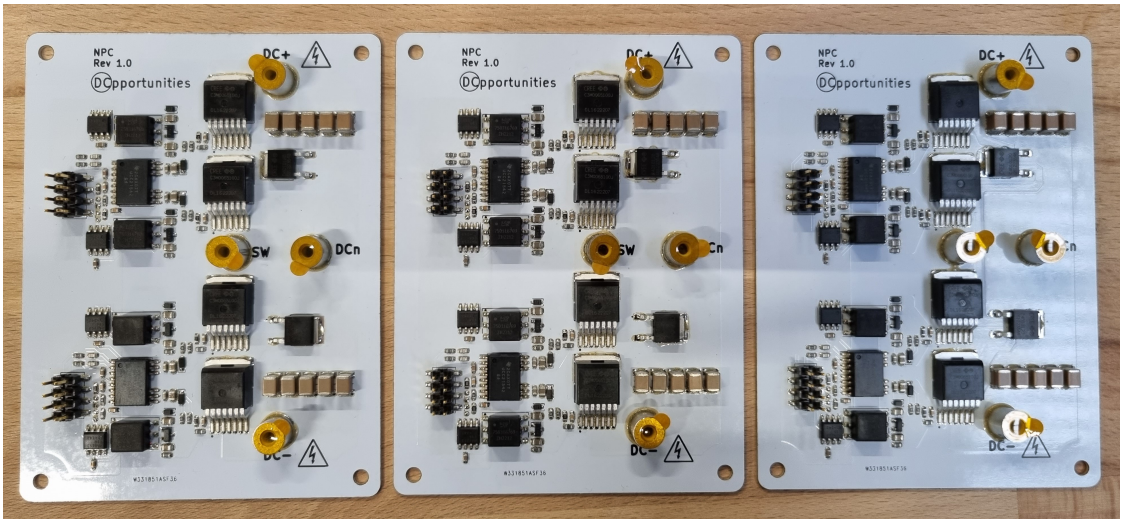


Figure 5.2: NPC power stage aluminum PCBs

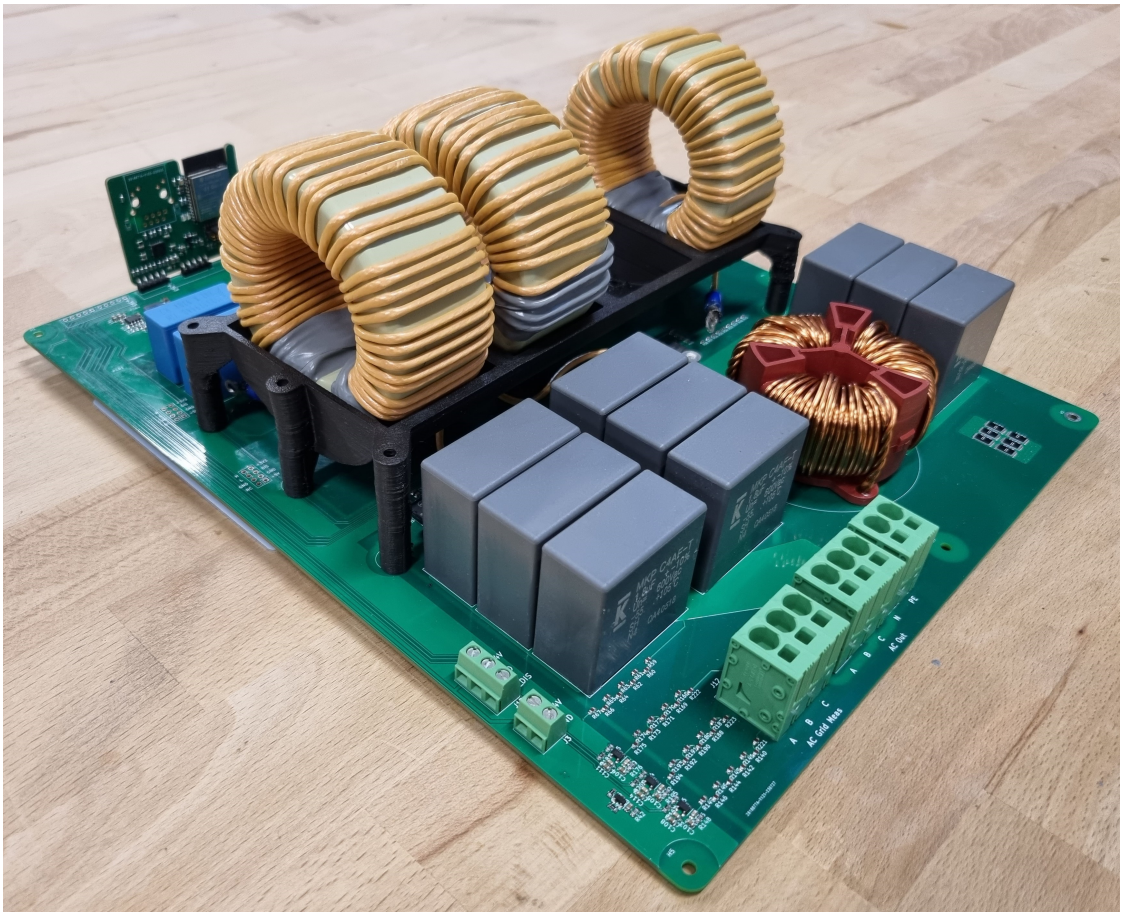


Figure 5.3: NPC main PCB with L1 filter inductors and power stage PCBs

The power stage boards are shown in Figure 5.2. They are implemented on single-layer, aluminum core PCBs for better heat dissipation for the SMD power devices compared to a standard multi-layer FR4 PCB. The power stage PCBs are mounted underneath the main PCB which is shown in Figure 5.3. SMD screw terminals are used for the power connections and header pins for the gate driver control connections. The PCB above the main board in Figure 5.1 contains contactors and passive filter components for when the converter is connected to the AC grid. It was removed for

ease of testing the converter PWM.

5.1 Low-Voltage Testing of PWM

The prototype NPC inverter modulation is implemented on a STM32 microcontroller unit (MCU). The inverter modulation was tested with a small DC bus voltage and no load to verify all the proper connections in the PCB and proper operation of the modulation code. The test setup is shown in Figure 5.4.

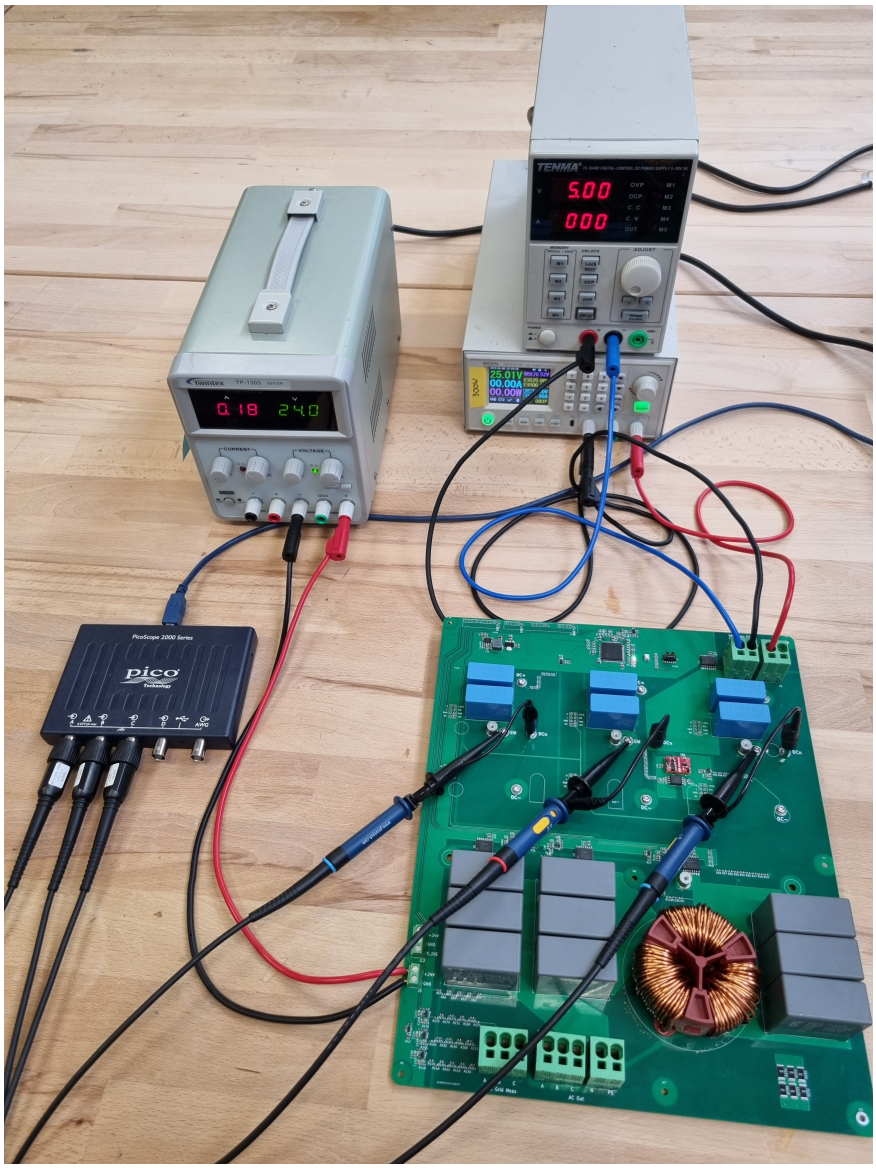
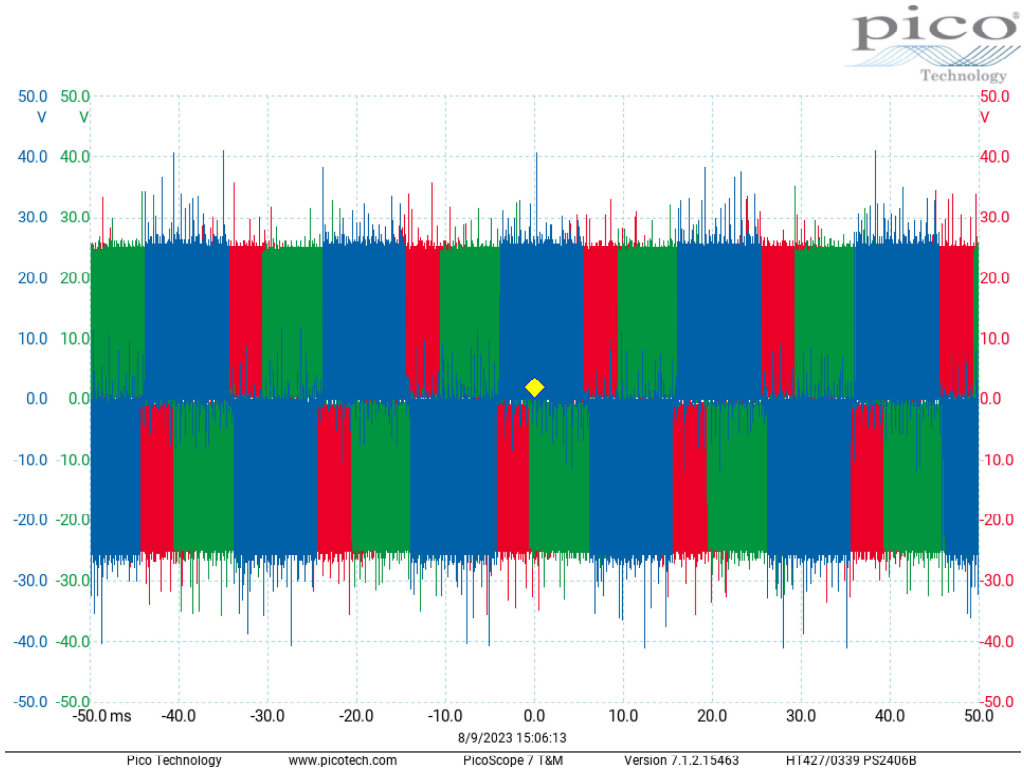


Figure 5.4: Low-voltage test setup of NPC inverter prototype

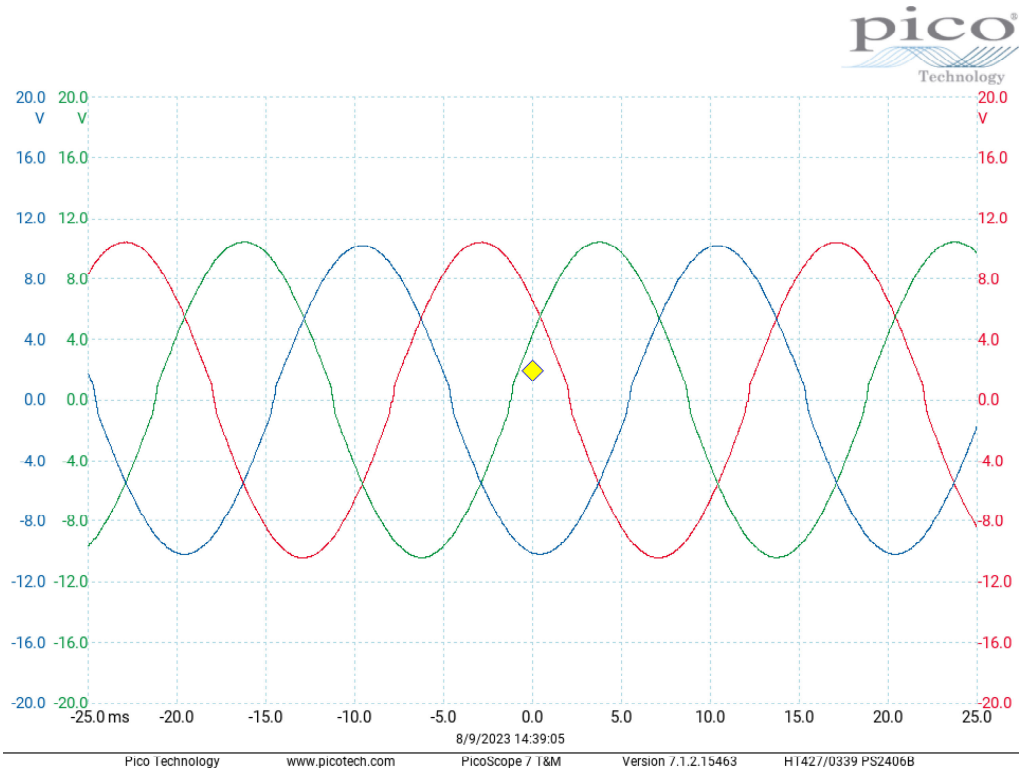
For the LV testing, both PD SPWM and POD SPWM were implemented. The DC bus voltage was set to 50 V (± 25 V) and the modulation index was set to 0.5. f_{sw} and f_{grid} were set to 50 kHz and 50 Hz, respectively. The AC filter was disconnected from the inverter output and the switch node voltages were directly measured with an oscilloscope. The resulting output voltages are shown for PD SPWM and POD SPWM in Figure 5.5. These voltages were then digitally filtered using the oscilloscope's low-pass filter function with the filter cutoff frequency set to 8 kHz. The filtered output voltages are shown in Figure 5.6. Small distortions at the voltage zero crossings due to minimum pulse width can be observed in the filtered output voltages.

(a) PD SPWM

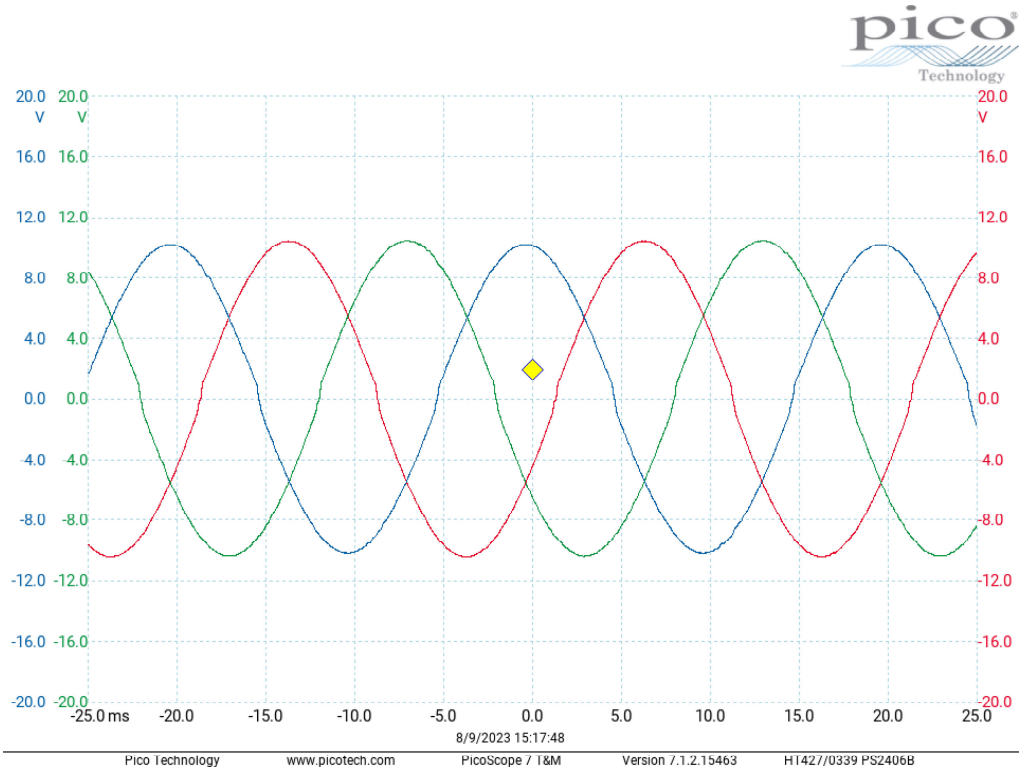


(b) POD SPWM

Figure 5.5: NPC inverter unfiltered switch node voltages in LV test

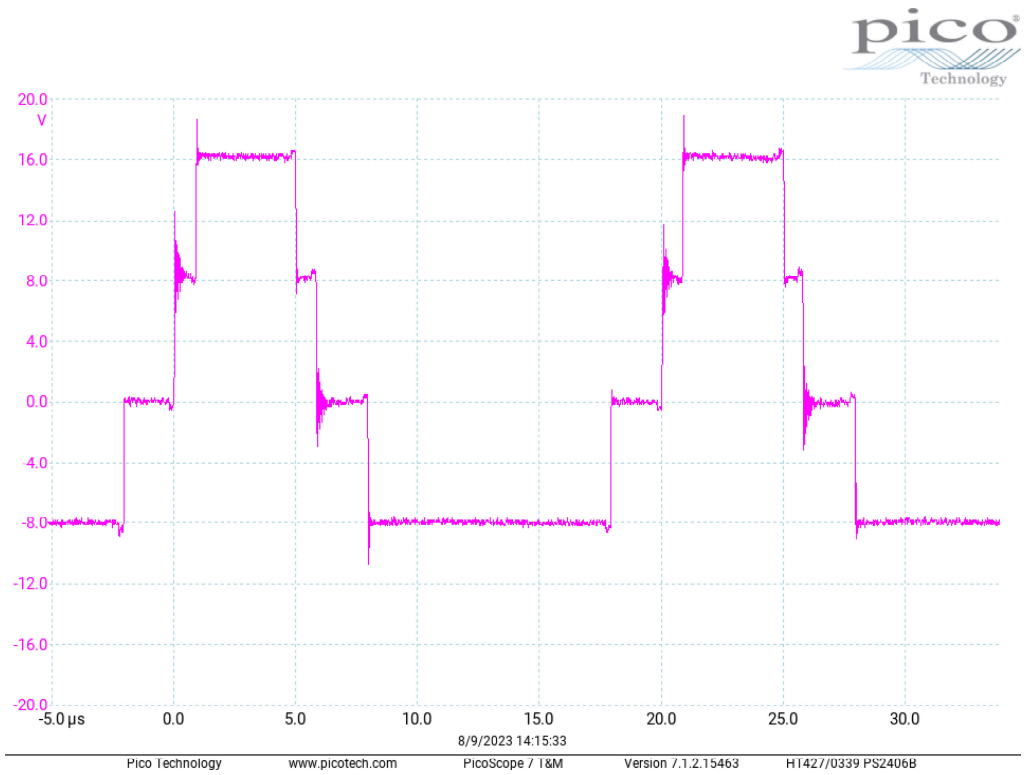


(a) PD SPWM

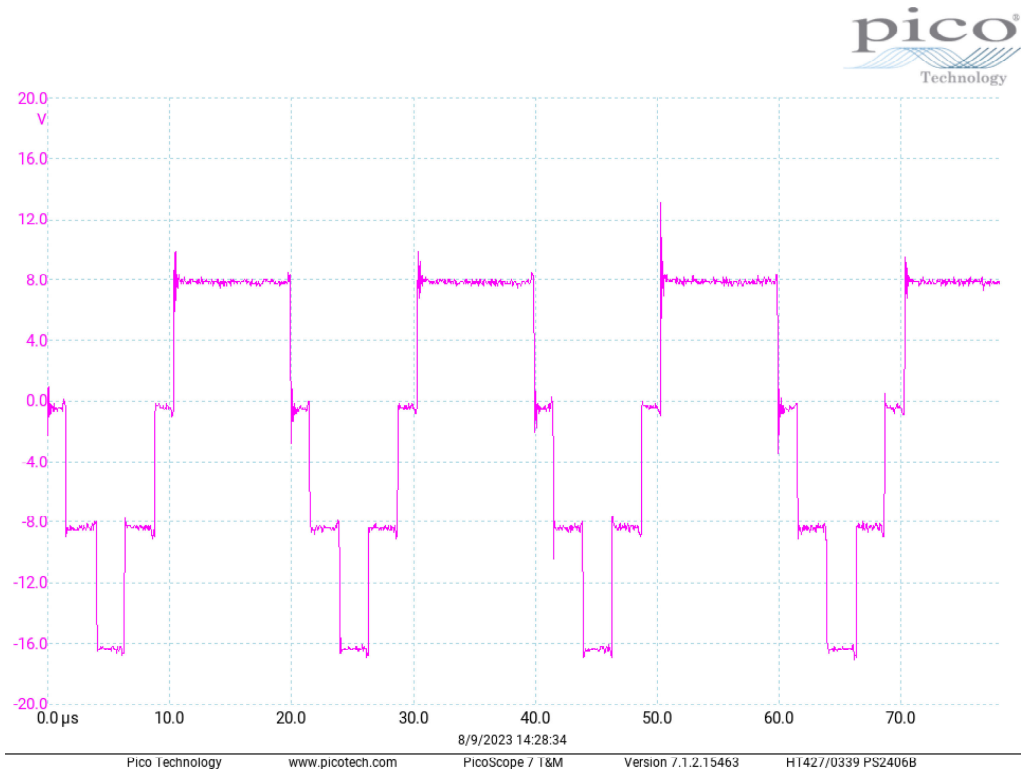


(b) POD SPWM

Figure 5.6: NPC inverter digitally filtered switch node voltages in LV test



(a) Positive half cycle



(b) Negative half cycle

Figure 5.7: PD SPWM V_{cm} in LV test

Next, the oscilloscope math channel was used to measure V_{cm} per Equation 3.2. The time domain V_{cm} plots for PD SPWM and POD SPWM are shown in Figures 5.7 and 5.8, respectively. V_{cm} consists of values of $\pm\frac{V_{dc}}{6}$, $\pm\frac{V_{dc}}{3}$ and zero in PD SPWM but only $\pm\frac{V_{dc}}{6}$ and zero in POD SPWM. For PD SPWM, V_{cm} takes on values from $-\frac{V_{dc}}{6}$ to $\frac{V_{dc}}{3}$ during the positive half cycle of the fundamental sine wave and values from $-\frac{V_{dc}}{3}$ to $\frac{V_{dc}}{6}$ during the negative half cycle as can be observed in Figure 5.7. These measurements are consistent with the simulation results.

The FFTs of V_{cm} in the grid harmonic range and f_{sw} range are shown for PD SPWM and POD SPWM in Figures 5.9 and 5.10, respectively. As can be observed, V_{cm} contains a distinct third harmonic component at 150 Hz for both modulation methods due to the minimum pulse-width distortion at the zero crossings in Figure 5.6. Additionally, V_{cm} contains a large component at f_{sw} and smaller components at its multiples for PD SPWM. For POD SPWM, V_{cm} contains large components at $2f_{sw}$ and $3f_{sw}$, and a smaller component at f_{sw}. These results are consistent with the simulated results, indicating that the modulation methods are working properly. The experimentally measured harmonic components between 1 kHz and 6 kHz are smaller than the 150 Hz component. In the simulations, some of these are larger than the 150 Hz component.

The results indicate that the NPC power stage and modulation operate as expected. The converter can be used in future testing of the V_{cm} performance for the SVM methods presented in Chapters 3 and 4.

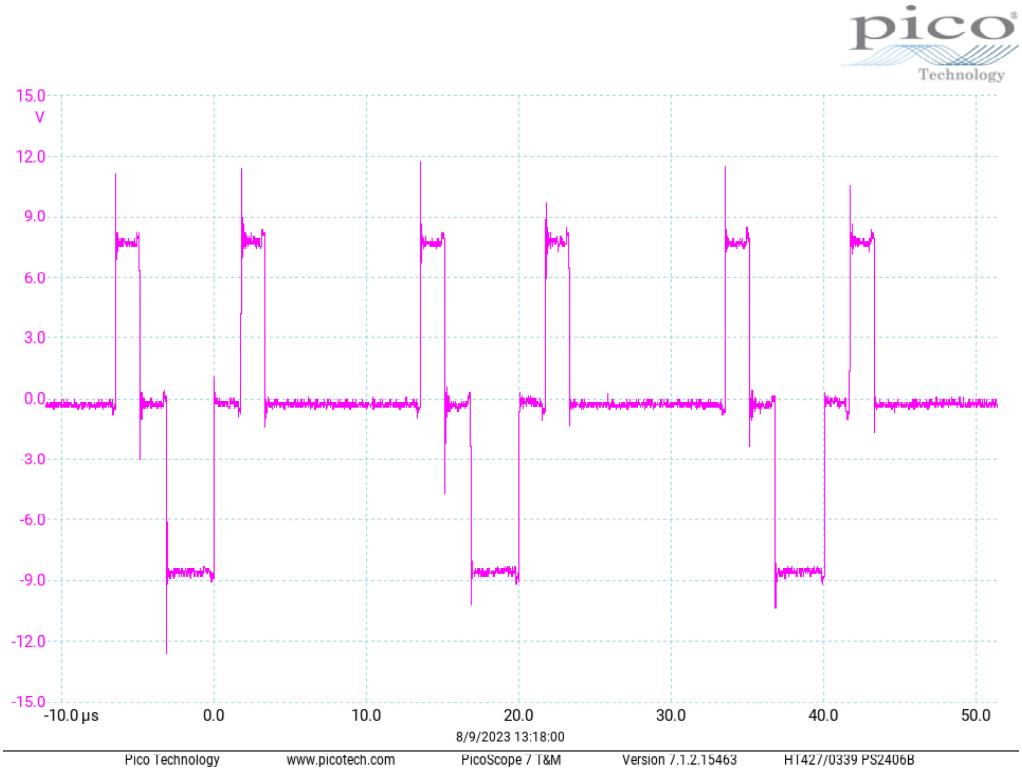
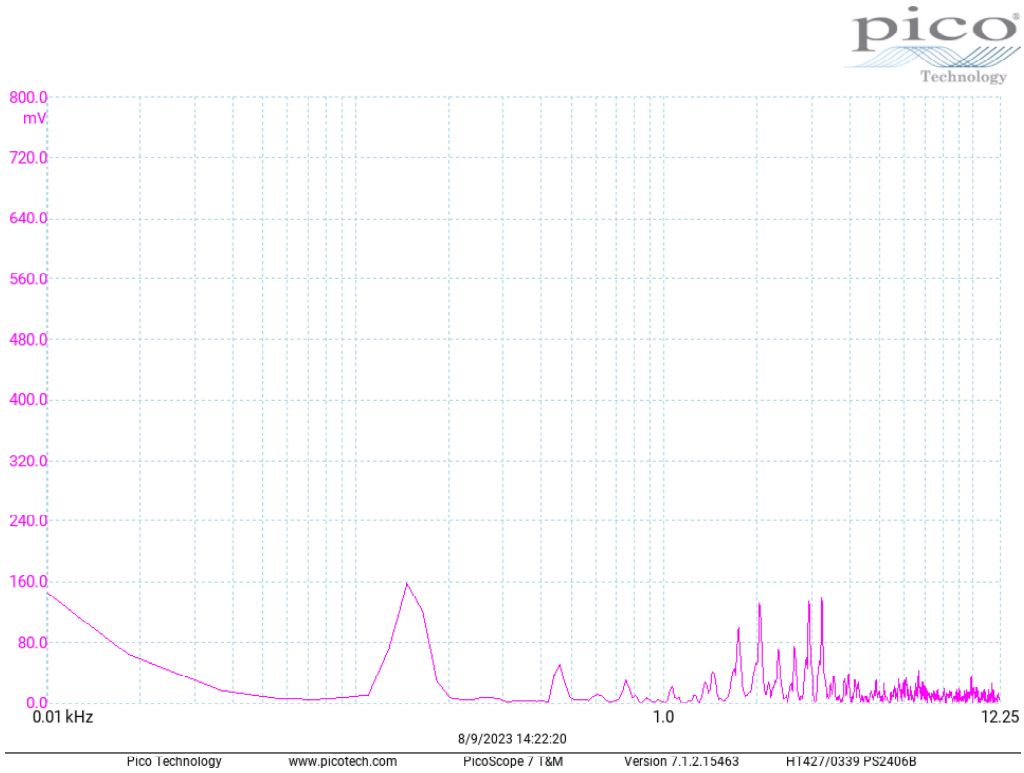
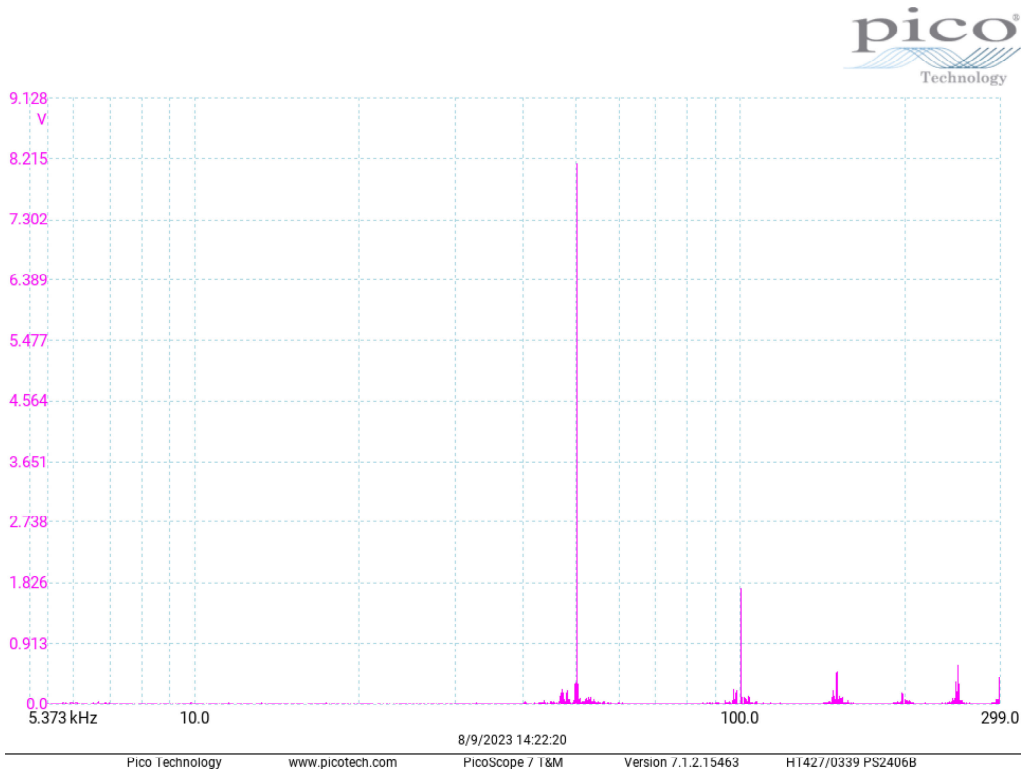


Figure 5.8: POD SPWM V_{cm} in LV test

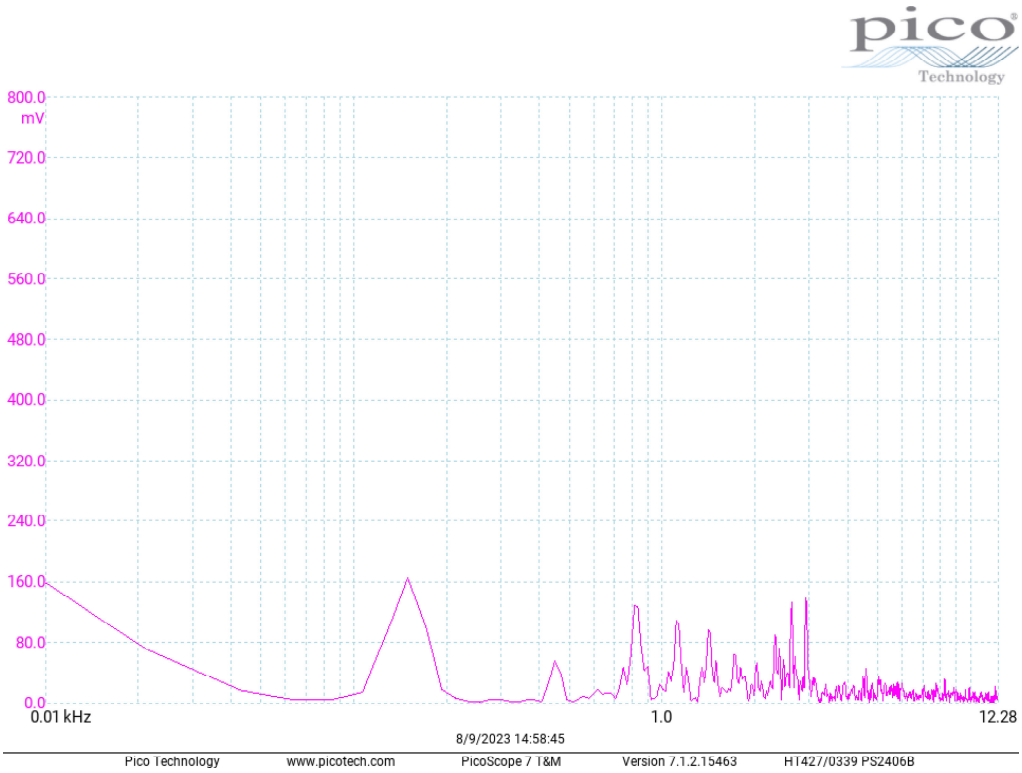


(a) Grid harmonic range FFT

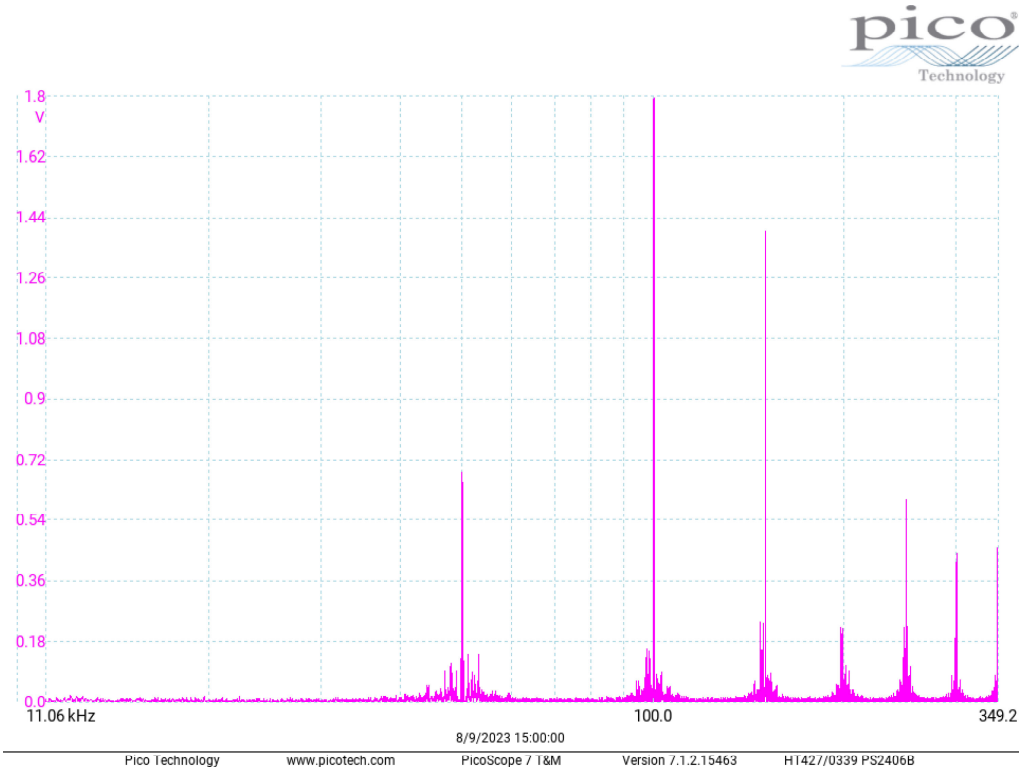


(b) f_{sw} range FFT

Figure 5.9: PD SPWM V_{cm} FFTs



(a) Grid harmonic range FFT

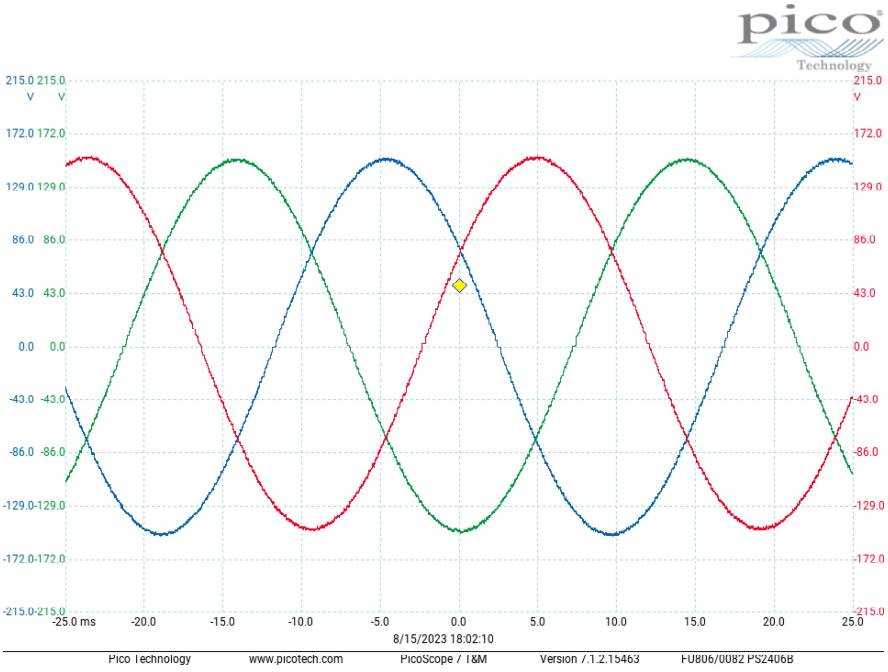


(b) f_{sw} range FFT

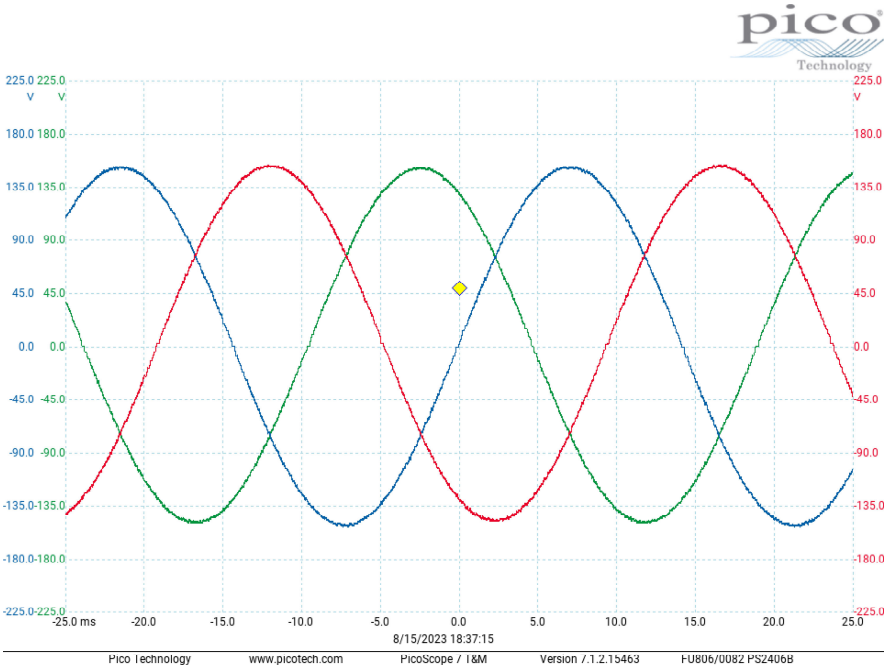
Figure 5.10: POD SPWM V_{cm} FFTs

5.2 PWM Testing with 600 V DC Bus

With the basic operation of the converter power stages verified, the PWM was tested with the same setup as in Section 5.1 but with higher voltage DC power supplies to provide a 600 V DC bus (±300 V). The digitally filtered converter switch node voltages are shown in Figure 5.11.



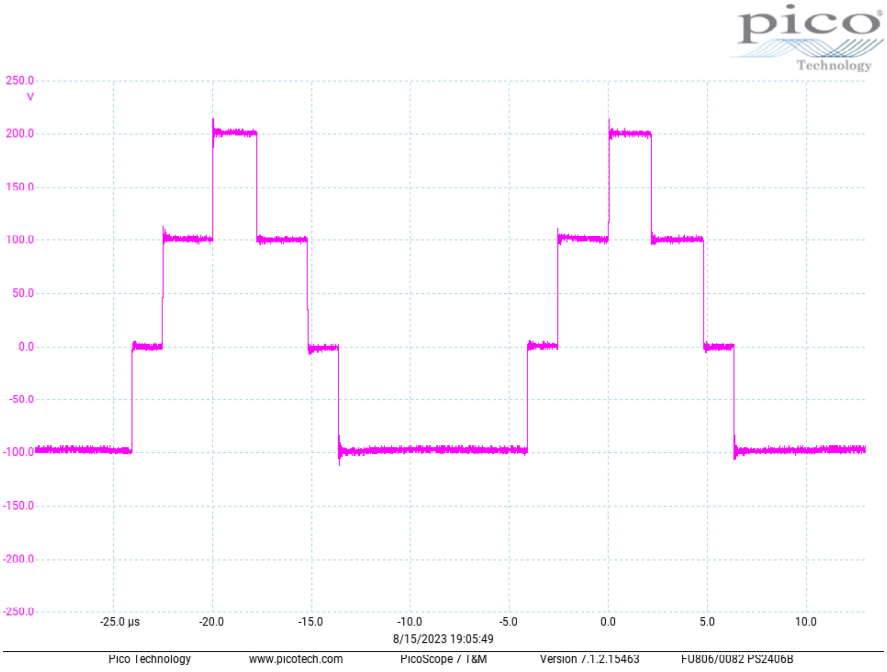
(a) PD SPWM



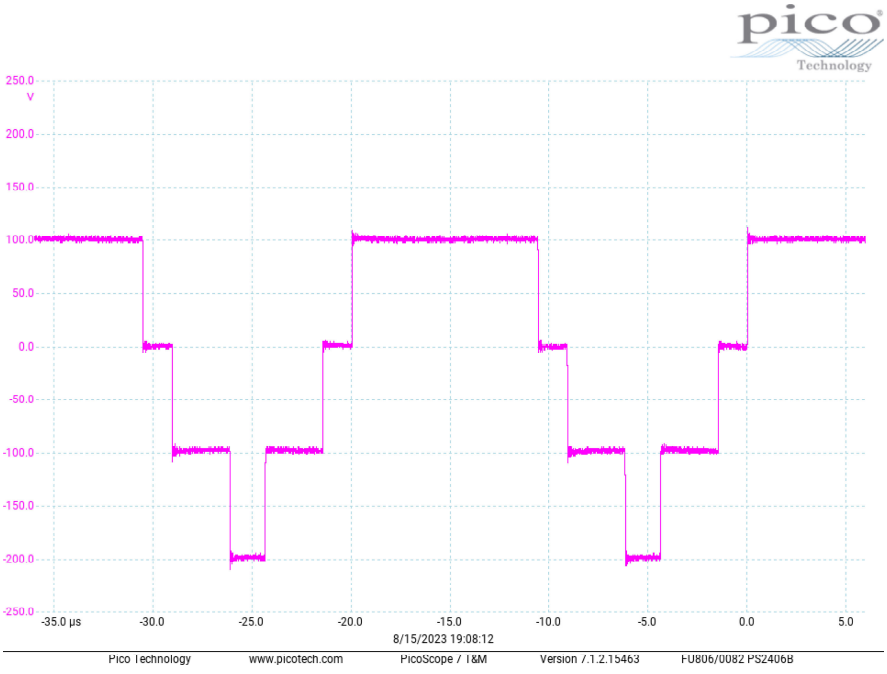
(b) POD SPWM

Figure 5.11: NPC inverter digitally filtered switch node voltages with 600 V DC Bus ($m_a = 0.5$)

The minimum pulse-width distortions at the zero crossings are still visible. However, they have not increased proportionally with voltage, indicating that the distortions at full voltage will be relatively small. Future testing should include measuring the output voltages with the AC filter in place to verify the output quality with the actual power filter.



(a) Positive half cycle



(b) Negative half cycle

Figure 5.12: PD SPWM V_{cm} with 600 V DC bus (m_a=0.5)

The V_{cm} of the two tested PWM methods were measured under operation with the 600 V DC bus. The results are shown for PD SPWM and POD SPWM in Figures 5.12 and 5.13, respectively. It can be observed that the measured V_{cm} has amplitude $\pm\frac{V_{dc}}{3}$ for PD SPWM and is reduced to $\pm\frac{V_{dc}}{6}$ with POD SPWM. This is consistent with both simulations and the LV PWM test results.

The FFTs of V_{cm} under operation with the 600 V DC bus are shown in Figures 5.14 and 5.15, respectively. As can be observed, the 150 Hz third harmonic is much smaller in comparison to the frequency components from 1 to 6 kHz. This is because the minimum pulse-width distortions do not increase proportionally with output voltage, as previously mentioned. The f_{sw} components are consistent with simulation results and the Section 5.1 results for both PWM methods. The ratio of the 150 Hz component and the 1 to 6 kHz components are closer to the simulation results because the operating voltages are closer.

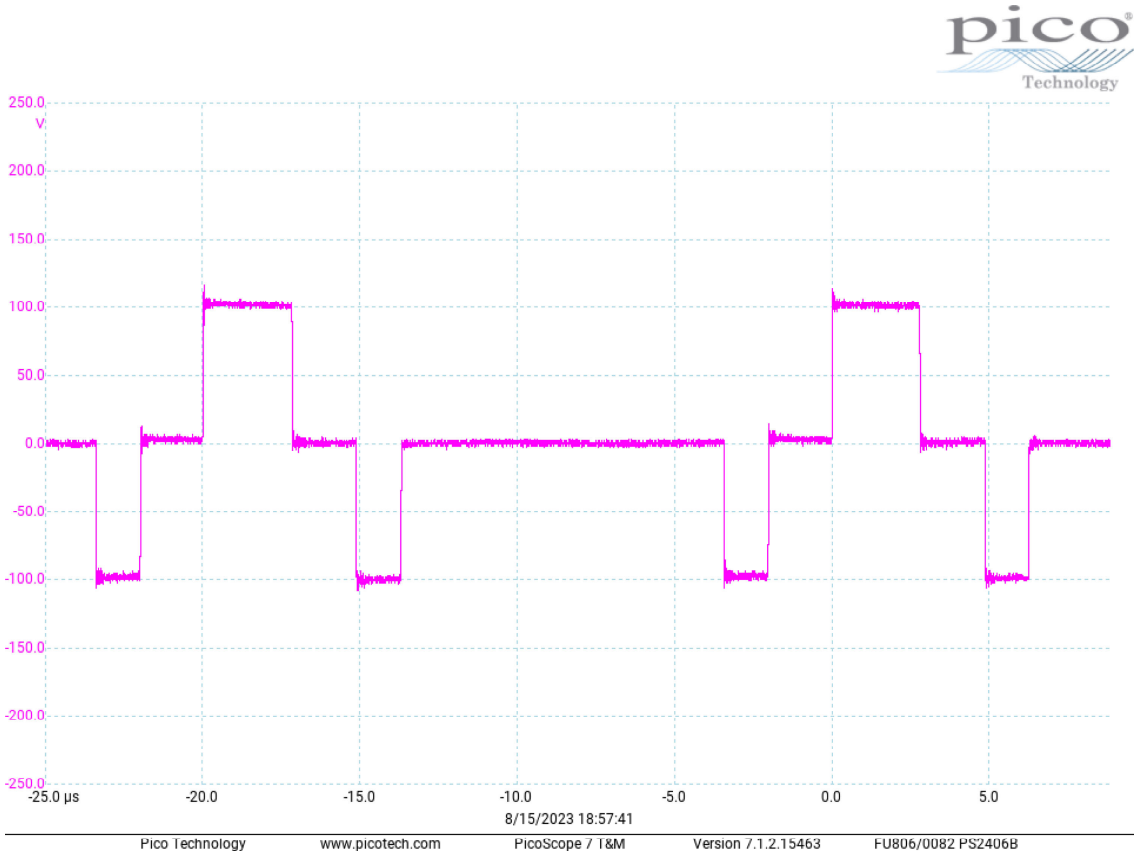
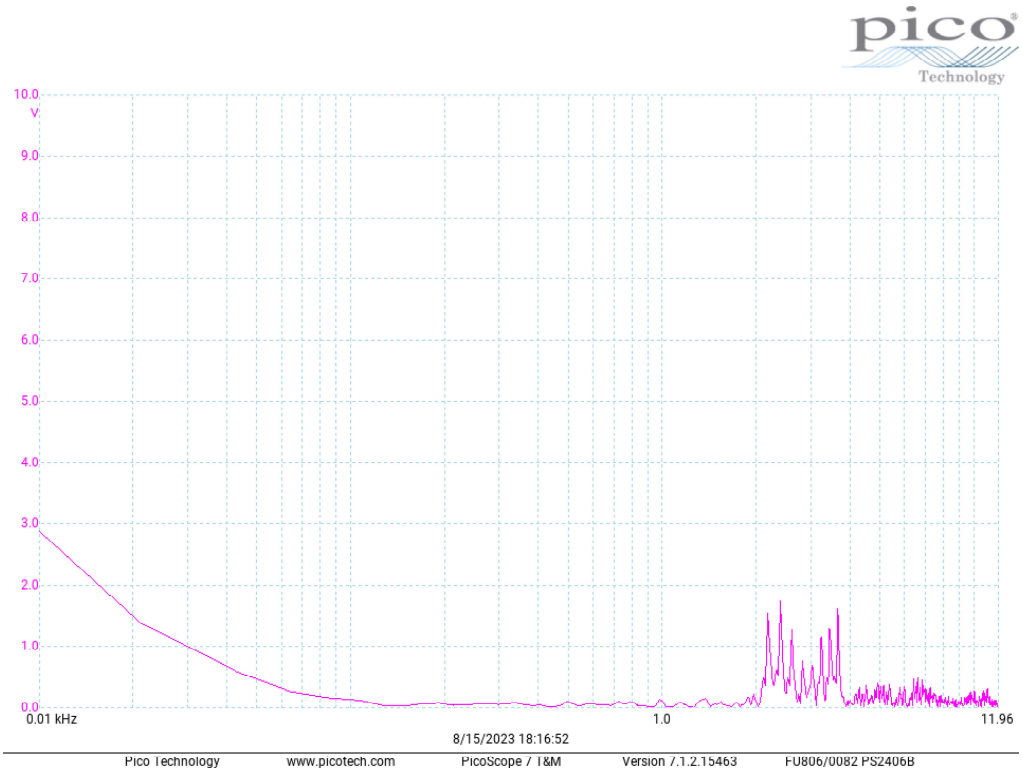
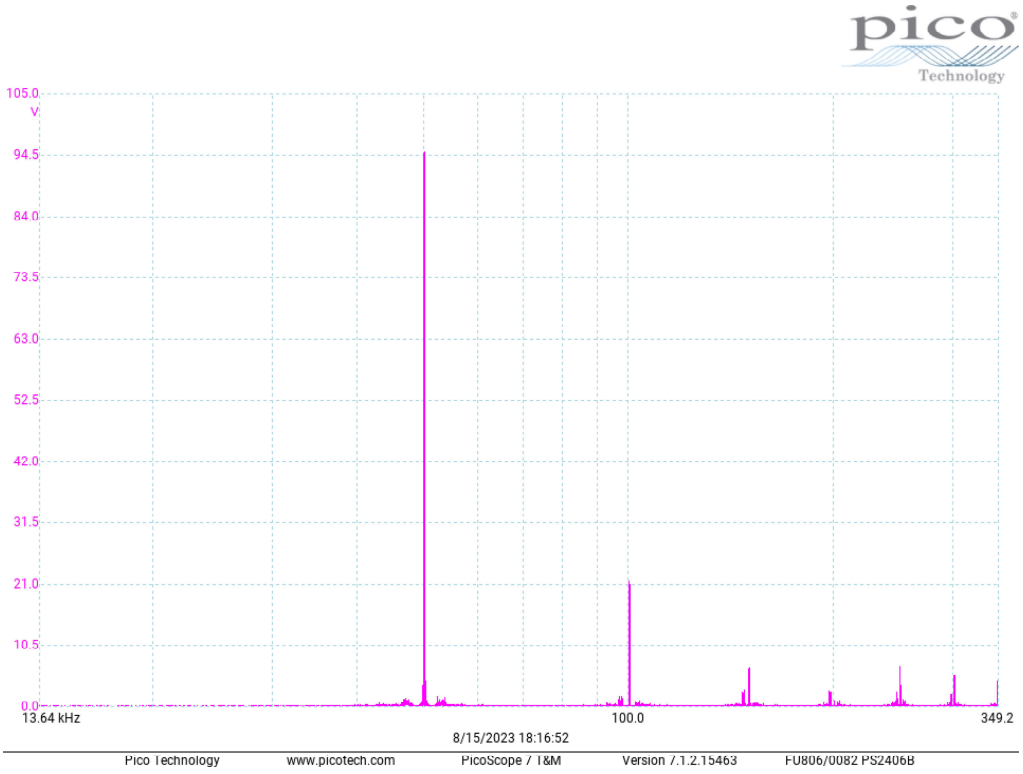


Figure 5.13: POD SPWM V_{cm} with 600 V DC bus (m_a=0.5)

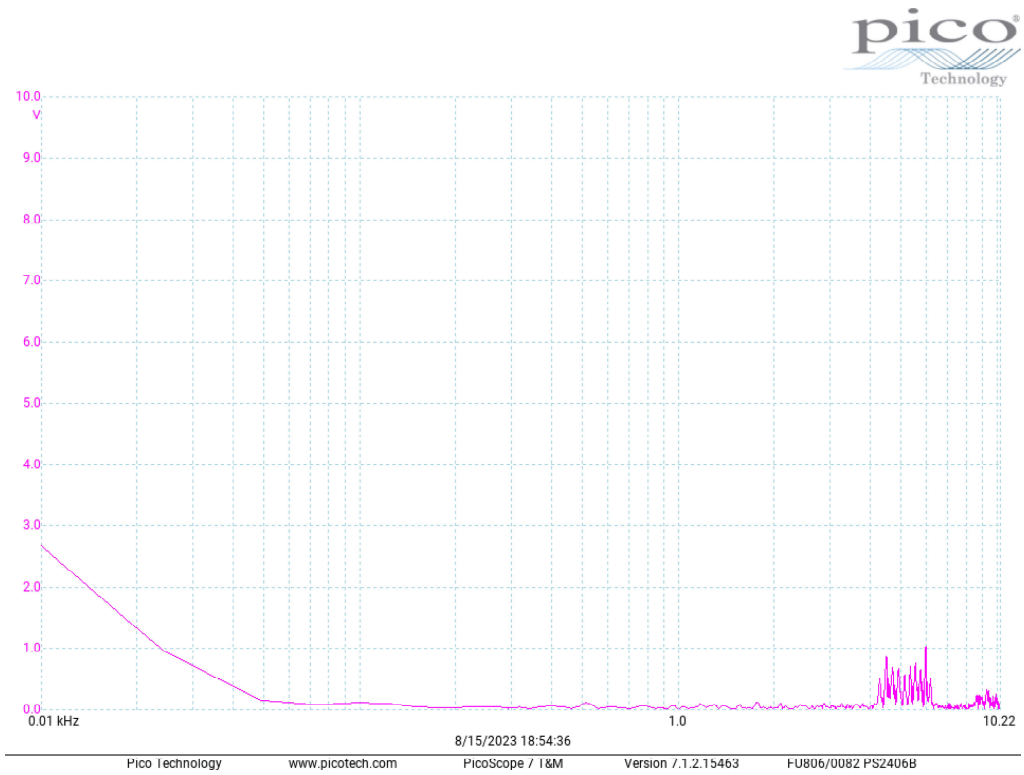


(a) Grid harmonic range FFT

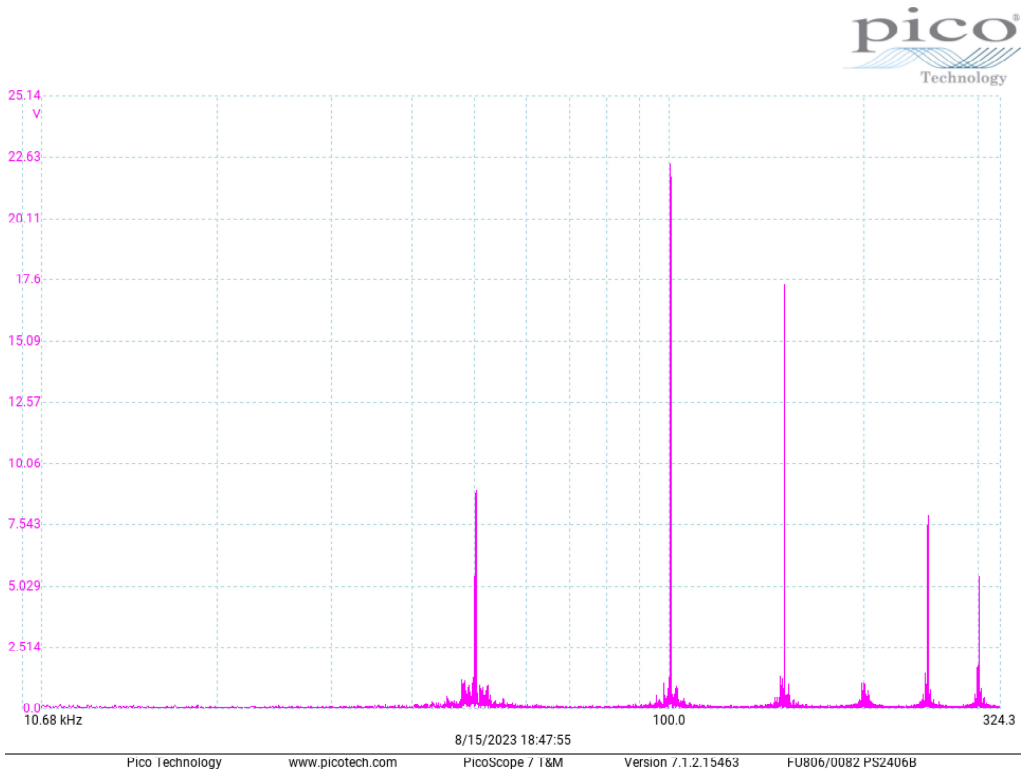


(b) f_{sw} range FFT

Figure 5.14: PD SPWM V_{cm} FFTs with 600 V DC bus (m_a=0.5)



(a) Grid harmonic range FFT



(b) f_{sw} range FFT

Figure 5.15: POD SPWM V_{cm} FFTs with 600 V DC bus (m_a=0.5)

5.3 Chapter Summary

This chapter discusses the experimental hardware prototype NPC inverter that was designed and built. Low-voltage testing was conducted to verify proper operation of the inverter PCBs. The two carrier-based SPWM methods, simulated in Chapters 3 and 4, are experimentally verified for their common-mode voltage frequency profiles. The measured common-mode voltages match the simulation results but the 150 Hz third harmonic component is disproportionately large compared to the other frequency components. This is due to the low operating voltages, resulting in minimum-pulse width distortion having a proportionally larger effect. The two SPWM modulation methods were then tested with a DC bus voltage of 600 V and modulation index of 0.5. At the higher voltage level, the proportional effect of minimum pulse-width distortion is lower and the measured common-mode voltage frequency profiles more closely match the simulation results. Future work should include implementing the SVM methods to evaluate their common-mode performance and testing the converter AC output with the AC filter in place.

Chapter 6: Conclusion and Recommended Future Work

The goal of this thesis work was to select a 3-ϕ DC-AC converter topology and develop modulation methods to enable a transformerless interface between a LV bipolar DC microgrid and the LV AC grid. It was desired for the modulation methods to keep ground leakage current below RCD tripping thresholds and for the selected converter topology to be capable of DC bus voltage balancing. The contributions of this work are extending the modulation method developed in [42] to 3-L converters and developing a modified version of the modulation method capable of simultaneous ground leakage current mitigation and active DC bus voltage balancing within a limited range of modulation index. The developed method also eliminates the characteristic third harmonic DC bus voltage ripple of the NPC converter. This chapter provides a summary of the thesis work, the approach taken and the results presented in the previous chapters. Recommendations for future work are also provided.

6.1 Summary of Chapters

- **Chapter 1** provided a background on bipolar DC microgrid systems. It was explained that having a transformerless power electronic interface between these systems and the LV AC grid can reduce the overall system size, cost and complexity because the need for a LF transformer or isolated DC-DC converter is eliminated. This chapter introduced the challenge of such a transformerless interface due to the resulting ground leakage current and its effect on RCDs. A review of several candidate DC-AC converter topologies was presented. The 3-L NPC topology was selected because it limits the switch blocking voltage to half of the DC bus voltage and can directly connect to the bipolar DC grid neutral-point for DC bus voltage balancing. Finally, this chapter presented the thesis research questions and gave an overview of the report chapters.

- **Chapter 2** provided an overview of carrier-based PWM and SVM. The general implementations of these two types of PWM was explained and a framework for discussing the modulation techniques in Chapters 3 and 4 was developed. The effect of dead-time and minimum pulse-width was briefly explained and a dead-time compensation method, used in the simulations of Chapters 3 and 4, was shown.

- **Chapter 3** explained how common-mode voltage is defined for a 3-ϕ inverter and how each converter switching state results in a fixed common-mode voltage, assuming a constant DC bus voltage. Then, as the converter transitions through the different switching states, based on the modulation, a time-varying common-mode voltage with AC components is produced. The common-mode circuit of a a 3-ϕ inverter connected to the AC grid via an LCL filter is presented. Then the resulting common-mode impedance for typical LCL filter component values is shown when the inverter DC side is connected to a bipolar DC microgrid with 50 μF of grounding capacitance. This chapter also explained the basic operation of RCDs, their tripping threshold limits set by the governing standards and why ground leakage current generated by a power electronic converter can cause RCDs to false trip. Finally, Chapter 3

presents the simulated common-mode performance of several existing modulation methods under ideal DC bus conditions. The results show that some of these modulation methods produce ground leakage currents that exceed the RCD tripping threshold limits. Additionally, others, such as PD SPWM and POD SPWM, do not exceed the RCD tripping thresholds defined for 50 Hz to 1 kHz, but produce appreciable ground leakage currents at the 4.3 kHz common-mode resonance of the LCL filter. Such frequency components are known to reduce the sensitivity of RCDs which presents a potential safety hazard. Finally, the proposed SVM method, which balances the common-mode voltage over a switching period by redistributing the small vector dwell-times, is explained. The simulation results show that this method produces significantly lower ground leakage currents compared to the other simulated modulation methods, most noticeably at the resonance points of the common-mode impedance.

- **Chapter 4** provided an overview of load imbalance in the bipolar DC microgrid system and presented the basic balancing converter solution to maintain voltage balance of the DC poles. The addition of a balancing converter increases system cost and complexity. Therefore, Chapter 4 analyzed methods of balancing the DC bus voltages with the 3-L NPC converter. The DC bus voltage balancing capability of the NPC converter with SVM using a 7-segment and 9-segment vector sequence was explained. The characteristic third harmonic DC bus ripple of the NPC converter, due to small and medium vector dwell-time distribution, was also analyzed and simulations showed that modulation methods can be used to eliminate this ripple. Additionally, simulation results showed that common-mode current flowing into the DC bus neutral-point can also cause DC bus voltage ripple. Then, the simulated common-mode performance of the selected modulation methods with a non-ideal DC bus was presented. For PD SPWM, POD SPWM, M^2ZV SVM and SPCMB SVM, an increase in the 150 Hz third harmonic component was observable in the common-mode voltage due to the DC bus voltage ripple. This increase resulted in a 150 Hz component in the ground leakage current that exceeded the RCD tripping threshold limit. Therefore, a modulation method is proposed which redistributes the small vector dwell-times to balance the DC bus voltage and uses the redundant zero state vectors to balance the common-mode voltage over a switching period. Thus, this method is able to simultaneously balance the DC bus voltages, shift the common-mode voltage to the switching frequency and eliminate the DC bus voltage third harmonic ripple. However, this modulation method was shown to have significant limitations as it can only work if the modulation index is below 0.571. Furthermore, the DC bus load ratio for which the common-mode voltage can be balanced is dependent on the modulation index. With higher modulation indexes, there is less zero vector dwell-time to compensate for the common-mode voltage volt-second balance of the small vectors.

- **Chapter 5** presented the 3-L NPC converter hardware prototype that was designed and built to experimentally test the modulation methods analyzed and simulated in Chapters 3 and 4. PD SPWM and POD SPWM are implemented on the hardware and the resulting switch node voltages are directly measured with an oscilloscope. Using the oscilloscope's digital filtering, the $3-\phi$ sinusoidal output is verified for both modulation methods. Distortions in the voltage zero crossings due to minimum pulse-width are observable in the measurements. The oscilloscope's math channel is used to measure the converter common-mode voltage which is consistent with simulation results for both PD SPWM and POD SPWM. Additionally, the common-mode voltage FFTs for both modulation methods show consistent results in the switching frequency range with the simulations.

6.2 Assessment of Research Questions

1. **What are the existing modulation methods for reducing/eliminating common-mode current in the 3-L 3-ϕ NPC DC-AC converter?**

   The existing modulation methods for reducing/eliminating common-mode current in the NPC converter are shown to consist of methods that avoid state vectors with $|V_{cm}| > \frac{V_{dc}}{6}$, such as POD SPWM, or methods that only use state vectors with $V_{cm} = 0$, such as M^{2}ZV SVM. The pros and cons of these different methods are shown through simulations. Although POD SPWM reduces the maximum instantaneous V_{cm}, it still results in V_{cm} transitioning between $\frac{V_{dc}}{6}$ and $-\frac{V_{dc}}{6}$. In M^{2}ZV SVM, only the neutral zero state vector and the medium state vectors are used in order to achieve $V_{cm} = 0$. However, due to dead-time, M^{2}ZV SVM produces non-zero V_{cm} during the intervals where phase reference voltage and phase current are opposite in polarity. Additionally, this method cannot actively balance the DC bus voltages because it does not use the small state vectors. A modulation method for reducing ground leakage current in 2-L 3-ϕ DC-AC converters was proposed in [42] that shifts the V_{cm} frequency composition to the converter switching frequency in order to take advantage of the AC filter's high attenuation at that frequency. In this work, the method is extended to the 3-L NPC converter as SPCMB SVM by modifying the small vector dwell-time distributions. Simulations showed that the proposed method produced significantly lower ground leakage current compared to the assessed existing methods.

2. **What are the existing modulation methods for active DC bus voltage balancing in the 3-L 3-ϕ NPC DC-AC converter?**

   The existing modulation methods for active DC bus voltage balancing vary in their implementation. However, they all rely on adjusting the distributions of the small state vector dwell-times to their redundancies in order to control the DC neutral-point current. By doing this, the DC bus voltages can be balanced by the modulation of the converter. The carrier-based methods generally implement DC bus voltage balancing by controlling the offset of the carrier waveforms relative to the reference waveforms. This work demonstrated how a 9-segment vector sequence enables the NPC converter to balance the DC bus voltages at load ratios up to 1 if the modulation index is below 0.577. This sequence requires a higher number of switching transitions compared to the 7-segment sequence used in [43] but enables increased DC bus balancing capabilities.

3. **Can the AC grid-connected 3-L 3-ϕ NPC DC-AC converter be modulated such that it can simultaneously keep ground leakage currents below protection equipment tripping thresholds and provide active DC pole voltage balancing?**

   There are several modulation methods proposed for the 3-L converters to achieve simultaneous common-mode reduction/elimination and DC bus voltage balancing. Most of them rely on switching between two or more different modulation modes depending on the level of voltage imbalance in the DC bus. They generally implement such modulation with hysteresis-based control logic where the modulator utilizes M^{2}ZV SVM when the DC bus voltage imbalance is below a set amount. If this imbalance limit is exceeded, the modulator switches modes to a modulation scheme that produces non-zero common-mode voltage but re-balances the DC bus voltages. Once the DC bus voltage has been re-balanced, the modulator then returns to M^{2}ZV SVM. For a DC bus with small amounts of drift or momentary imbalances, these methods are effective. However, in the bipolar DC microgrid application where continuous DC bus load imbalance often occurs, the modulation methods must continuously switch

modulation modes to re-balance the DC bus. Therefore, they will produce common-mode currents under these conditions that can interfere with RCDs in the case of a transformerless connection to the AC grid. A 3-L modulation method was developed in this work which can perform both functions simultaneously over a limited range of modulation indexes. While the limited modulation index range is an obvious disadvantage from a general perspective, the bipolar DC microgrid application considered in this work only requires the NPC inverter to operate at modulation indexes below 0.577. Therefore, the developed method is potentially quite useful for the considered application.

6.3 Recommended Future Work

This thesis work considered the common-mode voltage performance and DC bus voltage balancing of modulation methods for the 3-L 3-ϕ NPC DC-AC converter under steady-state conditions. Among considering the effects of dynamic conditions and closed-loop control on the modulator performance, some recommended future work is provided below.

1. **Transient conditions and dynamic control**

   In practice, the grid-tied DC-AC converter must contend with different transient conditions including AC grid faults and DC bus load changes. The DC-AC converter closed-loop control is used to handle these conditions and ultimately does so by adjusting the modulation index and phase of the modulator. Therefore, the performance of the developed modulation methods under dynamic conditions with closed-loop control should be assessed.

2. **Unbalanced AC Grid Voltages**

   This work considers the modulation performance only with balanced AC grid voltages. However, the AC grid voltages can become unequal due to unbalanced phase loading on the inverter side of the distribution transformer. Therefore, an assessment of the typical continuous phase voltage imbalance limits in the LV AC grid should be made and the modulation performance should be evaluated under this imbalance.

3. **Unbalanced DC Pole Voltages**

   Some of the existing modulation methods in the literature [56] consider the effect of unbalanced DC voltages on the modulation and implement techniques to avoid distortion in the converter output waveforms under such conditions. However, this work considers only the steady-state conditions when the DC bus voltages are balanced. Depending on how the bipolar DC grid is operated, it is possible to have unequal DC pole voltages for extended periods of time. Therefore, the NPC converter operation under unbalanced DC bus voltages where the NPC converter is not forming the DC grid should be considered.

4. **Semiconductor Losses**

   This work did not quantitatively assess the difference in switching losses of the analyzed modulation methods. However, converter losses and efficiency are important in practice and should therefore be rigorously analyzed. Additionally, the developed modulation methods will cause uneven semiconductor loss distribution under unbalanced DC load conditions. Semiconductor loss distribution with different levels of DC load imbalanced should be assessed to see how this will effect overall thermal performance and efficiency.

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Appendices

Appendix A: RZV SPCMB SVM DC Load Unbalance Limit Derivation

Considering that the DC bus voltage balance controller output, Δs, is equal to the load ratio, ϵ, at steady-state, the limit for $|\epsilon|$ under which the modulator can maintain the common-mode volt-second balance over a switching period throughout the full grid cycle can be derived below. The 3-L space vector hexagon with common-mode voltages labeled is shown below for convenience.

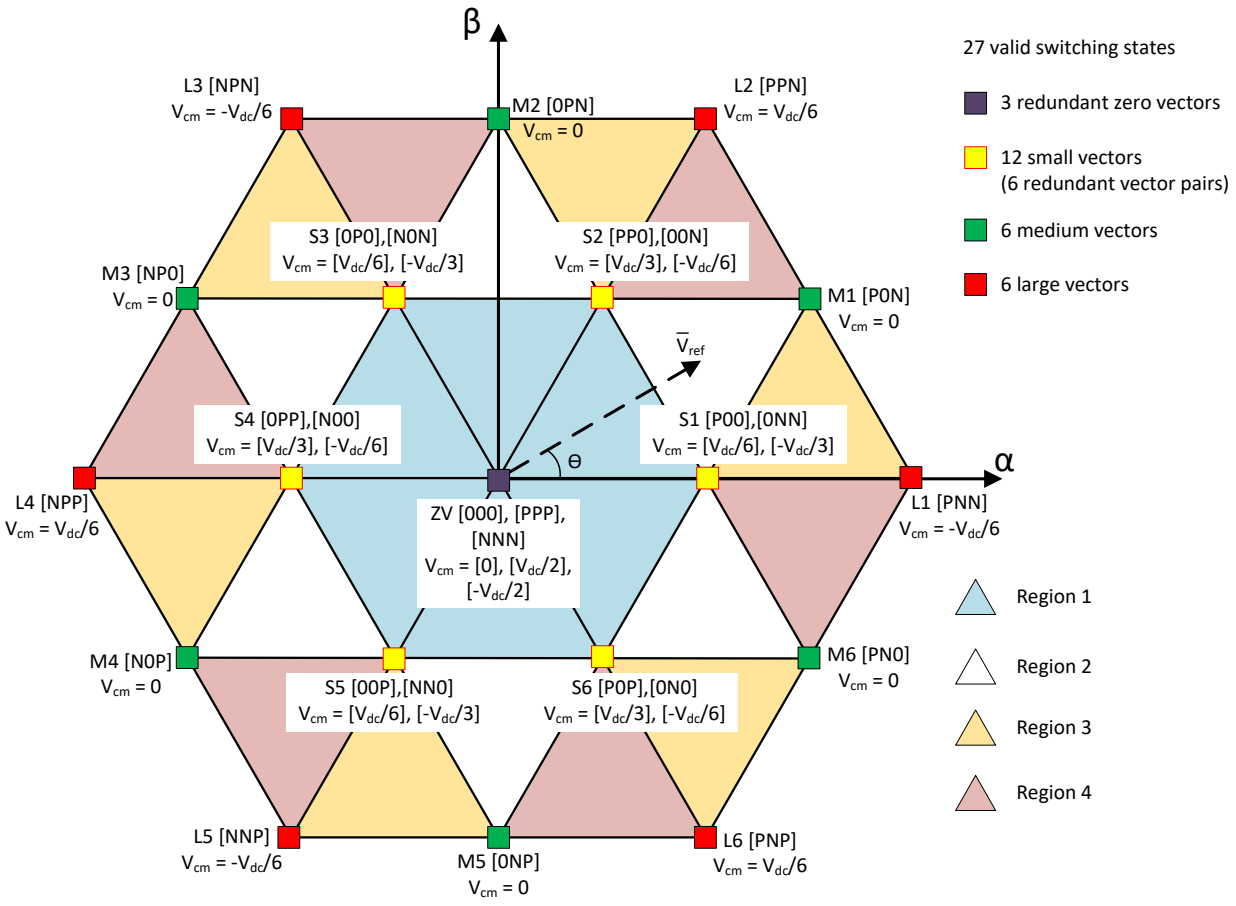

Figure A1: Three-level space vector hexagon with state vector common-mode voltages

$|\epsilon|_{max}$ will be determined by the point at which there is no longer sufficient zero vector dwell-time to redistribute to the redundant zero vectors in order to balance the net common-mode volt-second balance from the small vectors. The worst case will occur at the space vector hexagon sector boundaries where $\theta = 0°$or $60°$. At these points, all of the small vector dwell-time is allocated to the small vector corresponding to that sector boundary. As $|\epsilon|$ increases, more small vector dwell-time will be distributed to the small vector redundancy with $|V_{cm}| = \frac{V_{dc}}{3}$ at every other sector boundary,

resulting in the largest magnitude of common-mode volt-second balance at these boundaries.

The sector boundary between Sector I and Sector VI is taken as an example. When the reference vector is at this boundary, $\theta = 0$. From the equations of Table 2.6 for Region 1, it can be determined that T_{S1} is given by Equation A1. The positive and negative redundancy dwell-times of T_{S1} are given by Equations A2 and A3, respectively. This results in Equations A4 and A5.

$$T_{S1} = 1.5 * m_a * T_{sw} \tag{A1}$$

$$T_{S1p} = 0.5 * T_{S1} * (1 - \epsilon) \tag{A2}$$

$$T_{S1n} = 0.5 * T_{S1} * (1 + \epsilon) \tag{A3}$$

$$T_{S1p} = 0.75 * m_a * T_{sw} * (1 - \epsilon) \tag{A4}$$

$$T_{S1n} = 0.75 * m_a * T_{sw} * (1 + \epsilon) \tag{A5}$$

The small vector common-mode volt-second balance, $SV_{cmv-bal}$, is then given by Equation A6.

$$SV_{cmv-bal} = 0.75 * m_a * T_{sw} * [\frac{1}{3} * (1 + \epsilon) - \frac{1}{6} * (1 - \epsilon)] \tag{A6}$$

Considering the redundant zero vectors have $|V_{cm}| = \frac{V_{dc}}{2}$, the inequality of Equation A7 must be met for the common-mode voltage volt-second balance over the switching period to be achieved. Setting the two sides of the inequality equal and solving for ϵ in terms of m_a results in Equation A8. Recognizing that Equation A8 only applies for the conditions over which $|\epsilon| \leq 1$, the complete limit for ϵ is given by Equation A9. Above $m_a = 0.571$, the zero vector dwell time becomes too small to balance the net small vector common-mode volt-second balance over the complete fundamental cycle and a third harmonic will begin to appear in the common-mode voltage.

$$|0.75 * m_a * T_{sw} * [\frac{1}{3} * (1 + \epsilon) - \frac{1}{6} * (1 - \epsilon)]| < 0.5 * (1 - 1.5 * m_a * T_{sw}) \tag{A7}$$

$$|\epsilon|_{max} = \frac{4 - 7m_a}{3m_a} \tag{A8}$$

$$\begin{cases} |\epsilon|_{max} = 1, & 0 < m_a < 0.4 \\ |\epsilon|_{max} = \frac{4-7m_a}{3m_a}, & 0.4 < m_a < 0.571 \end{cases} \tag{A9}$$

Appendix B: PLECS Simulations

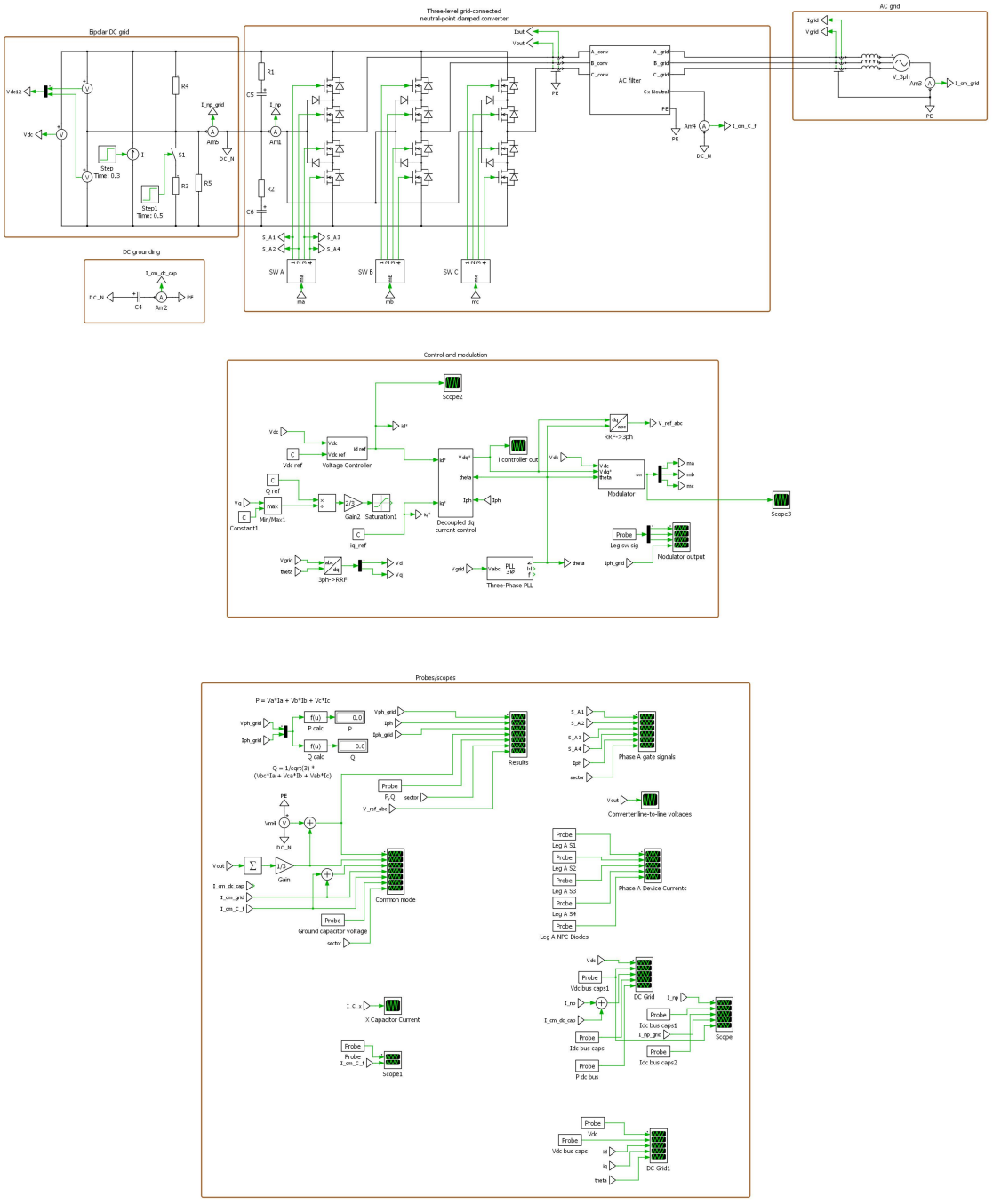

Figure B1: 3-L NPC converter PLECS simulations schematic

```
% DC and AC grid parameters
V_dc_grid = 1400; % DC grid voltage [V]
V_ac_grid = 400;   % AC grid RMS line-to-line voltage [V]
V_ac_grid_l_n = V_ac_grid/sqrt(3); % AC output RMS line-to-neutral voltage [V]
L_grid = 0e-9;     % Grid inductance [H]
f_grid = 50;       % AC grid frequency [Hz]
C_dc_g = 50e-6;    % DC grid neutral ground capacitor [F]
C_dc_pole = 390e-6; % DC bus pole capacitance [F]

% Power references and limits
P_ref = 11e3;     % Active power reference [W]
Q_ref = 1e3;       % Reactive power reference [VAR]
iq_ref = 15;       % q-axis current reference [A]
I_d_max = 30;     % d-axis current limit [A]
I_q_max = 5;      % q-axis current limit [A]
P_pv_1 = 0e3;     % PV initial power [W]
P_pv_2 = 0e3;     % PV final power [W]

% DC load parameters

P_dc_top = 5.5e3; % DC top nominal load [W]
P_dc_bottom_1 = 5.5e3; % DC bottom nominal load [W]
P_dc_bottom_2 = 5.92e3; % DC bottom nominal load [W]
R_dc_top = (0.5*V_dc_grid)^2/P_dc_top; % DC top load resistance [W]
R_dc_bottom_1 = (0.5*V_dc_grid)^2/P_dc_bottom_1; % DC bottom load resistance [W]
R_dc_bottom_2 = (0.5*V_dc_grid)^2/P_dc_bottom_2; % DC bottom load resistance [W]

% AC filter parameters
L_1 = 300e-6;        % Converter side filter inductance [H]
L_2 = 100e-6;        % Grid side filter inductance [H]
C_f = 5e-6;         % AC filter capacitance [F]
C_x = 5e-6;       % AC filter line-to-dc neutral capacitance [F]
R_damp_x = 100e-3;     % AC filter line-to-dc neutral damping resistance [Ohms]
C_y = 0e-9;       % AC filter line-to-PE capacitance [F]
R_damp_y = 10;  % AC filter line-to-PE damping resistance [Ohms]
CMC_Ls = 1e-3;      % Common-mode choke self-inductance [H]
CMC_Lm = 1e-3;      % Common-mode choke mutual inductance [H]

% Modulator parameters
f_sw = 50e3; % Switching frequency [Hz]
t_d = 200e-9; % Switch turn-on delay (dead-time) [s]

% Controller parameters

Kp_v = 1; % DC bus voltage controller proportional gain
Ki_v = 105; % DC bus voltage controller integral gain

Kp_i = 2; % Current controller proportional gain
Ki_i = 100; % Current controller integral gain

Kp_del_s = 0.005%0.3; % dc pole balancing controller proportional gain
Ki_del_s = 0.5; % dc pole balancing controller integral gain
```

Figure B2: 3-L NPC converter PLECS simulations parameter initializations

Appendix C: Hardware PCBs

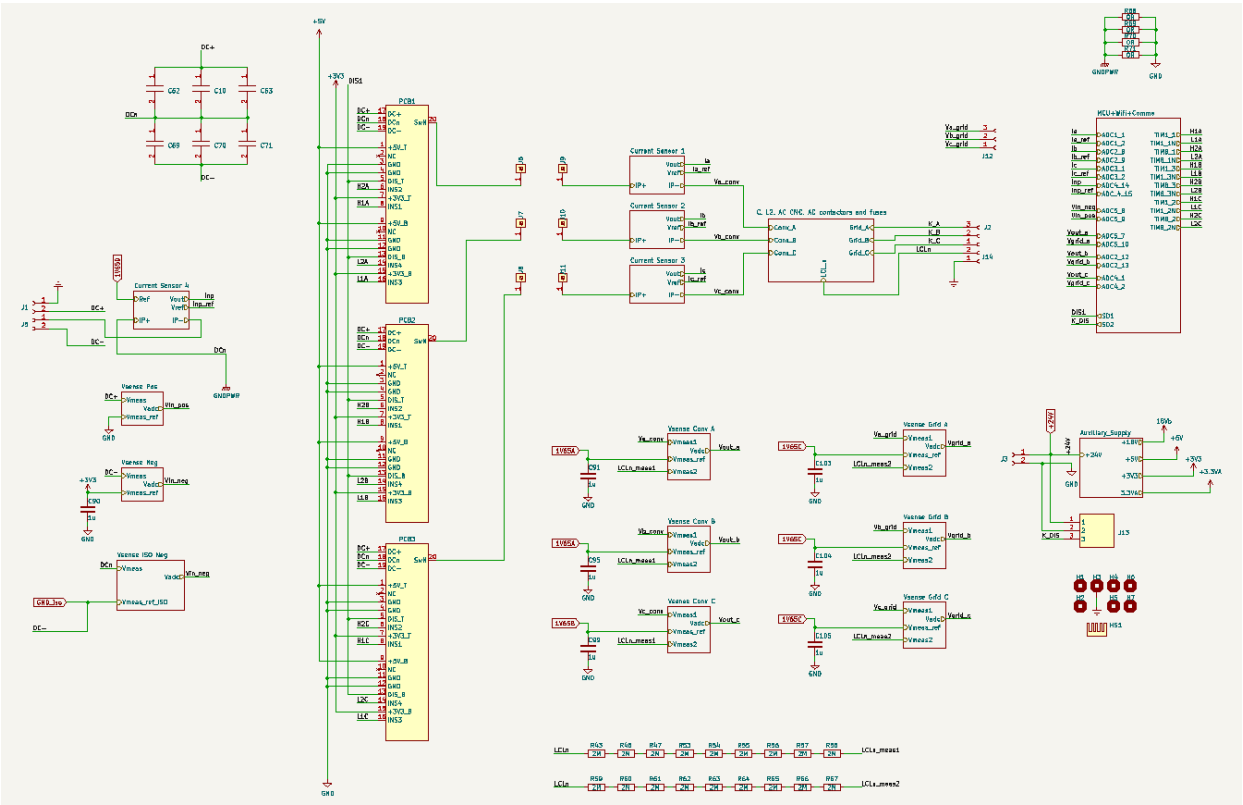

Figure C1: NPC converter main PCB schematic

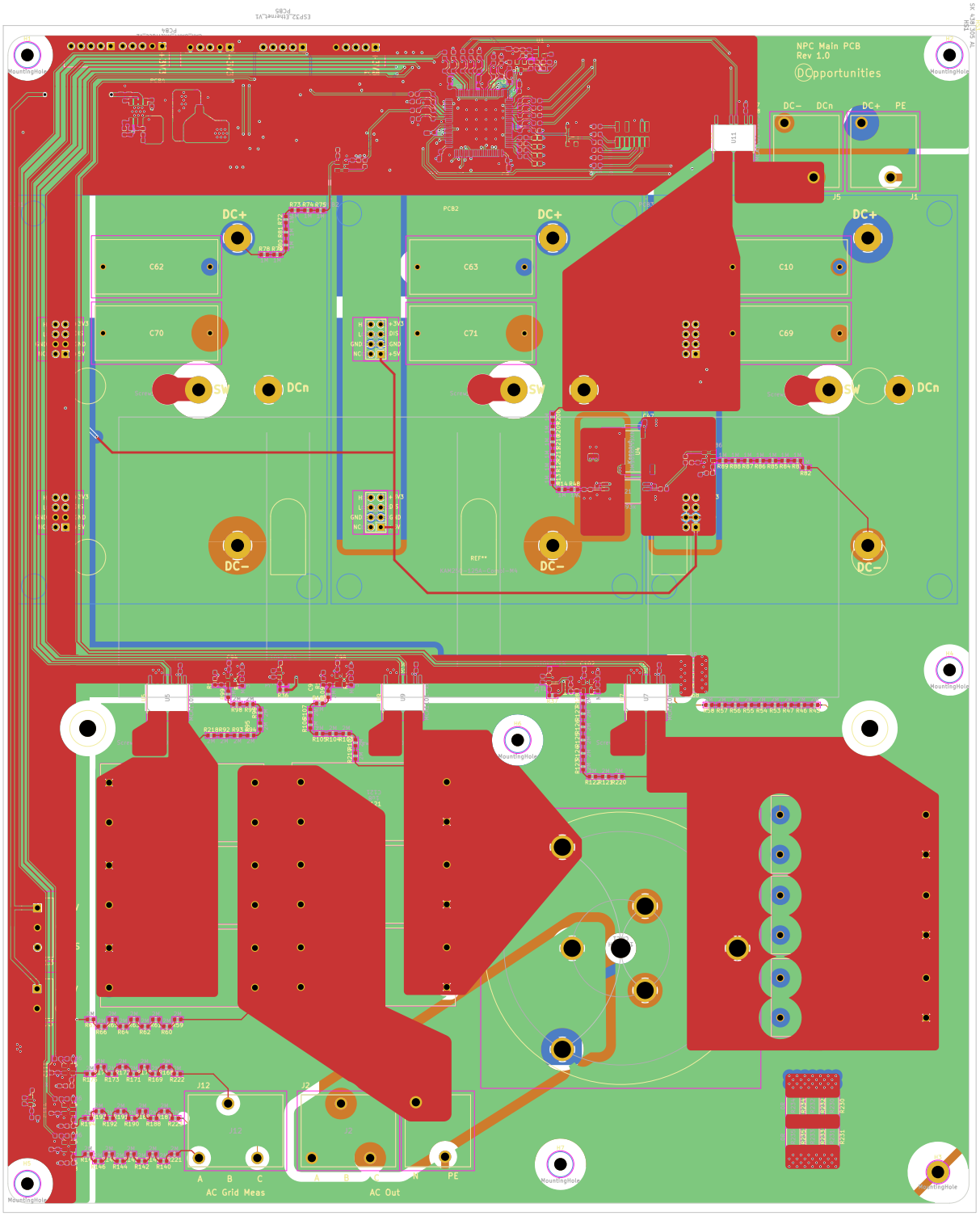

Figure C2: NPC converter main PCB layout

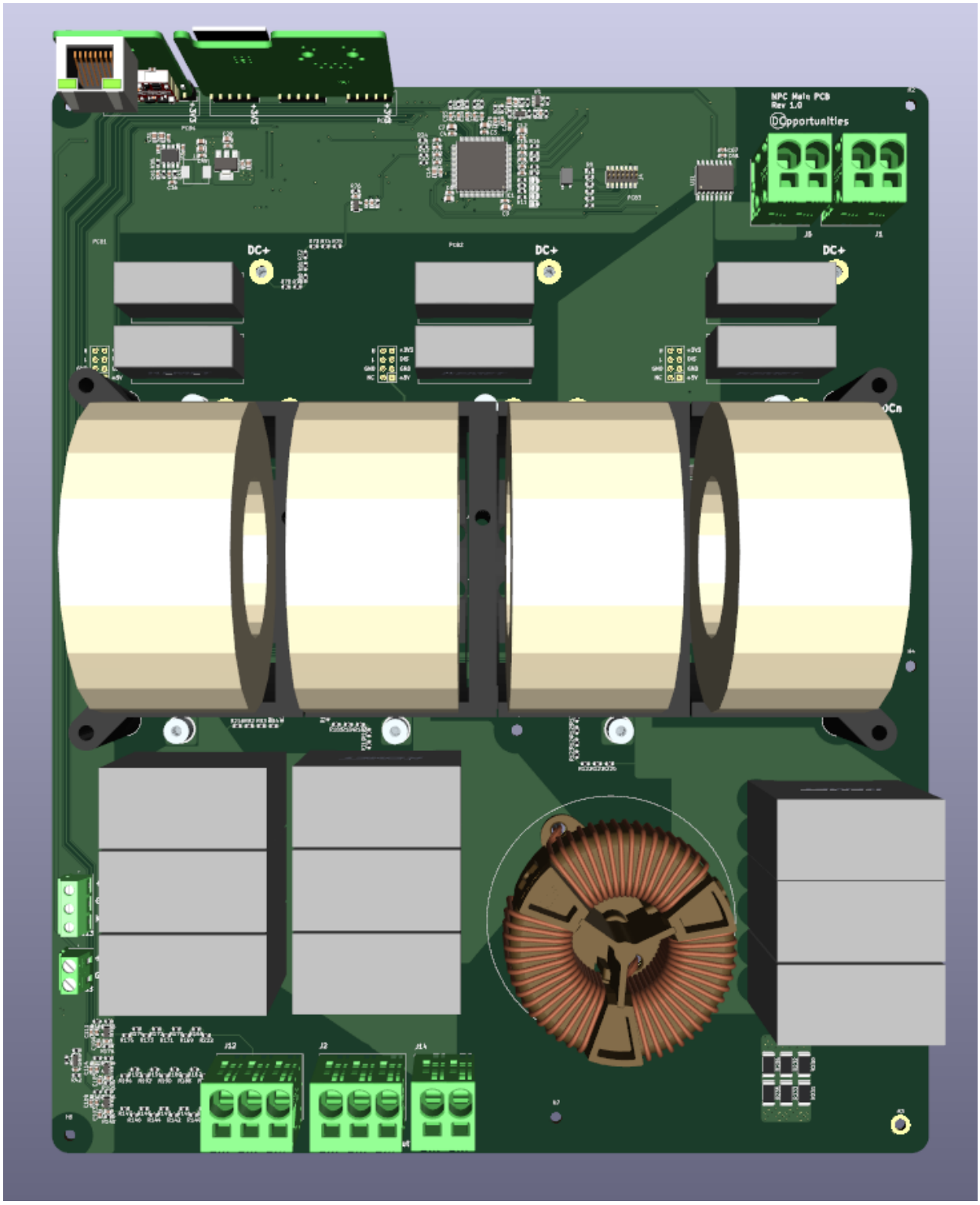

Figure C3: NPC converter main PCB 3D view

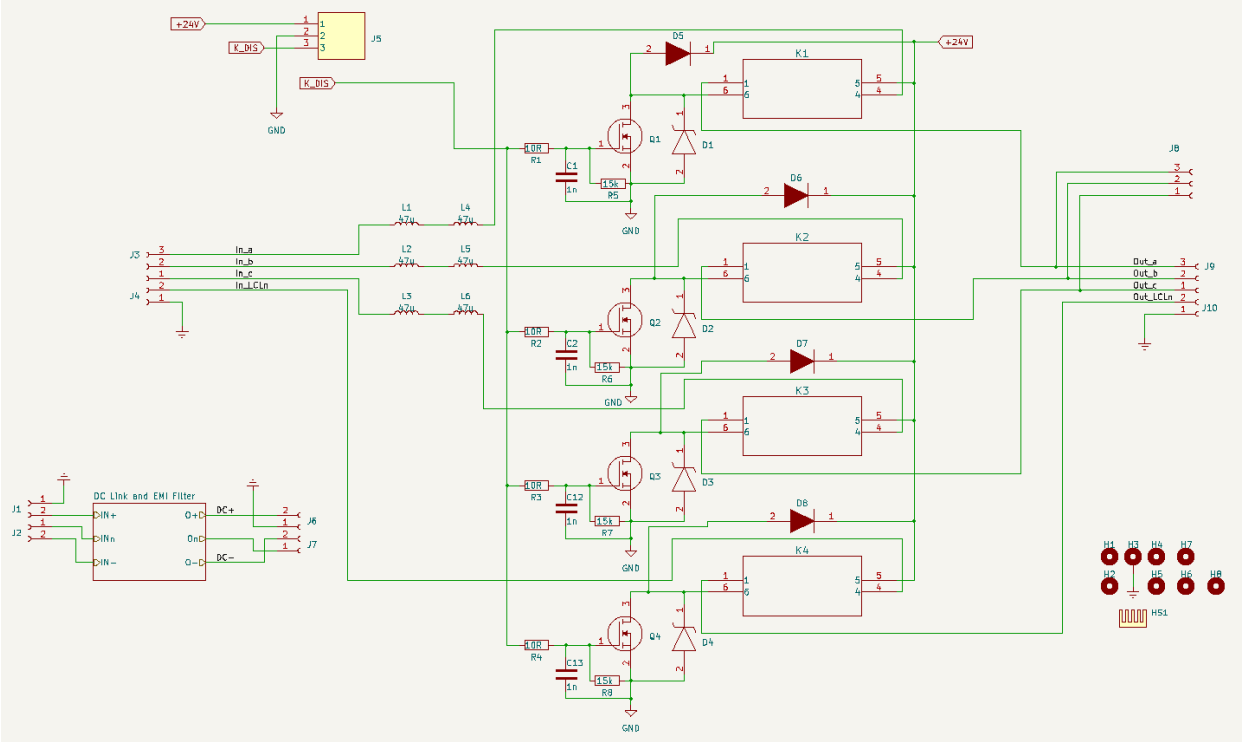

Figure C4: NPC converter contactor PCB schematic

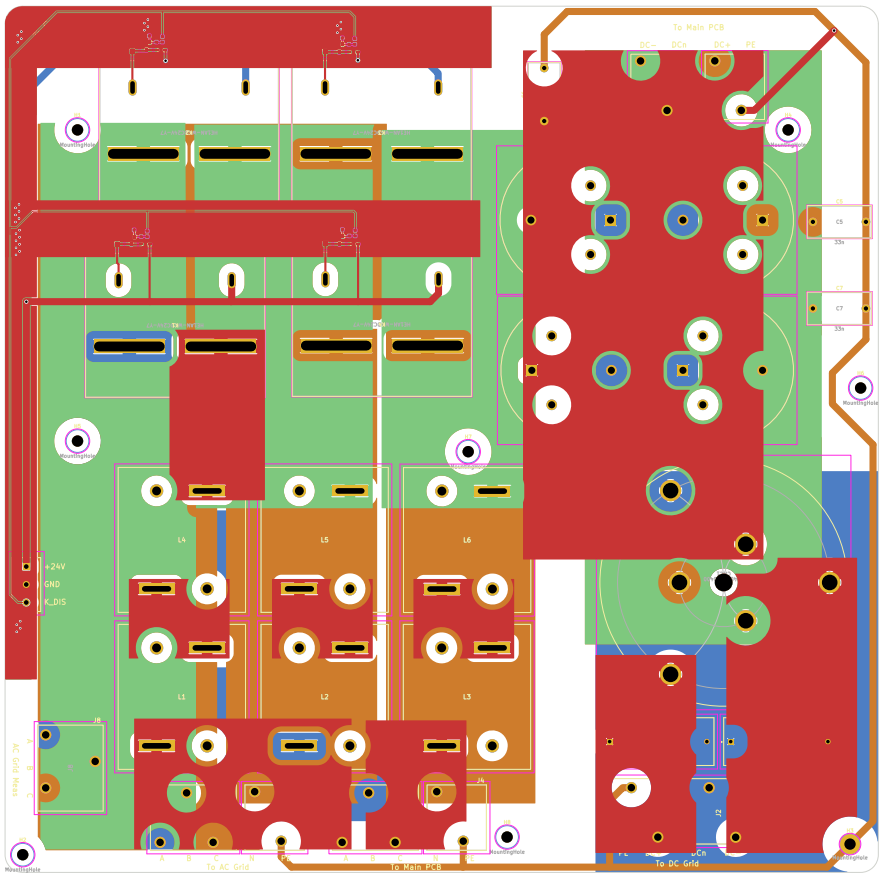

Figure C5: NPC converter contactor PCB layout

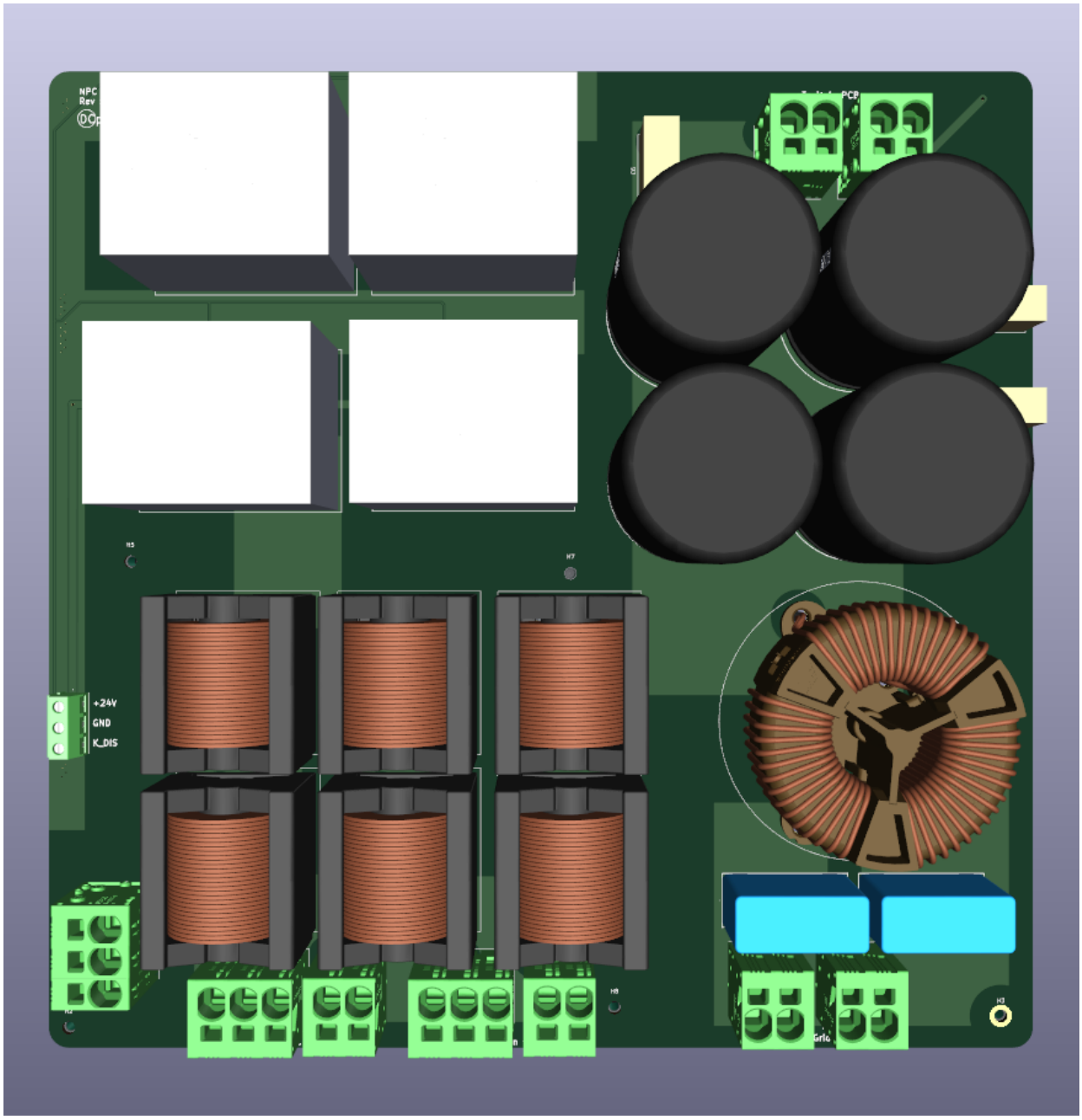

Figure C6: NPC converter contactor PCB 3D view

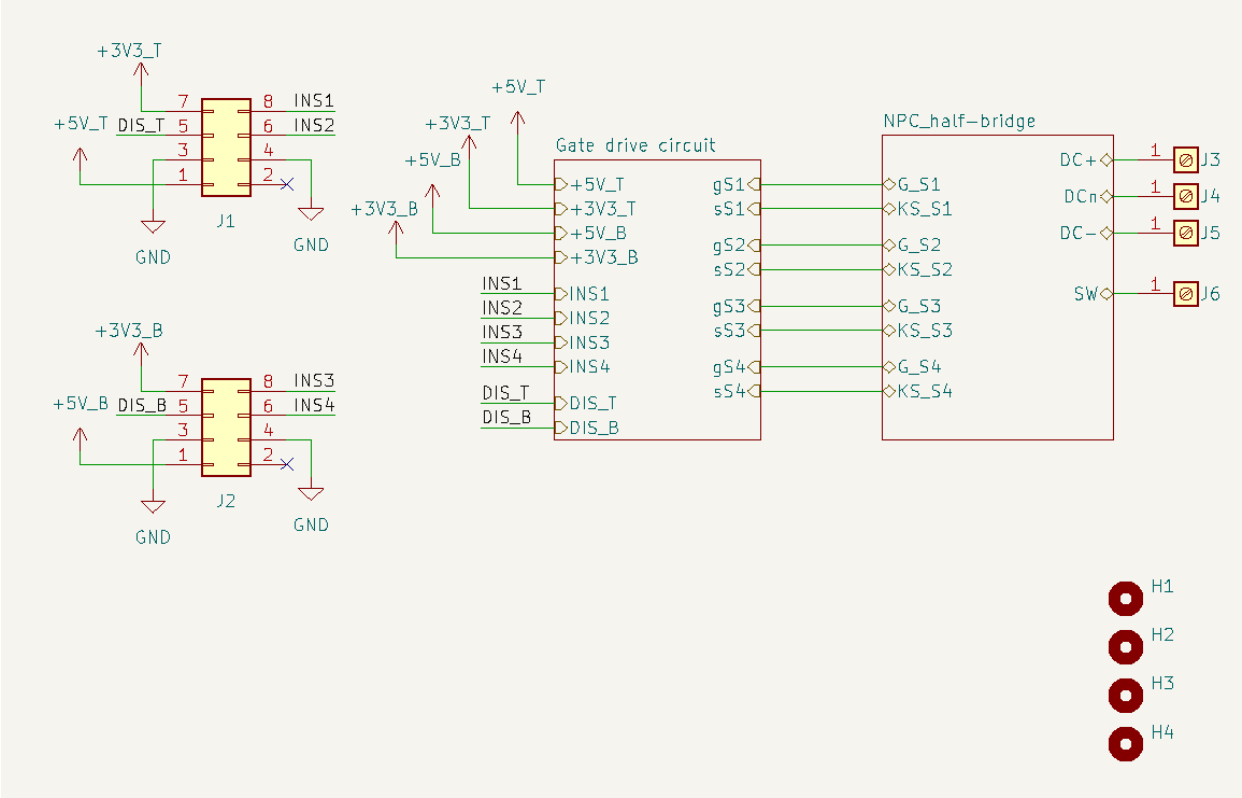

Figure C7: NPC converter power stage PCB schematic

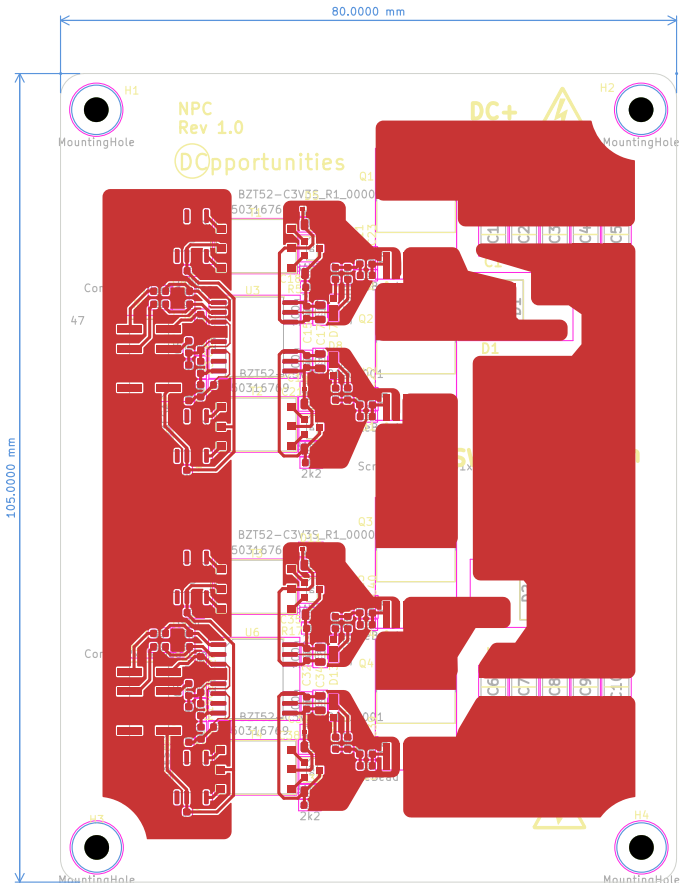

Figure C8: NPC converter power stage PCB layout

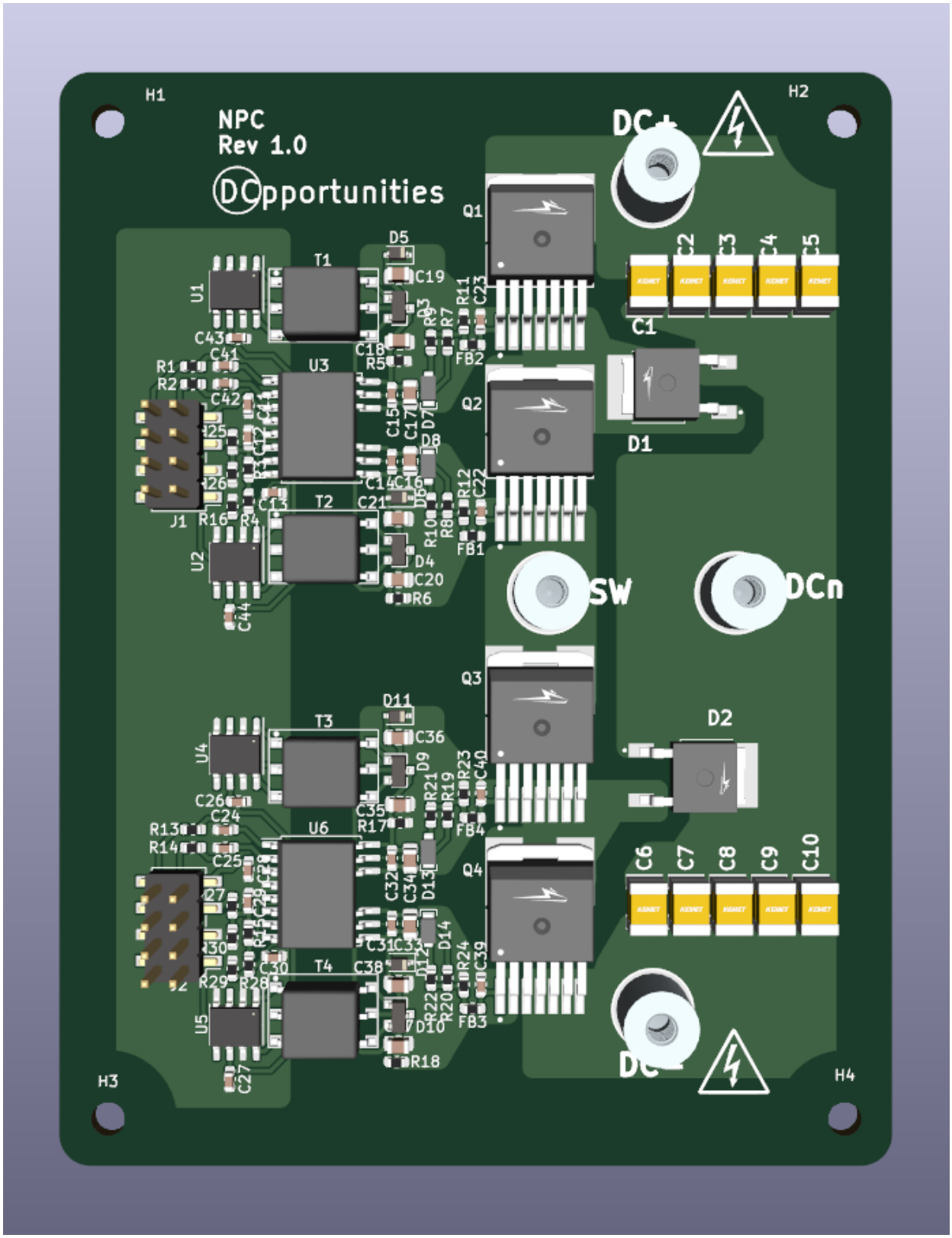

Figure C9: NPC converter power stage PCB 3D view