# Technical performance of different DC CB technologies for future HVDC Grids

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Master of Science

TU Delft Delft University of Technology

IEPG Intelligent Electrical Power Grids

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by

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*Never stop fighting until you arrive at your destined place — that is, the unique you. Have an aim in life, continuously acquire knowledge, work hard, and have perseverance to realize the great life.*

Dr APJ Abdul Kalam

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*Ajay Shetgaonkar*
*Delft, July 2020*

# Abstract

Multiterminal dc (MTDC) network is preferred due to its reliability, security of supply and flexibility. However, MTDC network also comes with the protection challenges resulting from dc faults. Hence, the dc circuit breaker (DC CB) is imperative in such a network. In these recent years, several DC CB technologies have been proposed and demonstrated by different manufacturers. Besides, these DC CB technologies differ from each other in terms of the speed of operation, interruption capability and costs. Hence, for the optimal performance of the MTDC network, a study of the co-ordinative operation of different DC CB technologies is required. In this thesis, two typical types of DC CBs are modelled in detail and implemented in a 4-terminal MTDC network in PSCAD environment, by considering operation time, interruption capability and interruption characteristics. The obtained results are used for DC CB's selection optimization methodology for the future MTDC networks. Similarly, a scaled model of DC CB has to be analysed in terms of its interruption capability in MTDC network considering various scenarios. Therefore, in this master thesis, technical performance of DC CB technologies is conducted for a test and multiterminal dc network in EMT based software environment.

The DC CB is the key to unlock the reliable operation of a Multi-terminal direct current network, whereas fast, effective and accurate models are frequently needed for system-level studies. Due to higher subsystem components in DC CB, a detailed DC CB model creates a bottleneck in the network analysis. This thesis also proposes and compares, an average model with a detailed model of Voltage source converter Assisted Resonant Current (VARC) and Mechanical DC CB in MTDC Network in terms of their performance and computation time for two typical simulation cases. The average and detailed model is modelled and simulated on the PSCAD/EMTDC electromagnetic transient platform. Decisively, this thesis concludes by presenting an accurate response of the average model during the fast transient event, showing additional computational advantage.

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# List of Abbreviations and Symbols

## Abbreviation

**AC CB** AC circuit breaker

**DC CB** Direct Current Circuit Breaker

**DSO** Distribution System Operators

**EHV** Extra High Voltage

**EMTDC** Electromagnetic Transients including DC

**HVAC** High Voltage Alternating Current

**HVDC** High Voltage Direct Current

**IGBT** Insulated Gate Bipolar Transistor

**ITIV** Initial Transient Interruption Voltage

**MMC** Modular Multilevel Converter

**MTDC** Multi-Terminal HVDC

**OHL** Over-head line

**RCB** Residual Current Breaker

**SA** Surge Arrester

**TIV** Transient Interruption Voltage

**TRV** Transient Recovery Voltage

**TSO** Transmission System Operator

**VARC** VSC Assisted Resonant Current

**VI** Vacuum interrupter

**VSC** Voltage-Source Converter

## Symbols

$\mathbf{C_P}$ Oscillating capacitor

$\mathbf{E_{SA}}$ Energy absorbed by SA

$\mathbf{I_{Line}}$ Line Current

$\mathbf{I_{OSC}}$ Oscillating current

$\mathbf{I_{SA}}$ Current in SA

$\mathbf{I_{VI}}$ Current in VI

$\mathbf{I_{VSC}}$ Current in VSC

$\mathbf{L_{DC}}$ Line inductor

$\mathbf{L_{P}}$ Oscillating inductor

$\mathbf{V_{DCCB}}$ Voltage across DC CB

$\mathbf{V_{DC}}$ System Voltage

$\mathbf{V_{OSC}}$ Voltage across VSC

$\mathbf{V_{SA}}$ Voltage across SA

$\mathbf{V_{th}}$ Threshold voltage

$\mathbf{V_{VI}}$ Voltage across VI

# 1

# Introduction

*This chapter summarizes the development of electrical power grids. It highlights the importance of the HVDC grids for the future energy transition. This chapter also introduces the concepts of multi-terminal DC system with its challenge. Similarly, it introduces the advantages and classification of HVDC breakers, followed by relevant research questions.*

1

## 1.1. HVDC - Driver for an energy revolution

Before the liberalisation of the energy market, the flow of power was from the generators to the loads. There was a signal entity which was driving the flow of power into the transmission networks. Furthermore, with an increase in the demand due to industrialisation and urbanisation, the transmission and distribution network expanded by having more generation plants at different locations. In order to maintain the security of supply with a minimum asset requirement, the local grids were interconnected. With the growing power demands, the interconnection of local grid increases, resulting in the electrification of the entire nation, which further resulted in better interconnection among countries. However, with an increase in the distance, the high voltage transmission lines were preferred. In Europe, the international transmission lines operate at 380 kV. While in India, the Inter-state power transmission operates at 765 kV, 400 kV, 230/220 kV, 110 kV and 66 kV AC lines [1] . Due to international transmission lines, cheap electricity is able to transport from different countries like hydropower from the alpha and nuclear energy from France. As stated earlier, due to the centralised nature of the transmission network, the nature of power flow was predicative which lead to congestion-free power transfer without Load shedding. Over the years, the AC system is matured, with defined disturbance and threats; and operating at economical and technological peak.

The liberalisation of the energy market transformed the traditionally centralised Power system into a decentralized entity. As a result, a single entity was separated into different entities, especially in Europe. For example, now the generator company can offer energy quantity and duration of energy into the energy market independently. In the energy market, upon matching of demand and generation bid, the prices are found. Consequently, the country does not entirely rely upon the generator companies in case of shortage, which results in dependency on interconnection with other countries.

Similarly, after liberalisation, Transmission system operator (TSO), is responsible for the operation of the transmission system. The main task of TSO is to operate the transmission system in the safe zone. Besides, it also maintain and invest into new assets and regulates energy market unbiasedly. Likewise, Distribution system operator (DSO), Prosumer and regulators were also formed. As a consequence of liberalisation, the interconnections between countries are congested due to the large transfer of energy.

Owing to the global concerns about climate change attributed to greenhouse gases emissions, the traditional power plants are being replaced by renewable sources. According to the Paris agreement in 2015, the target was set to limit global temperature rise "well below 2°C" in this century. In response to this, the European Union (EU) released different climate strategies and targets [2]. In the 2020 climate and energy package, EU first agreed on a reduction of greenhouse gases emission by 20 % compared to the 1990 level. Secondly, 20 % of EU energy will yield from renewable sources and lastly, improvement in energy efficiency by 20 %.

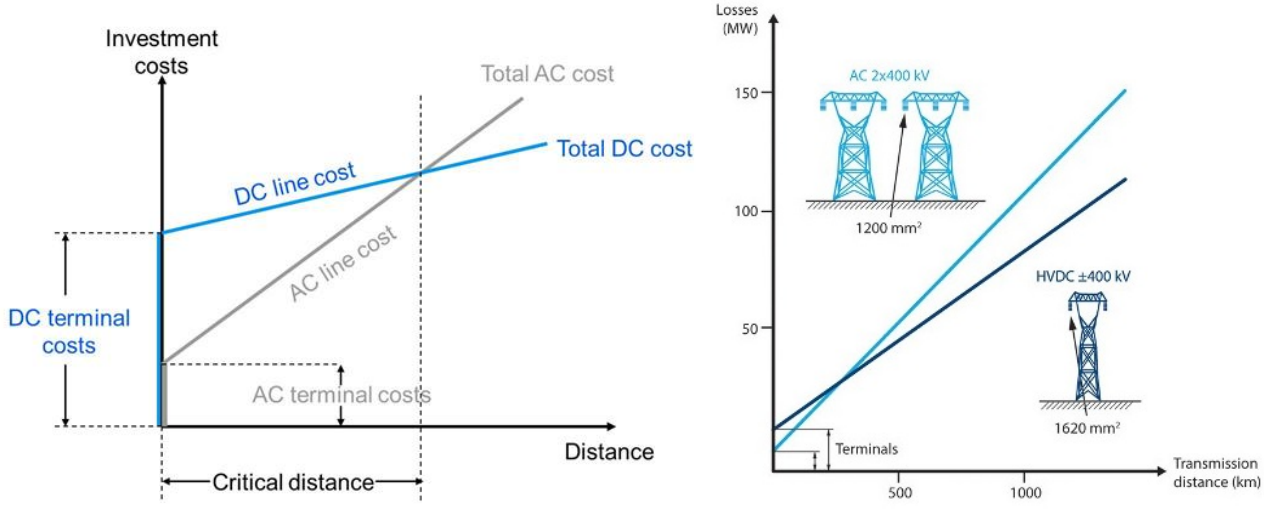
Further, in 2030 climate and energy package, EU agreed in further reduction of green gasses emission at least up to 40%, renewable energy share of at least 32 %, and improvement of energy efficiency by at least by 32.5 %. While, in the long term vision of 2050, the EU aims for zero greenhouse gas emissions. As per these packages, the EU is on track with the reduction of greenhouse gas emissions by 23 % between 1990 to 2018. In response to these strategies, there is a 2% reduction of greenhouse gas emissions in the period of 2017 to 2018. Furthermore, to meet the set target of renewable energy composition, EU has installed 131.9 GW of solar [3] and 205 GW of wind energy [4] at the end of 2019. According to windeurope [5], for 2030 scenario, the installation of wind energy should be 397 GW to meet the target, While 190 GW in case of solar.

Due to these large intermittent energy resources and non-directional flow of power due to liberalisation, existing transmission and distribution network cannot operate without congestion. In order to achieve the set targets, new investments are needed. One of the investment is the HVDC (High voltage Direct Current) link. HVDC supports bulky power transmission between both synchronous and asynchronous systems. Also, it provides flexible power control. The development of VSC (voltage source converter) HVDC has widened the scope for higher penetration of intermittent energy resources spread over different geographical areas into the existing system. Especially in Europe, where the location of solar resources is in the southern part of Europe. While the north sea region has abundance of wind energy, the alps and Scandinavia region have hydropower and

storage resources. Similarly, the Baltic Sea region and Eastern Europe utilizes both biomass and wind. Thus interconnection of these resources is possible with DC grids. In conclusion, HVDC is key to the energy transition.

## 1.2. HVDC v/s HVAC transmission

In AC transmission for the offshore network, with an increase in the distance, charging of cable increases, which limits the power transmission [6]. Hence, HVDC has a more significant advantage for longer transmission of power than HVAC. Moreover, the critical distance after which the investment cost of HVDC is lesser than HVAC and is known as "break-even distance" [7]. It is approximately 600 – 800 km, as shown in figure 1.1. The losses in the HVDC are lower than HVAC after the break-even




(a) (b)

Figure 1.1: Advantage of HVDC transmission compared with HVAC transmission in terms (a) investment cost and (b) Losses in OHL. [7, 8]

distance, as indicated in the figure. Similarly the requirement for the number of conductors are reduced in HVDC. However, regular maintenance is needed for the HVDC converters. Whereas HVAC transformer has lower losses and low maintenance[6], [7]. Furthermore, the voltage conversion is straightforward in AC while in DC, complex space vector transformations are being used for AC to DC transformation.

Since AC grid operates at a fixed frequency, the connection of grid with different frequencies is not possible. However, in HVDC, dependency on frequency and voltage is removed, making the operation of an asynchronous system possible. For example; the HVDC link between 50 Hz network in Eastern Japan to the 60 Hz network in Western Japan [9]. A significant technical advantage of the HVDC is the control over the active power. Besides constant power transfer, HVDC also provides auxiliary services to AC systems like constant frequency control, power redistribution in the AC system and damping in power swing [8].

## 1.3. Multi-terminal HVDC (MTDC) system

Easy active and reactive power control with islanding control mode of VSC based HVDC system enables the Multi-terminal HVDC (MTDC) system. Unlike the Line-commutated current-sourced converters (LCC), VSC has a constant voltage which makes parallel connection easier to construct and control. The MTDC network is HVDC system consists of two or more converters. Based on the topology, the MTDC network is classified into three types, namely Radial, Mesh and series-connected MTDC network [10].

In the radial MTDC network, each converter is separated by a single DC line intersected at a common point. Whereas, in Mesh, each converter can be connected to others with more than one

DC link. In the case of series-connected topology, all the converters are connected in series to form a ring-like structure. Compared too other topologies, the Mesh MTDC topology has higher reliability, and it mimics the traditional AC system. Besides, in meshed MTDC all nodes do not have to be connected to the converter. However, due to its sophisticated architecture, extra coordination and control are required for the secure operation of MTDC.

In 1990, the development of MTDC network was based on LCC technologies and which are still in operation. In the United States, the Hydro-Quebec-New-England MTDC network consists of 5 terminal with radial topology and system voltage is ± 450 kV with a power rating of 2000 MW [11]. The System was built in two phases. In phase 1, point to point HVDC link was established, while in the second phase, the additional terminals were commissioned. Similarly, in Europe, by 1988 Sardinia-Corsica-Italy (SACOI) interconnection was transformed from point to point into the MTDC network with 3 terminals [11]. Operating voltage of this System was 200 kV with monopole configuration.

With the development of IGBTs, the VSC-HVDC system gained popularity due to features like a quick reversal of power and fixed voltage. As of today, China has three MTDC network based on VSC technology [12]. Similarly, Europe's future north sea transnational MTDC network will meet the EU's energy targets and is analysed in PROMOTionN project [13].

## 1.4. Why HVDC Breaker?

The reliable operation of MTDC network depends upon detection of DC faults and DC fault current interruption. Unlike in AC system where the fault detection can be done by impedance relays, in MTDC network, the resistance of the cable is meagre, which makes fault detection difficult. Also, the detection of the fault should be less than 1 ms. Notably, the protection system should identify the location of the fault, i.e whether it has taken place at DC side or at AC side to eliminate nuisance tripping.

In case of a point to point HVDC link, the fault is interrupted by operating the AC circuit breaker, thus leading to zero power flow in the HVDC link. However, incase MTDC network with large power infeed, to interrupt the fault current, each terminal of MTDC has to be disconnected, which results in the de-energisation of DC grid if AC breakers are used. Moreover, this will reflect on the continuity of supply and is not economical. Hence, a DC breaker plays an essential role in an MTDC network as it provides complete selective fault isolation without affecting the power flow within sound DC lines. Due to the higher rate of rise of the DC fault current, the Direct Current Circuit Breaker (DC CB) has to be faster than the conventional AC breaker.

## 1.5. HVDC v/s HVAC breaker

Due to the presence of natural zero crossing in the AC system, the fault current interruption is more straightforward in HVAC breaker. The fault current interruption is divided into three steps, as shown in the figure :

- Upon trip command, Opening of contacts, results in the arc formation between them.
- Increase of distance between contacts, to a distance which will withstand the transient recovery voltage (TRV) at next current zero.
- Current interruption followed by the breaker withstand TRV and system voltage.

However, in the case of the DC system, there is no natural current zero. Thus upon fault, the current rises with higher di/dt as indicated in figure 1.2. Upon application of voltage greater than system voltage (which is known as transient interruption voltage (TIV) ), this rise in fault current is reduced. Furthermore, the current drops down to zero, which result in fault current interruption. Since the DC breaker determines the fault current and voltage across it during fault interruption, DC CB is active in nature [14]. In contrast, in the case of AC breaker, the system determines the TRV and the fault current. Hence, AC CB is considered as a passive element.

Due to the periodic nature of Sine wave in AC network, the line inductance of Over-head line (OHL) and cable magnetises and demagnetises at fixed system frequency. Whereas in the DC

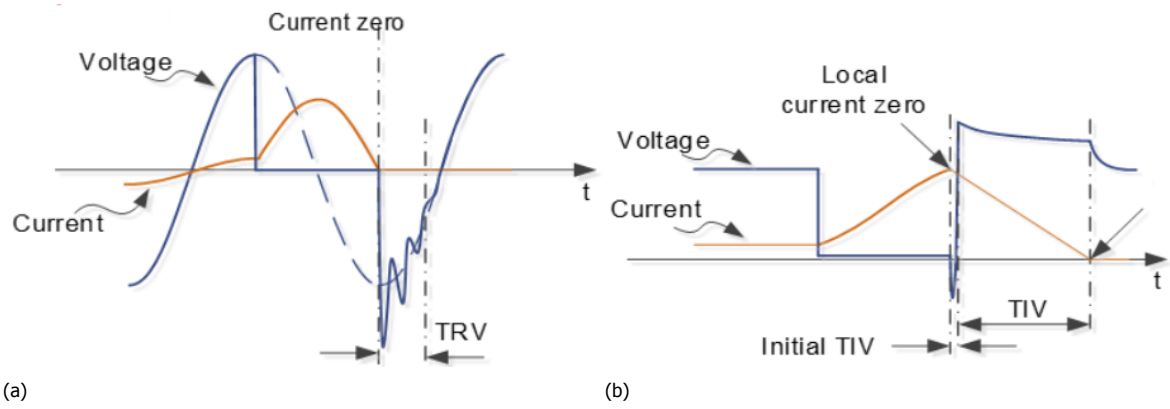



Figure 1.2: Current interruption in (a) AC and (b) DC breaker [14]

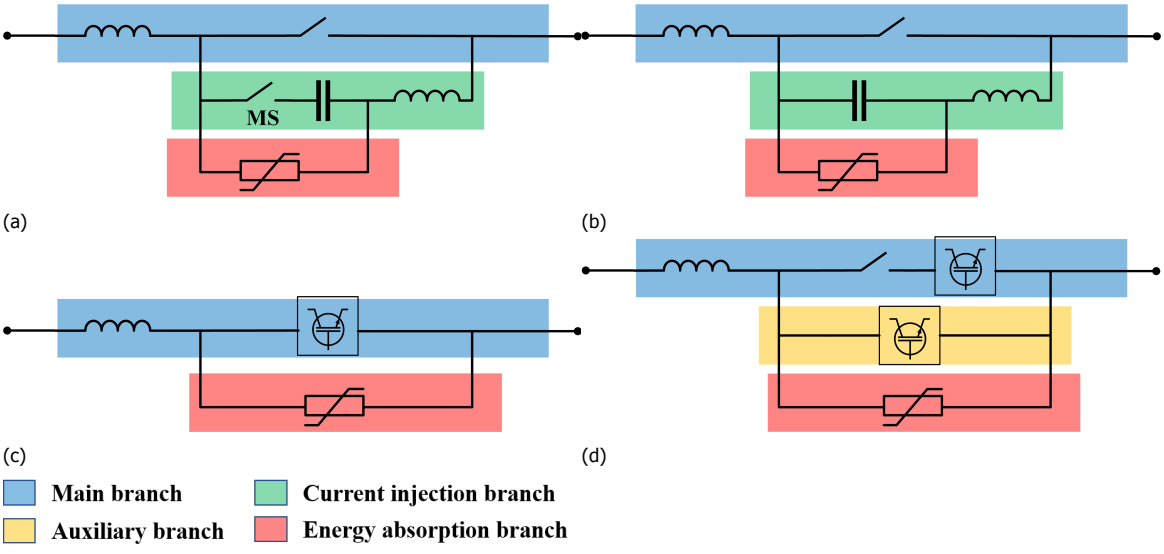



Figure 1.3: DC circuit breaker topologies of (a) Passive mechanical (b)Active mechanical (c) Solid-state and (d) Hybrid

network, line inductance of OHL and cable are not demagnetised, thus dissipating higher energy during the current interruption.

## 1.6. Classification of HVDC breakers

DC CBs are broadly classified into three types, namely, mechanical, solid-state and hybrid DC CB [14, 15]. In mechanical DC CB, Series RLC resonant circuit is used to create artificial zero crossings which ultimately interrupt fault current. The mechanical DC CB is further classified into the active and passive mechanical DC CB. Difference between active and passive DC CB is the presence of initial voltage across the capacitor. In the active mechanical DC CB, the capacitor is pre-charged, and the RLC circuit is closed with the help of a fast-acting switch during fault interruption. Whereas in passive mechanical DC CB, the capacitor is not- precharge, and it is always in parallel with the main branch, as shown in the figure 1.3. Among the mechanical DC CBs, the active type is faster as fault interruption is achieved between 5 ms to 8 ms [14]. Whereas the time required by the passive type to interrupt the fault is between 20 - 40 ms [14].

Among all the DC CB, the Solid-state breaker is fastest with fault interruption within 1 ms [15]. The Solid-state consists of a cascaded connection of semiconductor devices to increase the voltage withstand capability. It consists of two main branches and an energy absorption branch. Both the main branches are responsible for bi-directional interruption of fault current. Each branch consists of

series-connected semiconductor valve with a diode which prevents simultaneous conduction of both main branches. During the fault, the main branch is triggered, which will produce higher resistance and commute the fault current into energy absorption branch. As a result of this commutation, the fault is interrupted. Unlike mechanical, there is no arcing during fault interruption in the Solid-state. Despite the faster operation, it cannot be recommended for systems involving high voltages due to high on-state losses in the main branches and also due to the limitations on the voltage rating of semiconductor devices. Thus, the Solid-state CB are prevalent in the lower voltage and medium voltage DC system.

The Hybrid HVDC circuit breaker is the combination of the mechanical switch(es) and power electronics devices. Thus it has faster speed and lower on-state losses. Over the years, different concepts of the Hybrid breaker are presented. However, all concept has three common branches [10, 16]. The main branch consists of a mechanical switch in conjunction with a power electronic switch(es). This branch is always connected during normal operation. The auxiliary branch consists of series-connected power electronic switches which provide lower impedance than the main branch during commutation. The energy absorption branch consists of a surge arrester which absorbs the energy after commutation from the auxiliary branch, while producing a higher counter voltage across the DC CB. In hybrid DC CB, the fault current interruption occurs within 5 ms [14].

In recent years, a new DC breaker concept has been proposed and demonstrated which is known as voltage source converter assisted resonant current (VARC) DC CB. VARC DC CB makes use of a voltage source converter (VSC) along with a resonating series circuit to create high-frequency growing injected current oscillation in vacuum interrupter.

## 1.7. Motivation

As discussed in the previous section, the DC CB is an important component in the MTDC network and plays a key role in the future energy transition. The past decade has seen rapid development in HVDC circuit breaker technologies for MTDC networks. The performance of the DC CB has been studied by researchers using experiments and EMTDC simulations. The majority of these studies are performed considering the ideal operation of DC CB. However, previous studies on DC CB have not dealt with re-strike and re-ignition in vacuum interrupters.

More than 75% of DC CB size comprises of the surge arrester (SA). Although some research has been carried out on SA, only two have attempted to investigate the estimation of multi-column SA. However, far too little attention has been paid to the effect of circuit and system parameters on the number of SAs and the breaker performance.

Furthermore, several different HVDC CB technologies are emerging as a solution for the protection of MTDC networks. There is a need for co-ordinative operation between different types of DC CBs within the network.

Moreover, for the system level studies, the detailed model of DC CB is not recommended due to higher computational cost. Hence, there is a need for an average model to mitigate this problem without compromising the accuracy of the results

## 1.8. Research objectives

The main objective of this thesis is to analyse the technical performance of two different DC CB technology; namely, VARC and Active current injected mechanical DC CB in benchmark and MTDC networks. This objective is achieved by :

- Modelling of VARC and mechanical DC CB in PSCAD/EMTDC (Power Systems Computer Aided Design) software, an Electromagnetic transient program (EMTP) for MTDC network.
- Analysing the effect of restrike at different time instants in a scaled model of DC CB for MTDC network.
- Investigating the effect of network and circuit parameters on the current, voltage and energy absorbed by breakers
- Investigating the required number of multi-column surge arresters considering various scenarios.

Another objective is to determine the co-ordinative performance of different DC CB technologies in Two MTDC networks. And later, comparison of a detailed and average model of DC CB in MTDC network.

## 1.9. Outline of Thesis

This thesis report is divided into eight chapters. Chapter 1 gives a brief overview on the background of HVDC system and HVDC technologies, along with motivation and research objective of this thesis. For an accurate and reliable study of breaker performance, a detailed model of DC CB is essential due to the absence of an experimental setup. The modelling of VARC and mechanical DC CBs are addressed in Chapter 2 and Chapter 3 respectively. In addition, suitable scaling topologies for MTDC are explained in these chapters

The breaker's re-strike is crucial as it determines the technical performance of the DC CB. Moreover, the technical performance of DC CB during re-strike differs for different DC CB technologies and scaling topologies. Thus, the performance of DC CB during re-strike is analyzed in chapter 4. In addition, a re-strike during rise of TIV and fault current suppression time are also explored and discussed in Chapter 4. Furthermore, the effect of non-linear surge arrester resistance is also explained. During a fault in an HVDC system, a large amount of energy has to be absorbed by the DC CB. A Mega joules amount of energy depends upon various parameters. The energy dependence of these parameters are discussed in chapter 5, along with the estimation of number of multi-column SA. In addition, the study of current and voltage stress across the main branch and the energy absorption branch is presented in Chapter 5. Since, several different HVDC CB technologies are emerging as a solution for the protection of offshore MTDC networks. There is a need for co-ordinative operation between different types of DC CBs. In Chapter 6, two typical types of DC CBs that can be implemented in two 4-terminal MTDC networks are discussed. The simulations are performed in an EMT environment using PSCAD software. Here care has been taken to consider operation time, interruption capability and interruption characteristics.

For overall system studies, an relaxation can be given on model details. However, this model should provide similar results with minimum error. Thus, chapter 7 deals with the modelling and comparison of the detailed and average model for both technologies. Finally, Chapter 8 present the conclusions.

## 1.10. Contribution of the thesis

The main contribution of this thesis is to analyse the performance of the VARC and active current injection Mechanical DC CB in the test circuit and the MTDC network considering various scenarios like re-strike, re-ignition; and variation in the system and circuit parameters on the EMTDC platform. The optimum number of the multi-column surge arrester is derived based on the worst case scenario. Furthermore, the co-ordinative performance between these two DC CBs is analyzed, with generalised selection methodology for DC CB in MTDC network. Also, an average model for both DC CB technologies are derived for grid-level studies and model verification is performed using two typical case studies.

1

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# 2

# Modelling and Scaling VARC DC CB

*The presence of the DC breaker promotes the reliability of the MTDC. Over years different breaker technologies have emerged. Amongst the recently developed concepts, we have the voltage source converter assisted resonant current (VARC) DC CB. In this chapter, the working and modelling of VARC DC CB are discussed by considering the various parasitic components. Furthermore, the discussion on the topology selection for MTDC is carried out.*

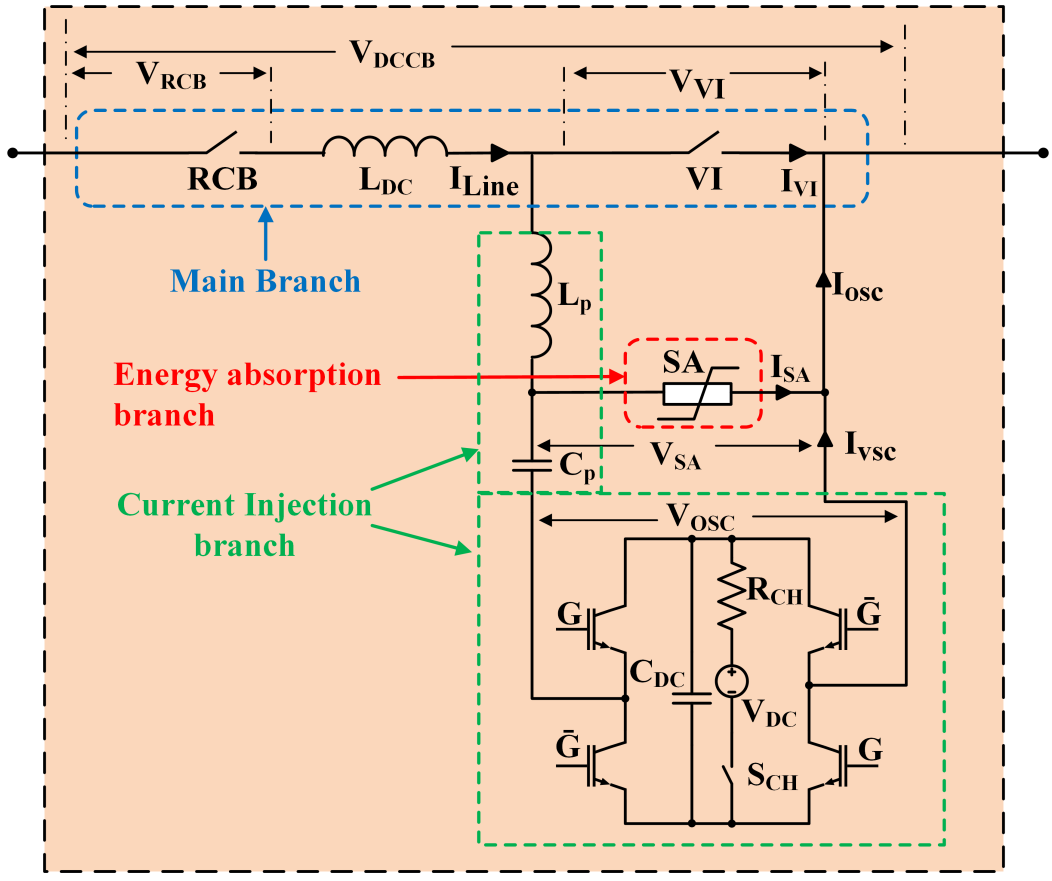


Figure 2.1: Structure of VARC DC CB [2]

## 2.1. Structure of VARC DC CB

The structure of VARC DC CB consists of three major branches, which includes the main branch, the energy absorption and the current injection branch, as shown in figure 2.1. The main branch consists of the residual current breaker (RCB), line inductor ($L_{DC}$) and Vacuum interrupter (VI). The RCB is a low current interrupting capability circuit breaker, whose primary function is to isolate the DC CB after the current interruption. The isolation is essential in order to block the leakage current in the surge arrester (SA) [1]. The RCB is modelled with an off-state resistance of $100 \times 10^{15}\Omega$ and an on-state resistance of $1 \times 10^{-4}\Omega$ in PSCAD/EMTDC environment. Here, the current chopping limit is set to 1 A.

The line inductor ($L_{DC}$) limits the rate of rise of fault current in the DC CB. The vital component in the main branch is VI. VI has higher interrupting capability; hence it is used in the DC breaker [3]. Thomson's coil (TC) serves as the driving mechanism for the VI. TC produces tremendous driving force within a fraction of milliseconds, results in the quick recovery of the dielectric strength of VI, thereby improving the operating time of the breaker.

The current injection branch consists of a voltage source converter (VSC), an oscillating inductor ($L_P$) and capacitor ($C_P$). VSC comprises of two sections, one is the charging circuit, which consists of a charging switch ($S_{CH}$), charging resistance ($R_{CH}$) and a DC source ($V_{DC}$); and Section 2 is the energy storing capacitor ($C_{DC}$). Based on the triggering of the IGBTs ($G$ or $\bar{G}$ ), the voltage ($V_{OSC}$) toggles between $\pm V_{DC}$ and this leads to injection of an oscillatory current ($I_{VSC}$) in the VI. $L_P$ and $C_P$ determine the frequency of $I_{VSC}$. Unlike the mechanical DC CB, the initial voltage across the $C_P$ is zero [2].

The modelling of VI is subject to the type of study conducted. Hence, in the case of steady-state studies, the VI can be modelled as a simple switch with on and off states. However, in the case of fast transient studies, VI model should provide the information of arcing voltage and resistance.

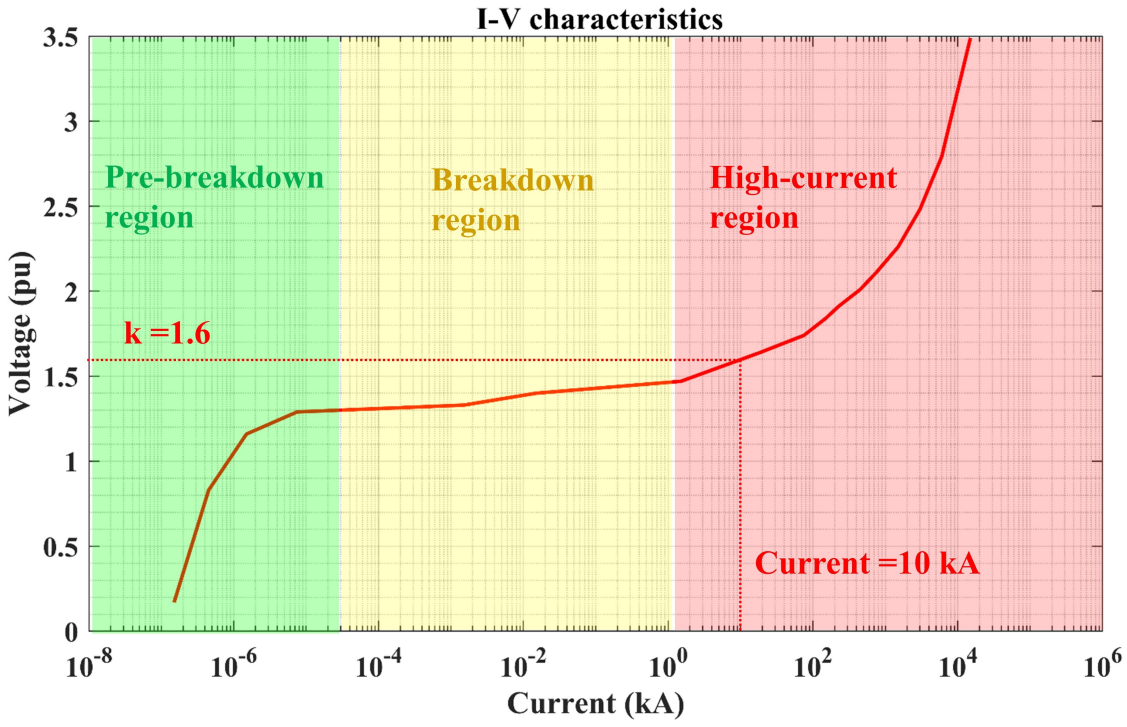


Figure 2.2: I-V characteristic of Surge arrester

This model is discussed in the next chapter.

The Energy absorption branch primarily consists of the SA, unlike in the AC network, SA in DC CB is used to absorb the energy during the current interruption. The characteristics of SA is expressed in terms of $V/mm$ v/s $A/mm^2$. This relationship between the electric field and current density of SA gives an insight into the development of metal oxide material, which makes up a SA. Alternatively, the characteristics can also be represented in terms of voltage and current for manufacturers and utility application. [4].

The SA is modelled as a piece-wise linear resistance (with voltage and current characteristic defined by the figure 2.2 in PSCAD/EMTDC environment). Figure 2.2 shows the typical aggregated I-V characteristics of SA used in this thesis. The characteristics of SA is divided into three regions, namely pre-breakdown region, breakdown region and high-current region.

The current in the pre-breakdown region is highly dependent on the temperature. Hence, the rise in temperature during the application of a voltage in this region can lead to the thermal breakdown of the material [5]. However, in the VARC DC CB, the initial voltage across the SA is zero. Hence it has a lower leakage current. In the breakdown region, the dependence of the resistivity on the temperature is very small, and the nature of characteristics is highly non-linear in the high-current region. The breakdown and high-current regions are essential in the designing of DC CB due to the non-linear nature of characteristics in these regions. For example, for a fault current of 10 kA, the voltage across SA rises to 1.6 times the rated voltage of SA. However, with an increase in current, the voltage across SA hardly exhibits any change. Furthermore, for a steady-state current of 2 kA, the voltage across SA drops below 1.6 times the rated voltage.

## 2.2. Operating sequence of VARC DC CB

Figure 2.3 shows the operating principle of VARC DC CB and is explained as follows [2]:

During the pre-fault period, the VSC's energy storage capacitor ($C_{DC}$) is charged to a lower voltage level ($V_{DC}$) by the charging circuit. Three events occur during pre-fault and fault neutralization time. Firstly, the occurrence of fault at instant $t_1$ causes rise of fault current. This rate of rise is limited by

the line inductor ($L_{DC}$). The trip signal is sent to the VARC DC CB at $t_2$. Secondly, during $t_2 - t_{2a}$ , the contact of the VI is separated by the ultra-fast Thomson's drive when the trip signal at $t_2$ is received. At $t_{2a}$, the separation between the contacts of the VI reaches an adequate distance which can withstand the TIV. The last event during pre-fault and fault neutralization time is the activation of the VSC at $t_{2a}$. During this interval, the oscillating current is produced. The amplitude of this current is increased at every half cycle. This process is continued until a zero crossing in the VI.

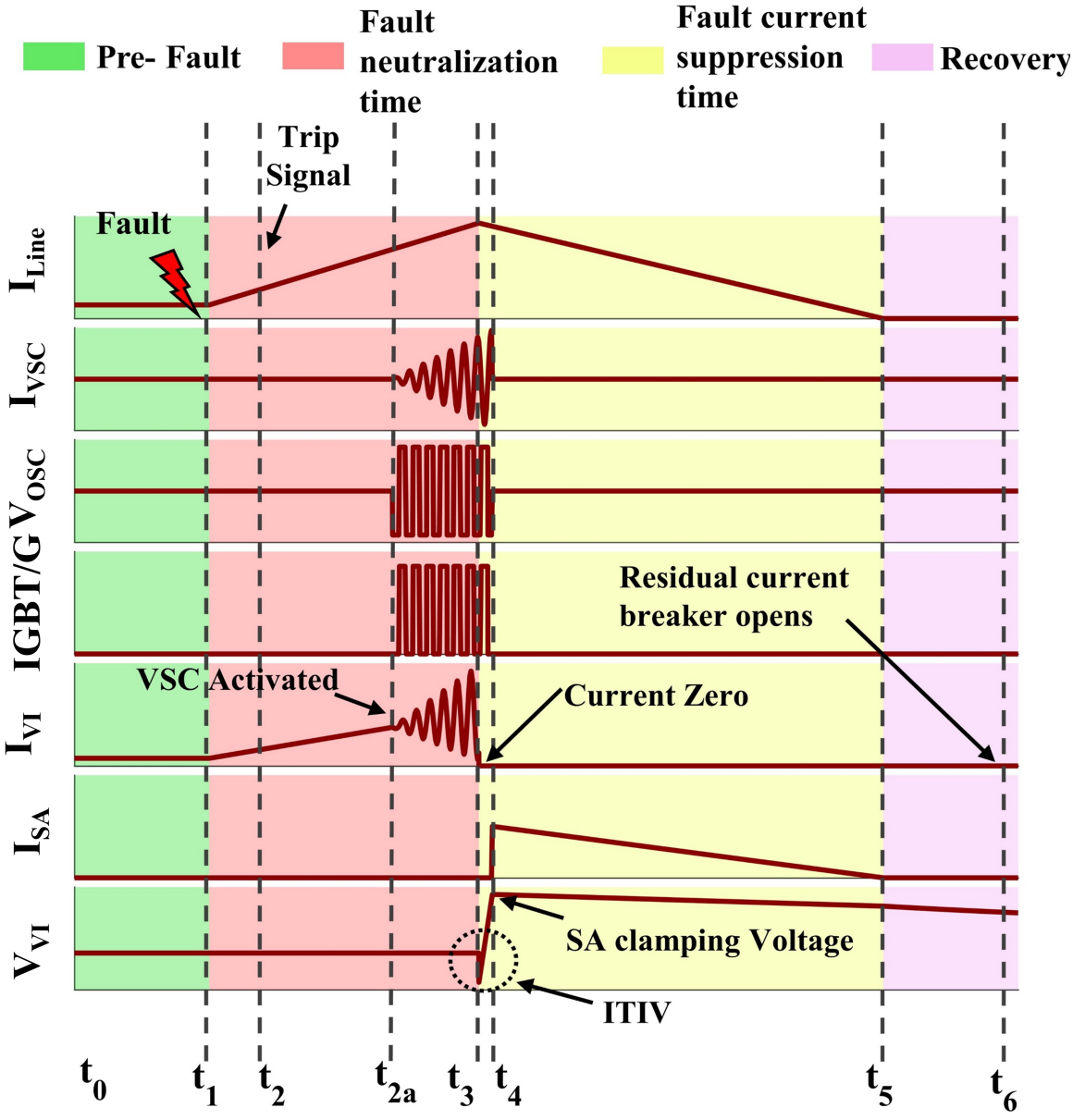


Figure 2.3: Current and Voltage waveform in VARC DC CB

At the beginning of the fault current suppression time i.e. at instant $t_3$, VI stops conducting, and the fault current is commutated to the current injection branch. As the VI is connected in parallel with the current injection branch, the voltage across the VI at $t_3$ is equal to the remaining voltage of the current injection branch capacitor and is known as initial transient interruption voltage (ITIV). During $t_3 - t_4$, the fault current charges the current injection branch capacitor $C_P$ until its voltage reaches the clamping voltage of SA at $t_4$. The SA is clamped at instant $t_5$, and now the fault current is commuted into the energy absorption branch. The SA is latched until the current through it does

not fall to zero, i.e. at time instant $t_5$. After the fault current interruption, some leakage current may still exist in the system, as well as a low-frequency interaction between the capacitor in the circuit breaker and the inductor connected in series with the breaker. The residual circuit breaker is opened at $t_6$ to clear the leakage current and separate the main breaker circuit from the grid.



## 2.3. Selection of the oscillating inductor and capacitor

The amplitude of the injected current in VARC DC CB increases after each reversal of $V_{OSC}$. The injected current ($I_{OSC}$) is given by [2]

$$I_{OSC}(t) = I_{pk}\sin(\omega t) \tag{2.1}$$

$$I_{pk} = V_{DC}(2N-1) \times \sqrt{\frac{C_{eq}}{L_P}} \tag{2.2}$$

$$\omega = \frac{1}{\sqrt{L_P C_{eq}}} \tag{2.3}$$

$$C_{eq} = \frac{C_P C_{DC}}{C_P + C_{DC}} \tag{2.4}$$

$$C_{eq} = \frac{C_P C_{DC}}{C_P + C_{DC}} \tag{2.5}$$

Where $N$ is the number of half-cycles, $L_P$ and $C_P$ are oscillating inductor and capacitor, and $V_{DC}$ indicates the pre-charged voltage across the $C_{DC}$. The high-frequency current interruption in the vacuum breaker depends upon the value of the $\frac{di}{dt}$ at current zero [6]. The critical range of the $\frac{di}{dt}$ at current zero is between 150 – 1000 A/µs for AC CBs [7]. Due to an artificial current zero in DC breaker, the slope at current zero must be within this range, for the current interruption. Assuming 1000 A/µs as an upper limit, the values for $L_P$ and $C_P$ are calculated in the following manner:

After differentiating (2.2) we get

$$\frac{\mathrm{d}I_{LC}(t)}{\mathrm{d}t} = I_{pk}\omega\cos(\omega t) \tag{2.6}$$

At current zero i.e ωt= $\pi$ , we get

$$\frac{\mathrm{d}I_{LC}(t)}{\mathrm{d}t} = -I_{pk} \times \frac{1}{\sqrt{L_P C_{eq}}} \tag{2.7}$$

Making use of the critical limit of 1000 A/µs at current zero, we deduce the upper bound equation

$$1000\ A/\mu s > \left|(dI_L C(t))/dt\right| = (2N-1) \times V_{DC}/L_P \tag{2.8}$$

The frequency of oscillation as suggested in [8] is 10 kHz. In VARC, the total voltage rating of the semiconductor devices is four times the $V_{DC}$. Hence, the rating of each IGBT Switch is equal to the charging voltage [8]. The development of the press pack IGBT's for HVDC and FACTs devices have enabled higher voltage and current levels. The demonstrated press pack IGBT with a rating of 4.5 kV and 1.5 kA shows higher robustness during the test [9]. Hence it can be safely assumed that the 10kV Voltage source in VSC can be utilised by an appropriate series and parallel combination of the press pack IGBTs. Furthermore, the number of half-cycles is assumed to be 6.5. Considering all the above assumptions, the $L_P$ should be higher than 120 µH. Thus, we selected $L_P$ value as 127 µH for entire project. Similarly, the $C_P$ can be calculated from the frequency and $L_P$ as follows: $C_P = \frac{1}{(2\pi \times 10\ kHz)^2 \times 127\ \mu H} \approx 2\ \mu F$.

## 2.4. Grading and Parasitic component

The grading and parasitic component of the 80 kV module (figure 2.4 (d)) is described in table 2.1. The value of the capacitance between the terminal of the module to the ground is determined practically [2]. Similarly, the value for stray resistance, inductance and capacitance across the VI interrupter is referred from [6, 10]. The parasitic capacitance across the SA is calculated based on the rated current and clamping voltage, as discussed in the [10]. Considering the rated fault current of 10 kA, energy absorbed is 80 MJ and with the consequent operation of breaker, this energy may rise to 160 MJ. As in the [10], the rated system voltage is 320 kV, and the number of modules are 4. The energy absorbed by each module will be 40 MJ. Using the formula from [10], we can compute the values of parasitic capacitance across SA:

$$C_{X1} = \frac{A}{4.42 \times 10^{-3}} \frac{23 \times 10^{-3}}{H}\ nF \tag{2.9}$$

$$H = \frac{V_{clamp}}{5.75 \times 10^{3}} \times 23 \times 10^{-3}\ m \tag{2.10}$$

$$A = \frac{E}{H \times 200 \times 10^{6}}\ m^2 \tag{2.11}$$

Where $V_{clamp}$ is the voltage imposed by the SA during the fault current suppression. And $E$ is the energy absorbed by SA. Upon substituting $V_{clamp}$ = 130 kV and $E$ = 40 MJ in (2.9), (2.10) and (2.11), we get $C_{X1}$ =3.85 nF.

Table 2.1: Grading and the parasitic component of the 80kV VARC module

| Parameter | Label | Unit | Value |
|---|---|---|---|
| Series RLC branch resistance across vacuum interrupter | $R_{X3}$ | Ω | 50 |
| Series RLC branch inductance across vacuum interrupter | $L_{X3}$ | nH | 50 |
| Series RLC branch capacitance across vacuum interrupter | $C_{X3}$ | pF | 200 |
| Capacitance across Surge arrester (SA) | $C_{X1}$ | nF | 3.85 |
| Capacitance between module terminal to ground | $C_{X2}$ | pF | 15 |
| Stray Resistance | $R_1$ | mΩ | 50 |
| Grading Resistance | $R_g$ | MΩ | 40 |
| Grading Capacitance | $C_g$ | pF | 50 |

## 2.5. Scaling of VARC DC CB for MTDC network

The separation between the VI's contacts after a certain point (distance) doesn't result in any increase in the dielectric strength. Similarly, it makes the design of DC CB uneconomical. In order to implement the DC CB in MTDC network, it has to be scaled. The scaling is done based on system voltage. The scaling of the DC CB can be carried out in two ways; i) by the series connection of the VI and ii) by modular topology. However, Modular topology is adopted for VARC DC CB in MTDC network [2].

Provided reference, topology (a) and (c) showed better performance in terms of Voltage sharing among the modules. Hence, based on this fact, the topology (a) is selected for the MTDC network analysis in this thesis.

Two MTDC systems with voltage ratings of 320 kV and 520 kV (respectively) are chosen for performance study. Thus, the number of modules (with a rating of 80 kV) are 4 and 7 respectively. It should be noted that extra modules can be used for redundancy in-case of module(s) failure.

## 2.6. Brief summary and Discussions

The VARC DC CB exhibits higher interruption performance during the steady-state and also as at times of faults due to successive increase of injected current in VI after each half cycle by the current

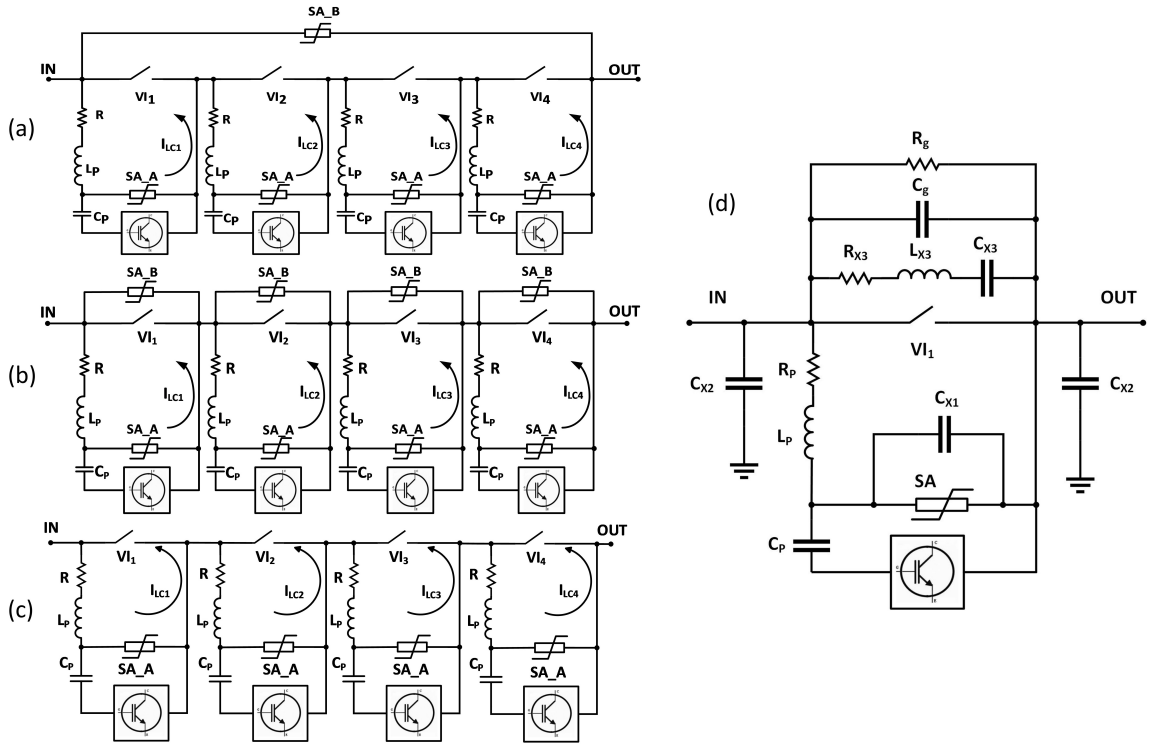


Figure 2.4: (a) - (c) Different Topologies for EHV of VARC DC CB [2] and (d) parasitic components in the VARC module

injection branch. The implementation of Thomson's coil in VARC DC CB results into fault current interruption within a time span of 3 ms, thus making it ideal for the DC grid application.

In summary, selection of the oscillating inductor and capacitor was based on the di/dt at the current zero. For a 525 kV system, the oscillating inductor and capacitor for each module was 127 $\mu$H and 2 $\mu$F respectively. Moreover, semiconductor switching devices present in the VSC of DC CB also determine the frequency of the injected current.

The modelled VARC DC CB consists of parasitic resistance, capacitance and inductance of surge arrester and a vacuum interrupter with grading resistance and capacitance. The developed model can be used to analyse the stress in the critical components of VARC with a higher degree of accuracy. Besides, this model can be used for re-strike and re-ignition performance analysis along with fast transient analysis. Furthermore, to implement VARC DC CB in multi-terminal HVDC grid, the modular topology was selected. The rating of each module was chosen to be 80 kV. The number of modules to be connected in series depends on the system voltage. Hence, for a 525 kV system, the number of modules required will be seven; whereas for 320 kV system number of modules will be four.

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# 3

# Modelling and scaling of Active current injected Mechanical DC CB

*The mechanical DC CB has been revamped to active DC CB. It is considered to be a less sophisticated breaker among the other technologies. Due to lower operational time with higher fault current and voltage rating of Active current injected Mechanical DC CB, make it an ideal choice for MTDC application. In this chapter, the operating principle and modelling of mechanical DC CB with due considerations to different parasitic and grading components are discussed. Furthermore, the scaling of mechanical DC CB for a 320 kV and a 525 kV system is carried out using appropriate topology.*

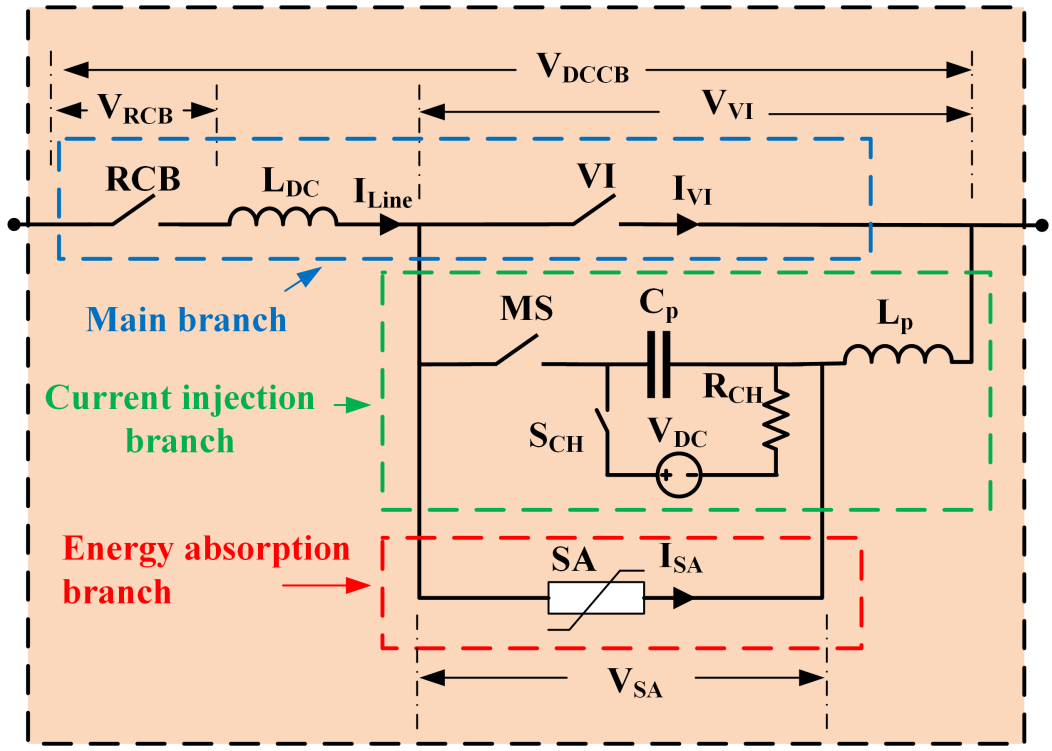


Figure 3.1: Structure of Active current injected mechanical DC CB [4]

## 3.1. Structure of Mechanical DC CB

Similar to the VARC DC CB, the structure of Active current injected mechanical DC CB consists of three major branches, main branch, energy absorption branch and the current injection branch, as shown by figure 3.1 [1–3]. The main branch consists of the residual current breaker (RCB), line inductor ($L_{DC}$) and vacuum interrupter (VI). The RCB is a circuit breaker with lower interrupting capability, whose primary functions is to isolate the DC CB after the current interruption. The isolation is essential in order to block the leakage current in the surge arrester (SA), thus preventing the damage to SA in the long run. The line inductor ($L_{DC}$) limits the rate of rise of fault current in the DC CB. The vital component of the main branch is VI. The VI has a higher number of operations which range from 10000 to 30000 operations. It can interrupt current within a few microseconds and is able to withstand higher voltage within a fraction of microseconds after the current zero-crossing. Hence it is used in the DC breaker. Thomson's coil (TC) serves as the driving mechanism for VI.

The current injection branch consists of a charging circuit and oscillating inductor ($L_P$) and capacitor ($C_P$). The charging circuit consists of a charging switch ($S_{CH}$), charging resistance ($R_{CH}$) and DC source ($V_{DC}$). However, the DC source ($V_{DC}$) represents the system voltage. Upon triggering of the Making Switch ($MS$), pre-charged capacitor ($C_P$) injects oscillatory current ($I_{OSC}$) in the VI, thus creating current zero. The $L_P$ and $C_P$ determine the frequency of $I_{OSC}$. In the mechanical DC CB, the polarity of the initial voltage across the $C_P$ is critical. The Energy absorption branch primarily consists of SA, unlike in the AC network, SA is used to absorb a large amount of energy during the interruption. The I-V characteristics and modelling of the SA are similar to that of SA in VARC DC CB.

## 3.2. Operating sequence of Mechanical DC CB

Figure 3.2 show the operating principle of Mechanical DC CB and is explained as follows :

During the pre-fault period, the $C_P$ is charged to the system voltage by the charging circuit. Two events occur during the Pre-fault and fault neutralization time. First, the occurrence of fault at instant $t_1$ causes rise of fault current, and the rate of rise of fault current is limited by the line inductor ($L_{DC}$).

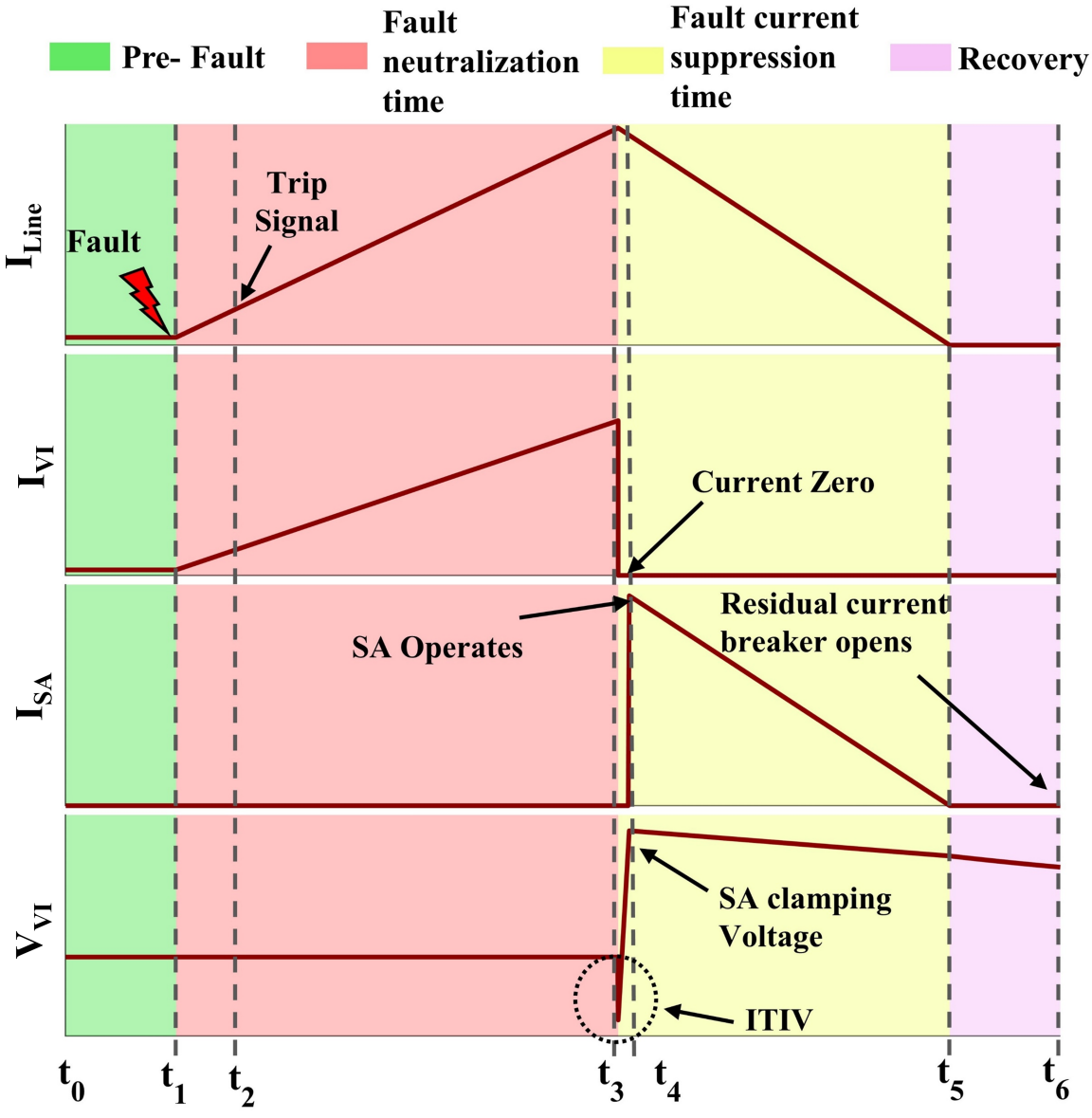


Figure 3.2: Current and Voltage waveform in active current injected mechanical DC CB

The trip signal is sent to the Mechanical DC CB at $t_2$. During $t_2 - t_3$, the contact of VI is separated by ultra-fast Thomson's drive when the trip signal is received at $t_2$. At the beginning of the fault current suppression time i.e at instant $t_3$, the separation between the contacts of the VI reaches an adequate distance which can withstand the TIV and the making switch (MS) is closed, which result in zero crossings in the VI. Thus, VI stops conducting, and the fault current is commutated to the current injection branch. As the VI is connected in parallel with the current injection branch, the voltage across the VI at $t_3$ is equal to the remaining voltage of the current injection branch capacitor and is known as initial transient interruption voltage (ITIV).

During $t_3 - t_4$, the fault current charges the current injection branch capacitor, until its voltage reaches the clamping voltage of SA at $t_4$. As the SA is clamped, the fault current is commuted into the energy absorption branch. The SA is latched until the SA current does not fall to zero, i.e. at time instant $t_5$. After the fault current interruption, some leakage current may exist in the DC CB, as well as a low-frequency interaction between the capacitor of the DC CB and the inductor connected in series with the breaker. The residual circuit breaker is opened at $t_6$ to clear the leakage current and separate the main breaker circuit from the grid.

## 3.3. Selection of the oscillating inductor and capacitor

As discussed in the modelling of VARC DC CB, it is essential to choose the appropriate value for the $L_P$ and $C_P$. Due to a different operating principle of DC CB, the interruption at first current zero not only depends upon the value of $L_P$ and $C_P$ value but also depends upon the amplitude of the current in VI at the end of fault neutralisation time [1, 5]. Similar to VARC DC CB, the selection of $L_P$ and $C_P$ is carried out based on the critical $\frac{di}{dt}$ at current zero. Hence, considering the assumption of critical $\frac{di}{dt}$ at current zero to be 1000 A/µs, $L_P$ and $C_P$ are calculated as follows:

The current injected by the injection branch is given as

$$I_{OSC}(t) = I_{pk} \sin(\omega t) \tag{3.1}$$

$$I_{pk} = V_{DC}(0) \times \sqrt{\frac{C_P}{L_P}} \tag{3.2}$$

Where $V_{DC}(0)$ is the initial voltage across the $C_P$. Upon differentiating w.r.t time and utilising the upper bound as critical $\frac{di}{dt}$ at current zero i.e. 1000 A/µs we get,

$$1000A/\ \mu s > \left|\frac{\mathrm{d}I_{OSC}(t)}{\mathrm{d}t}\right| = V_{DC}L_P \tag{3.3}$$

From (3.3) it can be seen that voltage across the $C_P$ plays a vital role in determining the value of $L_P$. However, the voltage across the $C_P$ is determined by the topology implemented for scaling. Hence, for different voltage levels, we can compute the range of values for $L_P$ as summarized in table 3.1.

Table 3.1: Values of $L_P$ for different initial voltage across $C_P$

| **Voltage Level** | **$L_P$** |
|---|---|
| 80 kV ( one module ) | >80 $\mu$H |
| 320 kV | >320 $\mu$H |
| 525 kV | >525 $\mu$H |

Similarly, the value of $C_P$ is computed by equating the maximum fault current and the peak value of $I_{OSC}(t)$. The maximum value of fault current for mechanical DC CB is taken to be 16 kA [6]. However, a safety factor of 2 is considered. Thus, $C_P$ is defined as

$$C_P = \left(\frac{2 \times 16\ kA}{V_C(0)}\right)^2 \times L_P \tag{3.4}$$

Similar to $L_P$, we can obtain a bound limit to values of $C_P$ for different initial voltage across the $C_P$ as summarised in table 3.4

Table 3.2: Values of $C_P$ for different initial voltage across $C_P$

| **Voltage Level** | **$C_P$** |
|---|---|
| 80 kV ( one module ) | >12.8 $\mu$F |
| 320 kV | >3.2 $\mu$F |
| 525 kV | >1.95 $\mu$F |

Hence, considering series-connected VI topology and system voltage of 525 kV, the chosen value of $C_P$ is 2.2 µF, and the corresponding value of $L_P$ is 600 $\mu$H. Also, at higher voltages, a lower value of capacitance is preferred.

## 3.4. Scaling of Mechanical DC CB for MTDC network

As discussed in the preceding section, the selection of topology for scaling is crucial in term of oscillatory circuit sizing. Similar to the VARC DC CB, the Mechanical DC CB can be utilised into EHV by connecting VI in series or by resorting to modular topology. In modular topology, we have 80 kV modules similar to VARC DC CB connected in series. In this topology, as the applied voltage is 80 kV across the $C_P$, a trade-off has to be made between the inductor and capacitor sizing and also, it is challenging to charge a capacitor with voltage level lower than system voltage.

On the other hand in series-connected VIs, the system voltage can be directly applied across the $C_P$. In this thesis, the series-connected VIs approach is selected for the mechanical DC CB. The number of VIs depends upon the system voltage and rating of VI. Hence, for the 320 kV, four series-connected VIs of 80 kV rating are required. Similarly, for 525 kV, seven series-connected VIs are needed, as illustrated in figure 3.3.

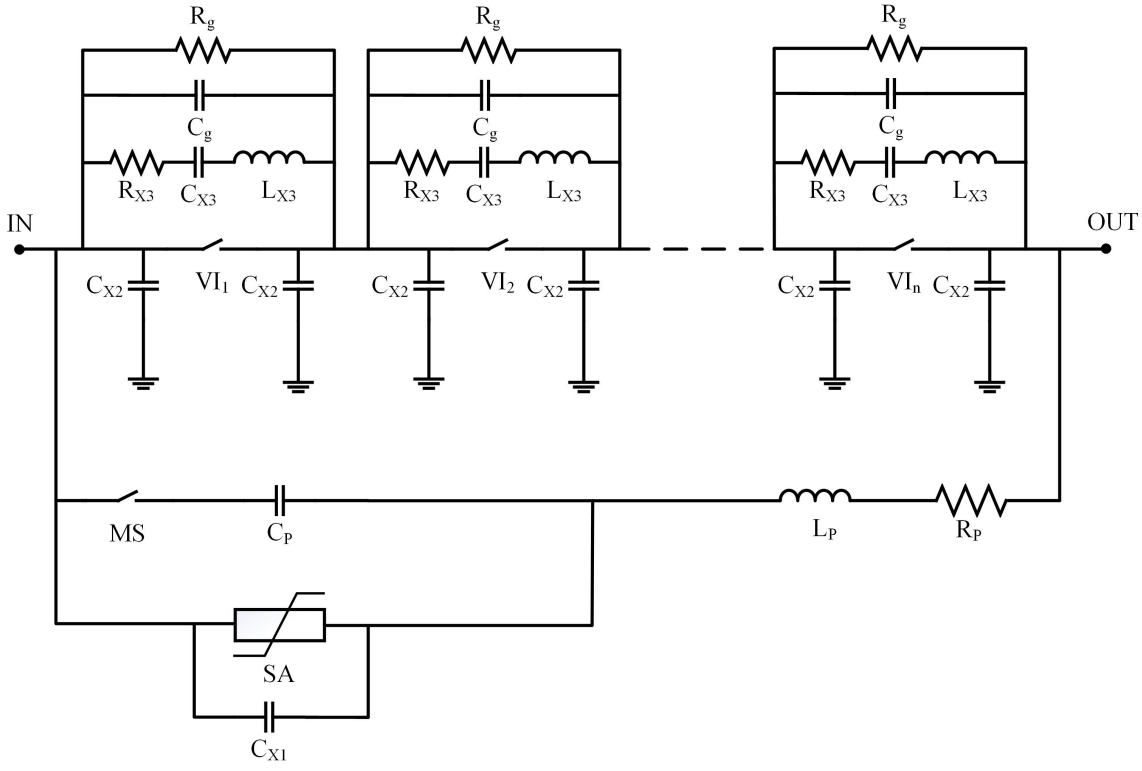


Figure 3.3: Scaled topology of mechanical DC CB for Extra High Voltage (EHV)

## 3.5. Grading and Parasitic component

The rating of the VI is the same as that of VARC DC CB. Thus, the $R_{X3}$, $L_{X3}$ and $C_{X3}$ are similar and listed in table 2.1. Similarly, the capacitance across the SA can be calculated using (2.9),(2.10) and (2.11) and upon substituting the value for $V_{clamp} = 840\ kV$ and $E = 140\ MJ$ value of $C_{X1}$ is $0.322\ nF$.

Due to the series connection of VIs, individual VI experience variation in voltage during fast transients than the modular topology. Similar to AC CB, grading capacitance is used for uniform voltage distribution across individual VIs. The effect of grading can be analysed by transforming figure 3.3 into a simple ladder network of capacitance, as shown in figure 3.4. Without any grading element, a higher voltage will be shared amongst the first VI in comparison with the VI, as shown in figure 3.5 during the transient behaviour.

The figure also reflects the effect of the VI terminal to ground capacitance ($C_{X2}$) on the volt-

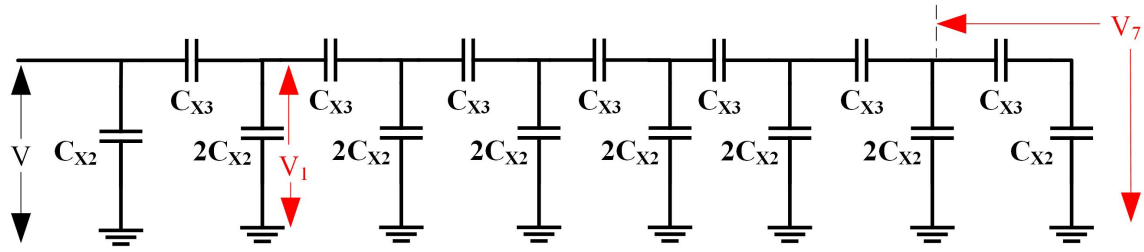


Figure 3.4: Capacitative ladder network representation of 525 kV mechanical DC CB

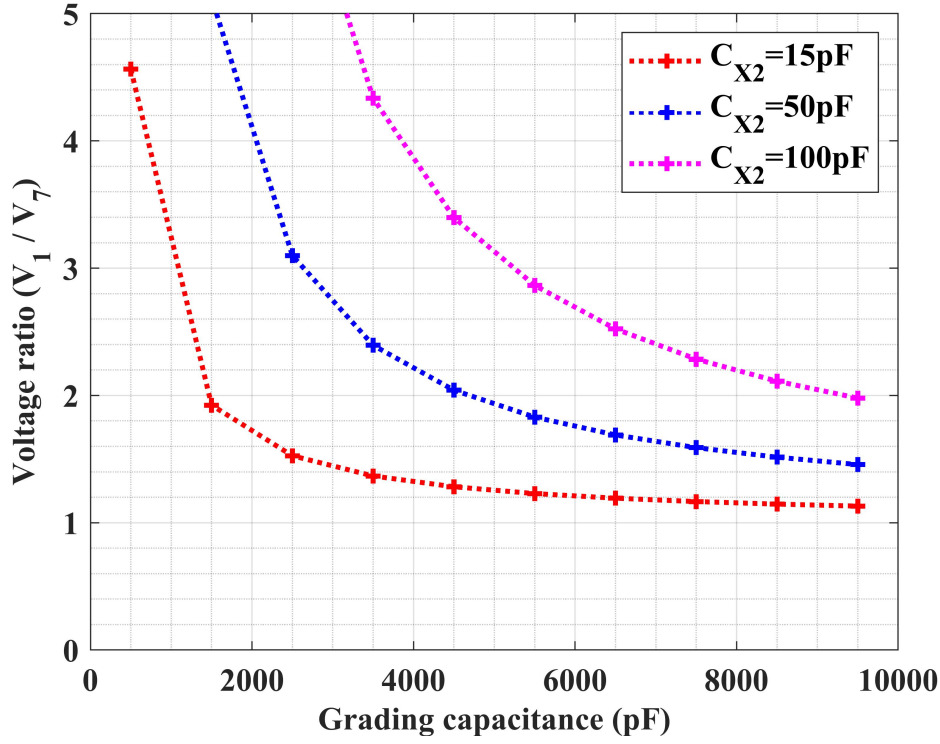


Figure 3.5: Effect of grading capacitance on the voltage distribution between first and last VI for three typical value of VI terminal to ground capacitance.

Table 3.3: Grading and the parasitic component of the 525 kV Mechanical DC CB

| Parameter | Label | Unit | Value |
|---|---|---|---|
| Series RLC branch resistance across vacuum interrupter | $R_{X3}$ | Ω | 50 |
| Series RLC branch inductance across vacuum interrupter | $L_{X3}$ | nH | 50 |
| Series RLC branch capacitance across vacuum interrupter | $C_{X3}$ | pF | 200 |
| Capacitance across Surge arrester (SA) | $C_{X1}$ | nF | 0.322 |
| Capacitance between VI terminal to ground | $C_{X2}$ | pF | 15 |
| Stray Resistance | $R_1$ | mΩ | 50 |
| Grading Resistance | $R_g$ | MΩ | 40 |
| Grading Capacitance | $C_g$ | pF | 5000 |

age ratio. This capacitance depends upon the structure and placement of the DC CB [2]. Upon connecting the grading capacitance ($C_g$) across the $C_{X3}$, the voltage distribution is improved signifi-

cantly in case of $C_{X2}$ = 15 pF with grading capacitance above 5000 pF. Hence, in this thesis, for the mechanical DC CB, the value of $C_g$ and $R_g$ are 5000 pF and 40 MΩ respectively.

## 3.6. Brief summary and Discussions

Due to the absence of the semiconductor switching devices in the main branch of active current injected mechanical DC CB, the on-state losses are very low. In addition, this breaker has an operating time between 5 ms - 8 ms, which makes the application of mechanical DC CB more convenient for MTDC grids.

The modelling of active current injected mechanical DC CB was carried out by considering the parasitic components of vacuum interrupters and surge arresters. The values of inductance and capacitance were computed based on the critical limit of VI at current zero. Consequently, for 525 kV system, the values of $C_P$ was 2 $\mu$F and $L_P$ was 600 $\mu$H. Similarly, a safety factor of 2 was considered in computing the values of $C_P$ and $L_P$.

Furthermore, the series-connected VI topology was chosen for the EHV system with a cascaded connection of seven VIs (each of rating 80 kV) for a 525 kV system. Whereas for a 320 kV system, four VIs had to be connected in series. It was also observed that the grading circuit plays a vital role in determining the voltage distribution among the VIs. Moreover, the impact of the grading was higher in series-connected VIs than the modular topology.



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# 4

# Performance of DC CB under Re-strike

*In this chapter, the performance of both technologies, explained in the previous chapter, is discussed during the re-strike. The current chapter focuses on re-strike during the rise of transient interrupting voltage (TIV) and the fault suppression time. Also, the significance of the surge arrester (SA) and circuit impedance on injected current is analysed.*

## 4.1. Test system

Figure 4.1 shows the test system, with system voltage ($V_S$) of 525 kV and a source impedance of 0.1 Ω for fast transient analysis. The DC CB is mounted between the line inductor $L_{DC}$ and cable 1 . The test system consists of two cables; cable 1 is 525 kV XLPE submarine cable with a length of 1 km, and cable 2 is 525 kV XLPE submarine cable with a length of 10 km. The Frequency Dependent (Phase) model is used to represent both cables in PSCAD environment. Both cables have a surge impedance of 60.71 Ω and a waves propagation velocity of $1.76 \times 10^8\ m/s$. The parameters for the cable geometry are enlisted in figure 4.2.

The value of the $L_{DC}$ and $R_L$ are 191 mH and 262 Ω. In this system, the fault is applied at 0.1 s with fault impedance of 0.01 Ω and is resistive in nature. This fault represents the pole to pole fault at the terminal of the converter in the MTDC system. During the pre-fault, the current through the DC CB is 2 kA.



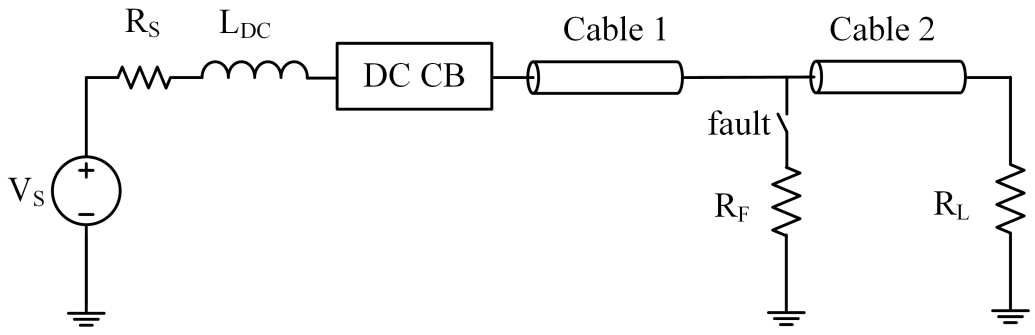



Figure 4.1: Test system for the technical performance of DC CB

In this test circuit, DC CB is replaced with VARC and Mechanical DC CB to observe the performance under re-strike. The topologies of DC CBs used are similar to the discussed topologies in section 2.5 and 3.4.

## 4.2. Re-strike in the DC CB

The re-strike due to breakdown in the DC CB arises if the vacuum interrupter(VI) is unable to withstand a voltage across it after the current zero [1] or the $\frac{di}{dt}$ at current zero is higher than the critical limit. The time of occurrence of the re-strike is crucial in terms of the energy absorbed by the SA and voltage shared by the VI. The breakdown in VI can occur at different time instances as described in [2]. If the breakdown occurs soon after the current zero, it is described as an instantaneous breakdown.

Furthermore, re-strike can be seen and experimentally verified in VI due to the Non-Sustained Disruptive Discharges (NSDD) phenomena [2, 3]. The NSDD occurs after a few milliseconds of the current interruption in VI. However, the primary objective of this chapter is to analyse the effect of breakdown on the performance of DC CB. Hence, two-time durations are considered, namely during the rise of TIV, which represents instantaneous breakdown and another is during fault current suppression time, which represents breakdown due to NSDD. These breakdowns are carried out by forced re-strike during these time intervals.

To understand the effect of re-strike due to breakdown, VI is modelled using variable resistance with parallel parasitic components. The value of the variable resistance is dependent upon the state of the VI as discussed in detail in [4]. During the arcing state, the value of the variable resistance is 80 μΩ and it is in series with the DC source. This DC source represents the arcing voltage. The dielectric strength of the VI can be determined by the cold breakdown [1] approach, which is given by

$$U_{b1}(s) = f \times s^{\alpha} \tag{4.1}$$

where $U_{b1}$ is the dielectric strength across the VI, $f$ = 30 kV [5], $s$ is gap distance (20 mm ) [6] and $\alpha$ is 0.55 [1]. The $f$ and $\alpha$ define the geometry of the co-planar profile. So, the net dielectric

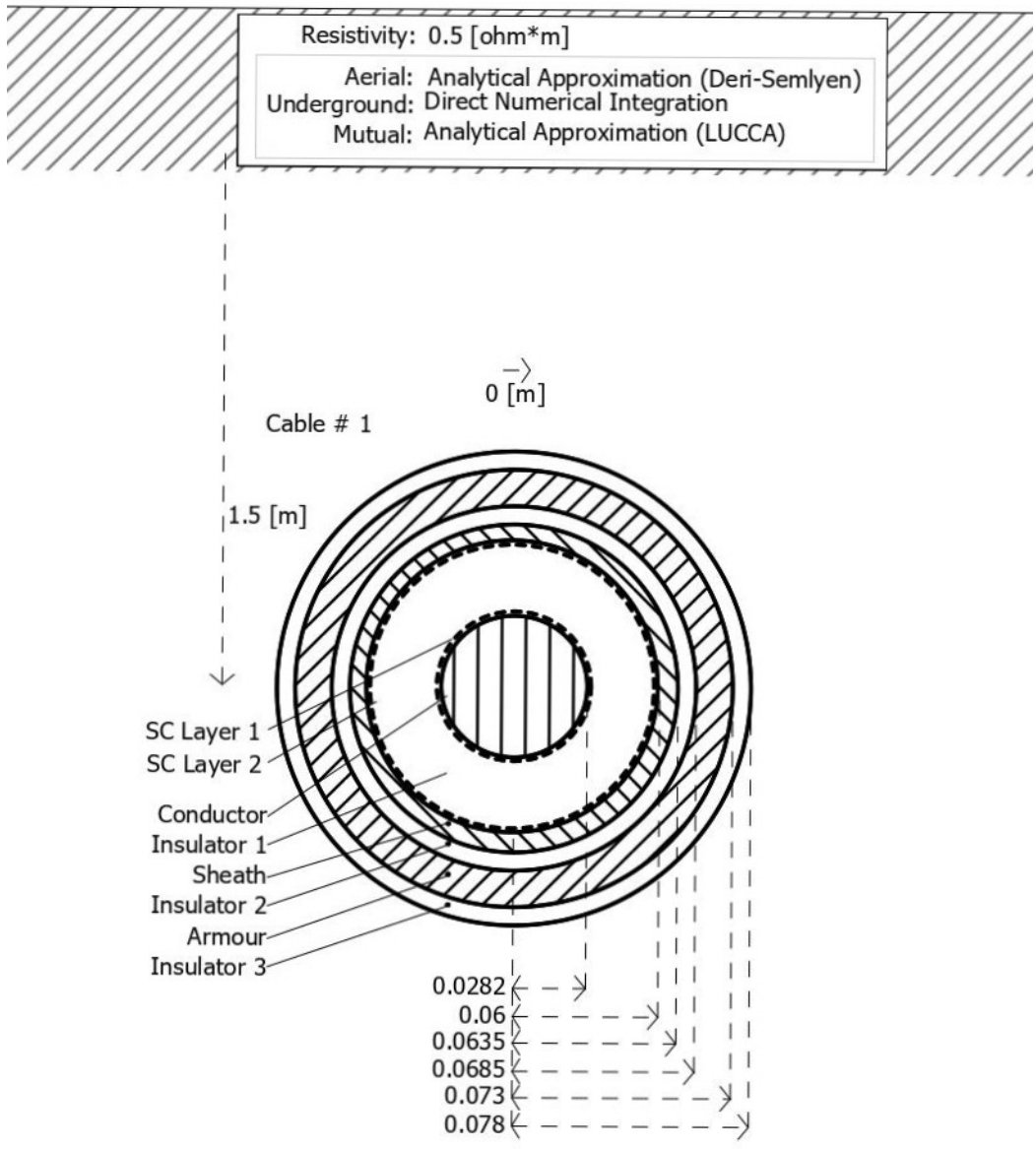



Figure 4.2: The parameters for the cable geometry of 525 kV XLPE submarine cable

strength of the breaker with $N$ VIs [5] is

$$U_b(s) = N \times U_{b1}(s) = N \times f \times s^{\alpha} \tag{4.2}$$

Hence, violation of this value results in the re-strike in the VI due to dielectric breakdown. Similarly, the re-strike in the VI can occurs if $\frac{di}{dt}$ at current zero is more than the critical limit as discussed in the previous chapters. Above values are chosen to replicate approximate physical behaviour of the VI since the experimental values are not known. From the voltage and energy stress point of view, the time instance of re-strike and duration of VIs unavailability have to be analysed and are discussed in the following sections.

## 4.3. Re-strike in VARC DC CB



The re-strike in the VARC DC CB affects the voltage shared among the different modules and energy absorbed by the SA. Hence, it is necessary to understand the significance of the re-strike in DC CB. In order to understand the effect of re-strike, different cases studies are carried out. These studies are generated based on the time instance, re-strike in the number of VIs and unavailability of VIs during different time periods.

### 4.3.1. Case 1 - During rise of TIV

Re-strike during the rise of TIV can lead to the permanent failure of the VI or it can also restore the interrupting capability of VI after first re-strike. Hence these two approaches are analysed in this section.

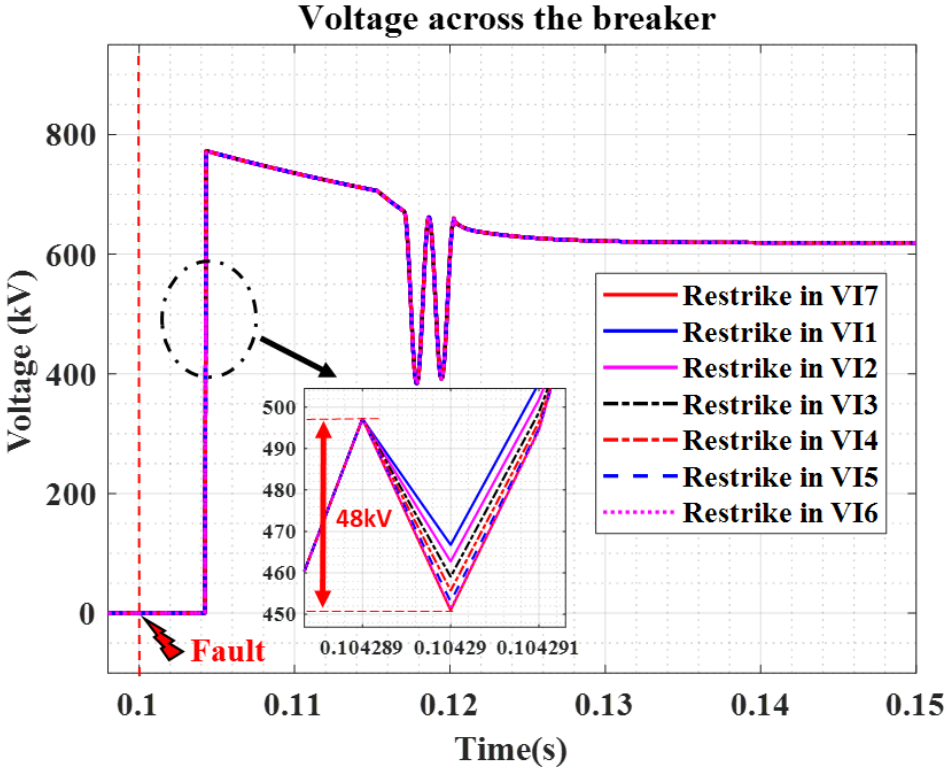



Figure 4.3: Voltage across the breaker during one VI re-strike with inability of VI to restore current interrupting capability after first re-strike, in various Vacuum interrupter (VI) during rise of TIV

Due to the occurrence of fault at 0.1 s, a trip signal is sent to the DC CB to isolate the fault. However, the time to generate this trip signal is assumed to be 1 ms. Hence, after 4 ms from the occurrence of a fault, current in VI approaches to zero due to current injected by the VSC (Voltage source converter). Further, a forced re-strike is carried out at 0.104288 s in the VI 7 of module 7, i.e.

after 10 μs of first current zero, which is depicted in figure 4.3. Moreover, it is assumed that re-strike causes permanent module failure, which leads to re-ignition in module 7. Hence, when compared to all the VIs, VI 7 shows higher distributed voltage variation. Similarly, simultaneous re-strike in VI 6 and VI 7 lead to higher voltage disturbance. However, this voltage disturbance has existed for a shorter duration. The loss of one VI indicates a loss of one module of DC CB. This leads to a reduction in the TIV of the DC CB, as depicted in figure 4.4. Similarly, with two VI re-strikes, there is a further reduction in the TIV. It is also observed that with an increase in the module failure due to re-strike, the oscillation in $V_{DCCB}$ after fault current neutralisation time is reduced, it is due to the fact that, time taken by the line current ($I_{Line}$), which is commuted into the SA, is longer. The frequency of this oscillation in figure 4.4 (a) is given by $f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{\left(\left(\frac{125}{7}\times10^{-6}\right)+(191\times10^{-6})\right)\times\left(\frac{2}{7}\times10^{-6}\right)}} = 681.26\ Hz$

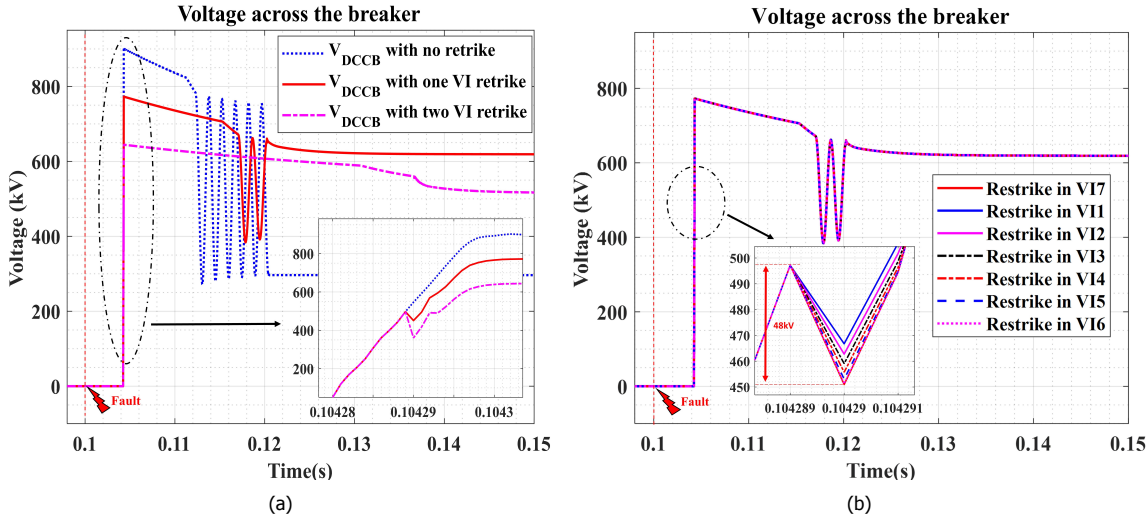



Figure 4.4: During rise of TIV, (a) Comparison of Voltage across the breaker with no, one and two VIs re-strike in absence of current interrupting capability of VIs after first re-strike (b) Voltage across each modules in absence of current interrupting capability of VI 7 after first re-strike

The dip in the voltage across breaker ($V_{DCCB}$) at 0.10429 s in figure 4.4(a) is due to the loss of the sub-module(s). With the loss of one sub-module, the individual voltage across the VI does not violate dielectric strength limit as depicted in figure 4.4(b). However, loss of a module causes voltage variation in remaining sound modules due to parasitic capacitance of the VI. In addition, due to the loss of one sub-module, the energy absorbed by the SAs in all of the modules increases. The following equation explains this increase in energy:

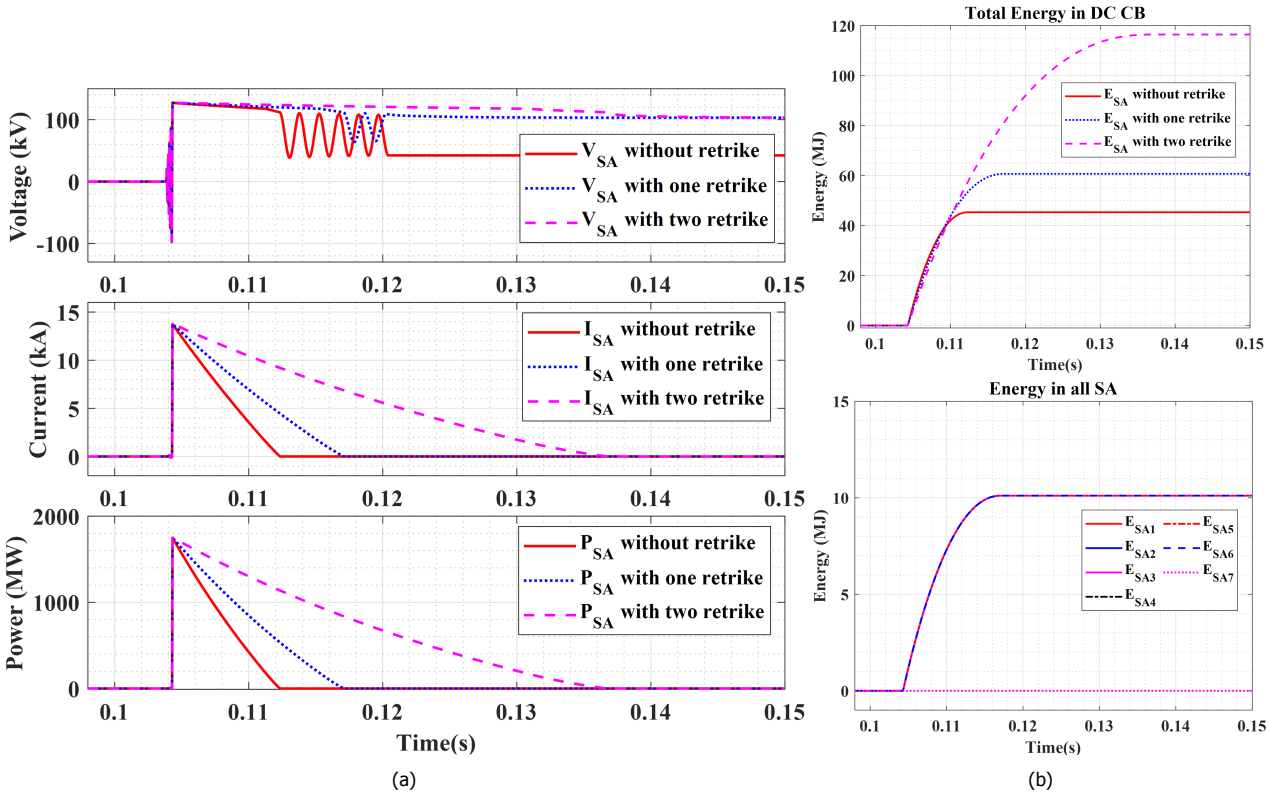
$$I_{SA} = \frac{\left(V_{system} - V_{DCCB}\right)}{L_{DC}} \times t \tag{4.3}$$

$$t_2 = \frac{I_P \times L_{DC}}{\left(V_{DCCB} - V_{system}\right)} \tag{4.4}$$

$$E_{SA} = \int_{t_1}^{t_2} I_{SA} \times V_{SA} dt \tag{4.5}$$

From (4.3) - (4.5), we can see that with reduction in $V_{DCCB}$ leads to the decrease in the slope of the current through the SA ($I_{SA}$). Also, it increases the $t_2$ time which in turn increases the energy stored in the SA, which is illustrated from figure 4.5. Moreover, the slope of $I_{SA}$ with no re-strike, one VI re-strike and two VIs re-strike are -1.94, -1.27 and - 0.60 kA/ms respectively. The energy absorbed by each SA of modules during one re-strike in the VI 7 is 10MJ whereas, without any re-strike in VI, energy absorbed by each SA is 6.4 MJ and with two VIs re-strike energy absorbed in the sound SAs rises to 23 MJ. Additionally, from the figure, we can see that $E_{SA7}$ does not absorb the energy due to the permanently closed state of VI 7 after re-strike. Hence, it can be concluded that with

an increase in the re-strike within modules with a permanently closed state of VI, the total energy absorbed by DC CB increases. However, the loss of more than two modules can lead to the failure of the entire DC CB due to insufficient TIV during the fault current suppression period.




(a) (b)

Figure 4.5: During rise of TIV with inability to interrupt current after first re-strike , (a) Voltage, Current and Power of the SA in first module during no re-strike, one VI re-strike and Two VI re-strike (b) Energy absorbed in all VIs during VI 7 re-strike. (Top) and Total energy absorbed by DC CB during no re-strike, one VI re-strike and two VI re-strike (bottom)

On many occasions, VI recovers from a re-strike due to its higher interrupting capability. So, now we assume that VI recovers before the second current zero in VI. With this added consideration to the previous case, but now we consider that the VI's current interrupting capability is restored after first re-strike. An analysis can be investigated.

Generally, the voltage source converter (VSC) is activated once the enable signal is received and remains activated until the voltage across the VI does not reach 7.6 % of 1.6 times the rated SA voltage ($V_{th}$), i.e. 10 kV. Hence, from figure 4.5(b) we can see that at the first re-strike, the voltage across VI 7 is 71 kV, a result the VSC is deactivated. However, due to the re-strike, VI 7 is closed, which results in a decrease in the peak amplitude of the injected current from VSC. Even with the restoration of current interrupting capability of the VI 7, VI 7 remains in the closed state. This malfunction is due to insufficient energy in the VSC, as indicated in figure 4.6.

Furthermore, it is observed that VSC with the $V_{th}$ = 10 kV setting, upon fault interruption at 0.1168 s, the VI 7 opens and the voltage is developed across it as indicated in figure 4.7 (a). The voltage across the VI 7 develops from zero as the capacitor in VSC discharges after a re-strike in VI 7.

Figure 4.6 illustrates the effect of variation in $V_{th}$ of the VSC. By changing the threshold limit from 10 kV to 110 kV, we increase the activation time of the VSC. Consequently, the peak amplitude of the injected current is incremented. Hence, once the threshold limit reaches the value of 110 kV, the VSC is deactivated.

Figure 4.7 (b) depicts that with a change in the threshold voltage of VSC from 10 kV to 110 kV, VI 7 interrupts the fault current. As a consequence, the voltage across the breaker rises to the rated clamped voltage (.i.e 910 kV).

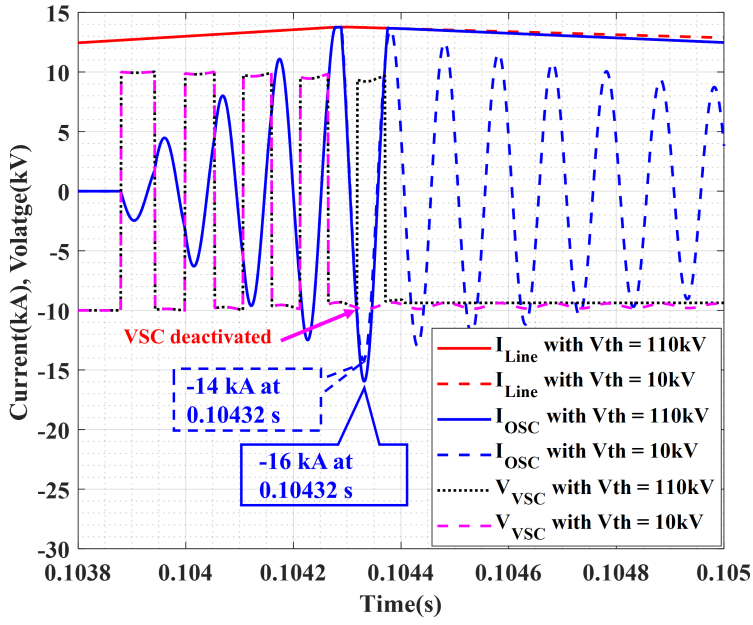



Figure 4.6: Effect of threshold setting of VSC on the $I_{OSC}$

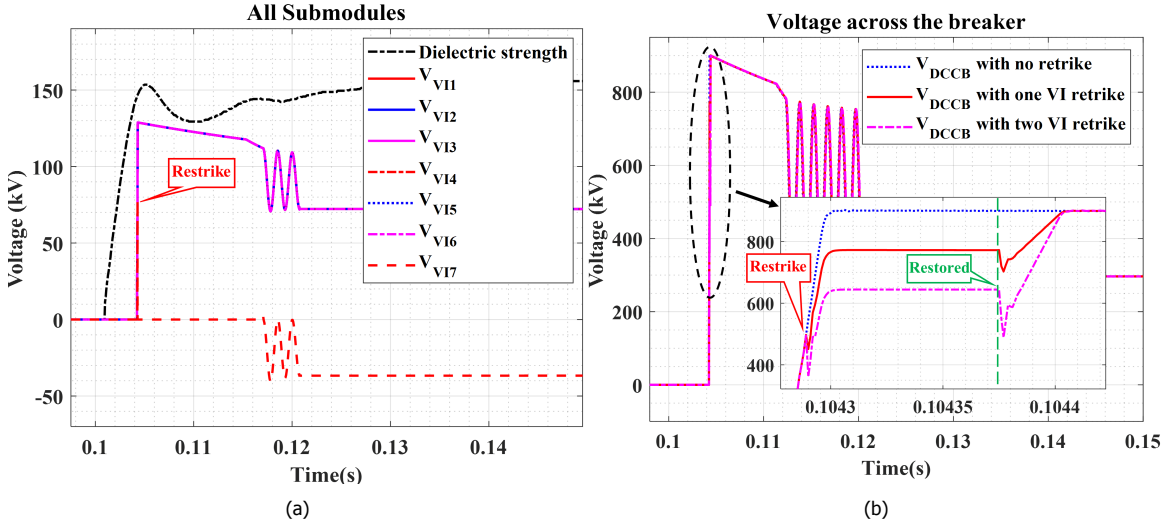



Figure 4.7: During rise of TIV, (a) Voltage across VIs of modules during VI 7 re-strike with the interrupting capability of VI 7 after first re-strike. (b) The voltage across the DC CB during and after re-strike with new threshold setting.

With the new threshold voltage of the VSC, the events of re-strike and re-close lead to variation in the energy absorbed by the modules as depicted by figure 4.9. As in the present case, due to re-strike in VI 7, energy absorption is delayed. Hence, 6.36 MJ is absorbed by the SA corresponding to VI 7 whereas healthy SAs absorbs 6.70 MJ. Further, re-strike in different VIs leads to an increase in the total energy absorption by DC CB. However, this increase is in proportionate ratio, as highlighted in figure 4.9 (b).

Now consider the multiple VI re-strike scenario. Figure 4.12 shows that simultaneously more than 5 VIs re-strike with the restoration of interrupting capability after the first re-strike in the DC CB, which can lead to a negative voltage across the breaker. Moreover, it is also observed that the slope of the TIV after restoration is different for different re-strike cases. Higher the number of VI re-strike, steeper the slope, as the duration of the TIV rise is fixed by the individual sub-module.

In reality, the re-strike in different VIs can occur randomly. Hence, considering this fact, figure

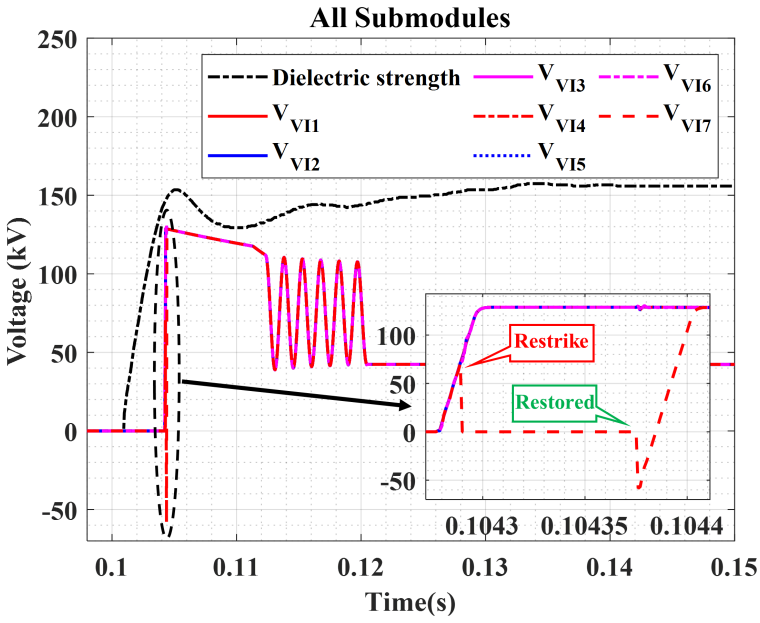



Figure 4.8: During rise of TIV, Voltage across each VI during and after re-strike with new threshold setting.

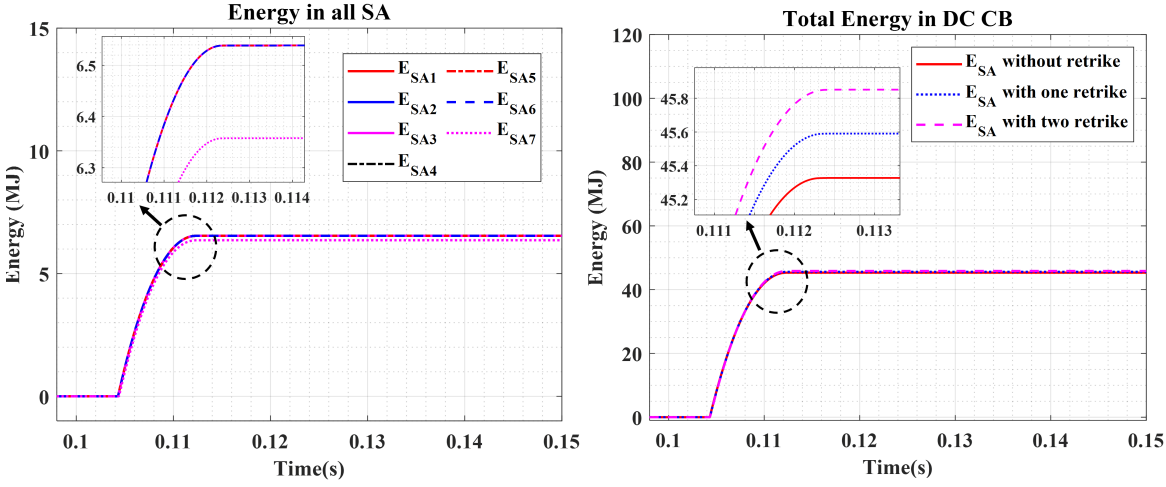



Figure 4.9: During rise of TIV,(a) Energy absorbed by each modules during and after one VI re-strike with new threshold setting. (b) Total energy absorbed by the DC CB during and after re-strike with new threshold setting for different VI re-strike.

4.11, depicts the effect of the random nature of the VI re-strike. Also, the random nature of the re-strike varies the voltage across DC CB. However, it appears that the DC CB does not reach the higher negative voltage as in the case of the simultaneous re-strikes. In the simultaneous re-strike, all the VIs after the re-strike were operation after the first re-strike. Nevertheless, in case of random re-strike, VI 7 does not come back in operation after the first re-strike. This is due to the fact that the injected current in VI 7 misses the peak of the fault current, as shown in figure 4.12. This miss-match is due to the deactivation of the VSC in module 7. This deactivation of VSC occurs as a result of rise in voltage across the VI 7 above the new threshold (.i.e 110 kV) at the time of the first re-strike.

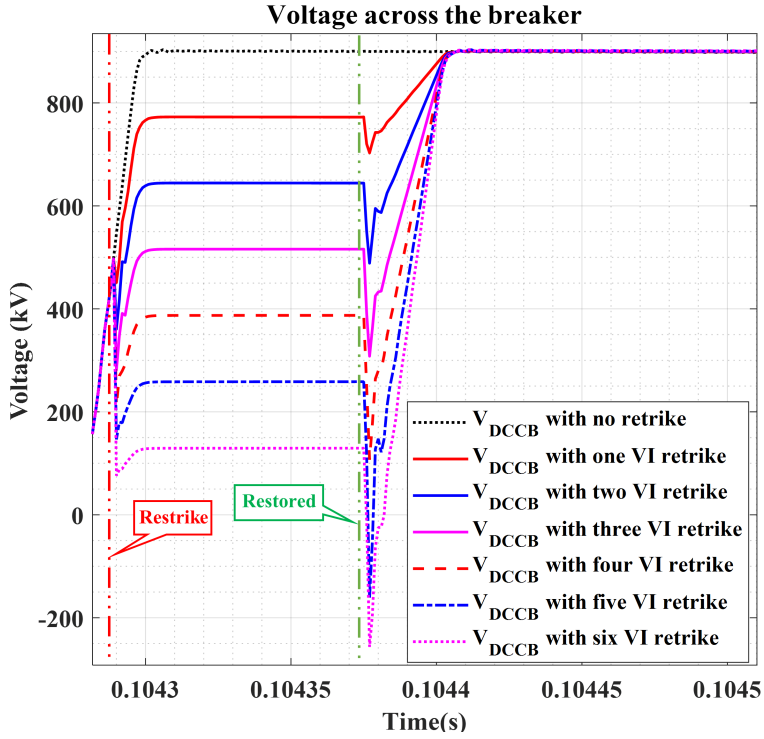
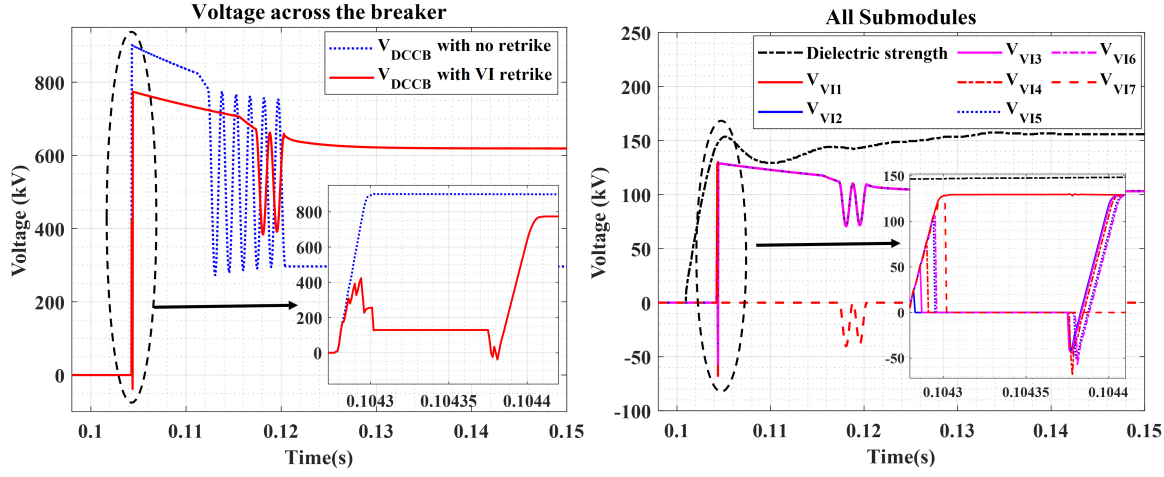



Figure 4.10: Comparison of Voltage across DC CB with the number of simultaneous VI re-strike during rise of TIV.




(a) (b)

Figure 4.11: During rise of TIV (a) Voltage across the breaker during random VI re-strike (b) Voltage across the each VI during random VI re-strike

### 4.3.2. Case 2 - During Fault current suppression time

A re-strike can occur after several milliseconds from the event of current interruption due to late breakdown. Therefore, a forced re-strike event is applied during the fault current suppression time to represent this. As previously stated, re-strike can lead to the permanent failure of the VI or restore its interrupting capability after a millisecond. Thus in order to investigate the performance of DC CB, these two cases are investigated in this section.

Considering the permanent failure of the VI to attain interrupting capability after the first re-strike, the following analysis is carried out. The fault occurs at 0.1 s, and after 4 ms, there is first current zero in VI due to the current injected by the VSC. Before any re-strike in VI, the fault current

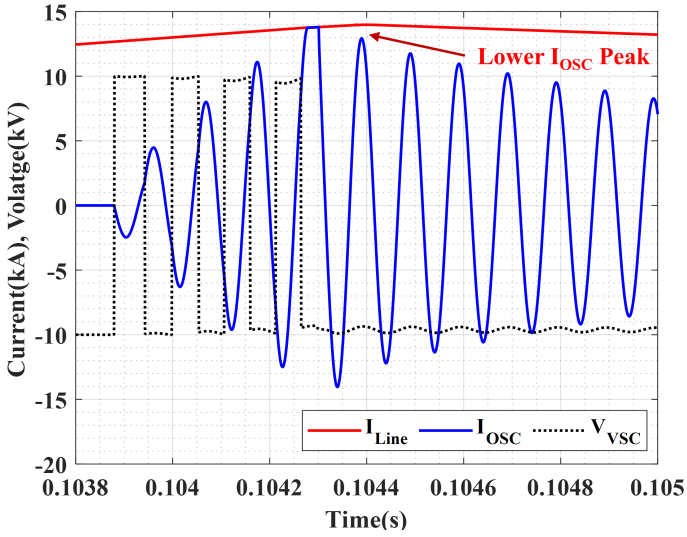



Figure 4.12: Failure of VI 7 during random VI re-strike as shown in figure 4.11

is commuted from the current injection branch to the energy absorption branch. Therefore, the voltage across the breaker is the sum total of the clamped voltage of the SA i.e. 7* 130 kV = 910 kV (figure 4.13). Similar to re-strike during rise of TIV , re-strike in the VI 7 lead to the higher voltage disturbance among other VIs as depicted in figure 4.13 and voltage drop by 130 kV in case re-strike occurs in the VI 7 at 0.1043655 s.

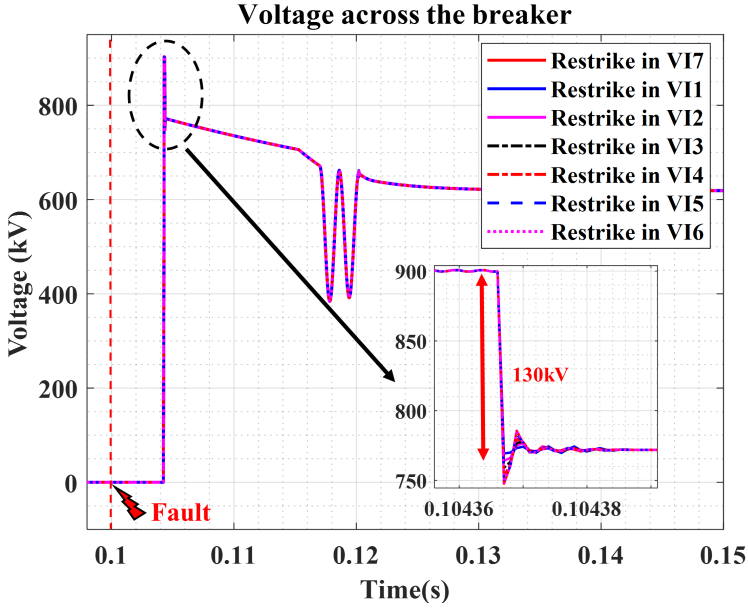
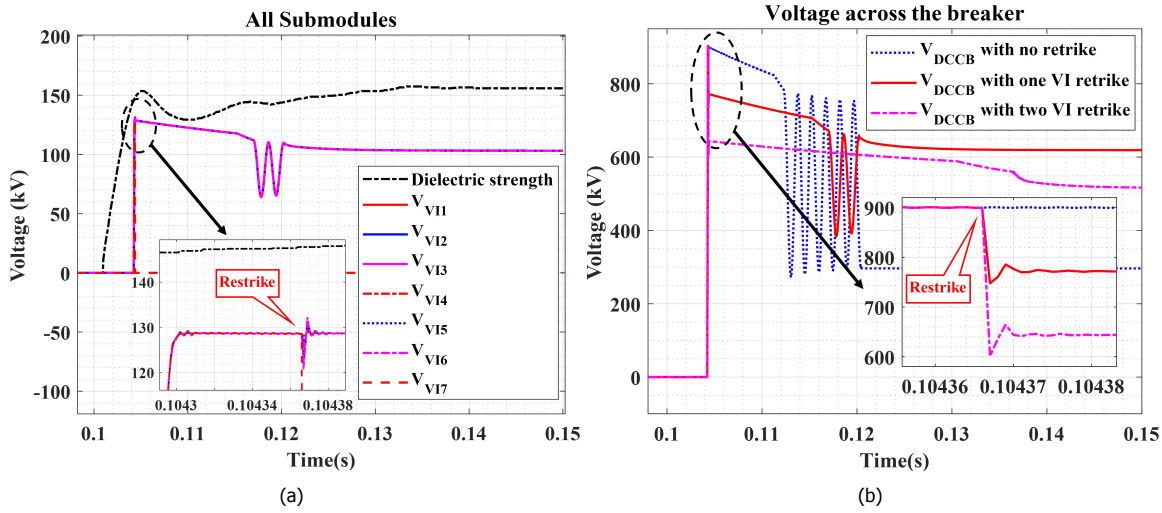



Figure 4.13: Voltage across the breaker during one VI re-strike with inability of VI to restore current interrupting capability after first re-strike, in various Vacuum interrupter (VI) during fault current suppression time

The voltage across the individual VIs and that across the breaker is illustrated in figure 4.14. It appears that re-strike at 0.1043655 s in VI 7 causes a spike in the sound VIs voltage, and this peak is also reflected in the $V_{DCCB}$. The spike amplitude is determined by the number of the VIs re-strike. Hence, re-strike in the two VI lead to a more substantial spike.

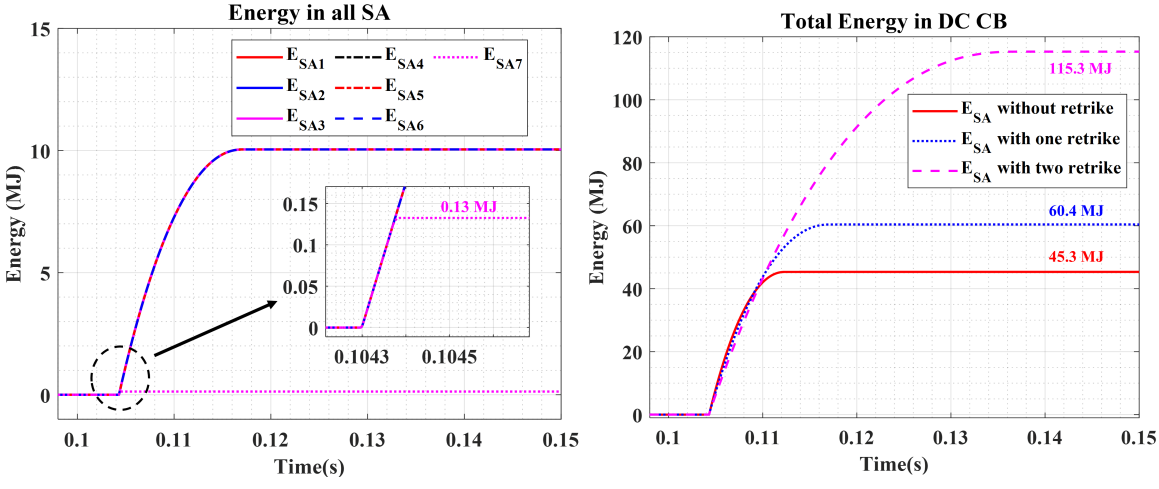
Consequently, the loss of one module due to re-strike leads to the reduction in the $V_{DCCB}$. As a result, there is an increase in energy absorption. figure 4.15 illustrates the energy absorbed by




(a) (b)

Figure 4.14: (a) Voltage across the VIs during the re-strike in VI 7 during fault current suppression time with inability of VI 7 to interrupt fault current after first re-strike (b) Voltage across the breaker with no, one and two VIs re-strike during Fault current suppression time and without current interrupting capability of VI after first re-strike

the individual SA during the VI 7 re-strike, and comparison of the energy absorbed by the entire breaker during VIs re-strike with the no re-strike case. However, it is interesting to note that the energy absorbed in the re-strike during fault current suppression and during the rise of TIV is the same. Unlike during the rise of TIV, the affected module absorbs the small percentage of energy which is depended on the occurrence of the first re-strike. Moreover, it is critical to note that if more




(a) (b)

Figure 4.15: During fault current suppression time and absence of current interrupting capability of VI after first re-strike, (a) Energy absorbed by each VI during VI 7 re-strike (b) Total Energy absorbed in DC CB with different VI re-strike

than two VIs are incapable of restoring the current interrupting capability after re-strike, then the entire breaker fails to isolate the fault.

As described in the previous section, if VI (in this case VI 7) is able to restore it's interrupting capability after the first re-strike, then the voltage across the $V_{DCCB}$ is restored to rated clamping voltage (i.e. 910 kV) at next current zero which is shown by the figure 4.16 (a). However, it is interesting to see that if two VI re-strike (in this case VI 6 and VI 7) and interrupting capability of VIs are restored after first re-strike, then both VIs do not interrupt current even after the restoration of VIs interrupting capability. Hence, the TIV is reduced to 650 kV, which in turn increases the energy absorbed by the SAs as displayed in figure 4.16(b).

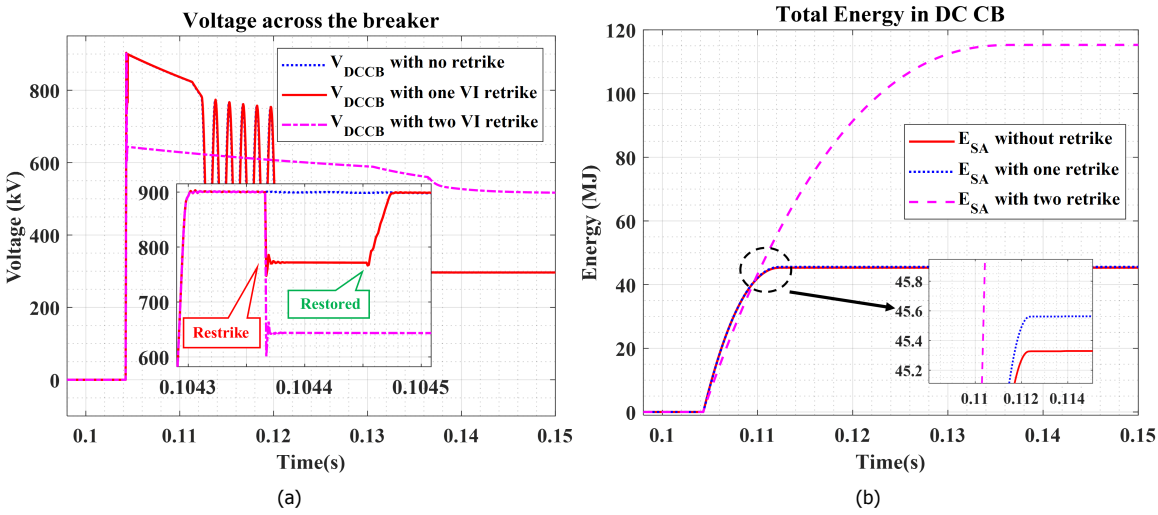



Figure 4.16: (a) Voltage across the breaker during the various VI re-strikes with restoration of the interrupting capability of VI after few micro second in fault current suppression time (b) Total energy absorbed by breaker during the various VI re-strikes with restoration of the interrupting capability of VI after few micro second in fault current suppression time

Inability to develop the interrupting capability of the VIs (in this case VI 6 and VI 7) after re-strike, is due to the insufficient energy in VSC. Since the voltage across the VI satisfies the $V_{th}$ criteria, the VSC is disabled. With the deactivation of VSC, the voltage across VSC remains constant. Now with the re-strike during fault current suppression time, the amplitude of the injected current in VI reduces after every half cycle due to the circuit resistance as VSC is disabled as seen in figure 4.17.

Unlike in the case of re-strike during the rise of TIV, adjusting the $V_{th}$ would not resolve this problem, as fault current is transferred to the energy absorption branch. The energy of VSC can only be increased by adjusting the $V_{DC}$. Although, this inability of VI 6 and VI 7 is resolved by

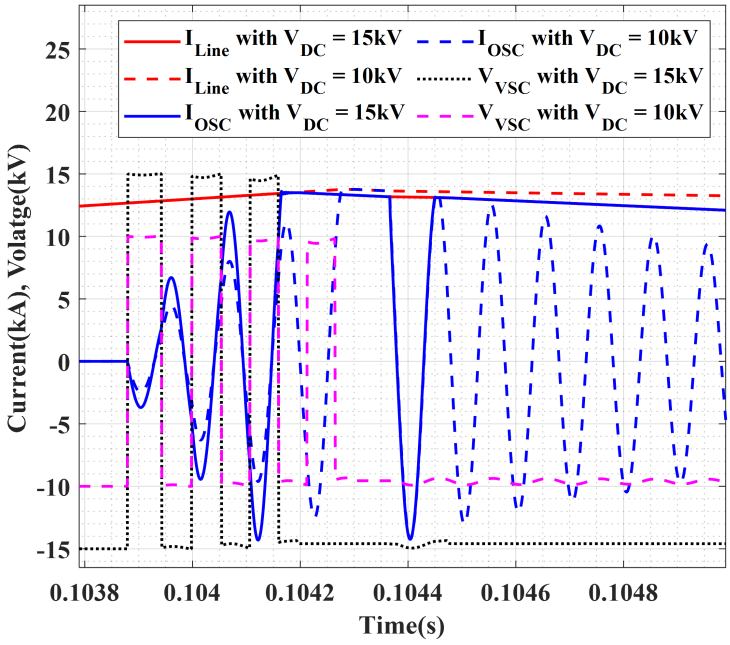



Figure 4.17: Effect of the change in $V_{DC}$ of the VSC in breaker.

increasing the $V_{DC}$ to 15 kV from 10 kV, as indicated in the figure 4.18 (b). With the increase in the

$V_{DC}$ there is an early occurrence of first current zero in VI .i.e at 0.10415 s as indicated in Figure 4.17 and figure 4.18

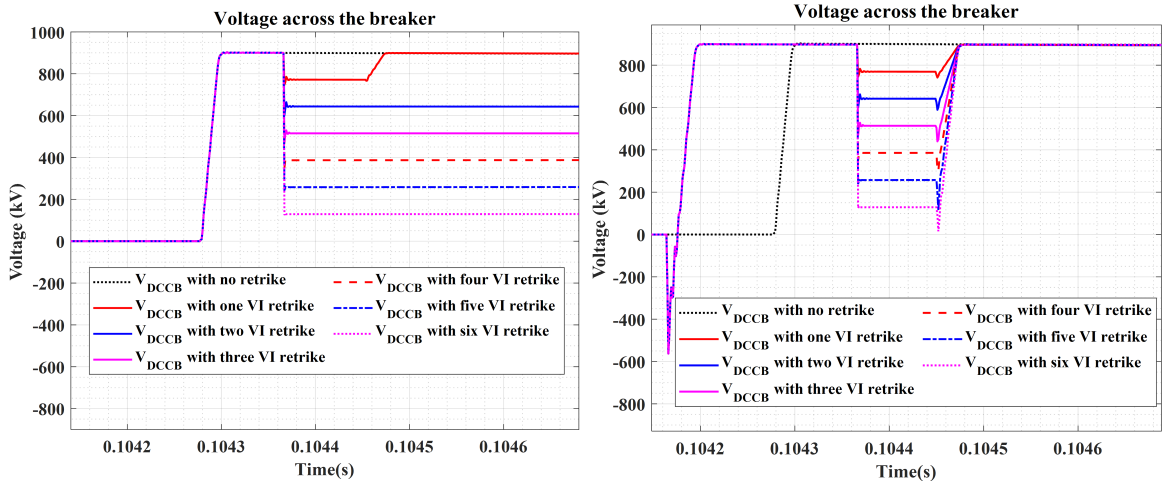



Figure 4.18: Comparison of voltage across DC CB with different VIs re-strike with (a) $V_{DC}$ = 10kV and (b) $V_{DC}$ = 15 kV.

Consequently, with the increased $V_{DC}$, the ITIV amplitude increases to -580 kV during the first current zero. This higher ITIV occurs as the voltage across the oscillating capacitor ($C_P$) is non-zero during the first current zero in VI. It is also observed that higher VI re-strike leads in larger voltage dip at 0.10445 s due to simultaneous opening of the VIs which in turn produces ITIV across each VI. This increases the net ITIV across the breaker.

The occurrence of the re-strike in the VI in AC application depends upon the different factors like presence of macroparticles between contacts [7], Ageing effect and voltage at the time of interruption [7]. As a result, VI re-strike occurs at different time instances in reality. Hence, the randomness of re-strike in the VI can be analyzed to observe the performance of the breaker, which is seen in figure 4.19. Unfortunately, random re-strike in VIs during fault suppression time leads failure of the entire breaker. This failure is due to the lower amplitude of the injected current. It is also noted from figure 4.19 that, re-strike in 6 modules at different time intervals, results in rise of fault current. However, even with the increase of $V_{DC}$, the amplitude of the injected current is lower than fault current in some modules, which leads to the re-ignition of these six modules. Since only one module (VI 1) is interrupting the fault current, the voltage across the VI increases beyond the dielectric strength of the VI. The increase in voltage across the VI is due to continuous rise of fault current. This increase is given by the characteristics of the SA. As a result, a breakdown takes place, and hence the DC CB re-ignites.

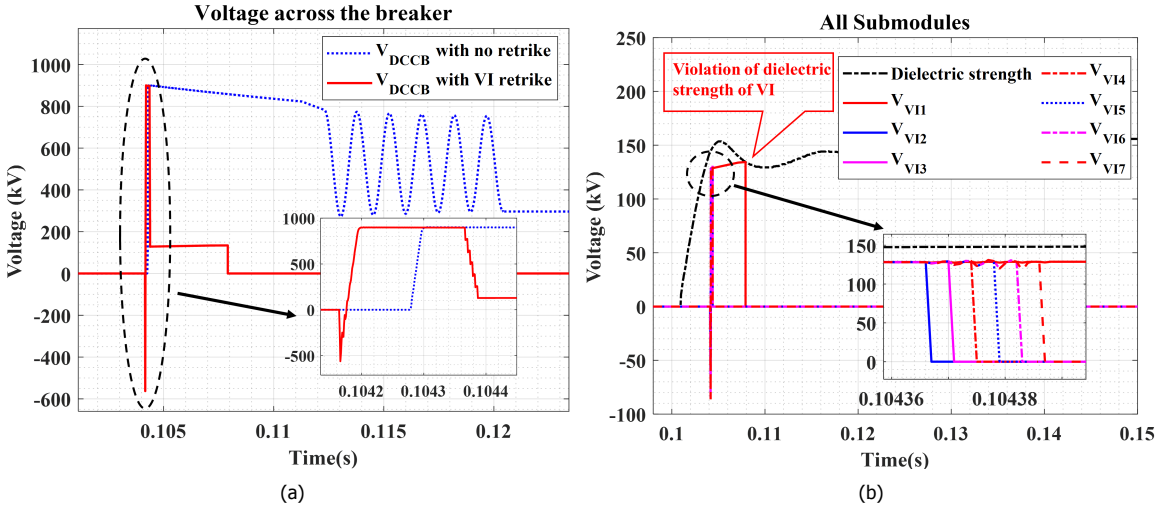
## 4.4. Re-strike in Active Current injected Mechanical DC CB

The re-strike in the Active current injected mechanical DC CB affects the voltage shared among the different VIs and energy absorbed by the SA. Hence, it is necessary to understand the significance of the re-strike in DC CB. In this section, different case studies are carried out to understand the effect of re-strike. The case studies are made based on the time instance, re-strike in the number of VIs and time duration.

### 4.4.1. Case 1 - During rise of TIV

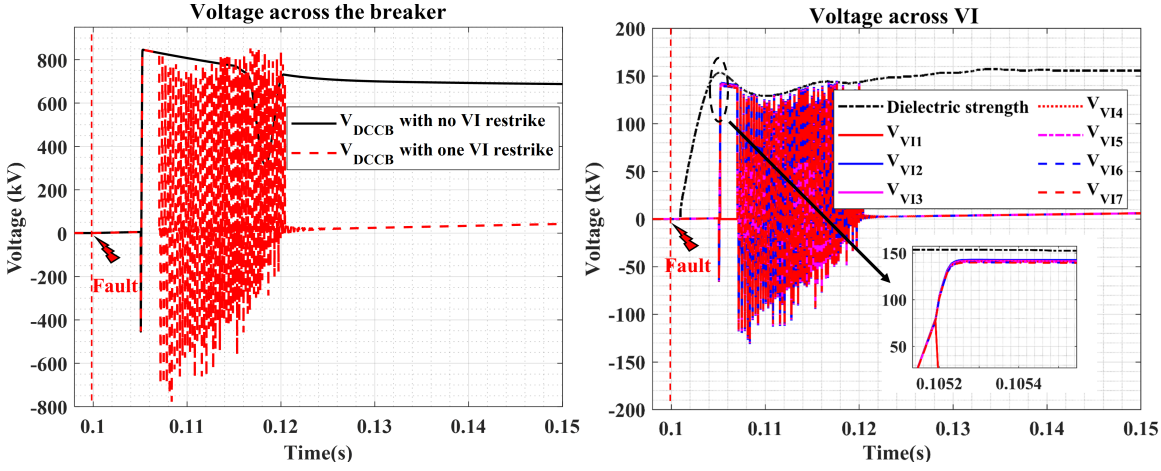
As explained earlier, the re-strike during the rise of TIV can lead to the permanent failure of the VI or restore the interrupting capability of VI after the first re-strike. Thus, in order to investigate the performance of mechanical DC CB, two significant cases are analysed in the following section.

Figure 4.20(a) depicts the comparison of the voltage across the DC CB with and without re-strike. The fault occurs at 0.1 s, and after 5ms, the current injection branch is activated by turning on the




(a) (b)

Figure 4.19: (a) Voltage across the breaker during random VI re-strike with restoration of interrupting capability and new $V_{DC}$, after first re-strike during fault current suppression time (b) Voltage across the each VI during random VI re-strike with restoration of interrupting capability and new $V_{DC}$, after first re-strike during fault current suppression time




(a) (b)

Figure 4.20: During rise of TIV and without interrupting capability of VI after first re-strike, (a) Voltage across the breaker during no re-strike and with one re-strike (b) Voltage across VIs during one re-strike in VI 1

making switch (MS). As a consequence, the first current zero-crossing in VI occurs at 0.10505 s. The transfer of fault current from the main branch to the current injection branch after current zero, leads to the formation of ITIV across VI. The amplitude of ITIV ($V_{ITIV}$) is given by the following equations [8]

$$V_{ITIV} = V_{DC} \times \cos(\theta) \tag{4.6}$$

$$\theta = \sin^{-1}\left(\frac{I_f}{I_P}\right) \tag{4.7}$$

$$I_P = V_{DC} \times \sqrt{\frac{C_P}{L_P}} \tag{4.8}$$

Where, $V_{DC}$ is the pre-charged voltage across the capacitor ($C_P$), $L_P$ and $C_P$ are oscillating inductor and capacitor and $I_f$ is maximum fault current i.e 16 kA. Solving (4.6) - (4.8), we get the amplitude of the ITIV as - 460 kV.

Furthermore, the forced re-strike is carried out at 0.10520 s in the VI 1. Considering that this re-strike causes permanent failure of VI 1, the effect can be seen in figure 4.20 (a). With the re-strike in VI 1, the voltage across rest VIs increases. This increase is due to the current flowing through the current injection branch, which develops a voltage across all series-connected VIs. Now a re-strike in one of the VIs results in redistribution of this voltage among the VIs, which further increases the voltage shared among the VIs. Consequently, this change in the voltage violates the dielectric strength limit of the individual VI, which in turn leads to the failure of DC CB. Thus, if even one VI is unable to restore the interrupting capability after the first re-strike, then the entire breaker fails to isolate the fault.

In comparison to the previous case, now we consider that the VI is able to recover its interrupting capability after the re-strike. Thus an investigation can be carried out on the performance of breaker in the following section.



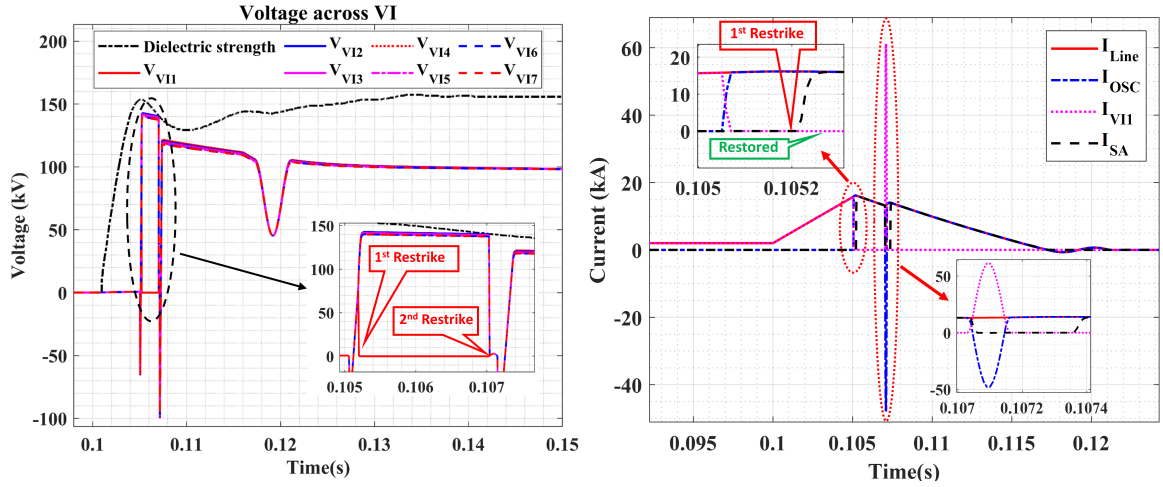



Figure 4.21: (a) Voltage across VIs during re-strike and after the restoration of Current interrupting capability of VI 1 during rise of TIV (b) Currents in the breaker during re-strike and after restoration of Current interrupting capability of VI 1 during rise of TIV

Figure 4.21 illustrates the one VI re-strike scenario with the restoration of current interrupting capability after the first re-strike. In figure 4.21 (a), even with restoration after 10 µs from the first re-strike in VI 1, the VI 1 still remains in a closed state, which results into increase in the voltage shared by other healthy VIs and further causing a violation of dielectric strength limit. Consequently, another re-strike is observed. The second re-strike is occurred in all the VIs, which result in the overshoot of the current in VI, as shown in figure 4.21 (b). This overshoot is calculated by:

$$V_C = 1.6 \times V_{DC} \tag{4.9}$$

$$I_{OSC} = V_C \times \sqrt{\frac{C}{L}} \tag{4.10}$$

$$I_{VI1} = I_f + I_{OSC} \tag{4.11}$$

Hence the peak amplitude of the current in VI 1 is $I_{VI1} = 16\ kA + \left(1.6 \times 525 \times \sqrt{\frac{2\times10^{-6}}{500\times10^{-6}}}\right)\ kA \approx 69.12\ kA$. Furthermore, at the next current zero, the TIV is built again, which does not violate the dielectric strength limit, as indicated in the figure 4.21 (a). With the restoration of the interrupting capability of VI 1 before the next current zero-crossing i.e. at 0.105210 s, DC CB is able to interrupt the fault. The dip in the voltage across the VIs at 0.117 s until 0.121 s is due to the oscillation of current in the current injection branch after the fault current suppression time. The frequency of this oscillation is given by $f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{((191\times10^{-3})+(500\times10^{-6}))\times(2\times10^{-6})}} \approx 257\ Hz$ . As a result

of the second re-strike, the energy in the SA increases by 6.07 MJ as depicted in figure 4.22. It is also observed that the energy absorption remains constant after the second re-strike for a defined period. This non increase in energy is because the current through the SA is diverted to VI after the second re-strike.

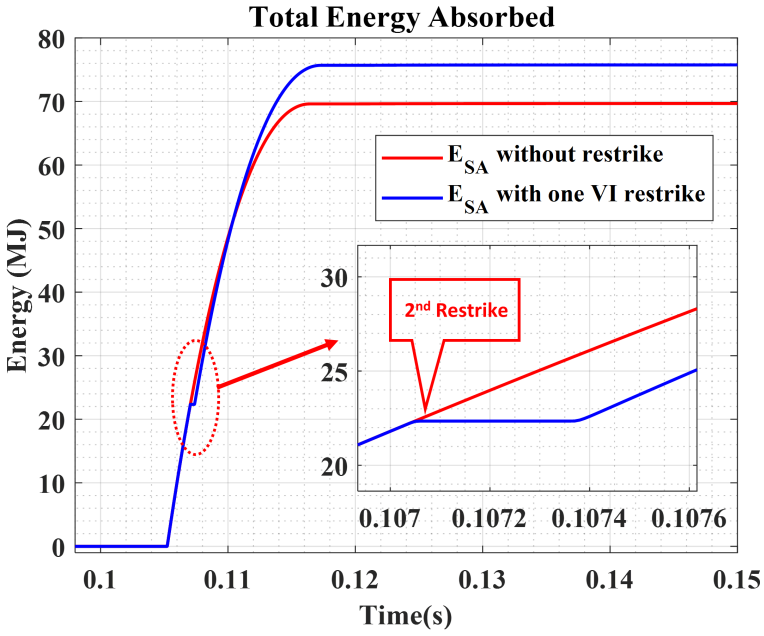


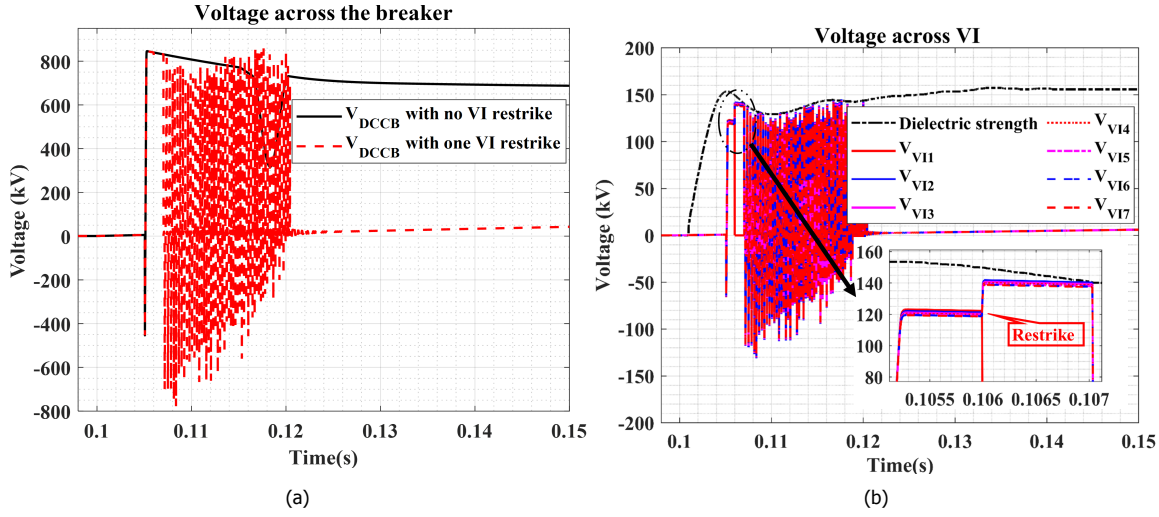

Figure 4.22: Energy absorbed in breaker during no re-strike and with one VI re-strike after restoration of Current interrupting capability of VI 1 during rise of TIV

### 4.4.2. Case 2 - Fault current suppression time

Similar to the previous sections, the occurrence of re-strike during the fault current suppression time in Mechanical DC CB can lead to permanent failure of the VI or restore the interrupting capability of VI after a millisecond. So as to understand the effect of these two scenarios, the following analysis is carried out in this section. As discussed in the previous section, the fault current is commuted to the SA after the first current zero-crossing in VI. Now, if the re-strike occurs in VI 1 during this period, i.e. during fault current suppression time at 0.106 s and VI 1 is unable to acquire the current interrupting capability after the first re-strike, then entire DC CB fails to interrupt the fault current. This failure is because of the permanent closure of VI 1 after re-strike, causing rise in the voltage shared by the non-re-striked VIs. As a result, the dielectric strength of the individual VI is violated, and failure occurs in DC CB system as depicted in figure 4.23.

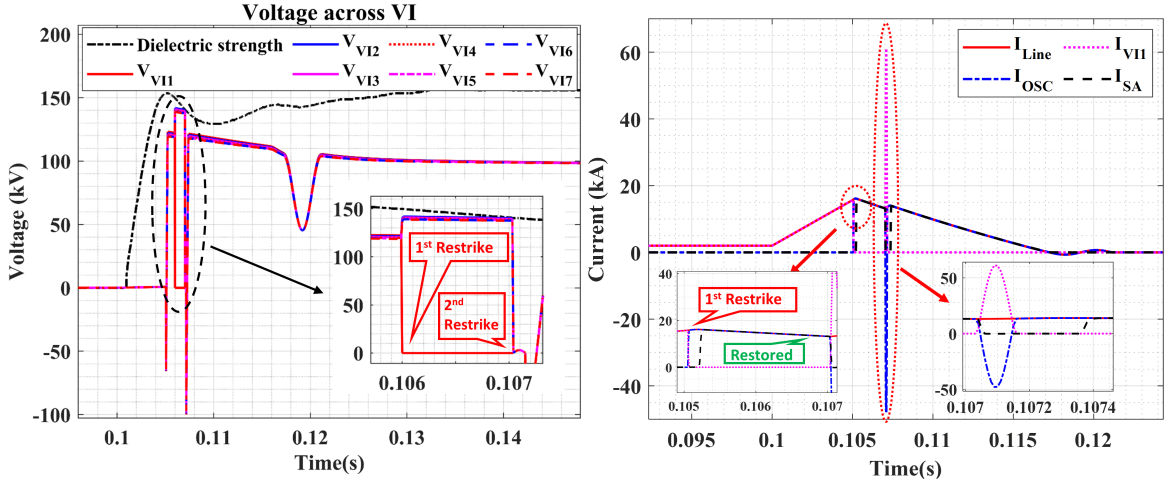
Similar to section 4.3.2, it is considered that the VI 1 able to restore the current interrupting capability within a few microseconds. However, even with the restoration of the interrupting capability of VI 1, there is a second re-strike. The second re-strike occurs in all of the VIs due to the violation of dielectric strength by sound VIs after re-strike in VI 1, as shown in figure 4.24 (b). Since, the current interrupting capability of VI 1 is restored, after the second re-strike, TIV across the each VI remains within the dielectric strength limit. Hence the fault is interrupted by DC CB (figure 4.24 (b)). Similarly to section 4.4.1, $I_{VI1}$ is calculated after the 2nd re-strike. The peak amplitude of the $I_{VI1}$ is $I_{VI1} = 13\ kA + \left(1.6 \times 525 \times \sqrt{\frac{2\times10^{-6}}{500\times10^{-6}}}\right)\ kA \approx 60.12\ kA$

However, increasing the number of VIs re-strike leads to early second re-strike in sound VIs. This early second re-strike is due to the fast increase of the voltage stress across the sound VIs. Furthermore, the random nature of the VI re-strike shows similar behaviour in mechanical-breaker for both time durations.




(a) (b)

Figure 4.23: Without interrupting capability of VI after first re-strike (a) Voltage across the breaker during no re-strike and with one re-strike in fault current suppression time (b) Voltage across VIs during one re-strike in VI 1 during Fault current suppression time




(a) (b)

Figure 4.24: (a) Voltage across VIs during re-strike and after restoration of Current interrupting capability of VI 1 in fault current suppression time (b) Currents in the breaker during re-strike and after restoration of Current interrupting capability of VI 1 in Fault current suppression time

## 4.5. Effect of circuit and SA resistance

In VARC and mechanical DC CB, the resistance of the circuit has a significant impact on the injected current by the current injection branch. In the case of VARC, presence of the resistance causes a damping effect on the current during the VSC activation. Similarly, during re-strike, both DC CB's experiences the drag, which affect the peak amplitude of the injected current.

The resistance in the network comprises of 2 components, linear resistance and non-linear resistance. The Linear resistance is due to the resistance of the oscillating inductor, wire resistance and on-state resistance of switches and VI. Whereas, the non-linear resistance is provided by the SA. The non-linearity of SA is due to the nature of SA's I-V characteristics. Further, the equation of injected current ($I_{OSC}$) in VARC DC CB can be formulated to incorporate the effect of these resistances, which

is given as follows:

$$I_{OSC} = \frac{V_{np}}{L\sqrt{y - \frac{x^2}{4}}}\left[e^{-\alpha t}\sin(\beta t)\right] \tag{4.12}$$

$$V_{np} = (2N-1)V_{DC}; N = \frac{\beta t}{\pi} \tag{4.13}$$

$$x = \frac{L_P + R_m R C_P}{L_P C_P R_m} \tag{4.14}$$

$$y = \frac{R + R_m}{L_P C_P R_m} \tag{4.15}$$

$$\alpha = \frac{x}{2} \tag{4.16}$$

$$\beta = \sqrt{\left(y - \frac{x^2}{4}\right)} \tag{4.17}$$

Where $L_P$ is oscillating inductor, $C_P$ is oscillating capacitor, $R_m$ is the resistance of SA, $R$ is the circuit resistance, and $V_{DC}$ is the source voltage in VSC.

### 4.5.1. Effect of the SA during VSC activation

Figure 4.25 (a) depicts the effect of SA resistance ($R_m$) on the injected current ($I_{OSC}$). It is noticed that with a higher value of the $R_m$, the damping is lower. This is due to the fact that the current is not conducted into the SA branch during the initial period. Hence, the amplitude of the injected current with $R_m = 100\ k\Omega$ is similar to the simulated value. However, if the VSC is activated for a few more cycles, the value of the $R_m$ changes and leads to an increase in the damping factor in $I_{OSC}$. This increase is because of the increase in the voltage across the SA after every reversal, leads to the conduction of the SA.

### 4.5.2. Effect of SA after a re-strike

In the re-strike scenario, depending upon the voltage across VI and threshold ($V_{th}$) setting, the VSC will be activated or deactivated. The typical value of the $V_{th}$ is set to 7.6 % of SA rated voltage. If re-strike occurs during the rise of TIV, and $V_{th}$ does not satisfy the threshold limit then, the VSC remains on for an indefinite period. Furthermore, with higher on-time of VSC, the voltage across SA rises, which lead to the conduction of SA. Consequently, the additional damping effect is added to $I_{OSC}$ which limits the peak value of the injected current. In contrast, if the voltage across VI satisfies the threshold condition at the time of re-strike, then the VSC is deactivated, and $I_{OSC}$ starts to damp out with lower initial damping factor. Figure 4.25 (b) depicts the scenario after the re-strike and the VI is unable to recover its current interrupting capability. Hence, due to the higher value of the voltage across the SA, the resistance is lower during the first peak, which is represented by the $R_m = 100\ \Omega$ curve. However, with the reduction in the voltage across the SA, the value of $R_m$ changes. Hence, over time, the simulated current matches with the different curves, indicating the variation of the $R_m$.

The equations (4.12) - (4.17) are also valid for the mechanical DC CB. In the mechanical breaker, $V_{np}$ will be equal to the system voltage.

## 4.6. Summary and Discussions

This chapter has investigated the effect of re-strike on the performance of active current injected mechanical CB and VARC DC CB. The re-strike effect was performed in two specific time durations for both DC CBs which was choosen based on type of breakdown. Also, in order to capture the transient behaviour of DC CB, a simplified representation of MTDC was implemented in PSCAD.

The investigation of re-strike in VARC DC CB during rise of TIV has shown that the failure in more than two VIs to recover their interrupting capabilities after the first re-strike can lead to failure of the entire DC CB. Moreover, during the above scenarios, the voltage shared amongst the sound

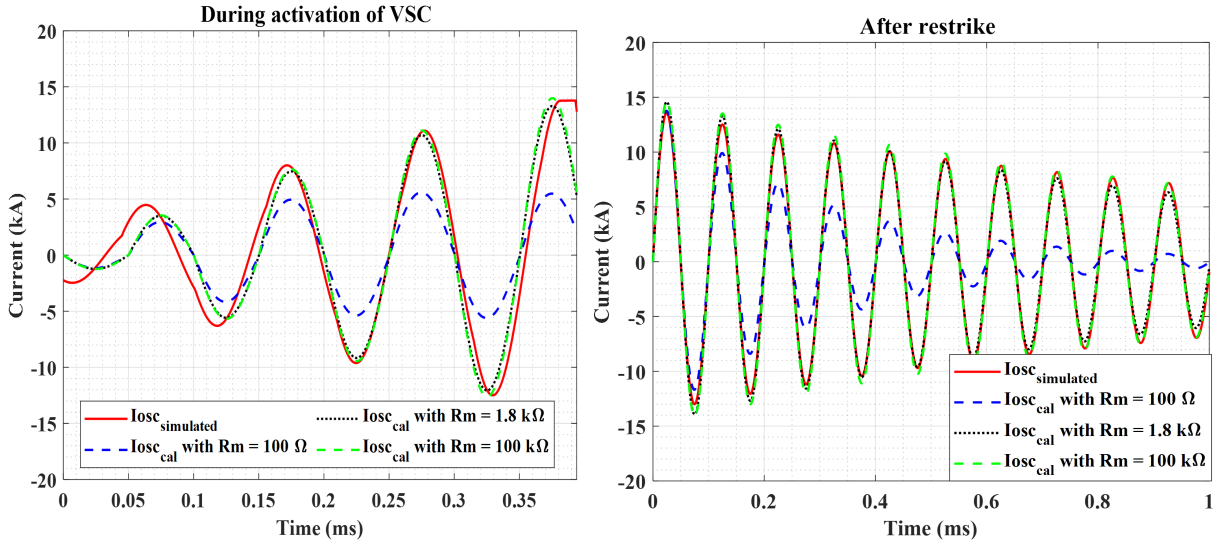



Figure 4.25: (a) Comparison of the simulated injected current ($I_{OSC_{simulated}}$) with different calculated injected current ($I_{OSC_{cal}}$) based on the different SA resistance ($R_m$) during activation of VSC in VARC (b) Comparison of the simulated injected current ($I_{OSC_{simulated}}$) with different calculated injected current ($I_{OSC_{cal}}$) based on the different SA resistance ($R_m$) after re-strike in VARC

modules was equal due to the presence of a parallel SA across each of the individual sub-modules. In addition, with the inability of the VI to interrupt current, the voltage offered by the DC CB against the source reduces. As a consequence, the fault current suppression time increases, which in turn increases the total energy absorbed by the DC CB. As a result, individual SA in healthy modules were stressed.

Unavailability of the VI after the first re-strike leads to 360% higher energy absorption in the individual modules. However, it was interesting to observe that, even with the restoration of the interrupting capability of VI, the affected VI during re-strike remains closed. This undesired operation of VI was due to insufficient energy in VSC. Moreover, with an increase in the energy level of VSC i.e. by increasing threshold settings, this problem was resolved. In the case of random VI re-strike during the rise of TIV, the time instant of re-strike also affects the current interruption in VI.

The re-strike during the fault current suppression time showed similar performance of DC CB as in the case of re-strike during rise of TIV. However, the inability of VI to interrupt current after restoration of interrupting capability was resolved by increasing $V_{DC}$ instead of adjusting the threshold settings. Furthermore, random re-strike during fault current suppression time can lead to failure of DC CB. Hence, this has to be considered while designing the VARC DC CB.

The second major investigation in this chapter was the effect of re-strike in mechanical DC CB during TIV rise and fault current suppression time. This investigation showed that in series-connected VI topology, even if one of the VI is unable to restore its interrupting capability after the first re-strike, the entire breaker operation fails. Furthermore, even with the restoration of VI's interrupting capability, there was a second re-strike due to the violation of the dielectric strength limit. Moreover, after the second re-strike, the breaker interrupts the fault current. Also, re-strike during the fault current suppression time produces similar outcomes.

In general, these results suggest that the modular topology of DC CB gives extra reliability than the series-connected VI topology. Also, the occurrence of re-strike affects the energy shared among the modules and the voltage across the VIs. Additionally, the presence of resistance in both technology has a significant impact on the injected current.

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# 5

# Estimation of parallel SAs in DC CB

*The Surge arrester(SA) is vital to the DC CB as it absorbs the energy during the fault. Since a single SA can not absorb megajoules (MJ) worth of energy, parallel connection of SAs is required. The required number of multi-column SA depends upon the worst case, which is analysed in this chapter. Furthermore, the effect of various circuit and system parameters on energy absorption is discussed.*

## 5.1. A brief about multi-column SA

During the fault suppression time, a large amount of energy is absorbed in the surge arrester (SA). Unlike in AC, the energy absorbed by the SA is tens of MJ during a DC fault interruption. Not only the stored energy in distributed line inductors; but also energy from the AC side of the MMC ( in case of the MTDC system) contributes to the energy absorbed by the SA [1]. The single SA column cannot absorb this energy, thus the multi-column arrangement of the SA has to be implemented.

The performance of the multi-column arrangement depends upon the current sharing among the columns. Hence it is essential to match the I-V characterises of the individual column. Due to the parallel arrangement, the voltage across each column is the same. Thus, energy absorbed by the SA has a direct relation with the total SA current and the individual column current. The energy absorbed by N number of SAs as discussed in [2] is given as

$$W_t = W_m\,[1 + S\,(N-1)] \tag{5.1}$$

Where $W_t$ indicates the net safe energy-absorbing capability of the SA, $W_m$ indicates the safe energy-absorbing capability of a column with the highest current amplitude and $S$ is the ratio of current in the sound column to the current in the column with the highest current amplitude. The value of $S$ is also dependent upon the manufacturer's experience [3]. Thus any changes in $W_m$ and $S$ will limit the energy absorbed by $N$ SAs.

Similarly, the current sharing among the columns is determined by a factor $\beta$, defined as follows :

$$\beta = N \times \frac{I_{max}}{I_{SA}} \tag{5.2}$$

Where $N$ represents the number of multi-column SAs, $I_{SA}$ represents the peak value of the total SA current and $I_{max}$ presents the peak value of the current in the column with the highest current amplitude. The manufacturer provides the factor $\beta$ by conducting a routine test on all SA units. The current sharing among the columns is better with a higher current level than that with a lower current level, which is discussed in [4]. Thus, in this thesis, the factor $S$ and $\beta$ are considered to be one.

Due to the enormous amount of energy absorbed by the SA during the interruption process, a rise in temperature among the multi-column is observed. However, the distribution of this temperature is not uniform. The temperature is higher in the middle and drops radially [5]. Furthermore, the dependence of $S$ and $\beta$ on the temperature is neglected in this thesis. Hence, the energy absorbed by the individual column is the same.

The energy absorbed by SA during the fault neutralisation time for mechanical DC CB is defined as follows.

$$E_{SA} = \int V_{SA} \times I_{SA} dt = k \times V_{DC} \times \left( I_f \times \Delta t + \frac{(1-k) \times V_{DC}}{L_{DC}} \times \frac{(\Delta t)^2}{2} \right) \tag{5.3}$$

$$\Delta t = \frac{V_{DC} \times t_{op} + I_0 \times L_{DC}}{(k-1) \times V_{DC}} \tag{5.4}$$

$$I_f = I_0 + \frac{V_{DC}}{L_{DC}} t_{op} \tag{5.5}$$

$$t_{op} = t_{DCCB} + t_{detection} \tag{5.6}$$

Where, k is the ratio of the clamping voltage to the rated voltage of SA, $t_{op}$ is defined as the Fault neutralisation time, $t_{DCCB}$ indicates the operation time of DC CB and $t_{detection}$ is the Fault Detection time. From equations (5.3) - (5.6), we can see that the energy in the SA depends upon the following element:

1. System voltage ($V_{DC}$)
2. Fault neutralisation time ($t_{op}$)
3. Characteristics of the SA ($k$)
4. Steady-state current ($I_0$)

5. Line inductor ($L_{DC}$)

For any given system, the system voltage $V_{DC}$ remains the same. Hence a sensitivity analysis can be carried out to check the effects of the remaining parameters on the energy absorption in the DC CB. However, module failure has to be considered in case of VARC DC CB, which can cause the voltage and energy stress among the individual modules. Similarly, the frequency of DC CB operation is also needs to considered.

In this chapter, sensitivity analysis is carried out on the Mechanical and VARC breaker. At the same time, estimation of the multi-column SAs in DC CB is performed by considering the worst case.

## 5.2. Fault neutralisation time ($t_{op}$)

Fault neutralisation time consists of the operation time of DC CB and the fault detection time. DC CB technology specifies the operation time. The operation time for the mechanical DC CB is considered to be 5 ms while the VARC has operation time of the 3 ms. However, the operation time can be delayed. Various factors can contribute towards this delay. For example, slow operation of the contact driving technology can lead to the delay in the operation of DC CB and also the direction in which the capacitor is charging can cause a delay in the DC CB operation. Another factor which can increase the Fault neutralisation time is the delay in fault detection. An analysis can be made to determine the effect of delay on energy absorption. For this analysis, 0.5 ms and 1 ms delay in the Fault neutralisation time are selected.

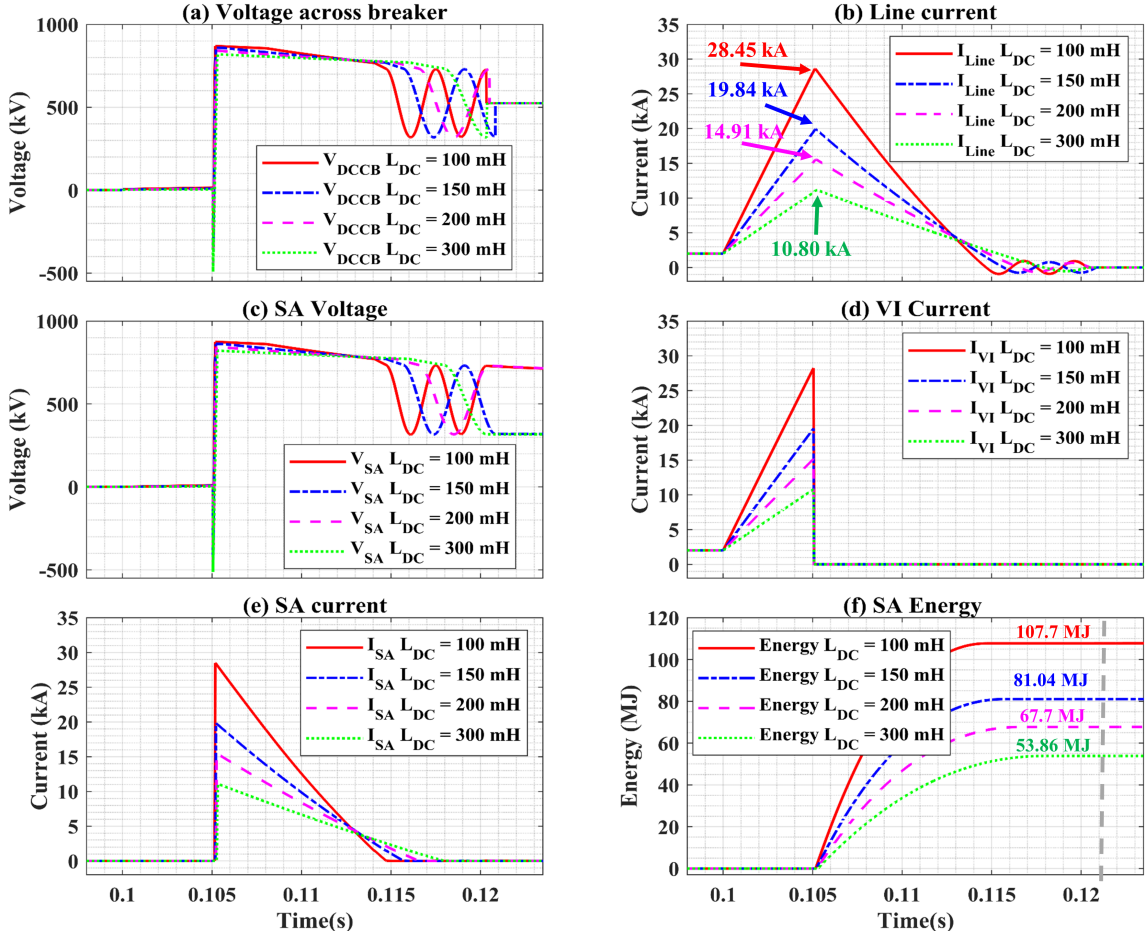



Figure 5.1: Effect of operational delay in mechanical DC CB on (a) voltage across breaker, (b) Line current, (c) surge arrester (SA) Voltage, (d) Vacuum interrupter (VI) Current, (e) SA current and (f) SA Energy

With an increase in the delay, the absorbed energy increases in the mechanical DC CB, as observed in figure 5.1. From equation (5.3), we can calculate the energy absorbed by the SA for the

increase in operational time ($t_{op}$) of mechanical DC CB. The detection of the fault is taken at the same instance of the occurrence of a fault. The delay of 0.5 ms leads to an increase in the $t_{op}$ to 5.5 ms.

In this case, the system voltage ($V_{DC}$) is 525 kV, with a steady state current ($I_0$) of 2 kA and the line inductor ($L_{DC}$) of 191 mH. Further, substituting this value in the (5.6), we get $\Delta t = \frac{V_{DC}\times t_{op}+I_0\times L_{DC}}{(k-1)\times V_{DC}} = \frac{525\times 5.5+2\times 191}{0.6\times 525\times 10^3} = 10.38\ ms$. Hence, increase in $t_{op}$, from 5 ms to 5.5 ms, causes fault current to rise to $I_f = I_0 + \frac{V_{DC}}{L_{DC}} t_{op} = 2\ kA + \frac{525}{191\times 10^{-3}} \times 5.5 \times 10^{-3}\ kA = 17.11\ kA$ and the energy absorbed by the SA during fault current suppression time is $E_{SA} = 1.6 \times 525\ kV \times \left(17.11 \times 10.38 + \frac{(1-1.6)\times 525\ kV)}{191\ mH} \times \frac{(10.38\ ms)^2)}{2}\right) = 74.55\ MJ$.

A similar, analysis is carried out for the 1 ms delay, which gives $E_{SA}$ = 87.26 MJ. As compared with the plot, the energy absorbed is more than the calculated value. This difference is because of the non-linear nature of SA's characteristics. Hence with the reduction in SA current, the voltage across SA drops gradually, which is depicted by figure 5.1 (c). Further, it results in the reduction of $k - factor$.

The figure 5.1 (a) indicates that with the increase in the delay, the ITIV value increases. The value of ITIV can be calculated from the equations (4.6) - (4.8). For the delay of 1 ms, the ITIV value is - 415.73 kV whereas, for 0.5 ms delay, ITIV value is -448.77 kV. This increase in ITIV is due to the voltage across the $C_P$ at the time of commutation of fault current. Moreover, this delay causes an increase in the current through VI. Consequently, in practice, the energy in the arc in the VI chamber increases. Hence, this energy can further delay the fault interruption.

A similar approach is applied to the VARC DC CB. In VARC DC CB, all the modules are delayed simultaneously for 0.5 and 1 ms. With 0.5 ms of delay, the total energy absorbed by DC CB is 34.34 MJ. The difference in energy absorbed between the no delay and 0.5 ms delayed case is 6.19 MJ, whereas, the difference in energy between the 0.5 ms and 1 ms case is 8.24 MJ. This variation is not only due to the delay, but, also due to damping of injected current by SA as explained in section 4.5. As VI is delayed to operate, the injected current grows, which result in the increase of voltage across the SA. As a consequence, the voltage reaches the knee point of SA which results in the conduction, as depicted in figure 5.2 (c) and (e). With an increase in the delay, the voltage across the breaker has a different value of the ITIV. With no delay, the ITIV is lower as the current zero occurs at the peak value of the injected current in VI. Hence the voltage across the $C_P$ is small. However, upon delay, the current zero does not occur at the peak, as shown in figure 5.2 (d), which results in the higher value of ITIV.

Also, due to the modular topology of VARC, the energy absorbed by each module will be $E = E_{SA}/7$. It should be noted that the rating of each SA ($V_{SAr}$) is 80 kV and the clamping voltage will be 130 kV. For a delay of 0.5 ms, Δt will be $\Delta t = \frac{V_{DC}\times t_{op}+I_0\times L_{DC}}{N\times k\times V_{SAr}-V_{DC}} = \frac{525\times 3.5+2\times 191}{7\times 1.6\times 80\times 10^3-525\times 10^3} = 6\ ms$ and Fault current will be $I_f = I_0 + \frac{V_{DC}}{L_{DC}} t_{op} = 2\ kA + \frac{525}{191\times 10^{-3}} \times 3.5 \times 10^{-3}\ kA = 11.62\ kA$. The difference between the simulated and the calculated fault current is because of miss-match of the injected current, which leads to extra reversal of VSC. The energy absorbed by each module ($E_{SAi}$) will be

$$E_{SAi} = \int V_{SA} \times I_{SA} dt = k \times V_{SAr} \times \left(I_f \times \Delta t + \frac{V_{DC} - N \times k \times V_{SAr}}{L_{DC}} \times \frac{(\Delta t)^2}{2}\right) = 4.4\ MJ$$

Total energy absorbed will be $E = E_{SAi} \times 7 = 31.12\ MJ$. The deviation of calculated energy from the simulated value is attributed to the I-V characteristics of the SA. Similar verifications can be performed for 1 ms delayed case.

Similar to the re-strike case, the occurrence of the delay in VI can be random. With a delay of 1 ms in module 1, the SAs of the remaining modules absorb higher energy, as illustrated in figure 5.3 (a). The sound modules provide sufficient voltage across the DC CB, which leads to a decrease in the fault current. After the delay, module 1 interrupts the reduced fault current; hence, absorbs lower energy. Similarly, with three modules delayed .i.e. module 1, 2 and 3, the voltage across the DC CB is lower than the system voltage. As a result, the fault current declines at a lower rate. Since, sound modules interrupt fault current before the delayed modules, energy absorbed by the sound modules is more as shown in figure 5.3 (b). Thus, a module which operates at a faster rate,

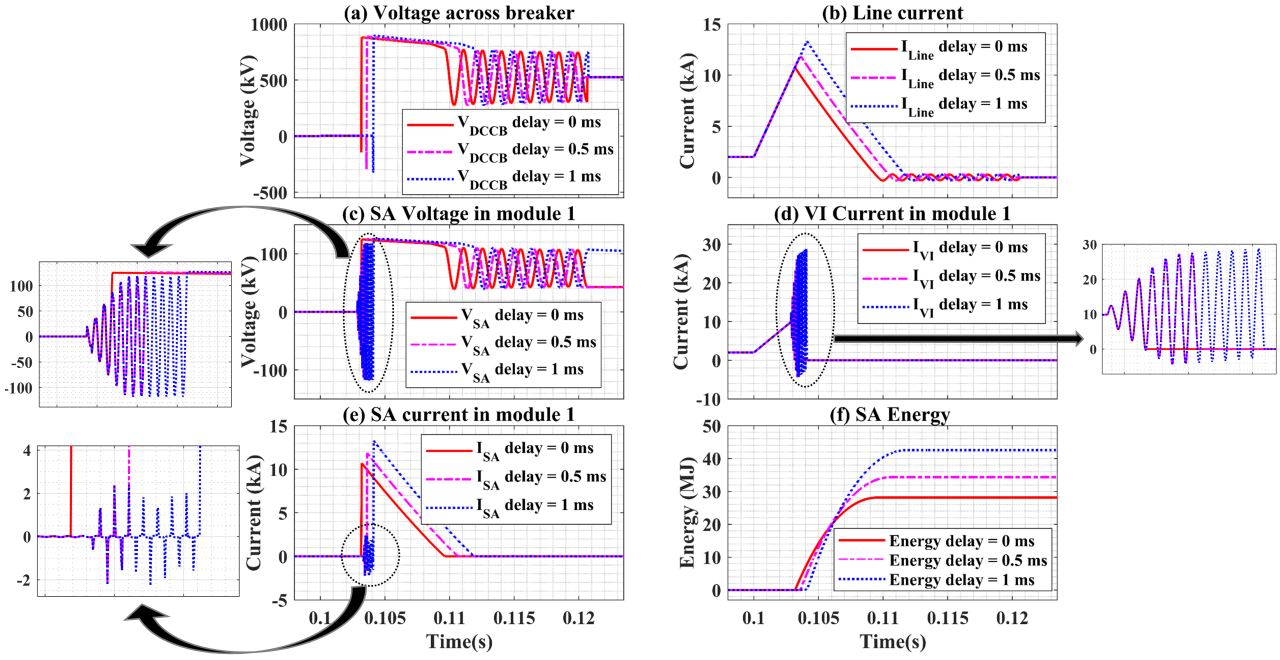



Figure 5.2: Effect of operational delay in VARC DC CB on (a) voltage across breaker, (b) Line current, (c) surge arrester (SA) Voltage, (d) Vacuum interrupter (VI) Current, (e) SA current and (f) SA Energy

absorbs higher energy.

Further, if we consider all the possible delay cases, then the energy absorbed by DC CB will be within the no delay and max delay limit i.e. ΔE, which is illustrated in figure 5.3 (d). Hence, it is observed that the delay of 1 ms can cause an increase in energy absorbed by 14.43 MJ in each module, keeping other parameters constant

## 5.3. I-V Characteristics of the SA ($k-factor$)

During the modelling of DC CB, the I-V characteristics of SA is considered. However, the characteristics of SA remains the same over its entire lifetime, but due to the higher energy absorption in HVDC interruption, these characteristics can be deteriorated [6]. Hence, this deterioration can cause reduction of the $k-factor$. Thus it is essential to study the effect of this deterioration on DC CB performance. Further, a comparison is made between $k-factor$ of 1.6 and 1.5 for both DC CB technologies. Figure 5.4 illustrates the effect of the $k-factor$ on the performance of mechanical DC CB. It is observed that the energy is absorbed by SA with lower $k-factor$ is higher. This energy can be calculated using (5.3) - (5.6). As the $k-factor$ is reduced from the 1.6 to 1.5, the Δt increases, thereby indicating an increase of the fault current suppression time. Hence, the total energy absorbed by the SA increase is given as:

$$\uparrow\Delta t = \frac{V_{DC} \times t_{op} + I_0 \times L_{DC}}{(\downarrow k - 1) \times V_{DC}}$$

$$\uparrow E_{SA} = \int V_{SA} \times I_{SA} dt = \downarrow k \times V_{DC} \times \left( I_f \times \uparrow\Delta t + \frac{(1 - \downarrow k) \times V_{DC}}{L_{DC}} \times \frac{(\uparrow\Delta t)^2}{2} \right)$$

It is also observed that the peak value of the fault current in the VI remains the same, as the $t_{op}$ is unaffected. Due to the change in the I-V characteristics, the clamping voltage changes for the same fault current, as seen in figure 5.4 (c). Although, the ITIV remains the same for both the I-V characteristics. The change in $k-factor$ from 1.6 to 1.5 also affects the slope of line current, which results in lesser stiffness of the line current in fault current suppression time.

Similarly, for the VARC breaker, the variation of the I-V characteristics of SA produces similar results. The energy absorbed by the DC CB for $k-factor$ of 1.5 is 29.23 MJ which is 1.08 MJ

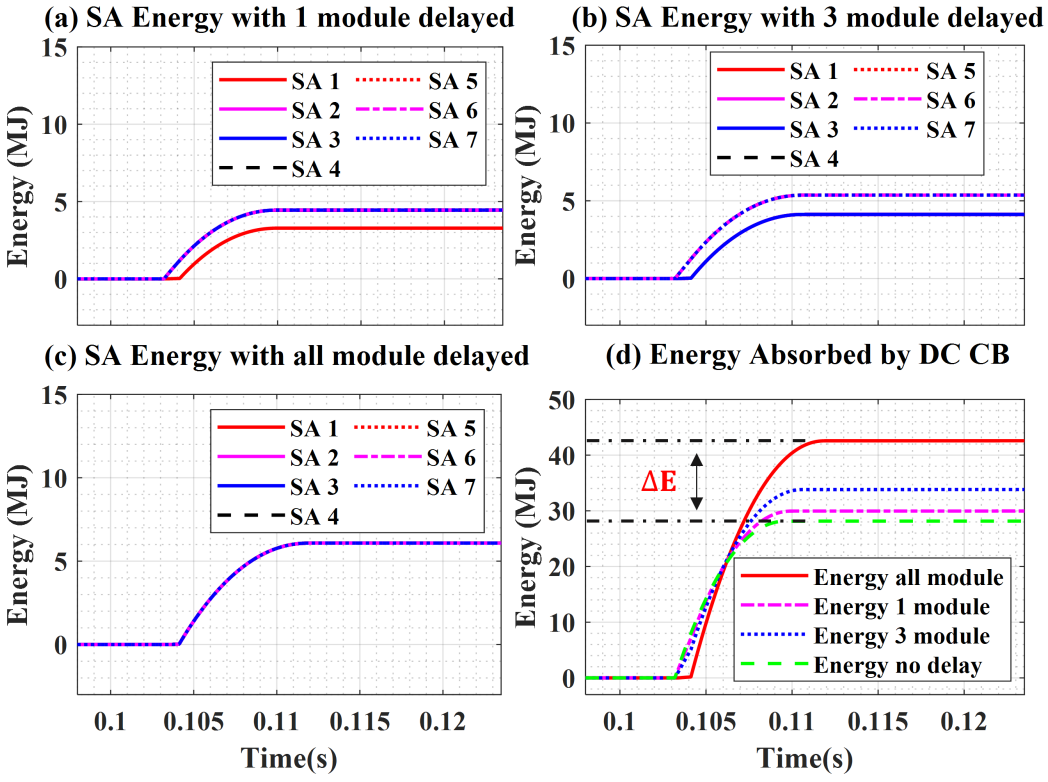



Figure 5.3: Effect of random delay in the VARC DC CB. (a) Energy absorbed by all modules during 1 module delayed by 1 ms (b) Energy absorbed by all modules during 3 module delayed by 1 ms (c) Energy absorbed by all modules during all module delayed by 1 ms (d) comparison of the total energy absorbed by DC CB during simultaneous delay of 1ms, 1 module delayed by 1 ms, 3 module delayed by 1 ms and no delay.

more than in $k-factor$ of 1.6. This difference is lower in the VARC DC CB in comparison with the mechanical DC CB. The peak amplitude of fault current in the VI remains the same for both characteristics as $t_{op}$ is kept constant. With a change in $k-factor$ from 1.6 to 1.5, the ITIV remains the same but the amplitude of TIV changes within a small margin.

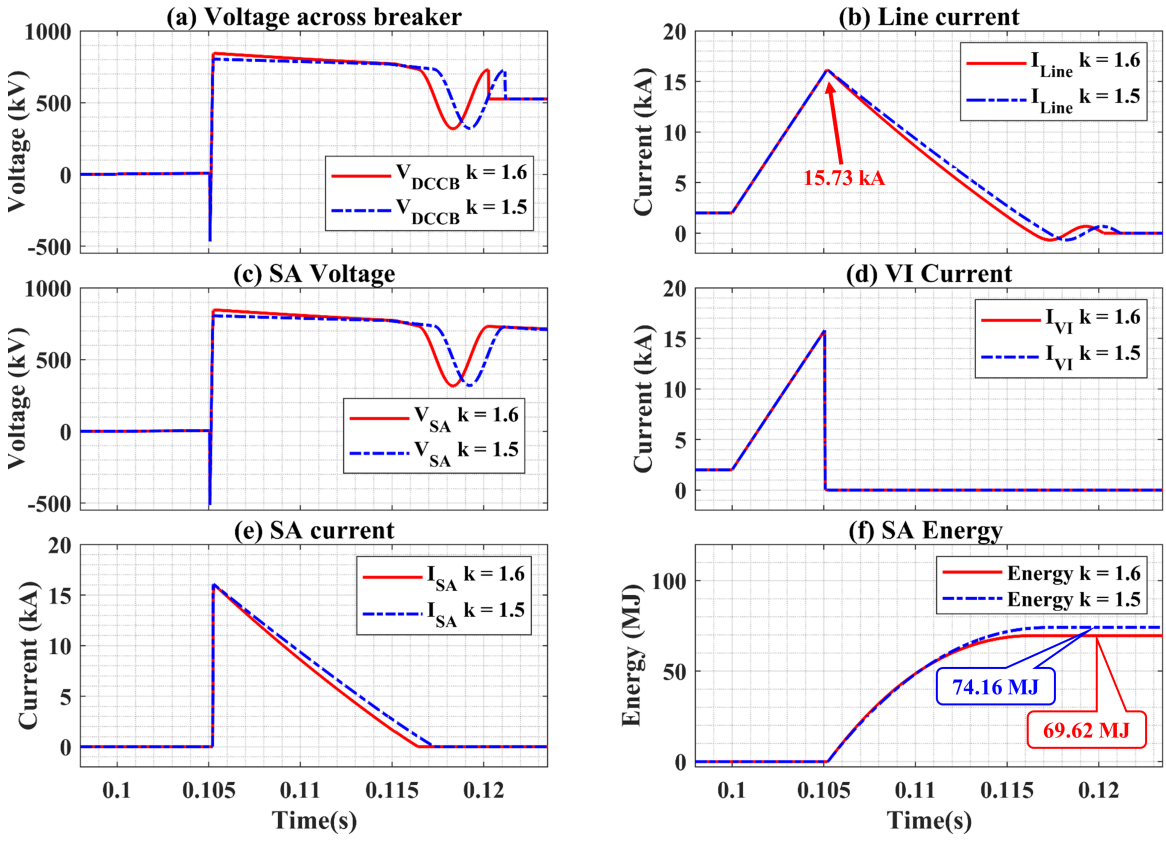



Figure 5.4: Effect of I-V characteristics of SA ($k - factor$) in Mechanical DC CB on (a) voltage across breaker, (b) Line current, (c) surge arrester (SA) Voltage, (d) Vacuum interrupter (VI) Current, (e) SA current and (f) SA Energy

## 5.4. Steady-state current ($I_0$)

The Steady-state current ($I_0$) depends upon the HVDC network topology. For an instance, having multiple lines at the bus in a multi-terminal HVDC network can lead to an increase in the $I_0$. Also, it is important to have an estimate of the maximum value of the steady-state current. The value of $I_0$ is determined from the power flow calculation. In order to see the effect of $I_0$ on energy absorption, two values are chosen i.e. 1 kA and 2 kA. The choice of this value is based on the studied network.

Figure 5.1 shows the effect of $I_0$ on the performance of mechanical DC CB. It is noticed that with an increase in the $I_0$, the energy absorbed by the SA increases. The difference in SA energy between the two scenarios is 7.67 MJ. This increase in energy is due to the increase in the fault current level and the Δt as seen in figure 5.1 (b) and figure 5.1 (e) respectively. Furthermore, the rise in steady-state current from the 1 kA to 2 kA, causes an increase in the ITIV, which can be computed by (4.6)-(4.8). With a rise in fault current, $t_{ITIV}$ increases, which leads to an increase in the ITIV. Although, the TIV in both cases remains the same. With the operation of RCB, i.e. after 20 ms of the trip signal, the voltage across the DC CB drops to the system voltage. However, the voltage across the SA is equal to the $C_P$ voltage. Since this voltage is close to the knee point of SA, a small leakage current flows through the SA.

Similarly, for the VARC DC CB, the energy absorbed by the SA with $I_0$ =1 kA and $I_0$ =2 kA, are 23.36 MJ and 28.15 MJ respectively. However, the ITIV in VARC is very small as current zero in VI takes place at an instant of zero voltage across the $C_P$.

## 5.5. Line inductor ($L_{DC}$)

Due to the lower impendence of HVDC network, the rate of rise of fault current is higher. So, in order to limit this rate, line inductor $L_{DC}$ also know as fault current limiting reactor is inserted in series with DC CB. By limiting the current rise, $L_{DC}$ can prevent multi-modular converter (MMC)

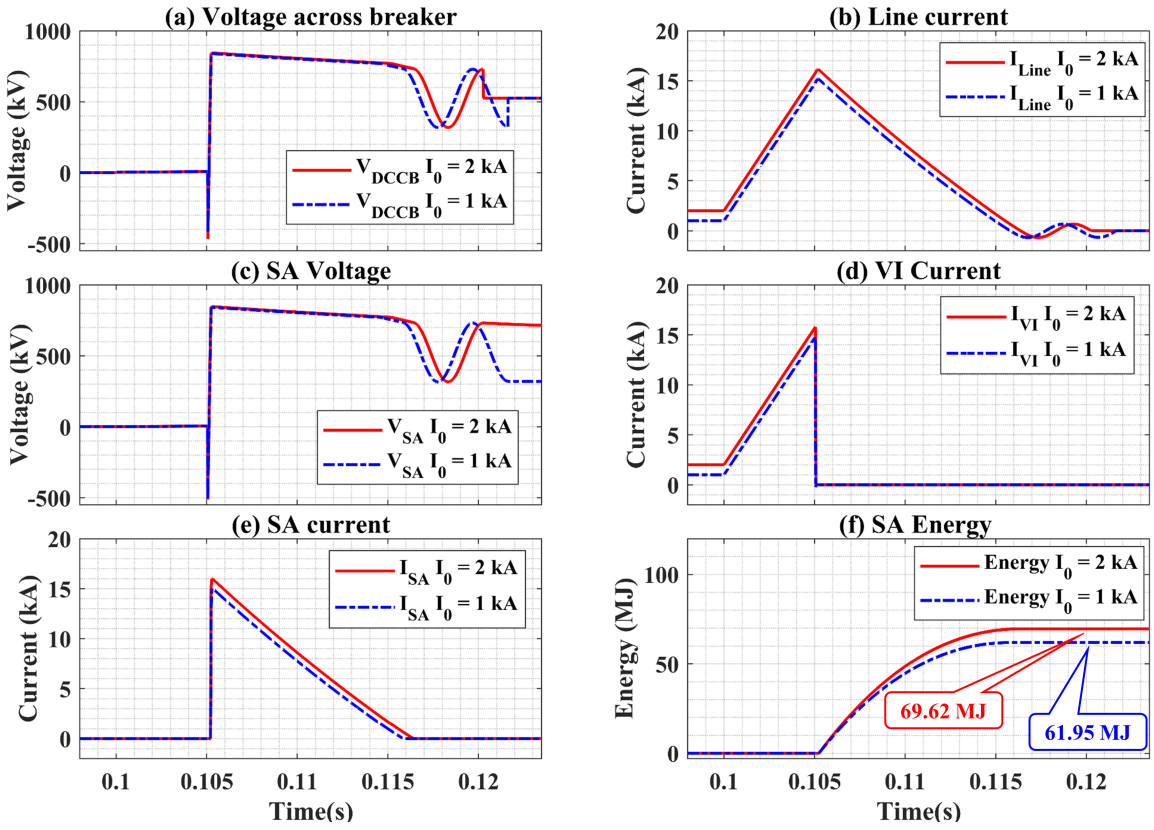



Figure 5.5: Effect of steady state current ($I_0$) in Mechanical DC CB on (a) voltage across breaker, (b) Line current, (c) surge arrester (SA) Voltage, (d) Vacuum interrupter (VI) Current, (e) SA current and (f) SA Energy

from blocking. As a result, continuity of the power is maintained in the sound links of the MTDC system [7]. In addition to $L_{DC}$, a smoothing reactor is installed in the HVDC network [8]. Besides limiting the DC fault current, the smoothing reactor also prevents intermittent current, eliminates the resonance in the DC circuit and reduces harmonic currents. The size of the smoothing reactor lies between the 100 to 300 mH for long-distance DC link. Furthermore, the line inductor ($L_{DC}$) is used to detect the fault current by monitoring the $L_{DC}$ voltage, as discussed in [9]. The sizing of the line inductor and smoothing reactor is vital in terms of stability and performance of the MTDC system.[10]. With the higher value for the inductance, the MMC losses its controllability over the voltage. In recent year, superconducting fault current limiters (SFCL) are proposed in [11] instead of passive fault current limiting reactor and smoothing reactor. The SFCL can function as a smoothing reactor during the pre-fault condition and limits the fault current rise during fault scenarios. At the same time, it reduces the requirement of a large reactor with extra expenditure.

The effect of the $L_{DC}$ on DC CB performance is analyzed by considering four values of inductances i.e.100 mH, 150 mH, 200 mH and 300 mH. Figure 5.6 shows the effect of variation of $L_{DC}$ on the performance of the mechanical DC CB. Change in the line inductor affects ITIV. This is due to the fact that the interruption of current in VI takes place at different amplitude as indicated in the figure. Hence, it is observed that the higher value of inductance causes larger ITIV, which is given by (5.7)-(5.9).

$$V_{ITIV} = V_{DC}\cos(\omega t_{ITIV}) \tag{5.7}$$

$$I_{max} = V_{DC} \times \sqrt{\frac{C_P}{L_P}} \tag{5.8}$$

$$t_{ITIV} = \sin^{-1}\left(\frac{I_f}{I_{max}}\right) \tag{5.9}$$

Further, with an increase in the inductance value, the peak amplitude of the fault current is reduced, as indicated in figure 5.6 (b). This reduction of the peak amplitude is due to the lowering of the rate of rise of fault current (RRFC). For 300 mH line inductor, RRFC is 1.75 kA/ms, whereas the for 100 mH, RRFC is 5.25 kA/ms. Due to the nonlinear characterises of the SA at higher fault current, the peak of TIV is slightly higher in comparison with value at the lower fault current. Similarly, the $L_{DC}$ affects the Δt. The lower inductance requires a shorter time for current zero during the fault neutralisation time. Moreover, the time of operation in mechanical DC CB is independent on the line inductor value.

The variation of the inductance causes energy stress in the SA, as depicted in figure 5.6 (f). The energy absorbed in the SA is given by 5.3. For the 300 mH, $\Delta t = \frac{V_{DC}\times t_{op}+I_0\times L_{DC}}{(k-1)\times V_{DC}} = \frac{525\times 5+2\times 300}{0.6\times 525\times 10^3} = 10.23\ ms$ and fault current rises to $I_f = I_0 + \frac{V_{DC}}{L_{DC}} t_{op} = 2\ kA + \frac{525}{300\times 10^{-3}} \times 5 \times 10^{-3}\ kA = 10.75\ kA$. Hence, the energy absorbed by the SA during fault suppression time is $E_{SA} = 1.6 \times 525\ kV \times \left(10.75 \times 10.23 + \frac{(1-1.6)\times 525\ kV)}{300\ mH} \times \frac{(10.23\ ms)^2)}{2}\right) = 46.22\ MJ$. The difference between the calculated and the simulated value is due to the I-V characteristics of SA. In conclusion, the energy absorbed by the DC CB with the lower line inductance is more than those with higher values of inductance.

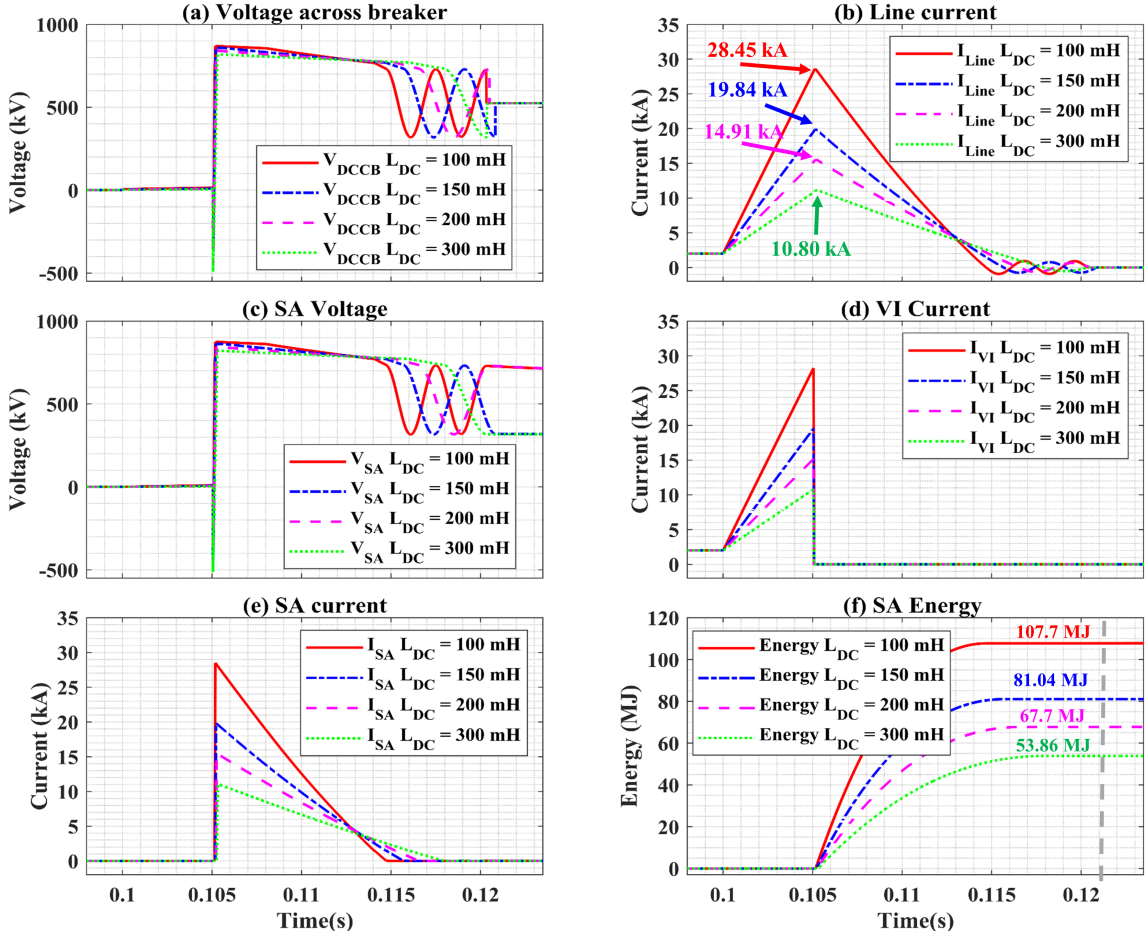



Figure 5.6: Effect of Line inductor ($L_{DC}$) in Mechanical DC CB on (a) voltage across breaker, (b) Line current, (c) surge arrester (SA) Voltage, (d) Vacuum interrupter (VI) Current, (e) SA current and (f) SA Energy

Figure 5.7 shows the effects of line inductor sizing on the performance of VARC DC CB. The ITIV is significantly larger for lower line inductance. The higher value of ITIV is due to the current zero in VI at a non-peak value of injected current as depicted in figure 5.7 (d). Hence, the voltage across the $C_P$ at this instant is non-zero, which causes a higher value of ITIV during the commutation period. The individual module produces the ITIV of 18.57 kV, as a result, net ITIV of the DC CB

is 130 kV for line inductance of 150 mH. Unlike in mechanical DC CB, time instant of peak TIV in VARC differs with the $L_{DC}$ value. The peak value of TIV in DC CB with Line inductance of 150 mH is delayed due to the lower value of injected current, causing an extra reversal of $V_{OSC}$ in VSC to reach the desired fault current limit as indicated in figure 5.7 (d).

Furthermore, the oscillation in the voltage across the DC CB, after fault current suppression time, arises due to the commutation of current back to the current injection branch from the energy absorption branch. The frequency of this oscillation depends upon the line inductor and the $C_P$. Hence, a line inductance of 150 mH causes oscillations with the frequency of 768.79 Hz, whereas a line inductance of 300 mH causes oscillations with a frequency of 543.61 Hz as shown in figure 5.7 (a). The energy absorbed by the DC CB with $L_{DC}$ = 300 mH is 21.5 MJ, whereas energy absorbed by the 150 mH is 34.16 MJ. The difference in the energy is due to the increase in the amplitude of fault current and decrease in fault current neutralisation time.

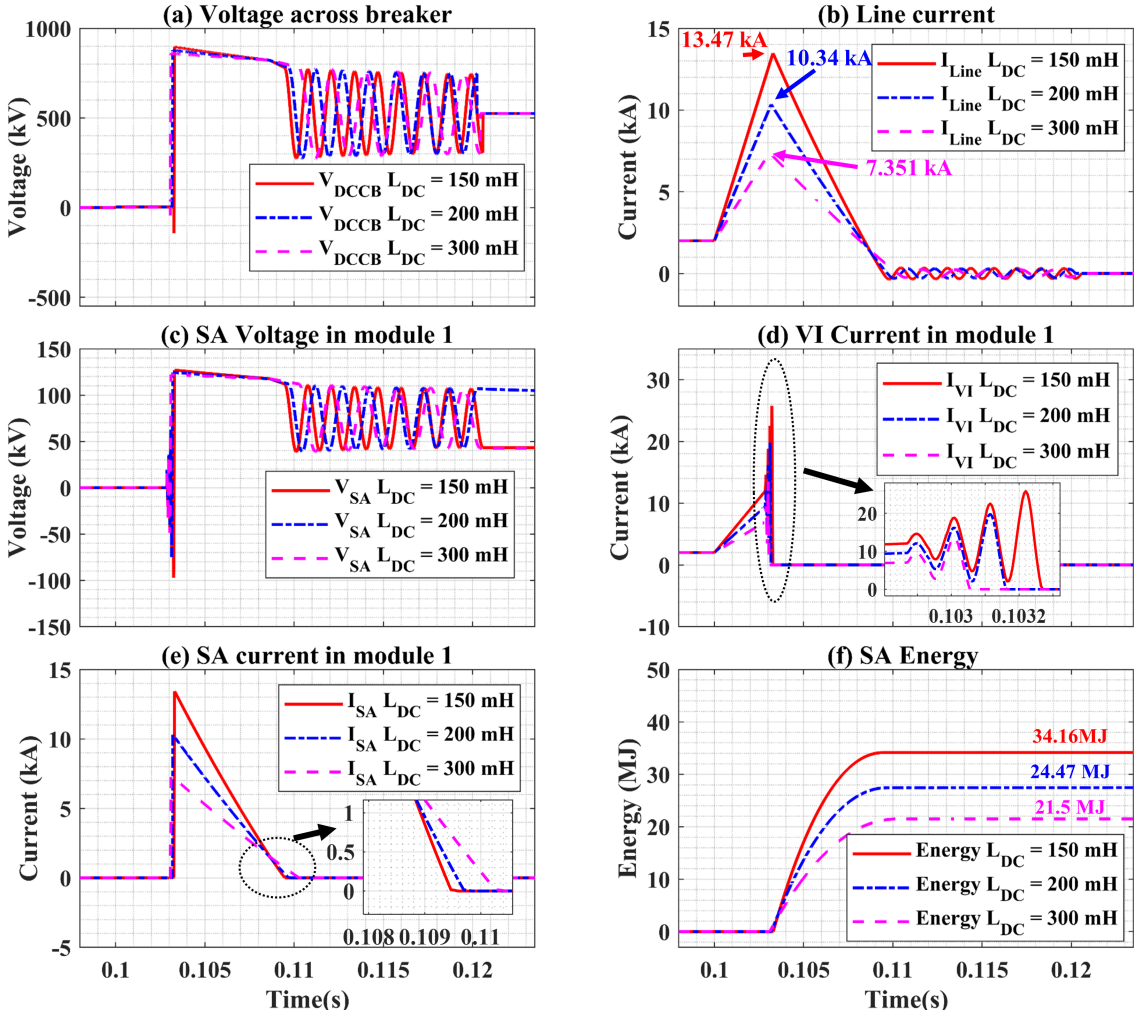



Figure 5.7: Effect of Line inductor ($L_{DC}$) in VARC DC CB on (a) voltage across breaker, (b) Line current, (c) surge arrester (SA) Voltage, (d) Vacuum interrupter (VI) Current, (e) SA current and (f) SA Energy

The energy absorbed by the SA arises from two significant sections of the network, namely from the source (AC in feed ) and energy stored elements. Hence the energy absorbed by the SA can be written in terms of these two sections. The energy absorbed in mechanical DC CB by the line inductor ($L_{DC}$) is given by

$$E_{L_{dc}} = \frac{1}{2} \times L_{dc} \times (I(t))^2 \tag{5.10}$$

Where

$$I(t) = I_0 \qquad 0 \geq t \geq t_1$$
$$I(t) = I_0 + \frac{V_{DC}}{L_{DC}}t \qquad t_1 \geq t \geq t_2$$
$$I(t) = I_f + \frac{(1-k)V_{DC}}{L_{DC}}t \qquad t_2 \geq t \geq t_3$$

From the above equations, we can find the maximum energy absorbed during the fault current suppression time to be $E_{L_{DC}} = \frac{1}{2} \times L_{DC} \times \left(I_0 + \frac{V_{DC}}{L_{DC}}t_2\right)^2 = \frac{1}{2} \times L_{DC} \times \left(I_f\right)^2$. However, at $t_3$ the total energy absorbed in the inductor will be zero, the energy is now commutated to the SA. The energy absorbed in the SA is given by

$$E_{SA} = E_{L_{DC}} + \int V_{DC} \times I(t)dt \tag{5.11}$$

$$E_{SA} = E_{L_{DC}} + V_{DC} \times I_f \times \Delta t + \frac{(1-k) \times (V_{DC})^2}{2 \times L_{DC}} \times (\Delta t)^2 \tag{5.12}$$

We can find the percentage of energy contributed by line inductor in SA Energy using (5.12). It is

Table 5.1: Percentage of energy contributed by $L_{DC}$ in mechanical DC CB

| $L_{DC}$ (mH) | (MJ) | % of Total Energy |
|---|---|---|
| 100 | 40.47 | 37.57 |
| 150 | 26.62 | 32.84 |
| 200 | 22.23 | 32.83 |
| 300 | 17.49 | 32.47 |

seen from table 5.1 that the energy provided by the $L_{DC}$ is about 40 % of the total energy. While the source provides the remaining energy during the fault. The percentage of the energy provided by the $L_{DC}$ can be calculated using (5.12) for VARC DC CB, and summarized in table 5.2, which indicates that the energy provided by $L_{DC}$ is about 40 % of the total energy. The variation of the

Table 5.2: Percentage of energy contributed by $L_{DC}$ in VARC DC CB

| $L_{DC}$ (mH) | (MJ) | % of Total Energy |
|---|---|---|
| 150 | 13.61 | 39.80 |
| 200 | 10.69 | 38.90 |
| 300 | 8.17 | 38.00 |

percentage of energy between the mechanical and VARC DC CB for the same value of inductance is due to the different operational time of the DC CB technology. With higher operational time, more energy is provided by the source.

## 5.6. Module failure (MF) and frequency of operation ($f_{op}$)

Due to modular topology of the VARC DC CB, all the modules must be operated within a given time margin. Any operation delay in modules causes energy stress in the sound modules. Similarly, failure of modules is sporadic [12] but can lead to voltage and energy stress on the DC CB, which can even further end up in failure of the entire DC CB. Hence, it is necessary to analyse the effects of module failure on the performance of VARC DC CB. With one module failure, the peak amplitude of

TIV across DC CB reduces to 780 kV. The reduced TIV is sufficiently higher than the system voltage i.e 525 kV. Thus the peak amplitude of the fault current remains the same as depicted by figure 5.8 (C). Furthermore, due to the loss of one module, fault current suppression time increases. As a result, the energy absorbed by the DC CB increases by 15.07 MJ from the reference case (without any module failure ). As far as the peak amplitude of fault current is the same, the ITIV remains unaffected. Two module failures cause extremely higher energy stress in the sound modules. The energy increases by 2.5 times the reference case as depicted in figure 5.8 (a). With two module failure, the TIV drops by 260 kV. As a result, the fault current suppression time and total energy absorbed by the DC CB increases. However, the failure of more than 2 modules leads to failure of the entire breaker as discussed in the re-strike case.

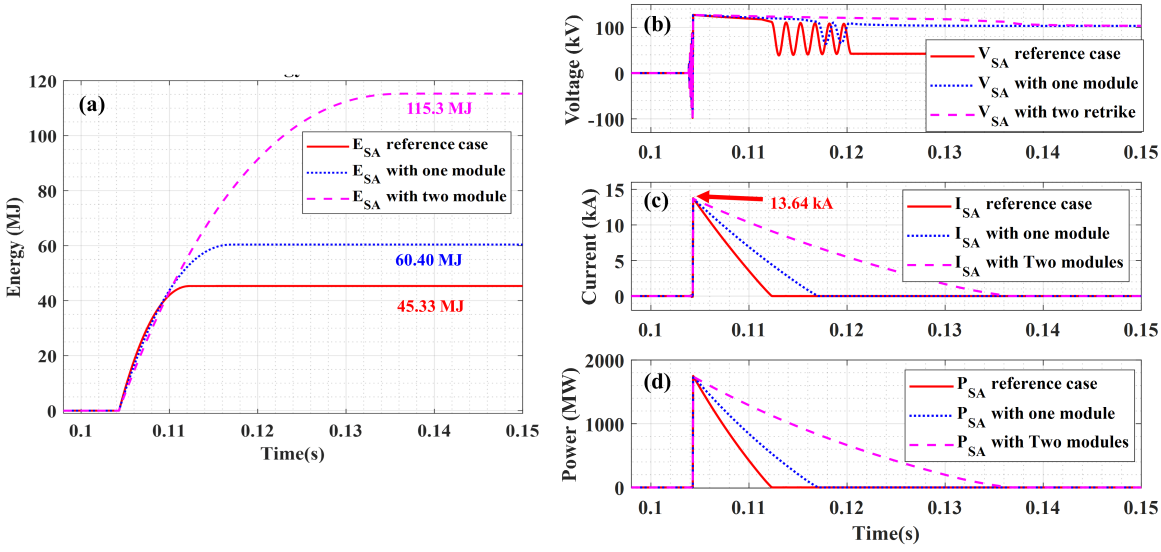



Figure 5.8: Effect of module(s) failure in VARC DC CB on (a) Total energy absorbed by DC CB (b) voltage across SA in module 1 (c) current in SA in module 1 and (d) power in SA in module 1

During the designing, the breaker is designed to operate for at least two operations in quick sequence. For the mechanical DC CB, energy absorption after two operations will be twice the energy absorbed during the first absorption. Similar arguments hold true for the VARC breaker. Thus, the energy absorbed by the SA during the first operation is 70 MJ and after the second operation, it will be 140 MJ. For VARC DC CB, the value will be 54 MJ.

## 5.7. Summary and Discussions

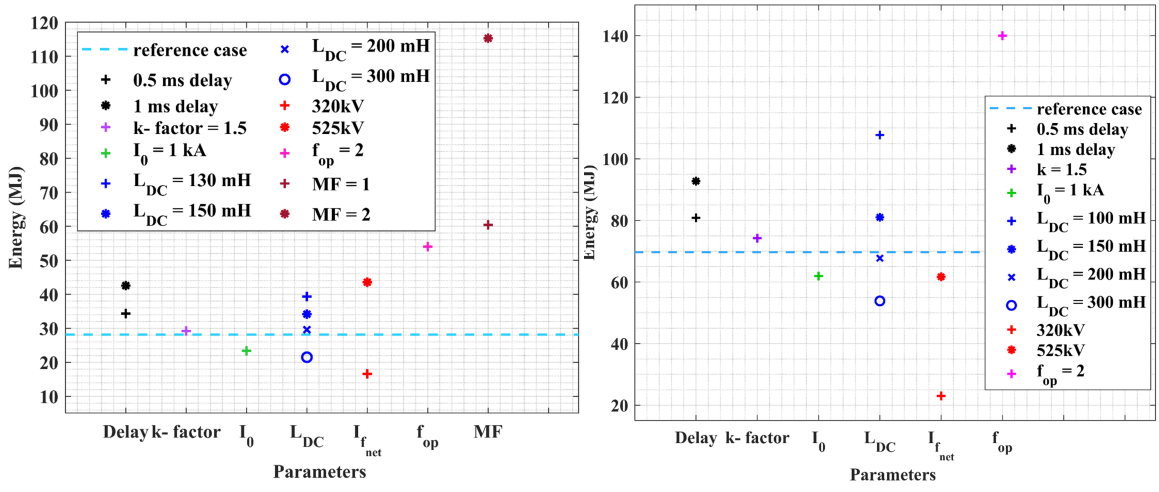
This chapter has investigated the dependence of the number of multi-column SAs in both DC CB technologies on various parameters. It also examined the performance of DC CB under the variation of system and circuit parameters.

The results of this study indicate that the energy absorbed by SA in both technologies depends upon system voltage, fault neutralisation time, characteristics of SA, steady-state current and Line inductor. Based on the previous discussion for each parameter, we can compare the energy absorbed by each technology and summarise it in figure 5.9. The reference case is the initially designed DC CB for a 525 kV as discussed in chapter 2 and 3.

In both DC CB technologies, $k - factor$ has the least effect on energy absorption. Similarly, reduction in the steady-state current ($I_0$) from 2 kA to 1 kA has minimum effect on the energy absorption in both DC CB technologies as depicted in figure 5.9. Neglecting the failure scenarios (namely, consequent two operations of the breaker ($fop$) and module failure), occurrence operation delay in the VARC DC CB acts as worst-case while in mechanical DC CB, the change in line inductances are more severe. However, for 525 kV MTDC network, the energy absorbed in VARC DC CB corresponding to a pole to pole fault near MMC, lead to a higher value.

Upon considering the failure cases, module failure leads to a higher energy absorption due to

reduced TIV and higher fault current neutralisation time in VARC DC CB. While in mechanical DC CB, consequent two operations $f_{op}$ of the breaker leads to higher energy absorption due to failure in the first attempt.




(a) (b)

Figure 5.9: Comparison of Energy absorbed due to different parameter variation in (a) VARC DC CB and (b) Mechanical DC CB

The estimation of the multi-column SAs in parallel can be done by considering the higher energy absorbed due to the variation of different parameters. With respect to the failure scenarios, module failure and frequency of breaker operation is considered for the estimation. $One\ cm^3$ of surge arrester ZnO based surge arrester can dissipate around $200\ J$ of energy , which is considered as the thumb rule for the calculation [6]. Hence, the number of multi-column SAs is given as

$$Number\ of\ multi-column\ SAs = \frac{highest\ energy\ absorbed\ among\ the\ Cases\ (MJ)}{16 \times 10^3 \times 200\ J}$$

The number of parallel SAs required for VARC DC CB per module are $\frac{115.3\times10^6}{5\times16\times10^3\times200} = 7.2 \cong 8$. Whereas in mechanical DC CB, the number of parallel SAs are $\frac{140\times10^6}{16\times10^3\times200} = 43.75 \cong 44$.

However, without considering the failure scenarios, the highest energy absorbed is 42.58 MJ in VARC DC CB and in mechanical DC CB, it will be 107.70 MJ. Thus, the number of parallel SAs for one VARC DC CB module will be two, and for mechanical it will be 34.

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# 6

# Co-ordination performance of different DC CB technologies in MTDC networks

*This chapter investigates the co-ordinative performance of VARC and Mechanical DC CB in two multi-terminal DC (MTDC) networks. Further, a selection methodology is discussed for MTDC network based on the energy, fault current, MMC's blocking status and MMC's operating mode.*

## 6.1. 4- Terminal test MTDC network layout

Figure 6.1 illustrates the 4-terminal test MTDC network, which is used for the fault current analysis. The converters used are half-bridge modular multilevel converters (MMC). The entire MTDC network is divided into two zones, onshore and offshore. The onshore consist of MMC 1 and MMC 2, which are then connected to the 400 kV AC grid via a transformer. The offshore grid consists of MMC 3 and 4, which are connected to the wind farms. The Onshore AC grids are independent voltage source. The MTDC network is configured as symmetric monopolar with ±320 kV dc voltage. The parameters of the MTDC network are indicated in table 6.1.

Four cables connect the Onshore and Offshore zone. The cable 12 with a length of 175 km, connects MMC 1 and MMC 2. While the MMC 3 is connected by a 350 km long cable to MMC 1, whereas another offshore zone MMC is connected to MMC 1 via a 300 km long cable. Both the offshore MMCs are connected via a 100 km long cable. The DC reactor, with the value of 10 mH, is installed between MMC and the bus. At each of the buses, which are indicated with the help of red dotted rectangles, we have a line inductor and a DC CB. The value of line inductance is 100 mH [1, 2]. This network uses 320 kV XLPE insulated cable with surge impedance of 33.73 Ω and a wave propagation velocity of $1.83 \times 10^8$ m/s. The frequency dependent phase model is used to represent cable in the PSCAD software.

The MMC used in this network is based on the continuous MMC model. The outer control loop of the MMC 1 and 3 controls the voltage, while MMC 2 and 4 controls the power. The MMC utilizes two protection strategies, first, the MMC gets blocked, if the maximum arm current exceeds 0.8 times the maximum current handling limit of the IGBTs and secondly, if the MMC voltage falls below 0.8.p.u, then the MMC is blocked either.



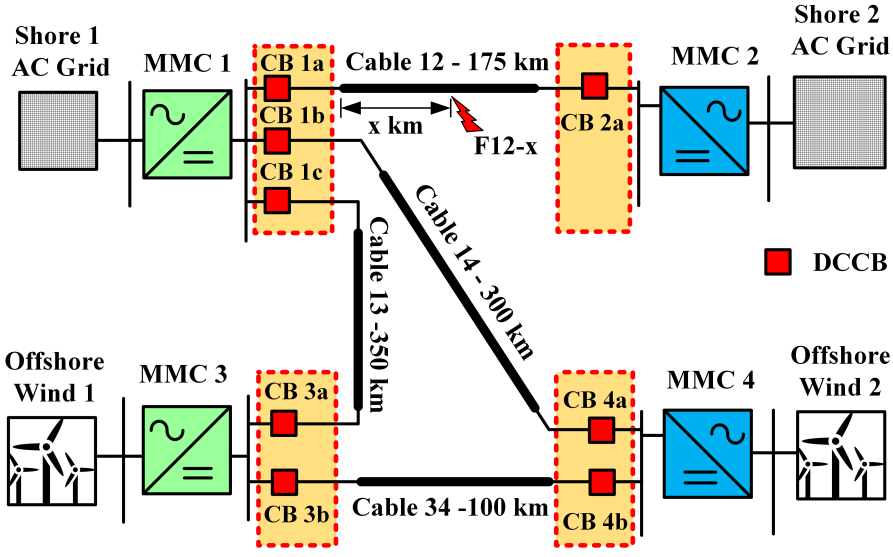


Figure 6.1: 4- Terminal test MTDC network

## 6.2. 4- Terminal TenneT MTDC network layout

Figure 6.2 shows the 4 - Terminal TenneT MTDC network, which is used for the fault current analysis. The converters used are half-bridge modular multilevel converters (MMC). The entire MTDC network is divided into two zones, onshore and offshore. The onshore consist of MMC 1 and MMC 3, which are connected to the 380 kV AC grid via a $\Delta/Y$ transformer with a voltage ratio of 380 kV/250 kV. The offshore grid consists of MMC 2 and 4, which are connected to the wind farms. Due to a lower voltage level of the wind farm, a 250 kV/66 kV $\Delta/Y$ transformer is used to step up the voltage level. The Onshore AC grids are independent voltage sources, which represents a stable grid. The MTDC network is configured as bipole with metallic return with ±525 kV DC voltage. The parameters of the MTDC network are indicated in table 6.1.

Table 6.1: Data of 4- Terminal test MTDC network

| Parameter | Converters | | | |
|---|---|---|---|---|
| | MMC 1 | MMC 2 | MMC 3 | MMC 4 |
| **Active power** | 500 MW | 500 MW | 500 MW | 500 MW |
| **Control mode** | PVdc | PVdc | PQ | PQ |
| **Reactive power** | 100 MVAR | 100 MVAR | 100 MVAR | 100 MVAR |
| **DC link Voltage** | ±320 kV | | | |
| **Rated power** | 1256 MW | | | |
| **Number of Submodules per arm** | 400 | | | |
| **Arm capacitance Carm** | 22 μF | | | |
| **Arm reactor Larm** | 42 mH | | | |
| **Arm resistance Rarm** | 0.544 Ω | | | |
| **AC converter voltage** | 400 kV | | | |
| **Transformer leakage reactance** | 0.18 p.u | | | |
| **AC grids and windfarms** | | | | |
| **AC grids voltage** | 400 kV | | | |



Four cables connect onshore and offshore zone. The cable 12 with a length of a 200 km connects MMC 1 and MMC 2. While the MMC 3 is connected by a 200 km long cable to MMC 1. Both the offshore MMCs are connected via a 10 km long cable. The MMC 1 is connected with MMC 3 by a 200 km long cable. Each MMC consists of a DC rector with the value of 25 mH and at each bus, which is indicated by the red rectangle, we have a line inductor and a DC CB. The value of the line inductance is 200 mH. This network uses 525 kV XLPE insulated submarine cable with surge impedance of 60.71 Ω and a wave propagation velocity of $1.76 \times 10^8$ m/s. The frequency dependent phase model is used to represent the cable in the PSCAD software.

The MMC used in this network is based on the detailed equivalent circuit models (Type 4) [3]. The outer control loop of the MMC 1 and 3 controls the voltage, while MMC 2 and 4 controls the power. Power is injected into the DC grid by the MMC 2 and 3 and fed back to the AC grid by MMC 1 and 2. The MMC utilizes two protection strategies, first, MMC is blocked, if the maximum arm current exceeds 0.8 times the maximum current handling limit of the IGBTs and secondly, if the MMC voltage falls below 0.8.p.u, then the MMC is blocked either. Fault detection and generation of a trip signal, occur at the same instant. The fault impedance is resistive with a value of 10 mΩ.

## 6.3. Fault current analysis in MTDC networks

The fault in a cable is more likely to occur, in comparison with a fault in the rest of the network. This is due to the dielectric deterioration and breakdown in the cable [4]. The fault current amplitude varies with the type and location of the fault. Similarly, the nature and amplitude of fault impedance also affects the amplitude. The peak value of the fault current also depends upon the fault neutralization time. The analysis of the DC fault cases are based on the type of fault, location of the fault and fault neutralization time. Fault neutralization time is referred to as the operation delay in the rest of the text. This section studies two types of fault, one, cable short circuit, i.e. pole to pole and the second, pole to ground fault. The location of the fault is considered in terms of percentage of the cable length.

Figure 6.3 illustrates the fault case scenarios performed in the 4 - Terminal test MTDC network. The type of the fault is denoted as PP and PG, representing the pole to pole fault and pole to ground fault respectively. Due to similarity in the results, the pole to pole to ground fault is not considered in this analysis. The terminology used in the plot should be interpreted as follows: for example, the notation PP12 3ms indicates a pole to pole fault on cable 12 where 1 is the starting and 2 is the ending node of cable, with an operation delay of 3 ms. Due to the symmetrical monopole, the total line inductance reduces by a factor 2 during the PG fault, which results in the lower peak amplitude than Pole to pole fault. With the increase in the operation delay, there is a notable difference

Table 6.2: Data of 4- Terminal TenneT MTDC network

| Parameter | Converters | | | |
|---|---|---|---|---|
| | MMC 1 | MMC 2 | MMC 3 | MMC 4 |
| **Active power** | 1000 MW | 1000 MW | 1000 MW | 1000 MW |
| **Control mode** | PVdc | PQ | PVdc | PQ |
| **Reactive power** | 0 MVAR | 0MVAR | 0 MVAR | 0 MVAR |
| **DC link Voltage** | ±525 kV | | | |
| **Rated power** | 1200 MW | | | |
| **Number of Submodules per arm** | 656 | | | |
| **Arm capacitance Carm** | 22 μF | | | |
| **Arm reactor Larm** | 42 mH | | | |
| **Arm resistance Rarm** | 0.08 Ω | | | |
| **AC converter voltage** | 250 kV | | | |
| **Transformer leakage reactance** | 0.18 p.u | | | |
| **AC grids and windfarms** | | | | |
| **AC grids voltage** | 380 kV | | | |
| **Windfarm output voltage** | 66 kV | | | |

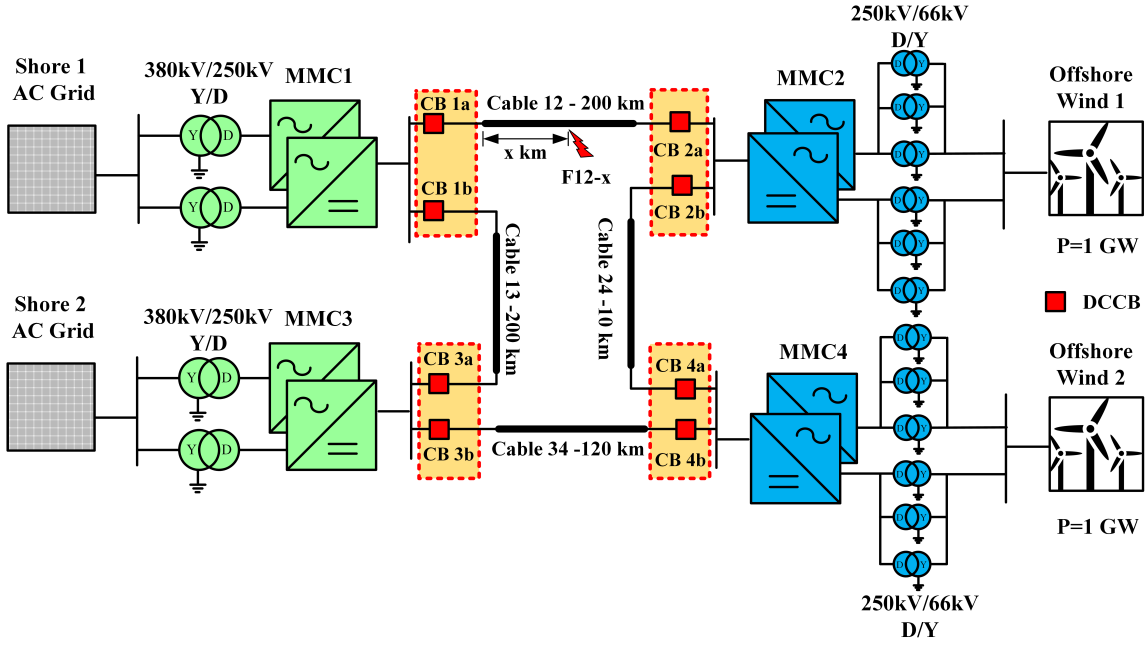


Figure 6.2: 4- Terminal TenneT MTDC network

between the peak amplitude of fault current during PP and PG fault. This difference occurs due to the infeed of the AC power. The cable fault in cable 12, cable 13 and cable 14 has a significantly higher amplitude of fault current near MMC 1 in comparison to the other locations in the same cable. In addition, a cable short circuit at terminals of MMC 1 in cable 12 leads to a peak fault current of 8.9 kA for an operation delay of 3 ms and 12.7 kA an operation delay of 5 ms and energy absorbed is 16.6 MJ and 23 MJ respectively. Hence,a terminal cable short circuit in this network is the worst fault as it yields the highest fault current.

In 4 - Terminal TenneT MTDC network, the amplitude of the fault current for a pole to pole fault near the MMC 1 and 3 is higher than those produced by faults in rest of the network, this can be clearly seen in figure 6.4. With the variation of the fault location on the cable, the amplitude of the

fault current changes. This change is due to the variation of the impedance seen by MMCs at both ends of the cable. Hence, a fault occurring at 50% of the total length will result into a fault current with lowest possible amplitude. However, due to the shorter length of cable 34, fault currents in the cable 34 have a near constant amplitude for all the locations.

During the first few milliseconds, the fault current is determined by the energy in the storage elements of the MTDC network. Hence, for the first few milliseconds, the fault current remains constant for different fault location in all the cables. However, with the passage of time, the amplitude of the fault current near onshore terminals increases due to the in-feed of AC power as starts acting as a rectifier.



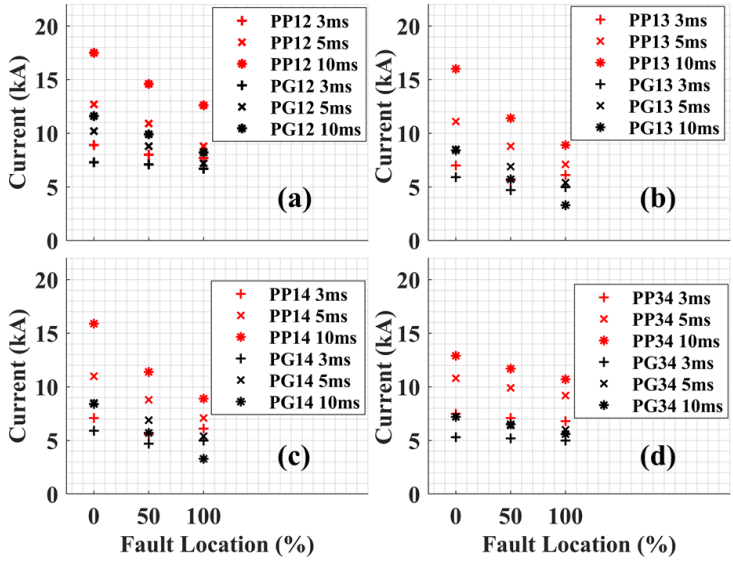


Figure 6.3: Summarization of the possible pole to pole and pole to ground faults with different operation time in 4- Terminal test MTDC network. (a) fault in cable 12 (b) fault in cable 13 (c) fault in cable 14 and (d) fault in cable 34

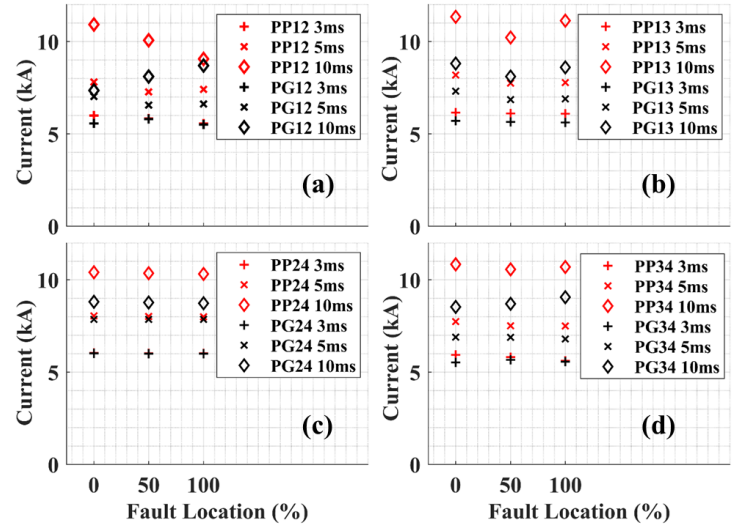


Figure 6.4: Summarization of the possible pole to pole and pole to ground faults with different operation time in 4- Terminal TenneT MTDC network. (a) fault in cable 12 (b) fault in cable 13 (c) fault in cable 24 and (d) fault in cable 34

## 6.4. Co-ordinative performance of DC CBs in 4- Terminal test MTDC network

Based on the faults considered in Section 6.3, four cases are considered on the worst fault cable 12 and cable 13, with two typical DC CBs at each end of the faulty cable. The following case studies are conducted on the Multi-terminal network. In the cases below, i and j represent the start and the endpoint of cable.

- **Case 1** : Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC i and VARC DC CB within 3 ms operational delay is introduced at the bus of MMC j.
- **Case 2** : Mechanical DC CB with 8 ms operational delay is introduced at the bus of MMC i and VARC DC CB with 3 ms operation delay is introduced at the bus of MMC j.
- **Case 3**: Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC i and Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC j.
- **Case 4**: VARC DC CB with 3 ms operational delay is introduced at the bus of MMC i and VARC DC CB with 3 ms operation delay is introduced at the bus of MMC j.

Table 6.3: Maximum fault current in a cable (worst scenarios in red)

| Location | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| Cable 12 | 13.11 kA | 16.72 kA | 13.11 kA | 8.69 kA |
| Cable 13 | 11.38 kA | 15.07 kA | 11.38 kA | 7.3 kA |
| Cable 14 | 11.18 kA | 14.8 kA | 11.18 kA | 7 kA |
| Cable 34 | 10.7 kA | 12.1 kA | 10.7 kA | 7.5 kA |



### 6.4.1. Interruption performance

Figure 6.5 shows the current and the voltage waveforms in CB 1a for the pole to pole fault on cable 12 near MMC 1. The $I_{Line}$ in case 2, has the most considerable magnitude of the current, due to slower breaking near MMC 1. The effect of the travelling wave is not as significant as the fault located near CB 1a. Hence, the rise of the fault current is linear. During the interruption, in case 2, as the capacitor charged with opposite polarity causes a rise of the current up to 34 kA in VI. However, in the case of VARC CB this rise reaches up to 18 kA with a high frequency growing oscillation in VI. During the fault current suppression, the time is determined based on the interrupted current. Hence, VARC has the least fault current suppression time in comparison with a mechanical circuit breaker with an operational delay of 8ms. The voltage across the VI, during the fault current suppression time remains the same for all the cases. Moreover, the amplitude of ITIV depends on the magnitude of the current in VI. For the mechanical CB, the higher current is interrupted, the lower is the ITIV [5]. There is a significant oscillation in the $V_{vi}$ for all cases except for case 2 after the fault current zero.

The fault located near MMC 1 has an effect on the current and the voltage waveforms in CB 2a as depicted in figure 6.6, For $I_{Line}$, the effect of travelling waves is visible and it changes the fault current rise rate non-linearly. For case 3, the presence of the mechanical circuit breaker with an operational delay of 5ms has peak amplitude of 6.9 kA at 1.0064 s. It is observed that, during the fault current suppression time for case 1, 2 and 4, the drop in the current is non-linear, and this is due to the travelling wave phenomena. Although, this effect is not seen in case 3, a significantly large ITIV is observed with an amplitude of -260 kV

For a fault that occurs in cable 13 near the MMC 1, identical waveforms are observed primarily in CB 1b. However, due to the similar voltage polarity of the DC capacitor for the mechanical DC breaker, there is no overshoot as it can be seen in CB 1a for current $I_{VI}$. Furthermore, significant changes can be seen in CB 3a as depicted in figure 6.7. For case 2, the fault current rises to 8.4 kA

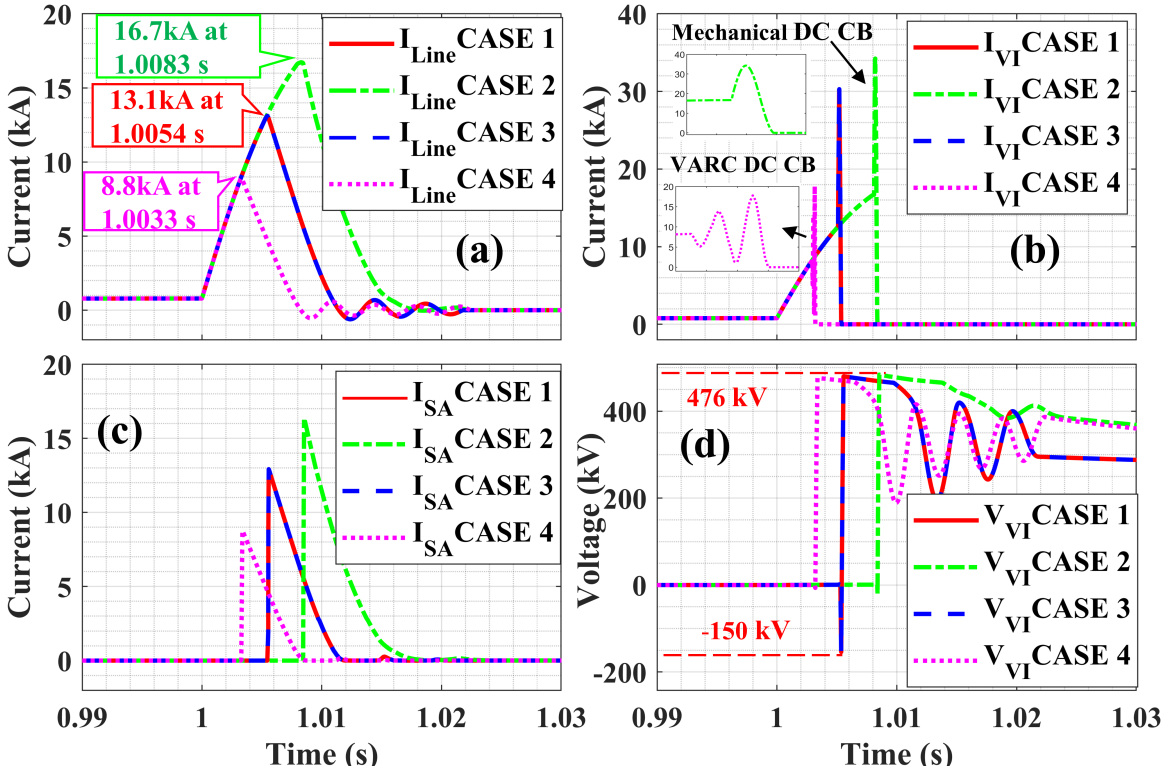


Figure 6.5: Current and voltage waveforms in CB 1a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the surge arrester (SA). (d) Voltage (in kV) across the VI.

due to the presence of a mechanical circuit breaker with an operational delay of 5 ms. Similarly, the fault current is quickly damped after the current zero. A non-linearity is observed in the SA current due to travelling waves as the distance is considerable, i.e. 350 km, however, case 3 is severely affected by it. The oscillation in $V_{VI}$ after the current zero reaches lower amplitude in comparison with figure 6.5.

### 6.4.2. MMC's Blocking Status

Table 6.4 illustrates the blocking status of the MMC. It is observed that among all the cases, for various fault locations, case 1 and case 4 do not block the converter. However, it is interesting to see that a fault that occurs on line 34 is mitigated for all of the cases except for case 2. This is due to the fact that the power flow between MMC 3 and MMC 4 is zero during the steady state. Hence, there is sufficient time for the current to reach the fault location.

### 6.4.3. Energy absorption

The total energy which is absorbed by the SA is contributed by two sources: the magnetic energy stored in the DC current limiter and the energy stored in the network. The energy stored in the DC current limiter is $\frac{1}{2}L_{DC}I_f^2$, which is the electrical energy supplied from the network during the fault current suppression. In some cases, the energy resulting from the grid side is even larger than the energy stored in the DC current limiter, because of the network voltage recovery during the energy period. Figure 6.8 shows the energy absorption by the DC CBs situated at different location for various case scenarios during a pole to pole fault. The amount of energy absorbed depends on the operational speed of the DC CB, as shown by case 4 , wherein the fastest topology absorbs least amount of energy in comparison with other cases. The energy absorption with different fault location is nearly constant. Similarly, in Case 3 the converter is not blocked, and the maximum energy absorbed by the SA is below 16 MJ. For the selection of the DC CB technology based on the energy absorbed, a line can be drawn. A faster case i.e. case 4 can be used for cable 12 as the

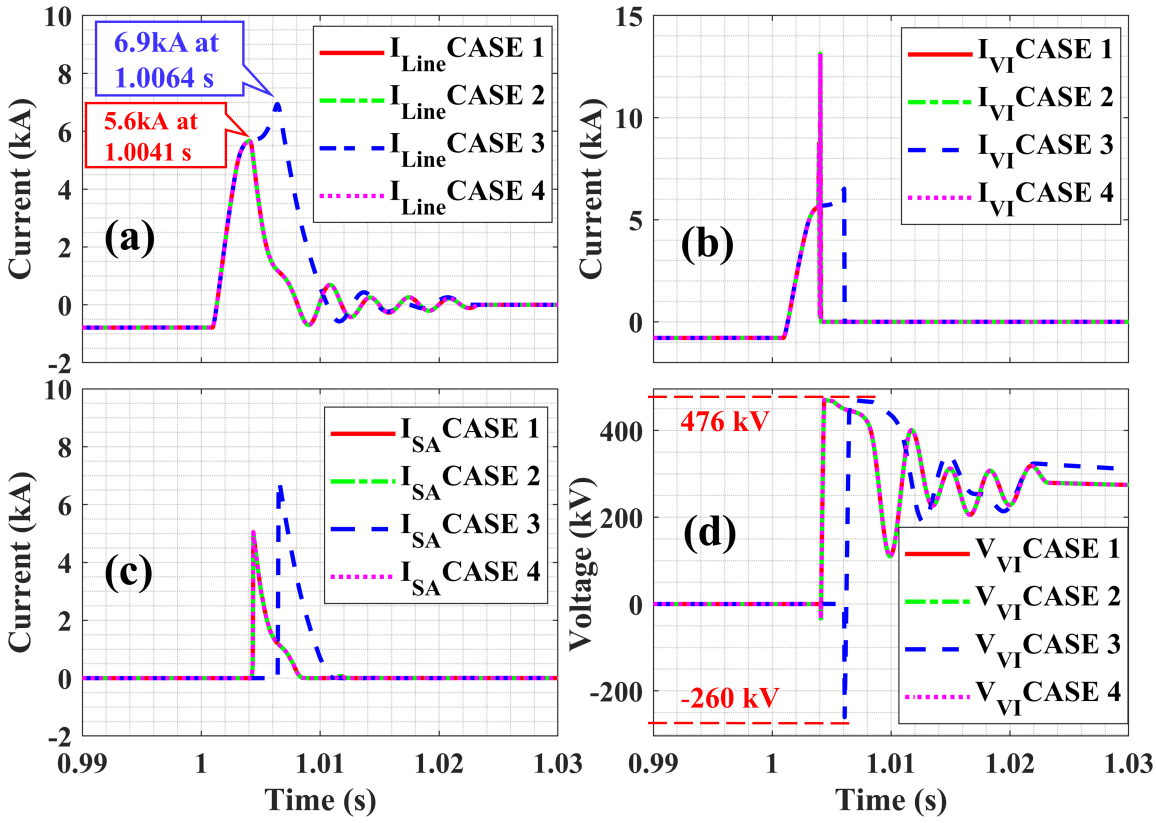


Figure 6.6: Current and voltage waveforms in CB 2a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the Surge arrester (SA). (d) Voltage (in kV) across the VI

Table 6.4: Blocking status of MMC for various case scenarios in 4- Terminal test MTDC network

| Location | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| Cable 12 - 0 | - | MMC 1 | - | - |
| Cable 12 - 50 | - | MMC 1 | - | - |
| Cable 12 - 100 | - | - | MMC 2 | - |
| Cable 13 - 0 | | MMC 1 | - | - |
| Cable 13 - 50 | - | - | - | - |
| Cable 13 - 100 | - | - | MMC 3 | - |
| Cable 14 - 0 | - | MMC 1 | - | - |
| Cable 14 - 50 | - | - | MMC 1 | - |
| Cable 14 – 100 | - | - | MMC 4 | - |
| Cable 34 - 0 | - | - | MMC 4 | - |
| Cable 34 - 50 | - | - | MMC 4 | - |
| Cable 34 - 100 | - | - | MMC 4 | - |

energy absorption difference between the opposite breakers (CB 1a and CB 2a) is larger. However, for cable 13 and cable 14, the difference in the absorbed energy is smaller, hence case 1 is found as suitable. Similarly, for cable 34, case 2 can be used. Figure 6.9 shows the selection of DC CB based on the status of MMC blocking, fault current, energy absorbed and operating time of DC CB. Each cable is divide into two zones i.e. Zone 1 and Zone 2. If a fault occurs in Zone 2, then either of the fast and slow breakers can be used for the terminal closest to the fault. However, if it lies in Zone 1, only fast breaker is employed. For example, consider a pole to pole (PP) fault at MMC 1 in cable

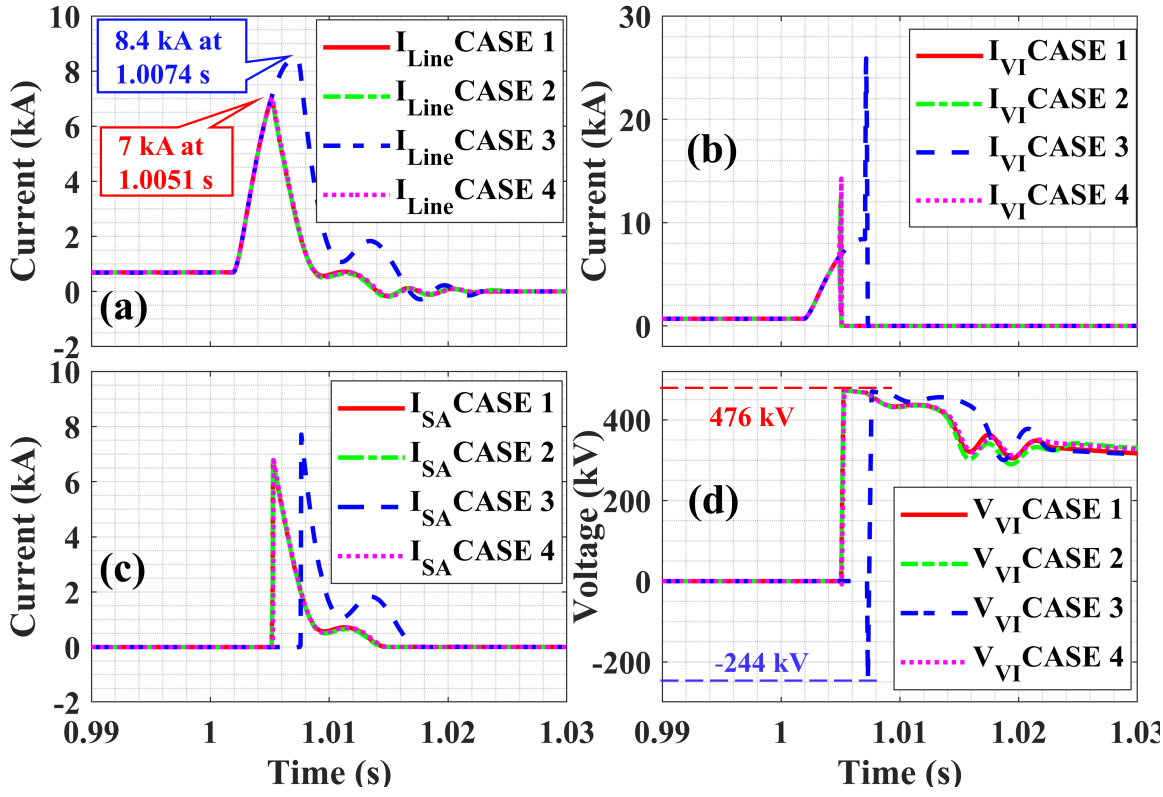


Figure 6.7: Current and voltage waveforms in CB 3a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the Surge arrester (SA). (d) Voltage (in kV) across the VI

12, at 5 ms the current level violates Zone 2 region. Hence it is suggested that fast breaker should be used at MMC 1 terminal. Although, PP fault near MMC 2 on the same cable does not violate zone limits, thus, either of the fast and slow breakers can be used.

## 6.5. Co-ordinative performance of DC CBs in 4 - Terminal TenneT MTDC network.

The methodology discussed in the previous section can be applied in 4 - Terminal TenneT MTDC network. In this network, the cable 12 and 13 show higher fault current levels as illustrated in figure 6.4. Considering this fact, two typical DC CBs are placed at each end of the cable. The following case studies are conducted on the Multi-terminal network. In the cases below, i and j represent the start and the endpoint of cable.

- **Case 1**: VARC DC CB with 3 ms operational delay is introduced at the bus of MMC i and Mechanical DC CB within 5 ms operational delay is introduced at the bus of MMC j
- **Case 2**: VARC DC CB with 3ms operational delay is introduced at the bus of MMC i and Mechanical DC CB with 8 ms operation delay is introduced at the bus of MMC j.
- **Case 3**: Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC i and Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC j.
- **Case 4**: VARC DC CB with 3 ms operational delay is introduced at the bus of MMC i and VARC DC CB with 3 ms operation delay is introduced at the bus of MMC j.

It can be seen from the data in table 6.5, that the cable 13 shows higher fault current level in two cases, namely case 3 and case 4 whereas case 1 and case 2 has a higher fault current with an amplitude of 7.55 kA and 9.90 kA in cable 24 and cable 34.

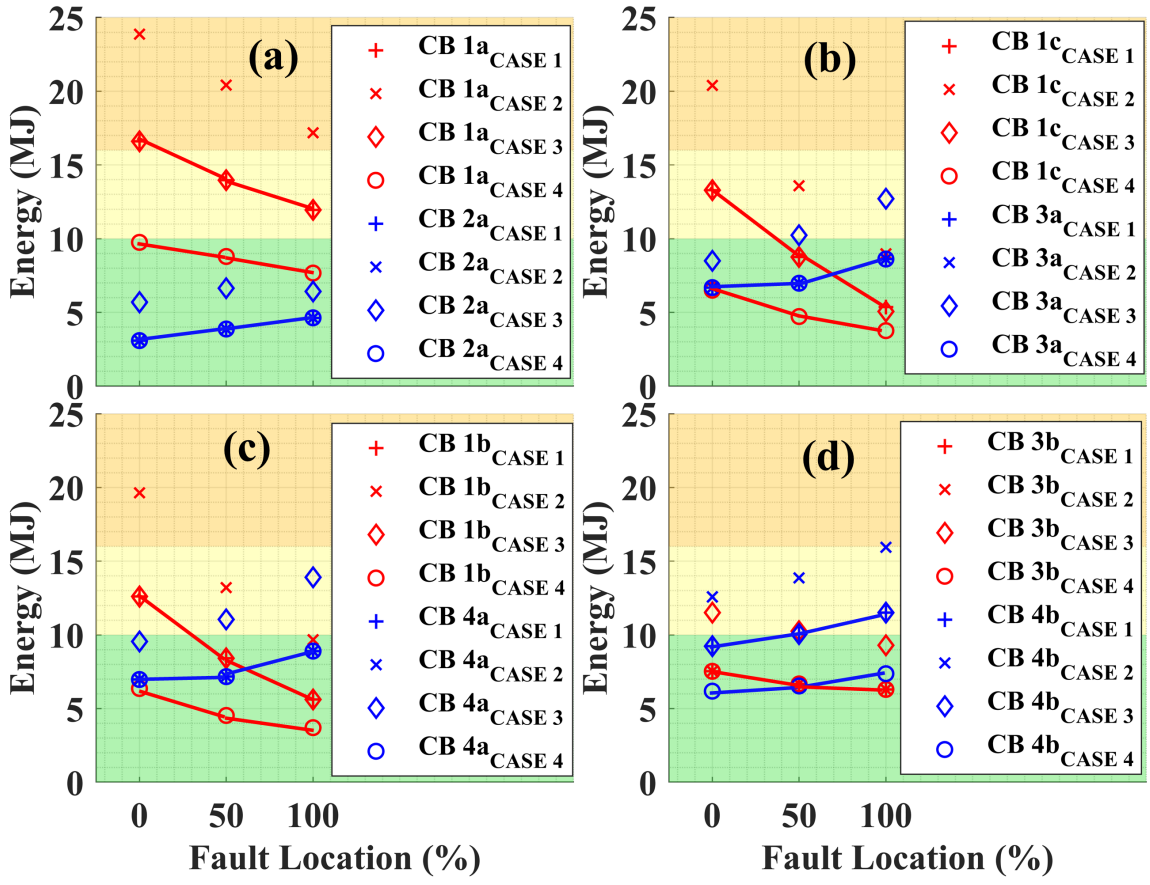


Figure 6.8: Energy absorbed in the grid by DC CBs during various case scenarios in (a) Cable 12. (b) Cable 13. (c) Cable 14. (d) Cable 34.

Table 6.5: Maximum fault current in a cable (worst scenarios in red)

| Location | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| Cable 12 | 7.00 kA | 9.40 kA | 7.80 kA | 5.76 kA |
| Cable 13 | 7.02 kA | 8.51 kA | 8.18 kA | 5.88 kA |
| Cable 24 | 7.55 kA | 8.73 kA | 8.04 kA | 5.18 kA |
| Cable 34 | 7.39 kA | 9.90 kA | 7.74 kA | 5.11 kA |

### 6.5.1. Interruption performance

Figure 6.10 shows the current interruption in DC CB 1a during the pole to pole fault near MMC 1 for various cases. The fault occurs at the 1.6 s, and the fault current rises with the rate of 1.82 kA/ms. Due to the presence of VARC DC CB near MMC 1 in case 1, 2 and 4, the fault current reaches a peak value of 5.01 kA and then commuted into the energy absorption at 1.604 s. Also due to the increase of the amplitude of injected current after every reversal in VARC DC CB, the current in VI reaches a peak of 8.55 kA as indicated in figure 6.10 (b). The presence of mechanical DC CB with an operating time of 5 ms, the rise of fault current is higher as indicated in the figure in case 3.

Upon commutating into SA, the voltage across the VI rises to 825 kV. Furthermore, the value of ITIV in case of VARC is lower, as fault current is interrupted at the instant when the voltage across the oscillating capacitor ($C_P$) is zero. However, due to the charged $C_P$, the mechanical DC CB produces ITIV with an amplitude of -454 kV as depicted in the figure. The oscillation in voltage across VI ($V_{vi}$) after fault current suppression is due to the interaction of the breaker capacitor and

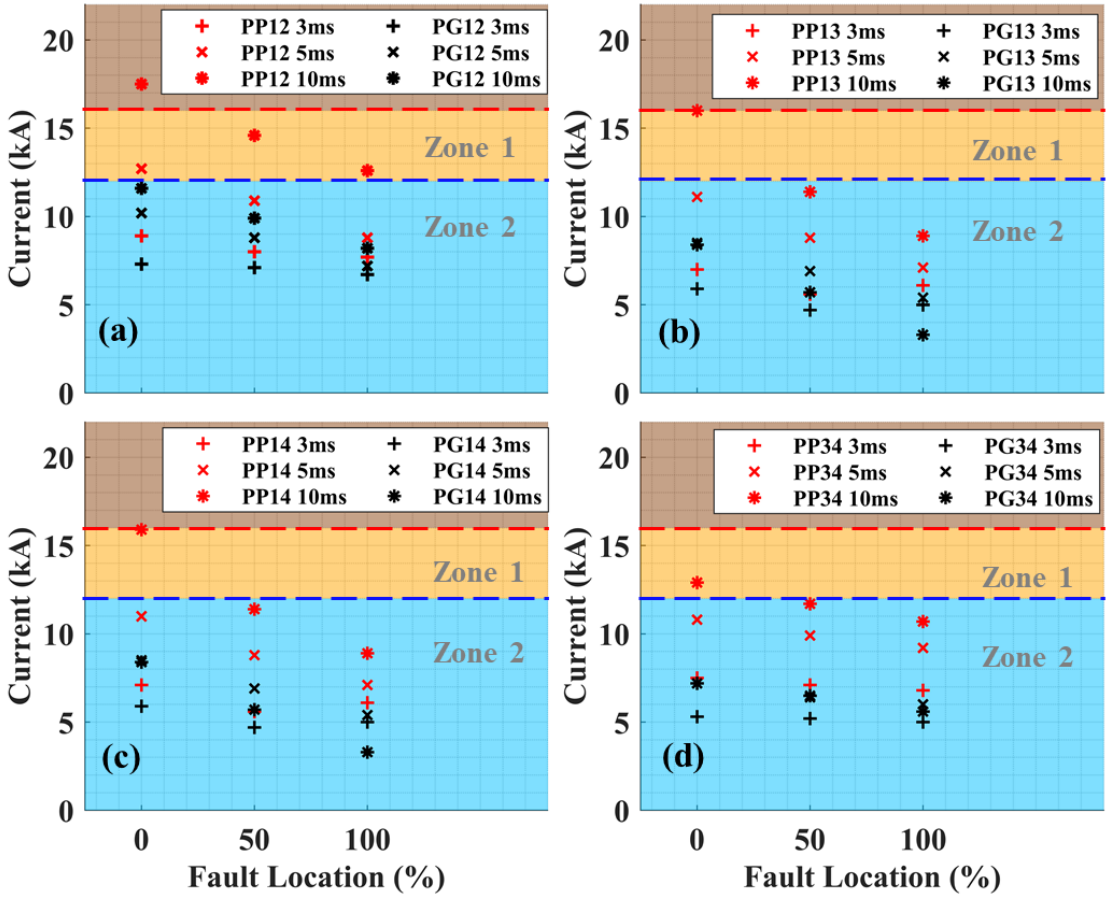


Figure 6.9: Selection of DC CB in (a) cable 12 (b) cable 13 (c) cable 14 and (d) cable 34

the network inductor. The frequency of this oscillation is $f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{225\ mH \times \frac{2\ \mu F}{7}}} = 627.72\ Hz$. It is also observed that the SA conducts after 1.61 s for a defined duration. The conduction of SA results from the variation of voltage at MMC 1 terminals. Due to the fault, MMC 1 goes into the transient state, which results in redistribution of power and causes oscillation in the voltage. Since the voltage at fault end of the DC CB remains constant, the net voltage across the SA Varies with the variation in bus voltage. As the voltage across SA reaches the knee point, the SA conducts and provides extra damping to the network. Further, re-clamping of SA is not observed in VARC due to fast current interruption. Because of the terminal short circuit, the effect of travelling waves is not observed in the fault current.

Figure 6.11 shows the performance of the DC CB 2a during the pole to pole fault near the MMC 1 on cable 12. Since the distance between the fault and breaker is 200 km apart, the rise of fault current is delayed. The time delay can be calculated from the cable distance and the speed of propagation of the electromagnetic wave, which results in the delay of 1.1 ms. The fault current reaches to 6.91 kA in case 1 and 3 due to the presence of mechanical DC CB with operation delay of 5 ms. In case of a mechanical DC CB with an operational delay of 8 ms, the fault current is higher in comparison with all other cases and exhibits a peak value of 9.40 kA. Similarly, in case 4, the fault current reaches an amplitude of 5.70 kA. Interestingly, the line current ($I_{Line}$) has a local peak at 1.6034 s for all cases. This second peak is due to the return of travelling wave.

The current in VI in case 4 reaches the peak amplitude of 12 kA due to injected current from the current injection branch. However, the voltage across the oscillating capacitor ($C_P$) is non zero at

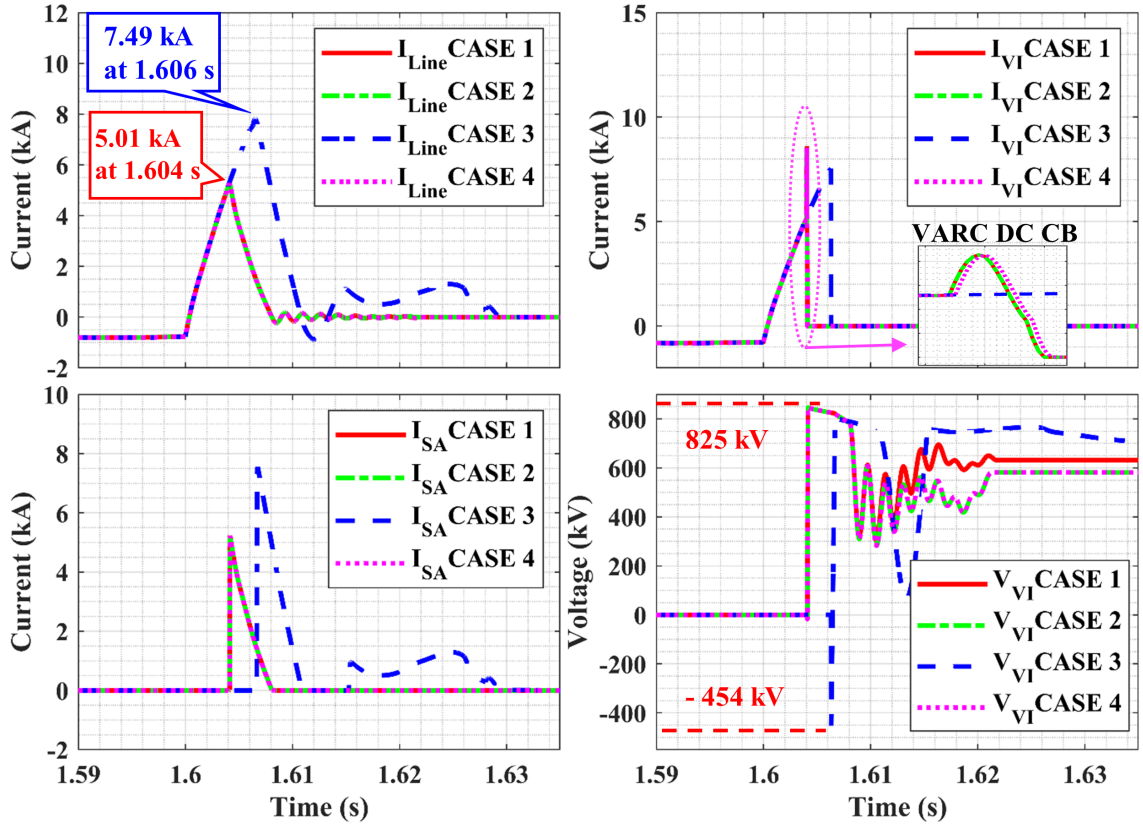


Figure 6.10: Current and voltage waveforms in CB 1a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the SA. (d) Voltage (in kV) across the VI.

the time of zero crossing and this leads to ITIV. The amplitude of the ITIV in this case is lower than the ITIV obtained in-case of an mechanical DC CB, as observed in the figure. The TIV for all the cases reaches a peak of 825 kV, which is 1.6 times the network voltage. Similar results are observed in case of a fault in cable 13, 24 and 34.

### 6.5.2. MMC's Blocking Status

Table 6.6 provides the blocking status of the MMC. In cable 12, case 1 and case 4 do not block the converter, while case 2 and case 3 do block the MMC 2 and MMC 1 respectively at a fault in the middle and near MMC 1. However, during a fault at the terminals of converter 2 on cable 12, only MMC 2 is blocked in case 2. In case of a fault in cable 13, only case 4 does not block converters, while rest cases block the converters. Furthermore, in cable 24, except case 2, the rest cases do not block the MMC, whereas, for a fault in cable 34, case 2 and case 3 block MMC 4 and MMC 3 respectively. In conclusion, Case 4 does not block any converter for various fault locations. Similarly, for fault in cable 13, case 1 block converter 3.

### 6.5.3. Energy absorption

Figure 6.12 summarises the energy absorbed in various cases at different locations during the pole to pole fault. The DC CB 2a, 3a, and 4b absorb higher energy in case 2 in comparison with other DC CBs. The higher absorption is due to the higher operating time of the mechanical DC CB in case 2. Upon including the information of the MMC blocking for various cases at different locations, we can define a range of energy absorption that will not block the MMC. The solid line (red and blue) in the figure indicates the cases which do not block the MMCs.

The MMC 1 and MMC 3 aren't blocked, if the energy absorbed by the DC CB closer to these MMCs is below 10 MJ, whereas remaining converters get blocked if the energy absorbed by the DC CB,

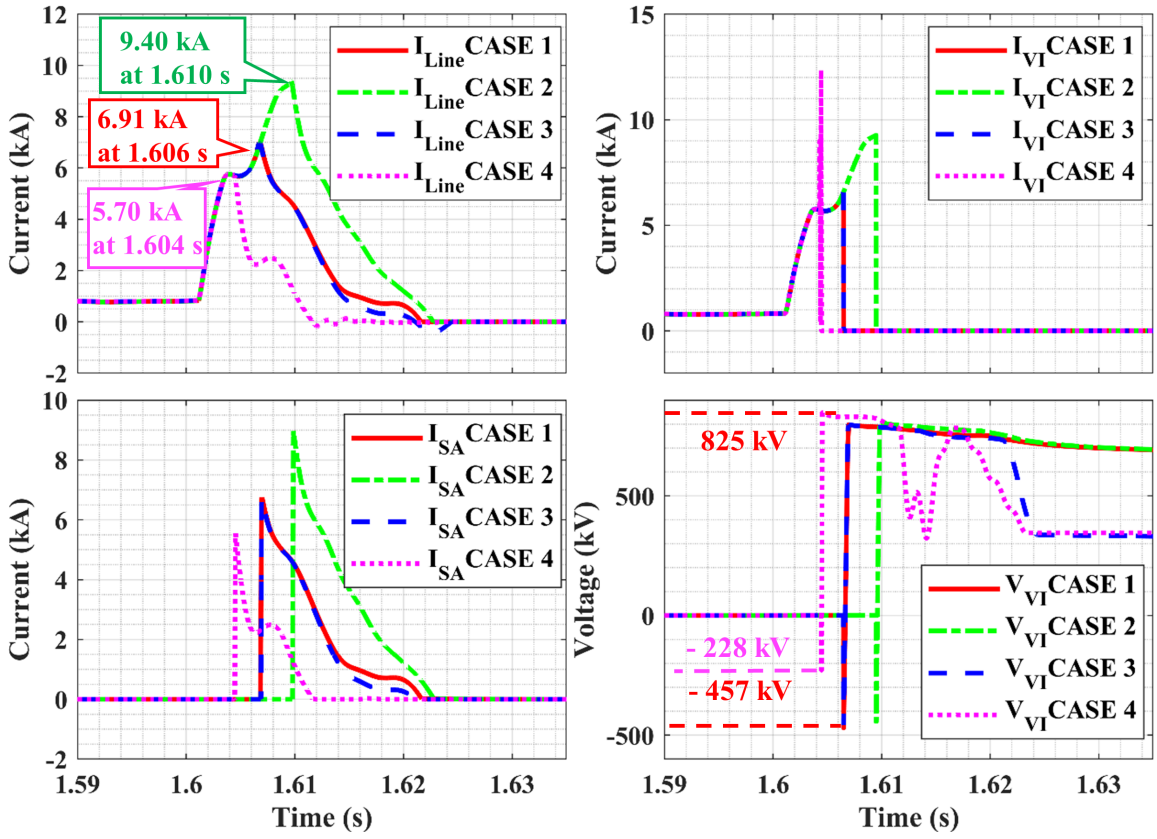


Figure 6.11: Current and voltage waveforms in CB 2a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the SA. (d) Voltage (in kV) across the VI.

Table 6.6: Blocking status of MMC for various case scenarios in 4- Terminal TenneT MTDC network

| Location | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| Cable 12 - 0 | - | MMC 2 | MMC 1 | - |
| Cable 12 - 50 | - | MMC 2 | MMC 1 | - |
| Cable 12 - 100 | - | MMC 2 | - | - |
| Cable 13 - 0 | MMC 3 | MMC 3 | MMC 1 & MMC 3 | - |
| Cable 13 - 50 | MMC 3 | MMC 3 | MMC 1 & MMC 3 | - |
| Cable 13 - 100 | MMC 3 | MMC 3 | MMC 3 | - |
| Cable 24 - 0 | - | MMC 4 | - | - |
| Cable 24 - 50 | - | MMC 4 | - | - |
| Cable 24 – 100 | - | MMC 4 | - | - |
| Cable 34 - 0 | - | MMC 4 | MMC 3 | - |
| Cable 34 - 50 | - | MMC 4 | MMC 3 | - |
| Cable 34 - 100 | - | MMC 4 | MMC 3 | - |

near to the converter is higher than 30 MJ in cable 12, 13 and 34. In cable 24, the energy absorbed, shows a different pattern in comparison with other cables. The energy absorbed in DC CB 4a in case 2 is lower than the case 1. This reduction of energy arises due to the lower fault current suppression time in case 2 as compared with that of case 1. However, even with lower energy in case 1, the higher fault current leads to the blocking of MMC 4. The selection of the DC CB not only depends upon the cable length, location of the fault and blocking status of MMC but also on the control of the MMC.

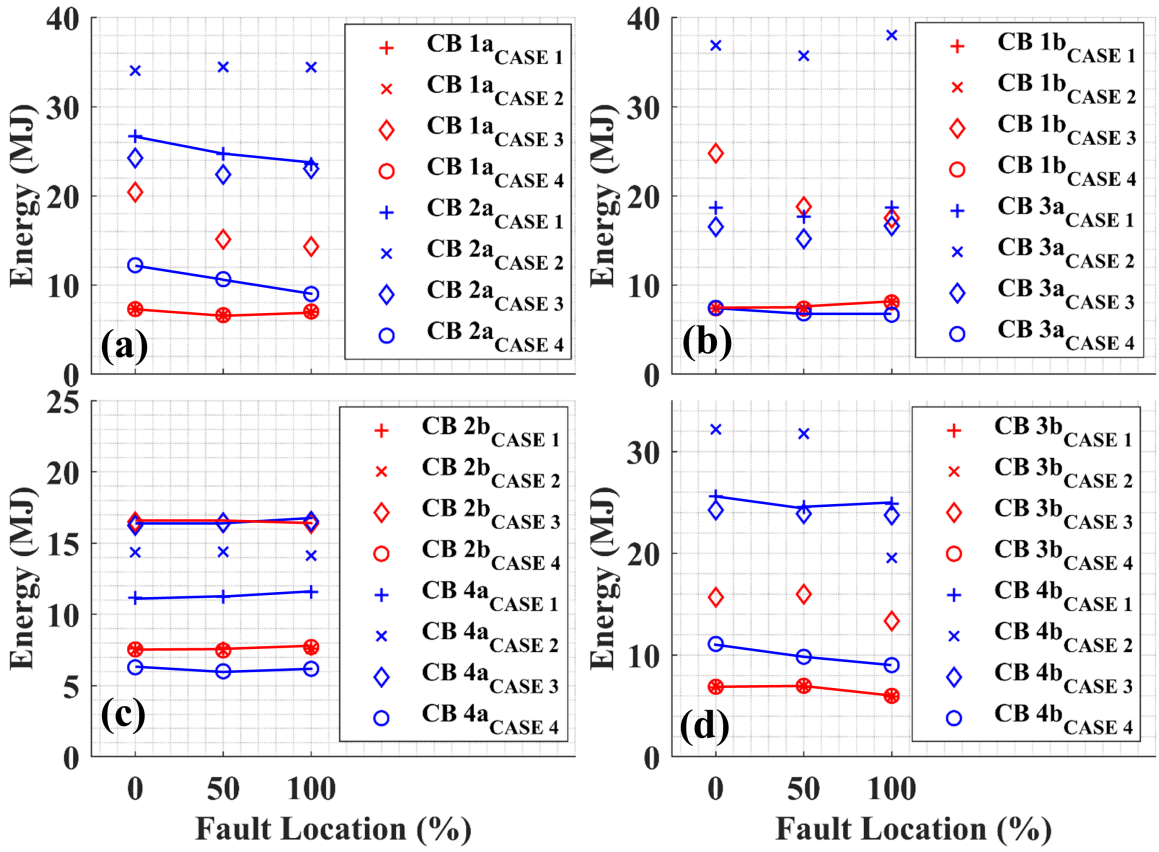


Figure 6.12: Energy absorbed in the grid by DC CBs during various case scenarios in (a) Cable 12. (b) Cable 13. (c) Cable 24. (d) Cable 34.

In HVDC network, there exist two types of controls, namely: power control and voltage control. The power controlling terminal of the HVDC network provides constant power into the network. During the fault, as power is constant, the terminal voltage is severely affected. The fault current arises from the energy storing elements of the DC network and the AC infeed power before blocking the converter. The energy is quickly drawn from the stored elements of the DC network in the first few milliseconds, after which, the fault current is mainly comprised of AC infeed current. The relation of AC infeed current in power controlled terminal is given by [6]

$$i_s(t) = \frac{P}{u_c(t)} \tag{6.1}$$

Where $P$ is AC power reference and $u_c(t)$ is the module capacitor voltage. Unlike power controlling terminal, voltage controlling terminal follows the reference voltage level with the help of the PI controller. The AC infeed current is given by [6]

$$i_s(t) = k_p \cdot (U_{DC} - u_c(t)) + k_i \int (U_{DC} - u_c(t))dt \tag{6.2}$$

Where $k_p$ and $k_i$ are the proportional and integral gain and $U_{DC}$ is the dc voltage reference. Equations (6.1) and (6.2) conclude that a terminal fault near the power controlling terminal has a lower rate of rise of fault current as compared with the voltage controlling terminal. Hence, the violation of the IGBT protection limit is much faster in voltage control. In the 4 - Terminal TenneT MTDC network, the onshore MMC controls the voltage, while the offshore MMC controls the power in the DC network. It is observed that the voltage control MMC gets block if the energy is above 10 MJ, while the power controlled MMCs, has a range of energy absorption without blocking the converter. It can be concluded that, a faster breaker should be installed at the terminal, which controls the voltage and

slower breaker near power controlling terminals. Making use of the status of MMC blocking, energy absorption, MMC control and fault current, selection of the DC CB can be made, as illustrated in figure 6.13. The selection of DC CB is explained with the following example: Considering the cable 12, fault at the terminal of MMC 1 leads to a higher fault current as compared with other locations on the same cable. If the amplitude of the fault crosses the Zone 2, then only fast breaker (VARC DC CB) should be installed at the closest terminal. For example, the amplitude of the terminal fault (pole to pole) near MMC 1 at 5 ms violates the Zone 2 limits, thus, CB 1a should operate with a lower operation time. However, a terminal fault near MMC 2 at 5 ms does not violate the zone 2 limits, hence either of the fast and slow DC CBs can be used. Thus, both case 1 and case 4, can be used for cable 12. Similarly, for cable 13, only case 4 can be utilized, since all PP faults at 5 ms violate Zone 2 limits. In contrast to cable 13, cable 24 does not violate the zone limits. Hence case 1, case 3 and case 4 can be used in cable 24.

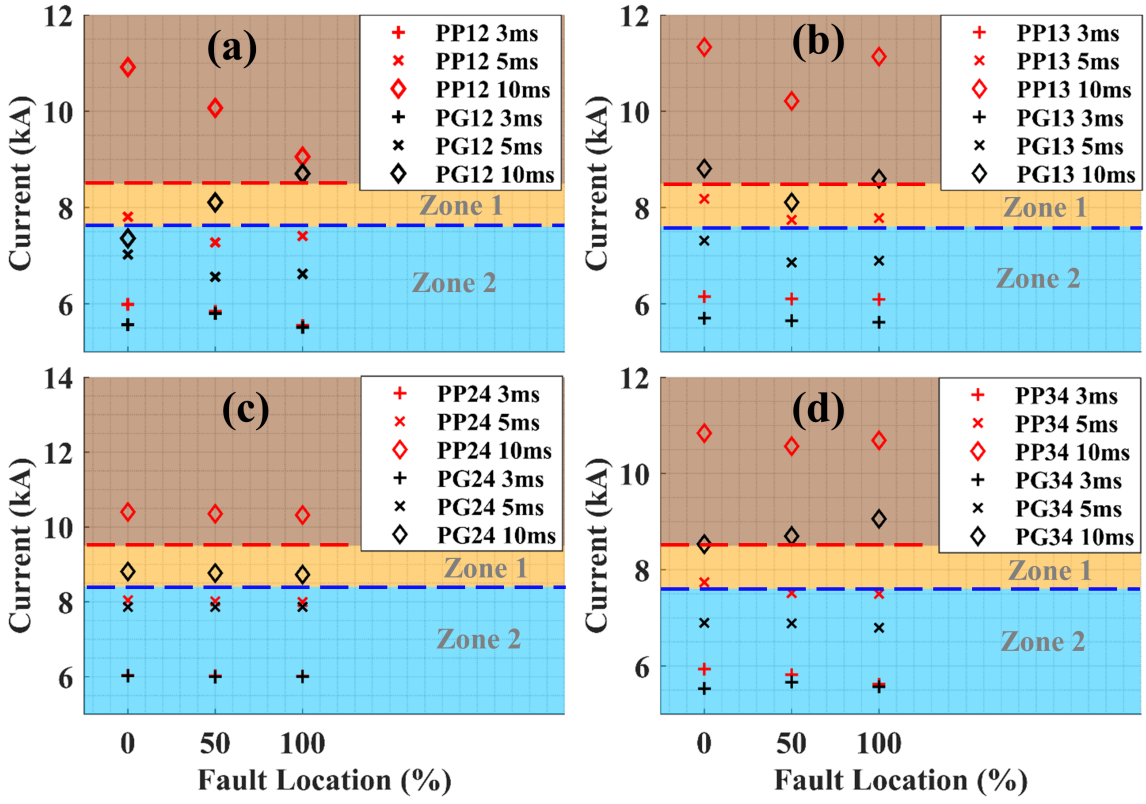


Figure 6.13: Selection of DC CB in (a) cable 12 (b) cable 13 (c) cable 24 and (d) cable 34.

## 6.6. Summary and Discussions

This chapter presents a co-ordinative performance of an active injection mechanical DC CB and a VARC DC CB for a 320 kV and a 525 kV 4 - terminal MTDC grid.

For a 320 kV 4-terminal MTDC grid, the worst-case scenario of a fault occurs for cable 12 and 13, when the fault is near the converter station. The co-ordinative performance of two types of DC CBs has been demonstrated accordingly. For case 1, the combination of a mechanical DC CB and a VARC DC CB with an operational delay of 5 ms and 3 ms respectively, can successfully clear the fault without blocking the MMC converters. For case 4, VARC DC CBs installed at remote terminals can interrupt the fault.

Similarly, For a 525 kV 4-terminal MTDC grid, a fault near the on-shore converter has the highest fault current magnitude. Co-ordinative performance between mechanical and VARC DC CB was verified on the cable 12, 24 and 34, i.e. case 1 without any blocking of MMC. However, for cable 13 only VARC DC CB was suitable as rest cases resulted in blocking of the converters. In addition,

not only the fault amplitude and the energy absorbed should be considered during the selection procedure, but also the mode of operation of MMC plays an essential role.

The co-ordinative operation of the DC CBs was very crucial as a possible failure at any DC CB may lead to the blocking of the converters. The methodology proposed in this chapter can be applied to other MTDC configurations in the future.

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# 7

# Comparison of DC CB models

*Based on the study, the selection of model is important in terms of computation time and cost. As such, this chapter discusses the performance of two different models for VARC and mechanical DC CB in MTDC network and a comparative analysis is performed in terms of speed of operation, suitability and efficiency is carried out in this chapter.*

## 7.1. Introduction

The previous studies on VARC and Mechanical DC CB have only focused on the performance of the breaker in the MTDC network using the detailed model. Despite this, no studies have been investigated which involve the simplification of detailed VARC and mechanical DC CB model for system-level studies. Depending upon the purpose of the study, the HVDC DC CB can be modelled in the Electromagnetic transient simulation (EMT) software environment with different degree of details. To identify the weak link within the DC CB, different critical components like vacuum interrupters (VIs), IGBTs, surge arrester (SA) and energy storage element have to be studied during the internal and external fault. Moreover, this study can be performed by considering the detailed model of the HVDC breaker. However, due to a larger number of switching devices with higher switching frequency, we get a larger admittance matrix. Hence, the detailed model is not recommended for the grid level study with the higher terminals as it requires larger computational time and computing resources.

In context to the above problem, this thesis proposes an average VARC DC CB model which can potentially run the simulation faster than the detailed model without compromising the accuracy in system study. Further, a similar approach can be applied to Mechanical DC CB. In order to demonstrate the effectiveness of the model, a comprehensive comparison between the detailed and average model is made and this will guide the reader to make a deliberate decision to utilise and to have credibility on DC CB models performance in MTDC network. Here, both models are implemented and simulated in PSCAD/EMTDC software environment and are compared in terms of their performance and simulation speed.

## 7.2. Detailed Equivalent model of VARC and Mechanical DC CB

Chapter 2 and 3 discuss the detailed equivalent model of VARC and Mechanical DC CB. The model consists of the three major branches, i.e. the main branch, energy absorption branch and current injection branch. In order to utilise this model for the grid application, it has to be scaled. For a 525 kV network application, the series connection of 7 modules of VARC DC CB, each with a rating of 80 kV is used, while in mechanical DC CB, series-connection of 7 VI with 80 kV rating is used.

In the detailed model of both DC CBs, the effect of the parasitic components has persevered. In this model, the current interrupting devices (VI and RCB), semiconductor switches ("$G$" and "$\bar{G}$" ) in VARC DC CB and SA are adopted from the PSCAD software library. The highly non-linear arc characteristics, which exists in the physical breaker, is not modelled in the VI model. However, the non-linear characteristics of the components have persevered. Hence, accurate voltage and current stress can be observed not only at the component level but at the system level also. Due to detailed modelling, various aspect can be studied like temperature and energy dissipation in SAs, on state power loss in VI and the switching losses. Furthermore, the modular topology of VARC enables the voltage distribution study due to the delay of the trip signal to each module. Hence the detailed model reflects the actual configuration of the models, i.e. whether it is modular or series-connected VI topology.

The main drawback of the detailed equivalent VARC and mechanical DC CB model is that solving electrical circuits with non-linear elements take a significant amount of time and data due to the re-calculation of the admittance matrix at every time step. For a complex power grid, the dimension of the admittance matrix is larger due to the higher number of nodes in the grids.

## 7.3. The average model of DC CB

Figure 7.1 (d) shows the average model for VARC DC CB. Similar to the detailed model, the average model has three major branches. During the fault neutralisation time (figure 7.1 (a)), the VI in the modules is conducting; hence it can be represented by a single switch from the PSCAD/EMTP database. The Voltage rating of this switch will be equivalent to the system voltage. At the beginning of the fault current suppression time, the line current is commuted to the current injection branch. As a result, all the oscillating capacitor of modules are connected in series, as shown in figure 7.1 b. Hence, the entire configuration is represented by a single capacitor. Furthermore, the value of this capacitance is equal to the equivalent series capacitance of the module's oscillating capacitor,

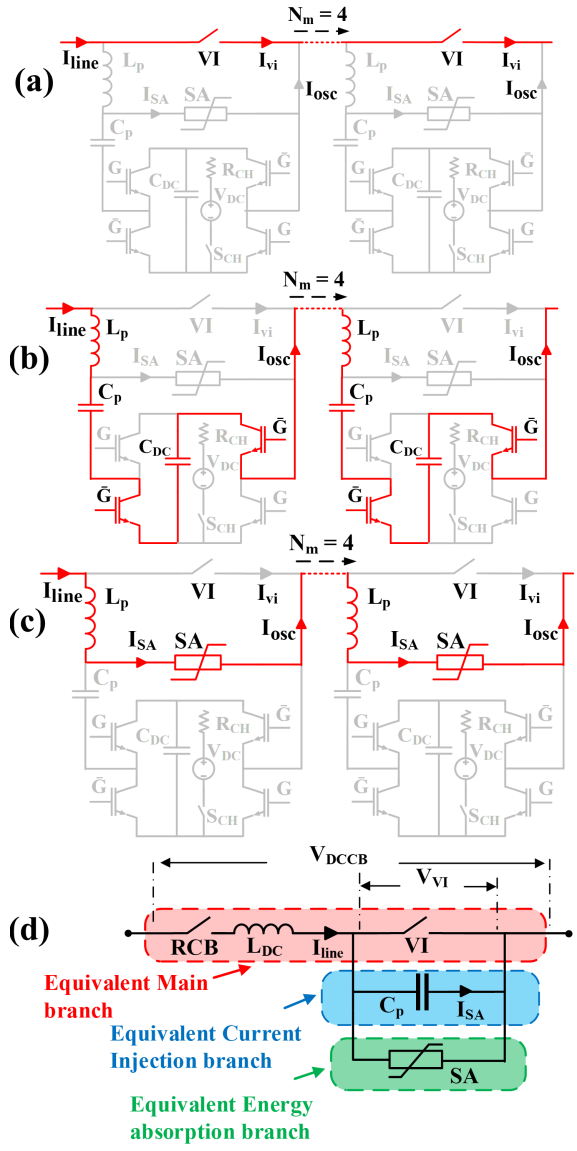


Figure 7.1: Flow of line current in VARC DC CB. (a) During fault neutralisation time, (b) During rise of TIV, (c) During fault current suppression time and (d) average model of VARC DC CB

which is given by (7.1).

$$C_{P_{eq}} = \frac{C_P}{N_m} \tag{7.1}$$

Where $C_P$ is an oscillating capacitor of a module and $N_m$ is the number of modules. Due to the presence of an equivalent oscillating capacitor, the interaction of this capacitor with the system can be analysed after the fault interruption. However, the oscillating inductance is omitted in the average model.

Upon clamping of the SA in the detailed model, the line current is commuted to energy absorption branch as presented in figure 7.1 (c). Hence, all the SAs of the modules are connected in series during this period. As a result, a single SA represents the series connected SAs and rated for the system voltage. Table 7.1, provides the data for a detailed and average model for a 320 kV network.

The VI and RCB in this model are modelled as a simple switch. This switch has two states, ON with a lower value of resistance and OFF state with a higher value of resistance. Furthermore, the switch is set to operate near current zero. Hence, this switch is accurate and reduces the

Table 7.1: Parameter of detailed and average VARC DC CB model for 320 kV system

| Parameters | Symbol | Detailed model | Average model |
|---|---|---|---|
| Oscillation inductor | $L_P$ | 95 $\mu$H | 0 $\mu$H |
| Oscillation Capacitor | $C_P$ | 2.72 $\mu$F | 0.68 $\mu$F |
| Rated / clamping voltage of Surge arrester | $V_{rated}/V_{clamp}$ | 80/120 kV | 320 / 480 kV |
| Initial Voltage across $C_P$ | $V_{iniC_P}$ | 10 kV | 0 kV |
| Number of modules | $N_m$ | 4 | 1 |

computation time as the complexity of equation is reduced.

During the modelling, line inductor ($L_{DC}$) is considered as a linear electrical component. However, the SA is modelled as a non-linear element in the EMTDC software environment. In the EMTDC software environment, the SA makes use of a Piecewise Linear Method, which reduces the amount of conductance matrix inversion per run with reasonable accuracy in outcomes [1]. Moreover, the details of the parasitic and grading components are removed in the average model.

Even though with the simplification of the current injection branch, average VARC DC CB model provides higher accuracy in terms of the energy absorption in SA and VI conduction losses. Further, the complex logic of VSC for each module is reduced.

## 7.4. Model Performance and Validation

A comparison of the two different models of the VARC DC CB can be made based on different technical performance Both models have a current interrupting functionality. The DC CBs in both models can interrupt designed fault current.

The average model shows similar technical performance in comparison with the detailed model. However, there is a small margin of error in some scenarios, for example, the nature of the injected oscillating current. In the VARC detailed model, the amplitude of injected oscillation current changes after each reversal. Whereas due to the lumped capacitor ($C_P$) in an average model, this growing oscillation is absent.

Besides, the average model loses some of the crucial component level information like VSC's voltage and current stress, voltage sharing and redundancy. Furthermore, the scaled topology information is absent in the average model. In addition, the average model can provide necessary information on the estimation of SA energy absorption, VI power loss estimation and fault interruption capability. For the purpose of verification, two transient studies are performed.

### 7.4.1. Terminal short circuit at MMC 1

In the first study, a pole to pole fault is applied at the terminal of MMC 1 in cable 12 of a 320 kV MTDC network (6.3). Initially, the system attains the steady-state condition after 0.9 s with a steady state current of 0.87 kA. At 1 s, the fault is applied. As a result, fault current rises with a rate of 2.9 kA/ms. The figure 7.2 compares the current and voltage response of the detailed and average model of VARC DC CB during Terminal short circuit on the cable 12 near MMC 1 for positive pole. Both models show an identical overlap of the Voltage across the DC CB during fault current suppression and neutralisation time. Similarly, both models have information about post fault interrupting oscillation. The cause of this oscillation is due to the interaction of system inductance and oscillating capacitor ($C_P$) of both models. The frequency of this oscillation is $f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{110\ mH \times \frac{2.72\ \mu F}{4}}} = 580\ Hz$.

Furthermore, due to higher damping components, the detailed model has a lower peak of this oscillation. In both models, the oscillating capacitor ($C_P$) determines the rate of rise of TIV. Also, both models have information about the TIV during the fault current suppression time, and the peak value is 1.5 times the rating SA.

In the detailed model, without considering the losses in the DC CB, the peak value of injected

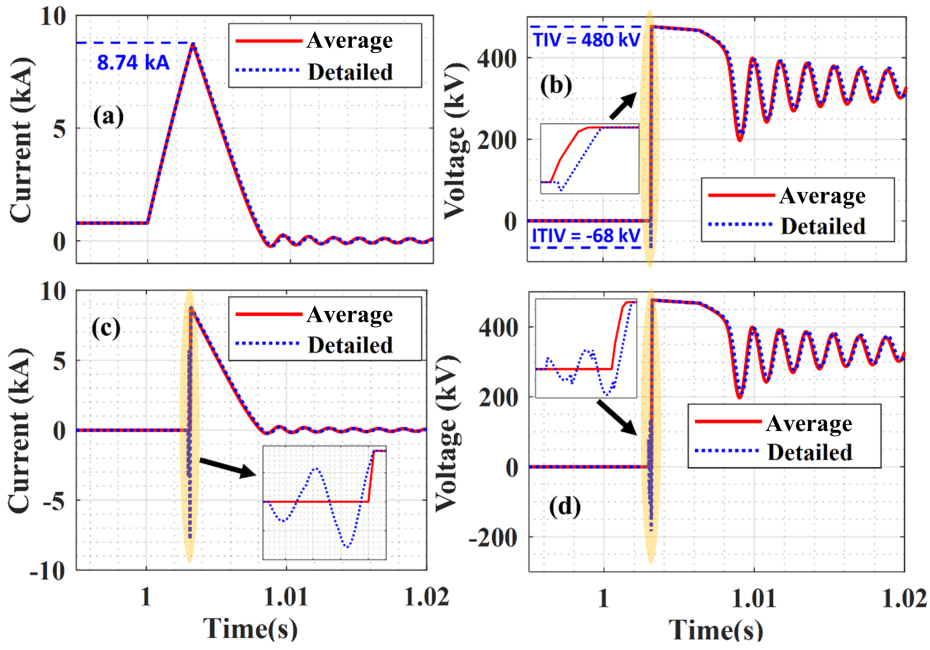


Figure 7.2: Comparison of VARC models during the Pole to pole fault on cable 12 near converter station 1.(a) CB 12 a Line Current (kA) (b) CB 12 a Voltage (kV) (c) CB 12 a injected current (kA) (d) CB 12 a SA Voltage (kV)



current is expressed as follows:

$$I_{OSC_{pk}} = \frac{(N+2) \times V_{DC}}{\sqrt{\frac{L_P}{C_P}}} \tag{7.2}$$

Where N is the number of reversals within the VSC. To reach the fault current amplitude of 8.74 kA, four reversal take place within VSC. Hence after four reversals, the prognosticated peak amplitude of injected current will be 10.15 kA. However, due to the lower fault current, the current in the VI (VI) is interrupted at the non-peak value of injected current. As a result, ITIV with the amplitude of -68 kV is developed across the VI which can be theoretically computed by

$$V_{ITIV} = N_m \times (N+1) \times V_{DC} \cos\theta \tag{7.3}$$

$$\theta = \sin^{-1}\left(\frac{I_f}{I_{OSC_{pk}}}\right) \tag{7.4}$$

Where $N_m$ is the number of VARC modules, furthermore, the theoretical value of ITIV is about 30% higher than the simulated value due to the resistive losses.

The average model of VARC does not provide information about the ITIV as observed in figure 4. Similarly, the information about the nature of the injected current is absent. However, the average model accurately follows the envelope of the detailed model with a smaller error in voltage and current, as indicated in table 7.2.

Table 7.2: Percentage of error of average model from detailed model during terminal short circuit at MMC1

| **Signals** | **% of Error** |
|---|---|
| Line Current | 1.18 |
| Voltage across DC CB | 0.12 |
| Injected Current | 1.17 |
| Voltage across Surge arresters | 0.04 |

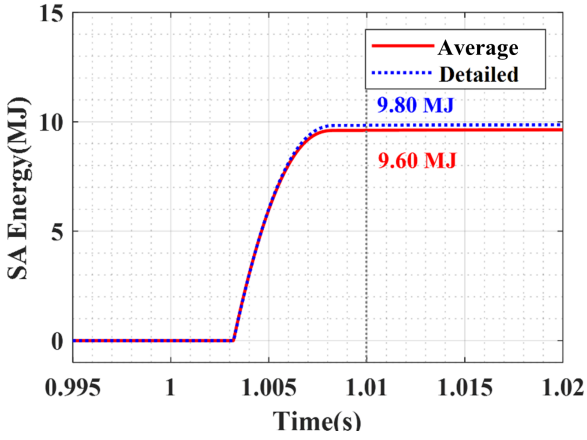


Figure 7.3: Comparison of the energy absorbed in CB 1a during terminal short circuit for average and detailed VARC model

There is an energy difference of 0.2 MJ between the average and detailed model. This energy difference occurs due to the extra time taken by the injected current to reach the peak current value of the fault current, as shown in figure 7.3 (a). The following steps can theoretically calculate this extra time: the injected current is given by

$$I_{OSC} = I_{OSC_{pk}} \times \sin(\theta) \tag{7.5}$$

At the end of fault neutralisation time, $I_{OSC} = I_f$. Thus for given data, $\theta = 60°$ and extra time, $t = \frac{0.1ms \times 60°}{360°} = 1.5 \times 10^{-5} s$.

The energy difference can be calculated based on the amount of current flowing through SA, the voltage across SA during energy absorption and the period for which this current is flown into SA. Considering the rate of rise of fault current to be 2.9 kA/ms and assuming the constant value of SA voltage and current during fault current suppression time, estimated energy absorbed by the average model is $E_{SA_{avg}} = 4 \times 8.7\ kA \times 120\ kV \times 5\ ms = 20.8\ MJ$. Similarly, in detailed model, energy absorbed by SA is $E_{SA_{det}} = 4 \times (8.7\ kA + 2.9\ kA/ms \times 1.5 \times 10^{-5}) \times 120\ kV \times (5\ ms + 1.5 \times 10^{-5}) = 21.0\ MJ$. Hence, the net difference for the SA energy absorbed, between both the models is 0.2 MJ.

The figure 7.4 (a) illustrates the MMC 1 positive pole bus voltage during the terminal short circuit for both models. As can be seen from figure 7.4, during the terminal fault, initially, MMC 1's voltage drops steeply followed by a gradual drop in voltage. The value of line inductance determines the rate of this drop. Further, with the operation of DC CB at 1.003 s, a spike is observed only in the detailed model, which represents the ITIV. Due to the TIV, the bus voltage starts to recover. However, after the current zero in VIs, the bus voltage is superimposed by the oscillation of 580 Hz. This oscillation represents the interaction of $C_P$ and system inductance, as explained in the previous paragraphs. Moreover, this oscillation is eliminated with the operation of the residual circuit breaker (RCB). During the entire fault scenario, the MMC remains unblocked, as the protection criteria are not violated. Furthermore, the MMC 1 positive pole current, reaches 4.4 kA at 1.003 s, after which it drops with a rate determined by the clamping voltage. However, the MMC remains in operation after a current interruption as only faulty line is isolated. The cable voltage of positive pole seen from both MMCs i.e 1 and 2, yields similar results for both models. Moreover, the cable voltage seen from MMC 2 has oscillations (figure 7.4 due to the reflection of the travelling wave during the transient event.

Similar to the VARC's DC CB model, the voltage and current plots in the average model of mechanical DC CB overlap over the detailed model during and after fault current suppression time with a small margin of error, as shown in figure 7.5 (a) and (b). However, during the start of the fault current suppression time, the detailed model has information about ITIV, which is lost in the average model. Absence of ITIV is due to the zero initial voltage across the oscillating capacitor.

As a result of ITIV, the time taken to reach the clamp voltage is more in case of the detailed model as compared to the average model, the same can be observed in figure 7.5 (b). This delayed

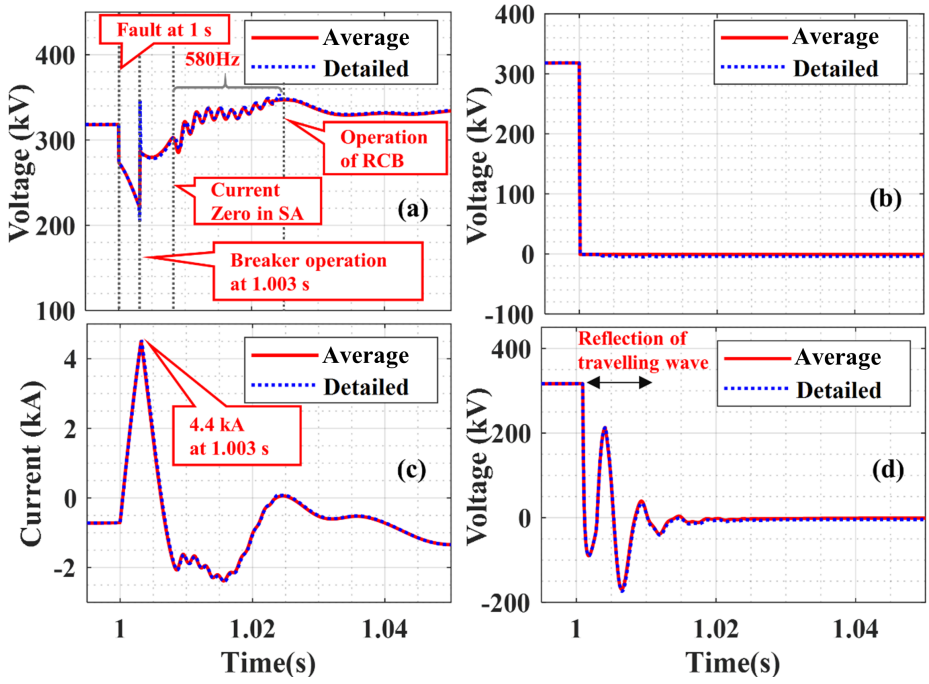


Figure 7.4: Average and detailed Model Comparison during the Pole to pole fault on cable 12 near converter station 1 in Positive pole (a) bus voltage (kV) (b) Cable voltage observed from MMC 1 (kV) (c) MMC 1 current (kA) and (d) able voltage observed from MMC 2 (kV)



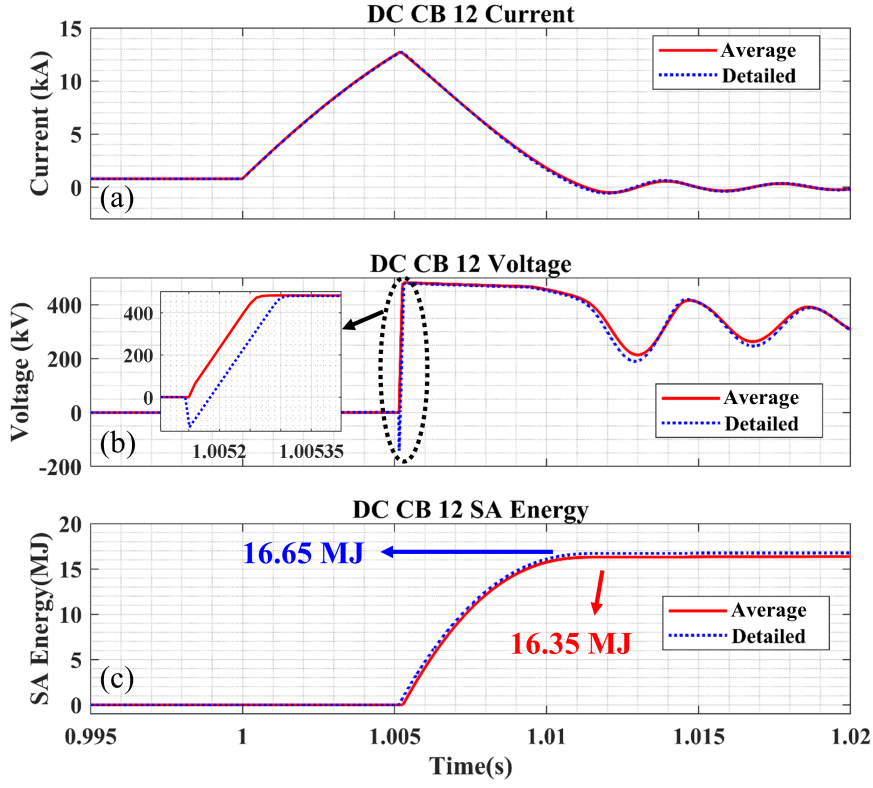


Figure 7.5: Comparison of Mechanical DC CB models during the Pole to pole fault on cable 12 near converter station 1.(a) CB 12 a current (b) CB 12 a voltage (c) CB 12 a SA energy

time leads to an increase in fault current level by 30 A. Furthermore, this change of fault current causes SA to absorb more energy. The energy absorbed by a detailed model is 16.65 MJ, which is 2% higher than the average model.

### 7.4.2. Steady-state current interruption

In the following study, a switching action is carried out in cable 12. The MTDC network is again operating at the steady-state condition with line current of 0.87 kA in cable 12. Then, at 1 s, a switching action is carried out in cable 12 by sending a trip signal to the CB 1a and CB 2a. At the lower current interruption, only the main and current injection branch interact with the system. Hence, line current in both the models have oscillation with the frequency of 580 Hz after the fault neutralisation time. This oscillation arises from the interaction of the oscillating capacitor and system inductor, as explained in the previous section. Moreover, the energy absorption branch is not engaged as the voltage across the SA does not reach the clamping voltage of 480 kV.

The VARC DC CB is primarily designed to interrupt the rated fault current. Thus with the first reversal of VSC voltage, the peak value of injected current given by (7.2) is 3.3 kA (figure 7.6 c). Moreover, due to the higher value of the $I_{OSC_{pk}}$, corresponding ITIV is higher. The value of ITIV can be estimated using (7.3) and (7.4) with N = 1, which results in the theoretical value of -155 kV. The resistive losses cause about 3% lower value of ITIV in the simulated result than the theoretical value. However, due to the equivalent representation of the current injection branch in the average model, the details about $I_{OSC_{pk}}$ and ITIV are missing. Similarly, the voltage stress information about the SA is omitted. Throughout the entire transient study, the result anticipated by the average model remains in great harmony concerning the reference solution by the detailed model.

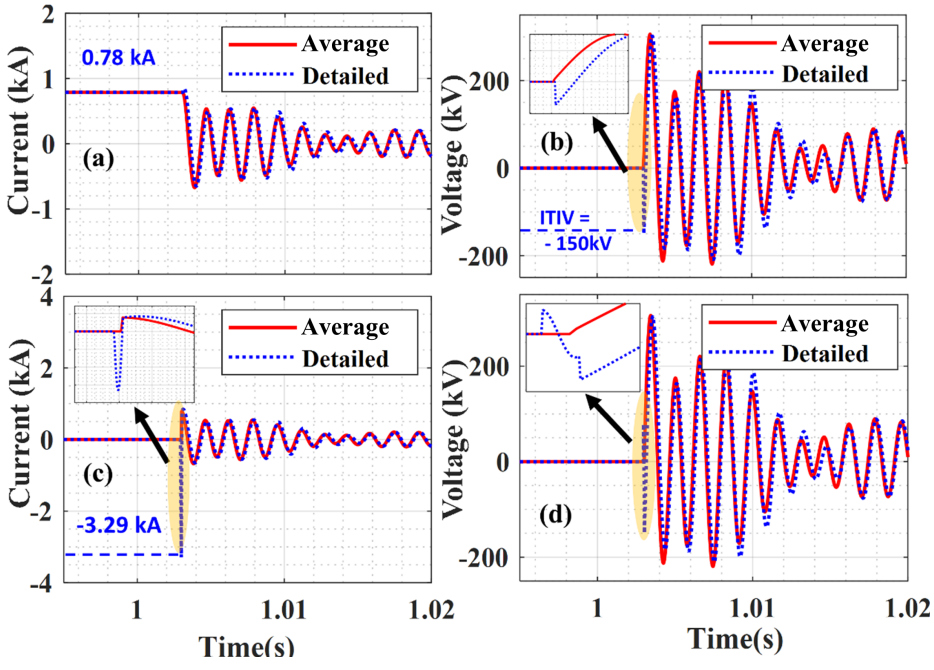


Figure 7.6: Comparison of VARC DC CB models during Steady-state current interruption in cable 12. (a) CB 12 a Line Current (kA) (b) CB 12 a Voltage (kV) (c) CB 12 a injected current (kA) (d) CB 12 a SA Voltage

For low current interruptions, the current and voltage signals in average model show identical curve profile with a slight error as shown in table 7.3

## 7.5. Computational time

The 4-terminal HVDC system is simulated for 1.2 s using the detailed and average model at two different time steps. The simulations were performed on the same PC equipped with 8 GB of RAM using PSCAD V4.6.

Table 7.3: Percentage of error of average model from detailed model during Steady-state current interruption

| Signals | % of Error |
|---|---|
| Line Current | 3.55 |
| Voltage across DC CB | 0.94 |
| Injected Current | 3.51 |
| Voltage across Surge arresters | 0.68 |

With the average modelling of MMCs of 4 - terminal HVDC system, the simulation can run at higher time steps maintain acceptable accuracy. This HVDC system can run at a time step of 2 - 10 $\mu$s, without losing its dynamic response. For detailed VARC model, the time step of at most 2 $\mu$s is required to, also maintaining the accuracy. Hence the detailed model creates a bottleneck in the system. As a result, the overall time step is reduced for the accurate transient and steady-state response.

Due to the reduction in the admittance matrix, the average model of VARC can be simulated at higher time steps without changing the transient response. The preferred time step for the average model is at least 10 $\mu$s. The comparison of simulation speed for two models is summarized in table 7.4. As can be seen from table 7.4, the average model reports lower simulation time with a difference of 19 minutes from the detailed model.

Table 7.4: Comparison of Computation time of different models for time interval from t = 0 s to t = 1.2 s

| Model | Time step | Simulation time |
|---|---|---|
| Detailed model | 2 $\mu s$ | 22 min |
| Average model | 10 $\mu s$ | 3 min |



## 7.6. Summary and Discussions

In summary, this chapter presented the comparative study of two different models for both DC CB technologies, namely, detailed equivalent and average model. The current and voltage waveforms for both models in a 320 kV MTDC network overlap with each other, thereby maintaining higher accuracy. However, there was a slight variation in energy absorbed due to the time taken by the oscillation current to reach the peak current value of the fault current. Similarly, the details of ITIV were absent in case of the average model. The significance of the average model was that, it has reduced the simulation time by 86% in comparison with the detailed model, thereby enabling the average model for the system-level simulations.

## References

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# 8

# Conclusion

The High Voltage Direct Current (HVDC) breaker is the missing link in the development of Multi-Terminal Direct Current (MTDC) network. In recent years, several HVDC breakers have been proposed and demonstrated in the testing environment. Due to the variation in operating principle, speed of operation and interrupting capability, an investigation on the technical performance of these DC CBs in MTDC network is essential. The main goal of this thesis was to investigate the technical performance of two popular DC CBs namely, the VARC and Mechanical DC CB in MTDC network. In addition, a methodology for the selection of different DC CBs in MTDC networks and an average model of DC CB for grid-level studies was presented in this project.

These objectives were achieved by modelling the VARC and Mechanical DC CB in PSCAD / EMTDC software environment. The modelled DC CBs were able to provide critical information about the fast transient due to the presence of grading and parasitic components in the model. Also, this model can be used for the investigation of re-strike and re-ignition in DC CB. Furthermore, DC CB voltage rating was up-scaled using modular topology for VARC and series-connected vacuum interrupter topology for mechanical DC CB. Also, for both DC CBs, the rating of the vacuum interrupter (VI) was chosen to be 80 kV and dielectric strength of VI was modelled using cold break down approach.

The VARC and Mechanical DC CB's performance under the re-strike was carried on a test system, which represented a critical case of MTDC system i.e. terminal short circuit. This re-strike in breaker was performed for two time instants, i.e during the rise of TIV and during the fault current suppression time. This investigation suggested that, in VARC DC CB with modular topology, if more than two modules re-strike without attaining their interrupting capability after the first re-strike then the entire breaker fails to interrupt the fault. However, in case of Mechanical DC CB with series-connected VI topology, even if one of the VI's re-strikes without attaining its interrupting capability after the first re-strike then the entire breaker fails to interrupt the fault. In VARC, the unavailability of the module after first re-strike leads to higher energy absorption, which is 3.6 times the reference case. Further, it was also observed that even with the sufficient interrupting capability of VI after first re-strike, the module did not engage in the fault interruption due to the insufficient energy in the VSC. In mechanical DC CB, the restoration of interrupting capability of VI after the first re-strike, causes a second re-strike due to the violation of the dielectric strength of the VI. In general, the modular topology of DC CB provides extra N-2 reliability in comparison with the series-connected VI topology. Also, the presence of resistance has a significant impact on the injected current in both the DC CB technologies.

The system voltage, fault neutralisation time, characteristics of SA, steady-state current and line inductor have a significant effect on the performance of both DC CB technologies. The failure scenarios show a greater impact on the energy absorption, while the variation of I-V characteristics of SA shows the least effect on the energy absorption. However, by neglecting the failure scenarios, the operation delay in VARC DC CB caused higher energy absorption while, variation in the line inductance produced large energy in mechanical DC CB. In addition, the line inductance produces energy which is approximately 40 % of the total energy absorbed.

The co-ordinative performance of the mechanical DC CB and VARC DC CB for a 320 kV 4-terminal MTDC network and a 525 kV 4-terminal TenneT MTDC network was performed. The worst-case scenario of a fault occurs for cable 12 and 13, when the fault was near the converter station. The co-ordinative performance of two types of DC CBs are demonstrated accordingly. In case 1, the combination of a mechanical DC CB and a VARC DC CB with an operational delay of 5 ms and 3 ms respectively can successfully clear the fault without blocking the MMC converters. Similarly, in case 4, VARC DC CBs installed at remote terminals can interrupt the fault without blocking the MMC converters. However, case 2 and 3 are able to interrupt the fault current only by blocking of the converters.

The amount of energy absorption depends on the operational times and the type of DC CB. Thus the energy absorber should be designed accordingly. The co-ordinative operation of the DC CBs is very important as a possible failure at any DC CB may lead to the blocking of the converters. The methodology proposed in this thesis can be applied to other MTDC configurations in future.

Finally, this thesis presented a comparative study of two different model representations of VARC and mechanical DC CB technology, namely, detailed and average model in the PSCAD software environment. The performance of the proposed average model was examined graphically and theoretically for the low and high current interruption. The results contained in this thesis have illustrated that the average model provides a good level of accuracy during the transient condition. The significance of the average model was that it had reduced the simulation time by 86% than the detailed model without losing accuracy, thereby enabling the average model for the system-level simulations. Proving, the average model being both light and computationally efficient.

It was interesting to note that, the percentage of error during a terminal short circuit case was lower than that obtained during a low current interruption case. Furthermore, the information regarding the components that make up the module was simplified. Similarly, the details of the initial transient interruption voltage and scaling information were condensed. The developed average model and results will be useful for the researchers and the practice engineers in the areas of power system which deal with HVDC transients and system studies.

# A

# Appendix A

*The work related to Co-ordination performance of different HVDC circuit breaker is accepted by* ***IEEE PES GM 2020*** *with the title of* ***"Coordinative performance of HVDC circuit breakers in MTDC grids"***

A

# Coordinative performance of HVDC circuit breakers in MTDC grids

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***Abstract*—The objective of this paper is to investigate the coordinative performance of different types of high voltage DC (HVDC) circuit breakers (CBs) in multi-terminal DC (MTDC) grids. Several different HVDC CB technologies are emerging as a solution for the protection of offshore MTDC grids. There is a need for coordinative operation between different types of DC CBs in the same network. In this paper, two typical types of DC CBs are modelled in detail and implemented in a 4-terminal MTDC grid in PSCAD environment, by considering operation time, interruption capability and interruption characteristics. Since the requirement of the DC CBs depends on the magnitude of the interrupted current where they are implemented, the fault scenarios in all terminals are studied and the worst scenarios are selected to demonstrate the coordinative performance of different DC CBs. Four cases are defined and demonstrated by two different types of CBs at each terminal of the cable. DC CBs perform differently with the change of the operating time and the locations where they are implemented. The performances and energy absorption are compared and analyzed. The obtained results can be used as DC CB's selection optimization methodology for future MTDC grids.**

***Index Terms*—HVDC circuit breaker, DC grid protection, offshore windfarm, circuit breaker performance**

## I. Introduction

The demands to utilize renewable energy significantly promote the integration of energy transmission systems [1]. MTDC grids provide a feasible solution to utilize the offshore wind farm resources because of the benefits like more operating flexibility and increase in reliability [2]. However, the development of meshed offshore MTDC grids is hindered by a few technical barriers. One of the main barriers is the lack of reliable, fast, low loss and cost-effective HVDC CBs, which can isolate the fault segments of the HVDC grid and keep the other components operating continuously [3].

Extensive studies have been done on the development of HVDC CBs, and several DC CB topologies have been proposed and realized to deal with the protection matters in MTDC grids [4]–[7]. Based on different operating principles, these HVDC CBs can be divide in two categories: hybrid circuit breakers and mechanical circuit breakers. In the hybrid circuit breaker, the main branch comprises a string of series-connected semiconductor devices having turn-off capability (e.g. IGBTs), which eliminates the line current within 3-5 ms [8]. Meanwhile, the series-connected semiconductor devices need to withstand the transient interruption voltage (TIV), which results in relatively high costs. Mechanical circuit breakers, on the other hand, utilize mechanical interrupters to clear the fault current at current zero-crossing. However, the long operation delay of traditional spring-based driving mechanisms cannot meet the fast protection requirements of MTDC grids. The development of ultra-fast actuators based on Tomson's coils makes it possible for mechanical CBs to interrupt the current within 5-8 ms [9]. The different characteristics of hybrid CBs and mechanical CBs are challenging to study the coordinative performance when they are implemented in the same MTDC grid and operate at the same time.

Currently, three MTDC grids are commissioned in China, namely, 160 kV 4 terminal MTDC grid at Nan'ao with active injection mechanical DC CBs [10], 200 kV 5 terminal MTDC grid at Zhoushan with hybrid DC CBs [11] and 500 kV 4 terminal MTDC grid at Zhangbei with different types of DC CBs [12]. The technical performance of one type of HVDC CBs in MTDC grids have been well studied. However, currently no coordinative performance of two different types of HVDC CBs implemented in the same MTDC have been reported in the literature.

This paper investigates the coordinative performance by implementing two types of DC CBs in a four-terminal MTDC grid. The two DC interruption technologies are active injection mechanical DC CB [13], and VSC assisted resonant current (VARC) DC CB [14], respectively. It needs to point out that these two types of DC CBs implemented in the MTDC are only used to represent the mechanical DC CB and hybrid DC CB, and the comparison of interruption characteristics of these two CB topologies is not the objective of this paper. The maximum fault current in each terminal of the MTDC depends on the fault type, fault impedance, fault duration and the amount of supplied power. Therefore, the requirement of DC CB interruption capability at each terminal is also different. Some terminals can endure the fault for a longer period without blocking the Multilevel Modular Converters (MMC), whilst at some other terminals the fault should be promptly cleared in order to keep the MMC working continuously. This paper proposes a solution to optimize the selection of DC CBs in MTDC so that the coordinative operations of different types of DC CB works without blocking MMC.

## II. Test 4-terminal MTDC grid description

Fig. 1 shows the four-terminal DC network consisting of two onshore converter stations (MMC 1 and MMC 2) and two offshore converter stations (MMC 3 and MMC 4). In this network, MMC 1, 2 and 4 form a smallest mesh and MMC 3 forms a radial connection.

Onshore AC grid operates at the voltage level of 400kV, and the offshore wind operates at 155 kV. The DC link operating voltage is +/- 320kV. The system configuration is symmetrical monopole with the cable connections. VSC technology is adopted for the converter with a half-bridge VSC type. Distance between MMC 1 and 2 is 175 km. Moreover, the distance between MMC 1 and 4 is about 300 km. Two onshore converters i.e. MMC 1 and 3 are separated with a distance of 350 km. The distance between MMC 2 and

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4 is smallest i.e. 100 km. DC CBs are placed at each end of the line. The nomenclature of the line is given based on the starting and termination end, for example, Cable 12 indicates a cable that begins from the bus at MMC 1 and ends up at the bus at MMC 2.

The data of the four-terminal MTDC system is shown in Table 1, and it is modelled in PSCAD environment. The fault types, the fault location, the fault impedance, and the fault duration are all adjustable. The MMC converters will be blocked when the voltage is less than 0.8 p.u and arm current exceeds 1.6 p.u.

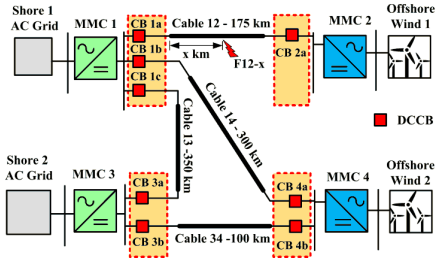


Fig. 1 Test 4 - terminal MTDC system

Table 1 Data of MMCs in 4 - terminal MTDC system

| Parameter | Converters | | | |
|---|---|---|---|---|
| | MMCs 1 | MMC 2 | MMC 3 | MMC 4 |
| **Active power** | 500 MW | 500 MW | 500 MW | 500 MW |
| **Control mode** | PVdc | PQ | PVdc | PQ |
| **Reactive power** | 100 MVAR | 100 MVAR | 100 MVAR | 100 MVAR |
| **DC link Voltage** | ±320 kV | | | |
| **Rated power** | 1256 MW | | | |
| **Number of Submodules per arm** | 400 | | | |
| **Arm capacitance $C_{arm}$** | 22 µF | | | |
| **Arm indcutance $L_{arm}$** | 42 mH | | | |
| **Arm resistance $R_{arm}$** | 0.544 Ω | | | |
| **AC converter voltage** | 400kV | | | |
| **Transformer leakage reactance** | 0.18 p.u | | | |
| **AC grids and windfarms** | | | | |
| **AC grids voltage** | 400 kV | | | |

## III. Considered Types of DC CB

### A. *Topologies of typical DC CBs*

Fig. 2 illustrates the structure of the mechanical DC CB with current injection. The model of this DC CB is described in detail in [1], and the DC CB prototype has been tested in [15].

Fig. 3 shows the structure of the VARC DC, which is proposed in [15]. The detailed model has been verified by the experimental results performed at KEMA laboratories [15].

### B. *Operating principle and timing sequence*

Fig. 4 shows the current and the voltage waveforms of the VARC DC CB and the mechanical DC CB during the interruption where $I_{line}$ is the current through the DC CB, $I_{vi}$ is the current through the vacuum interrupter (VI), $I_{sa}$ is the current through the energy absorption branch, and $V_{vi}$ is the voltage across the VI. $L_{DC}$ is chosen to limit the rising rate of the fault current with the value of 100 mH based on [14], the same $L_{DC}$ value is applied in both types of DC CBs. The detailed operation sequence for both circuit breaker topologies is explained as follows:

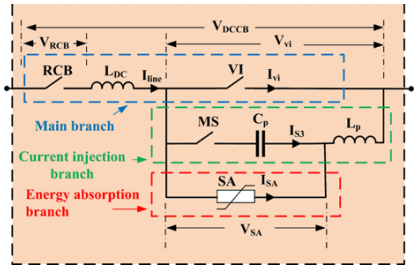


Fig. 2 Configuration of Mechanical Circuit breaker

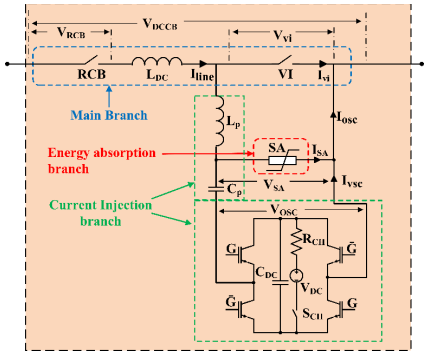


Fig. 3 Configuration of VARC Circuit breaker

$t_0$ - $t_1$: Before the operation of the DC CB, the VSC energy storage capacitor ($C_{DC}$) is pre-charged by the charging circuit in VARC. For the mechanical DC CB, capacitor ($C_P$) in the oscillating circuit is charged to the system voltage level by the charging circuit.

$t_1$ – $t_2$: A fault occurs at instant $t_1$. As a result, the line current begins to rise, and the rate-of-rise of the line current is limited by the fault current limiting reactor ($L_{DC}$). At instant $t_2$, a trip signal is sent to both DC CBs at the ends of the faulty cable.

$t_2$ – $t_{2a}$: The VARC DC CB receives the trip signal at $t_2$, and the ultra-fast actuator starts to drive the separation of contacts. The contacts in the VI reach a sufficient gap distance to withstand the TIV at $t_3$.

$t_{2a}$ – $t_3$: Shortly before the VI reaches sufficient contact separation at $t_{2a}$, the VSC is activated. The oscillating current is generated, and its amplitude gradually increases every half cycle until a zero-crossing is created in the arc current in VARC DC CB. The special characteristic of VI make it possible to clear the fault current at zero-crossing.

$t_3$ – $t_4$: The VI stops conducting at $t_3$ in both DC CBs. As the VI is connected in parallel to the oscillation branch, the initial transient interruption voltage (ITIV) across VI equals the remaining voltage of the current injection branch capacitor. At the same time, the line current is commutated to the current injection branch. During $t_3$ – $t_4$, the system keeps

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charging the current injection branch capacitor, until its voltage reaches the clamping voltage of SA at $t_4$.

$t_4 – t_5$: The SA begins to conduct at $t_5$, and the line current is commutated into the energy absorption branch. The SA current then decreases until it drops to zero at $t_6$.

$t_5 – t_6$: After the fault current interruption, some leakage current may exist in the system, as well as a low-frequency interaction between the capacitor in the circuit breaker and the inductance connected in series with the breaker. The residual circuit breaker is opened at $t_7$ to clear the leakage current and separate the breaker main circuit from the grid.

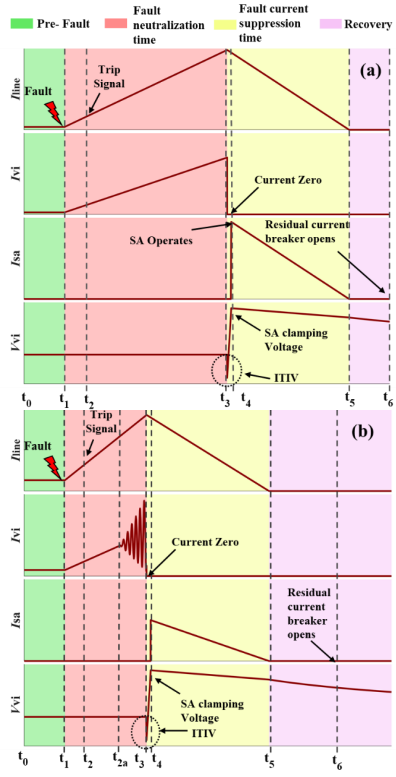


Fig. 4 Voltage and current waveforms of the (a) Mechanical DC CB (b) VARC DC CB.

## IV. Fault Case

In order to analysis the coordinative performance of the DC CB, the DC fault is analysed. The analysis of the DC fault cases is based on the type of fault, location of the fault and fault neutralization time. Fault neutralization time referred to as the operation delay in further text. The fault location is considered in terms of percentage of the cable length. Fig. 5 illustrates the fault case scenarios performed in the test topology. The type of the fault is denoted as PP and PG representing pole to pole fault and pole to ground fault respectively. Due to similar results produced, pole to pole to ground fault is not considered. The terminology used in the plot is, for example, PP12 3ms indicating pole to pole fault on cable12 where 1 is the starting and 2 is the ending node of cable with 3 ms operation delay.

When analysing the fault case scenarios, it can be seen that the faulty cable 12 has a larger fault current amplitude especially a fault location near bus 1; this is due to the power which is fed from MMC 3 and MMC 4 at bus 1. Similarly, the fault current amplitude is considerably high in cable 13 and 14. As it is shown in Table 2, the worst-case scenarios are always cable 12 and 13. Hence, a fault in cable 12 and 13 is analysed for the selection of breaker.

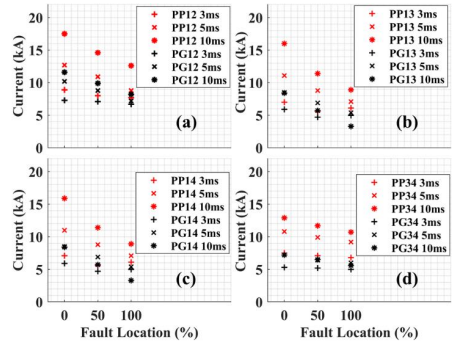


Fig. 5 Results of the possible pole to pole and pole to ground faults with different operation time in test topology; (a) fault in cable 12 (b) fault in cable 13 (c) fault in cable 14 and (d) fault in cable 34

Table 2 Maximum fault current in a cable (worst scenarios in red)

| Location | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| Cable 12 | 13.11 kA | 16.72 kA | 13.11 kA | 8.69 kA |
| Cable 13 | 11.38 kA | 15.07 kA | 11.38 kA | 7.3 kA |
| Cable 14 | 11.18 kA | 14.8 kA | 11.18 kA | 7 kA |
| Cable 34 | 10.7 kA | 12.1 kA | 10.7 kA | 7.5 kA |

## V. Results and Analysis

Based on the fault case scenarios in Section IV, 4 cases are carried out on the worst fault cable 12 and cable 13, with two typical DC CBs at each end of the faulty cable. The following case studies are conducted on the Multi-terminal terminal network. In the cases below, i and j represent the start and endpoint of cable.

- ***Case 1***: Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC i and VARC DC CB within 3 ms operational delay is introduced at the bus of MMC j.
- ***Case 2***: Mechanical DC CB with 8 ms operational delay is introduced at the bus of MMC i and VARC DC CB with 3 ms operation delay is introduced at the bus of MMC j.
- ***Case 3***: Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC i and Mechanical DC CB with 5 ms operational delay is introduced at the bus of MMC j.
- ***Case 4***: VARC DC CB with 3 ms operational delay is introduced at the bus of MMC i and VARC DC CB with 3 ms operation delay is introduced at the bus of MMC j.

### A. Interruption performance

Fig. 6 shows the current and the voltage waveforms in CB 1a for the pole to pole fault on cable 12 near MMC 1. The $I_{line}$

in case 2 has the most considerable magnitude of the current due to slower breaking near MMC 1. The effect of the travelling wave is not as significant as the fault located near CB 1a. Hence, the rise of the fault current is linear. During the interruption, in case 2, as the capacitor charged with opposite polarity causes a rise of the current up to 34 kA in VI. However, in the case of VARC CB this rise reaches up to 18kA with a high frequency growing oscillation in VI. During the fault current suppression, the time is determined based on the interrupted current. Hence, VARC has the least fault current suppression time as compared to a mechanical circuit breaker with an operational delay of 8ms. The voltage across the VI after, during the fault current suppression time remains the same for all the cases. Moreover, the amplitude of ITIV depends on the magnitude of the current in VI. For the mechanical CB, the higher current is interrupted, the lower is the ITIV [1]. There is a significant oscillation in the $V_{vi}$ for all cases except for case 2 after the fault current zero.

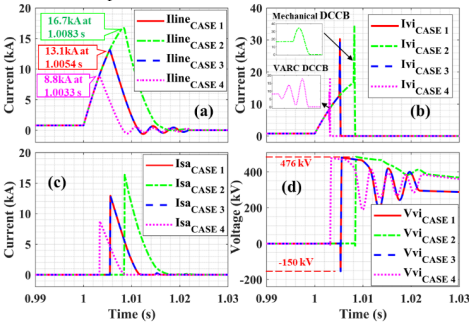


Fig. 6 Current and voltage waveforms in CB 1a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the surge arrester (SA). (d) Voltage (in kV) across the VI.

The fault located near MMC 1 has an effect on the current and the voltage waveforms in CB 2a as depicted in Fig. 7, For $I_{line}$, the effect of travelling waves is visible and it changes the fault current rise rate non-linearity. For case 3, as the presence of the mechanical circuit breaker with an operational delay of 5ms has peak amplitude of 6.9 kA at 1.0064 s. It is observed that during the fault current suppression time for case 1,2 and 4, the drop of current is non-linear, and this is due to the travelling wave phenomena. However, the effect is not seen in case 3. Significantly large ITIV is observed for case 3 with an amplitude of -260 kV.

For a fault that occurs in cable 13 near the MMC 1, identical waveforms are observed primarily in CB 1b. However, due to the same charging of the DC capacitor for the mechanical DC breaker, there is no overshoot as it can be seen in CB 1a for current $I_{vi}$.

Furthermore, significant changes can be seen in CB 3a as depicted in Fig. 8. For case 2, the fault current rises to 8.4 kA due to the presence of a mechanical circuit breaker with an operational delay of 5 ms. Similarly, the fault current is quickly damped after the current zero. A non-linearity is observed in the SA current due to travelling waves as the distance is considerable, i.e. 350 km, however, case 3 is severely affected by it. The oscillation in $V_{vi}$ after the current zero reaches lower amplitude as compared to Fig.6.

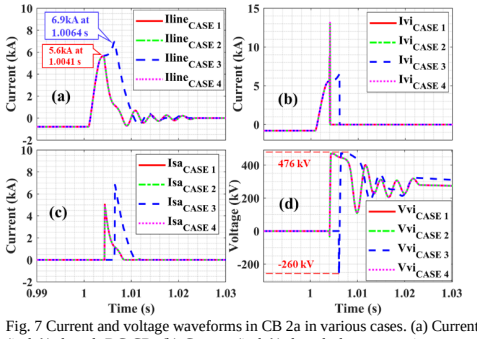


Fig. 7 Current and voltage waveforms in CB 2a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the Surge arrester (SA). (d) Voltage (in kV) across the VI

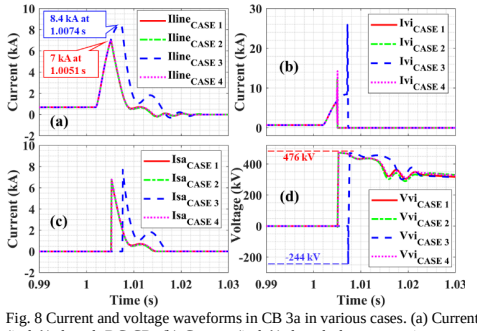


Fig. 8 Current and voltage waveforms in CB 3a in various cases. (a) Current (in kA) though DC CB. (b) Current (in kA) though the vacuum interrupter (VI). (c) Current (in kA) though the SA. (d) Voltage (in kV) across the VI.

### B. *MMC's Blocking Status*

Table 3 illustrates the blocking status of the MMC. It is observed that among all the cases, for various fault locations case 1 and case 4 do not block the converter. However, it is interesting to see that a fault that occurs on line 34 is mitigated for all cases except for case 2. This is due to the fact that the power flow between MMC 3 and MMC 4 is zero during the steady state. Hence, there is sufficient time for the current to reach the fault location.

Table 3 Blocking status of MMC for various case scenarios

| Location | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| Cable 12 - 0 | - | MMC 1 | - | - |
| Cable 12 - 50 | - | MMC 1 | - | - |
| Cable 12 - 100 | - | - | MMC 2 | - |
| Cable 13 - 0 | | MMC 1 | - | - |
| Cable 13 - 50 | - | - | - | - |
| Cable 13 - 100 | - | - | MMC 3 | - |
| Cable 14 - 0 | - | MMC 1 | - | - |
| Cable 14 - 50 | - | - | MMC 1 | - |
| Cable 14 – 100 | - | - | MMC 4 | - |
| Cable 34 - 0 | - | - | MMC 4 | - |
| Cable 34 - 50 | - | - | MMC 4 | - |
| Cable 34 - 100 | - | - | MMC 4 | - |

### C. *Energy absorption*

The total energy absorption by the SA consists of two sources, magnetic energy stored in the DC current limiter and the energy stored in the system. The energy stored in the DC

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current limiter is $\frac{1}{2}L_{DC}I_f^2$; the electrical energy supplied from the system during the fault current suppression. In some cases, the energy resulting from the grid side is even larger than the energy stored in the DC current limiter because of the system voltage recovery during the energy period. Fig. 9 shows the energy absorption by the DC CB's at a different location for various case scenarios during pole to pole fault. The amount of energy absorbed depends on the operational speed of the DC CB, as case 4 shows the fastest topology, it absorbs less energy than other cases. The energy absorption with different fault location is nearly constant. Similarly, in Case 3 the converter is not blocked, and the maximum energy absorbed by the SA is below 16 MJ.

For the selection of the DC CB technology based on the energy absorbed, a line can be drawn. A faster case i.e. case 4 can be used for cable 12 as the energy absorption difference between the opposite breakers (CB 1a and CB 2a) is larger. However, for cable 13 and cable 14, the difference in the absorbed energy is smaller, hence case 1 is found as suitable and similarly, for cable 34, case 2 can be used.

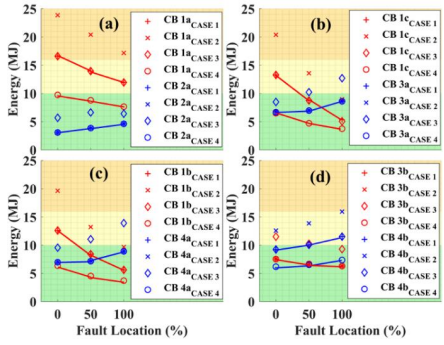


Fig. 9 Energy absorbed in the grid by DC CB's during various case scenarios in (a) Cable 12. (b) Cable 13. (c) Cable 14. (d) Cable 34.

### *D. Selection of DC CBs*

The selection of DC CBs for the specific MTDC should consider the maximum fault current, MMC blocking feature, operational delay of the breaker and the energy absorption. Since the requirement of the DC CBs depends on the magnitude of the interrupted current where they are implemented, for some terminals with a high rate of rise of the fault current, the application of fast VARC DC CBs are essential. On the other hand, for other terminals, when the mechanical DC CBs interrupt the fault without the blocking of the MMC converters, the combination of VARC DC CBs and mechanical DC CBs may reduce the cost of the MTDC protection system.

## VI. Conclusion

The paper presents a coordinative performance of an active injection mechanical DC CB and a VARC DC CB for a 320 kV 4-terminal MTDC grid. The worst-case scenario of a fault occurs for cable 12 and 13, when the fault is near the converter station. The coordinative performance of two types of DC CBs are demonstrated accordingly. For case 1, the combination of a mechanical DC CB and a VARC DC CB with an operational delay of 5ms and 3 ms respectively can successfully clear the fault without blocking the MMC converters. For case 4, VARC DC CBs installed at remote terminals can interrupt the fault.

The amount of energy absorption depends on the operational times and the type of DC CB, and the energy absorber should be designed accordingly. The coordinative operation of the DC CBs is very important as a possible failure at any DC CB may lead to the blocking of the converters. The methodology proposed in this paper can be applicable to other MTDC configurations in the future.

## VII. Reference

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# B

# Appendix B

*The work related of Model comparison and performance of model of different HVDC circuit breaker in MTDC grids is scheduled to submit to the* ***IPST 2021*** *with the title of* ***"Coordinative performance of HVDC circuit breakers in MTDC grids"***

B

# Comparison and Performance of Detailed and Average VARC model in MTDC System

Ajay Shetgaonkar, Marjan Popov, *Senior IEEE Member* and Siyuan Liu

***Abstract*—Direct current circuit breaker (DC CB) is the key to unlock the reliable operation of Multi-terminal direct current (MTDC) system, whereas fast, effective and accurate models are frequently needed for system-level studies. Due to higher subsystem components in DC CB, detailed DC CB model creates a bottleneck in the system. This paper proposes and compares, an Average model with a detailed model of Voltage-source-converter resonant current (VARC) DC CB in MTDC system in terms of their performance and computation time for two typical simulation cases. The Average and detailed model is modelled and simulated on the PSCAD/EMTDC electromagnetic transient platform . Finally, this paper concludes by presenting an accurate response of average a model during the fast transient event, showing additional computational advantage.**

***Index Terms*—Average model, VARC DC circuit breaker, HVDC, MTDC.**

## I. Introduction

THE reliable operation of MTDC system depends upon detection of DC fault and current interruption [1]. In case of point to point HVDC link, the fault is interrupted by operating the AC circuit breakers. Thus, lead to zero power flow in the HVDC link. However, incase MTDC system with large power infeed, to interrupt fault, each terminal of MTDC has to be disconnected if AC breakers are used, which results in the de-energization of DC grid. Moreover, this will reflect on the continuity of supply and is not economical. Hence, DC breaker plays an essential role in MTDC system as it provides complete selective fault isolation without affecting the power flow within healthy DC lines. Due to the higher rising rate of DC fault current, the DC breaker has to be faster than conventional AC breaker.

The DC CB's are classified into three types, namely, mechanical, solid-state and hybrid DC CB [2], [3]. In mechanical DC CB, Series RLC resonate circuit is used to create artificial zero crossings which ultimately interrupt fault current. The mechanical CBs are further classified into active and passive mechanical breakers. Among these, the active type is faster as the fault interruption time lies between 5 ms to 8 ms [2]. Whereas the time required by passive CBs to interrupt fault is between 20 – 40 ms [2]. Among all the DC CBs, the solid-state breaker is fastest with fault interruption within 1 ms [3], [4]. Solid-state consists of a cascaded connection of semiconductor devices to increase the voltage withstand capability. However, despite the faster operation, it cannot be applicable for high voltages due to high on-state losses in the main branches and limitation of the voltage rating of semiconductor switches. The Hybrid HVDC circuit breaker is the fusion of the mechanical switch(es) and power electronics. Thus, it has faster speed and lower on-state losses. Over the years, different concepts of the hybrid breaker are presented and demonstrated. In hybrid DC CBs, the fault current is interrupted within 5 ms [2].

In recent years, a novel DC breaker concept has been proposed which is know as VSC assisted resonant current (VARC) DC CB [5]–[7]. VARC DC CB make used of voltage source converter (VSC) in combination with resonating LC circuit to create high-frequency growing injected current oscillation in vacuum interrupter. The operating time of VARC DC CB is 3 ms. In 2018, a prototype of VARC DC CB with interrupting capability of 10 kA and transient interrupting voltage (TIV) of 40 kV had been demonstrated in the KEMA laboratories, Arnhem [5].

The previous studies on VARC DC CB have only focused on the performance of breaker in MTDC network using the detailed model. Despite this, no studies have been investigated the simplification of detailed VARC model for system-level study. Depending upon the purpose of the study, the HVDC DC CB can be modelled in the Electromagnetic transient simulation (EMT) programs with different degree of details. To identify the weak link within the DC CB, different critical components like vacuum interrupters, IGBTs, surge arrester and energy storage element has to be studied during the internal and external fault. Moreover, this study can be performed by considering the detailed model of the HVDC breaker. However, due to the larger number of switching devices with the higher switching frequency, results in large admittance matrix. Hence, the detailed model is not recommended for the grid level study with higher terminals as it requires large computational time and computing resources.

In context to the above problem, this paper proposes an average VARC model which can potentially run the simulation faster than detailed model without compromising accuracy in system study. Further, to demonstrate the effectiveness of the model, a comprehensive comparison between a detailed and average model which will guide the reader to make a deliberate decision to utilise and to have credibility on DC CB

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models' performance in MTDC system. Here, both models are implemented and simulated in PSCAD/EMTDC software and compared in terms of performance and simulation speed.

## II. Model Comparison and Calibration

### A. Detailed model of VARC DC CB

The modelling of the detailed model of VARC DC CB is discussed in [7] and illustrated in fig. 1. The author has comprehensively described the operating principle and time sequence. The model mainly consists of the three major branches, i.e. Main branch, Energy absorption branch and Current Injection branch. The main branch consist of Residual Circuit Breaker (RCB), Line Inductor ($L_{DC}$) and Vacuum Interrupter (VI). The Energy absorption branch mainly comprises of surge arrester (SA) and lastly, current injection Branch consist of oscillating inductor ($L_P$) and capacitor ($C_P$) in series with voltage source converter (VSC). To utilise this model for the grid application, it needs to be connected in series to scale to a higher voltage level. For 320 kV grid application, the series connection of 4 modules of VARC DC CB with a rating of 80 kV is used. In the detailed model

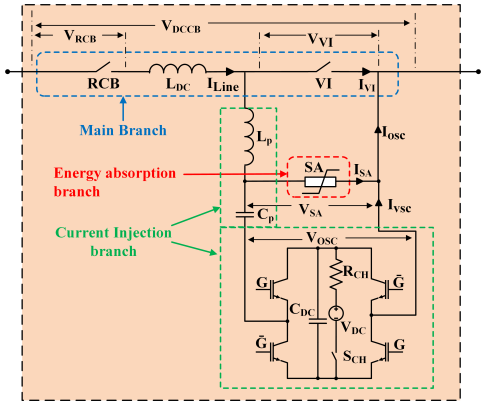


Fig. 1. Structure of VARC DC CB [7]

of VARC DC CB, the effect of the parasitic components has persevered. In this model, the current interrupting devices VI and RCB), semiconductor switches ("$G$" and "$\bar{G}$" ) and Surge arresters are adopted from the PSCAD master library. The highly non-linear arc characteristic, which exists in the physical breaker, is not modelled in the VI model. However, the non-linear characteristics of the components is persevered. Hence, accurate voltage and current stress can be observed not only at the component level but at the system level also. Due to detailed modelling, various aspect can be studied like temperature and energy dissipation in surge arresters, on state power loss in vacuum interrupter and the switching losses. Furthermore, the modular topology of VARC enables the voltage distribution study due to the delay of the trip signal to each module [7]. Hence, the detailed model reflects the actual configuration of the model topology, i.e. whether it is modular or series-connected VI topology.

The main drawback of the detailed model of VARC DC CB is that solving electrical circuits with non-linear elements take a significant amount of time and data due to the re-calculation of the admittance matrix at every time step. In the complex power system, the dimension of the admittance matrix is larger due to the higher number of nodes in the grids, which will further increase the computational time.

### B. Average model of VARC DC CB

Fig. 2 (d) shows the Average model VARC DC CB. Similar to the detailed model, the Average model has three major branches. During the fault neutralisation time (fig. 2 (a)), the vacuum interrupter of modules conducts; hence it can be represented by the single switch from the PSCAD/EMTP database. The Voltage rating of this switch will be equivalent to the system voltage. At the beginning of the fault current suppression time, the line current is commuted to the current injection branch. As a result, all the oscillating capacitor of modules are connected in series, as shown in fig. 2 b. Hence, the entire configuration is represented by a single capacitor. Furthermore, the value of this capacitance is equal to the equivalent series capacitance of the module's oscillating capacitor, which is given by (1).

$$C_{P_{eq}} = \frac{C_P}{N_m} \tag{1}$$

Where $C_P$ is an oscillating capacitor of a module and $N_m$ is the number of modules. Due to the presence of an equivalent oscillating capacitor, the interaction of this capacitor with the system can be analysed after the fault interruption. However, the oscillating inductance is omitted in the average model.

Upon clamping of the Surge arrester in the detailed model, the line current is commuted to energy absorption branch as presented in fig. 2 (c). Hence, all the surge arrested of the modules are connected in series during this period. As a result, a single surge arrester represents the series connected surge arresters with a rating of system voltage. Table I, provides the data for detailed and average model for 320 kV system.

TABLE I
Parameter of detailed and average VARC model for 320 kV system

| Parameters | Symbol | Detailed model | Average model |
|---|---|---|---|
| Oscillation inductor | $L_P$ | 95 $\mu$H | 0 $\mu$H |
| Oscillation Capacitor | $C_P$ | 2.72 $\mu$F | 0.68 $\mu$F |
| Rated / clamping voltage of Surge arrester | $V_{rated}/V_{clamp}$ | 80/120 kV | 320 / 480 kV |
| Initial Voltage across $C_P$ | $V_{iniC_P}$ | 10 kV | 0 kV |
| Number of modules | $N_m$ | 4 | 1 |

The vacuum interrupter (VI) and residual CB (RCB) in this model are modelled as a simple switch. This switch has two states, ON with lower value of the resistance and OFF state with the high value of the resistance. Furthermore, the switch is set to operate near current zero. Hence, this switch is

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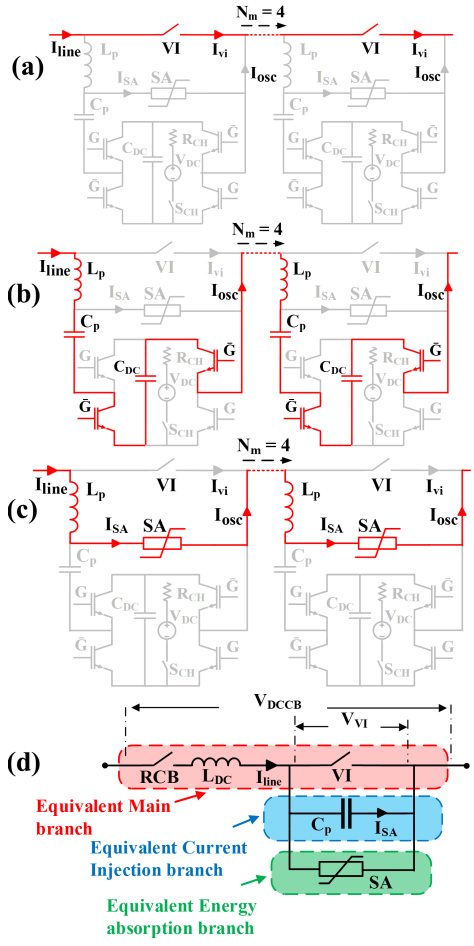


Fig. 2. Flow of line current in VARC DC CB. (a) During fault neutralisation time, (b) During rise of TIV, (c) During fault current suppression time and (d) Average model of VARC DC CB

accurate and reduces the computation time as the complexity of equation is reduced.

During the modelling, line inductor ($L_{DC}$) is considered as the linear electrical component. However, the SA is modelled as a non-linear element in EMTDC environment. In EMTDC software, the SA make use of Piecewise Linear Method, which reduces the amount of conductance matrix inversion per run with reasonable accuracy in outcomes [8]. Moreover, the details of the parasitic and grading components are removed in the average model.

Even though with the simplification of the current injection branch, Average VARC model provides higher accuracy in terms of the Energy absorption in SA and VI conduction losses. Further, the complex logic of VSC for each module is reduced.

## III. 4-Terminal MTDC System

Fig. 3 illustrates the 4-terminal test MTDC system, which is used to study the fault current interruption analysis. The converters used are half-bridge modular multilevel converters (MMC). The entire MTDC system is divided into two zones, onshore and offshore. The onshore consist of MMC 1 and MMC 2, which are then connected to the 400 kV AC grid via a transformer. The offshore grid consists of MMC 3 and 4, which are connected to the wind farms. The Onshore AC grids are independent voltage source. The MTDC system is configured as symmetric monopolar with ±320 kV dc voltage. The parameters of the MTDC system are indicated in Table II.

The four cables connect the Onshore and Offshore zone. The cable 12 with a length of 175 km, connects MMC 1 and MMC 2. While the MMC 3 is connected by 350 km long cable to MMC 1, whereas another offshore zone MMC is connected to MMC 1 via 300 km long cable. Both the offshore MMC are connected via 100 km long cable. The DC reactor, with the value of 10 mH, is installed between MMC and the bus. At each bus, which is indicated by the red dotted rectangle, consist of a line inductor and DC CB. The value of line inductance is 100 mH [9]. This system uses 320 kV XLPE insulated cable with surge impedance of 33.73 Ω and waves propagation velocity of $1.8310^8$ m/s. The frequency dependent phase model is used to represent cable in PSCAD environment.

The MMC used in this system is based on the continuous MMC model. The outer control loop of the MMC 1 and 3 controls the voltage, while MMC 2 and 4 controls the power. The MMC utilizes two protection strategies, first, MMC blocks, if the maximum arm current exceeds the 0.8 times the maximum current handling limit of the IGBT and second if the MMC voltage falls below 0.8.p.u, then MMC blocks.

## IV. Model Performance and Validation

A comparison of the two different models of the VARC DC CB can be made based on different technical performance Both models have a current interrupting functionality. The DCCBs in both models can interrupt designed fault current.

The Average model shows similar technical performance with the detailed model. However, there is a small margin of error in some scenarios, for example, the nature of the injected oscillating current. In the VARC detailed model, the amplitude of injected oscillation current changes after each reversal. Whereas due to the lumped capacitor ($C_P$) in an Average model, this growing oscillation is absent.

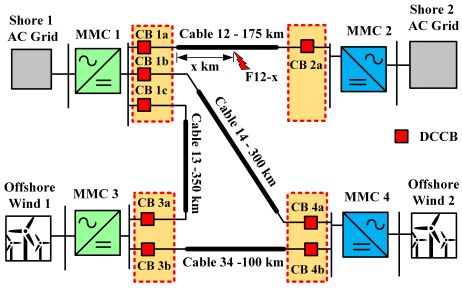


Fig. 3. 4- Terminal MTDC system

TABLE II
DATA OF 4- TERMINAL MTDC SYSTEM

| Parameter | Converters | | | |
|---|---|---|---|---|
| | MMC 1 | MMC 2 | MMC 3 | MMC 4 |
| Active power | 500 MW | 500 MW | 500 MW | 500 MW |
| Control mode | PVdc | PVdc | PQ | PQ |
| Reactive power | 100 MVAR | 100 MVAR | 100 MVAR | 100 MVAR |
| DC link Voltage | ±320 kV | | | |
| Rated power | 1256 MW | | | |
| Number of Submodules per arm | 400 | | | |
| Arm capacitance Carm | 22 μF | | | |
| Arm reactor Larm | 42 mH | | | |
| Arm resistance Rarm | 0.544 Ω | | | |
| AC converter voltage | 400kV | | | |
| Transformer leakage reactance | 0.18 p.u | | | |
| AC grids and windfarms | | | | |
| AC grids voltage | 400 kV | | | |

Besides, the Average model loses some of the curial component level information like VSC's Voltage and Current stress, Voltage sharing and Redundancy. Furthermore, the scaled topology information is absent in the Average model. In additionally, the Average model can provide necessary information on the estimation of SA energy absorption, VI power loss estimation and fault interruption capability. For verification, two transient studies are performed.

### A. Terminal short circuit at MMC 1

In the first study, a pole to pole fault is applied at the terminal of MMC 1 in cable 12. Initially, the system attends the steady-state condition after 0.9 s with steady sate current of 0.87 kA. At 1 s, the fault is applied. As a result, fault current rises with a rate of 2.9 kA/ms. The fig. 4 compares the Current and Voltage response of the detailed and Average model of VARC DC CB during Terminal short circuit on the cable 12 near MMC 1 for positive pole. Both models show an identical overlap of the Voltage across the DC CB during fault current suppression and neutralisation time. Similarly, both models have information about post fault interrupting oscillation. The cause of this oscillation is due to the interaction of system inductance and oscillating capacitor ($C_P$) of both models. The frequency of this oscillation is $f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{110mH \times \frac{2.72\mu F}{4}}} = 580Hz$. Furthermore, due to higher damping components, the detailed model has a lower peak of this oscillation. In both models, the oscillating capacitor ($C_P$) determines the rate of rise of TIV. Also, both models have information about the TIV during the fault current suppression time, and the peak value is 1.5 times the rating surge arrester.

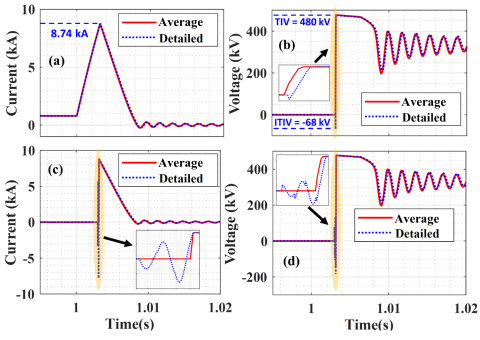


Fig. 4. Comparison of VARC models during the Pole to pole fault on cable 12 near converter station 1.(a) CB 12 a Line Current (kA) (b) CB 12 a Voltage (kV) (c) CB 12 a injected current (kA) (d) CB 12 a SA Voltage (kV)

In the detailed model, Without considering the losses in the DC CB, the peak value of injected current is expressed as follows:

$$I_{OSC_{pk}} = \frac{(N+2) \times V_{DC}}{\sqrt{\frac{L_P}{C_P}}} \tag{2}$$

Where N is the number of reversal within the VSC. To reach the fault current amplitude of 8.74 kA, four reversal take place within VSC. Hence after four reversals, the prognosticated peak amplitude of injected current will be 10.15 kA. However, due to lower fault current, the current in the vacuum interrupter (VI) is interrupted at the non-peak value of injected current. As a result, ITIV with the amplitude of -68 kV is developed across the VI which can be theoretically computed by

$$V_{ITIV} = N_m \times (N+1) \times V_{DC} \cos\theta \tag{3}$$

$$\theta = \sin^{-1}\left(\frac{I_f}{I_{OSC_{pk}}}\right) \tag{4}$$

Where $N_m$ is the number of VARC modules, furthermore, the theoretical value of ITIV is about 30% higher than simulated value due to the resistive losses.

The average model of VARC does not provide information about the ITIV as observed in fig. 4. Similarly, the information about the nature of the injected current is absent. However, the average model accurately follows the envelope of the detailed model with a smaller error in voltage and current, as indicated in table III.

There is an energy difference of 0.2 MJ between the Average and detailed model. This energy difference occurs due to the extra time taken by the injected current to reach the peak

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TABLE III
PERCENTAGE OF ERROR OF AVERAGE MODEL FROM DETAILED MODEL DURING TERMINAL SHORT CIRCUIT AT MMC1

| Signals | % of Error |
|---|---|
| Line Current | 1.18 |
| Voltage across DC CB | 0.12 |
| Injected Current | 1.17 |
| Voltage across Surge arresters | 0.04 |

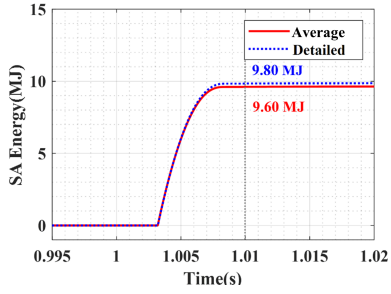


Fig. 5. Comparison of the energy absorbed in CB 1a during terminal short circuit for average and detailed VARC model

current value of the fault current, as shown in fig. 5 (a). The following steps can theoretically calculate this extra time: The injected current is given by

$$I_{OSC} = I_{OSC_{pk}} \times \sin(\theta) \tag{5}$$

At the end of fault neutralisation time, $I_{OSC} = I_f$. Thus for given data, $\theta = 60^\circ$ and extra time, $t = \frac{0.1ms \times 60^\circ}{360^\circ} = 1.5 \times 10^{-5} s$.

The energy difference can be calculated based on the amount of current flows through SA, the voltage across SA during energy absorption and the period for which this current is flown into SA. Considering the rate of rise of fault current is 2.9 kA/ms and assuming the constant value of SA voltage and current during fault current suppression time, estimated energy absorbed by the average model is $E_{SA_{avg}} = 4 \times 8.7kA \times 120kV \times 5ms = 20.8MJ$. Similarly, in detailed model, energy absorbed by SA is $E_{SA_{det}} = 4 \times (8.7kA + 2.9kA/ms \times 1.5 \times 10^{-5}) \times 120kV \times (5ms + 1.5 \times 10^{-5}) = 21.0MJ$. Hence, net difference of both model SA energy is 0.2 MJ.

The fig. 6 (a) illustrates the MMC 1 positive pole bus voltage during the terminal short circuit is for both models. As can be seen from fig. 6, during the terminal fault, MMC 1 voltage drop initially followed by a gradual drop in voltage. The value of line inductance determines the rate of this drop. Further, with the operation of DC CB at 1.003 s, a spike is observed only in the detailed model, which represents the ITIV. Due to the TIV, the bus voltage starts to recover. However, after the current zero in Vacuum interrupters, the bus voltage is superimposed by the oscillation of 580 Hz. This oscillation represents the interaction of $C_P$ and system inductance, as explained in the previous paragraphs. Moreover, this oscillation is eliminated with the operation of the residual circuit breaker (RCB). During the entire fault scenario, the MMC remains unblocked, as the protection criteria are not violated. Furthermore, the MMC 1 positive pole current, reaches 4.4 kA at 1.003 s, after which it drops with a rate determined by the clamping voltage. However, the MMC remains in operation after current interruption as only faulty line is isolated. The cable voltage of positive pole seen from both MMC's i.e 1 and 2, yields similar results for both models. Moreover, the cable voltage seen from MMC 2 has oscillations (fig.6 due to the reflection of the travelling wave during to the transient event.

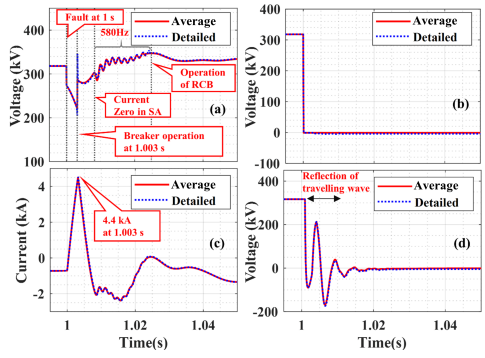


Fig. 6. Average and detailed Model Comparison during the Pole to pole fault on cable 12 near converter station 1 in Positive pole (a) bus voltage (kV) (b) Cable voltage observed from MMC 1 (kV) (c) MMC 1 current (kA) and (d) able voltage observed from MMC 2 (kV)

### B. Steady-state current interruption

In the following study, a switching action is carried out in cable 12. The MTDC system is again operating at the steady-state condition with line current of 0.87 kA in cable 12. Then, at 1 s, a switching action is carried out in cable 12 by sending a trip signal to the CB 1a and CB 2a. At the lower current interruption, only the main and current injection branch interact with the system. Hence, line current in both the models has oscillation with the frequency of 580 Hz after the fault neutralisation time. This oscillation arises from the interaction of the oscillating capacitor and system inductor, as explained in the previous section. Moreover, the energy absorption branch is not engaged as the voltage across the surge arrester does not reach the clamping voltage of 480 kV.

The VARC DC CB is primarily designed to interrupt the rated fault current. Thus with the first reversal of VSC voltage, the peak value of injected current given by (2) is 3.3 kA (fig. 7 c). Moreover, due to the higher value of the $I_{OSC_{pk}}$, corresponding ITIV is higher. The value of ITIV can be estimated using (3) and (4) with N = 1, which result in the theoretical value of -155 kV. The resistive losses cause about 3% lower value of ITIV in the simulated result than

theoretically. However, due to the equivalent representation of the current injection branch is the average model, the details about $I_{OSC_{pk}}$ and ITIV are missing. Similarly, the Voltage stress information about the surge arrester is omitted. Throughout the entire transient study, the result anticipated by the average model remains in great harmony concerning the reference solution by detailed model.

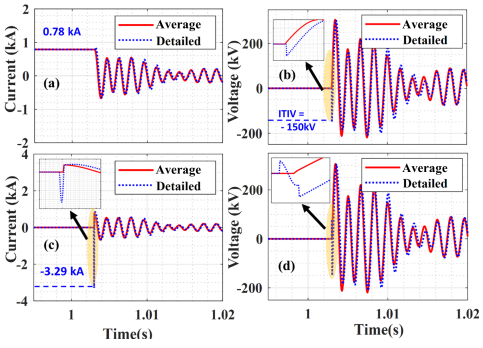


Fig. 7. Comparison of VARC models during Steady-state current interruption in cable 12. (a) CB 12 a Line Current (kA) (b) CB 12 a Voltage (kV) (c) CB 12 a injected current (kA) (d) CB 12 a SA Voltage

During low current interruption, the current and voltage signals in average model show identical curve profile with slightest error as shown in table IV

TABLE IV
PERCENTAGE OF ERROR OF AVERAGE MODEL FROM DETAILED MODEL DURING STEADY-STATE CURRENT INTERRUPTION

| Signals | % of Error |
|---|---|
| Line Current | 3.55 |
| Voltage across DC CB | 0.94 |
| Injected Current | 3.51 |
| Voltage across Surge arresters | 0.68 |

## V. COMPUTATIONAL TIME

The 4-terminal HVDC system is simulated for 1.2 s using the detailed and average model at two different time steps. The simulations were performed on same PC with 8 GB of RAM using PSCAD V4.6.

As the average modelling of MMC's of 4-terminal HVDC system, the simulation can run at higher time steps maintain acceptable accuracy. This HVDC system can run at a time step of 2 - 10 $\mu s$, without losing its dynamic response. For detailed VARC model, the time step of at most 2 $\mu s$ is required to maintain the accuracy. Hence the detailed model creates a bottleneck in the system. As a result, the overall time step is reduced for the accurate transient and steady-state response.

Due to the reduction in the admittance matrix, the average model of VARC can be simulated at higher time steps without uttering the transient response. The preferred time step for the average model is at least 10$\mu s$. The comparison of simulation speed for two models is summarized in table V. As can be seen from table V, the average model reports lower simulation time with the difference of 19 min from the detailed model.

TABLE V
COMPARISON OF COMPUTATION TIME OF DIFFERENT MODELS FOR TIME INTERVAL FROM T = 0 S TO T = 1.2 S

| Model | Time step | Simulation time |
|---|---|---|
| Detailed model | 2 $\mu s$ | 22 min |
| Average model | 10 $\mu s$ | 3 min |

## VI. CONCLUSION

In conclusion, this paper presented the comparative study of two different model representation of VARC DC CB technology, namely, Detailed and Average model in PSCAD. The performance of the proposed average model was examined graphically and theoretically for the low and high current interruption. The results contained in this paper have illustrated that the average model provides a good level of accuracy during the transient condition. The significance of the Average model was that it had reduced the simulation time by 86% than the detailed model without losing accuracy, thereby enabling the Average model for the system-level simulation. Hence make it computationally efficient.

It was interesting to note that the percentage of error during terminal short circuit was lower than during low current interruption. Furthermore, the module's component information was absent in the average model. Similarly, the details of ITIV and scaling information were absent. The developed average model and results will be useful to the researcher and practice engineer in the power system area, which deals with HVDC transient and system studies.

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