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Review

Exploring the benefits, challenges, and feasibility of integrating power electronics into c-Si solar cells

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SUMMARY

Power electronics traditionally plays a crucial role in conditioning the power of photovoltaic (PV) modules and connecting the systems to the electricity grid. Recently, PV module designs with more sub-module power electronics are gaining increased attention. These designs can offer higher reliability and improved resilience against non-uniform illumination. In this review, we explore an innovative method to facilitate sub-module power electronics, which is to integrate the power components into crystalline silicon (c-Si) PV cells. This approach has the potential to enable numerous design innovations. However, the fabrication processes of the integrated power electronics should be compatible with the PV cell fabrication methods. Moreover, only a limited amount of additional processing steps can be added with respect to standard solar cell manufacturing processes to achieve a cost-effective design. After reviewing previous research on this topic, we propose various new design possibilities for PV-cell-integrated diodes, transistors, capacitors, and inductors. Furthermore, we discuss the technical trade-offs and challenges that need to be overcome for successful industry adoption.

INTRODUCTION

About 95% of the worldwide photovoltaic (PV) capacity is currently based on crystalline silicon (c-Si) cells.[1] The PV industry mainly produces c-Si -based modules with standardized designs, aimed at producing cheap power under uniform irradiation.[2] This approach has already led to record-low utility-scale solar energy prices below 2 $/kWh in different regions around the world.[3] Power electronics is essential to condition the power from PV modules.[4] For example, power electronics is necessary to implement maximum power point tracking (MPPT), which ensures that the operating point of the PV system always corresponds to its maximum power.[5] Furthermore, power electronic converters are used in grid-connected systems to connect the PV modules to the electricity grid.[6] This connection can be performed through various system architectures.[7] For large-scale PV power plants, the central inverter or string inverter topology is most commonly used.[5] Nevertheless, systems with module-distributed power electronics architectures can be used to better deal with mismatch effects between PV modules. Indeed, the energy yield under partially shaded conditions can be increased substantially by using PV system topologies with micro-inverters[8] or direct current (DC) power optimizers.[9]

Furthermore, power electronics plays a crucial role within PV modules. It is well known that PV modules are affected by current mismatching between different cells,

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which can, for example, be caused by inhomogeneities during production, partial shading, dirt, thermal gradients, or aging.[10] When certain cells of a PV module become shaded, they might become reverse biased, acting as loads instead of generators. This can lead to hot-spot issues, hereby irreversibly damaging the affected cells.[11] In conventional PV modules, this effect is typically mitigated by connecting bypass diodes in antiparallel to three substrings of series-connected cells.[12] Nevertheless, the incorporation of bypass diodes into these standard designs does not completely eliminate the hot-spot problems.[13] Furthermore, the power production of PV modules with these standardized module designs drops substantially under non-uniform operating conditions. To illustrate this, the power production decreases by a third when only a single PV cell, corresponding to less than one-sixtieth of the module area, becomes shaded.[14] Thus, to further improve the reliability and energy yield of PV systems in non-uniform operation conditions, different PV module topologies are being investigated.[10,15,16] For example, the number of bypass diodes in a module can be increased. This can be done up to the point where the number of bypass diodes in the module equals the number of solar cells.[17,18] Alternatively, series and parallel interconnections in PV modules can be changed during operation to optimize the energy yield depending on the uniformity of the illumination, which is usually referred to as the reconfigurable module concept.[19] Furthermore, power conversion can be performed at a sub-module level, allowing for MPPT with higher granularity.[20–22] This way, the operating point of smaller groups of solar cells can be adapted without affecting the operation of the other cells in the PV module.

Power electronics for module or sub-module purposes is typically attached to the PV module frame, installed in the PV junction box, or embedded into the PV laminate.[20,23,24] However, in this review, we explore a different approach to facilitate sub-module power electronics, increase granularity, and enable novel approaches to power conditioning. This approach is to integrate power electronics into c-Si PV cells, which could be a next step in the development of PV-based intelligent energy agents.[2] In particular, we discuss the integration of diodes, transistors, capacitors, and inductors, since they are the basic power electronic components relevant to PV modules. In the following section, the most important possibilities and benefits of cell-integrated power electronics are explained. Then, we review the research efforts that have been performed on the topic so far and outline the feasibility of different unexplored possibilities. In the final sections, the challenges and a concluding discussion are presented.

BENEFITS AND POSSIBILITIES

Integration of power electronic components into c-Si solar cells could enable a whole new range of design possibilities as well as benefits for PV systems. In this section, some notable examples are discussed, after which the costs and benefits of these solutions are described.

Design innovations for module- and system-level power electronics

When considering common PV system topologies that are in use nowadays, possibilities for new designs would be enabled by integrating part of the power electronic components into c-Si PV cells. For example, most module-level power optimizers are attached to the back of each PV module in a separate enclosure.[9] In power converters, the inductor is generally the bulkiest and most expensive component.[25–28] Thus, it could be beneficial to integrate the inductor onto the solar cells instead. By leaving the inductor out of a power optimizer, the development of smaller,

simpler, and cheaper designs could be enabled. Another example is that bypass diodes could be integrated into the PV cells directly instead of being connected externally in the junction box. This could facilitate the development of simpler and smaller junction boxes.

Support the development of shade-resilient PV modules

In the introduction, several approaches were described that can be deployed to improve the shade tolerance of PV modules. These were increasing bypass diode granularity, applying a reconfiguration strategy, or performing sub-module MPPT. However, for increased power electronics granularity, these approaches can make the junction box bulkier. Besides, it has to be taken into account that each of the individual power electronic components that is added has a probability to fail, which could eventually affect the system reliability. Especially failure in the solder joints of discrete power transistors has been identified as one of the main failure modes of power converters in PV applications.[29,30] This type of failure could be mitigated by integrating the transistors into the PV cells and connecting them monolithically. Thus, by integrating power electronic components into the c-Si PV cells, it might become possible to realize shade-tolerant PV modules that have higher reliability and do not require a bulky junction box. Moreover, researchers have performed attempts toward shade-tolerant PV module designs by lamination of sub-module power converters. In Deline et al.,[20] sub-module power optimizers based on a buck converter topology were laminated within the PV module. Bauwens et al.[31] instead proposed switched-capacitor converters as an alternative to reduce the cost and volume of sub-module power converters and facilitate their lamination. However, switched capacitors typically work with fixed conversion ratios between their input and output voltage, therefore they are less suited for MPPT applications. Integrating power electronics into PV cells could work well with the lamination approach, as it would be advantageous if the relatively bulky components such as inductors were integrated into the solar cells. By reducing the cost and size of the external power electronic devices, such a solution would pave the way toward small-area system-on-chip solutions that can be laminated in any place of the PV module to enable granular power optimization. Taking these ideas one step further, the combination of laminated and cell-integrated power electronics could even remove the need for junction boxes altogether. If most power electronics were integrated into the cells themselves, only their driving circuits would remain. These components have such a small area that they could be laminated into the small gaps that are present in between the PV cells.

Enable cable-free PV modules through wireless power transfer

Integration of power electronics into c-Si solar cells brings DC-alternating current (AC) conversion within PV modules one step closer. This not only allows sub-module MPPT but might at the same time facilitate wireless power transfer (WPT). WPT was the dream of Nikola Tesla,[32,33] and has the potential to revolutionize energy transmission, similar to the way that wireless communication has almost completely replaced telegraphy with wires.[2] Conventionally, the housing of PV modules is opened up beneath the junction box to connect the strings of cells. For a PV module that is capable of WPT, the housing can be completely sealed off instead. This would increase the reliability of PV modules as well as making the on-site installation procedures simpler and safer. It is worth mentioning that not only would the PV modules require design changes to enable WPT but the point where they are installed should be adapted as well.

Simplify the development of autonomous devices with integrated PV cells

There are various autonomous devices available on the market that are directly powered by PV cells. For example, many consumer or lighting products are presented by Apostolou and Reinders.[34] Moreover, using PV to power wireless sensors for Internet

of Things (IoT) applications is gaining attention.[35–38] In such autonomous devices, power electronics is typically deployed to perform MPPT and condition the power from the PV cell.[39,40] Thus, in these applications, the power electronics is often working with a single PV cell already, making the integration of part of the electronics into the cells more straightforward than for complete PV modules. Furthermore, as these PV cells often produce small currents, the design of the power electronic components is simpler. If manufacturers of autonomous devices powered by PV could directly buy PV cells that can condition their power, the remaining fabrication process would be simplified significantly.

Cost-benefit analysis

Most of the proposed concepts of integrating power electronics into c-Si PV cells will require additional costs compared with regular cell production. For that reason, it is important to reflect on the general trade-off between the costs and benefits of cell-integrated power electronics.

The costs of modern PV rooftop systems range between 1.05 and 1.85 €/Wp, of which 0.03–0.25 €/Wp can be attributed to the power converters, depending on the topology that is used.[1] To realize shade-resilient modules, the system costs increase as a result of the additional power electronics that is added at the sub-module level. The incremental costs for adding power electronics should be compensated by the additional energy that is generated due to the increased shade resilience of PV modules. Studies have shown that the energy yield in locations with partial shading can be increased up to 25%–30% when shade-resilient PV modules are used instead of conventional designs.[41,42] For PV module designs with either a reconfiguration strategy or sub-module DC-DC power optimizers, cost-benefit analyses have shown that the concepts can be profitable in locations where partial shading occurs regularly.[43,44] The incremental costs of adding sub-module power electronics can potentially be lowered by integrating (part of) the power electronics into PV cells. As was described previously, there is a wide range of possibilities in which shade-resilient PV module designs could be supported by this approach. Since the development of cell-integrated power electronics is relatively unexplored, it is not possible to quantify the capital expenditures yet. For instance, the various concepts that are described in this manuscript do not necessarily need to be applied simultaneously on the same cell. As such, the costs depend entirely on the exact components and topologies that are used. Finally, it should be mentioned that the system-level costs can be lowered by designing a module with mostly regular cells, and only a few cells with integrated components. Manufacturers could potentially realize such a module by processing the cells with integrated power electronics in a separate production line. However, it could also be a possibility that new companies enter the market that only focus on the production of these advanced cells.

When considering the autonomous PV devices described earlier, the cost-benefit analysis is different. The benefit in this case is in simplicity and volume. For instance, if the full converter is integrated into the PV device, the manufacturers of autonomous devices would no longer need to design the power electronics needed for MPPT. Furthermore, the volume usually taken up by the power converter is freed up. Concerning costs, it is important to notice that the PV cells used to power autonomous devices are often smaller than those used in conventional PV modules. When several cells with integrated power electronics are processed on a single wafer, the costs per cell for integration of the power electronics would become lower. Further research is required to verify whether this approach can indeed become cost-effective.

FEASIBILITY

Although integration of power electronics into c-Si solar cells is a relatively novel research field, several first attempts have already been made. In this section, we review the work that has already been done on this topic, and we will propose new concepts and investigate their feasibility. When exploring the different options to integrate power electronics into solar cells, aside from the cost-effectiveness, one of the most important factors that need to be considered is the ease of integration, which can be captured in two main points.

First, to create a c-Si solar cell with integrated power electronic components, it is necessary to adjust the fabrication processes used for regular cells. As the standard fabrication processes are thoroughly optimized to make high-efficiency cells, the changes must have as limited an impact as possible on the performance of the solar cell device itself. The processing steps needed to integrate the power electronics should not harm the solar cell and vice versa. For example, plasma etching is often used for transistor fabrication, since it allows for high-resolution pattern transfer to the underlying layer with less undercutting than for wet etching steps.[45] However, plasma etching steps can be detrimental to the passivation of a solar cell.[46] Thus, the first factor determining the ease of integration of a power electronic component into a solar cell is the extent to which the fabrication process is compatible with the manufacturing process of a solar cell.

Second, some of the integrated power electronics designs compete with the PV cell area used for the collection of charge carriers. For example, this is the case for integrated semiconductor devices like diodes and transistors, which should thus occupy as little area as possible to maintain a high PV conversion efficiency. When these devices are fabricated in industry, the maximum number of devices that fit on the wafer is processed simultaneously. This scalable nature of the process facilitates cheap manufacturing.[47] However, in the integrated approach, we postulate that only a few of these small-area devices are processed per wafer. Thus, for this approach to become cost-effective compared with discrete power electronics from industry, it is crucial that only a limited number of additional processing steps are introduced compared with standard solar cell manufacturing. Combining some of the processing steps required for the fabrication of power electronics components with similar processing steps that are already used for the fabrication of the solar cell would be the smartest way to reduce the total processing time and cost. Several examples of designs where fabrication steps can be combined will be given later in this section. Thus, the second factor determining the ease of integration of a power electronic component into a solar cell is the extent to which its fabrication steps can be combined with fabrication steps that are already used to create PV cells.

Furthermore, it should be mentioned that the optimal design of integrated power electronic components depends on the PV cell structure that is considered. Thus, it is important to distinguish between front-back contacted (FBC) and interdigitated back contacted (IBC) PV cells. Both types of structures are presented in Figure 1. Although the contacts responsible for collecting charge carriers are located on opposite sides of the wafer in FBC designs, all contacts are located on the back of the cell in IBC designs.[5] The different power electronic components that are considered for integration can also have either vertical (contacts on opposite sides of the wafer) or lateral structures (contacts on the same side of the wafer). As a result, there are many design options available for the integration of power electronics into PV cells. In this article, we consider lateral and vertical power electronic components

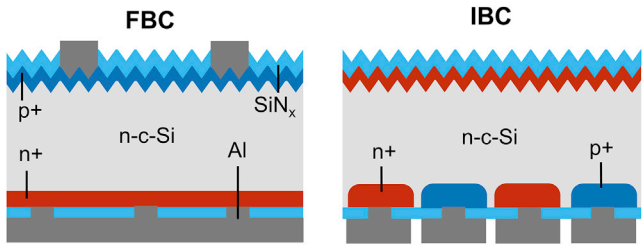

Figure 1. Standard c-Si PV cell structures

as well as FBC and IBC PV cell structures. Finally, it is worth noting that, in the case of bifacial cell designs, additional optimization is required for some of the proposed concepts.

Diodes

Standard c-Si-based PV module designs include several bypass diodes in the junction box. There are two main types of diodes being used nowadays, which are the pn junction diode and the Schottky barrier diode. Both devices can be fabricated in lateral and vertical designs, as presented in the example structures in Figure 2. Note that the n-c-Si region in the figures is a lowly doped drift region that is present to increase the reverse breakdown voltage. In low-power diodes that do not require a large blocking voltage capability, such a drift region is not required.[48]

Since diodes consist of metal-semiconductor contacts and pn junctions, there are some clear similarities with various c-Si solar cell designs. These similarities were already noticed by Green et al. in 1981, who reported the development of solar cells with integrated bypass diodes.[49] When these devices were used in a PV module prototype, improved shade resilience was demonstrated.[50] A few decades later, in 2012, a new study about a PV module with cell-integrated bypass diodes was published.[51] In this work, the leakage currents of the diode in reverse-bias conditions were reduced by isolating the device from the solar cell substrate by laser isolation.

In all the studies that were just mentioned, a pn junction diode with a vertical structure was integrated into an FBC solar cell. Indeed, if we compare the vertical diode structure of Figure 2B with the FBC solar cell structure of Figure 1, the clear similarities between the two allow for high ease of integration. However, there are some inherent drawbacks to this approach, which can be explained by reviewing some theory about breakdown in pn junctions. The breakdown voltage of a pn junction is the reverse-biased voltage at which the current rapidly increases. Two mechanisms that can cause breakdown in pn junctions are the Zener effect and the avalanche effect.[52] Zener breakdown occurs in highly doped pn junctions through a tunneling mechanism. Avalanche breakdown occurs when charge carriers moving across the space charge region acquire sufficient energy from the electric field to create new electron-hole pairs by colliding with atomic electrons within the depletion region. In diodes, the breakdown voltage due to Zener and avalanche effects can be increased by lowering the doping concentration of the lowly doped drift region.[45] However, lowering this doping concentration implies that the depletion region of the pn junction extends further into the lowly doped region. This can induce a third breakdown mechanism, called punch-through breakdown, where the depletion region extends all the way across the drift region under influence of a reverse-bias voltage.[52] The lowest diode on-resistance per unit area of the wafer can be achieved when the drift region length is minimized while still preventing

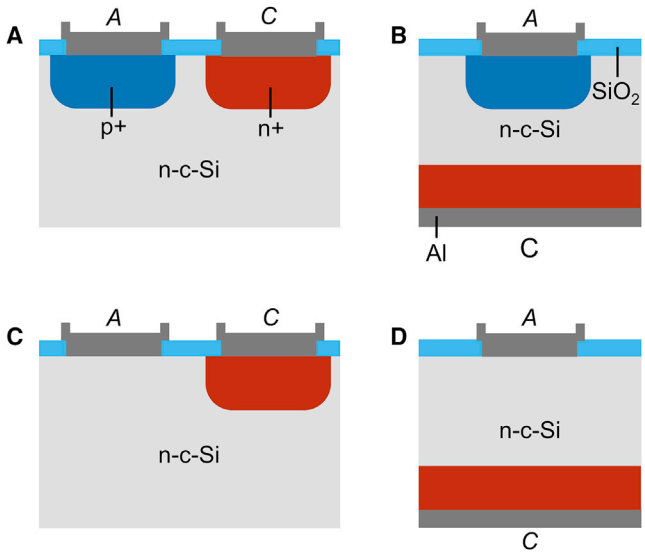

Figure 2. Basic diode structures

(A) Lateral pn junction diode. The anode and cathode are represented by A and C, respectively.

(B) Vertical pn junction diode.

(C) Lateral Schottky barrier diode.

(D) Vertical Schottky barrier diode.

punch-through breakdown. Thus, for diodes fabricated in industry, the doping concentration and length of the drift region are carefully optimized to minimize the on-resistance of the device while achieving the desired blocking voltage capability.[48] Considering the above, it becomes clear that the major drawback of integrating a vertical pn junction diode into an FBC solar cell is that there is little flexibility to tune the length and doping concentration of the drift region. Most solar cells produced in the photovoltaic industry nowadays are based on boron-doped p-type wafers with a thickness of around 100 μm.[3,53] At the pn junction doping levels that are typically used in c-Si PV cells, a combination of Zener and avalanche effects is typically causing breakdown.[54–56] Depending on the illumination conditions and temperature, the breakdown voltage of pn junctions in c-Si PV cells was reported in the range of 10–25 V. However, as the PV wafer thickness is usually 100 μm or higher, the drift region length of a vertically integrated diode is unnecessarily long with respect to such blocking voltages.[48] As a result, the on-resistance per unit area of the wafer of a vertically integrated diode is sub-optimal. Despite this drawback, the on-resistance of vertical diodes can be lowered by increasing the cross-sectional area of the diode. This way, the dissipation losses can be reduced, which ensures that the diode temperature does not rise dangerously above that of the rest of the cell.[57] However, as already explained earlier, it is crucial for integrated power electronics that their surface area is as limited as possible to maintain a high PV conversion efficiency. In the I-V curves of the vertically integrated bypass diode in Chen et al.,[51] it can indeed be seen that the trade-off between a low diode on-resistance and a high PV conversion efficiency resulted in a device with a larger on-resistance than is achieved for state-of-the-art bypass diodes. Thus, to make vertically integrated diodes a success, further research to adequately handle this trade-off is required. Furthermore, if we consider the role that vertically integrated pn junction diodes can play on a system level, we have to take into account that blocking voltages in the range of 10–25 V can be expected. Although the devices would thus not be able to block the voltage of 60 cells, they could play a role in PV module designs with a high bypass diode granularity.

An alternative method that has not been reported thus far would be to integrate a pn junction diode with a lateral structure into a c-Si solar cell. As the lateral design has highly doped p^+ and n^+ regions on the same side of the wafer, the ease of integration might be higher for IBC than for FBC PV cell structures. An important advantage of the lateral diode design is that the length of the drift region can be controlled. Thus, the bias voltage at which avalanche or Zener effects cause junction breakdown can be chosen as the aimed breakdown voltage of the device, and the drift region length can be adjusted accordingly to prevent punch-through effects. However, a drawback of these lateral structures is that the width of the device needs to be large enough to accommodate for a sufficiently low on-resistance in forward bias. As the resistive effects in the metal contacts start to play a role in devices with a large width,[58] designs where separate diodes are connected in parallel might be most efficient. Furthermore, also for integrated lateral diode designs, the total area of the device must be as limited as possible.

Most arguments that are thus far made for vertical and lateral pn junction diode structure are also true for Schottky diodes. However, Schottky barrier diodes can offer some important advantages over pn junction diodes. Most notably, the on-state voltage drop over the Schottky diode is lower and it has faster switching capabilities due to it being a majority carrier device.[52] Although a low Schottky barrier height facilitates a low on-state voltage drop, a minimum barrier height is necessary to achieve sufficient blocking voltage capability and suppress leakage currents in reverse bias. Schottky power devices are typically designed with a barrier height of around 0.7 eV.[59] To achieve a sufficiently high Schottky barrier for n-type silicon, high work function metals such as Cr, W, Mo, and Pt are typically deployed. These materials are rarely used as metal contacts of solar cells, which poses a challenge to the ease of integration. When considering metals that are more commonly used in PV cells, such as Al and Ag, these are known to result in relatively low Schottky barrier heights below 0.6 eV for both n-type and p-type wafers.[60] However, in the case of Al/p-Si, it has been shown that the diode performance can be improved if the metal deposition is preceded by a certain wet etching, dry etching, or implantation step. Using these fabrication methods has resulted in devices with a Schottky barrier height between 0.75 and 0.83 eV and good ideality factors between 1.05–1.25.[61–63] As such, integration of Al/p-Si Schottky diodes into p-type PV cells could result in well-performing devices with high ease of integration.

Transistors

Optimal operation of PV is not possible without transistors. These devices are necessary for power optimizers and inverters that are already commonly used in PV systems nowadays. In this article, we argue that power conversion at sub-module or even cell level can be facilitated by including transistors into c-Si solar cells. When it comes to power converters, high switching frequencies are considered beneficial since they allow for smaller passive components.[64] Therefore, solar-cell-integrated transistors should ideally be able to switch at high frequencies when they are part of a sub-module power converter. Another application of cell-integrated transistors is to facilitate the reconfigurable module concept. A straightforward design of reconfigurable modules is to implement the so-called reconfiguration matrix on a printed circuit board that is installed into the junction box. However, the potential benefits of solar-cell-integrated transistors to support reconfigurable module concepts have already been mentioned in previous research.[65,66] The transistors used in reconfigurable modules must either conduct or divert the current generated by (groups of) PV cells, but they do not work at a high switching frequency. Therefore,

compared with the transistors used in power converters, it is more crucial to reduce on-resistance to limit conduction losses than to focus on high-speed designs.

First, it must be noted that for the fabrication of transistors, photolithographic patterning steps are used.[45] Although photolithography is known to work well in supporting high-efficiency PV cell concepts such as IBC designs, it is a relatively costly process that the photovoltaic industry is trying to move away from.[67–69] As such, the need for lithography poses a challenge to the cost-effectiveness of transistor integration into PV cells. However, as was explained earlier, combining fabrication steps can increase the cost-effectiveness of processing steps, which is also true for lithographic steps. For example, it is interesting to highlight the option of integrating transistors with lateral structures onto IBC solar cells. As this allows all contacts to be located on the backside of the PV cell, monolithic integration between the components and the cell contacts can be achieved. As was explained earlier, monolithic integration of power electronics can have a positive effect on the reliability of power converters.

Furthermore, it is worth mentioning that the worldwide market share of c-Si PV cell technology has shifted from predominantly multi-c-Si to mono-c-Si material, the latter now having an 84% market share of total c-Si production.[1] Since mono-c-Si is more suitable for the fabrication of high-quality semiconductor devices than multi-c-Si,[70] this recent market trend can make the integration of transistors into c-Si PV cells more viable. However, it must be noted that transistors should preferably be fabricated on flat wafer surfaces, instead of the pyramidal surface texture used in solar cells. Although the processing of industrial FBC cells typically starts with creating a double-sided texture on both sides of the wafer, for most cell types the rear side of the wafer is flattened by a subsequent etching step.[3] Since single-side wafer texturing does not prohibit subsequent photolithographic steps,[71] the texturing process does not prohibit transistor integration. Furthermore, in the case of IBC cell fabrication, the rear side of the wafer is often flat throughout the full process and the front side texturing takes place toward the end of the process.[71–73]

Another factor that must be considered is the compatibility in thermal budget between transistors and PV cells. In the case of solar cells, the thermal budgets vary for different cell designs.[3] However, there is only a limited thermal budget available for the fabrication of transistors.[74] Although combined designs could be achieved by performing part of the process flows consecutively instead of simultaneously, this approach poses a challenge to the cost-effectiveness. Thus, to be able to combine as much of the process flows as possible, similar thermal budgets for the different devices are beneficial. As such, depending on the transistor design, a low thermal budget silicon heterojunction process could be preferred over PV cell processes with higher thermal budgets.

Finally, in industry, transistors are typically fabricated into layers that are epitaxially grown on semiconductor substrates. By accurately controlling the desired doping profile through the growth of an epitaxial layer, the desired transistor properties can be achieved.[45] However, preceding the transistor integration by the growth of an epitaxial layer would pose a challenge to the cost-effectiveness and ease of integration.[75] Thus, it could be more favorable to integrate the device directly into the bulk of the c-Si solar cell wafer. On the other hand, this approach would leave less flexibility to control the doping profile of the substrate. The substrate doping concentration influences important properties of the transistors, such as the breakdown

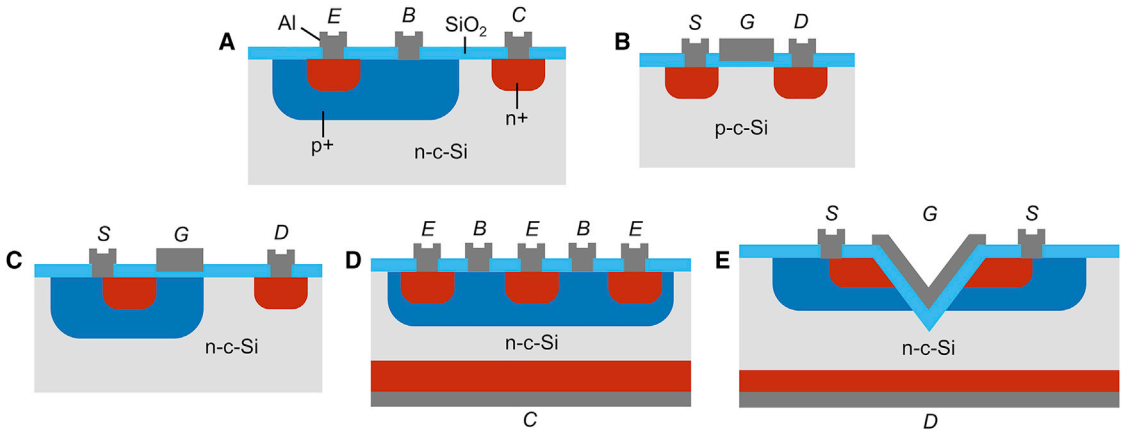

Figure 3. Basic transistor structures

(A) Bipolar junction transistor (BJT) structure. The emitter, base, and collector are represented by E, B, and C, respectively.

(B) Metal-oxide-semiconductor field-effect transistor (MOSFET) structure. The source, gate, and drain are represented by S, G, and D, respectively.

(C) Lateral double-diffused metal-oxide-semiconductor (LDMOS) structure.

(D) Power BJT structure.

(E) V-groove double-diffused metal-oxide-semiconductor (VDMOS) structure.

voltage.[52] Furthermore, the doping concentration across the wafer might be too heterogeneous for reproducible transistor fabrication. P-doped wafers have the advantage that boron or gallium doping is typically more homogeneously distributed across the wafer than phosphorus doping in n-type wafers.[5,76] Thus, the potential to leave out the epitaxial layer from the fabrication process might be higher for p-type than for n-type wafers.

When considering transistor integration into a c-Si solar cell, a wide range of devices can be considered. In this work, we will limit ourselves to the most used ones, which are bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). The insulated-gate bipolar transistor (IGBT) is out of the scope of this article, as this device would be relatively complex to integrate into a solar cell and is typically designed for a higher blocking voltage capability than what is necessary for sub-module PV applications. When comparing the BJT and MOSFET, the latter is usually the preferred type of device for high-frequency switching applications in the range from a few watts to a few kilowatts due to its fast switching characteristics.[77] On the other hand, both BJTs and MOSFETs are suitable to serve as switches in reconfigurable modules, where fast switching characteristics are less crucial.

When comparing the ease of integration of these two types of transistors into a c-Si solar cell, each has its advantages and drawbacks. In Figures 3A and 3B, the standard structures of the BJT and the MOSFET, respectively, are presented. For the BJT, a double-diffused structure is present beneath the emitter and the base contacts. Such a double-diffused structure is usually not present in c-Si solar cells, which implies that integration of a BJT into a solar cell would necessarily require additional processing steps to create this structure. On the other hand, the source and drain in the MOSFET structure as presented in Figure 3B can be fabricated in one single implantation step. As an implantation step with a similar dose and implantation energy is typically used to form the source and drain of a MOSFET and carrier-selective contacts of a solar cell,[45,72] this step can potentially be combined. However, the main challenge for the integration of a MOSFET into a solar cell is the fabrication

of the gate oxide, which has the purpose to isolate the substrate from the gate contact. To create the gate oxide, a high-quality SiO_2 layer up to a thickness of tens of nanometers is typically grown using thermal oxidation.[52] As such, integration of the MOSFET structure as presented in Figure 3B would require additional processing steps to fabricate a gate oxide.

A transistor must be designed such that it is capable of handling the desired voltage and current. To achieve the desired blocking voltage, the design considerations are similar to those of the diode. Thus, the substrate doping concentration can be lowered to prevent avalanche and Zener effects, while punch-through effects can be avoided by giving the depletion regions sufficient space to extend. In the BJT, this implies that the width of the base region needs to be sufficiently large. However, a relatively large base width is known to cause a smaller current gain, thus increasing the losses in the device.[52] In the MOSFET, a similar trade-off is present. The source-drain spacing needs to be increased to prevent punch-through effects,[47] but for the regular MOSFET design, this implies that the channel length increases. This is unfavorable, as the channel length should be as short as possible to minimize the on-resistance and to maximize the switching speed.[52,78] An additional downside of the regular MOSFET design is that the voltage at which avalanche breakdown effects occur is known to decrease if the gate overlaps with the drain region.[79] Thus, the MOSFET design from Figure 3B is generally not considered to be well suited for power applications.[80]

There exists an alternative lateral MOSFET design that is more suitable for power applications, often called the lateral double-diffused metal-oxide-semiconductor (LDMOS) transistor, as presented in Figure 3C.[81] It is worth noting that such lateral power MOSFETs are mainly used in power integrated circuits, but are rarely used as discrete devices.[47] In the LDMOS design in Figure 3C, the gate oxide no longer covers the full distance between the source and drain. This means that enlarging the source-drain spacing to prevent punch-through effects does no longer imply that the channel length increases as well. Thus, if blocking voltages are required where the standard MOSFET structure would need a relatively large channel length, the LDMOS structure can be used instead to achieve a smaller on-resistance and higher switching speed. Furthermore, in the LDMOS design, the gate plate does not overlap with the drain region, thereby mitigating the enhanced avalanche effect mentioned earlier.[79] Although the LDMOS design has some clear advantages over the regular MOSFET design for power applications, the ease of integration into a solar cell is challenging. The LDMOS design combines the difficulties that were mentioned earlier for integration of the BJT (double-diffused structures) and the MOSFET (gate oxide fabrication).

Neither of the previously mentioned lateral transistor structures is commonly used in industry for the fabrication of discrete power devices.[47] Examples of power transistors preferred in industry are presented in Figures 3D and 3E. Both these structures consist of vertical designs, which dominate the market of power transistors. The main motivation for use these vertical structures is that lateral structures for power devices typically take up more surface area of the silicon as the required blocking voltage capability increases. Since this is not the case for vertical designs, a higher packing density of transistors on a wafer can be achieved.[47] Furthermore, in vertical devices, the desired current carrying capability can be achieved by using a sufficiently large cross-sectional area of the wafer. As such, the cross-sectional area through which current is flowing through the device is maximized.[52] Although vertical structures are preferred in industry for the fabrication of power transistors, these structures

are less suitable for solar cell integration. Compared with the simpler structures from Figures 3A and 3B, numerous additional processing steps are required for the fabrication. Another drawback of these vertical transistor structures is that monolithic integration of these devices with other components in the IBC solar cell would be a challenge, as the contacts are located on opposite sides of the wafer. Integration of vertical power transistors into ICs is also known to be a challenge.[82] Furthermore, as was presented earlier in the section on diodes, the breakdown voltages of pn junctions in solar cells typically lie in the range between 10 and 25 V. If the bulk region of the PV wafer serves as the drift region, similar breakdown voltages can be expected for a vertically integrated MOSFET. As was the case for the integration of a vertical diode, the drift region would in this case be unnecessarily long with respect to these blocking voltages.

Having reviewed the design adaptations that are typically deployed in industry to make the transistors more suitable for power applications, we found that these adaptations are less favorable for transistor integration into a solar cell. Thus, it is worth considering what roles the standard designs from Figures 3A and 3B might play when they are integrated into a solar cell. If the device were directly integrated into the bulk of the wafer, the drain-source breakdown voltage that can be achieved would be similar to the case of the integrated diode (10–25 V). Assuming that the Voc value of typical c-Si solar cells lies in the range of 0.5–0.75 V, the most simple transistor structures from Figures 3A and 3B would be perfectly capable of blocking the voltage of a single cell or several series-connected cells.[83] Thus, these cell-integrated transistors are not limited by their blocking voltage capability to play a role in sub-module power conversion. However, the main challenge for the lateral MOSFET structures might be to design them such that they have sufficient current carrying capability. For solar cells that are typically used in industrial PV modules, the Impp typically lies in the range of 5–10 A at STC conditions.[53] To enable such current levels in the transistor structures from Figures 3A and 3B, the device width should be orders of magnitude higher than their counterparts used in integrated circuits. Designs with large widths are not straightforward to make, as the power dissipation in the metal fingers and interconnections become more dominant, also referred to as the scaling issue.[58] To this end, a similar design to the one that is used in the LDMOS design in Sun and Plummer[81] could be adapted to increase the current carrying capability. Here, several devices are effectively connected in parallel while sharing a common gate. Furthermore, an additional challenge for MOSFET structures with a large width is that the switching speed becomes lower due to the switching process not occurring uniformly over the whole device.[84]

Capacitors

A capacitor is a device that stores energy in the form of an electric field. It typically consists of two electrical conductors separated by a dielectric medium. For a parallel-plate capacitor, the capacitance is given by:

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \qquad \text{(Equation 1)}$$

where $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm is the permittivity of vacuum, ϵ_r (≥ 1) is the relative permittivity of the dielectric, A the area of the plates, and d the distance between the plates. To realize a high capacitance per unit area, the dielectric layer thickness d should be as small as possible. On the other hand, a minimum thickness d is necessary to avoid dielectric breakdown.[52] For example, a commonly used insulator such as thermally grown SiO_2 has a dielectric strength of 10 MV/cm.[45] Therefore, such a layer requires a thickness of at least 10 nm to prevent dielectric breakdown at a

voltage of 10 V between the plates. In the remainder of this section, several possibilities to integrate a capacitor in c-Si solar cells are explored.

First, we consider the possibility to exploit the capacitive behavior that solar cells naturally exhibit. As the capacitive behavior of c-Si solar cells originates in their pn junctions, it is worth reviewing the two main capacitive components of which any pn junction is constituted:

Junction capacitance

The junction capacitance is the capacitance that is associated with the ionized donor and acceptor atoms in a depletion region of a pn junction. The junction capacitance is influenced by the dopant concentrations and the applied voltage, since these factors influence the depletion region width and charge density. The junction capacitance can be expressed by the following equation if the abrupt junction approximation is applied:[52]

$$C_j = A\sqrt{\frac{q\epsilon_s N_a N_d}{2(V_{bi}+V_r)(N_a+N_d)}} \qquad \text{(Equation 2)}$$

where A is the cross-sectional area of the pn junction, q is the elementary charge constant, ε_s is the permittivity of the semiconductor, N_a and N_d the acceptor and donor concentrations, V_{bi} the built-in voltage, and V_r the applied reverse-bias voltage. As can be deduced from the equation, the main design parameters that can be varied to influence the junction capacitance are the doping concentrations and the cross-sectional area.

Diffusion capacitance

The diffusion capacitance is the capacitance that is associated with the diffusion of electrons toward the P region and holes toward the n region. The injection of these charge carriers across the depletion region leads to charge in the quasi-neutral regions. The diffusion current has an exponential dependence on the applied forward bias voltage. The diffusion capacitance can be expressed by the following equation if the abrupt junction approximation is applied and the assumptions $\omega\tau_{p0}<<1$ and $\omega\tau_{n0}<<1$ are valid:[52]

$$C_d = \frac{q^2 n_i^2 A}{2kT}\left(\frac{\sqrt{D_p\tau_{p0}}}{N_d}+\frac{\sqrt{D_n\tau_{n0}}}{N_a}\right)\exp\left(\frac{qV_a}{kT}\right) \qquad \text{(Equation 3)}$$

where ω is the radian frequency, n_i is the intrinsic carrier concentration, k is the Boltzmann constant, T is the temperature, D_p and D_n are the diffusion constants of holes and electrons, τ_{p0} and τ_{n0} are the minority charge carrier lifetimes, and V_a is the applied forward-bias voltage.

As can be deduced from Equations (2) and (3), the total capacitance exhibited by pn junctions is dominated by the junction capacitance at low applied forward bias voltages up to about 0.3 V.[85–88] At higher voltages, the total capacitance becomes dominated by the diffusion capacitance, which increases exponentially with voltage.[89] As the V_{mpp} of solar cells is typically higher than 0.3 V, the capacitance during normal operation is dominated by the diffusion capacitance.[90,91] It is worth noting that the cell temperature, as well as exposure to sunlight, can change the capacitance of a pn junction at a given operating voltage. In the short circuit condition, illumination is known to increase the capacitance, whereas the capacitance remains unaffected in the open circuit condition.[88] Taking the junction capacitance and the diffusion capacitance of c-Si solar cells into account, the two-diode

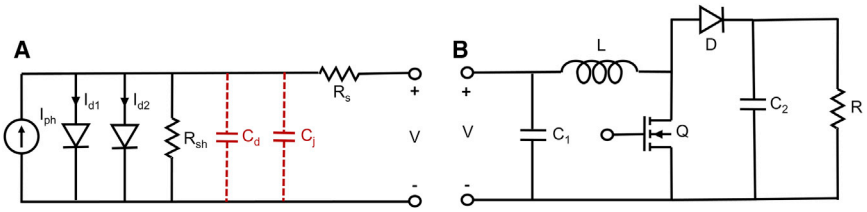

Figure 4. PV cell and DC-DC boost converter equivalent circuits

(A) Two-diode equivalent solar cell model expanded with the diffusion capacitance C_d and junction capacitance C_j (red).

(B) Example circuit of a DC-DC boost converter. The capacitors, inductor, MOSFET, diode, and resistor are represented by C, L, Q, D, and R, respectively.

equivalent model can be expanded with the self-capacitance, as presented in Figure 4A. It should be noted that the total capacitance of a string of series-connected cells scales inversely with the number of cells, which implies that the capacitive effects that can be observed at a module level are smaller than at cell level.

At present, in the research that has been done on the capacitance of solar cells, the capacitive effects were most often considered parasitic and unwanted. For example, the capacitance of c-Si solar cells is known to limit the minimal time required for J-V measurements.[92,93] Thus far, it appears that only in the work of Chang et al.[91] has a method been investigated to exploit the capacitive effects in solar cells. In this work, it was concluded that it can potentially become cost-effective to use the diffusion capacitance for power balancing among photovoltaic cells.

We propose another potential application for the self-capacitance of solar cells. In different types of power converters, such as the DC-DC boost converter shown in Figure 4B, an input capacitor C1 is used to reduce the ripple voltage at the input of the converter.[94] If such a converter were used in a PV module at cell or sub-module level, the self-capacitance of the solar cells could potentially fulfill the function of this input capacitor. The main advantage of exploiting the self-capacitance in this manner is that it removes the need to add a physical input capacitor to the power converter. However, a challenge to tackle would be that in this application the capacitance of the input capacitor depends on the operating conditions of the solar cell. Furthermore, it is important to comment on whether the self-capacitance of PV cells is large enough to fulfill the function of an input capacitor and keep the voltage ripple sufficiently low. When Equations 12 and 21 in Ayop and Tan[94] are combined, the minimum required input capacitance of a DC-DC boost converter for MPPT application can be approximated by:

$$C = \frac{I_{mpp}\gamma_{I_L}}{8V_{mpp}\gamma_{V_{mpp}}f} \qquad \text{(Equation 4)}$$

where I_{mpp} is the maximum power point current, γ_{IL} the inductor current ripple factor, V_{mpp} the maximum power point voltage, γ_{Vmpp} the maximum power point voltage ripple, and f the switching frequency. Thus, the exact capacitance that is required depends on the type and amount of PV cells (V_{mpp}, I_{mpp}). Besides, the switching speed of the transistors in the power converter is of crucial importance to the required input capacitance, since this determines the maximum operation frequency f. Furthermore, a design choice needs to be made for the maximum allowed voltage ripple, which is typically chosen below 1%.[94] If some typical numbers for cell-level power conversion are considered (γ_{IL} of 10%, γ_{Vmpp} of 1% an I_{mpp} of 6 A, a V_{mpp} of 0.625 V, and an f of 100 kHz), Equation (4) gives a required input capacitance of

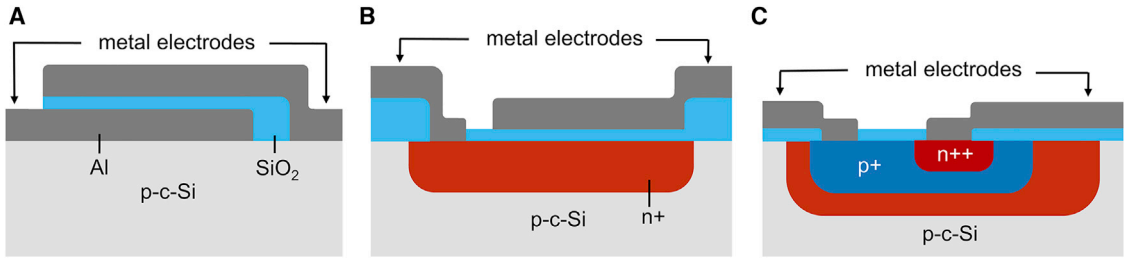

Figure 5. Basic thin-film capacitor structures

(A) Metal-insulator-metal (MIM) capacitor, where two metal layers are separated by a dielectric.

(B) Metal-oxide-semiconductor (MOS) capacitor, where a dielectric is separating a metal layer and a highly doped region.

(C) Pn junction capacitor structure, where the junction capacitance creates the capacitive effects.

120 μF. It is worth comparing this required capacitance with the values at which the self-capacitance of PV cells has been characterized in previous work. In the literature, capacitance densities between 0.1 and 2.3 μF/cm^2 were reported for c-Si cells operating at maximum power point.[86,90,91,95] Thus, the self-capacitance of industrial c-Si PV cells can be sufficiently large to fulfill the role of input capacitor at cell or submodule-level power conversion. However, it should be noted that, for operation at high frequency, the assumptions $\omega\tau_{p0}<<1$ and $\omega\tau_{n0}<<1$ may no longer be valid. Since in this case Equation (3) no longer accurately describes a pn junction, further research is required to understand whether the self-impedance of PV cells can still play a similar role in power converters at such high frequency.

Since the self-capacitance discussed earlier is a result of the physical processes taking place in solar cells, the capacitor cannot be connected in a place of choice. For example, it is unlikely that the self-capacitance can fulfill the function of C_2 in Figure 4B, as it is not naturally in the right place in the equivalent solar cell circuit. As such, it is worth considering a decoupled approach, where one or both of the electrodes of the PV-integrated capacitor are decoupled from the PV device.

First, we consider the integration of so-called thin-film capacitors, which are commonly used in integrated circuits. The most used types of these thin-film capacitors are the metal-insulator-metal (MIM) capacitor, the metal-oxide-semiconductor (MOS) capacitor, and the pn junction capacitor, all presented in Figure 5. When thin-film capacitor structures as in Figure 5 are integrated into c-Si PV cells, the surface area that the devices occupy competes with the area used for charge carrier collection in the PV cells. Thus, for the feasibility of this approach, a sufficiently high capacitance density must be achieved. However, it is worth noting that a high capacitance density is often counterbalanced by a low maximum voltage rating. This can be explained by the fact that dielectric breakdown occurs at a lower voltage as the dielectric layer gets thinner, as was explained earlier in this section. When reviewing the literature, it appears that reported densities of planar CMOS-compatible thin-film capacitors are currently lower than 1 μF/cm^2.[96] In Roberts at al.,[97] the development of a CMOS-compatible capacitor is reported with a capacitance density of 0.8 μF/cm^2 and a maximum voltage rating of 3 V. The highest capacitance densities are achieved for designs with advanced 3D structures, resulting in capacitance densities of 28 μF/cm^2 and 1.15 μF/cm^2 for MIM and pn junction capacitors, respectively.[98,99] However, the relatively complex fabrication steps required for the fabrication of such devices deteriorate the ease of integration into PV cells. Thus, a planar thin-film capacitor that is integrated into a PV cell is unlikely to exceed a capacitance density of 1 μF/cm^2. As explained earlier in this section, the input

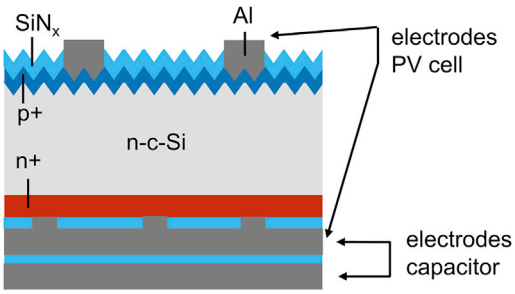

Figure 6. Three-electrode interconnection scheme, where the PV cell and capacitor share a common electrode

capacitor of a cell or sub-module-level DC-DC boost power converter typically requires a capacitance in the order of tens of microfarads. Although the required capacitance might differ for other applications and power converter configurations, it can be concluded that it is challenging to achieve PV-integrated thin-film capacitors with a high enough capacitance to be applied in PV power converters.

An alternative approach is presented in Berestok et al.,[100] where a photosupercapacitor is added to the back of a perovskite solar cell. Here, a three-electrode interconnection scheme is used and the PV cell and capacitor share a common electrode to realize a hybrid solar-storage device. In Figure 6, a similar structure is presented for a c-Si PV cell. The main advantage of this approach is that the capacitor does not compete with the PV cell area used for charge carrier collection. Since this allows for the integration of capacitors with a larger area, it becomes simpler to create integrated devices with sufficiently high capacitance. However, a drawback of this three-electrode interconnection approach is that the application is restricted to configurations where the capacitor is directly connected to the PV cell. As such, the flexibility to apply this capacitor integration method in different power converter topologies is limited.

Inductors

An inductor is a device that stores energy in the form of a magnetic field. Inductors are based on the principle of Lenz's law, which states that a change in current in all electrical conductors creates a magnetic flux that tends to cancel the change, an effect referred to as inductance.[101] To achieve a high inductance, most inductors consist of an electrical conductor that is wound around a ferromagnetic core. As such, inductors are often the bulkiest and most expensive components in power converters.[25–28] However, like all conductors, regular c-Si PV cells themselves exhibit inductive effects. To the best of our knowledge, Kumar et al.[86] is one of the few works (if not the only work) in which the inductance of a PV cell is characterized. Here, the inductance of a 2 × 4-cm c-Si PV cell was found to be 0.28 μH. Further research is required to explain how the area and cell design affect the self-inductance of PV cells. Nevertheless, to further explore the integration of inductors into PV cells, we can review related research from the fields of integrated circuits (ICs) and WPT.

In ICs, thin-film inductors are formed by creating spiral-like metallization patterns on top of silicon wafers.[45] It has been demonstrated experimentally that thin-film inductors can be used for DC-DC power conversion.[102–104] It is worth noting that screen printing, which is commonly used for the fabrication of solar cells, can be used as well to fabricate planar inductors.[105] Thin-film inductors can be fabricated in various layouts, such as square, hexagonal, circular, and octagonal patterns.[106] Although more background on analytical expressions for the self-inductances of these different spiral metal patterns can be found in Grover,[107] the dependence of the

inductance on the number of turns is usually quadratic.[108] The main drawback of increasing the number of turns on a given area is that this causes the series resistance of the conductor to increase as well. An important figure of merit for inductors that quantifies the trade-off between inductance and resistance is the quality factor $Q = \omega L/R$. It is worth noting that both the Q and the inductance density can be increased by enclosing the conductor with magnetic material.[109] On the other hand, magnetic materials bring along fundamental loss mechanisms, such as hysteresis and Eddy-currents.[110] The core losses become increasingly dominant for operation at higher frequencies,[111] and can have a significant effect on the watt-hour efficiency of DC-DC power converters.[112] Thus, air-core inductors are more suitable for very-high-frequency (VHF) applications (30–300 MHz).[113] Apart from the intended operating frequency, the optimal design of an inductor depends on the power level that the device should be able to support. Since the power levels in WPT are usually higher than those in ICs, the planar inductors in WPT applications typically require a higher Q and a lower parasitic resistance. As such, the planar coils reported in the field of WPT give a better indication of which inductances can be achieved on PV cells. In Li and Costinett,[114] a planar coil structure with an outer diameter of 10 cm for application in WPT was reported to exhibit a self-inductance of 3.13 μH and a Q of 185. In Low et al.,[115] a self-inductance of 12.52 μH and a Q of 63 were reported for a planar coil with an outer diameter of 13 cm. For diameters up to 20 cm, it has been demonstrated that inductance values from several tens of microhenries up to 80 μH can be achieved, corresponding to Q values between 50 and 120.[115–119] Such inductance values are in the same order of magnitude as inductors that are used in module-level power optimizers in PV applications. For example, the inductor of the module-level power optimizer in Chen at al.[120] has an inductance of 22 μH. It is worth mentioning that the inductance of several solar cells connected in series adds up. This means that the inductance of a string of cells can be increased in a relatively simple manner by increasing the number of series-connected cells. Thus, we can conclude that the area of c-Si PV cells is sufficiently large to facilitate the integration of planar inductors exhibiting inductance values and quality factors that are useful for power conversion and WPT. Moreover, when considering the performance at system level, it could also be a possibility to design the interconnections between cells such that the self-inductance is increased. However, it is out of the scope of this article to further describe this option. Next, we investigate how planar coils can be integrated onto c-Si PV cells.

First, we consider re-designing the metallization patterns that are already present in common PV cell designs. This approach offers ease of integration, since it might be realized without any additional fabrication steps compared with standard c-Si cell process flows. For FBC solar cell designs, there are metal front and back contacts present. Since the classic metal grid pattern on the front surface involves a careful optimization in the trade-off between resistive and shading losses,[5] there is little room to create spiral-like metallization patterns here. There might be more potential to create such patterns on the backside, where the absence of shading losses (at least in non-bifacial cells) gives more room to make alterations to the metallization pattern. On the backside of an FBC solar cell, the metal contacts with underlying point contacts can be re-designed into a spiral-like shape, as presented in Figure 7B. A similar approach could be used for IBC solar cells, as presented in Figure 7D. It is worth mentioning that the latter solution only shows a possible geometrical re-design option for the IBC fingers and metal contacts. However, the interaction between the two coils must be properly studied to verify whether this topology can be effectively used as an integrated inductor within a power converter. The two-diode equivalent circuit of a solar cell with increased self-inductance is presented in Figure 7E.

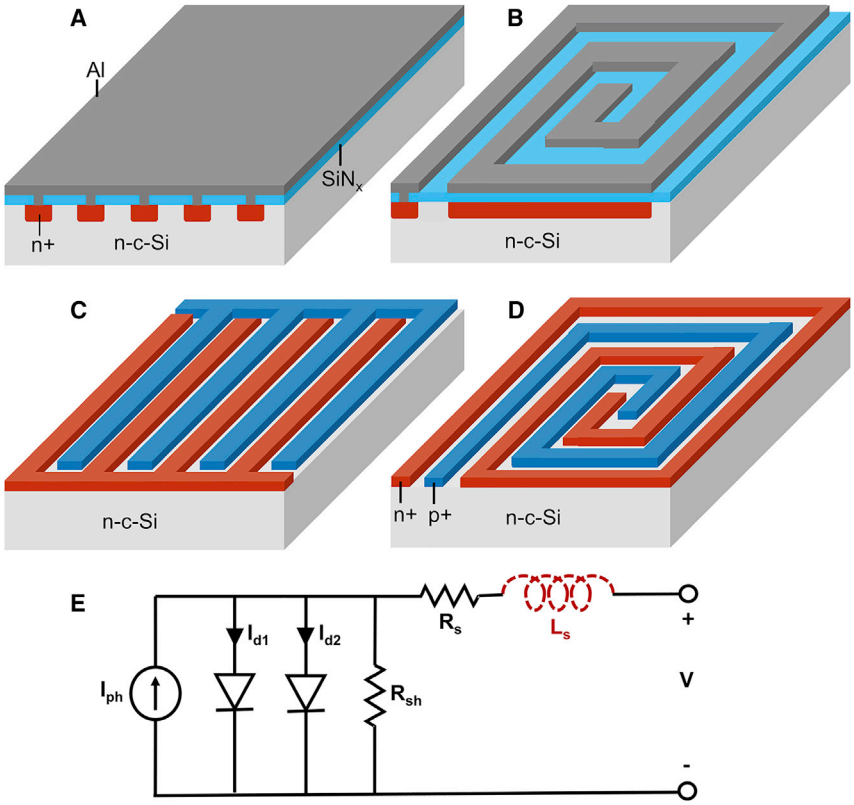

Figure 7. Enhancing PV self-inductance by re-designing metal contacts into spiral-like patterns

(A) Rear side of an FBC cell structure with point contacts.

(B) Possible re-design of the FBC cell structure, aimed at an increased self-inductance.

(C) Rear side of an IBC solar cell structure, where highly doped layers are used for collection of charge carriers. In an IBC cell, metal contacts are placed on top of these doped layers.

(D) Possible re-design of the IBC cell structure, aimed at an increased self-inductance.

(E) Two-diode equivalent solar cell model expanded with self-inductance (red).

It should be taken into consideration that the analytical formulas developed for inductors are not directly applicable for this solar-cell-integrated approach, as the current through the metal layer will increase toward the outer side of the spiral. Thus, quantifying the exact inductances that the proposed structures will exhibit requires further research. Furthermore, these spiral-like metallization patterns on the back of solar cells will affect the series resistance and thus the fill factor with respect to standard c-Si solar cell designs. Future research will need to verify whether it is possible to create a c-Si solar cell with a good fill factor and a high self-inductance at the same time. Finally, it is worth noting that the addition of a magnetic material can also be considered to increase the self-inductance without increasing the number of turns. The deposition of magnetic material on one side of the inductor can increase the inductance up to 100%.[121] However, including such magnetic materials would increase fabrication costs and require additional processing steps using materials that have not been studied in combination with solar cells, such as Ni-Fe, Co-Zr-Ta, and Fe-Al-O.[122,123]

Furthermore, it is worth considering a decoupled approach, where the inductor is separated from the charge carrier collection layers by an insulator, as presented in Figure 8. This method offers more flexibility in the inductor design, as it allows the charge carrier collection layers and the planar coil to be optimized separately. Thus, the process of increasing the self-inductance without causing too large a

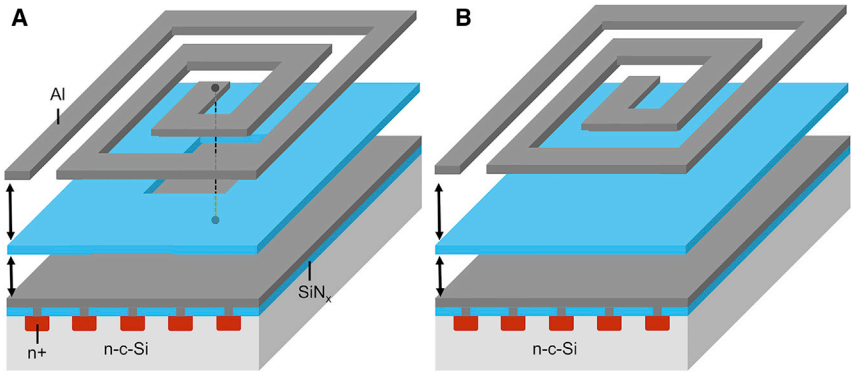

Figure 8. Decoupled inductor integration, where a planar inductor is spatially separated from the PV cell by an insulating layer

(A) The inductor is electrically connected to one of the PV cell contacts but spatially separated from the PV cell by an insulating layer.

(B) In the decoupled approach, the design can be adapted in a relatively simple way to create a four-terminal configuration.

loss in fill factor is simplified. Furthermore, the decoupled approach allows configurations where the cell is transformed into a four-terminal device. As such, it would enable integrated designs where the inductor is not directly connected to the PV generator, such as the buck converter. A final advantage of this approach is the reduced probability that the addition of magnetic materials will affect the solar cell, as it is separated by an insulating layer. The structure would also allow for designs where the magnetic material is present on both sides of the inductor, also known as the sandwich structure.[124] However, the decoupled approach will require additional processing steps compared with regular PV cell fabrication processes. Every step from the deposition of the insulating layer onwards needs to be performed specifically to create the inductor. Thus, it would be more challenging to achieve cost-effective designs for this decoupled approach.

Combining the different solutions

Although integration of each power electronic component was treated separately in the previous sections, the main potential lies in combining the different approaches. For example, the integration of power transistors and the exploitation of PV self-capacitance and self-inductance were discussed in the previous sections. For successful implementation of these three concepts into one PV cell, the equivalent circuit of the cell can be expanded as in Figure 9.

If we refer to back to the equivalent circuit of a DC-DC boost converter from Figure 4B, a large part of the boost converter would already naturally be included in the solar cell. Solar cell integration of a DC-DC boost converter is particularly promising because the self-capacitance and self-inductance of the solar cell are naturally complementary to the boost converter topology. Nevertheless, when power electronics can be successfully integrated into solar cells, numerous new topologies for power converters and reconfigurable modules will become possible.

CHALLENGES

In the previous section about feasibility, the importance of ease of integration has already been stressed. Moreover, several specific challenges of the different power electronic components were treated. In this section, we describe some more general

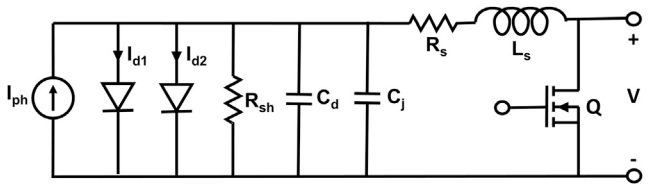

Figure 9. Equivalent circuit of a solar cell, expanded with the self-capacitance, self-inductance, and an integrated MOSFET

challenges related to successful integration of power electronic components into c-Si PV cells.

Thermal management

Thermal management will be a challenge for successful integration of power electronics, as power dissipation due to the parasitic resistance of the devices might cause the PV cells to heat up. It is well known that the efficiency of solar cells decreases with increasing temperatures. This is caused by the diminishing of the Voc and FF, even though the Jsc increases slightly.[125,126] Non-uniformities in the temperature distribution across a cell lead to further losses. For instance, in Zhai et al.,[127] it was shown that non-uniformities in the temperature distribution of a solar cell are amplified during exposure to sunlight. In the case of 1,000 W/m^2, a specific pre-heated part of the cell heats up 14.2% faster than the surrounding cell area. As such, an initial temperature mismatch of 5.9 K leads to an 8.6% reduction in Isc and a 10.8% reduction in Voc compared with a uniformly illuminated device. Thus, especially in the case of integrated power electronic components that only occupy part of the wafer surface, the heat dissipation in the devices must be limited by ensuring that the parasitic resistance of the integrated power electronics is sufficiently low. For successful industry adoption, additional measures might be required to improve thermal management, either at cell or module level.

Opto-electrical challenges

Moreover, there are opto-electrical challenges involved in successful integration of power electronics into the bulk of c-Si solar cells. For discrete semiconductor power devices from industry, packaging protects the silicon from sunlight and other external influences. However, in the integrated approach, the power electronics and solar cell share a common bulk. First, this means that the integrated power electronics will be exposed to photogenerated charge carriers that are generated in the bulk of the wafer. In the case of a diode or a pn junction capacitor, it is possible that the device would start acting like a solar cell itself, which means an undesired current would be generated from inside the device. There might be differences between pn junction diodes and Schottky barrier diodes in how sensitive the devices are to such an effect. However, the previous studies about integrated bypass diodes into solar cells did not report any effect of photogenerated carriers, which can presumably be explained by the effect being minor due to the small area of the device on the wafer. In the case of transistors, the photogenerated charge carriers could pose a challenge to their performance and controllability. Here, there might be differences between current-controlled transistors (BJT) and voltage-controlled transistors (MOSFET) in their sensitivity to such an effect. Furthermore, electrical interactions in the bulk of the wafer could lead to undesired effects. For example, the potential differences that are generated during PV operations might affect the operation of integrated transistors. It is worth mentioning that there have been reports of transistors and PV cells sharing a common bulk.[128–132] These reports describe low-power chips

(microwatts to milliwatts) that are self-powered by an on-chip PV cell. Although this application differs from this manuscript and concerns lower power levels, the reports do demonstrate the technical feasibility of transistors and PV cells sharing a common bulk. However, further research is required on the opto-electrical challenges related to device integration into PV cells to fully understand and properly describe them. If these challenges turn out to be too detrimental, alternative integration approaches can be considered. For example, the power electronics can be separated from the bulk of the PV wafer by an insulating layer. Nonetheless, such an approach would require additional processing steps.

Repairability and long-term reliability

When a failure occurs in a single PV component nowadays, the complete module is often decommissioned and directed toward disposal.[133] Nevertheless, interest in on- or off-site repairability has been increasing. For example, it has been reported that special PV module designs with higher repairability can become cost-effective.[134] However, the integration of power electronics into solar cells poses a challenge to the repairability when a single component fails. In such cases, the only possibility would be to replace the complete cell with a new one. It is worth mentioning that there are developments toward PV modules in which the cells are not laminated,[135] making it more feasible to replace individual cells in the module.

For successful industry adoption, it is thus important that the lifespan of the integrated power electronics is similar to that of PV modules. Typical lifetimes of PV systems are in the range of 25 years. However, most system-level inverters come only with a 10-year warranty, which means that owners of PV installations should account for a replacement of the inverter during the lifetime of the PV system. Nevertheless, manufacturers of module-level converters typically provide higher warranties of 25 years. Taking these typical PV module and power converter lifespans into account, the analysis in Olalla et al.[10] shows that adding sub-module-level power electronics can improve the lifetime of PV systems by 5–10 years. Furthermore, as explained earlier, monolithically integrated components into PV cells hold the promise of higher reliability, potentially increasing the converter lifetime further.

DISCUSSION

In this article, we explored the possibility to integrate power electronics into c-Si PV cells. This approach has the potential to (partly) replace module-level power electronics and enable highly granular sub-module-level power optimization for higher energy yield. Furthermore, cell-integrated power electronics might simplify designs of autonomous devices powered by PV cells. Eventually, cell-integrated power electronics could even facilitate innovative PV module designs that are capable of wireless power transmission.

The feasibility of integrating various designs of diodes, transistors, capacitors, and inductors into c-Si solar cells was discussed. First of all, diodes exhibit high ease of integration into PV cells, and successfully integrated designs have already been demonstrated. On the other hand, the integration of transistors is more complex. Since transistor fabrication processes require lithographic steps, it is necessary for cost-effective integration to combine as many processing steps as possible with PV fabrication. It was found that there is limited flexibility to combine processing steps of standard vertical power transistor designs with PV fabrication. As such, possibilities were suggested to combine certain aspects of small-signal and power transistors to end up with transistor designs that have appropriate properties and could

be integrated in a relatively simple way. Regarding passive component integration, several promising approaches were found. For instance, the pn junction capacitance density of PV cells during operation at maximum power point can be as high as 2.3 $\mu F/cm^2$, which is sufficiently large for deployment in power converters for PV applications. On the other hand, for thin-film capacitor integration, it is challenging to achieve a sufficiently high capacitance. For this approach, the capacitor area competes with the cell area that is used for charge carrier collection, and reported capacitance densities are typically lower than 1 $\mu F/cm^2$. Thus, to achieve the desired capacitance with an integrated capacitor, a more promising configuration is a three-electrode interconnection scheme on the backside of an FBC cell. However, this approach has thus far only been used to realize a hybrid solar-storage device and allows for limited flexibility to be applied in different power converter topologies. Finally, regarding the integration of inductors, it was concluded that the area of PV cells is sufficiently large to facilitate the integration of planar coils exhibiting inductance values that are useful for power conversion. In WPT applications, planar coil inductances of 3–80 μH have been demonstrated on areas similar to those of industrial PV cells. Thus, several design options were proposed to integrate spiral-like metallization patterns and planar coils on the backside of FBC and IBC PV cells.

Generally, it is a challenge to realize integrated power electronics designs that have high ease of integration and are at the same time competitive with discrete power devices that can be bought on the market. Future research will prove whether the trade-offs that need to be overcome can be adequately handled. Finally, general challenges that should be considered for successful integration of power electronics are appropriate thermal management, opto-electric behavior under illumination, and repairability.

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AUTHOR CONTRIBUTIONS

Conceptualization, P.M. and O.I.; investigation, D.N. and P.M.; writing – original draft, D.N. and P.M.; writing – review & editing, D.N., P.M., M.Z., and O.I.; visualization, D.N.; supervision, P.M. and O.I.; project administration, P.M., M.Z., and O.I.

DECLARATION OF INTERESTS

The authors have submitted a patent application entitled *Integration of Inductors on Silicon-based Solar Cells*.

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