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An Effective dq-based Control Technique for a Grid-Connected Single-Phase PUC5 Inverter

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***Abstract*— This paper presents a simple yet robust dq-frame current control strategy for a single-phase 5-level Packed U-Cell (PUC5) inverter, targeting efficient and reliable integration of renewable energy (RE) sources into the grid. The proposed approach exploits the inherent self-balancing characteristics of the PUC5 topology, thereby eliminating the need for capacitor voltage sensors or active balancing circuits. This leads to a simplified hardware structure and reduced overall system complexity and cost. A conventional PI-based dq controller is employed to regulate the injected grid current, ensuring decoupled control of active and reactive powers. Extensive simulations in MATLAB/Simulink demonstrate that the system maintains a unity power factor and achieves low total harmonic distortion (THD) using a basic L-type filter. Moreover, one of the key outcomes is the natural and stable self-balancing of the flying capacitor voltage, which consistently maintains its voltage around half the DC link voltage with low ripples, even under dynamic changes in current reference and DC input voltage. These results confirm the PUC5-controller solution's reliability and suitability (compelling alternative to more complex multilevel converter architectures) for grid-connected applications.**

***Keywords*—Multilevel Inverter, Packed U-Cell, dq Control, PUC5, Grid-Connection.**

I. Introduction and Literature Review

Conventional 2-level inverters often suffer from high output harmonic content, necessitating large and costly passive filters to meet grid code requirements [1]. To address these limitations, multilevel inverters (MLIs) have gained interest as a key solution for enhancing both power quality and conversion efficiency in DC-AC systems [2]. By generating multilevel output voltages, MLIs produce waveforms with significantly reduced total harmonic distortion (THD). This improvement not only reduces filter size but also contributes to lower electromagnetic interference and overall system cost [3]. Motivated by these advantages, considerable research has focused on developing advanced MLI topologies that maximize the number of voltage levels while minimizing the number of power components and isolated sources. This interest has led to the development of various topologies such as cascaded H-bridge (CHB) inverters, flying capacitors inverters (FCIs), and neutral-point clamped (NPC) inverters [4]–[5]. Recently, Packed U-Cell (PUC) topology has emerged as a promising alternative, offering a reduced component count and simplified structure, particularly attractive for medium-power applications [6]. The PUC inverter produces a multi-level AC output voltage while using only a single DC source and a reduced number of passive/active components in comparison to traditional MLI topologies [7]-[9]. However, replacing DC sources with floating capacitors introduces the challenge of maintaining stable capacitor voltage levels. These capacitors must be actively balanced to ensure correct output voltage generation and waveform symmetry [10]. Achieving this balance often requires extra voltage sensors or sophisticated control techniques, which can undermine the PUC topology's key advantage of hardware simplicity.

In the 5-level Packed U-Cell (PUC5) inverter, five distinct output voltage levels ($\pm V$dc, $\pm V$dc/2, and 0) are achieved using only a single DC source and one floating capacitor. A key advantage of the PUC5 topology is its ability to utilize redundant switching states to passively regulate the capacitor voltage, thereby eliminating the need for multiple isolated DC supplies [11]. Compared to other 5-level inverters, the PUC5 design significantly reduces the number of power switches and omits the use of transformers, resulting in a more compact, lightweight, and efficient system architecture [12].

In [10], a sensorless capacitor voltage balancing method was introduced, where carefully selected PWM switching states automatically regulate the flying capacitor voltage around the desired value (half of the DC-link voltage level) without the need for direct voltage measurement. This approach not only preserves the symmetric structure of the output waveform but also simplifies the control implementation. By keeping the capacitor voltage stable, even under dynamic operating conditions, this self-balancing method reduces control overhead and enhances reliability, particularly in grid-connected applications. Such features make the PUC5 inverter highly attractive for practical applications, as it shifts the control focus toward optimizing output current quality without additional sensing or complex balancing algorithms.

Maintaining a stable capacitor voltage while ensuring high-quality current injection has motivated the development of various control strategies for PUC5 inverters. A commonly adopted approach relies on proportional–integral (PI) controllers [13]. While PI control remains a popular and well-established method due to its simplicity and ease of implementation, it often requires meticulous gain tuning and the addition of auxiliary control loops to simultaneously manage the dual objective of current regulation and capacitor voltage stabilization inherent to the PUC5 topology.

Thus, researchers have investigated modern state-space and nonlinear controllers. Linear Quadratic Regulator (LQR) based designs use full-state feedback to optimally regulate the grid current while inherently accounting for the capacitor voltage dynamics. In [14], authors have modelled the single-

phase PUC5 in the dq-frame and designed an LQR with integral action (LQRI) for a grid-tied PUC5 with LCL filter, integrating the sensor-less capacitor control into the modulation process. This approach actively damps the filter resonance and maintains the five-level waveform without needing direct capacitor voltage feedback. Model Predictive Control (MPC) has also been applied to PUC5 systems [15]. In MPC, the strategy depends on fast microprocessors to determine optimal switching actions in real time. MPC has been shown to perform better than classical PI in dynamic tracking and THD reduction [16]. It can also handle multi-variable constraints, such as limiting capacitor voltage deviation and current overshoot. Sliding Mode Control (SMC) techniques have further been investigated to enhance robustness [17]. To simply stabilize the capacitor voltage, the authors in [18] used a low-complexity carrier-based modulation to implement a super-twisting SMC on a sensor-less PUC5. The SMC produced high power quality along with rapid self-balancing of the capacitor even when the system experienced dynamic changes in load or disturbances during stand-alone operation, and their results demonstrated enhanced reference tracking accuracy and disturbance rejection. Fuzzy logic controllers have also been proposed by researchers to manage parametric uncertainties and nonlinearity in PUC5 inverters [19]. Despite fluctuations in the grid or load, a reliable fuzzy-based controller can adjust the inverter's duty cycle in real-time based on error rule evaluation, achieving low THD in the injected current and near-unity power factor [20]. As they offer adaptability without necessitating a precise system model, these intelligent controllers are attractive in renewable energy scenarios with variable operating conditions.

Despite these control techniques' advancements explored in the literature, a notable gap exists. For instance, a proportional-resonant (PR) controller for a grid-connected PUC5 inverter was proposed in [21], which provided satisfactory tracking at the fundamental frequency but lacked robustness under harmonic disturbances and did not address voltage balancing or high-order harmonic suppression in detail. A fixed switching frequency model predictive controller (MPC) was developed in [22], avoiding voltage sensors to reduce cost, but requiring heavy computation and accurate system modeling. Similarly, [23] proposed an ANN-based control strategy for a modified PUC5 inverter, achieving impressive current tracking performance and low total harmonic distortion (THD). However, the approach required an elaborate training process and introduced considerable implementation complexity, potentially limiting its practicality for real-time applications. A voltage-sensorless first-order sliding mode controller was presented in [24], demonstrating rapid self-balancing and strong robustness with minimal sensing requirements. However, the method exhibited control chattering. Most existing studies either introduce auxiliary control loops to regulate the capacitor voltage or rely on computationally intensive algorithms, such as MPC or observer-based methods, to manage the internal voltage dynamics of the PUC5 inverter. Few investigations have focused on leveraging the inherent self-balancing characteristics of the topology through a simple synchronous dq-frame current control—specifically, a grid-following PI-based regulator capable of maintaining stable capacitor voltage without the need for complex estimators or additional sensing hardware. To the best of the authors' knowledge, no prior work has addressed the grid integration of a single-phase PUC5 inverter using only a conventional dq control scheme with minimal sensor requirements. This paper aims to fill this gap by presenting a streamlined yet effective dq-frame control approach that benefits from the PUC5's natural balancing behavior, enabling reliable power injection with reduced implementation complexity.

II. System Description and Mathematical Modeling

The five-level PUC5 inverter under study (Fig. 1) is a single-phase multilevel converter that utilizes a single DC source, six power semiconductor switches, and one flying capacitor to produce five distinct output voltage levels ($\pm V$dc, $\pm V$dc/2, and 0) provided that the voltage across the flying capacitor is maintained at half of the input DC voltage (Vdc/2). The different switching states (including the redundant states) and the corresponding output voltage levels are compiled in Table I.

For instance, To generate an output voltage of Vdc/2, the PUC5 inverter can employ two distinct switching configurations: one that connects the flying capacitor in series with the lower half-bridge leg—resulting in a charging operation—and another that routes the connection through the upper leg, leading to the capacitor discharge. Although both switching states yield the same output voltage level, they exert opposing impacts on the capacitor's voltage. The modulation strategy of the PUC5 topology exploits this redundancy to achieve passive voltage balancing, allowing the flying capacitor to self-regulate around its reference value of Vdc/2 without the need for direct voltage sensing or feedback control. Maintaining the capacitor voltage near this nominal midpoint ensures that the five-level output waveform remains uniformly symmetric, thereby reducing low-frequency harmonic distortion and enhancing output power quality.

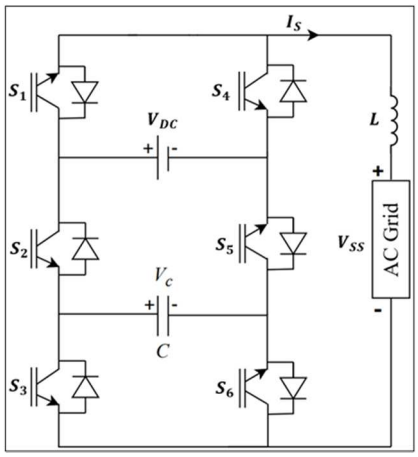

Fig. 1. PUC5 inverter [19]

TABLE I ALL POSSIBLE SWITCHING STATES OF PUC5 INVERTER

States	S1	S2	S3	S4	S5	S6	Output Voltage
1	1	0	0	0	1	1	$+V_{DC}$
2	1	0	1	0	0	0	$+0.5V_{DC}$
3	1	1	0	0	1	1	$+0.5V_{DC}$
4	1	1	1	0	0	0	0
5	0	0	0	1	1	1	0
6	0	0	1	1	0	0	$-0.5V_{DC}$
7	0	1	0	1	1	1	$-0.5V_{DC}$
8	0	1	1	1	0	0	$-V_{DC}$

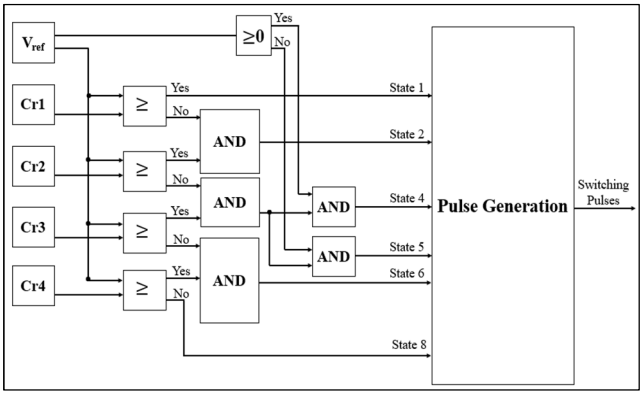

Fig. 2. PWM-based switching control unit for PUC5 inverter

In this paper, a multicarrier pulse-width modulation (PWM) scheme is employed. This method utilizes four high-frequency triangular carrier signals (Cr1–Cr4), each corresponding to one of the four voltage intervals that collectively define the five discrete output levels, as illustrated in Fig. 2. A single sinusoidal reference signal V_{ref}, representing the control target, is continuously compared against the carrier waveforms to determine the appropriate switching state at each instant. This modulation strategy ensures accurate and continuous generation of the multilevel output waveform, enabling smooth transitions between voltage levels and contributing to enhanced harmonic performance and dynamic behavior. The modulation reference V_{ref} is a normalized control voltage signal derived from the dq-frame current controller, and it typically follows a sinusoidal trajectory at the fundamental frequency of the grid (60 Hz). The gating logic incorporates an additional layer of control to select between redundant switching states for the intermediate voltage levels (Vdc/2 and -Vdc/2) based on the real-time condition of the flying capacitor voltage. When the capacitor voltage deviates from its nominal value (e.g., 100 V for a 200 DC-link voltage), the control algorithm alternates between charging and discharging states on a half-cycle basis to restore balance, effectively serving as an embedded voltage regulation mechanism without the need for explicit sensing or control loops. The PWM switching frequency is set to 2 kHz, which provides a suitable compromise between switching losses and waveform quality. To further reduce high-frequency ripples, a 3 mH filter inductor is employed. In conjunction with the grid or load impedance, this filter attenuates switching harmonics, ensuring that the inverter delivers a smooth and low-distortion AC output current.

The proposed control strategy is based on a single-phase synchronous reference frame (dq) current control scheme, designed to regulate the power injected into the grid. The overall control structure is illustrated in Fig. 3. A phase-locked loop (PLL) is used to synchronize with the grid voltage v_{ss}. The PLL generates reference signals sin(ωt) and cos(ωt), which define the rotating reference frame aligned with the grid voltage vector. By convention, the grid voltage is aligned with the d-axis, such that under ideal unity power factor conditions, the entire current component is concentrated along the d-axis, while the q-axis component remains zero.

The grid current is sampled and projected onto the synchronous rotating frame using the Park transformation. This yields the direct-axis (id) and quadrature-axis (iq) components of the current, representing the active and reactive current contributions, respectively. For implementation in single-phase systems, the transformation leverages a 90° phase-shifted version of the current signal, denoted $i_s\angle 90°$, to compute the orthogonal components as follows:

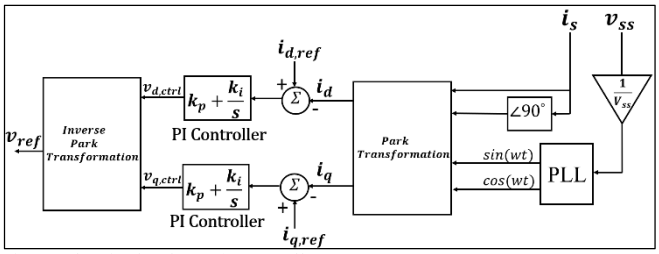

Fig. 3. The single-phase *dq* controller

$$i_d(t) = i_s * sin(\omega t) - i_s\angle 90° * cos(\omega t) \quad (1)$$

$$i_q(t) = i_s * cos(\omega t) + i_s\angle 90° * sin(\omega t) \quad (2)$$

Under ideal unity power factor conditions, i_d carries the full current magnitude and $i_q \approx 0$. The controller consists of two PI regulators: one for i_d and one for i_q. The reference for the direct current component $i_{d,ref}$ is set based on the desired active power injection. In the simulation, $i_{d,ref}$ is adjusted to deliver approximately 400 W of active power to the grid, this corresponds to an $i_{d,ref}$ equal to 5 A. The quadrature current reference $i_{q,ref}$ is set to 0 to deliver zero reactive power. The measured i_d is compared with $i_{d,ref}$, and the error is fed into the d-axis PI controller, which outputs a control voltage $v_{d,ctrl}$. Similarly, any small error in i_q (with $i_{q,ref}$=0) is corrected by the q-axis PI, yielding $v_{q,ctrl}$.

$$v_{d,ctrl} = k_p(i_{d,ref} - i_d) + k_i \int (i_{d,ref} - i_d)dt \quad (3)$$

$$v_{q,ctrl} = k_p(i_{q,ref} - i_q) + k_i \int (i_{q,ref} - i_q)dt \quad (4)$$

These controller outputs represent the voltage components (in the *d–q* frame) that the inverter should generate across the filter inductor to drive the current errors toward zero. The values of the proportional gain (k_p) and integral gain (k_i) were set to be 1 and 100, respectively.

Finally, the *d–q* control voltages are transformed back to the stationary frame to form the reference signal Vref for the modulation scheme. The inverse transform is given by:

$$v_{ref} = v_{d,ctrl} * sin(\omega t) + v_{q,ctrl} * cos(\omega t) \quad (5)$$

The computed control voltage V_{ref} is continuously updated to ensure that the inverter output current accurately tracks its reference. Through this approach, the control system achieves decoupled regulation of the active and reactive current components, thereby enforcing unity power factor operation. As a result, all the injected current contributes to active power transfer, with minimal reactive content. The complete set of parameters used in the simulation model is provided in Table II.

TABLE II. SYSTEM PARAMETERS

Parameter	Value (Unit)
DC Source, V_{DC}	200 V
Capacitor, C	2000 µF
Capacitor's Voltage, V_C	100 V

Grid Voltage,V_{SS}	170 V_P (120 V_{RMS})
Grid Current, I_s	5 A_P
Grid Frequency f_{grid}	60 Hz
Switching Frequency, f_{SW}	2000 Hz
Filter Inductance, L	5 mH

III. SIMULATION RESULTS

The proposed control strategy was implemented and validated using MATLAB/Simulink. Fig. 4 presents the realization of the PWM scheme employed to synthesize the inverter output voltage. The control reference waveform vref, a sinusoidal signal derived from the dq controller, is superimposed on four high-frequency triangular carrier signals, labeled Cr1 through Cr4. The modulation scheme effectively drives the inverter switches to generate symmetrical, low-distortion waveforms with precise transitions between the five voltage states. This contributes to enhanced output quality and reduced total harmonic distortion in the delivered AC signal.

Fig. 5 displays the output voltage waveform of the PUC5 inverter under steady-state operating conditions. All five voltage levels ($\pm V$dc , $\pm V$dc/2, and 0) are distinctly shown, confirming the proper operation of the multilevel modulation and switching scheme. The symmetry of the voltage steps around the zero axis indicates that the flying capacitor voltage is effectively regulated, maintaining balance without external sensing or control intervention. This 5-level waveform significantly improves output quality by reducing total harmonic distortion (THD), which in turn alleviates the need for bulky filters. As a result, the PUC5 inverter presents an efficient and compact solution for grid-connected applications where waveform precision and compliance with harmonic standards are critical.

Fig. 6 illustrates the synchronization of the grid voltage and inverter output current waveforms. The orange trace corresponds to the grid voltage, maintained at approximately 170 V peak (120 V RMS), while the blue one shows the output current (scaled by a factor of 10 for visualization purposes). The phase alignment between voltage and current confirms unity power factor operation, indicating that the inverter delivers purely active power to the grid. The current waveform is smooth and sinusoidal, with only minor high-frequency ripple attributed to the 2 kHz switching frequency and the discrete nature of the five-level output voltage. The series inductor effectively attenuates these switching-induced ripples, preserving waveform quality. This is further validated in Fig. 7, where the Fast Fourier Transform (FFT) analysis reveals a low THD of approximately 4.59% when the grid current is 5 A. The THD is calculated using the following equation 5, where I_1 is the RMS value of the fundamental current, and I_n is the RMS value of the n^{th} order harmonic.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} * 100\% \quad (6)$$

Fig. 8 presents the steady-state performance of the inverter's output power after synchronization with the grid has been established. The active power (P), represented by the orange curve, remains consistently around 420 W, which closely aligns with the intended power injection target. Simultaneously, the reactive power (Q), shown in blue, remains effectively at 0 VAR. This indicates that the dq-frame controller successfully regulates the i_d and i_q current components to achieve the desired power delivery with high accuracy. The steady zero reactive power confirms unity power factor operation, while the stable active power output reflects the controller's ability to maintain reliable power injection under steady-state conditions.

As shown in Fig. 9, the capacitor voltage remains consistently centered around 100 V, which corresponds to the expected value of half the 200 V DC-link voltage. The voltage ripple is kept within ±1 V—representing less than 2% deviation from the nominal setpoint—which indicates excellent voltage stability.

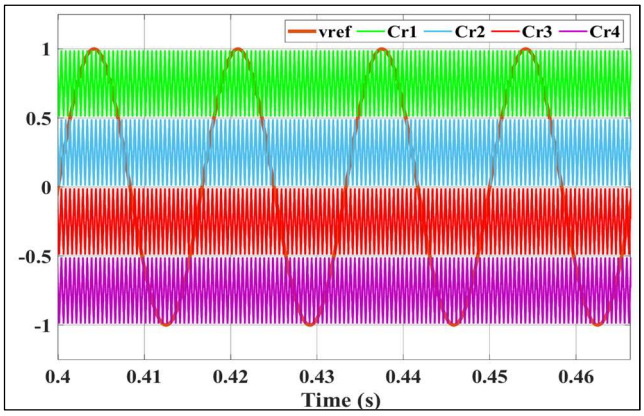

Fig. 4. Reference and carrier signals used in the five-level PWM scheme

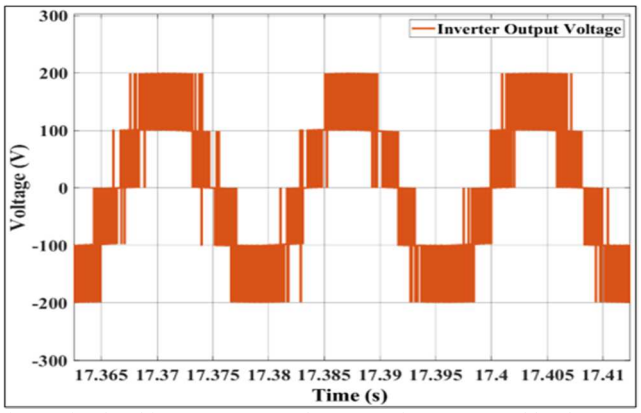

Fig. 5. Five-level inverter output voltage waveform generated by the PUC5 topology

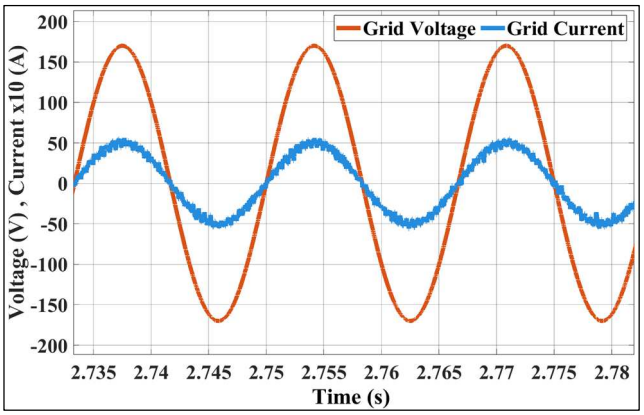

Fig. 6. Grid voltage and scaled grid current waveforms during steady-state operation

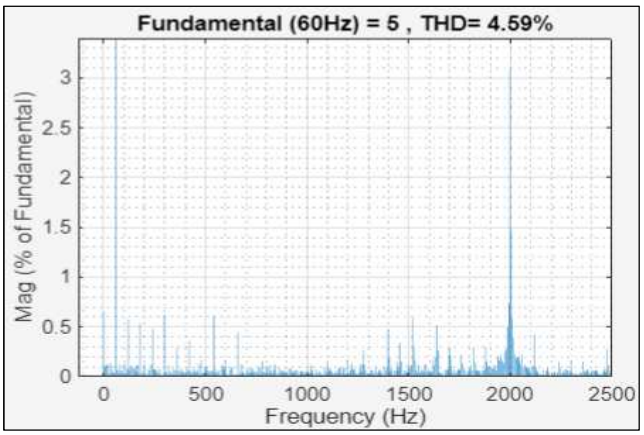

Fig. 7. Fast Fourier Transform (FFT) of the grid current waveform showing the THD to be 4.59% at grid current of 5 A

This minimal ripple confirms the effectiveness of the switching strategy in maintaining charge balance and highlights the robustness of the PUC5 topology's inherent self-balancing mechanism. Notably, this voltage regulation is achieved without the aid of external sensors or active balancing circuits, validating the feasibility of sensorless operation in grid-connected scenarios.

To assess the robustness of the proposed control strategy, Fig. 10 presents the inverter's dynamic response to step changes in the current reference, simulating ±50% deviations from the nominal load condition. In each case, the actual current tracks the reference accurately, with negligible delay, overshoot, or oscillation. The system exhibits fast settling and maintains stability throughout the transitions, highlighting the effectiveness of the PI-based dq control in regulating the output current across a wide range of operating conditions. These results confirm the controller's capability to handle rapid load fluctuations, making it well-suited for real-time applications such as grid-connected photovoltaic systems and energy storage interfaces.

To further evaluate the self-balancing capability of the PUC5 inverter under non-ideal operating conditions, Fig. 11 analyzes the flying capacitor's response to a step change in the DC input voltage from 200 V to 300 V. As expected, the capacitor voltage stabilizes at the new desired value of 150 V (Vdc/2), demonstrating consistent tracking behavior. This result affirms the robustness of the topology's inherent balancing mechanism, which remains effective even under significant variations in the DC supply. Notably, the transition occurs without any observable oscillations or instability, validating the stability and scalability of the proposed control-topology framework for broader input voltage ranges, as typically encountered in photovoltaic or battery-powered systems. Post-transition, the voltage ripple across the capacitor remains within ±2 V, representing approximately 1.5% of the new steady-state value—well within acceptable design limits. This behavior underscores the system's ability to maintain reliable and balanced operation across diverse and dynamic power conditions.

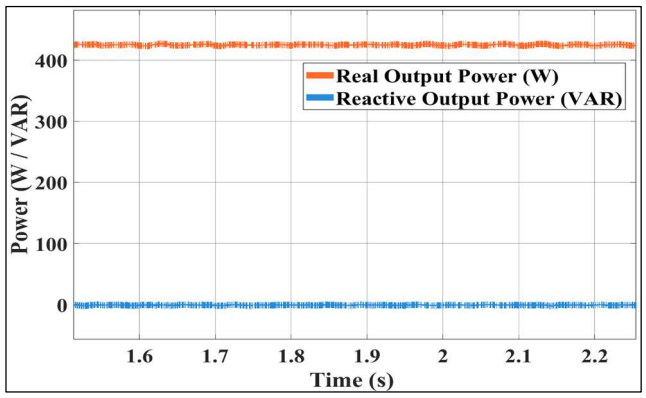

Fig. 8. Active and reactive output power under steady-state operation

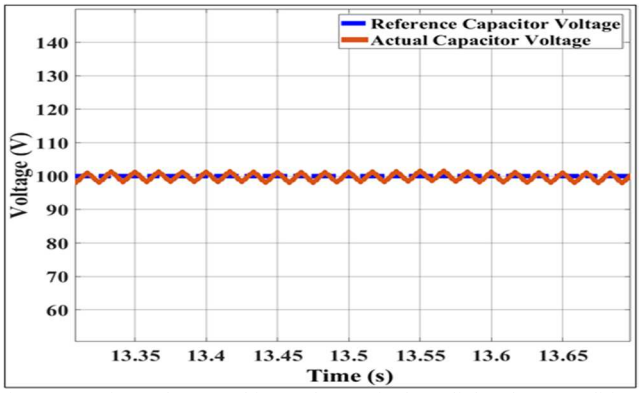

Fig. 9. Capacitor voltage tracking under nominal DC-link voltage conditions (V_{DC} = 200 V)

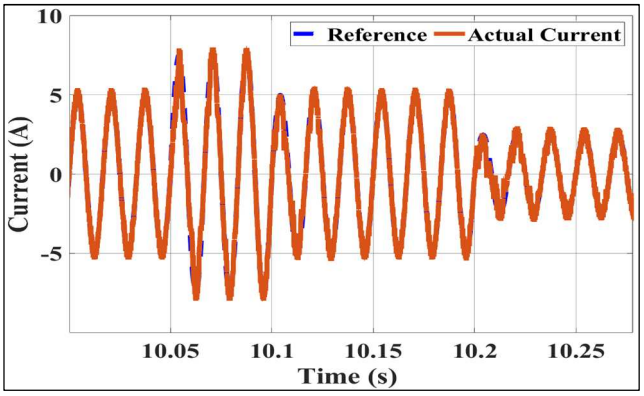

Fig. 10. Dynamic response of the grid current to a step change in the reference

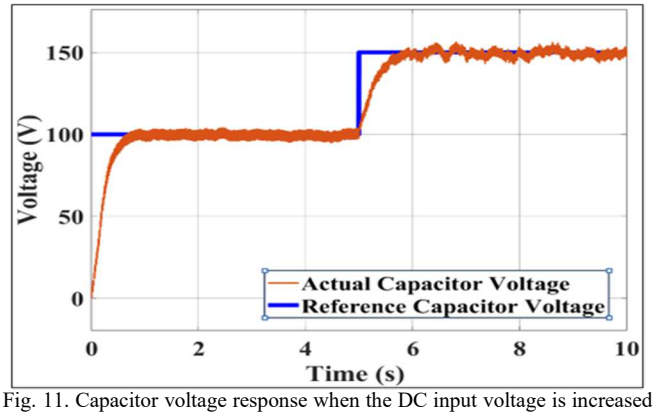

Fig. 11. Capacitor voltage response when the DC input voltage is increased to 300 V

IV. Conclusion

This paper presented a simple dq-frame PI control strategy for a single-phase grid-connected five-level PUC5 inverter. The approach eliminates the need for capacitor voltage sensors or active balancing circuits by leveraging the topology's inherent self-balancing behavior, thereby simplifying hardware and reducing system complexity.

Simulation results demonstrated high-quality current injection with low THD using a basic L-type filter, achieving unity power factor under varying conditions. The flying capacitor maintained a stable voltage around half the DC-link value with minimal ripple across both steady-state and dynamic scenarios.

Overall, the proposed control method offers a reliable, cost-effective solution for renewable energy integration in single-phase applications, meeting grid requirements while avoiding complex control techniques or sensing hardware.

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